TJA1055

Enhanced fault-tolerant CAN transceiver

Rev. 5 — 6 December 2013 Product data sheet

1. General description

The TJA1055 is the interface between the protocol controller and the physical bus wires in a Controller Area Network (CAN). It is primarily intended for low-speed applications up to 125 kBd in passenger cars. The device provides differential receive and transmit capability but will switch to single-wire transmitter and/or receiver in error conditions. The TJA1055 is the enhanced version of the TJA1054 and TJA1054A. TJA1055 has the same functionality but in addition offering a number of improvements. The most important improvements of the TJA1055 with respect to the TJA1054 and TJA1054A are:

- Improved ElectroStatic Discharge (ESD) performance
- Lower current consumption in sleep mode
- Wake-up signalling on RXD and $\overline{\text{ERR}}$ without V_{CC} active
- 3 V interfacing with microcontroller possible with TJA1055T/3

2. Features and benefits

2.1 Optimized for in-car low-speed communication

- Pin-to-pin compatible with TJA1054 and TJA1054A
- Baud rate up to 125 kBd
- Up to 32 nodes can be connected
- Supports unshielded bus wires
- Very low ElectroMagnetic Emission (EME) due to built-in slope control function and a very good matching of the CANL and CANH bus outputs
- Very high ElectroMagnetic Immunity (EMI) in normal operating mode and in low power modes
- Fully integrated receiver filters
- Transmit Data (TxD) dominant time-out function
- High ESD robustness:
  - ±8 kV Electrostatic Discharge (ESD) protection Human Body Model (HBM) for off-board pins
  - ±6 kV Electrostatic Discharge (ESD) protection IEC 61000-4-2 for off-board pins
- Low-voltage microcontroller support

2.2 Bus failure management

- Supports single-wire transmission modes with ground offset voltages up to 1.5 V
- Automatic switching to single-wire mode in the event of bus failures, even when the CANH bus wire is short-circuited to V_{CC}

- Automatic reset to differential mode if bus failure is removed
- Full wake-up capability during failure modes

2.3 Protections

- Bus pins short-circuit safe to battery and to ground
- Thermally protected
- Bus lines protected against transients in an automotive environment
- An unpowered node does not disturb the bus lines
- Microcontroller interface without reverse current paths, if unpowered

2.4 Support for low power modes

- Low current sleep mode and standby mode with wake-up via the bus lines
- Software accessible power-on reset flag

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.75	-	5.25	V
V_{BAT}	battery supply voltage	no time limit	−0.3	-	+40	V
		operating mode	5.0	-	40	V
		load dump	-	-	58	V
I_{BAT}	battery supply current	sleep mode at $V_{RTL} = V_{WAKE} = V_{INH} = V_{BAT}$ = 14 V; T_{amb} = −40 °C to +125 °C	-	25	40	µA
V_{CANH}	voltage on pin CANH	$V_{CC} \geq 0$ V; $V_{BAT} \geq 0$ V; no time limit; with respect to any other pin	−58	-	+58	V
V_{CANL}	voltage on pin CANL	$V_{CC} \geq 0$ V; $V_{BAT} \geq 0$ V; no time limit; with respect to any other pin	−58	-	+58	V
$V_{O(dom)}$	dominant output voltage	V_{TXD} = 0 V; $V_{EN} = V_{CC}$				
	on pin CANH	I_{CANH} = −40 mA	V_{CC} − 1.4	-	-	V
	on pin CANL	I_{CANL} = 40 mA	-	-	1.4	V
$t_{PD(L)}$	propagation delay TXD (LOW) to RXD (LOW)	no failures; $R_{CAN_L} = R_{CAN_H}$ = 125 Ω; $C_{CAN_L} = C_{CAN_H}$ = 1 nF; see Figure 4 to Figure 6	-	-	1.5	µs
T_{vj}	virtual junction temperature	[1]	−40	-	+150	°C

[1] Junction temperature in accordance with *"IEC 60747-1"*. An alternative definition is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$ where $R_{th(vj-a)}$ is a fixed value to be used for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and operating ambient temperature (T_{amb}).

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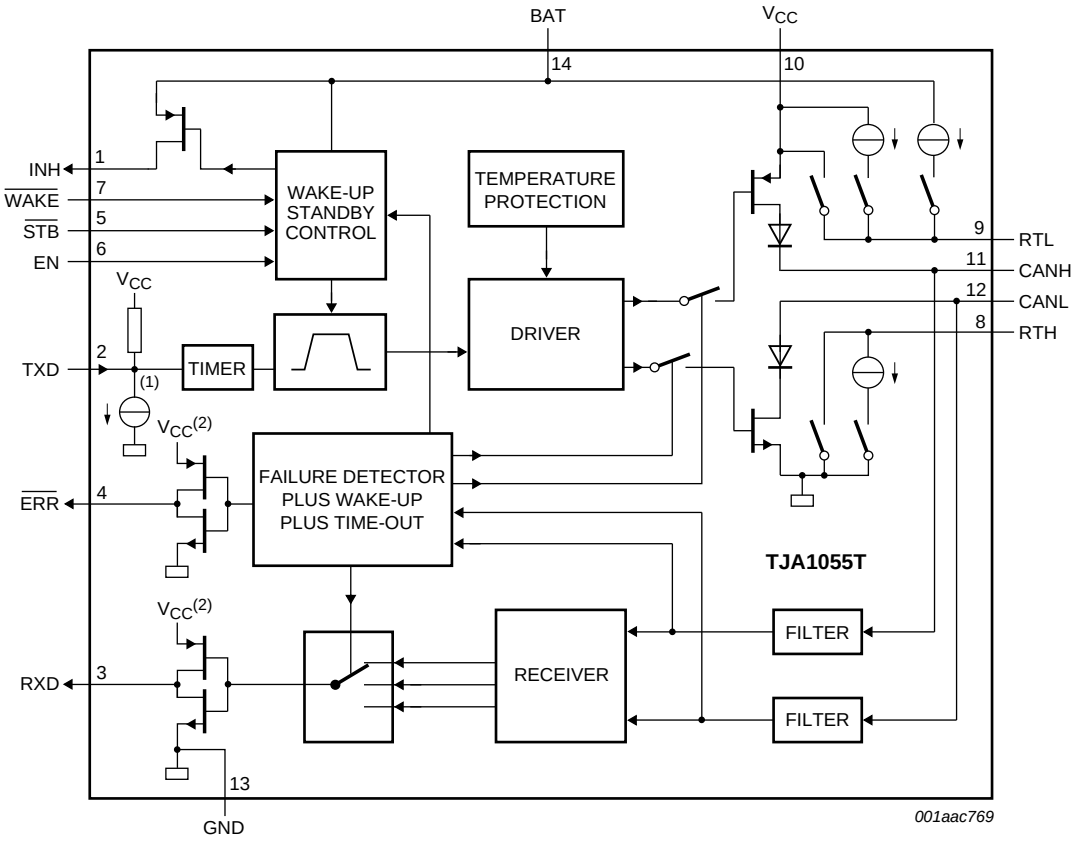
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4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TJA1055T	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
TJA1055T/3			

5. Block diagram



(1) For TJA1055T/3 current source to GND; for TJA1055T pull-up resistor to V_{CC}.

(2) Not within TJA1055T/3.

Fig 1. Block diagram

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6. Pinning information

6.1 Pinning

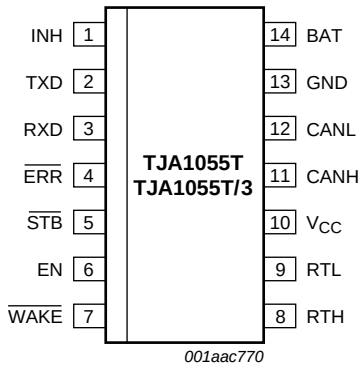


Fig 2. Pin configuration

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
INH	1	inhibit output for switching an external voltage regulator if a wake-up signal occurs
TXD	2	transmit data input for activating the driver to the bus lines
RXD	3	receive data output for reading out the data from the bus lines
$\overline{\text{ERR}}$	4	error, wake-up and power-on indication output; active LOW in normal operating mode when a bus failure is detected; active LOW in standby and sleep mode when a wake-up is detected; active LOW in power-on standby when a V_{BAT} power-on event is detected
$\overline{\text{STB}}$	5	standby digital control signal input; together with the input signal on pin EN this input determines the state of the transceiver; see Table 5 and Figure 3
EN	6	enable digital control signal input; together with the input signal on pin $\overline{\text{STB}}$ this input determines the state of the transceiver; see Table 5 and Figure 3
$\overline{\text{WAKE}}$	7	local wake-up signal input (active LOW); both falling and rising edges are detected
RTH	8	termination resistor connection; in case of a CANH bus wire error the line is terminated with a predefined impedance
RTL	9	termination resistor connection; in case of a CANL bus wire error the line is terminated with a predefined impedance
V_{CC}	10	supply voltage
CANH	11	HIGH-level CAN bus line
CANL	12	LOW-level CAN bus line
GND	13	ground
BAT	14	battery supply voltage

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7. Functional description

The TJA1055 is the interface between the CAN protocol controller and the physical wires of the CAN bus (see Figure 7 and Figure 8). It is primarily intended for low-speed applications, up to 125 kBd, in passenger cars. The device provides differential transmit capability to the CAN bus and differential receive capability to the CAN controller.

To reduce EME, the rise and fall slopes are limited. This allows the use of an unshielded twisted pair or a parallel pair of wires for the bus lines. Moreover, the device supports transmission capability on either bus line if one of the wires is corrupted. The failure detection logic automatically selects a suitable transmission mode.

In normal operating mode (no wiring failures) the differential receiver is output on pin RXD (see Figure 1). The differential receiver inputs are connected to pins CANH and CANL through integrated filters. The filtered input signals are also used for the single-wire receivers. The receivers connected to pins CANH and CANL have threshold voltages that ensure a maximum noise margin in single-wire mode.

A timer function (TxD dominant time-out function) has been integrated to prevent the bus lines from being driven into a permanent dominant state (thus blocking the entire network communication) due to a situation in which pin TXD is permanently forced to a LOW level, caused by a hardware and/or software application failure.

If the duration of the LOW level on pin TXD exceeds a certain time, the transmitter will be disabled. The timer will be reset by a HIGH level on pin TXD.

7.1 Failure detector

The failure detector is fully active in the normal operating mode. After the detection of a single bus failure the detector switches to the appropriate mode (see Table 4). The differential receiver threshold voltage is set at −3.2 V typical (V_{CC} = 5 V). This ensures correct reception with a noise margin as high as possible in the normal operating mode and in the event of failures 1, 2, 5 and 6a. These failures, or recovery from them, do not destroy ongoing transmissions. The output drivers remain active, the termination does not change and the receiver remains in differential mode (see Table 4).

Failures 3, 3a and 6 are detected by comparators connected to the CANH and CANL bus lines. Failures 3 and 3a are detected in a two-step approach. If the CANH bus line exceeds a certain voltage level, the differential comparator signals a continuous dominant condition. Because of inter operability reasons with the predecessor products TJA1054 and TJA1054A, after a first time-out the transceiver switches to single-wire operation through CANH. If the CANH bus line is still exceeding the CANH detection voltage for a second time-out, the TJA1055 switches to CANL operation; the CANH driver is switched off and the RTH bias changes to the pull-down current source. The time-outs (delays) are needed to avoid false triggering by external RF fields.

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Table 4. Bus failures

Failure	Description	Termination CANH (RTH)	Termination CANL (RTL)	CANH driver	CANL driver	Receiver mode
1	CANH wire interrupted	on	on	on	on	differential
2	CANL wire interrupted	on	on	on	on	differential
3	CANH short-circuited to battery	weak[1]	on	off	on	CANL
3a	CANH short-circuited to V_{CC}	weak[1]	on	off	on	CANL
4	CANL short-circuited to ground	on	weak[2]	on	off	CANH
5	CANH short-circuited to ground	on	on	on	on	differential
6	CANL short-circuited to battery	on	weak[2]	on	off	CANH
6a	CANL short-circuited to V_{CC}	on	on	on	on	differential
7	CANL and CANH mutually short-circuited	on	weak[2]	on	off	CANH

[1] A weak termination implies a pull-down current source behavior of 75 μA typical.

[2] A weak termination implies a pull-up current source behavior of 75 μA typical.

Failure 6 is detected if the CANL bus line exceeds its comparator threshold for a certain period of time. This delay is needed to avoid false triggering by external RF fields. After detection of failure 6, the reception is switched to the single-wire mode through CANH; the CANL driver is switched off and the RTL bias changes to the pull-up current source.

Recovery from failures 3, 3a and 6 is detected automatically after reading a consecutive recessive level by corresponding comparators for a certain period of time.

Failures 4 and 7 initially result in a permanent dominant level on pin RXD. After a time-out the CANL driver is switched off and the RTL bias changes to the pull-up current source. Reception continues by switching to the single-wire mode via pins CANH or CANL. When failures 4 or 7 are removed, the recessive bus levels are restored. If the differential voltage remains below the recessive threshold level for a certain period of time, reception and transmission switch back to the differential mode.

If any of the wiring failure occurs, the output signal on pin $\overline{\text{ERR}}$ will be set to LOW. On error recovery, the output signal on pin $\overline{\text{ERR}}$ will be set to HIGH again. In case of an interrupted open bus wire, this failure will be detected and signalled only if there is an open wire between the transmitting and receiving node(s). Thus, during open wire failures, pin $\overline{\text{ERR}}$ typically toggles.

During all single-wire transmissions, EMC performance (both immunity and emission) is worse than in the differential mode. The integrated receiver filters suppress any HF noise induced into the bus wires. The cut-off frequency of these filters is a compromise between propagation delay and HF suppression. In single-wire mode, LF noise cannot be distinguished from the required signal.

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7.2 Low power modes

The transceiver provides three low power modes which can be entered and exited via $\overline{STB}$ and EN (see Table 5 and Figure 3).

The sleep mode is the mode with the lowest power consumption. Pin INH is switched to HIGH-impedance for deactivation of the external voltage regulator. Pin CANL is biased to the battery voltage via pin RTL. Pins RXD and $\overline{ERR}$ will signal the wake-up interrupt even in case V_{CC} is not present.

The standby mode operates in the same way as the sleep mode but with a HIGH level on pin INH.

The power-on standby mode is the same as the standby mode, however, in this mode the battery power-on flag is shown on pin $\overline{ERR}$ instead of the wake-up interrupt signal. The output on pin RXD will show the wake-up interrupt. This mode is only for reading out the power-on flag.

Table 5. Normal operating and low power modes

Mode	Pin $\overline{STB}$	Pin EN	Pin $\overline{ERR}$		Pin RXD		Pin RTL switched to
			LOW	HIGH	LOW	HIGH	
Goto-sleep command	LOW	HIGH	wake-up interrupt signal[1]	[2][3]	wake-up interrupt signal[1]	[2][3]	V_{BAT}
Sleep	LOW	LOW[4]					
Standby	LOW	LOW					
Power-on standby	HIGH	LOW	V_{BAT} power-on flag[5]		wake-up interrupt signal[1]		V_{BAT}
Normal operating	HIGH	HIGH	error flag	no error flag	dominant received data	recessive received data	V_{CC}

[1] Wake-up interrupts are released when entering normal operating mode.

[2] For TJA1055T a diode is added in series with the high-side driver of $\overline{ERR}$ and RXD to prevent a reverse current from $\overline{ERR}$ to V_{CC} in the unpowered state.

[3] For TJA1055T/3, $\overline{ERR}$ and RXD are open-drain.

[4] In case the goto-sleep command was used before. When V_{CC} drops, pin EN will become LOW, but due to the fail-safe functionality this does not effect the internal functions.

[5] V_{BAT} power-on flag will be reset when entering normal operating mode.

Wake-up requests are recognized by the transceiver through two possible channels:

- The bus lines for remote wake-up
- Pin $\overline{WAKE}$ for local wake-up

In order to wake-up the transceiver remotely through the bus lines, a filter mechanism is integrated. This mechanism makes sure that noise and any present bus failure conditions do not result into an erroneous wake-up. Because of this mechanism it is not sufficient to simply pull the CANH or CANL bus lines to a dominant level for a certain time. To guarantee a successful remote wake-up under all conditions, a message frame with a dominant phase of at least the maximum specified $t_{dom(CANH)}$ or $t_{dom(CANL)}$ in it is required.

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A local wake-up through pin $\overline{\text{WAKE}}$ is detected by a rising or falling edge with a consecutive level exceeding the maximum specified t_{WAKE}.

On a wake-up request the transceiver will set the output on pin INH to HIGH which can be used to activate the external supply voltage regulator.

A wake-up request is signalled on $\overline{\text{ERR}}$ or RXD with an active LOW signal. So the external microcontroller can activate the transceiver (switch to normal operating mode) via pins $\overline{\text{STB}}$ and EN.

To prevent a false remote wake-up due to transients or RF fields, the wake-up voltage levels have to be maintained for a certain period of time. In the low power modes the failure detection circuit remains partly active to prevent an increased power consumption in the event of failures 3, 3a, 4 and 7.

To prevent a false local wake-up during an open wire at pin $\overline{\text{WAKE}}$, this pin has a weak pull-up current source towards V_{BAT}. However, in order to protect the transceiver against any EMC immunity issues, it is recommended to connect a not used pin $\overline{\text{WAKE}}$ to pin BAT. Pin INH is set to floating only if the goto-sleep command is entered successfully. To enter a successful goto-sleep command under all conditions, this command must be kept stable for the maximum specified $t_{d(sleep)}$.

Pin INH will be set to a HIGH level again by the following events only:

- V_{BAT} power-on (cold start)
- Rising or falling edge on pin $\overline{\text{WAKE}}$
- A message frame with a dominant phase of at least the maximum specified $t_{dom(CANH)}$ or $t_{dom(CANL)}$, while pin EN or pin $\overline{\text{STB}}$ is at a LOW level
- Pin $\overline{\text{STB}}$ goes to a HIGH level with V_{CC} active

To provide fail-safe functionality, the signals on pins $\overline{\text{STB}}$ and EN will internally be set to LOW when V_{CC} is below a certain threshold voltage ($V_{CC(stb)}$). An unused output pin INH can simply be left open within the application.

7.3 Power-on

After power-on (V_{BAT} switched on) the signal on pin INH will become HIGH and an internal power-on flag will be set. This flag can be read in the power-on standby mode through pin $\overline{\text{ERR}}$ ($\overline{\text{STB}}$ = 1; EN = 0) and will be reset by entering the normal operating mode.

7.4 Protections

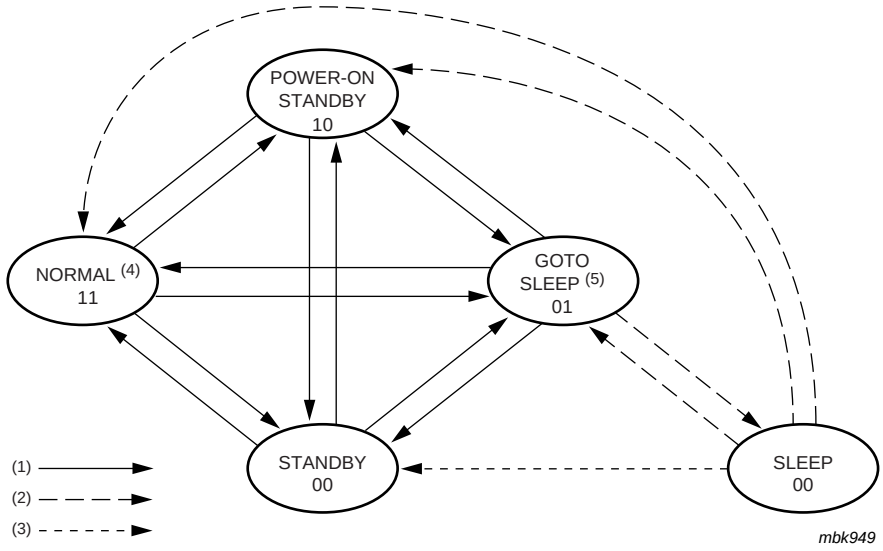
A current limiting circuit protects the transmitter output stages against short-circuit to positive and negative battery voltage.

If the junction temperature exceeds the typical value of 175 °C, the transmitter output stages are disabled. Because the transmitter is responsible for the major part of the power dissipation, this will result in a reduced power dissipation and hence a lower chip temperature. All other parts of the device will continue to operate.

The pins CANH and CANL are protected against electrical transients which may occur in an automotive environment.

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Mode 10 stands for: Pin $\overline{\text{STB}}$ = HIGH and pin EN = LOW.

(1) Mode change via input pins $\overline{\text{STB}}$ and EN.

(2) Mode change via input pins $\overline{\text{STB}}$ and EN; it should be noted that in the sleep mode pin INH is inactive and possibly there is no V_{CC}. Mode control is only possible if V_{CC} of the transceiver is active.

(3) Pin INH is activated and pins RXD and $\overline{\text{ERR}}$ are pulled LOW after wake-up via bus or input pin $\overline{\text{WAKE}}$.

(4) Transitions to normal mode clear the internal wake-up: wake-up interrupt flag and power-on flag are cleared.

(5) Transitions to sleep mode: pin INH is deactivated.

Fig 3. Mode control

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.3	+6	V
V_{BAT}	battery supply voltage		–0.3	+58	V
V_{TXD}	voltage on pin TXD		–0.3	V_{CC} + 0.3	V
V_{RXD}	voltage on pin RXD		–0.3	V_{CC} + 0.3	V
V_{ERR}	voltage on pin $\overline{\text{ERR}}$		–0.3	V_{CC} + 0.3	V
V_{STB}	voltage on pin $\overline{\text{STB}}$		–0.3	V_{CC} + 0.3	V
V_{EN}	voltage on pin EN		–0.3	V_{CC} + 0.3	V
V_{CANH}	voltage on pin CANH	$V_{CC} \geq 0$ V; $V_{BAT} \geq 0$ V; no time limit; with respect to any other pin	–58	+58	V
V_{CANL}	voltage on pin CANL	$V_{CC} \geq 0$ V; $V_{BAT} \geq 0$ V; no time limit; with respect to any other pin	–58	+58	V

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Table 6. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{trt(n)}$	transient voltage on pins CANH and CANL		[2]	−150	+100	V
$V_{I(WAKE)}$	input voltage on pin $\overline{WAKE}$	with respect to any other pin		−0.3	+58	V
$I_{I(WAKE)}$	input current on pin $\overline{WAKE}$		[3]	−15	-	mA
V_{INH}	voltage on pin INH			−0.3	V_{BAT} + 0.3	V
V_{RTH}	voltage on pin RTH	with respect to any other pin		−58	+58	V
V_{RTL}	voltage on pin RTL	with respect to any other pin		−58	+58	V
R_{RTH}	termination resistance on pin RTH			500	16000	Ω
R_{RTL}	termination resistance on pin RTL			500	16000	Ω
T_{vj}	virtual junction temperature		[4]	−40	+150	°C
T_{stg}	storage temperature			−55	+150	°C
V_{esd}	electrostatic discharge voltage	human body model	[5]			
		pins RTH, RTL, CANH and CANL		−8	+8	kV
		all other pins		−2	+2	kV
		IEC 61000-4-2	[6]			
		pins RTH, RTL, CANH and CANL		−6	+6	kV
		machine model	[7]			
		any pin		−300	+300	V

[1] All voltages are defined with respect to pin GND, unless otherwise specified. Positive current flows into the device.

[2] Test set-up according to IEC TS 62228, section 4.2.4. Verified by an external test house to ensure pins can withstand ISO 7637 part 1 & 2 automotive transient test pulses 1, 2a, 3a and 3b.

[3] Only relevant if $V_{WAKE} < V_{GND} - 0.3$ V; current will flow into pin GND.

[4] Junction temperature in accordance with *"IEC 60747-1"*. An alternative definition is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$ where $R_{th(vj-a)}$ is a fixed value to be used for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and operating ambient temperature (T_{amb}).

[5] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.

[6] The ESD performance of pins CANH, CANL, RTH and RTL, with respect to GND, was verified by an external test house in accordance with IEC-61000-4-2 (C = 150 pF, R = 330 Ω). The results were equal to, or better than, ±6 kV.

[7] Equivalent to discharging a 200 pF capacitor through a 10 Ω resistor and a 0.75 μH coil.

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9. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	120	K/W
$R_{th(j-s)}$	thermal resistance from junction to substrate	in free air	40	K/W

10. Static characteristics

Table 8. Static characteristics

V_{CC} = 4.75 V to 5.25 V; V_{BAT} = 5.0 V to 40 V; V_{STB} = V_{CC}; T_{vj} = −40 °C to +150 °C; all voltages are defined with respect to ground; positive currents flow into the device; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies (pins V_{CC} and BAT)						
V_{CC}	supply voltage		4.75	-	5.25	V
$V_{CC(stb)}$	supply voltage for forced standby mode (fail-safe)		3.1	-	4.5	V
I_{CC}	supply current	normal operating mode; V_{TXD} = V_{CC} (recessive)	2.5	6	10	mA
		normal operating mode; V_{TXD} = 0 V (dominant); no load	3	13	21	mA
		low power modes at V_{TXD} = V_{CC}				
		T_{amb} = −40 °C to +85 °C	0	0	5	µA
		T_{amb} = +85 °C to +125 °C	0	0	25	µA
V_{BAT}	battery supply voltage	no time limit	−0.3	-	+40	V
		operating mode	5.0	-	40	V
		load dump	-	-	58	V
I_{BAT}	battery supply current	sleep mode at V_{RTL} = V_{WAKE} = V_{INH} = V_{BAT} = 14 V; T_{amb} = −40 °C to +125 °C	-	25	40	µA
		low power mode at V_{RTL} = V_{WAKE} = V_{INH} = V_{BAT}; T_{amb} = −40 °C to +125 °C				
		V_{BAT} = 5 V to 8 V	10	-	100	µA
		V_{BAT} = 8 V to 40 V	10	-	75	µA
		normal operating mode at V_{RTL} = V_{WAKE} = V_{INH} = V_{BAT} = 5 V to 40 V	-	150	220	µA
$V_{pof(BAT)}$	power-on flag voltage on pin BAT	low power modes				
		power-on flag set	-	-	3.8	V
		power-on flag not set	5	-	-	V
Pins $\overline{STB}$, EN and TXD						
V_{IH}	HIGH-level input voltage		2.2	-	V_{CC} + 0.3	V
V_{IL}	LOW-level input voltage		−0.3	-	+0.8	V

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Table 8. Static characteristics *...continued*

V_{CC} = 4.75 V to 5.25 V; V_{BAT} = 5.0 V to 40 V; V_{STB} = V_{CC}; T_{vj} = −40 °C to +150 °C; all voltages are defined with respect to ground; positive currents flow into the device; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IH}	HIGH-level input current					
	pins $\overline{STB}$ and EN	V_I = 4 V	-	11	21	µA
	pin TXD (TJA1055T)	V_I = 3 V	−160	−80	−40	µA
	pin TXD (TJA1055T/3)	normal operating mode; V_I = 2.4 V	2	11	21	µA
		low power mode; V_I = 2.4 V	0.1	0.9	2	µA
I_{IL}	LOW-level input current					
	pins $\overline{STB}$ and EN	V_I = 1 V	2	11	-	µA
	pin TXD (TJA1055T)	V_I = 1 V	−400	−240	−100	µA
	pin TXD (TJA1055T/3)	normal operating mode; V_I = 1 V	2	11	-	µA
		low power mode; V_I = 1 V	0.1	0.9	2	µA
Pins RXD and $\overline{ERR}$ (TJA1055T)						
$V_{OH(norm)}$	HIGH-level output voltage in normal mode					
	on pin $\overline{ERR}$	I_O = −100 µA	V_{CC} − 0.9	-	V_{CC}	V
	on pin RXD	I_O = −1 mA	V_{CC} − 0.9	-	V_{CC}	V
$V_{OH(lp)}$	HIGH-level output voltage in low-power mode					
	on pin $\overline{ERR}$	I_O = −100 µA	V_{CC} − 1.1	V_{CC} − 0.7	V_{CC} − 0.4	V
	on pin RXD	I_O = −100 µA	V_{CC} − 1.1	V_{CC} − 0.7	V_{CC} − 0.4	V
V_{OL}	LOW-level output voltage	I_O = 1.6 mA	0	-	0.4	V
		I_O = 1.2 mA; V_{CC} < 4.75 V	0	-	0.4	V
		I_O = 5 mA	0	-	1.5	V
Pins RXD and $\overline{ERR}$ (TJA1055T/3)						
I_{OL}	LOW-level output current	V_O = 0.4 V	1.3	3.5	-	mA
I_{LH}	HIGH-level leakage current	V_O = 3 V	−5	0	+8	µA
Pin $\overline{WAKE}$						
I_{IL}	LOW-level input current	V_{WAKE} = 0 V; V_{BAT} = 40 V	−12	−4	−1	µA
$V_{th(wake)}$	wake-up threshold voltage	V_{STB} = 0 V	2.5	3.2	3.9	V
Pin INH						
ΔV_H	HIGH-level voltage drop	I_{INH} = −0.18 mA; $V_{BAT} \geq$ 5.5 V	-	-	0.8	V
		I_{INH} = −0.18 mA; V_{BAT} = 5.0 V	-	-	1.0	V
$\lvert I_L \rvert$	leakage current	sleep mode; V_{INH} = 0 V	-	-	5	µA
Pins CANH and CANL						
$V_{th(dif)}$	differential receiver threshold voltage	no failures and bus failures 1, 2, 5 and 6a; see Figure 4				
		V_{CC} = 5 V	−3.5	−3.2	−2.9	V
		V_{CC} = 4.75 V to 5.25 V	$-0.70V_{CC}$	$-0.64V_{CC}$	$-0.58V_{CC}$	V

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Table 8. Static characteristics *...continued*

V_{CC} = 4.75 V to 5.25 V; V_{BAT} = 5.0 V to 40 V; V_{STB} = V_{CC}; T_{vj} = −40 °C to +150 °C; all voltages are defined with respect to ground; positive currents flow into the device; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{O(reces)}$	recessive output voltage	V_{TXD} = V_{CC}				
	on pin CANH	R_{RTH} < 4 kΩ	-	-	0.2	V
	on pin CANL	R_{RTL} < 4 kΩ	V_{CC} − 0.2	-	-	V
$V_{O(dom)}$	dominant output voltage	V_{TXD} = 0 V; V_{EN} = V_{CC}				
	on pin CANH	I_{CANH} = −40 mA	V_{CC} − 1.4	-	-	V
	on pin CANL	I_{CANL} = 40 mA	-	-	1.4	V
$I_{O(CANH)}$	output current on pin CANH	normal operating mode; V_{CANH} = 0 V; V_{TXD} = 0 V	−110	−80	−45	mA
		low power modes; V_{CANH} = 0 V; V_{CC} = 5 V	-	−0.25	-	μA
$I_{O(CANL)}$	output current on pin CANL	normal operating mode; V_{CANL} = 14 V; V_{TXD} = 0 V	45	70	100	mA
		low power modes; V_{CANL} = 14 V; V_{BAT} = 14 V	-	0	-	μA
$V_{det(sc)(CANH)}$	detection voltage for short-circuit to battery voltage on pin CANH	normal operating mode; V_{CC} = 5 V	1.5	1.7	1.85	V
		low power modes	1.1	1.8	2.5	V
$V_{det(sc)(CANL)}$	detection voltage for short-circuit to battery voltage on pin CANL	normal operating mode				
		V_{CC} = 5 V	6.6	7.2	7.8	V
		V_{CC} = 4.75 V to 5.25 V	1.32V_{CC}	1.44V_{CC}	1.56V_{CC}	V
$V_{th(wake)}$	wake-up threshold voltage					
	on pin CANL	low power modes	2.5	3.2	3.9	V
	on pin CANH	low power modes	1.1	1.8	2.5	V
$\Delta V_{th(wake)}$	difference of wake-up threshold voltages (on pins CANL and CANH)	low power modes	0.8	1.4	-	V
$V_{th(se)(CANH)}$	single-ended receiver threshold voltage on pin CANH	normal operating mode and failures 4, 6 and 7				
		V_{CC} = 5 V	1.5	1.7	1.85	V
		V_{CC} = 4.75 V to 5.25 V	0.30V_{CC}	0.34V_{CC}	0.37V_{CC}	V
$V_{th(se)(CANL)}$	single-ended receiver threshold voltage on pin CANL	normal operating mode and failures 3 and 3a				
		V_{CC} = 5 V	3.15	3.3	3.45	V
		V_{CC} = 4.75 V to 5.25 V	0.63V_{CC}	0.66V_{CC}	0.69V_{CC}	V
$R_{i(se)(CANH)}$	single-ended input resistance on pin CANH	normal operating mode	110	165	270	kΩ
$R_{i(se)(CANL)}$	single-ended input resistance on pin CANL	normal operating mode	110	165	270	kΩ
$R_{i(dif)}$	differential input resistance	normal operating mode	220	330	540	kΩ

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Table 8. Static characteristics *...continued*

V_{CC} = 4.75 V to 5.25 V; V_{BAT} = 5.0 V to 40 V; V_{STB} = V_{CC}; T_{vj} = −40 °C to +150 °C; all voltages are defined with respect to ground; positive currents flow into the device; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pins RTH and RTL						
$R_{sw(RTL)}$	switch-on resistance on pin RTL	normal operating mode; switch-on resistance between pin RTL and V_{CC}; $\|I_O\|$ < 10 mA	-	40	100	Ω
$R_{sw(RTH)}$	switch-on resistance on pin RTH	normal operating mode; switch-on resistance between pin RTH and ground; $\|I_O\|$ < 10 mA	-	40	100	Ω
$V_{O(RTH)}$	output voltage on pin RTH	low power modes; I_O = 100 µA	-	0.7	1.0	V
$I_{O(RTL)}$	output current on pin RTL	low power modes; V_{RTL} = 0 V	−1.5	−0.65	−0.1	mA
$I_{pu(RTL)}$	pull-up current on pin RTL	normal operating mode and failures 4, 6 and 7	-	75	-	µA
$I_{pd(RTH)}$	pull-down current on pin RTH	normal operating mode and failures 3 and 3a	-	75	-	µA
Thermal shutdown						
$T_{j(sd)}$	shutdown junction temperature		160	175	190	°C

[1] All parameters are guaranteed over the virtual junction temperature range by design, but only 100 % tested at T_{amb} = 125 °C for dies on wafer level, and above this for cased products 100 % tested at T_{amb} = 25 °C, unless otherwise specified.

11. Dynamic characteristics

Table 9. Dynamic characteristics

V_{CC} = 4.75 V to 5.25 V; V_{BAT} = 5.0 V to 40 V; V_{STB} = V_{CC}; T_{vj} = −40 °C to +150 °C; R_{CAN_L} = R_{CAN_H} = 125 Ω; C_{CAN_L} = C_{CAN_H} = 1 nF*; all voltages are defined with respect to ground; unless otherwise specified.*[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{t(reces-dom)}$	transition time for recessive to dominant (on pins CANL and CANH)	between 10 % and 90 %; see Figure 5 and 6	0.2	-	-	µs
$t_{t(dom-reces)}$	transition time for dominant to recessive (on pins CANL and CANH)	between 10 % and 90 %; see Figure 5 and 6	0.2	-	-	µs
$t_{PD(L)}$	propagation delay TXD (LOW) to RXD (LOW)	no failures; see Figure 4 to Figure 6	-	-	1.5	µs
		all failures except CAN_L shorted to CAN_H; see Figure 4 to Figure 6	-	-	1.9	µs
		failure 7, CAN_L shorted to CAN_H; R_{CAN_L} = 1 MΩ; see Figure 4 to Figure 6	-	-	1.9	µs
$t_{PD(H)}$	propagation delay TXD (HIGH) to RXD (HIGH)	no failures; see Figure 4 to Figure 6	-	-	1.5	µs
		all failures except CAN_L shorted to CAN_H; see Figure 4 to Figure 6	-	-	1.9	µs
		failure 7, CAN_L shorted to CAN_H; R_{CAN_L} = 1 MΩ; see Figure 4 to Figure 6	-	-	1.9	µs
$t_{d(sleep)}$	delay time to sleep	[2]	5	-	50	µs
$t_{dis(TxD)}$	disable time of TxD permanent dominant timer	normal operating mode; V_{TXD} = 0 V	0.75	-	4	ms

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Table 9. Dynamic characteristics *...continued*

V_{CC} = 4.75 V to 5.25 V; V_{BAT} = 5.0 V to 40 V; V_{STB} = V_{CC}; T_{vj} = −40 °C to +150 °C; R_{CAN_L} = R_{CAN_H} = 125 Ω; C_{CAN_L} = C_{CAN_H} = 1 nF*; all voltages are defined with respect to ground; unless otherwise specified.* [1]

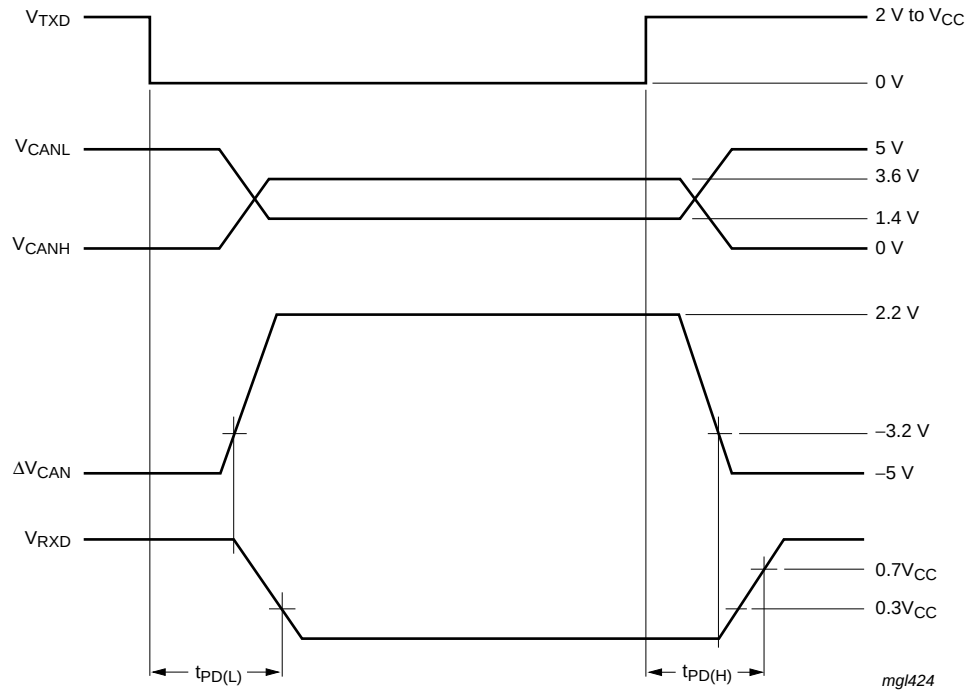
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{dom(CANH)}$	dominant time on pin CANH	low power modes; V_{BAT} = 14 V	[2]	7	-	38	µs
$t_{dom(CANL)}$	dominant time on pin CANL	low power modes; V_{BAT} = 14 V	[2]	7	-	38	µs
t_{WAKE}	local wake-up time on pin $\overline{WAKE}$	low power modes; V_{BAT} = 14 V; for wake-up after receiving a falling or rising edge	[2]	7	-	38	µs
t_{det}	failure detection time	normal operating mode					
		failures 3 and 3a		1.6	-	8.0	ms
		failures 4, 6 and 7		0.3	-	1.6	ms
		low power modes; V_{BAT} = 14 V					
		failures 3 and 3a		1.6	-	8.0	ms
		failures 4 and 7		0.1	-	1.6	ms
t_{rec}	failure recovery time	normal operating mode					
		failures 3 and 3a		0.3	-	1.6	ms
		failures 4 and 7		7	-	38	µs
		failure 6		125	-	750	µs
		low power modes; V_{BAT} = 14 V					
		failures 3, 3a, 4 and 7		0.3	-	1.6	ms
n_{det}	pulse-count failure detection	difference between CANH and CANL; normal operating mode and failures 1, 2, 5 and 6a; pin $\overline{ERR}$ becomes LOW		-	4	-	
n_{rec}	number of consecutive pulses for failure recovery	on CANH and CANL simultaneously; failures 1, 2, 5 and 6a		-	4	-	

[1] All parameters are guaranteed over the virtual junction temperature range by design, but only 100 % tested at T_{amb} = 125 °C for dies on wafer level, and above this for cased products 100 % tested at T_{amb} = 25 °C, unless otherwise specified.

[2] To guarantee a successful mode transition under all conditions, the maximum specified time must be applied.

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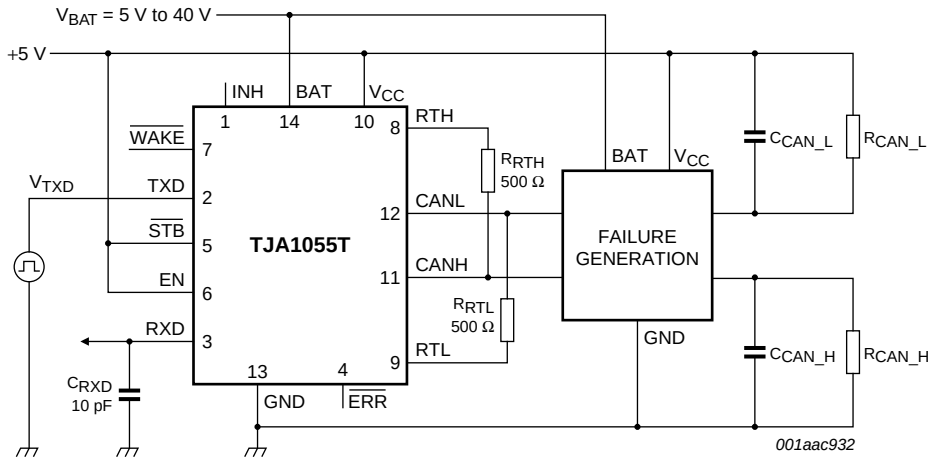
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$\Delta V_{CAN} = V_{CANH} - V_{CANL}$

Fig 4. Timing diagram for dynamic characteristics

12. Test information



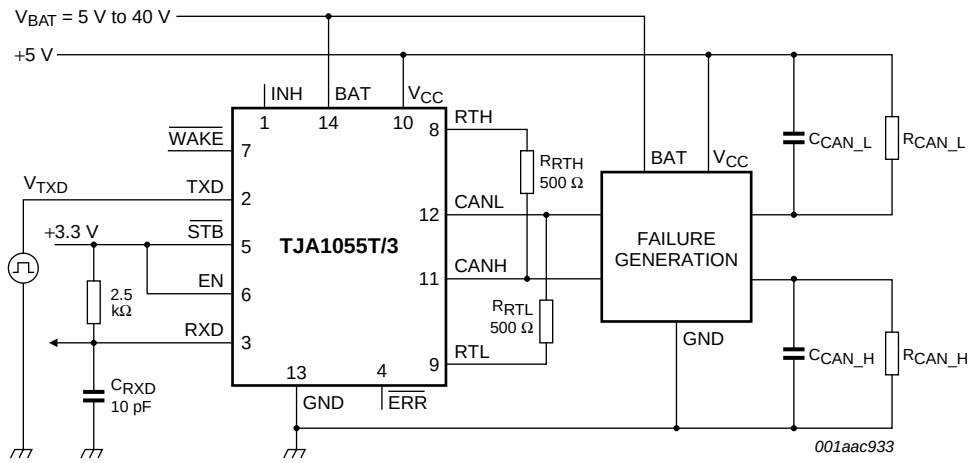
V_{TXD} is a rectangular signal of 50 kHz with 50 % duty cycle and slope time < 10 ns.

Termination resistors R_{CAN_L} and R_{CAN_H} (125 Ω) are not connected to pin RTL or pin RTH for testing purposes because the minimum load allowed on the CAN bus lines is 500 Ω per transceiver.

Fig 5. Test circuit for dynamic characteristics

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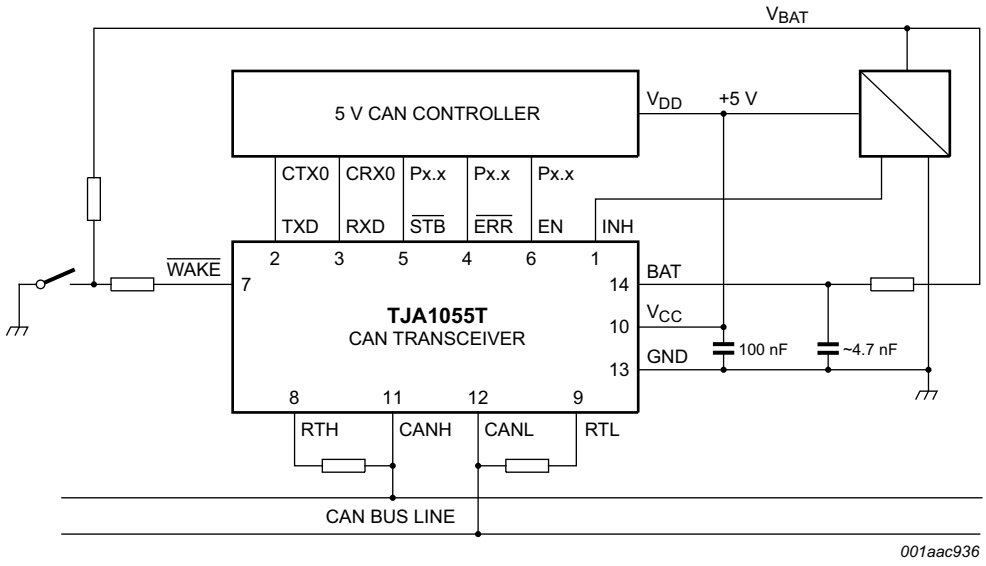
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V_{TXD} is a rectangular signal of 50 kHz with 50 % duty cycle and slope time < 10 ns.

Termination resistors R_{CAN_L} and R_{CAN_H} (125 Ω) are not connected to pin RTL or pin RTH for testing purposes because the minimum load allowed on the CAN bus lines is 500 Ω per transceiver.

Fig 6. Test circuit for dynamic characteristics (TJA1055T/3)

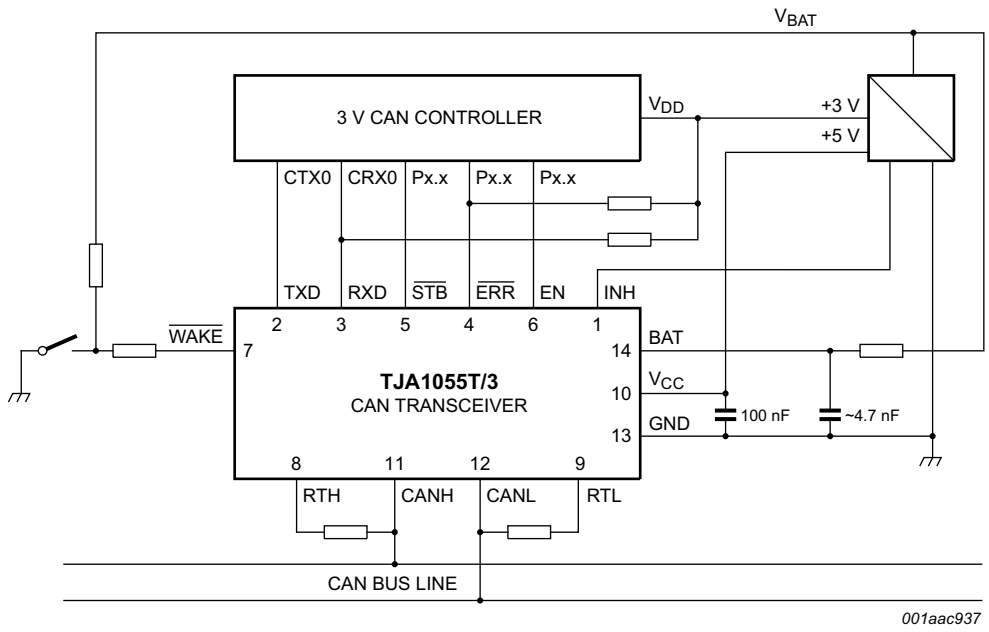


For more information: refer to the separate FTCAN information available on our web site.

Fig 7. Application diagram

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For more information: refer to the separate FTCAN information available on our web site.

Fig 8. Application diagram (TJA1055T/3)

12.1 Quality information

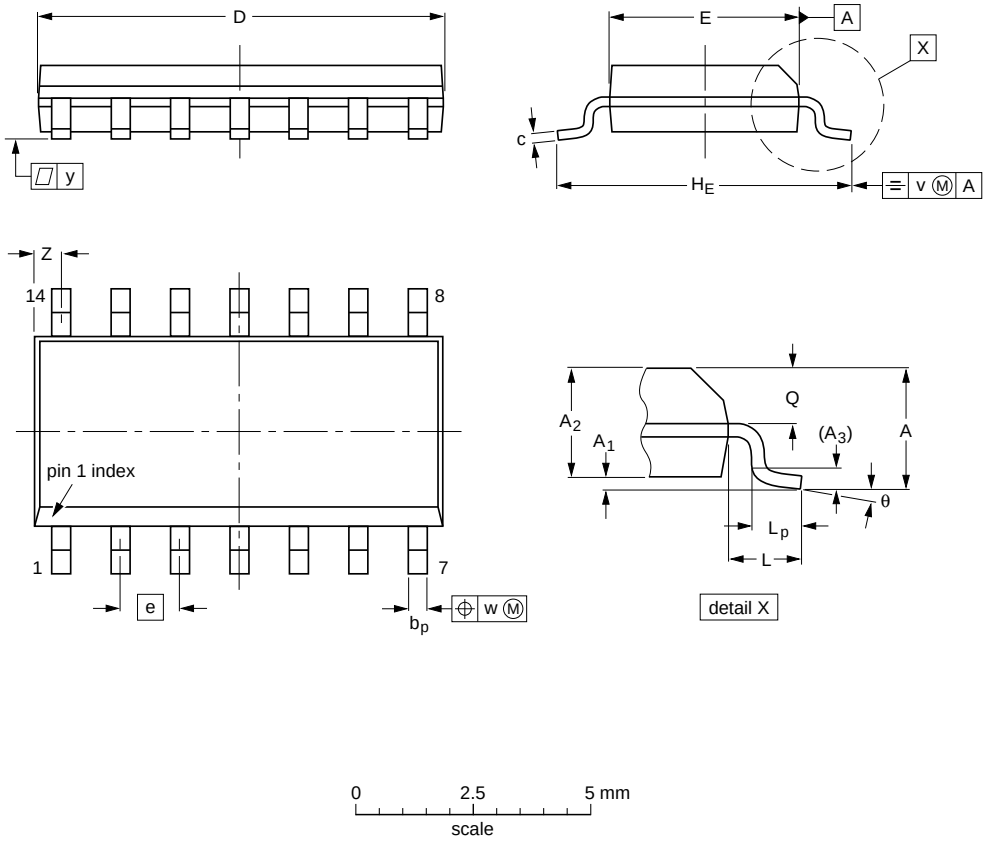
This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 Rev-G - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

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13. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT108-1 (SO14)

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14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 10) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 10 and 11

Table 10. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 11. Lead-free process (from J-STD-020D)

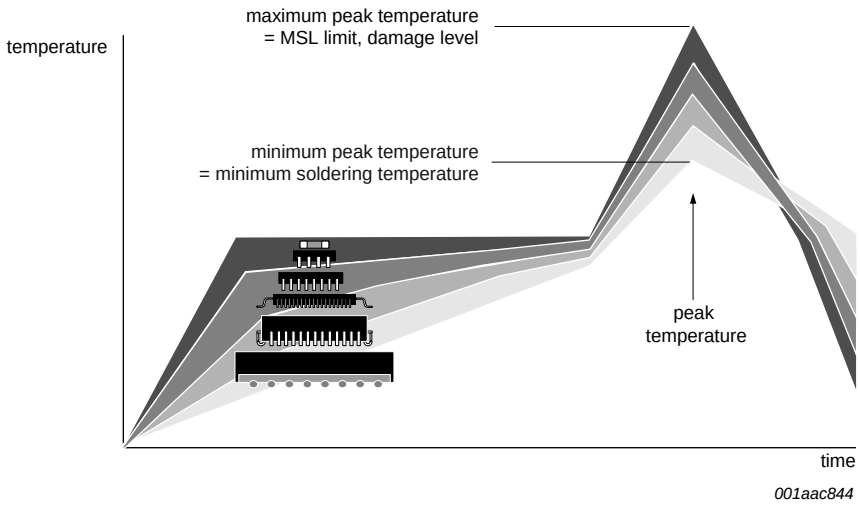
Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 10.

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MSL: Moisture Sensitivity Level

Fig 10. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

15. Appendix

15.1 Overview of differences between the TJA1055 and the TJA1054A

Table 12. Limiting values

Symbol	Parameter	Conditions	TJA1055		TJA1054A		Unit
			Min	Max	Min	Max	
V_{CANH}	voltage on pin CANH		–58	+58	–27	+40	V
V_{CANL}	voltage on pin CANL		–58	+58	–27	+40	V
V_{esd}	electrostatic discharge voltage	pins RTH, RTL, CANH, CANL					
		human body model	–8	+8	–4	+4	kV
		IEC 61000-4-2 [1]					

[1] The ESD performance of pins CANH, CANL, RTH and RTL, with respect to GND, was verified by an external test house in accordance with IEC-61000-4-2 (C = 150 pF, R = 330 Ω). The results were equal to, or better than, ±6 kV for TJA1055 and equal to, or better than, ±1.5 kV for TJA1054A.

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16. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1055 v.5	20131206	Product data sheet	-	TJA1055 v.4
Modifications:	• Template and legal information (Section 17) updated • Table 1, Table 6: measurement conditions changed for parameters V_{CANH} and V_{CANL} • Table 6, Table note 2 added; Fig. 7 and Fig. 8 deleted • Table 8: parameter $I_{sup(tot)}$ deleted; parameter values changed: V_{IH} for pins $\overline{STB}$, EN and TXD; ΔV_H for pin INH • Table 9: parameter values changed: $t_{t(reces-dom)}$, $t_{t(dom-reces)}$; table reformatted • Figure 7, Figure 8: revised (capacitor added) • Section 12.1: text revised			
TJA1055 v.4	20090217	Product data sheet	-	TJA1055 v.3
TJA1055 v.3	20070313	Product data sheet	-	TJA1055 v.2
TJA1055 v.2	20061030	Preliminary data sheet	-	TJA1055 v.1
TJA1055 v.1 (9397 750 14908)	20060801	Objective data sheet	-	-

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17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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