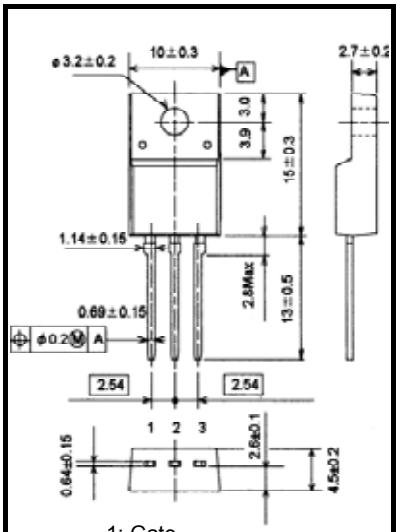
TOSHIBA Field Effect Transistor Silicon N-Channel MOS Type (U-MOSⅣ)

TK8A10K3

Swiching Regulator Applications

- Low drain-source ON resistance: $R_{DS\ (ON)}$ = 90 mΩ (typ.)
- Low leakage current: I_{DSS} = 10 μA (max) (V_{DS} = 100 V)
- Enhancement-model: V_{th} = 2.0 to 4.0 V (V_{DS} = 10 V, I_D = 1.0 mA)

Unit: mm



1: Gate
2: Drain
3: Source

JEDEC	―
JEITA	SC-67
TOSHIBA	2-10U1B

Weight: 1.7 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	100	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	100	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	DC (Note 1)	I_D	8	A
	Pulse (Note 1)	I_{DP}	16	
Drain power dissipation (Tc = 25°C)		P_D	18	W
Single pulse avalanche energy (Note 2)		E_{AS}	4	mJ
Avalanche current		I_{AR}	8	A
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

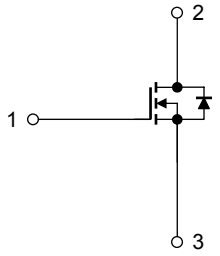
Note : Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Please use devices on condition that the channel temperature is below 150°C.

Note 2: V_{DD} = 25 V, T_{ch} = 25°C, L = 100 μH, R_G = 25 Ω, I_{AR} = 8 A

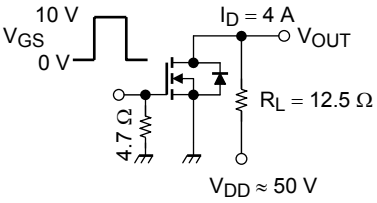
Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch-c)}$	6.94	°C / W
Thermal resistance, channel to ambient	$R_{th\ (ch-a)}$	62.5	°C / W



This transistor is an electrostatic sensitive device. Please handle with caution.

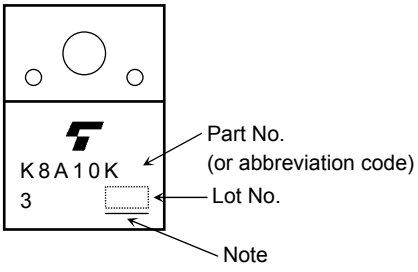
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	—	—	±100	nA
Drain cut-OFF current		I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V	—	—	10	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	100	—	—	V
		$V_{(BR)\ DSX}$	I_D = 10 mA, V_{GS} = −20 V	65	—	—	
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1.0 mA	2.0	—	4.0	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 10 V, I_D = 4 A	—	90	120	mΩ
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 4 A	3.6	7.2	—	S
Input capacitance		C_{iss}	V_{DS} = 10V, V_{GS} = 0 V, f = 1 MHz	—	530	—	pF
Reverse transfer capacitance		C_{rss}		—	55	—	
Output capacitance		C_{oss}		—	75	—	
Switching time	Rise time	t_r	 Duty ≤ 1%, t_w = 10 μs	—	15	—	ns
	Turn-ON time	t_{on}		—	25	—	
	Fall time	t_f		—	5.4	—	
	Turn-OFF time	t_{off}		—	27	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≈ 80 V, V_{GS} = 10 V, I_D = 8 A	—	12.9	—	nC
Gate-source charge		Q_{gs1}		—	5.4	—	
Gate-drain (“miller”) charge		Q_{gd}		—	6.4	—	

Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	8	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	16	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 8 A, V_{GS} = 0 V	—	—	−1.4	V
Reverse recovery time	t_{rr}	I_{DR} = 8 A, V_{GS} = 0 V,	—	50	—	ns
Reverse recovery charge	Q_{rr}	dI_{DR}/dt = 50 A/μs	—	50	—	nC

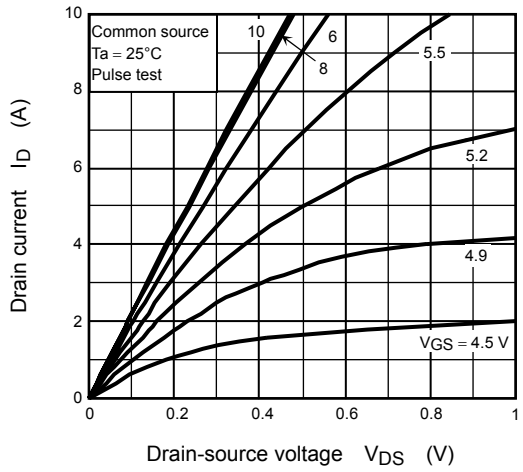
Marking



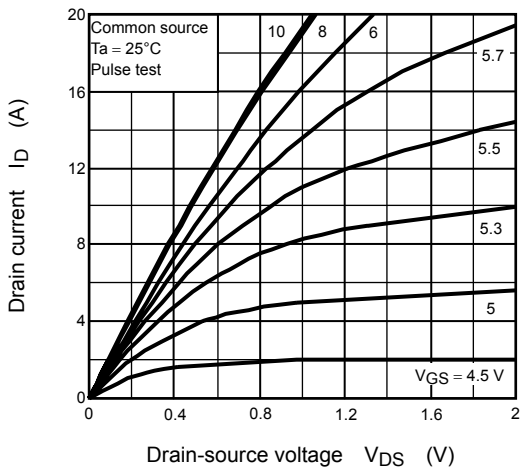
Note : A line under a Lot No. identifies the indication of product Labels
[[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. The RoHS is Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

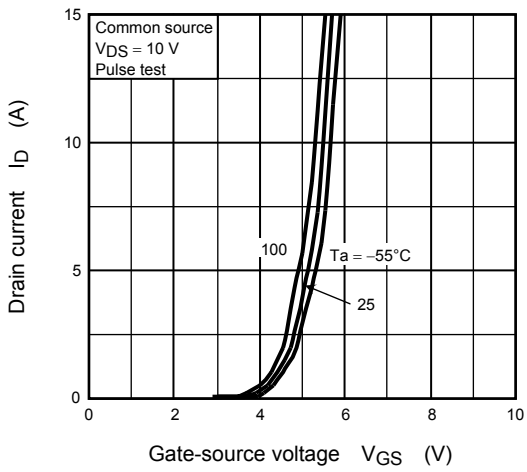
$I_D - V_{DS}$



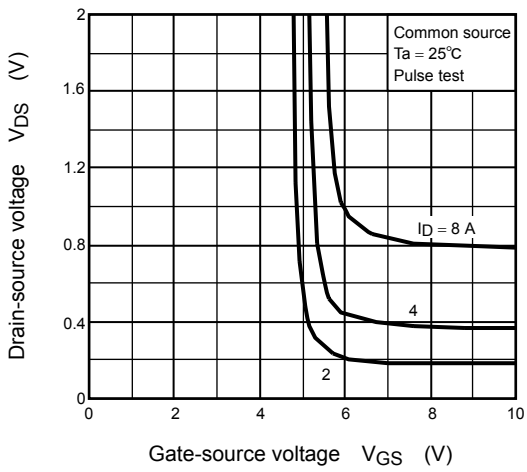
$I_D - V_{DS}$



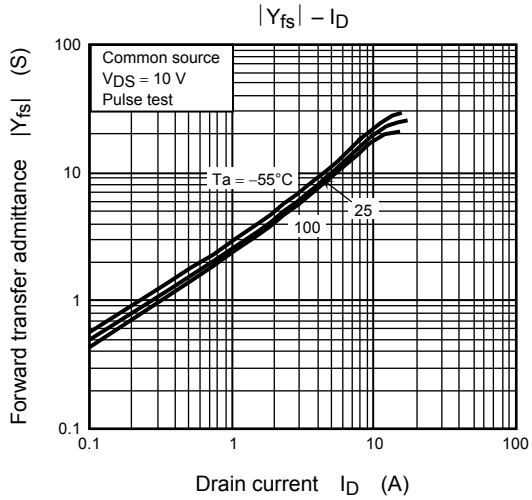
$I_D - V_{GS}$



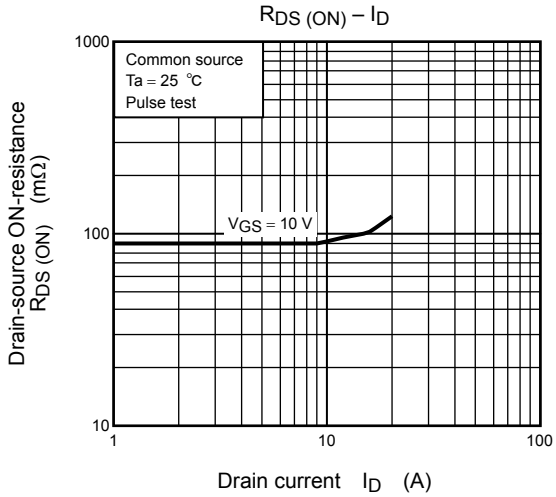
$V_{DS} - V_{GS}$



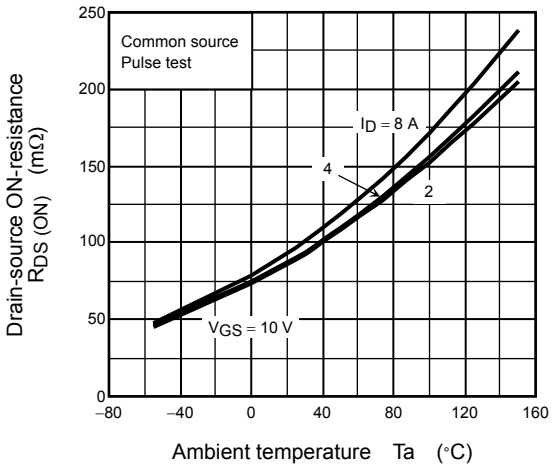
$|Y_{fs}| - I_D$



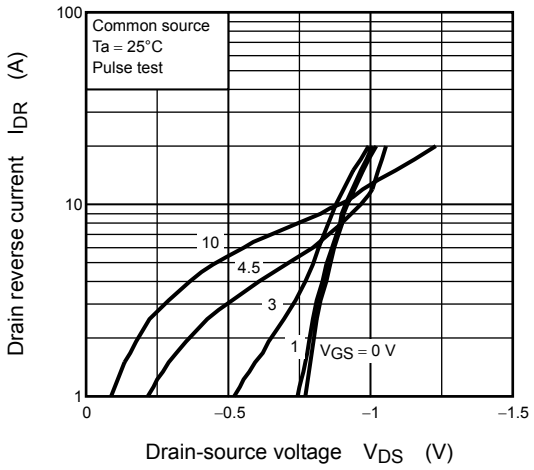
$R_{DS\ (ON)} - I_D$



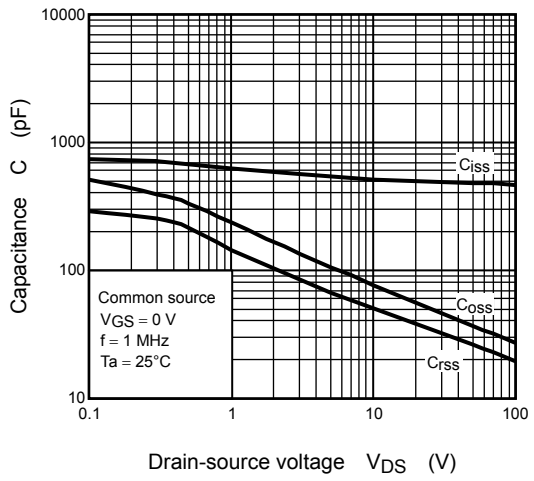
$R_{DS\ (ON)}$ – Ta



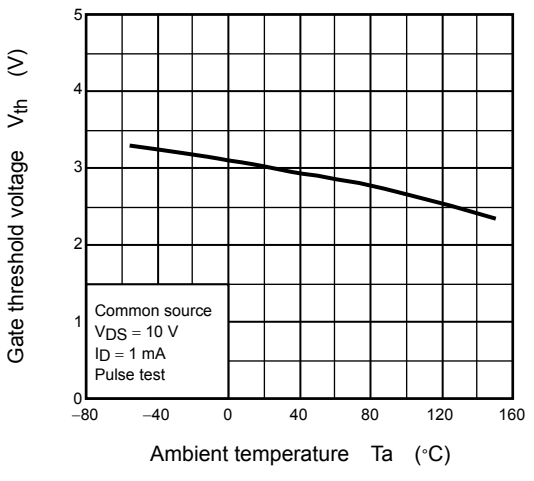
I_{DR} – V_{DS}



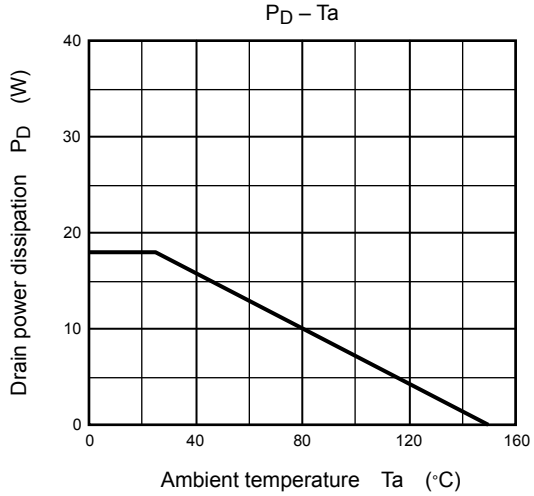
Capacitance – V_{DS}



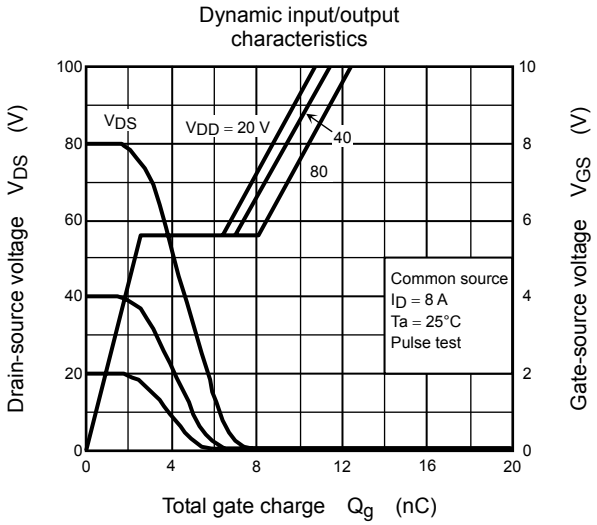
V_{th} – Ta



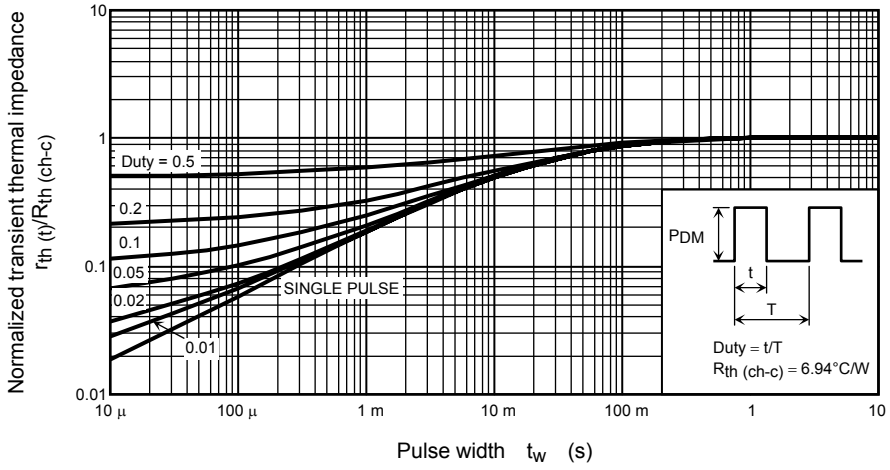
P_D – Ta



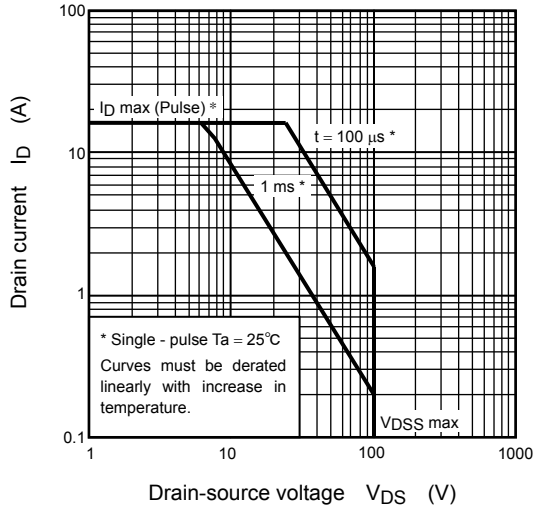
Dynamic input/output characteristics



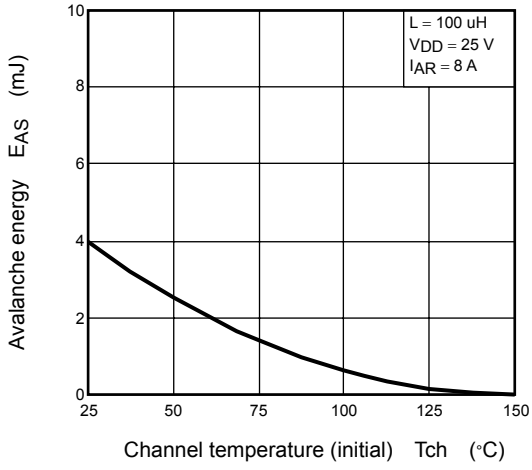
r_{th} /$R_{th\ (ch\text{-}c)}$ – t_w

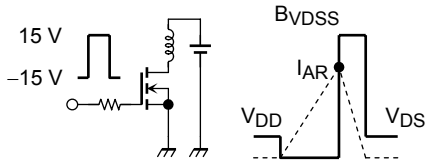


Safe operating area



E_{AS} – Ta





Test circuit Wave form

$R_G = 25\ \Omega$
$V_{DD} = 25$ V, L = 100 μH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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