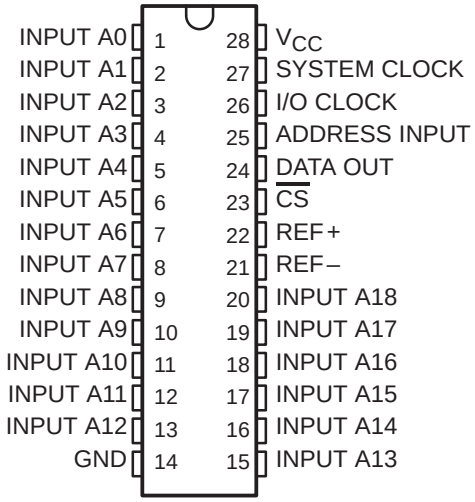
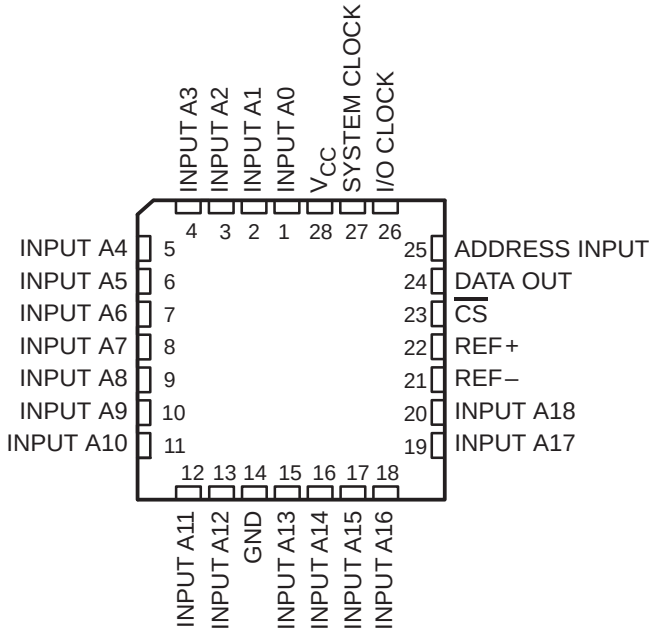
- **8-Bit Resolution A/D Converter**
- **Microprocessor Peripheral or Stand-Alone Operation**
- **On-Chip 20-Channel Analog Multiplexer**
- **Built-in Self-Test Mode**
- **Software-Controllable Sample and Hold**
- **Total Unadjusted Error . . . ±0.5 LSB Max**
- **Timing and Control Signals Compatible With 8-Bit TLC540 and 10-Bit TLC1540 A/D Converter Families**
- **CMOS Technology**

PARAMETER	TL545	TL546
Channel Acquisition Time	1.5 µs	2.7 µs
Conversion Time (Max)	9 µs	17 µs
Sampling Rate (Max)	76 x 10^3	40 x 10^3
Power Dissipation (Max)	15 mW	15 mW

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The TLC545 and TLC546 are CMOS analog-to-digital converters built around an 8-bit switched capacitor successive-approximation analog-to-digital converter. They are designed for serial interface to a microprocessor or peripheral via a 3-state output with up to four control inputs including independent SYSTEM CLOCK, I/O CLOCK, chip select ($\overline{CS}$), and ADDRESS INPUT. A 4-MHz system clock for the TLC545 and a 2.1-MHz system clock for the TLC546 with a design that includes simultaneous read/write operation allowing high-speed data transfers and sample rates of up to 76,923 samples per second for the TLC545, and 40,000 samples per second for the TLC546.

In addition to the high-speed converter and versatile control logic, there is an on-chip 20-channel analog multiplexer that can be used to sample any one of 19 inputs or an internal self-test voltage, and a sample-and-hold that can operate automatically or under microprocessor control.

The converters incorporated in the TLC545 and TLC546 feature differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A totally switched capacitor design allows low-error (±0.5 LSB) conversion in 9 µs for the TLC545, and 17 µs for the TLC546, over the full operating temperature range.

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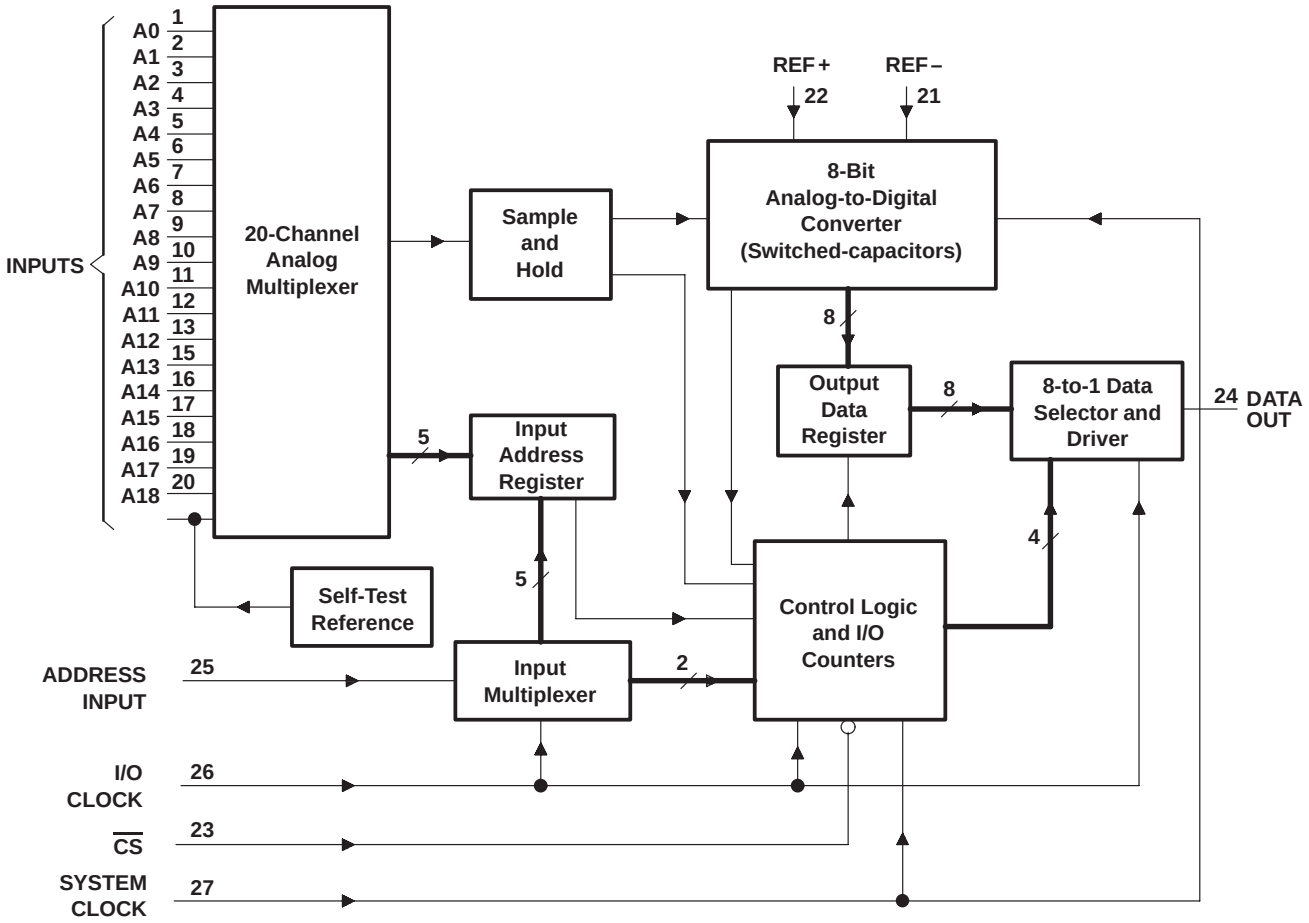
AVAILABLE OPTIONS

T_A	PACKAGE	
	CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	TLC545CFN —	TLC545CN —
–40°C to 85°C	TLC545IFN TLC546IFN	TLC545IN TLC546IN

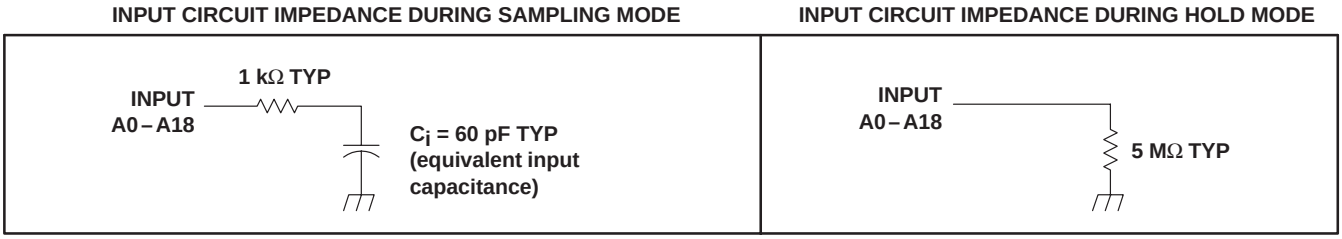
description (continued)

The TLC545C and the TLC546C are characterized for operation from 0°C to 70°C. The TLC545I and the TLC546I are characterized for operation from –40°C to 85°C.

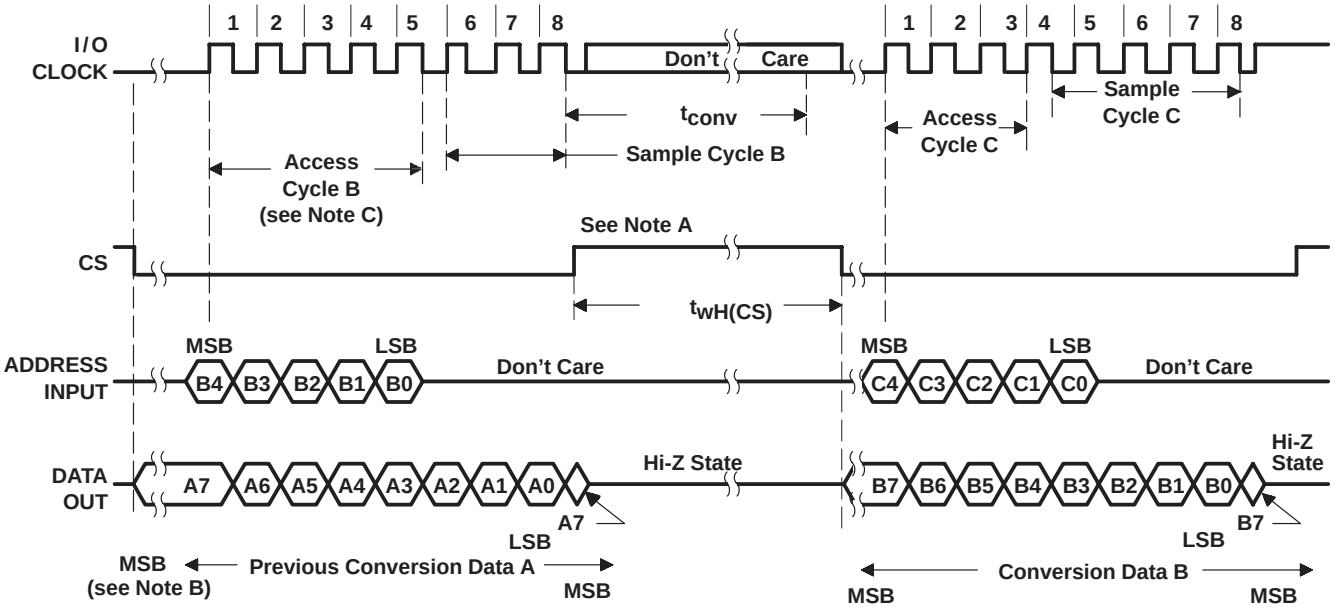
functional block diagram



typical equivalent inputs



operating sequence



NOTES: A. The conversion cycle, which requires 36 system clock periods, is initiated with the eighth I/O CLOCK↓ after $\overline{CS}$↓ for the channel whose address exists in memory at that time.

B. The most significant bit (MSB) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining seven bits (A6–A0) will be clocked out on the first seven I/O CLOCK falling edges.

C. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for three system clock cycles (or less) after a chip select transition before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip-select setup time has elapsed.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range, V_I (any input) . . . . . –0.3 V to V_{CC} +0.3 V
Output voltage range, V_O . . . . . –0.3 V to V_{CC} +0.3 V
Peak input current range (any input) . . . . . ±10 mA
Peak total input current (all inputs) . . . . . ±30 mA
Operating free-air temperature range, T_A: TLC545C, TLC546C . . . . . 0°C to 70°C
TLC545I, TLC546I . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Case temperature for 10 seconds, T_C: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

			TLC545			TLC546			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.75	5	5.5	4.75	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 2)			0	V_{CC}	V_{CC} +0.1	0	V_{CC}	V_{CC} +0.1	V
Negative reference voltage, V_{ref-} (see Note 3)			–0.1	0	V_{CC}	–0.1	0	V_{CC}	V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 3)			0	V_{CC}	V_{CC} +0.2	0	V_{CC}	V_{CC} +0.2	V
Analog input voltage (see Note 3)			0		V_{CC}	0		V_{CC}	V
High-level control input voltage, V_{IH}			2			2			V
Low-level control input voltage, V_{IL}					0.8			0.8	V
Setup time, address bits at data input before I/O CLOCK↑, $t_{su(A)}$			200			400			ns
Address hold time, t_h			0			0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 2)			3			3			System clock cycles
I/O CLOCK frequency, $f_{clock(I/O)}$			0		2.048	0		1.1	MHz
SYSTEM CLOCK frequency, $f_{clock(SYS)}$			$f_{clock(I/O)}$		4	$f_{clock(I/O)}$		2.1	MHz
Pulse duration, $\overline{CS}$ high during conversion, $t_{wH(CS)}$			36			36			System clock cycles
Pulse duration, SYSTEM CLOCK high, $t_{wH(SYS)}$			110			210			ns
Pulse duration, SYSTEM CLOCK low, $t_{wL(SYS)}$			100			190			ns
Pulse duration, I/O CLOCK high, $t_{wH(I/O)}$			200			404			ns
Pulse duration, I/O CLOCK low, $t_{wL(I/O)}$			200			404			ns
Clock transition time (see Note 4)	System	$f_{clock(SYS)} \le 1048$ kHz			30			30	ns
		$f_{clock(SYS)} > 1048$ kHz			20			20	
	I/O	$f_{clock(I/O)} \le 525$ kHz			100			100	ns
		$f_{clock(I/O)} > 525$ kHz			40			40	
Operating free-air temperature, T_A		TLC545C, TLC546C	0		70	0		70	°C
		TLC545I, TLC546I	–40		85	–40		85	

NOTES: 2. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for three system clock cycles (or less) after a chip select falling edge or rising edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip select setup time has elapsed.

3. Analog input voltages greater than that applied to REF+ convert as all “1”s (11111111), while input voltages less than that applied to REF– convert as all “0”s (00000000). As the differential reference voltage decreases below 4.75 V, the total unadjusted error tends to increase.

4. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 µs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating temperature range, $V_{CC} = V_{ref+} = 4.75$ V to 5.5 V, $f_{clock(I/O)} = 2.048$ MHz for TLC545 or $f_{clock(I/O)} = 1.1$ MHz for TLC546 (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (DATA OUT)		V_{CC} = 4.75 V,	I_{OH} = –360 μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V,	I_{OL} = 3.2 mA			0.4	V
I_{OZ}	Off-state (high-impedance state) ouput current		$V_O = V_{CC}$,	$\overline{CS}$ at V_{CC}			10	μA
			V_O = 0,	$\overline{CS}$ at V_{CC}			–10	
I_{IH}	High-level input current		$V_I = V_{CC}$			0.005	2.5	μA
I_{IL}	Low-level input current		V_I = 0			–0.005	–2.5	μA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			1.2	2.5	mA
	Selected channel leakage current		Selected channel at V_{CC}, Unselected channel at 0 V			0.4	1	μA
			Selected channel at 0 V, Unselected channel at V_{CC}			–0.4	–1	
$I_{CC} + I_{ref}$	Supply and reference current		$V_{ref+} = V_{CC}$,	$\overline{CS}$ at 0 V		1.3	3	mA
C_i	Input capacitance	Analog inputs				7	55	pF
		Control inputs				5	15	

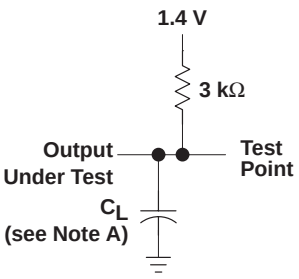
† All typical values are at T_A = 25°C.

operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+} = 4.75$ V to 5.5 V, $f_{clock(I/O)} = 2.048$ MHz for TLC545 or 1.1 MHz for TLC546, $f_{clock(SYS)} = 4$ MHz for TLC545 or 2.1 MHz for TLC546

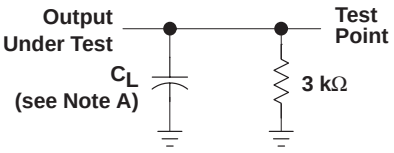
PARAMETER		TEST CONDITIONS	TLC545			TLC546			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
E_L	Linearity error	See Note 5			±0.5			±0.5	LSB
E_{ZS}	Zero-scale error	See Note 6			±0.5			±0.5	LSB
E_{FS}	Full-scale error	See Note 6			±0.5			±0.5	LSB
	Total unadjusted error	See Note 7			±0.5			±0.5	LSB
	Self-test output code	INPUT A19 address = 10011 (see Note 8)	01111101 (125)		10000011 (131)	01111101 (125)		10000011 (131)	
t_{conv}	Conversion time	See Operating Sequence			9			17	µs
	Total access and conversion time	See Operating Sequence			13			25	µs
t_{acq}	Channel acquisition time (sample cycle)	See Operating Sequence			3			3	I/O clock cycles
t_v	Time output data remains valid after I/O CLOCK↓		10			10			ns
t_d	Delay time, I/O CLOCK to DATA OUT valid	See Parameter Measurement Information			300			400	ns
t_{en}	Output enable time				150			150	ns
t_{dis}	Output disable time				150			150	ns
$t_{r(bus)}$	Data bus rise time				300			300	ns
$t_{f(bus)}$	Data bus fall time				300			300	ns

NOTES: 5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Zero-scale error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
7. Total unadjusted error is the sum of linearity, zero-scale, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic. The INPUT A19 analog input signal is internally generated and is used for test purposes.

PARAMETER MEASUREMENT INFORMATION

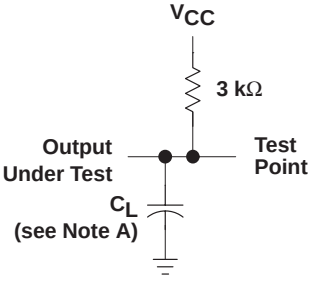


LOAD CIRCUIT FOR t_d, t_r, AND t_f



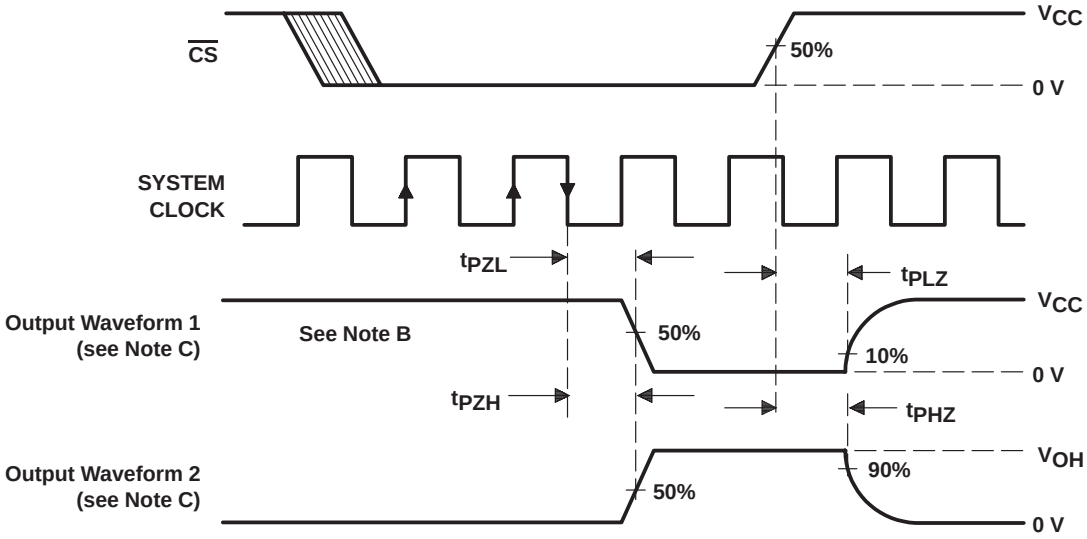
See Note B

LOAD CIRCUIT FOR t_{PZH} AND t_{PHZ}

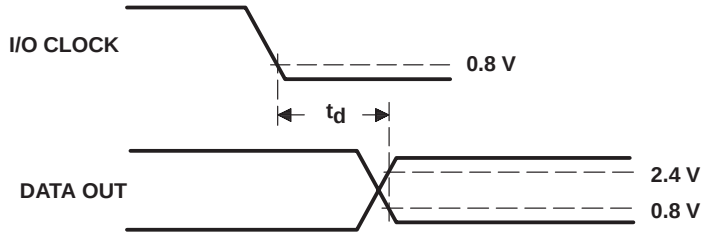


See Note B

LOAD CIRCUIT FOR t_{PZL} AND t_{PLZ}



VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS FOR DELAY TIME



VOLTAGE WAVEFORMS FOR RISE AND FALL TIMES

NOTES: A. C_L = 50 pF for TLC545 and 100 pF for TLC546
B. $t_{en} = t_{PZH}$ or t_{PZL}, $t_{dis} = t_{PHZ}$ or t_{PLZ}
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

PARAMETER MEASUREMENT INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 1, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S \left(1 - e^{-t_c/R_t C_i}\right) \quad (1)$$

where

$$R_t = R_S + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C \text{ (1/2 LSB)} = V_S - (V_S/512) \quad (2)$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - (V_S/512) = V_S \left(1 - e^{-t_c/R_t C_i}\right) \quad (3)$$

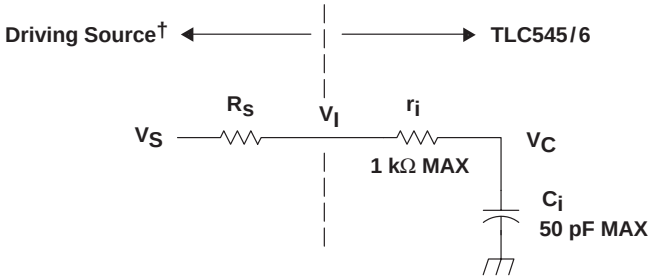
and

$$t_c \text{ (1/2 LSB)} = R_t \times C_i \times \ln(512) \quad (4)$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c \text{ (1/2 LSB)} = (R_S + 1\ \text{k}\Omega) \times 60\ \text{pF} \times \ln(512) \quad (5)$$

This time must be less than the converter sample time shown in the timing diagrams.



V_I = Input Voltage at INPUT A0 – A18
V_S = External Driving Source Voltage
R_S = Source Resistance
r_i = Input Resistance
C_i = Input Capacitance

† Driving source requirements:

- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_S must be real at the input frequency.

Figure 1. Equivalent Input Circuit Including the Driving Source

PRINCIPLES OF OPERATION

The TLC545 and TLC546 are both complete data acquisition systems on single chips. Each includes such functions as system clock, sample and hold, 8-bit A/D converter, data and control registers, and control logic. For flexibility and access speed, there are four control inputs; $\overline{CS}$, ADDRESS INPUT, I/O CLOCK, and SYSTEM CLOCK. These control inputs and a TTL-compatible 3-state output facilitate serial communications with a microprocessor or microcomputer. The TLC545 and TLC546 can complete conversions in a maximum of 9 and 17 μs respectively, while complete input-conversion-output cycles can be repeated at a maximum of 13 and 25 μs, respectively.

The system clock and I/O clock are normally used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Once a clock signal within the specification range is applied to the SYSTEM CLOCK input, the control hardware and software need only be concerned with addressing the desired analog channel, reading the previous conversion result, and starting the conversion by using the I/O CLOCK. SYSTEM CLOCK will drive the “conversion crunching” circuitry so that the control hardware and software need not be concerned with this task.

When $\overline{CS}$ is high, DATA OUT is in a high-impedance condition, and ADDRESS INPUT and I/O CLOCK are disabled. This feature allows each of these terminals, with the exception of $\overline{CS}$, to share a control logic point with their counterpart terminals on additional A/D devices when additional TLC545/TLC546 devices are used. Thus, the above feature serves to minimize the required control logic terminals when using multiple A/D devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for two rising edges and then a falling edge of the SYSTEM CLOCK after a $\overline{CS}$ transition before the transition is recognized. The MSB of the previous conversion result automatically appears on DATA OUT.
2. A new positive-logic multiplexer address is shifted in on the first five rising edges of I/O CLOCK. The MSB of the address is shifted in first. The negative edges of these five I/O clocks shift out the second, third, fourth, fifth, and sixth most significant bits of the previous conversion result. The on-chip sample and hold begins sampling the newly addressed analog input after the fifth falling edge. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Two clock cycles are then applied to I/O CLOCK and the seventh and eighth conversion bits are shifted out on the negative edges of these clock cycles.
4. The final eighth clock cycle is applied to I/O CLOCK. The falling edge of this clock cycle completes the analog sampling process and initiates the hold function. Conversion is then performed during the next 36 system clock cycles. After this final I/O clock cycle, $\overline{CS}$ must go high or the I/O CLOCK must remain low for at least 36 system clock cycles to allow for the conversion function.

$\overline{CS}$ can be kept low during periods of multiple conversion. When keeping $\overline{CS}$ low during periods of multiple conversion, special care must be exercised to prevent noise glitches on the I/O CLOCK line. If glitches occur on the I/O CLOCK line, the I/O sequence between the microprocessor/controller and the device loses synchronization. Also, if $\overline{CS}$ is taken high, it must remain high until the end of conversion. Otherwise, a valid falling edge of $\overline{CS}$ causes a reset condition, which aborts the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 system clock cycles occur. Such action yields the conversion result of the previous conversion and not the ongoing conversion.

PRINCIPLES OF OPERATION

It is possible to connect SYSTEM CLOCK and I/O CLOCK together in special situations in which controlling circuitry points must be minimized. In this case, the following special points must be considered in addition to the requirements of the normal control sequence previously described.

1. The first two clocks are required for this device to recognize $\overline{CS}$ is at a valid low level when the common clock signal is used as an I/O CLOCK. When $\overline{CS}$ is recognized by the device to be at a high level, the common clock signal is used for the conversion clock also.
2. A low $\overline{CS}$ must be recognized before the I/O CLOCK can shift in an analog channel address. The device recognizes a $\overline{CS}$ transition when the SYSTEM CLOCK terminal receives two positive edges and then a negative edge. For this reason, after a $\overline{CS}$ negative edge, the first two clock cycles do not shift in the address. Also, upon shifting in the address, $\overline{CS}$ must be raised after the eighth valid (10 total) I/O CLOCK. Otherwise, additional common clock cycles are recognized as I/O CLOCKS and shift in an erroneous address.

For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device accommodates these applications. Although the on-chip sample and hold begins sampling upon the negative edge of the fourth valid I/O clock cycle, the hold function is not initiated until the negative edge of the eighth valid I/O clock cycle. Thus, the control circuitry can leave the I/O clock signal in its high state during the eighth valid I/O clock cycle, until the moment at which the analog signal must be converted. The TLC545/546 continues sampling the analog input until the eighth valid falling edge of the I/O clock. The control circuitry or software must then immediately lower the I/O clock signal to initiate the hold function at the desired point in time and to start conversion.

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