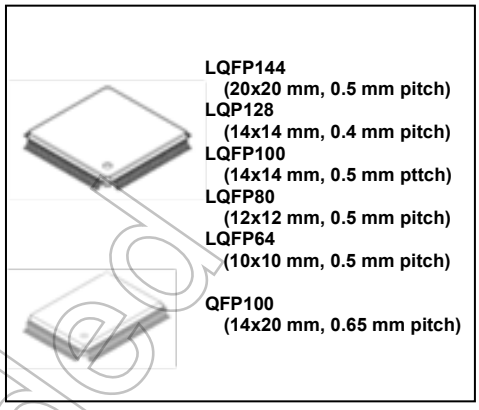
CMOS Digital Integrated Circuit Silicon Monolithic

TMPM3H Group(2)



LQFP144
(20x20 mm, 0.5 mm pitch)
LQP128
(14x14 mm, 0.4 mm pitch)
LQFP100
(14x14 mm, 0.5 mm pttch)
LQFP80
(12x12 mm, 0.5 mm pitch)
LQFP64
(10x10 mm, 0.5 mm pitch)

QFP100
(14x20 mm, 0.65 mm pitch)

General Description

- Arm ® Cortex®-M3 core. Operating frequency: 1 to 80 MHz.
  Operating voltage: 2.7 to 5.5V
- Code flash: 256KB to 512KB. Data flash: 32KB.
- Package: 64-pin to 144-pin. 6 types of packages are available.

Applications

Widely used for consumer products and industrial products including home appliances, OA equipment, household equipment, AV devices, and motor control devices.

Features

- ARM Cortex-M3 core
  - Operating frequency: 1 to 80 MHz
  - Memory Protection Unit (MPU)
- Low-power consumption mode
  - Operating voltage: 2.7 to 5.5V
  - Low-power consumption operation: IDLE, STOP1,STOP2
- Operating temperature: -40 to +85°C
- Internal memory
  - Code flash: 256KB to 512 KB, rewritable up to 10,000 times
  - Data flash: 32 KB, rewritable up to 100,000 times
  - Data flash is rewritable in parallel with instruction execution
  - RAM: 64KB(with Parity) and Backup RAM 2 KB
- Clock
  - External High-speed Oscillator: 6 MHz to 12 MHz(Ceramic, Crystal)
  - External High-speed clock input: 6 to 20 MHz
  - Internal High-speed Oscillator (IHOSC1): 10 MHz, user trimming function
  - PLL: 80 MHz output
  - External Low-speed Oscillator: 32.768kHz
- Oscillation Frequency Detector (OFD): Abnormal system clock detection
- Voltage Detection circuit (LVD): 8 level, Generate interrupts and reset outputs
- Interruption
  - External: 12 to 32 factors, with DNF
  - internal: 116 to 136 factors
- I/O ports: GPIO: 56 to 134 (Include Input only: 4, Output only: 1)
  - pull-up/pull-down resistor,Open-drain,5V-tolerant
- On chip Debug(JTAG/SW)
- Trigger Selection Circuit(TRGSEL)
  - Expand Trigger request for DMAC, Timer, others
- DMA Controller(DMAC)
  - DMA requests: 2units,62 to 64 factors, internal/external triggers
- Universal Asynchronous Receiver Transmitter(UART): 6 channels
  - 2.5Mbps(Max),FIFO(Send 8-stage, Receive 8-stage)
- Serial Peripheral Interface(TSPI): 1 to 5 channels
  - SIO/SPI mode,20MHz(MAX),FIFO(Send 16bitx8,Receive 16bitx8)
- I^2C Interface(I2C): 2 to 4 channels
  - Multi Master, Release function for Low Power Mode
- Comparator: 1 channels. EMG signal output to A-PMD
- 8-bit DA Converter(DAC): 2 channels
- 12-bit ADC(ADC): 10 to 21 channels analog inputs
  - Sample-and-hold circuit
  - Conversion time: 1.5μs@ADCLK=40MHz
  - Self-diagnosis support function
- Advanced Programmable Motor Control Circuit (A-PMD): 1 channel
  - 3 phase PWM output, Synchronized with 12-bit ADC
  - Emergency stop function by external inputs (EMG0 pin, OVV0 pin)
- Advanced Encoder Input Circuit (A-ENC): 1 channel
  - Encoder/sensor (3 types)/Timer /Phase counter mode
- 32bit Timer Event Counter (T32A)
  - 8 channels as 32-bit Timers:16 channels as 16-bit Timers
  - Interval Timer, event counter, input capture, phase difference input, PPG output, Sync Start, Trigger Start
- Real Time Clock (RTC): 1 channel
- Watchdog Timer (SIWDT): 1 channel
  - Clock system other than the system clock can be selected
  - Clear window, interrupts and reset output
- Remote control signal preprocessor (RMC): 1 channel
- CRC calculation circuit(CRC): 1channel, CRC32, CRC16

Start of commercial production
2018-03

Not Recommended for New Design

© 2017-2021
Toshiba Electronic Devices & Storage Corporation

Products Lists Categorized by Functions

The product under development is contained in this table.
For the newest status of each product, please contact your sales representative.

Table 1 Products List

Built-in Functions		TMPM3HQFDFG TMPM3HQFZFG TMPM3HQFYFG	TMPM3HPFDFG TMPM3HPFZFG TMPM3HPFYFG	TMPM3HNFDFG TMPM3HNFZFG TMPM3HNFYFG	TMPM3HNFDDFG TMPM3HNFZDFG TMPM3HNFYDFG	TMPM3HMFDFG TMPM3HMFZFG TMPM3HMFYFG	TMPM3HLFDUG TMPM3HLFZUG TMPM3HLFYUG
Memory	Code Flash (KB)	512 384 256	512 384 256	512 384 256	512 384 256	512 384 256	512 384 256
	Data Flash (KB)	32 32 32	32 32 32	32 32 32	32 32 32	32 32 32	32 32 32
	RAM (KB)	64 64 64	64 64 64	64 64 64	64 64 64	64 64 64	64 64 64
	Backup RAM (KB)	2	2	2	2	2	2
I/O port	PORT (Pin)	134	118	92	92	72	56
External interrupt	INT (Pin)	32	29	19	19	15	12
DMA	DMAC (ch)	64	64	64	64	62	53
Timer function	T32A (ch)	8	8	8	8	8	8
	RTC (ch)	1	1	1	1	1	1
Serial communication function	UART (ch)	6	6	6	6	6	6
	I²C (ch)	4	4	3	3	3	2
	TSPI (ch)	5	5	4	4	4	1
Analog function	12-bit ADC (ch)	21	19	13	13	10	10
	8-bit DAC (ch)	2	2	2	2	2	2
	Comparator(ch)	1	1	1	1	1	1
Motor Control peripherals	A-ENC (ch)	1	1	1	1	1	1
	A-PMD (ch)	1	1	1	1	1	1
Other peripherals	RMC (ch)	1	1	1	1	1	1
	CRC(ch)	1	1	1	1	1	1
System function	RAMP	1	1	1	1	1	1
	LVD (ch)	1	1	1	1	1	1
	SIWDT (ch)	1	1	1	1	1	1
	OFD (ch)	1	1	1	1	1	1
	POR	1	1	1	1	1	1
Debug interface	Debug	JTAG/SW TRACE(4bit)	JTAG/SW TRACE(4bit)	JTAG/SW TRACE(4bit)	JTAG/SW TRACE(4bit)	JTAG/SW TRACE(2bit)	JTAG/SW
Package	Package type	LQFP144 (20 mm x 20 mm, 0.5 mm pitch)	LQFP128 (14 mm x 14 mm, 0.4 mm pitch)	LQFP100 (14 mm x 14 mm, 0.5 mm pitch)	QFP100 (14 mm x 20 mm, 0.65 mm pitch)	LQFP80 (12 mm x 12 mm, 0.5 mm pitch)	LQFP64 (10 mm x 10 mm, 0.5 mm pitch)
	Package name	P-LQFP144-2020 -0.50-002	P-LQFP128-1414 -0.40-001	P-LQFP100-1414 -050-002	P-QFP100-1420 -0.65-001	P-LQF80-1212 - 0.50-003	P-LQFP64-1010 - 0.50-003

Not Recommended for New Design

Contents

General Description 1
Applications 1
Features 1
Products Lists Categorized by Functions 2
Contents 3
List of Figures 6
List of Tables 7
Preface 8
Conventions 8
Terms and Abbreviations 10
1. Block Diagram 11
2. Pin Assignment 12
2.1. LQFP144 12
2.2. QFP128 13
2.3. LQFP100 14
2.4. QFP100 15
2.5. LQFP80 16
2.6. LQFP64 17
3. Memory Map 18
3.1. List of Memory Sizes 19
4. Pin Description 20
4.1. Functional Pin Name and Functions 20
4.1.1. Function Pins of Peripheral 20
4.1.2. Debug Pins 22
4.1.3. Control Pins 23
4.1.4. Power Supply Pins 23
4.1.5. Capacitors between power supply pins 24
4.2. Functional Pin and Ports Assignment (Pin Number) 25
4.3. Ports 38
4.3.1. Port Specifications Table 39
5. Functional Description and Operation Description 43
5.1. Reference Manuals 43
5.2. Processor Core 44
5.2.1. Core Information 44
5.2.2. Configurable Options 44
5.3. Clock Control and Operation mode (CG) 45
5.4. Flash Memory (Code FLASH, Data FLASH) 45
5.5. Oscillation Circuit 46
5.6. Trimming Circuit (TRM) 46

Not Recommended for New Design

5.7. Oscillation Frequency Detector (OFD) 46
5.8. Voltage Detection Circuit (LVD) 47
5.9. Digital Noise Filter (DNF) 47
5.10. Debug Interface (DEBUG) 48
5.11. DMA Controller (DMAC) 49
5.12. Universal Asynchronous Receiver Transmitter (UART) 49
5.13. Serial Peripheral Interface (TSPI) 50
5.14. I²C Interface (I²C) 50
5.15. 8-bit Digital to Analog Converter (DAC) 51
5.16. 12-bit Analog to Digital Converter (ADC) 51
5.17. Comparator (COMP) 51
5.18. Advanced Programmable Motor Control Circuit (A-PMD) 52
5.19. Advanced Encoder Input Circuit (A-ENC) 52
5.20. 32-bit Timer Event Counter (T32A) 53
5.21. Real Time Clock (RTC) 53
5.22. Clock Selective Watchdog Timer (SIWDT) 54
5.23. Remote control signal preprocessor (RMC) 54
5.24. CRC calculation circuit (CRC) 54
5.25. RAM Parity (RAMP) 55
6. Equivalent Circuit 56
6.1. Port 56
6.2. Analog Power pin 60
6.3. Control Pin 60
6.4. Clock control 61
7. Electrical Characteristics 62
7.1. Absolute Maximum Ratings 62
7.2. DC Electrical Characteristics (1/2) 63
7.3. DC Electrical Characteristics (2/2) 67
7.4. 12-bit AD Converter Characteristics 69
7.5. 8-bit DA Converter Characteristics 70
7.6. Comparator Characteristics 70
7.7. Characteristics of Internal processing at RESET 71
7.8. Characteristics of Power On Reset 71
7.9. Characteristics of Voltage Detection Circuit 72
7.10. AC Electrical Characteristics 73
7.10.1. Serial Peripheral Interface (TSPI) 73
7.10.2. I²C Interface (I²C) 81
7.10.3. 32-bit Timer Event Counter (T32A) 83
7.10.4. External Interrupt 84
7.10.5. Trigger Input (TRGINx) 85

Not Recommended for New Design

7.10.6. Debug Communication 86
7.10.7. SCOUT Pin 89
7.10.8. Noise Filter Characteristics 89
7.10.9. External Clock Input 90
7.11. Flash Memory Characteristics 91
7.11.1. Code Flash 91
7.11.2. Data Flash 91
7.11.3. Chip Erase 91
7.12. Regulator 92
7.13. Oscillation Circuit 92
7.13.1. Internal Oscillator 92
7.13.2. External Oscillator 92
7.13.3. Oscillation Circuit 93
7.13.4. Ceramic resonator 93
7.13.5. Crystal unit 93
7.13.6. Precautions for designing printed circuit board 93
8. Package Dimensions 94
8.1. P-LQFP144-2020-0.50-002 94
8.2. P-LQFP128-1414-0.40-001 95
8.3. P-LQFP100-1414-0.50-002 96
8.4. P-QFP100-1420-0.65-001 97
8.5. P-LQFP80-1212-0.50-003 98
8.6. P-LQFP64-1010-0.50-003 99
9. Precautions 100
10. Revision History 101
Appendix 103
List of All pins 103
Part Naming Conventions 107
RESTRICTIONS ON PRODUCT USE 108

Not Recommended for New Design

List of Figures

Figure 1.1 Block diagram of the TMPM3H Group(2) 11
Figure 3.1 Example of the TMPM3HQFDFG 18
Figure 4.1 Capacitors for power supply pins connection circuit 24
Figure 7.1 1st clock edge sampling (Master) 79
Figure 7.2 2nd clock edge sampling (Master) 79
Figure 7.3 2nd clock edge sampling (Slave) 80
Figure 7.4 AC timing of I^2C 82
Figure 7.5 Count Pulse input 84
Figure 7.6 JTAG/SWD waveform 87
Figure 7.7 Trace signal waveform 88
Figure 7.8 SCOUT wave output 89
Figure 7.9 External clock input waveform 90
Figure 7.10 Oscillation circuit sample 93

Not Recommended for New Design

List of Tables

Table 1 Products List 2
Table 3.1 Memory sizes and addresses 19
Table 4.1 Pin names and functions of peripheral pins 20
Table 4.2 Debug pin names and their function 22
Table 4.3 Control pin names and their function 23
Table 4.4 Power supply pin names and their function 23
Table 4.5 Signal connection List(1/13) 25
Table 4.6 Signal connection List(2/13) 26
Table 4.7 Signal connection List (3/13) 27
Table 4.8 Signal connection List (4/13) 28
Table 4.9 Signal Connection List (5/13) 29
Table 4.10 Signal connection List (6/13) 30
Table 4.11 Signal connection List (7/13) 31
Table 4.12 Signal connection List (8/13) 32
Table 4.13 Signal connection List (9/13) 33
Table 4.14 Signal connection List (10/13) 34
Table 4.15 Signal connection List (11/13) 35
Table 4.16 Signal connection List (12/13) 36
Table 4.17 Signal connection List (13/13) 37
Table 4.18 Port names, and specifications of Port A, B, C, D, E 39
Table 4.19 Port names, and specifications of Port F, G, H, J, K 40
Table 4.20 Port names, and specifications of Port L, M, N, P, R 41
Table 4.21 Port names, and specifications of Port T, U, V 42
Table 5.1 Reference Manuals for TMPM3H Group(2) 43
Table 5.2 Core revision 44
Table 5.3 Configurable options and their implementations 44
Table 5.4 Built-in Oscillator 46
Table 5.5 Built-in TRM 46
Table 5.6 Built-in OFD 46
Table 5.7 Built-in LVD 47
Table 5.8 Number of External Interrupt (Built-in DNF) 47
Table 5.9 Built-in Debug Interface 48
Table 5.10 Built-in DMAC 49
Table 5.11 Built-in UART 49
Table 5.12 Built-in TSPI 50
Table 5.13 Built-in I^2C 50
Table 5.14 Built-in DAC 51
Table 5.15 Built-in ADC 51
Table 5.16 Number of analog inputs for ADC 51
Table 5.17 Built-in Comparator 51
Table 5.18 Built-in A-PMD 52
Table 5.19 Built-in A-ENC 52
Table 5.20 Built-in T32A 53
Table 5.21 Built-in RTC 53
Table 5.22 Built-in SIWDT 54
Table 5.23 Built-in RMC 54
Table 5.24 Built-in CRC calculation circuit 54
Table 5.25 Built-in RAM parity circuit 55
Table 7.1 Absolute maximum ratings 62
Table 7.2 IDD measurement condition (Pin setting, Oscillation Circuit) 67
Table 7.3 IDD measurement condition (CPU, Peripheral) 68
Table 10.1 Revision History 101

Not Recommended for New Design

Preface

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C . . .
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] →[ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 . . .
  Example: [***T32A0RUNA], [T32A1RUNA], [T32A2RUNA] → [T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Not Recommended for New Design

****
Arm, Cortex and Thumb are registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere. All rights reserved.
****

The flash memory uses the Super Flash® technology under license from Silicon Storage Technology, Inc.
SuperFlash® is registered trademark of Silicon Storage Technology, Inc.

All other company names, product names, and service names mentioned herein may be trademarks of their respective companies.

Not Recommended for New Design

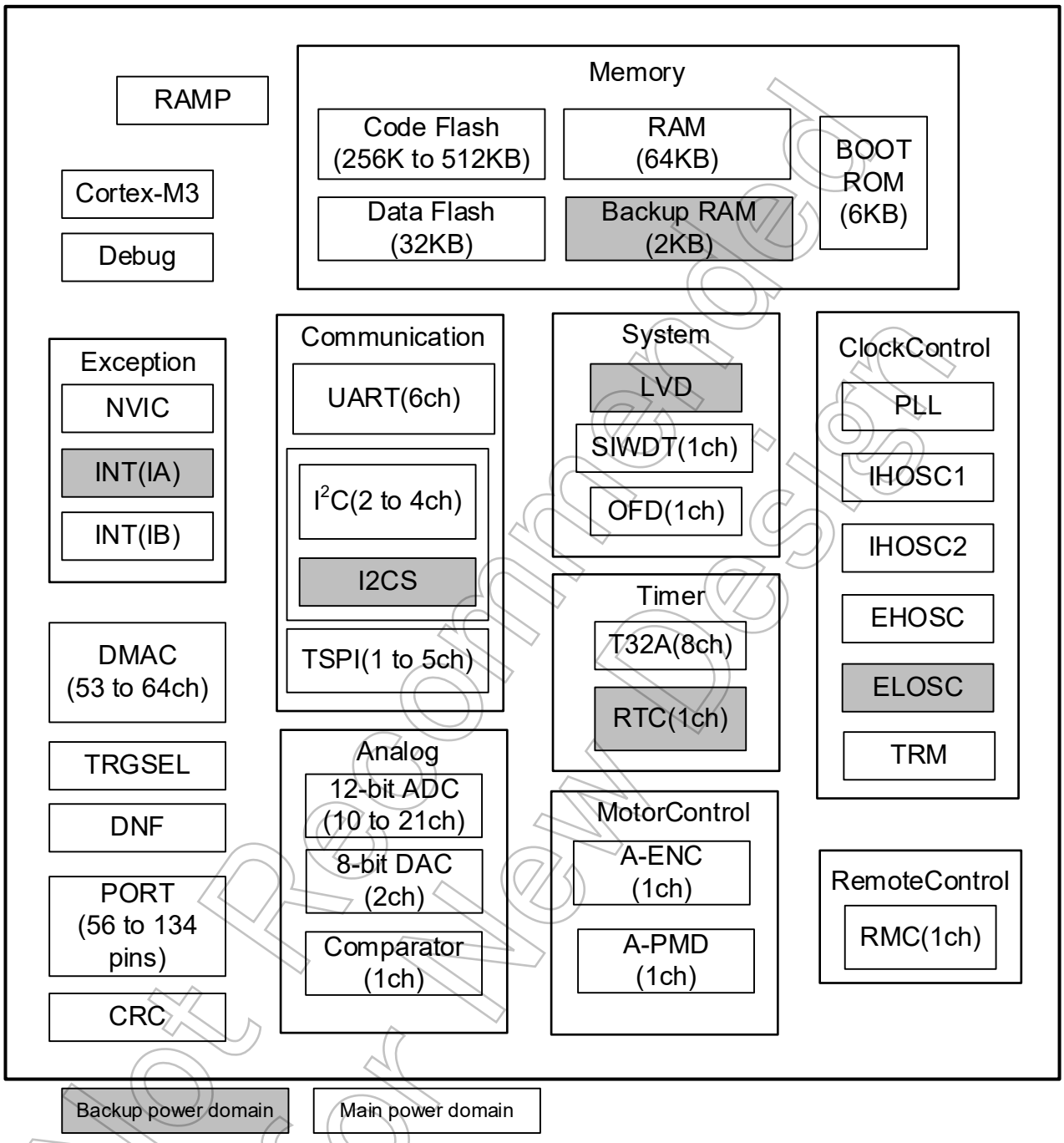
Terms and Abbreviations

The following words are terms or abbreviations mainly used in this datasheet.

ADC	Analog to Digital Converter
A-ENC	Advanced Encoder input Circuit
A-PMD	Advanced Programmable Motor Control Circuit
COMP	Comparator
CRC	Cyclic Redundancy Check
DAC	Digital to Analog Converter
DMAC	Direct Memory Access Controler
DNF	Digital Noise Filter
EHOSC	External High speed Oscillator
ELOSC	External Low speed Oscillator
Fm	I^2C Fast Mode
IHOSC	Internal High speed Oscillator
INT	Interrupt
I^2C	Inter-Integrated Circuit
I2CS	I^2C wake-up circuit from Stand-by mode
LVD	Voltage Detection Circuit
NMI	Non-Maskable Interrupt
OFD	Oscillation Frequency Detector
POR	Power On Reset Circuit
RAMP	RAM Parity
RMC	Remote control signal preprocessor
RTC	Real Time Clock
SIWDT	Clock Selective Watchdog Timer
TRGSEL	Trigger Selection circuit
TRM	Trimming circuit
TSPI	Serial Peripheral Interface
T32A	32-bit Timer Event Counter
UART	Universal Asynchronous Receiver Transmitter

Not Recommended for New Design

1. Block Diagram

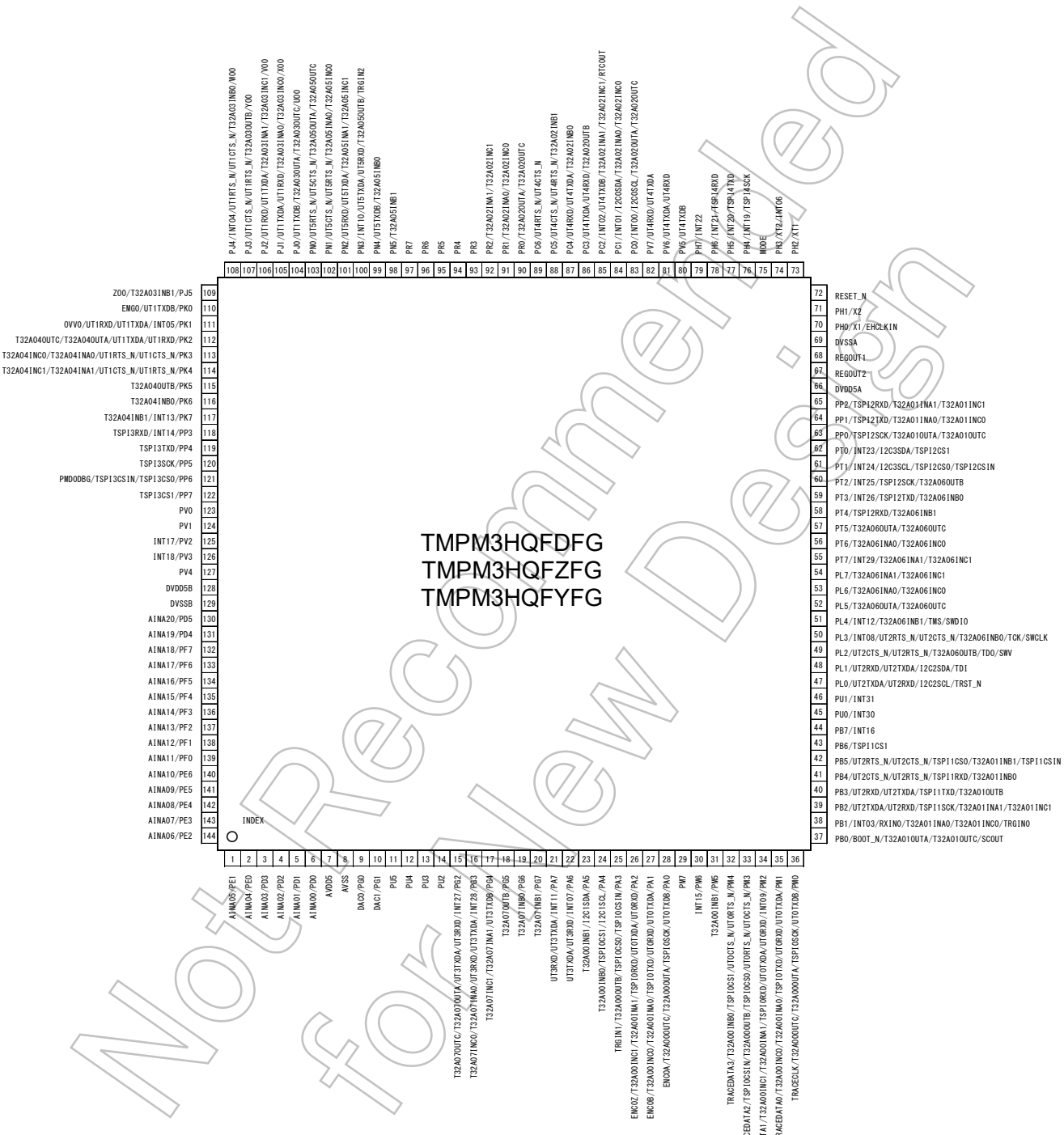


Not Recommended for New Design

Figure 1.1 Block diagram of the TMPM3H Group(2)

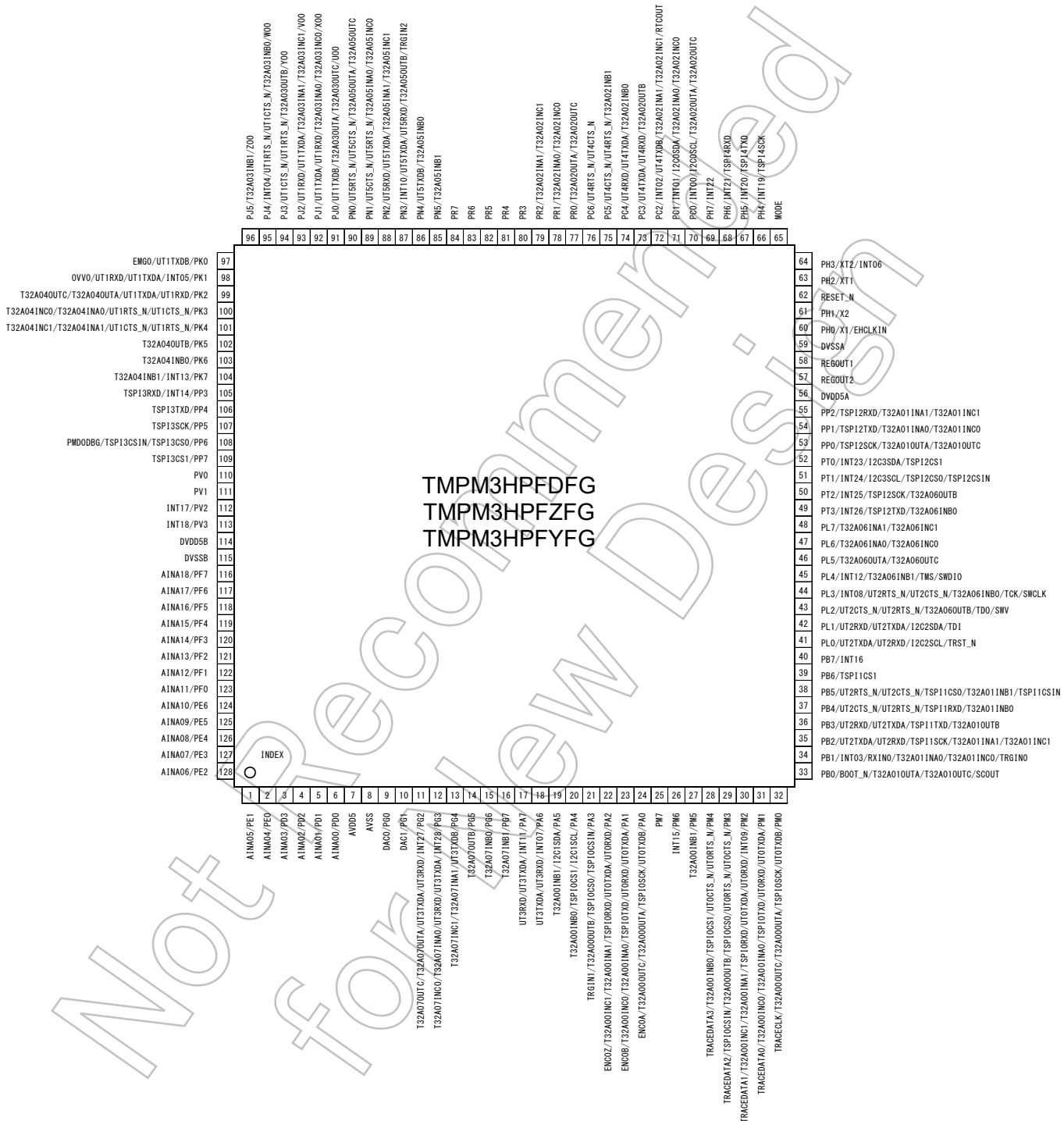
2. Pin Assignment

2.1. LQFP144



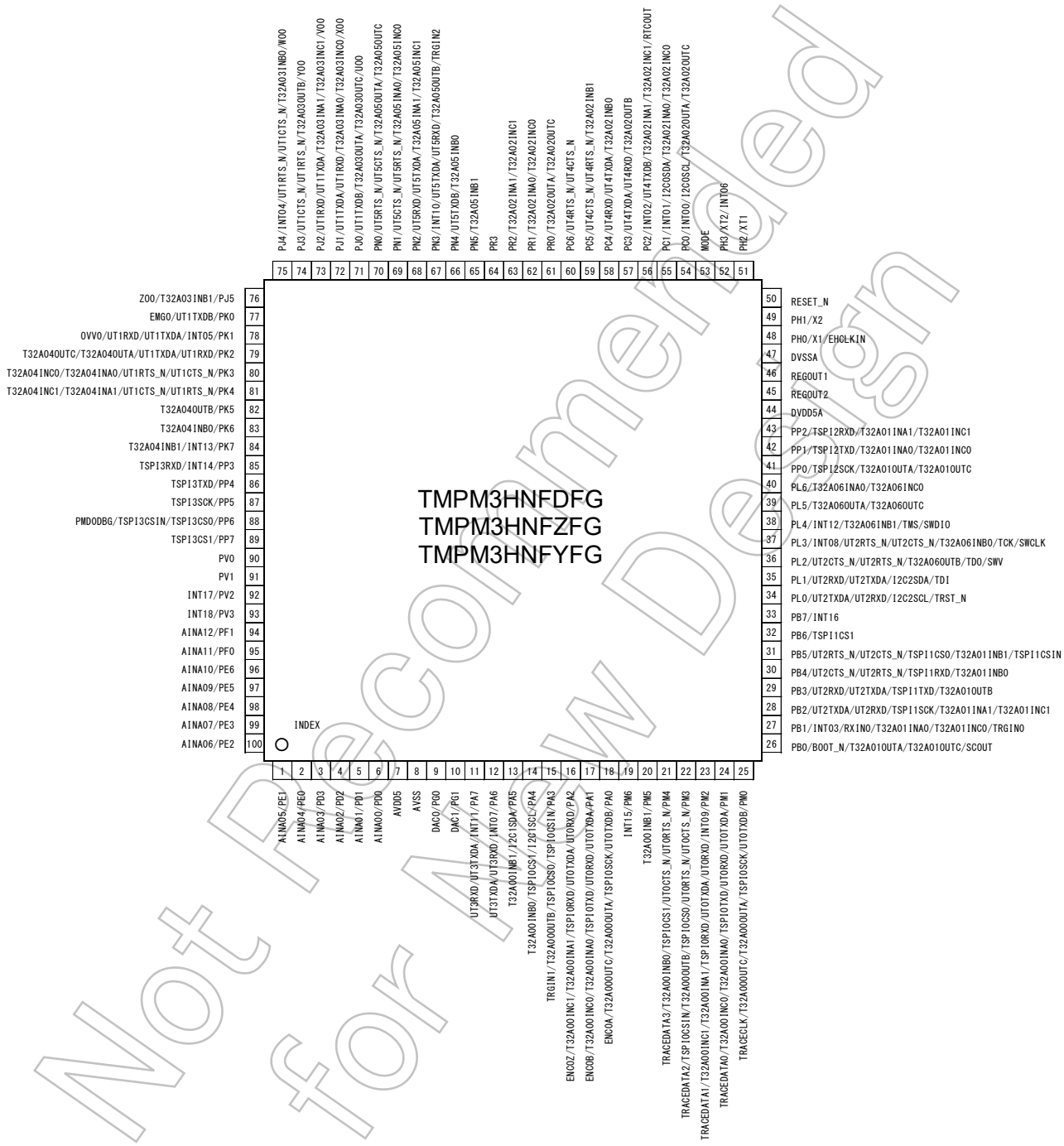
Not Recommended for New Design

2.2. QFP128



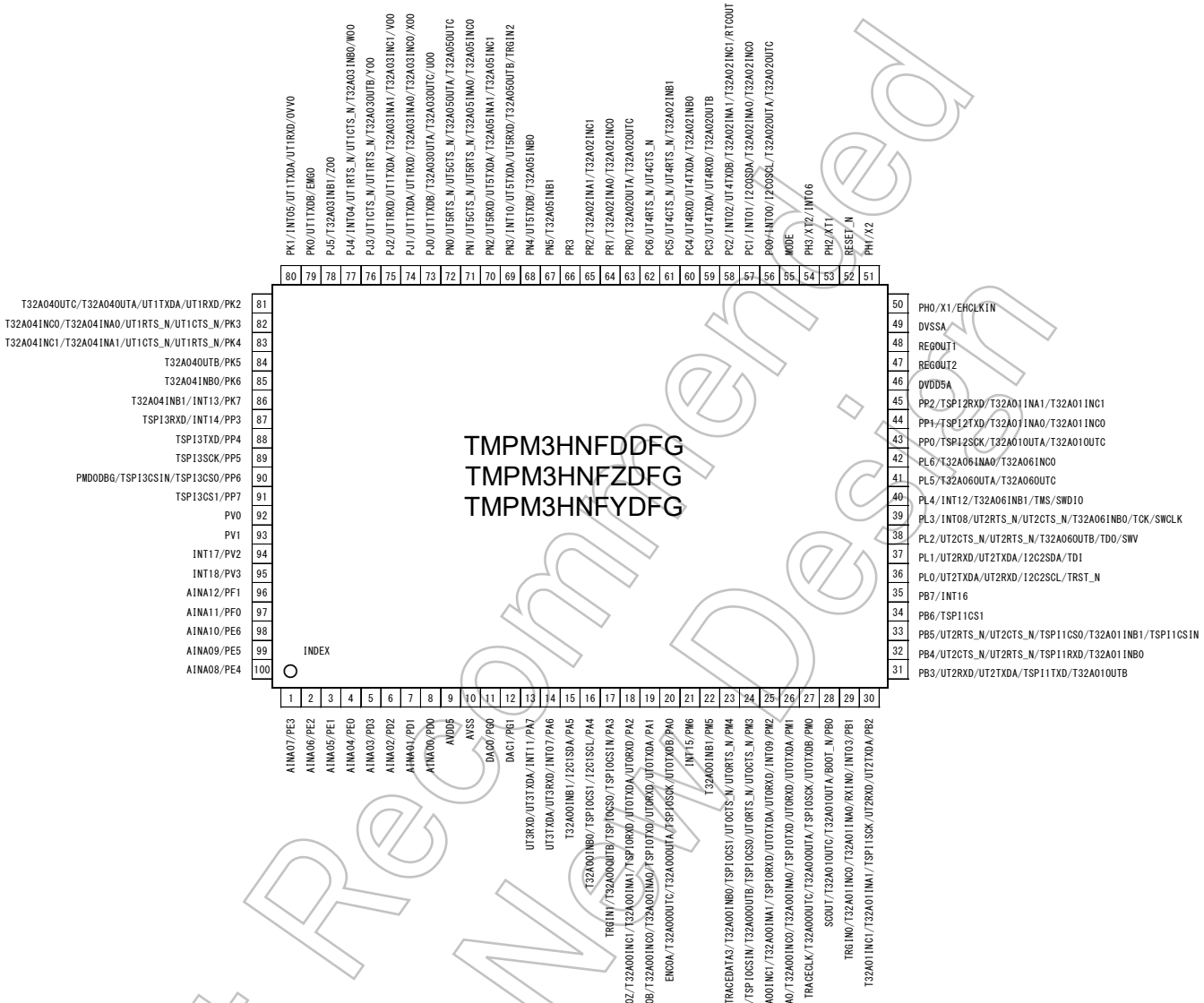
Not Recommended for New Design

2.3. LQFP100



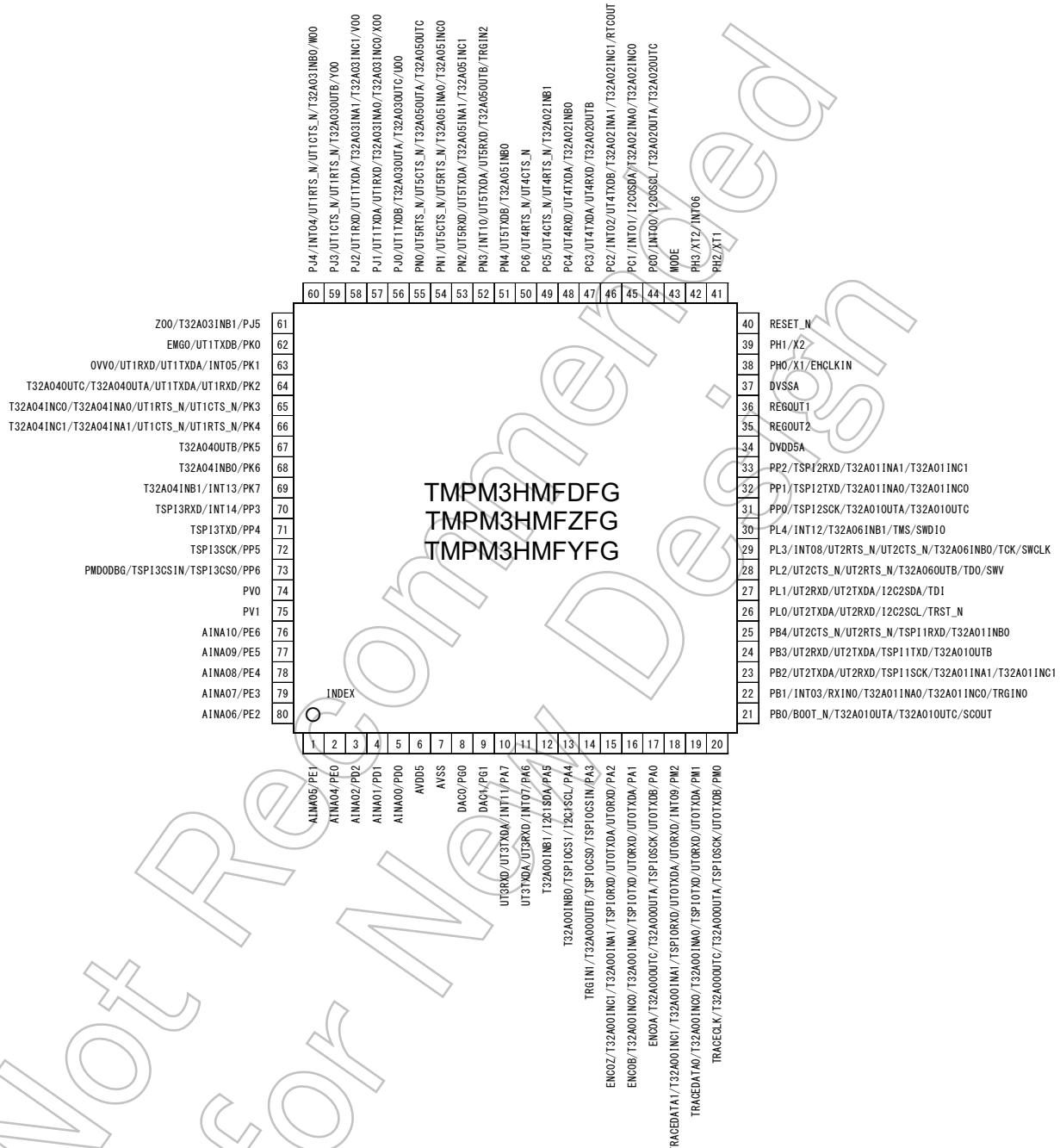
Not Recommended for New Design

2.4. QFP100



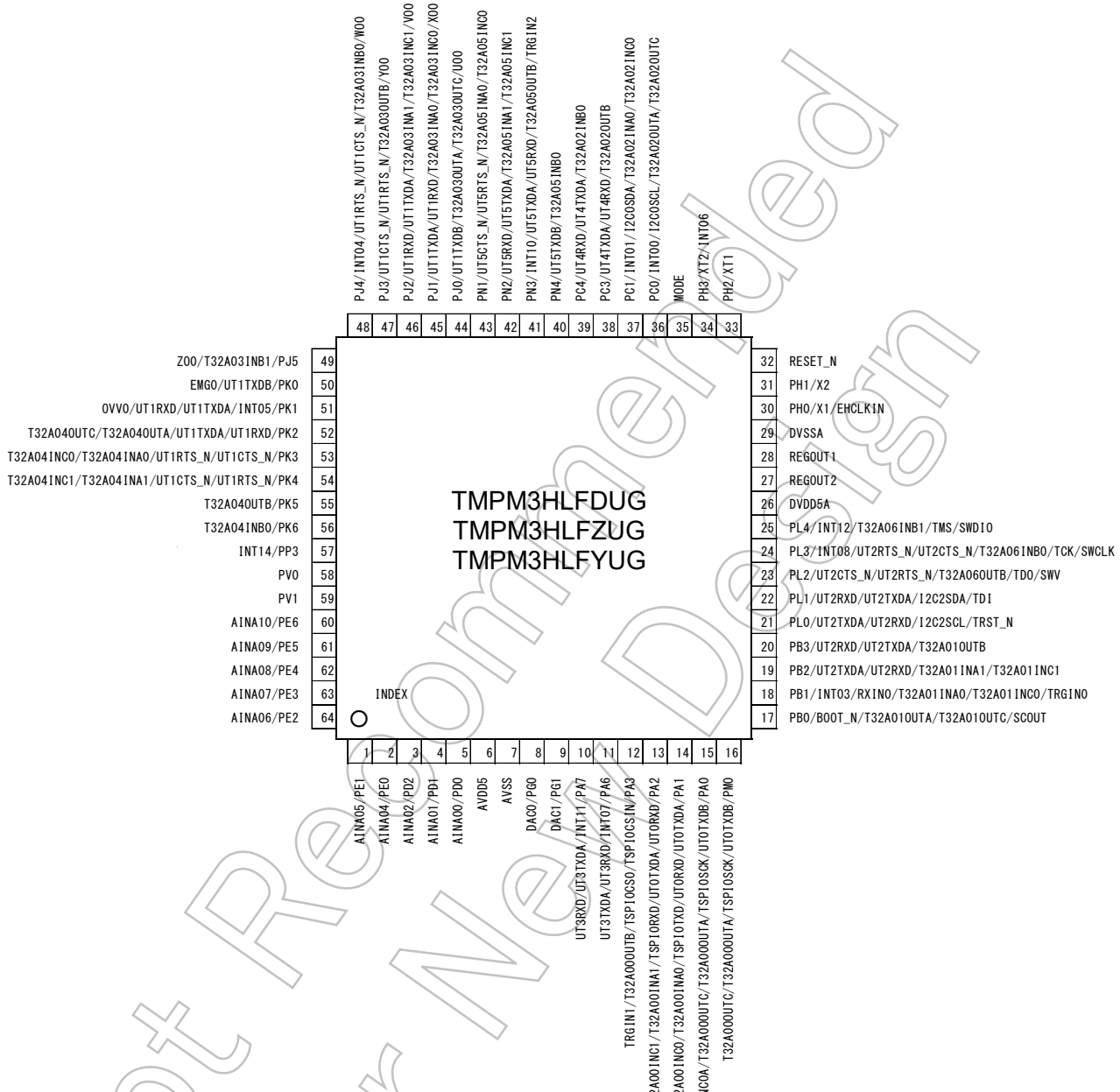
Not Recommended for New Design

2.5. LQFP80



Not Recommended for New Design

2.6. LQFP64



Not Recommended for New Design

3. Memory Map

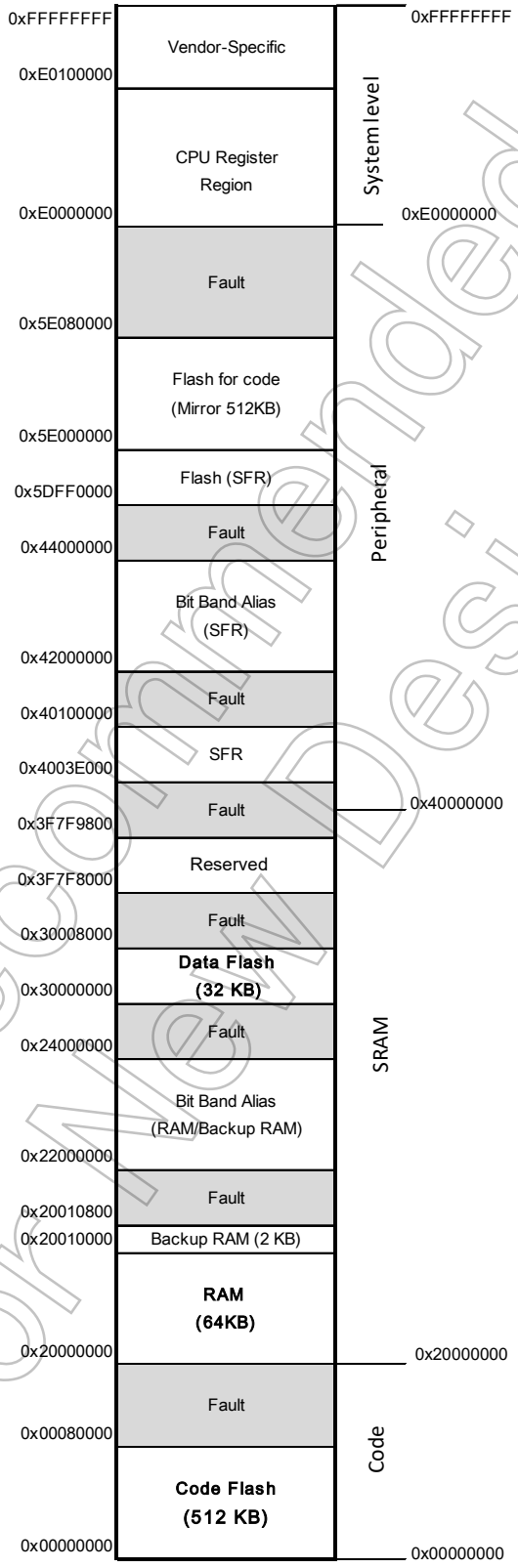


Figure 3.1 Example of the TMPM3HQFDFG

Not Recommended for New Design

3.1. List of Memory Sizes

Table 3.1 Memory sizes and addresses

Products			TMPM3HQFDFG TMPM3HPFDFG TMPM3HNFDFG TMPM3HNFDDFG TMPM3HMFDFG TMPM3HLFDUG	TMPM3HQFZFG TMPM3HPFZFG TMPM3HNFZFG TMPM3HNFZDFG TMPM3HMFZFG TMPM3HLFZUG	TMPM3HQFYFG TMPM3HPFYFG TMPM3HNFYFG TMPM3HNFYDFG TMPM3HMFYFG TMPM3HLFYUG
Peripheral region	Code Flash (Mirror)	Size	512KB	384KB	256KB
		START	0x5E000000	0x5E000000	0x5E000000
		END	0x5E07FFFF	0x5E05FFFF	0x5E03FFFF
SRAM region	Data Flash	Size	32KB		
		START	0x30000000		
		END	0x30007FFF		
	Backup RAM	Size	2KB		
		START	0x20010000		
		END	0x200107FF		
	RAM	Size	64KB		
		START	0x20000000		
		END	0x2000FFFF		
Code Region	Code Flash	Size	512KB	384KB	256KB
		START	0x00000000	0x00000000	0x00000000
		END	0x0007FFFF	0x0005FFFF	0x0003FFFF

Not Recommended for New Design

4. Pin Description

4.1. Functional Pin Name and Functions

4.1.1. Function Pins of Peripheral

Table 4.1 Pin names and functions of peripheral pins

Peripheral function	Pin name	Input or Output	Function
Clock Control and Operation Mode (CG)	SCOUT	Output	Output pin for the system clock
Interrupt control (IA/IB)	INTx	Input	External interrupt input pin External input pin provides the noise filter (filter width: typ. 30 ns).
32-bit Timer Event Counter (T32A)	T32AxINA0	Input	16-bit timer-A input capture input pin 0
	T32AxINA1	Input	16-bit timer-A input capture input pin 1
	T32AxOUTA	Output	16-bit timer A output pin
	T32AxINB0	Input	16-bit timer B input capture input pin 0
	T32AxINB1	Input	16-bit timer B input capture input pin 1
	T32AxOUTB	Output	16-bit timer B output pin
	T32AxINC0	Input	32-bit timer input capture input pin 0
	T32AxINC1	Input	32-bit timer input capture input pin 1
	T32AxOUTC	Output	32-bit timer output pin
Serial Peripheral Interface (TSPI)	TSPIxCSIN	Input	Chip select input pin
	TSPIxCS0	Output	Chip select output pin 0
	TSPIxCS1	Output	Chip select output pin 1
	TSPIxRXD	Input	Data input pin
	TSPIxTXD	Output	Data output pin
	TSPIxSCK	I/O	Clock input/output pin
Universal Asynchronous Receiver Transmitter (UART)	UTxRXD	Input	Data input
	UTxTXDA	Output	Data output pin A
	UTxTXDB	Output	Data output pin B
	UTxCTS_N	Input	Transmission control input pin
	UTxRTS_N	Output	Transmission request output pin
I^2C Interface (I^2C)	I2CxSDA	I/O	Data input/output pin
	I2CxSCL	I/O	Clock input/output pin

Not Recommended for New Design

Advanced Programmable Motor Control Circuit (A-PMD)	EMGx	Input	Emergency state detection input pin
	OVVx	Input	Over voltage detection input
	UOx	Output	U-phase output pin
	VOx	Output	V-phase output pin
	WOx	Output	W-phase output pin
	XOx	Output	X-phase output pin
	YOx	Output	Y-phase output pin
	ZOx	Output	Z-phase output pin
	PMDxDBG	Output	PMD Operation Status output pin
Advanced Encoder Input Circuit (A-ENC)	ENCxA	Input	Encoder input A
	ENCxB	Input	Encoder input B
	ENCxZ	Input	Encoder input Z
Analog to Digital Converter (ADC)	AINAx	Input	Analog input pin
Digital to Analog Converter (DAC)	DACx	Output	DAC output pin
Trigger input	TRGINx	Input	External trigger input pin
Remote control signal preprocessor (RMC)	RXINx	Input	Remote Signaling Data input pin
Real Time clock (RTC)	RTCOUT	Output	1Hz clock output pin

Note: “x” means channel number, unit number, or interrupt number.

Not Recommended for New Design

4.1.2. Debug Pins

Table 4.2 Debug pin names and their function

Debug Port	Pin name	Input or Output	Function
JTAG	TMS	Input	JTAG test mode selection input pin
	TCK	Input	JTAG serial clock input pin
	TDO	Output	JTAG serial data output pin
	TDI	Input	JTAG serial data input pin
	TRST_N	Input	JTAG test reset input pin
SW	SWDIO	I/O	Serial wire data input/output pin
	SWCLK	Input	Serial wire clock input pin
	SWV	Output	Serial wire viewer output pin
TRACE	TRACECLK	Output	Trace clock output pin
	TRACEDATA0	Output	Trace data output pin 0
	TRACEDATA1	Output	Trace data output pin 1
	TRACEDATA2	Output	Trace data output pin 2
	TRACEDATA3	Output	Trace data output pin 3

Not Recommended for New Design

4.1.3. Control Pins

Table 4.3 Control pin names and their function

	Pin name	Input or Output	Function
Control Pin	X1	Input	High Speed oscillator connection pin
	X2	Output	High Speed oscillator connection pin
	XT1	Input	Low Speed oscillator connection pin
	XT2	Output	Low Speed oscillator connection pin
	EHCLKIN	Input	External High speed Clock input pin
	BOOT_N	Input	BOOT mode control pin The BOOT mode control pin is sampled on the rising edge of the RESET_N input. It's not sampled by internal Reset factor. If the BOOT mode control pin is "Low" level, the MCU enters the single-boot mode. If it is "High", the MCU enters the single-chip mode. For details, refer to "Flash Memory" reference manual.
	RESET_N	Input	Reset signal input pin
	MODE	Input	Mode pin This pin must be fixed to "Low" level.

4.1.4. Power Supply Pins

Table 4.4 Power supply pin names and their function

	Pin name	Function
Power Supply	DVDD5A (Note 1) DVDD5B (Note 1)	Power supply pin for digital DVDD5A/B supplies the power to the following pins: PA to PC, PG2 to PG7, PH to PV, MODE, RESET_N, BOOT_N A power supply is supplied to an oscillating circuit from a built-in regulator. X1,X2,XT1,XT2
	DVSSA (Note 2) DVSSB (Note 2)	GND pin for digital
	REGOUT1 (Note 3)	Capacitor for a regulator connection pin (Note 4)
	REGOUT2 (Note 3)	Capacitor for a regulator connection pin (Note 4)
	AVDD5	Power supply pin and reference power pin (VREFH) for analog are combination pins. AVDD5 supplies the power to the following pins: PD, PE, PF, PG0 to1
	AVSS	GND pin for analog, reference GND (VREFL) for analog are combination pins.

Note1: Apply the voltage to DVDD5Aand DVDD5B at the same potential except the case that the pins are not provided.

Note2: Apply the external voltage to DVSSA and DVSSB at the same potential except the case that the pins are not provided.

Note3: For REGOUT1 and REGOUT2, do not cause a short circuit with DVDD5A, DVDD5B; or DVSSA, DVSSB.

Note4: For the capacitor value, refer to the "Electrical Characteristics"

Not Recommended for New Design

4.1.5. Capacitors between power supply pins

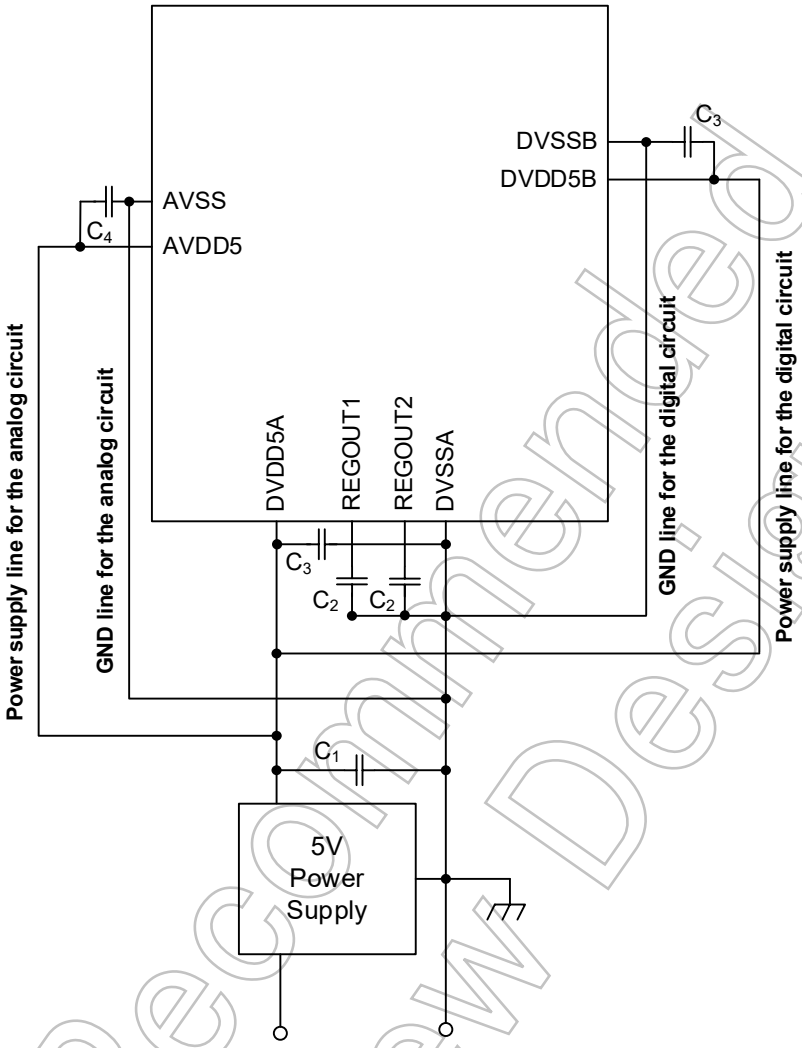


Figure 4.1 Capacitors for power supply pins connection circuit

Note1: 5V power supply output capacitor (C_1: min 1 µF) must be placed on the shortest distance from the output pin of 5V power supply. Ceramic capacitor recommended for C_1.

Note2: Bypass capacitor must be placed between the 5V power supply and GND near each MCU power supply pin.(C_3,C_4:0.01 to 0.1µF)

Note3: Power stabilizing Capacitors of REGOUT1 and REGOUT2 for built-in regulators must be the same capacity(C_2:4.7µF), and ceramic capacitor recommended for C_2. They must be placed on the shortest distance from DVSSA.

Note4: Separate the analog power supply line and the digital power supply line near the 5V power supply output pin in order to reduce noise mixing into the analog circuit from the digital power supply.

Note5: When inserting a filter circuit or pull-up / down resistor at the input / output pin of the analog power supply system to reduce noise mixing from the peripheral circuit to the analog circuit, connect the components that make up these circuits to the analog power supply line.

Note6: Do not separate the power supply line and the GND line from each other in order to reduce high frequency noise etc, received by the power supply line, the GND line, and the loop circuit of the capacitor.

Not Recommended for New Design

4.2. Functional Pin and Ports Assignment (Pin Number)

Following table shows a pin number of the port assignment and each product which were seen from the functional pin.

"-" means that it does not have a pin or there is no assignment of a function.

Table 4.5 Signal connection List(1/13)

Combination functional pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
UT0TXDA	PA1	27	23	17	19	16	14
	PA2	26	22	16	18	15	13
	PM1	35	31	24	26	19	-
	PM2	34	30	23	25	18	-
UT0TXDB	PA0	28	24	18	20	17	15
	PM0	36	32	25	27	20	16
UT0RXD	PA2	26	22	16	18	15	13
	PA1	27	23	17	19	16	14
	PM2	34	30	23	25	18	-
	PM1	35	31	24	26	19	-
UT0CTS_N	PM3	33	29	22	24	-	-
	PM4	32	28	21	23	-	-
UT0RTS_N	PM4	32	28	21	23	-	-
	PM3	33	29	22	24	-	-
Combination functional pin name	**Port Name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
UT1TXDA	PJ1	105	92	72	74	57	45
	PJ2	106	93	73	75	58	46
	PK1	111	98	78	80	63	51
	PK2	112	99	79	81	64	52
UT1TXDB	PJ0	104	91	71	73	56	44
	PK0	110	97	77	79	62	50
UT1RXD	PJ2	106	93	73	75	58	46
	PJ1	105	92	72	74	57	45
	PK2	112	99	79	81	64	52
	PK1	111	98	78	80	63	51
UT1CTS_N	PJ3	107	94	74	76	59	47
	PJ4	108	95	75	77	60	48
	PK3	113	100	80	82	65	53
	PK4	114	101	81	83	66	54
UT1RTS_N	PJ4	108	95	75	77	60	48
	PJ3	107	94	74	76	59	47
	PK4	114	101	81	83	66	54
	PK3	113	100	80	82	65	53

Not Recommended for New Design

Table 4.6 Signal connection List(2/13)

Combination functional pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
UT2TXDA	PB2	39	35	28	30	23	19
	PB3	40	36	29	31	24	20
	PL0	47	41	34	36	26	21
	PL1	48	42	35	37	27	22
UT2RXD	PB3	40	36	29	31	24	20
	PB2	39	35	28	30	23	19
	PL1	48	42	35	37	27	22
	PL0	47	41	34	36	26	21
UT2CTS_N	PB4	41	37	30	32	25	-
	PB5	42	38	31	33	-	-
	PL2	49	43	36	38	28	23
	PL3	50	44	37	39	29	24
UT2RTS_N	PB5	42	38	31	33	-	-
	PB4	41	37	30	32	25	-
	PL3	50	44	37	39	29	24
	PL2	49	43	36	38	28	23
Combination functional pin name	**Port Name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
UT3TXDA	PA7	21	17	11	13	10	10
	PA6	22	18	12	14	11	11
	PG3	16	12	-	-	-	-
	PG2	15	11	-	-	-	-
UT3TXDB	PG4	17	13	-	-	-	-
UT3RXD	PA6	22	18	12	14	11	11
	PA7	21	17	11	13	10	10
	PG2	15	11	-	-	-	-
	PG3	16	12	-	-	-	-

Not Recommended for New Design

Table 4.7 Signal connection List (3/13)

Combination functional pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
UT4TXDA	PC3	86	73	57	59	47	38
	PC4	87	74	58	60	48	39
	PV6	81	-	-	-	-	-
	PV7	82	-	-	-	-	-
UT4TXDB	PC2	85	72	56	58	46	-
	PV5	80	-	-	-	-	-
UT4RXD	PC4	87	74	58	60	48	39
	PC3	86	73	57	59	47	38
	PV7	82	-	-	-	-	-
	PV6	81	-	-	-	-	-
UT4CTS_N	PC5	88	75	59	61	49	-
	PC6	89	76	60	62	50	-
UT4RTS_N	PC6	89	76	60	62	50	-
	PC5	88	75	59	61	49	-
Combination functional pin name	**Port Name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
UT5TXDA	PN3	100	87	67	69	52	41
	PN2	101	88	68	70	53	42
UT5TXDB	PN4	99	86	66	68	51	40
UT5RXD	PN2	101	88	68	70	53	42
	PN3	100	87	67	69	52	41
UT5CTS_N	PN1	102	89	69	71	54	43
	PN0	103	90	70	72	55	-
UT5RTS_N	PN0	103	90	70	72	55	-
	PN1	102	89	69	71	54	43
Combination functional pin name	**Port Name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
I2C0SCL	PC0	83	70	54	56	44	36
I2C0SDA	PC1	84	71	55	57	45	37
I2C1SCL	PA4	24	20	14	16	13	-
I2C1SDA	PA5	23	19	13	15	12	-
I2C2SCL	PL0	47	41	34	36	26	21
I2C2SDA	PL1	48	42	35	37	27	22
I2C3SCL	PT1	61	51	-	-	-	-
I2C3SDA	PT0	62	52	-	-	-	-

Not Recommended for New Design

Table 4.8 Signal connection List (4/13)

Combination functional pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
TSPI0SCK	PM0	36	32	25	27	20	16
	PA0	28	24	18	20	17	15
TSPI0TXD	PM1	35	31	24	26	19	-
	PA1	27	23	17	19	16	14
TSPI0RXD	PM2	34	30	23	25	18	-
	PA2	26	22	16	18	15	13
TSPI0CS0	PM3	33	29	22	24	-	-
	PA3	25	21	15	17	14	12
TSPI0CS1	PM4	32	28	21	23	-	-
	PA4	24	20	14	16	13	-
TSPI0CSIN	PM3	33	29	22	24	-	-
	PA3	25	21	15	17	14	12
Combination functional pin name	**Port Name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
TSPI1SCK	PB2	39	35	28	30	23	-
TSPI1TXD	PB3	40	36	29	31	24	-
TSPI1RXD	PB4	41	37	30	32	25	-
TSPI1CS0	PB5	42	38	31	33	-	-
TSPI1CS1	PB6	43	39	32	34	-	-
TSPI1CSIN	PB5	42	38	31	33	-	-
Combination functional pin name	**Port Name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
TSPI2SCK	PP0	63	53	41	43	31	-
	PT2	60	50	-	-	-	-
TSPI2TXD	PP1	64	54	42	44	32	-
	PT3	59	49	-	-	-	-
TSPI2RXD	PP2	65	55	43	45	33	-
	PT4	58	-	-	-	-	-
TSPI2CS0	PT1	61	51	-	-	-	-
TSPI2CS1	PT0	62	52	-	-	-	-
TSPI2CSIN	PT1	61	51	-	-	-	-

Not Recommended for New Design

Table 4.9 Signal Connection List (5/13)

Combination functional pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
TSPI3SCK	PP5	120	107	87	89	72	-
TSPI3TXD	PP4	119	106	86	88	71	-
TSPI3RXD	PP3	118	105	85	87	70	-
TSPI3CS0	PP6	121	108	88	90	73	-
TSPI3CS1	PP7	122	109	89	91	-	-
TSPI3CSIN	PP6	121	108	88	90	73	-
Combination functional pin name	**Port Name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
TSPI4SCK	PH4	76	66	-	-	-	-
TSPI4TXD	PH5	77	67	-	-	-	-
TSPI4RXD	PH6	78	68	-	-	-	-
Combination functional pin name	**Port Name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
T32A00OUTA	PA0	28	24	18	20	17	15
	PM0	36	32	25	27	20	16
T32A00OUTB	PA3	25	21	15	17	14	12
	PM3	33	29	22	24	-	-
T32A00OUTC	PA0	28	24	18	20	17	15
	PM0	36	32	25	27	20	16
T32A00INA0	PA1	27	23	17	19	16	14
	PM1	35	31	24	26	19	-
T32A00INA1	PA2	26	22	16	18	15	13
	PM2	34	30	23	25	18	-
T32A00INB0	PA4	24	20	14	16	13	-
	PM4	32	28	21	23	-	-
T32A00INB1	PA5	23	19	13	15	12	-
	PM5	31	27	20	22	-	-
T32A00INC0	PA1	27	23	17	19	16	14
	PM1	35	31	24	26	19	-
T32A00INC1	PA2	26	22	16	18	15	13
	PM2	34	30	23	25	18	-

Not Recommended for New Design

Table 4.10 Signal connection List (6/13)

Combination functional pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
T32A01OUTA	PB0	37	33	26	28	21	17
	PP0	63	53	41	43	31	-
T32A01OUTB	PB3	40	36	29	31	24	20
T32A01OUTC	PB0	37	33	26	28	21	17
	PP0	63	53	41	43	31	-
T32A01INA0	PB1	38	34	27	29	22	18
	PP1	64	54	42	44	32	-
T32A01INA1	PB2	39	35	28	30	23	19
	PP2	65	55	43	45	33	-
T32A01INB0	PB4	41	37	30	32	25	-
T32A01INB1	PB5	42	38	31	33	-	-
T32A01INC0	PB1	38	34	27	29	22	18
	PP1	64	54	42	44	32	-
T32A01INC1	PB2	39	35	28	30	23	19
	PP2	65	55	43	45	33	-
Combination functional pin name	**Port Name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
T32A02OUTA	PC0	83	70	54	56	44	36
	PR0	90	77	61	63	-	-
T32A02OUTB	PC3	86	73	57	59	47	38
T32A02OUTC	PC0	83	70	54	56	44	36
	PR0	90	77	61	63	-	-
T32A02INA0	PC1	84	71	55	57	45	37
	PR1	91	78	62	64	-	-
T32A02INA1	PC2	85	72	56	58	46	-
	PR2	92	79	63	65	-	-
T32A02INB0	PC4	87	74	58	60	48	39
T32A02INB1	PC5	88	75	59	61	49	-
T32A02INC0	PC1	84	71	55	57	45	37
	PR1	91	78	62	64	-	-
T32A02INC1	PC2	85	72	56	58	46	-
	PR2	92	79	63	65	-	-

Not Recommended for New Design

Table 4.11 Signal connection List (7/13)

Combination functional pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
T32A03OUTB	PJ3	107	94	74	76	59	47
T32A03OUTA	PJ0	104	91	71	73	56	44
T32A03OUTC	PJ0	104	91	71	73	56	44
T32A03INA0	PJ1	105	92	72	74	57	45
T32A03INA1	PJ2	106	93	73	75	58	46
T32A03INB0	PJ4	108	95	75	77	60	48
T32A03INB1	PJ5	109	96	76	78	61	49
T32A03INC0	PJ1	105	92	72	74	57	45
T32A03INC1	PJ2	106	93	73	75	58	46
Combination functional pin name	**Port Name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
T32A04OUTA	PK2	112	99	79	81	64	52
T32A04INA0	PK3	113	100	80	82	65	53
T32A04INA1	PK4	114	101	81	83	66	54
T32A04OUTB	PK5	115	102	82	84	67	55
T32A04INB0	PK6	116	103	83	85	68	56
T32A04INB1	PK7	117	104	84	86	69	-
T32A04OUTC	PK2	112	99	79	81	64	52
T32A04INC0	PK3	113	100	80	82	65	53
T32A04INC1	PK4	114	101	81	83	66	54
Combination functional pin name	**Port Name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
T32A05OUTA	PN0	103	90	70	72	55	-
T32A05INA0	PN1	102	89	69	71	54	43
T32A05INA1	PN2	101	88	68	70	53	42
T32A05OUTB	PN3	100	87	67	69	52	41
T32A05INB0	PN4	99	86	66	68	51	40
T32A05INB1	PN5	98	85	65	67	-	-
T32A05OUTC	PN0	103	90	70	72	55	-
T32A05INC0	PN1	102	89	69	71	54	43
T32A05INC1	PN2	101	88	68	70	53	42

Not Recommended for New Design

Table 4.12 Signal connection List (8/13)

Combination functional pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
T32A06OUTA	PL5	52	46	39	41	-	-
	PT5	57	-	-	-	-	-
T32A06INA0	PL6	53	47	40	42	-	-
	PT6	56	-	-	-	-	-
T32A06INA1	PL7	54	48	-	-	-	-
	PT7	55	-	-	-	-	-
T32A06OUTB	PL2	49	43	36	38	28	23
	PT2	60	50	-	-	-	-
T32A06INB0	PL3	50	44	37	39	29	24
	PT3	59	49	-	-	-	-
T32A06INB1	PL4	51	45	38	40	30	25
	PT4	58	-	-	-	-	-
T32A06OUTC	PL5	52	46	39	41	-	-
	PT5	57	-	-	-	-	-
T32A06INC0	PL6	53	47	40	42	-	-
	PT6	56	-	-	-	-	-
T32A06INC1	PL7	54	48	-	-	-	-
	PT7	55	-	-	-	-	-
Combination functional pin name	**Port Name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
T32A07OUTA	PG2	15	11	-	-	-	-
T32A07INA0	PG3	16	12	-	-	-	-
T32A07INA1	PG4	17	13	-	-	-	-
T32A07OUTB	PG5	18	14	-	-	-	-
T32A07INB0	PG6	19	15	-	-	-	-
T32A07INB1	PG7	20	16	-	-	-	-
T32A07OUTC	PG2	15	11	-	-	-	-
T32A07INC0	PG3	16	12	-	-	-	-
T32A07INC1	PG4	17	13	-	-	-	-

Not Recommended for New Design

Table 4.13 Signal connection List (9/13)

Combination functional pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
AINA00	PD0	6	6	6	8	5	5
AINA01	PD1	5	5	5	7	4	4
AINA02	PD2	4	4	4	6	3	3
AINA03	PD3	3	3	3	5	-	-
AINA04	PE0	2	2	2	4	2	2
AINA05	PE1	1	1	1	3	1	1
AINA06	PE2	144	128	100	2	80	64
AINA07	PE3	143	127	99	1	79	63
AINA08	PE4	142	126	98	100	78	62
AINA09	PE5	141	125	97	99	77	61
AINA10	PE6	140	124	96	98	76	60
AINA11	PF0	139	123	95	97	-	-
AINA12	PF1	138	122	94	96	-	-
AINA13	PF2	137	121	-	-	-	-
AINA14	PF3	136	120	-	-	-	-
AINA15	PF4	135	119	-	-	-	-
AINA16	PF5	134	118	-	-	-	-
AINA17	PF6	133	117	-	-	-	-
AINA18	PF7	132	116	-	-	-	-
AINA19	PD4	131	-	-	-	-	-
AINA20	PD5	130	-	-	-	-	-
Combination functional pin name	**Port Name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
DAC0	PG0	9	9	9	11	8	8
DAC1	PG1	10	10	10	12	9	9

Not Recommended for New Design

Table 4.14 Signal connection List (10/13)

Combination functional pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
INT00	PC0	83	70	54	56	44	36
INT01	PC1	84	71	55	57	45	37
INT02	PC2	85	72	56	58	46	-
INT03	PB1	38	34	27	29	22	18
INT04	PJ4	108	95	75	77	60	48
INT05	PK1	111	98	78	80	63	51
INT06	PH3	74	64	52	54	42	34
INT07	PA6	22	18	12	14	11	11
INT08	PL3	50	44	37	39	29	24
INT09	PM2	34	30	23	25	18	-
INT10	PN3	100	87	67	69	52	41
INT11	PA7	21	17	11	13	10	10
INT12	PL4	51	45	38	40	30	25
INT13	PK7	117	104	84	86	69	-
INT14	PP3	118	105	85	87	70	57
INT15	PM6	30	26	19	21	-	-
INT16	PB7	44	40	33	35	-	-
INT17	PV2	125	112	92	94	-	-
INT18	PV3	126	113	93	95	-	-
INT19	PH4	76	66	-	-	-	-
INT20	PH5	77	67	-	-	-	-
INT21	PH6	78	68	-	-	-	-
INT22	PH7	79	69	-	-	-	-
INT23	PT0	62	52	-	-	-	-
INT24	PT1	61	51	-	-	-	-
INT25	PT2	60	50	-	-	-	-
INT26	PT3	59	49	-	-	-	-
INT27	PG2	15	11	-	-	-	-
INT28	PG3	16	12	-	-	-	-
INT29	PT7	55	-	-	-	-	-
INT30	PU0	45	-	-	-	-	-
INT31	PU1	46	-	-	-	-	-

Not Recommended for New Design

Table 4.15 Signal connection List (11/13)

Combination functional pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
UO0	PJ0	104	91	71	73	56	44
XO0	PJ1	105	92	72	74	57	45
VO0	PJ2	106	93	73	75	58	46
YO0	PJ3	107	94	74	76	59	47
WO0	PJ4	108	95	75	77	60	48
ZO0	PJ5	109	96	76	78	61	49
EMG0	PK0	110	97	77	79	62	50
OVV0	PK1	111	98	78	80	63	51
ENC0A	PA0	28	24	18	20	17	15
ENC0B	PA1	27	23	17	19	16	14
ENC0Z	PA2	26	22	16	18	15	13
PMD0DBG	PP6	121	108	88	90	73	-
Combination functional pin name	**Port Name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
SCOUT	PB0	37	33	26	28	21	17
Combination functional pin name	**Port Name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
TRGIN0	PB1	38	34	27	29	22	18
TRGIN1	PA3	25	21	15	17	14	12
TRGIN2	PN3	100	87	67	69	52	41
Combination functional pin name	**Port Name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
RXIN0	PB1	38	34	27	29	22	18
Combination functional pin name	**Port Name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
RTCOUT	PC2	85	72	56	58	46	-

Not Recommended for New Design

Table 4.16 Signal connection List (12/13)

Combination functional pin name	Port Name	M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
TMS	PL4	51	45	38	40	30	25
TCK	PL3	50	44	37	39	29	24
TDO	PL2	49	43	36	38	28	23
TDI	PL1	48	42	35	37	27	22
TRST_N	PL0	47	41	34	36	26	21
SWDIO	PL4	51	45	38	40	30	25
SWCLK	PL3	50	44	37	39	29	24
SWV	PL2	49	43	36	38	28	23
TRACECLK	PM0	36	32	25	27	20	-
TRACEDATA0	PM1	35	31	24	26	19	-
TRACEDATA1	PM2	34	30	23	25	18	-
TRACEDATA2	PM3	33	29	22	24	-	-
TRACEDATA3	PM4	32	28	21	23	-	-
Combination functional pin name	**Port Name**	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
X1	PH0	70	60	48	50	38	30
X2	PH1	71	61	49	51	39	31
XT1	PH2	73	63	51	53	41	33
XT2	PH3	74	64	52	54	42	34
EHCLKIN	PH0	70	60	48	50	38	30
BOOT_N	PB0	37	33	26	28	21	17

Not Recommended for New Design

Table 4.17 Signal connection List (13/13)

Port Name	M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	M3HL (LQFP64)
PM7	29	25	-	-	-	-
PR3	93	80	64	66	-	-
PR4	94	81	-	-	-	-
PR5	95	82	-	-	-	-
PR6	96	83	-	-	-	-
PR7	97	84	-	-	-	-
PU2	14	-	-	-	-	-
PU3	13	-	-	-	-	-
PU4	12	-	-	-	-	-
PU5	11	-	-	-	-	-
PV0	123	110	90	92	74	58
PV1	124	111	91	93	75	59
PV4	127	-	-	-	-	-
Pin name	**M3HQ (LQFP144)**	**M3HP (LQFP128)**	**M3HN (LQFP100)**	**M3HN (QFP100)**	**M3HM (LQFP80)**	**M3HL (LQFP64)**
RESET_N	72	62	50	52	40	32
MODE	75	65	53	55	43	35
AVDD5	7	7	7	9	6	6
AVSS	8	8	8	10	7	7
DVDD5A	66	56	44	46	34	26
DVDD5B	128	114	-	-	-	-
DVSSA	69	59	47	49	37	29
DVSSB	129	115	-	-	-	-
REGOUT1	68	58	46	47	36	28
REGOUT2	67	57	45	48	35	27

Not Recommended for New Design

4.3. Ports

The symbols of each table of the port have the following meanings.

The right-hand side of the port shows specification with the symbol.

The symbols have the following meanings.

- Input/Output: Input and/or Output of Port
  Input: Input port
  Output: Output port
  I/O: Input/Output port

- PU/PD: Programmable pull-up/pull-down
  PU: Programmable pull-up is selectable
  PD: Programmable pull-down is selectable

- OD: Programmable open-drain output
  Yes: Support
  No: Non support

- 5V_T: 5V-tolerant
  Yes: Support
  N/A: Not available

- SMT/CMOS: Input gate
  SMT: Schmitt trigger input
  CMOS: CMOS input

- Under Reset: Port state under Reset
  Hi-Z: High impedance
  PU: Pull-up
  PD: Pull-down

- After Reset: Port state after Reset
  Hi-Z: High impedance
  PU: Pull-up
  PD: Pull-down

Not Recommended for New Design

4.3.1. Port Specifications Table

Table 4.18 Port names, and specifications of Port A, B, C, D, E

Port Name	Input/Output	PU/PD	OD	5V_T	SMT/CMOS	Under Reset	After Reset
PA0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PA1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PA2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PA3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PA4	I/O	PU/PD	YES	YES	SMT	Hi-Z	Hi-Z
PA5	I/O	PU/PD	YES	YES	SMT	Hi-Z	Hi-Z
PA6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PA7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PB0	Output	PU/PD (Note)	YES	N/A	SMT	Hi-Z (Note)	Hi-Z
PB1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PB2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PB3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PB4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PB5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PB6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PB7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PC0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PC1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PC2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PC3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PC4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PC5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PC6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PD0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PD1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PD2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PD3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PD4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PD5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PE0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PE1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PE2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PE3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PE4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PE5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PE6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z

Note: combination with BOOT_N. When RESET_N=0, Pull-up resistor is enabled.
When RESET_N=1, the pin state is Hi-Z with internal reset.

Not Recommended for New Design

Table 4.19 Port names, and specifications of Port F, G, H, J, K

Port Name	Input/Output	PU/PD	OD	5V_T	SMT/CMOS	Under Reset	After Reset
PF0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PF1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PF2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PF3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PF4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PF5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PF6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PF7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PG0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PG1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PG2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PG3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PG4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PG5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PG6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PG7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PH0	Input	PD	YES	N/A	SMT	Hi-Z	Hi-Z
PH1	Input	PD	YES	N/A	SMT	Hi-Z	Hi-Z
PH2	Input	PD	YES	N/A	SMT	Hi-Z	Hi-Z
PH3	Input	PD	YES	N/A	SMT	Hi-Z	Hi-Z
PH4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PH5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PH6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PH7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PJ0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PJ1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PJ2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PJ3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PJ4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PJ5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PK0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PK1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PK2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PK3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PK4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PK5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PK6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PK7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z

Not Recommended for New Design

Table 4.20 Port names, and specifications of Port L, M, N, P, R

Port Name	Input/Output	PU/PD	OD	5V_T	SMT/CMOS	Under Reset	After Reset
PL0	I/O	PU/PD	YES	N/A	SMT	PU(Note)	PU(Note)
PL1	I/O	PU/PD	YES	N/A	SMT	PU(Note)	PU(Note)
PL2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PL3	I/O	PU/PD	YES	N/A	SMT	PD(Note)	PD(Note)
PL4	I/O	PU/PD	YES	N/A	SMT	PU(Note)	PU(Note)
PL5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PL6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PL7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PM0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PM1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PM2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PM3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PM4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PM5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PM6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PM7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PN0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PN1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PN2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PN3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PN4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PN5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PP0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PP1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PP2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PP3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PP4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PP5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PP6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PP7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PR0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PR1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PR2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PR3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PR4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PR5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PR6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PR7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z

Note: It is assigned to a debugging pin in the state of the initial stage. PL4: TMS/SWDIO, PL3:TCK/SWCLK, PL2:TDO/SWV,PL1:TDI, PL0:TRST_N)

Not Recommended for New Design

Table 4.21 Port names, and specifications of Port T, U, V

PortName	Input/Output	PU/PD	OD	5V_T	SMT/CMOS	Under Reset	After Reset
PT0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PT1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PT2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PT3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PT4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PT5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PT6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PT7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PU0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PU1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PU2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PU3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PU4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PU5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PV0	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PV1	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PV2	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PV3	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PV4	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PV5	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PV6	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z
PV7	I/O	PU/PD	YES	N/A	SMT	Hi-Z	Hi-Z

Not Recommended for New Design

5. Functional Description and Operation Description

5.1. Reference Manuals

For more information on the product of TMPM3H Group(2), please refer to Reference Manuals below;

Table 5.1 Reference Manuals for TMPM3H Group(2)

Reference Manual	IP Symbol	Category
Port (TMPM3H Group(2))	PORT-M3H(2)	System
Memory Map (TMPM3H Group(2))	MMAP-M3H(2)	System
Exception (TMPM3H Group(2))	EXCEPT-M3H(2)	System
Clock Control and operation mode (TMPM3H Group(2))	CG-M3H(2)-D	System
Product Information (TMPM3H Group(2))	PINFO-M3H(2)	System
Power supply and Reset operation (TMPM3H Group(2))	RESET-M3H(2)	System
Flash Memory (512KB Code FLASH and 32KB Data FLASH)	FLASH512_32-A	Peripheral
Trimming Circuit	TRM-A	Peripheral
Oscillation Frequency Detector	OFD-A	Peripheral
Voltage Detection Circuit	LVD-A	Peripheral
Digital Noise Filter Circuit	DNF-A	Peripheral
Debug Interface	DEBUG-A	Peripheral
DMA Controller	DMAC-B	Peripheral
Universal Asynchronous Receiver Transmitter	UART-C	Peripheral
Serial Peripheral Interface	TSPI-B	Peripheral
I^2C interface	I2C-B	Peripheral
8-bit Digital to Analog Converter	DAC-A	Peripheral
12-bit Analog to Digital Converter	ADC-A	Peripheral
Comparator	COMP-B	Peripheral
Advanced Programmable Motor Control Circuit	A-PMD-B	Peripheral
Advanced Encoder Input Circuit	A-ENC-A	Peripheral
32-bit Timer Event Counter	T32A-B	Peripheral
Real Time Clock	RTC-A	Peripheral
Clock Selective Watchdog Timer	SIWDT-A	Peripheral
Remote control signal preprocessor	RMC-A	Peripheral
CRC calculation circuit	CRC-A	Peripheral
RAM Parity	RAMP-A	Peripheral

Not Recommended for New Design

5.2. Processor Core

The TMPM3H Group(2) incorporates a high-performance 32-bit processor core (Arm Cortex-M3 core).
For the operation of the processor core, refer to the Arm documentation set of the Arm "Cortex-M" series processor. This section explains the product-specific information.

5.2.1. Core Information

The Cortex-M3 core revision used in the TMPM3H Group(2) is shown as below:
For details of the CPU core and the architecture, refer to the documentation of the Arm in the following URL:
http: //infocenter.arm.com/help/index.jsp

Table 5.2 Core revision

Group name	Core revision
TMPM3H Group(2)	r2p1

5.2.2. Configurable Options

In the Cortex-M3 core, some blocks can be selected to implement. The following table shows the configurations of the TMPM3H Group(2).

Table 5.3 Configurable options and their implementations

Configurable option	Implementation
FWB	Literal comparator: 2 Instruction comparator: 6
DWT	Comparator: 4
ITM	Available
MPU	Available
ETM	Available
AHB-AP	Available
AHB trace macro cell interface	Not available
TPIU	Available
WIC	Not available
Debug port	JTAG/serial wire
Bit band	Available
Sequential control of AHB	Not available

Not Recommended for New Design

5.3. Clock Control and Operation mode (CG)

The CG selects a clock gear ratio and the prescaler clock, or warm up time of the oscillator.

There are NORMAL mode and low-power consumption mode as operation modes. Power consumption can be decreased by mode transition.

The outline of the clock control circuit is as follows:

- Internal high-speed oscillation circuit: 10MHz
- Selectable from the external high-speed oscillation circuit or internal high-speed oscillation circuit.
- PLL (Clock Multiplication Circuit): Capable of 80 MHz output by changing the multiplication ratio according to the frequency of the high-speed oscillation circuit
- Clock gear: The high-speed clock can be divided by 1, 2, 4, 8, or 16 and the clock is used as the system clock (fsys).
- Low-power consumption mode:

  IDLE: Only the CPU is stopped in this mode. Each peripheral circuit can enable or disable operation in the IDLE mode.

  STOP1: Except some peripheral circuits, all the internal circuits including the internal oscillator are brought to a stop in STOP1 mode. External low frequency oscillator can oscillate. RTC and RMC can be used.

  STOP2: This mode halts voltage supply, retaining some peripheral circuits operation. External low frequency oscillator can oscillate (RTC can be used.), and wake-up by I^2C slave address matching.

5.4. Flash Memory (Code FLASH, Data FLASH)

The cord flash stores instruction code, and CPU read instruction code and executes. The data flash stores data, and even if a power supply is off, data can be kept.

It has the dual mode that possible to write and erase a data flash while executing an order by a code flash, and it's also possible to continue executing an application program during writing or erasing data flash.

It has protection function which prohibits write or erase by the block unit and it has the security function which prohibits the reading of the program code by the 3rd person.

Not Recommended for New Design

5.5. Oscillation Circuit

External High Speed Oscillator (EHOSC): Connect crystal resonator or ceramic resonator to terminals. Use clock source for System clock.
External Low Speed Oscillator (ELOSC): Connect crystal resonator (32.768 kHz) to terminals. Use clock source for Real Time Clock or Power consumption mode.
Internal High Speed Oscillator 1(IHOSC1): Oscillation frequency is 10MHz. Use clock source for System clock.
Internal High Speed Oscillator 2(IHOSC2): Oscillation frequency is 10MHz. Use clock source for OFD and SIWDT.

Table 5.4 Built-in Oscillator

	M3HQ	M3HP	M3HN	M3HM	M3HL
EHOSC	✓	✓	✓	✓	✓
ELOSC	✓	✓	✓	✓	✓
IHOSC1	✓	✓	✓	✓	✓
IHOSC2	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.6. Trimming Circuit (TRM)

The trimming function can adjust the frequency of the internal high-speed oscillator1 (IHOSC1).

Table 5.5 Built-in TRM

	M3HQ	M3HP	M3HN	M3HM	M3HL
TRM	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.7. Oscillation Frequency Detector (OFD)

The oscillation frequency detector (OFD) is a function that detects an abnormal state of the clock. It measures the external high-speed oscillation (f_{EHOSC}) or high-speed clock (fc) based on the internal reference clock (f_{IHOSC2}). If an oscillation or clock frequency is out of the specified range, a reset signal occurs.
The upper limit and the lower limit of detection frequency ranges can be specified.

Table 5.6 Built-in OFD

	M3HQ	M3HP	M3HN	M3HM	M3HL
OFD	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

Not Recommended for New Design

5.8. Voltage Detection Circuit (LVD)

The LVD is a peripheral function that detects whether a power supply voltage is lower or higher than the preset voltage. When a low voltage or higher voltage than the preset voltage is detected, the LVD generates an interrupt request or reset the MCU.

Setting voltage can be chosen from eight kinds. LVD is set to enable from the Reset state at the Power-on.

Table 5.7 Built-in LVD

	M3HQ	M3HP	M3HN	M3HM	M3HL
LVD	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.9. Digital Noise Filter (DNF)

The digital noise canceler circuit can eliminate the noise of input signals from external interrupt pins at a certain range. The noise of the High level / Low level input of the external interrupt signal INTx is removed.

Table 5.8 Number of External Interrupts (Built-in DNF)

	M3HQ	M3HP	M3HN	M3HM	M3HL
Number of External Interrupt	32	29	19	15	12

Not Recommended for New Design

5.10. Debug Interface (DEBUG)

TMPM3H Group(2) contains Interface for connecting debug tool, which is the Serial Wire Debug Port (SWCLK, SWDIO) and the JTAG Debug Port (TDI, TDO, TMS, TCK, TRST_N). These are connected with the Debug tool and used for program development. And also it contains the trace clock (TRACECLK) and data output (TRACEDATA 0 to 3) to reduce the Debug Process.

Table 5.9 Built-in Debug Interface

Debug Pin (Signal Name)	Port	M3HQ	M3HP	M3HN	M3HM	M3HL
SWDIO	PL4	✓	✓	✓	✓	✓
TMS						
SWCLK	PL3	✓	✓	✓	✓	✓
TCK						
SWV	PL2	✓	✓	✓	✓	✓
TDO						
TDI	PL1	✓	✓	✓	✓	✓
TRST_N	PL0	✓	✓	✓	✓	✓
TRACECLK	PM0	✓	✓	✓	✓	-
TRACEDATA0	PM1	✓	✓	✓	✓	-
TRACEDATA1	PM2	✓	✓	✓	✓	-
TRACEDATA2	PM3	✓	✓	✓	-	-
TRACEDATA3	PM4	✓	✓	✓	-	-

Note: ✓: Available, -: N/A

Not Recommended for New Design

5.11. DMA Controller (DMAC)

The DMAC is the peripheral function to move the data between peripheral functions and the memory, or between memories. These operations are performed separately from the CPU control; thus, the Load of CPU can greatly be reduced by using the DMA.

TMPM3H Group(2) have two units DMA controller(DMAC), DMAC has the 32 channels DMA requests per unit.

Table 5.10 Built-in DMAC

UNIT	M3HQ	M3HP	M3HN	M3HM	M3HL
UNIT A	✓	✓	✓	✓	✓
UNIT B	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.12. Universal Asynchronous Receiver Transmitter (UART)

The UART is asynchronous serial communication function. It can choose the data length of 7, 8 or 9bits, parity existence, and a STOP bit length function. Moreover, selection of the MSB first / LSB first and reversal of data polarity can be performed and Terminal exchanged of TXD/RXD can be performed in a Port setting.

The FIFO buffer supports data communication on 8-stage at transmission, and on 8-stage at reception.

The telecommunication control by CTS/RTS and half clock mode are supported.

Table 5.11 Built-in UART

Channel	M3HQ	M3HP	M3HN	M3HM	M3HL
Channel 0	✓	✓	✓	✓	✓
Channel 1	✓	✓	✓	✓	✓
Channel 2	✓	✓	✓	✓	✓
Channel 3	✓	✓	✓	✓	✓
Channel 4	✓	✓	✓	✓	✓
Channel 5	✓	✓	✓	✓	✓

Note1: ✓: Available, -: N/A

Note2: External pins are not the same by product. Please refer to section “2 Pin Assignment”.

Not Recommended for New Design

5.13. Serial Peripheral Interface (TSPI)

The TSPI supports two communication methods and enables to perform serial communication between other devices at high speed. The SPI bus type, which uses a CS (Chip Select) signal at communications, and SIO bus type, which does not use a CS signal at communications can be selected.

The data length can be changed from 7 bits (with a parity bit) to 32 bits (without a parity bit) in the unit of one bit. There are an 8-stage 16-bit FIFO for reception and transmission, each. The TSPI supports the master and slave communications.

Table 5.12 Built-in TSPI

Channel	M3HQ	M3HP	M3HN	M3HM	M3HL
Channel 0	✓	✓	✓	✓	✓
Channel 1	✓	✓	✓	✓	-
Channel 2	✓	✓	✓	✓	-
Channel 3	✓	✓	✓	✓	-
Channel 4	✓	✓	-	-	-

Note1: ✓: Available, -: N/A

Note2: External pins are not the same by product. Please refer to section "2 Pin Assignment ".

5.14. I²C Interface (I²C)

I²C is two-wire bi-directional serial communications between Master and Slave device. The mode in which two or more masters can exist on the same bus called a multi-master is supported. It supports STD mode (Max 100kHz), Fast mode (Max 400kHz).

Channel 0 provides the address match wake up function. Depending on the setting, the MCU can receive data even in low power consumption mode including IDLE, STOP1, or STOP2 mode and can return to normal mode by the Slave address match wake up function. (Note2)

Table 5.13 Built-in I²C

Channel	M3HQ	M3HP	M3HN	M3HM	M3HL
Channel 0 (Note2)	✓	✓	✓	✓	✓
Channel 1	✓	✓	✓	✓	-
Channel 2	✓	✓	✓	✓	✓
Channel 3	✓	✓	-	-	-

Note1: ✓: Available, -: N/A

Note2: The address match wake up function is available.

Not Recommended for New Design

5.15. 8-bit Digital to Analog Converter (DAC)

The DAC is an R-2R type 8-bit digital to analog converter that can output the specified voltage. A buffer amplifier is not incorporated.

Channel0 (DAC0) can be used also as the reference voltage (VREFC) of a comparator (COMP).

Table 5.14 Built-in DAC

Channel	M3HQ	M3HP	M3HN	M3HM	M3HL
Channel 0	✓	✓	✓	✓	✓
Channel 1	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.16. 12-bit Analog to Digital Converter (ADC)

The ADC is a successive-approximation analog to digital converter. It supports maximum 21 analog inputs. The combination of a conversion result register and analog input can be programmed in each startup trigger of AD conversion. A startup trigger for analog to digital conversion can be selected from software or peripheral functions (A-PMD trigger outputs, timer/event counter outputs, port inputs).

A motor is easily controllable by cooperating especially with A-PMD.

The monitor function is also available and it can generate an interrupt request when the compare conditions are matched.

Table 5.15 Built-in ADC

UNIT	M3HQ	M3HP	M3HN	M3HM	M3HL
UNIT A	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

Table 5.16 Number of analog inputs for ADC

	M3HQ	M3HP	M3HN	M3HM	M3HL
Analog Inputs Pin count	21	19	13	10	10

5.17. Comparator (COMP)

The comparator compared an Analog Input value to Output value of Built-in 8-bits DAC, a compared result are outputted to EMG input of A-PMD.

Table 5.17 Built-in Comparator

Channel	M3HQ	M3HP	M3HN	M3HM	M3HL
Channel0	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

Not Recommended for New Design

5.18. Advanced Programmable Motor Control Circuit (A-PMD)

The motor control circuit (A-PMD) enables users to control brushless DC motors easily. It incorporates the three-phase pulse modulation circuit and dead-time circuit, and easily generates waveforms for motor control by operating with the ADC in a coordinated fashion.

It also provides over-voltage detection input and abnormal detection input to support safety measures.

Table 5.18 Built-in A-PMD

Channel	M3HQ	M3HP	M3HN	M3HM	M3HL
Channel 0	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.19. Advanced Encoder Input Circuit (A-ENC)

The advanced encoder input circuit (A-ENC) supports an incremental encoder to acquire the motor position easily. The noise canceller is installed in the input pins, so that the signals from an incremental encoder or Hall sensor can be input directly.

The A-ENC provides six operation modes: encoder mode, sensor modes (3 kinds), timer mode, and phase counter mode.

Table 5.19 Built-in A-ENC

Channel	M3HQ	M3HP	M3HN	M3HM	M3HL
Channel 0	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

Not Recommended for New Design

5.20. 32-bit Timer Event Counter (T32A)

The T32A is a timer event counter that can operate as a 32-bit Timer or two 16-bit Timers. 16-bit Timer or 32-bit Timer can be selected. In 16-bit Timer, the T32A is comprised of Timer A and Timer B incorporating a 16-bit counter. In 32-bit Timer, the T32A operates as Timer C incorporating a 32-bit counter.

The T32A has an interval timer, event counter, input capture, 2-phase counter input, PPG output, Synchronous Start, and Trigger start/stop functions.

Table 5.20 Built-in T32A

Channel	M3HQ	M3HP	M3HN	M3HM	M3HL
Channel 0	✓	✓	✓	✓	✓
Channel 1	✓	✓	✓	✓	✓
Channel 2	✓	✓	✓	✓	✓
Channel 3	✓	✓	✓	✓	✓
Channel 4	✓	✓	✓	✓	✓
Channel 5	✓	✓	✓	✓	✓
Channel 6	✓	✓	✓	✓	✓
Channel 7	✓	✓	✓	✓	✓

Note1:✓: Available, -: N/A
Note2: External pins are not the same by product. Please refer to section “2 Pin Assignment”.

5.21. Real Time Clock (RTC)

The RTC is a peripheral function that has a second counter, clock function, and leap-year calendar function. It also has the alarm function that generates an interrupt on a specified time and date.

Since the RTC operates on a low-speed external oscillation clock, it can operate in low-power consumption mode such as IDLE, STOP1 or STOP2 modes. In addition, the MCU can be returned from low-power consumption mode by an interrupt request of the RTC.

The RTC easily corrects a gain/loss of the clock caused by an error of low-speed oscillation frequency using the clock correction function.

Table 5.21 Built-in RTC

	M3HQ	M3HP	M3HN	M3HM	M3HL
RTC	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

Not Recommended for New Design

5.22. Clock Selective Watchdog Timer (SIWDT)

The SIWDT is a peripheral function that detects an overflow of the binary counter and generates an interrupt request or resets the MCU. This state occurs when a binary counter cannot be cleared within the preset detection time.

The count clock can be selected from three clocks: system clock (fsys/4), internal oscillator1 (f_{IHOSC1}), or internal oscillator2 (f_{IHOSC2}).

It also provides the count-clear window function that can clear the count only for the specified period.

Moreover, the change of a register can be forbidden until the reset starts by setting to protected mode.(the count-clear function is possible)

Table 5.22 Built-in SIWDT

	M3HQ	M3HP	M3HN	M3HM	M3HL
SIWDT	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.23. Remote control signal preprocessor (RMC)

The RMC is a peripheral function that receives signals excluding carrier signal from remote control reception signals. The RMC detects a leader signal to receive 72 bits data in a collective manner. Two data formats can be received: synchronous format and fixed-synchronous phase format.

In addition, it contains a digital noise canceller to avoid external noise.

Since the RMC operates on a low-frequency clock, it can operate in low power consumption mode, such as IDLE mode or STOP1 mode according to the setting (except STOP2). The MCU can also be returned from low-power consumption mode by an interrupt request of the RMC.

Table 5.23 Built-in RMC

Channel	M3HQ	M3HP	M3HN	M3HM	M3HL
Channel0	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.24. CRC calculation circuit (CRC)

This product has the Hardware calculation circuit for CRC32 and CRC16.
It can be used for detecting a memory and communication data error.

Table 5.24 Built-in CRC calculation circuit

Channel	M3HQ	M3HP	M3HN	M3HM	M3HL
Channel 0	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

Not Recommended for New Design

5.25. RAM Parity (RAMP)

A RAM parity function generates and (8-bit unit) stores even parity data at the time of the writing to RAM, and performs a parity judging at the time of reading from RAM.

The interrupt is generated when it becomes an error by judgment. The Status and Address which the error generated are known.

A parity error is detectable in real time, since parity generating/ judgment is hardware.

Table 5.25 Built-in RAM parity circuit

	M3HQ	M3HP	M3HN	M3HM	M3HL
RAMP	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

Not Recommended for New Design

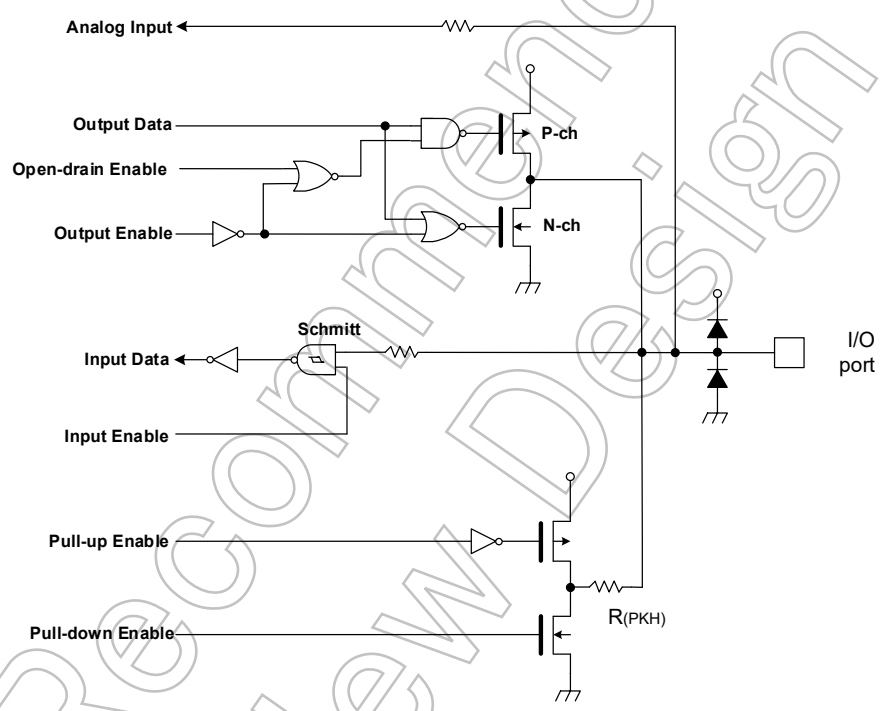
6. Equivalent Circuit

Basically, the gate symbols written are the same as those used for the standard CMOS logic IC [74HCXX] series.

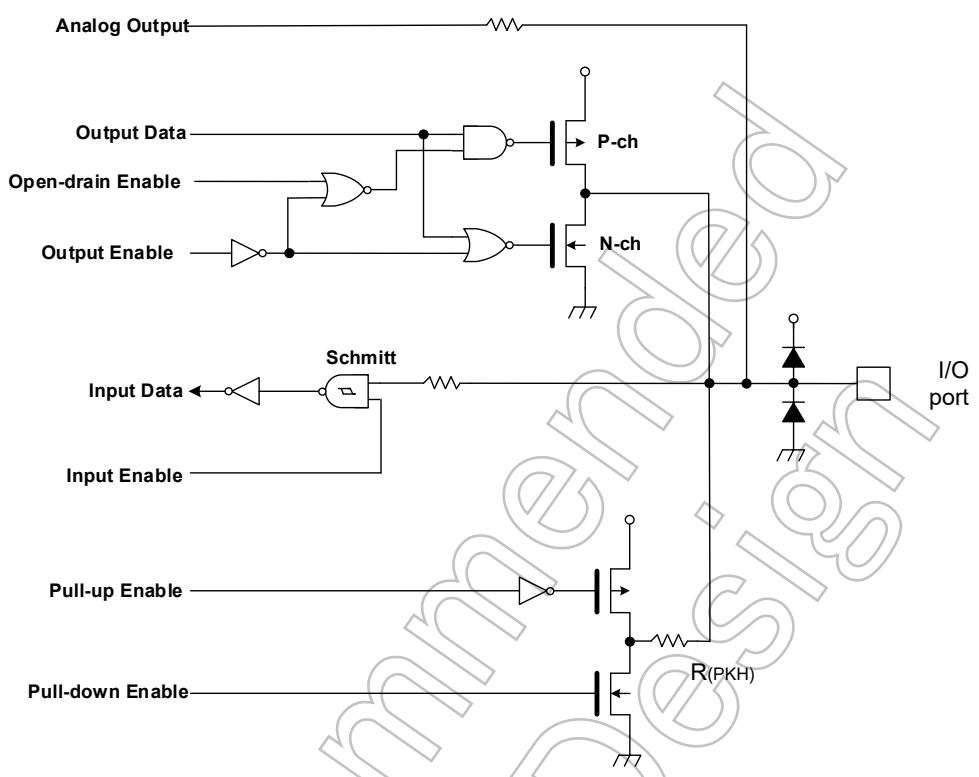
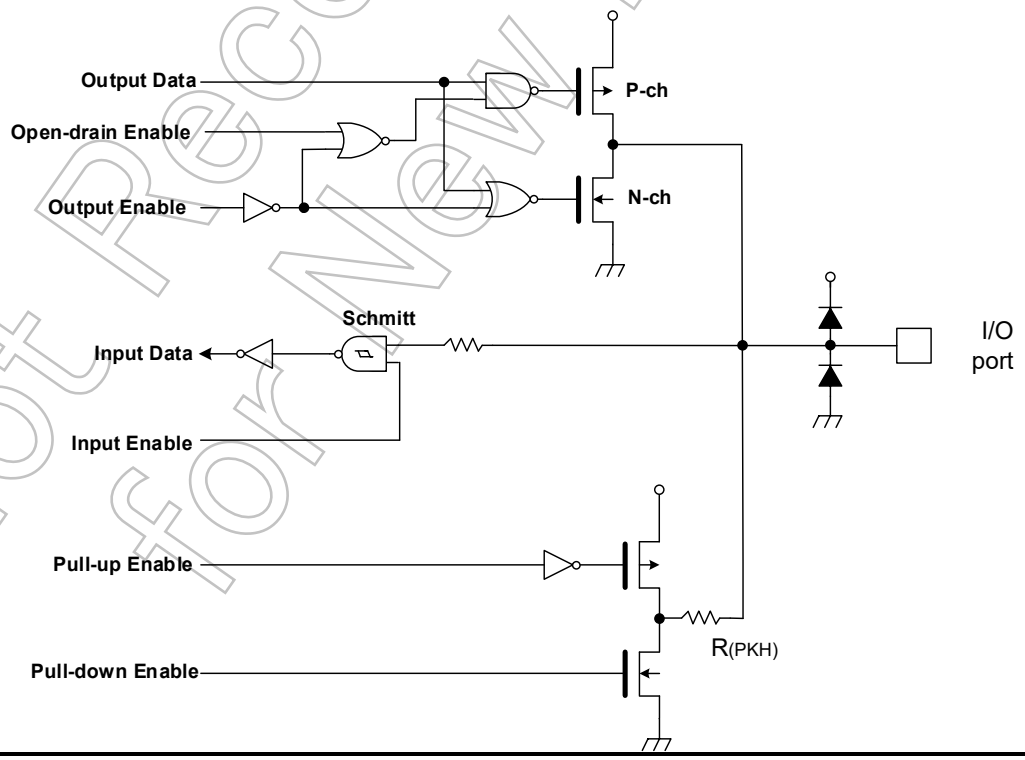
The input protection resistance ranges from several tens of Ω to several hundred Ω Feedback resistor and Damping resistor are shown with a typical value.

Note: The resistance without the statement of the numerical value in the figure shows input protection resistance.

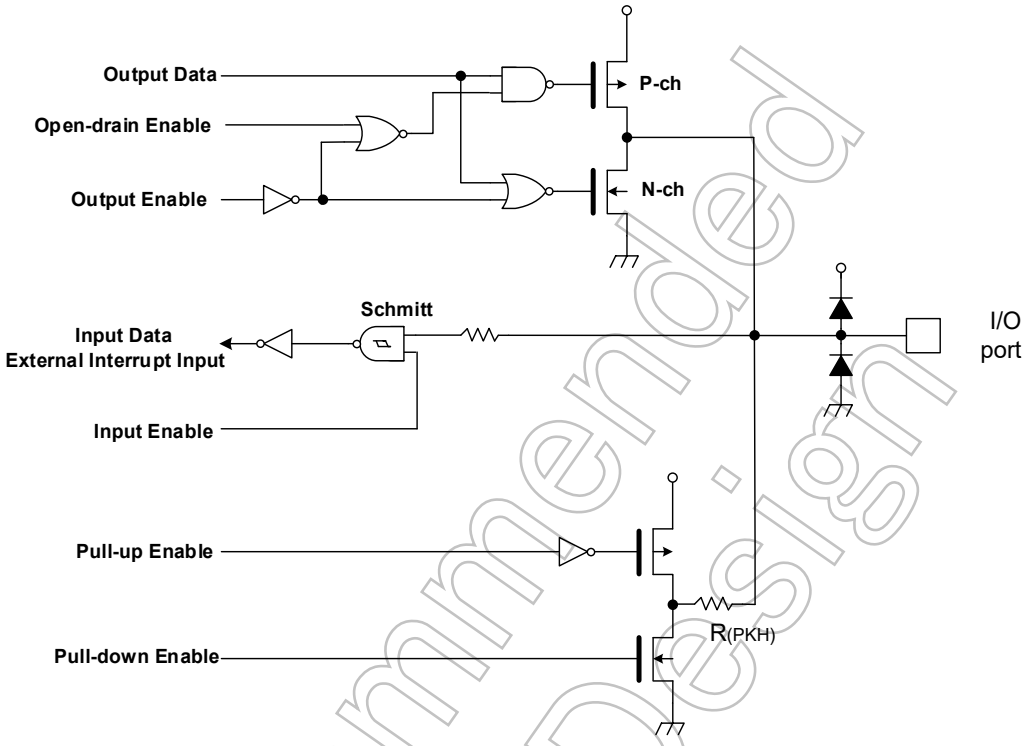
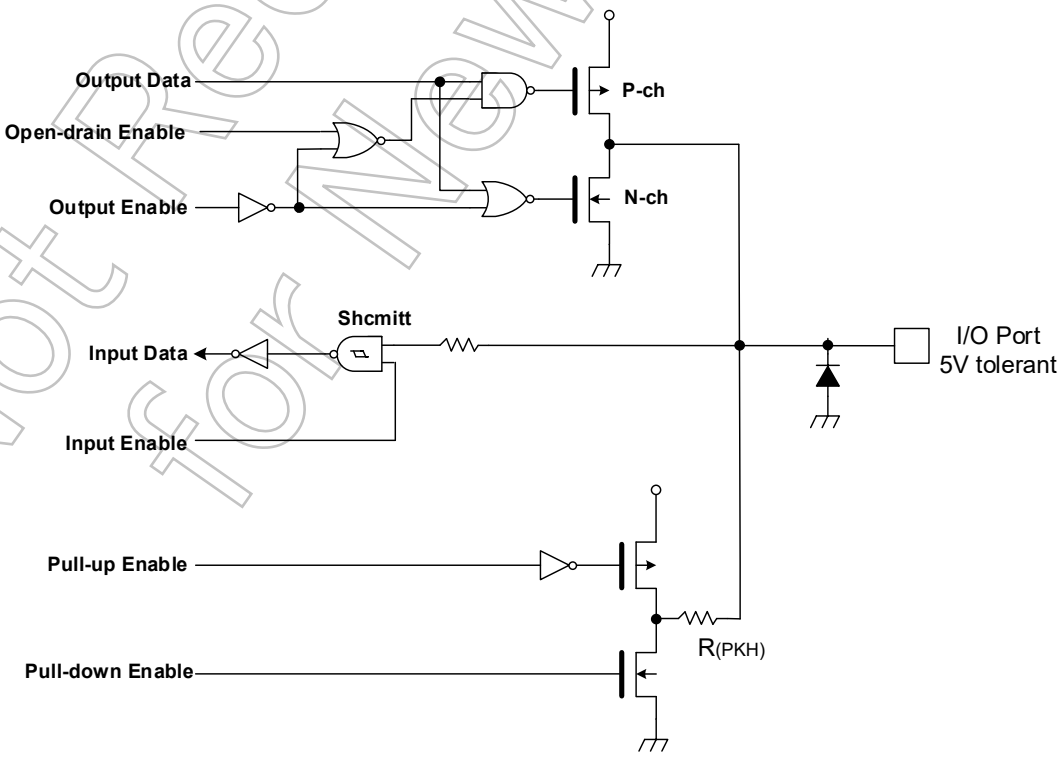
6.1. Port

PD0 to PD5 **PE0 to PE6** **PF0 to PF7**	**(Programmable pull-up/pull-down, Programmable Open-drain output, Schmitt input, Analog input)** 

Not Recommended for New Design

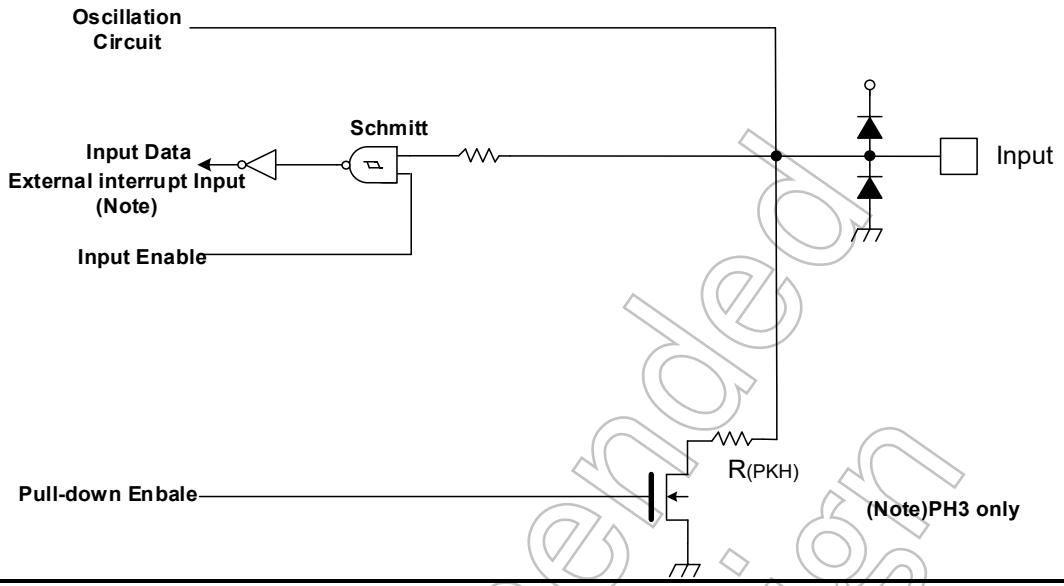
PG0 to PG1	(Programmable Pull-up/Pull-down, Programmable Open-drain Output, Schmitt input, Analog Output) 
PA0 to PA3 PB2 to PB6 PC3 to PC6 PG4 to PG7 PJ0 to PJ3 PJ5,PK0 PK2 to PK6 PL0 to PL2, PL5 to PL7 PM0,PM1 PM3 to PM5 PM7 PN0 to PN2, PN4,PN5 PP0 to PP2 PP4 to PP7 PR0 to PR7 PT4 to PT6 PU2 to PU5 PV0 to PV1 PV4 to PV7	(Programmable Pull-up/Pull-down, Programmable Open-drain Output, Schmitt Input) 

Not Recommended for New Design

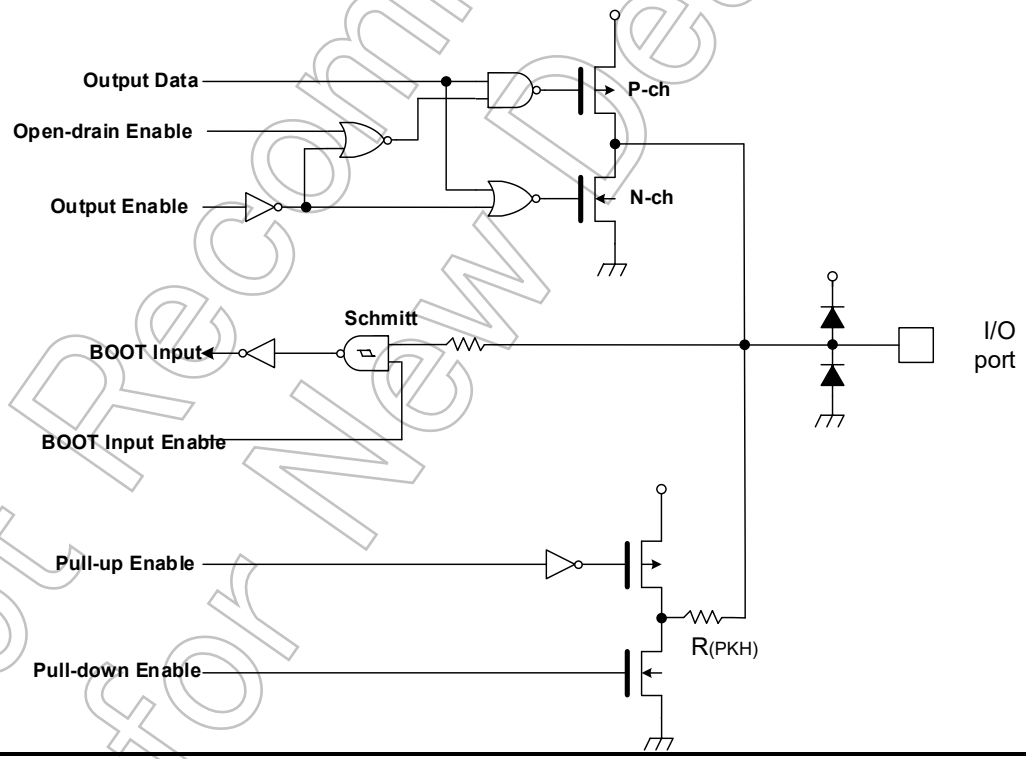
PA6,PA7, PB1,PB7, PC0,PC1, PC2,PG2, PG3,PH4, PH5,PH6, PH7,PJ4, PK1,PK7, PL3,PL4, PM2,PM6, PN3,PP3, PT0,PT1, PT2,PT3, PT7,PU0, PU1,PV2, PV3,	(Programmable Pull-up/Pull-down, Programmable Open-drain Output, Schmitt Input, External Interrupt Input) 
PA4,PA5	(5V tolerant, Programmable pull-up/pull-down, Programmable Open-drain output, Schmitt Input) 

Not Recommended for New Design

PH0 to PH3	(Programmable Pull-down, Schmitt Input, Oscillation Circuit)

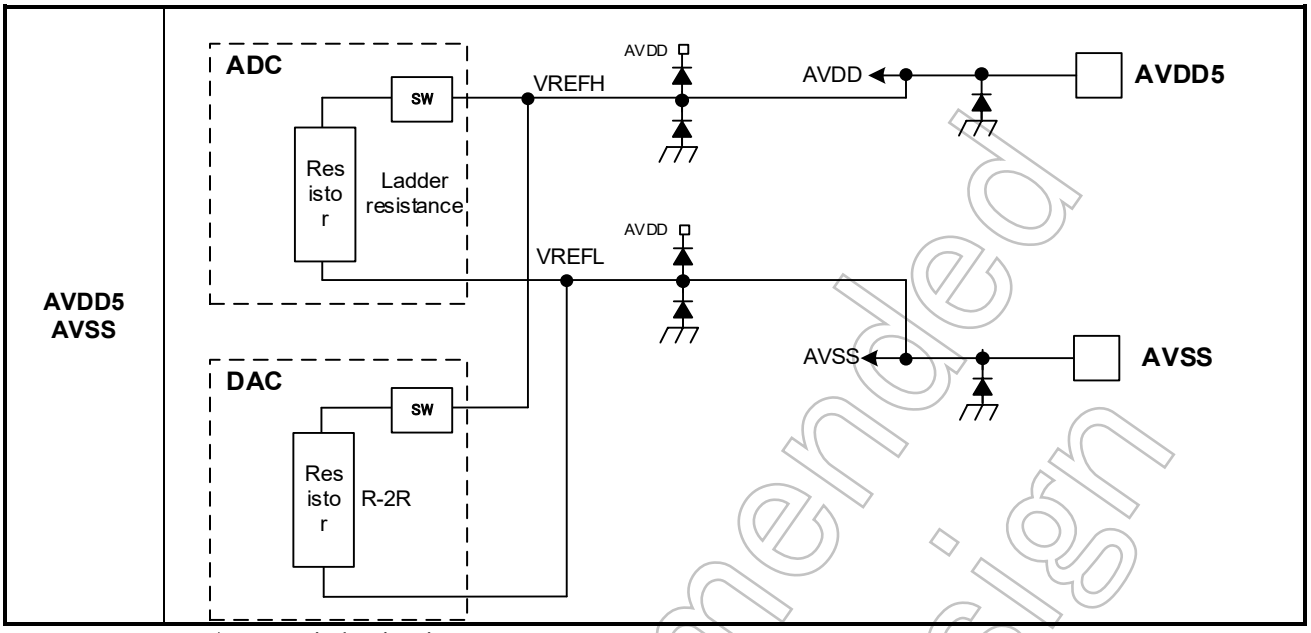


PB0/BOOT_N	(Programmable Pull-up/Pull-down, Programmable Open-drain Output, Schmitt Input)



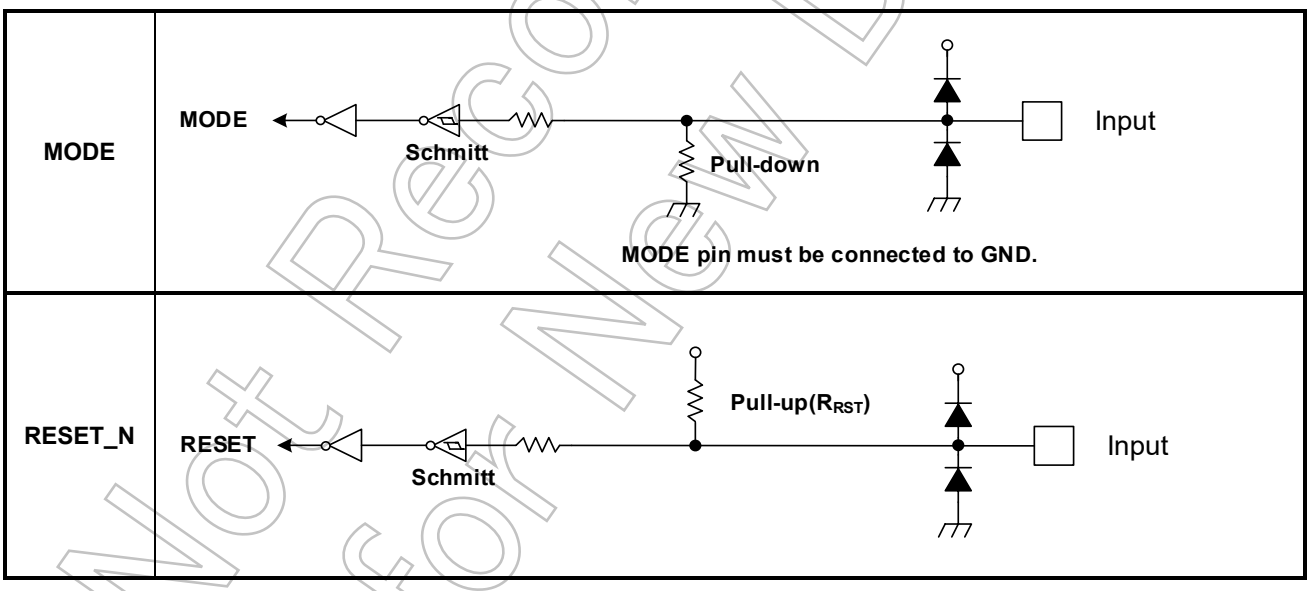
Not Recommended for New Design

6.2. Analog Power pin



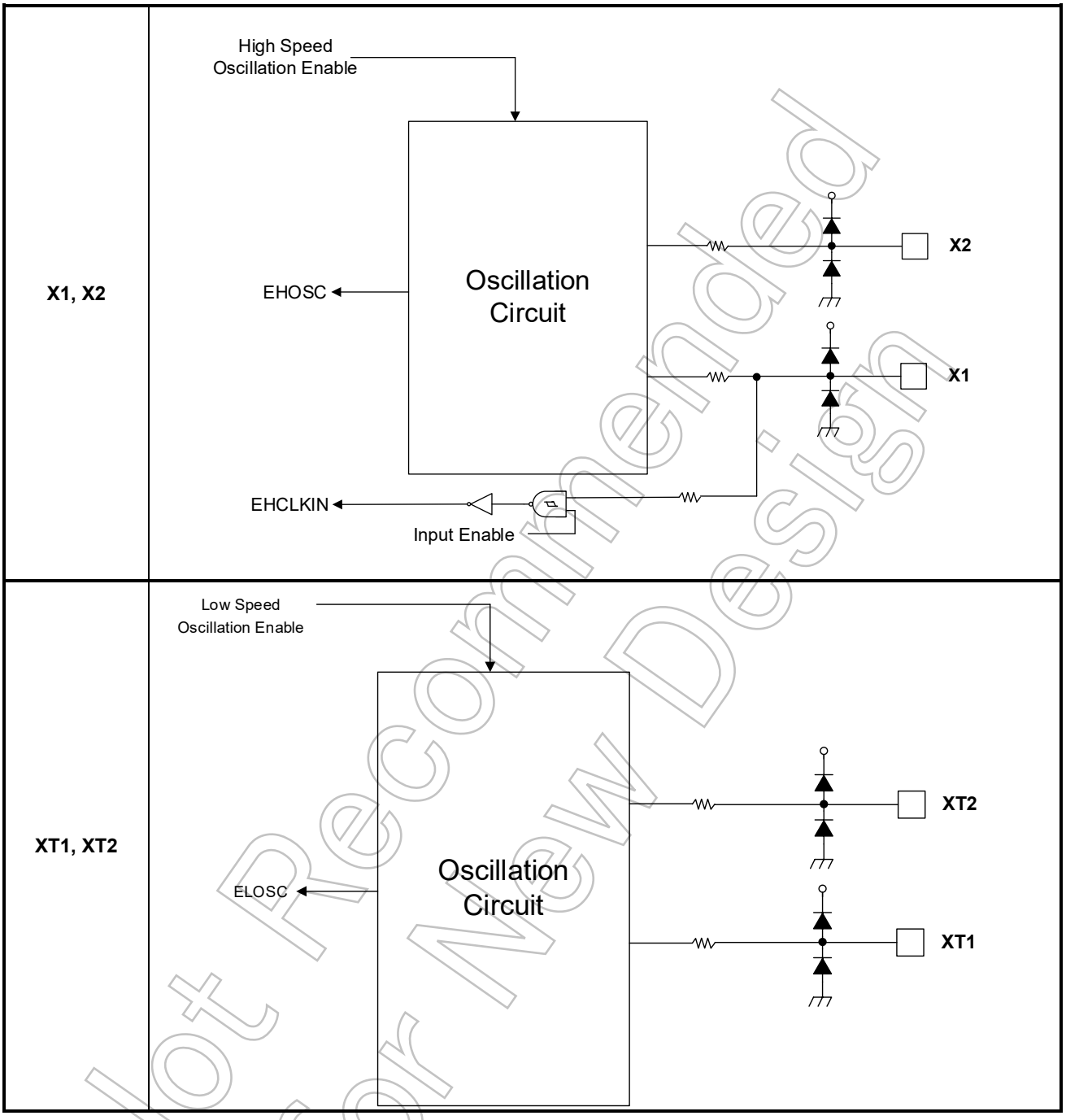
Note: SW: ON/OFF Switch Circuit

6.3. Control Pin



Not Recommended for New Design

6.4. Clock control



Not Recommended for New Design

7. Electrical Characteristics

7.1. Absolute Maximum Ratings

Table 7.1 Absolute maximum ratings

Parameter		Symbol	Rating	Unit
Power supply voltage		DVDD5A DVDD5B	-0.3 to 6.0	V
		AVDD5	-0.3 to DVDD5 (Note1)	
Capacitor pin voltage for voltage maintenance		REGOUT1	-0.3 to 1.7	V
		REGOUT2	-0.3 to 3.9	
Input voltage	PC0 to 6, PH0 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PR0 to 7, PV0 to 7, PA0 to 3, PA6 to 7, PB1 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 7, PT0 to 7, PU0 to 5, MODE, RESET_N,BOOT_N	V_{IN1} V_{IN2}	-0.3 to DVDD5+0.3(≤6.0V) (Note1)	V
	PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	V_{IN3}	-0.3 to AVDD5+0.3(≤6.0V)	
	PA4 to 5	V_{IN4}	-0.3 to 6.0	
Low level output current	Per Pin, PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PR0 to 7, PV0 to 7, PA0 to 3, PA6 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 7, PT0 to 7, PU0 to 5, PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	I_{OL}	5	mA
	Per Pin, PA4 to 5	I_{OL4}	25	
	Total	ΣI_{OL}	50	
High level output current	Per pin, PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PR0 to 7, PV0 to 7, PA0 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 7, PT0 to 7, PU0 to 5, PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	I_{OH}	-5	
	Total	ΣI_{OH}	-50	
Power consumption (Ta= 85°C)		PD	600	mW
Soldering temperature		T_{SOLDER}	260	°C
Storage temperature		T_{STG}	-55 to 125	°C
Operational temperature		T_{OPR}	-40 to 85	°C

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B. Apply the same voltage to DVDD5 and AVDD5.

Note2: Absolute maximum ratings are limiting values of operating and environmental conditions which should not be exceeded under the worst possible conditions. The equipment manufacturer should design so that no Absolute maximum rating value is exceeded with respect to current, voltage, power consumption, temperature, etc. Exposure to conditions beyond those listed above may cause permanent damage to the device or affect device reliability, which could increase potential risks of personal injury due to IC blow up and/or burning.

Not Recommended for New Design

7.2. DC Electrical Characteristics (1/2)

4.5V ≤DVDD5=AVDD5≤ 5.5V
DVSS=AVSS=0V
Ta=-40 to 85 °C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Power supply voltage	DVDD5A,DVDD5B, AVDD5	VDD	f_{OSC} = 6 to 12MHz f_{sys} = 1 to 80MHz fs = 30 to 34kHz	4.5	-	5.5	V
Low level Input voltage	PC0 to 6, PH0 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP3 to 7, PR0 to 7, PV0 to 7, MODE, RESET_N,	V_{IL1}	-	-0.3	-	DVDD5×0.25	V
	PA0 to 3, PA6 to 7, PB1 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 2, PT0 to 7, PU0 to 5, BOOT_N	V_{IL2}					
	PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	V_{IL3}				AVDD5×0.25	
	PA4 to 5	V_{IL4}				DVDD5×0.3	
High level Input voltage	PC0 to 6, PH0 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP3 to 7, PR0 to 7, PV0 to 7, MODE, RESET_N,	V_{IH1}	-	DVDD5×0.75	-	DVDD5+0.3	V
	PA0 to 3, PA6 to 7, PB1 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 2, PT0 to 7, PU0 to 5, BOOT_N	V_{IH2}					
	PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	V_{IH3}		AVDD5×0.75		AVDD5+0.3	
	PA4 to 5	V_{IH4}		DVDD5×0.7		DVDD5+0.3	
Low level output voltage	PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP0 to 7, PR0 to 7, PV0 to 7, PA0 to 3, PA6 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PT0 to 7, PU0 to 5,	V_{OL1} V_{OL2}	DVDD5=4.5V I_{OL} = 1.6mA	-	-	0.4	V
	PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	V_{OL3}	AVDD5=4.5V I_{OL}=1.6mA	-	-	0.4	
	PA4 to 5	V_{OL4}	DVDD5=4.5V I_{OL}=8mA	-	-	1.0	
High level output voltage	PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP0 to 7, PR0 to 7, PV0 to 7, PA0 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PT0 to 7, PU0 to 5,	V_{OH1} V_{OH2}	DVDD5=4.5V I_{OH}=-1.6mA	DVDD5-0.4	-	-	V
	PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	V_{OH3}	AVDD5=4.5V I_{OH}=-1.6mA	AVDD5-0.4	-	-	

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B.
Note 2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 5V, unless otherwise noted.
Note 3: Apply the same voltage to DVDD5 and AVDD5.

Not Recommended for New Design

4.5V ≤DVDD5=AVDD5≤ 5.5 V
DVSS=AVSS=0V
Ta= -40 to 85°C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Input leak current		I_{LI}	0.0V ≤ VIN ≤ DVDD5 0.0V ≤ VIN ≤ AVDD5	-5	0.05	5	μA
Output leak current		I_{LO}	0.2 ≤VIN ≤DVDD5-0.2 0.2 ≤ VIN ≤ AVDD5-0.2	-10	0.05	10	
Schmitt trigger Input width		VTH	DVDD5=AVDD5=5V	-	1	-	V
Reset pull-up resistor		R_{RST}		25	30	100	kΩ
Programmable pull-up/-down resistor		P_{KH}	Pull-up	25	30	100	kΩ
			Pull-down	25	50	100	
Pin capacity (except power supply pin)		C_{IO}	fc =1MHz	-	-	10	pF
Low level output current	Per pin except below ports	I_{OL}	DVDD5=5V AVDD5=5V	-	-	2 (Note4)	mA
	Per pin PA4 to 5	I_{OL4}	DVDD5=5V	-	-	12 (Note4)	
	Total of PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP3 to 7, PR0 to 7, PV0 to 7	ΣI_{OL1}	DVDD5=5V	-	-	35 (Note5)	
	Total of PA0 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 2, PT0 to 7, PU0 to 5	ΣI_{OL2}	DVDD5=5V	-	-	35 (Note5)	
	Total of PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	ΣI_{OL3}	AVDD5=5V	-	-	20 (Note5)	
High level output current	Per pin	I_{OH}	DVDD5=5V AVDD5=5V	-2 (Note4)	-	-	mA
	Total of PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP3 to 7, PR0 to 7, PV0 to 7	ΣI_{OH1}	DVDD5=5V	-35 (Note5)	-	-	
	Total of PA0 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 2, PT0 to 7, PU0 to 5	ΣI_{OH2}	DVDD5=5V	-35 (Note5)	-	-	
	Total of PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	ΣI_{OH3}	AVDD5=5V	-20 (Note5)	-	-	

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B.

Note 2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 5V, unless otherwise noted

Note 3: Apply the same voltage to DVDD5 and AVDD5.

Note 4: The current sum total of a terminal should not exceed the sum total of each group current.

Note 5: The sum total of each group current should not exceed the absolute maximum rating.

Not Recommended for New Design

2.7V ≤DVDD5=AVDD5< 4.5V
DVSS=AVSS=0V
Ta=-40 to 85 °C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Power supply voltage	DVDD5A,DVDD5B, AVDD5	VDD	f_{OSC} = 6 to 12MHz f_{sys} = 1 to 80MHz fs = 30 to 34kHz	2.7	-	4.5	V
Low level Input voltage	PC0 to 6, PH0 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP3 to 7, PR0 to 7, PV0 to 7, MODE, RESET_N,	V_{IL1}		-0.3	-	DVDD5×0.25	V
	PA0 to 3, PA6 to 7, PB1 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 2, PT0 to 7, PU0 to 5, BOOT_N	V_{IL2}					
	PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	V_{IL3}				AVDD5×0.25	
	PA4 to 5	V_{IL4}				DVDD5×0.3	
High level Input voltage	PC0 to 6, PH0 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP3 to 7, PR0 to 7, PV0 to 7, MODE, RESET_N,	V_{IH1}		DVDD5×0.75	-	DVDD5+0.3	V
	PA0 to 3, PA6 to 7, PB1 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 2, PT0 to 7, PU0 to 5, BOOT_N	V_{IH2}					
	PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	V_{IH3}		AVDD5×0.75		AVDD5+0.3	
	PA4 to 5	V_{IH4}		DVDD5×0.7		DVDD5+0.3	
Low level output voltage	PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP0 to 7, PR0 to 7, PV0 to 7, PA0 to 3, PA6 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PT0 to 7, PU0 to 5,	V_{OL1} V_{OL2}	DVDD5=2.7V I_{OL} = 0.8mA	-	-	0.4	V
	PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	V_{OL3}	AVDD5=2.7V I_{OL}= 0.8mA	-	-	0.4	
	PA4 to 5	V_{OL4}	DVDD5=2.7V I_{OL}= 4mA	-	-	1.0	
High level output voltage	PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP0 to 7, PR0 to 7, PV0 to 7, PA0 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PT0 to 7, PU0 to 5,	V_{OH1} V_{OH2}	DVDD5=2.7V I_{OH}= -0.8mA	DVDD5-0.4	-	-	V
	PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	V_{OH3}	AVDD5=2.7V I_{OH}= -0.8mA	AVDD5-0.4	-	-	

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B.

Note 2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 3V, unless otherwise noted.

Note 3: Apply the same voltage to DVDD5 and AVDD5.

Not Recommended for New Design

2.7V ≤DVDD5=AVDD5< 4.5V
DVSS=AVSS=0V
Ta= -40 to 85°C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Input leak current		I_{LI}	0.0V ≤ VIN ≤ DVDD5 0.0V ≤ VIN ≤ AVDD5	-5	0.05	5	μA
Output leak current		I_{LO}	0.2 ≤VIN ≤DVDD5-0.2 0.2 ≤ VIN ≤ AVDD5-0.2	-10	0.05	10	
Schmitt trigger Input width		VTH	DVDD5 =AVDD5= 3V	-	0.5	-	V
Reset pull-up resistor		R_{RST}		25	100	200	kΩ
Programmable pull-up/-down resistor		P_{KH}	Pull-up	25	100	200	
			Pull-down	25	100	200	
Pin capacity (except power supply pin)		C_{IO}	fc =1MHz	-	-	10	pF
Low level output current	Per pin except below ports	I_{OL}	DVDD5=3V AVDD5=3V	-	-	1 (Note4)	mA
	Per pin PA4 to 5	I_{OL4}	DVDD5=3V	-	-	6 (Note4)	
	Total of PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP3 to 4, PR0 to 7, PV0 to 7	ΣI_{OL1}	DVDD5=3V	-	-	18 (Note5)	
	Total of PA0 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 2, PT0 to 7, PU0 to 5	ΣI_{OL2}	DVDD5=3V	-	-	18 (Note5)	
	Total of PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	ΣI_{OL3}	AVDD5=3V	-	-	10 (Note5)	
High level output current	Per pin	I_{OH}	DVDD5=3V AVDD5=3V	-1 (Note4)	-	-	mA
	Total of PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP3 to 4, PR0 to 7, PV0 to 7	ΣI_{OH1}	DVDD5=3V	-18 (Note5)	-	-	
	Total of PA0 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 2, PT0 to 7, PU0 to 5	ΣI_{OH2}	DVDD5=3V	-18 (Note5)	-	-	
	Total of PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	ΣI_{OH3}	AVDD5=3V	-10 (Note5)	-	-	

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B.

Note 2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 3.0V, unless otherwise noted.

Note 3: Apply the same voltage to DVDD5 and AVDD5.

Note 4: The current sum total of a terminal should not exceed the sum total of each group current.

Note 5: The sum total of each group current should not exceed the absolute maximum rating.

Not Recommended for New Design

7.3. DC Electrical Characteristics (2/2)

Consumption current

Ta =-40 to 85°C

Parameter	Symbol	Conditions				Min	Typ. (Note2)	Max	Unit
		Supply voltage	High-speed oscillator	Low-speed oscillator	Operating condition				
Normal	I_{DD}	DVDD5= AVDD5= 5.5V	Refer to the table 7.2 and 7.3 for detail			-	19.6	27.4	mA
IDLE			Oscillation	Oscillation	Refer to the table 7.2 and 7.3 for detail	-	3.2	12.2	
STOP1			Stop	Oscillation		-	220	5200	μA
STOP2						-	18	300	
				Stop		-	17	300	

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B.

Note 2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 5V, unless otherwise noted.

Note 3: Apply the same voltage to DVDD5 and AVDD5.

Note 4: Input pin is fixed level, Output pin is open.

Table 7.2 IDD measurement condition (Pin setting, Oscillation Circuit)

		NORMAL	IDLE	STOP1	STOP2	
				ELOSC run		ELOSC stop
Pin setting	DVDD5= AVDD5=	5.0V(Typ.), 5.5V(max)				
	X1,X2	Oscillator connected (10MHz)				
	XT1,XT2	Oscillator connected(32.768kHz)				
	Input pins	Fixed				
	Output pins	Open				
Operation condition (Oscillation Circuit)	System clock (fsys)	80MHz		Stop		
	External High speed frequency oscillator (EHOSC)	Oscillation		Stop		
	Internal High speed frequency oscillator1 (IHOSC1)	Stop				
	PLL	run(8times)		Stop		
	External low speed oscillator (ELOSC)	Oscillation				Stop

Not Recommended for New Design

Table 7.3 IDD measurement condition (CPU, Peripheral)

Peripheral	unit number	NORMAL	IDLE	STOP1	STOP2
				LOSC oscillation	LOSC stop
CPU	1	Run (Dhrystone Ver.2.1)	Stop		
DMAC	1	(Request from UARTch0 TX, destination: RAM)	Stop		
ADC	1	Run (1.5μs, Repeated conversion)	Stop		
DAC	2	Run	Stop		
T32A	6	All Ch: Run	Stop		
A-PMD	1	Run	Stop		
A-ENC	1	Run	Stop		
RTC	1	Run			
SIWDT	1	Run	Stop		
UART	6	All Ch: UART, Transmission(2.5Mbps)	Stop		
I^2C	4	Stop			
TSPI	5	Ch0, Ch1: Transmission(20MHz)	Stop		
RMC	1	Run	Stop		
LVD	1	Stop			
OFD	1	Stop			
Input Output Port	-	Run	Stop		

Not Recommended for New Design

7.4. 12-bit AD Converter Characteristics

DVDD5=AVDD5=2.7V to 5.5V
DVSS=AVSS=0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog reference voltage (+)	AVDD5 (VREFH)		AVDD5-0.3	-	AVDD5+0.3	V
Analog input voltage	VAIN		AVSS (VREFL)	-	AVDD5 (VREFH)	V
Integral nonlinearity error (INL)	-	4.5 ≤ AVDD5 ≤ 5.5 AIN load resistor = 600 Ω AIN load capacity ≥ 0.1μF Conversion time = 1.5μs	-2.5	-	2.5	LSB
Differential nonlinearity error (DNL)			-2	-	1.5	
Zero-scale error			-1	-	3	
Full-scale error			-2	-	3	
Total errors			-3	-	3	
Integral nonlinearity error (INL)	-	2.7 ≤ AVDD5 < 4.5 AIN load resistor = 600 Ω AIN load capacity ≥ 0.1μF Conversion time = 2.95μs	-3	-	3	LSB
Differential nonlinearity error (DNL)			-2	-	1.5	
Zero-scale error			-4	-	4.5	
Full-scale error			-4	-	4.5	
Total errors			-5.5	-	4	
Stable time	t_{sta}	After ***[ADMOD0]***<DACON>= 1 is set.	3	-	-	μs
Conversion time (Note3)	t_{conv}	4.5V ≤ AVDD5 ≤ 5.5V SCLK=40MHz	1.5	-	16.3	
		2.7V ≤ AVDD5 < 4.5V SCLK=40MHz	2.95	-	16.65	

Note1: 1LSB = (AVDD5(VREFH) - AVSS(VREFL)) / 4096 [V]
Note2: The characteristic when a single unit AD converter operates only.
Note3: For detail of setting, refer to “Analog to Digital Converter” of the reference manual.

DVDD5=AVDD5=2.7Vto 5.5V
DVSS=AVSS=0V
Ta= -40to 85°C

Parameter	Conditions	Min	Typ.	Max	Unit
Reference power	ch23 selected	1.1	-	1.3	V

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

Not Recommended for New Design

7.5. 8-bit DA Converter Characteristics

DVDD5=AVDD5=2.7V to 5.5V
DVSS=AVSS=0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog reference voltage (+)	AVDD5 (VREFH)		AVDD5-0.3	-	AVDD5+0.3	V
Integral nonlinearity error (INL)	-	4.5V ≤ AVDD5 ≤ 5.5V Rload = 10MΩ	-1	-	+1	LSB
Differential nonlinearity error (DNL)			-1	-	+1	
Total errors			-1	-	+1	
Integral nonlinearity error (INL)	-	2.7V ≤ AVDD5 < 4.5V Rload = 10MΩ	-2	-	+2	LSB
Differential nonlinearity error (DNL)			-1	-	+1	
Total errors			-2	-	+2	
Stable time	t_{sta}	Cload = 20pF	4.5	-	-	μs

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B.
Note 2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 5V, unless otherwise noted.
Note 3: 1LSB = (AVDD5(VREFH) - AVSS(VREFL)) / 256 [V]
Note 4: This is the characteristic in case only DA converter is operating.
Note 5: When using DAC0 as the reference voltage of Comparator, DAC0 pin should be open.

7.6. Comparator Characteristics

DVDD5=AVDD5=2.7V to 5.5V
DVSS=AVSS=0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
AIN Input voltage Range	VINC		VREF-1.5	-	VREF+1.5	V
Reference Voltage Range (Note1)	VREFC		0.2	-	AVDD5-0.5	V
Response time(Note2)			-	-	0.7	μs
Comparator Start-up time	Tsta		-	-	5	μs

Note 1: Output of On-chip 8-bit DA converter (DAC0)
Note 2: In case of the VIN change from VREF-100mV to +100mV, or from VREF+100mV to -100mV.
Note 3: This is the characteristic in case only Comparator is operation.

Not Recommended for New Design

7.7. Characteristics of Internal processing at RESET

DVSS=AVSS=0V
Ta= -40to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Internal Initialized time	t_{IINIT}	Power-On	-	-	2.15	ms
		STOP2 Release by RESET with RESET_N	-	-	1.8	
		STOP2 Release by Interrupt	-	-	1.55	
Internal processing time for Reset	t_{IRST}		0.16	-	0.2	
Waiting time till CPU running	t_{CPUWT}	Cold Reset	12	-	15	μs
		Warm Reset	70	-	90	
Power-on rising gradient	V_{PON}		0.01	-	100	mV/μs

7.8. Characteristics of Power On Reset

DVSS=AVSS=0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Detection voltage	V_{PREL}	Power-up	2.25	2.4	2.55	V
	V_{PDET}	Power-down	2.2	2.35	2.5	
Detection pulse width	T_{PDET}		200	-	-	μs

Not Recommended for New Design

7.9. Characteristics of Voltage Detection Circuit

DVDD5=AVDD5=2.7V to 5.5V
DVSS=AVSS=0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Detection voltage	V_{LVL0}	Power-up	2.55	2.65	2.75	V
		Power-down	2.5	2.6	2.7	
	V_{LVL1}	Power-up	2.65	2.75	2.85	V
		Power-down	2.6	2.7	2.8	
	V_{LVL2}	Power-up	2.75	2.85	2.95	V
		Power-down	2.7	2.8	2.9	
	V_{LVL3}	Power-up	2.85	2.95	3.05	V
		Power-down	2.8	2.9	3.0	
	V_{LVL4}	Power-up	3.75	3.85	3.95	V
		Power-down	3.7	3.8	3.9	
	V_{LVL5}	Power-up	3.95	4.05	4.15	V
		Power-down	3.9	4.0	4.1	
	V_{LVL6}	Power-up	4.15	4.25	4.35	V
		Power-down	4.1	4.2	4.3	
	V_{LVL7}	Power-up	4.35	4.45	4.55	V
		Power-down	4.3	4.4	4.5	
Detection response time	t_{VDDT1}	Power-down	-	50	200	μs
Detection Release time	t_{VDDT2}	Power-up	-	250	-	
setup time	t_{LVDEN}		-	-	100	
Detection Minimum pulse width	t_{LVDPW}		200	-	-	

Not Recommended for New Design

7.10. AC Electrical Characteristics

7.10.1. Serial Peripheral Interface (TSPI)

7.10.1.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5=2.7V to 5.5V
- Ta = -40 to 85°C
- Output level: High = 0.8 × DVDD5, Low = 0.2 × DVDD5
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.10.1.2. AC Electrical Characteristics

"T" indicates an operation clock cycle of the TSPI. This operation clock has the same cycle of the system clock (fsys). This cycle depends on the clock gear setting.

The number of cycles can be 1 to 16. It is specified with TSPIxSCK. The value of k1 is specified with ***[TSPIxFMTR0]***<CSSCKDL[3:0]>; the value of k2 is specified with ***[TSPIxFMTR0]***<SCKCSDL[3:0]>. These values are 1 to 16.

Not Recommended for New Design

(1) Master in SPI mode (TSPI1/2/3/4)

4.5V ≤DVDD5=AVDD5≤ 5.5V

Parameter	Symbol	Equation		fsys=80MHz k1=k2=1		Unit
		Min	Max	Min	Max	
TSPIxSCK output frequency	f_{CYC}	-	20	-	20	MHz
TSPIxSCK output cycle	t_{CYC}	50	-	50	-	ns
TSPIxSCK low level output pulse width	t_{WL}	(t_{CYC}/2) - 13	-	12	-	
TSPIxSCK high level output pulse width	t_{WH}	(t_{CYC}/2) - 13	-	12	-	
TSPIxCSn output ← TSPIxSCK rise/fall time	t_{CSU}	(t_{CYC} × k1) - 20	(t_{CYC} x k1) + 9	30	59	
TSPIxSCK rise/fall time → TSPIxCSn hold time	t_{CHD}	(t_{CYC} x (k2 + 0.5))-20	-	55	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	35 - 2× T(Note1)	-	10	-	
		35 - T(Note2)				
TSPIxSCK rise/fall time → TSPIxRXD hold time	t_{DHD}	2×T - 10.5 (Note1)	-	14.5	-	
		T-10.5 (Note2)		14.5		
TSPIxSCK rise/fall time → TSPIxTXD delay time	t_{ODLY1}	-18	-	-18	-	
TSPIxSCK rise/fall time → TSPIxTXD delay time	t_{ODLY2}	-	16	-	16	
TSPIxCSn fall → TSPIxTXD delay time	t_{ODLY3}	(t_{CYC} x (k1 - 0.5))-25	(t_{CYC} x (k1 - 0.5))+9	0	34	

Note 1: In this case ***[TSPIxCR2]***<RXDLY>=1 ,fsys=80MHz

Note 2: In this case ***[TSPIxCR2]***<RXDLY>=0 ,fsys=40MHz

2.7V ≤DVDD5=AVDD5< 4.5V

Parameter	Symbol	Equation		fsys =80MHz k1=k2=1		Unit
		Min	Max	Min	Max	
TSPIxSCK output frequency	f_{CYC}	-	20	-	20	MHz
TSPIxSCK output cycle	t_{CYC}	50	-	50	-	ns
TSPIxSCK low level output pulse width	t_{WL}	(t_{CYC}/2) - 16	-	9	-	
TSPIxSCK high level output pulse width	t_{WH}	(t_{CYC}/2) - 16	-	9	-	
TSPIxCSn output ← TSPIxSCK rise/fall time	t_{CSU}	(t_{CYC} × k1) - 20	(t_{CYC} × k1) + 11	30	61	
TSPIxSCK rise/fall time → TSPIxCSn hold time	t_{CHD}	(t_{CYC} × (k2 + 0.5))-20	-	55	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	45 - 2×T (Note1)	-	20	-	
		45 - T(Note2)		20		
TSPIxSCK rise/fall time → TSPIxRXD hold time	t_{DHD}	2×T-10.5 (Note1)	-	14.5	-	
		T- 10.5 (Note2)	-	14.5		
TSPIxSCK rise/fall time → TSPIxTXD delay time	t_{ODLY1}	-18	-	-18	-	
TSPIxSCK rise/fall time → TSPIxTXD delay time	t_{ODLY2}	-	16	-	16	
TSPIxCSn fall → TSPIxTXD delay time	t_{ODLY3}	(t_{CYC} × (k1 - 0.5))-25	(t_{CYC} × (k1 - 0.5))+13	0	38	

Note 1: In this case ***[TSPIxCR2]***<RXDLY>=1 ,fsys=80MHz

Note 2: In this case ***[TSPIxCR2]***<RXDLY>=0 ,fsys=40MHz

Not Recommended for New Design

(2) Master in SPI mode (TSPI0)

4.5V ≤DVDD5=AVDD5≤ 5.5V

Parameter	Symbol	Equation		fsys = 80MHz k1=k2=1		Unit
		Min	Max	Min	Max	
TSPIxSCK output frequency	f_{CYC}	-	5.88	-	5.88	MHz
TSPIxSCK output cycle	t_{CYC}	170	-	170	-	ns
TSPIxSCK low level output pulse width	t_{WL}	(t_{CYC}/2) - 13	-	72	-	
TSPIxSCK high level output pulse width	t_{WH}	(t_{CYC}/2) - 13	-	72	-	
TSPIxCSn output ← TSPIxSCK rise/fall time	t_{CSU}	(t_{CYC} × k1) - 140	(t_{CYC} ×k1) + 9	30	179	
TSPIxSCK rise/fall time → TSPIxCSn hold time	t_{CHD}	(t_{CYC} × (k2 + 0.5))-20	-	235	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	35 - 2× T(Note1)	-	10	-	
		35 - T(Note2)		10		
TSPIxSCK rise/fall time → TSPIxRXD hold time	t_{DHD}	2×T - 10.5 (Note1)	-	14.5	-	
		T - 10.5(Note2)	-	14.5		
TSPIxSCK rise/fall time → TSPIxTXD delay time	t_{ODLY1}	-18	-	-18	-	
TSPIxSCK rise/fall time → TSPIxTXD delay time	t_{ODLY2}	-	16	-	16	
TSPIxCSn fall → TSPIxTXD delay time	t_{ODLY3}	(t_{CYC} × (k1- 0.5))-145	(t_{CYC} × (k1- 0.5))+9	-60	94	

Note 1: In this case ***[TSPIxCR2]***<RXDLY>=1, fsys=80MHz

Note 2: In this case ***[TSPIxCR2]***<RXDLY>=0, fsys=40MHz

2.7V ≤DVDD5=AVDD5< 4.5V

Parameter	Symbol	Equation		fsys =80MHz k1=k2=1		Unit
		Min	Max	Min	Max	
TSPIxSCK output frequency	f_{CYC}	-	4.34	-	4.34	MHz
TSPIxSCK output cycle	t_{CYC}	230	-	230	-	ns
TSPIxSCK low level output pulse width	t_{WL}	(t_{CYC}/2) - 16	-	99	-	
TSPIxSCK high level output pulse width	t_{WH}	(t_{CYC}/2) - 16	-	99	-	
TSPIxCSn output ← TSPIxSCK rise/fall time	t_{CSU}	(t_{CYC} × k1) - 200	(t_{CYC} × k1) + 9	30	239	
TSPIxSCK rise/fall time → TSPIxCSn hold time	t_{CHD}	(t_{CYC} ×(k2 + 0.5))-20	-	325	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	45 - 2×T (Note1)	-	20	-	
		45 - T(Note2)	-	20		
TSPIxSCK rise/fall time → TSPIxRXD hold time	t_{DHD}	2×T-10.5 (Note1)	-	14.5	-	
		T-10.5(Note2)	-	14.5		
TSPIxSCK rise/fall time → TSPIxTXD delay time	t_{ODLY1}	-18	-	-18	-	
TSPIxSCK rise/fall time → TSPIxTXD delay time	t_{ODLY2}	-	16	-	16	
TSPIxCSn fall → TSPIxTXD delay time	t_{ODLY3}	(t_{CYC} ×(k1-0.5))-211	(t_{CYC} × (k1-0.5))+13	-96	128	

Note 1: In this case ***[TSPIxCR2]***<RXDLY>=1, fsys=80MHz

Note 2: In this case ***[TSPIxCR2]***<RXDLY>=0, fsys=40MHz

Not Recommended for New Design

(3) Slave in SPI mode(TSPI0/1/2/3/4)

4.5V ≤DVDD5=AVDD5≤ 5.5V

Parameter	Symbol	Equation		fsys = 80MHz k1=1		Unit
		Min	Max	Min	Max	
TSPIxSCK Input frequency	f_{CYC}	-	10	-	10	MHz
TSPIxSCK Input cycle	t_{CYC}	100	-	100	-	ns
TSPIxSCK low level Input pulse width	t_{WL}	37	-	37	-	
TSPIxSCK high level Input pulse width	t_{WH}	37	-	37	-	
TSPIxCSIN Input ← TSPIxSCK rise/fall time	t_{CSU1}	(t_{CYC} × (k1 + 0.5)) +20	-	170	-	
TSPIxCSIN Input ← TSPIxSCK rise/fall time	t_{CSU2}	(t_{CYC} × k1) - 20	-	80	-	
TSPIxSCK rise/fall time → TSPIxCSIN hold time	t_{CHD}	7	-	7	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	7	-	7	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	10	-	10	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	0	-	0	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	49	-	49	
TSPIxCSIN fall → TSPIxTXD delay time	t_{ODLY3}	-	(t_{CYC} × (k1 - 0.5)) +5	-	55	
TSPIxCSIN high level input pulse width	t_{WDIS}	T × 2 + 20	-	45	-	

2.7V ≤DVDD5=AVDD5<4.5V

Parameter	Symbol	Equation		fsys = 80MHz k1=1		Unit
		Min	Max	Min	Max	
TSPIxSCK Input frequency	f_{CYC}	-	10	-	10	MHz
TSPIxSCK Input cycle	t_{CYC}	100	-	100	-	ns
TSPIxSCK low level Input pulse width	t_{WL}	37	-	37	-	
TSPIxSCK high level Input pulse width	t_{WH}	37	-	37	-	
TSPIxCSIN Input ← TSPIxSCK rise/fall time	t_{CSU1}	(t_{CYC} × (k1 + 0.5)) +20	-	170	-	
TSPIxCSIN Input ← TSPIxSCK rise/fall time	t_{CSU2}	(t_{CYC} × k1) - 20	-	80	-	
TSPIxSCK rise/fall time → TSPIxCSIN hold time	t_{CHD}	7	-	7	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	7	-	7	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	10	-	10	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	0	-	0	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	55	-	55	
TSPIxCSIN fall → TSPIxTXD delay time	t_{ODLY3}	-	(t_{CYC} × (k1 - 0.5)) +5	-	55	
TSPIxCSIN high level input pulse width	t_{WDIS}	T × 2 + 20	-	45	-	

Not Recommended for New Design

(4) Master in SIO Mode (TSPI0/1/2/3/4)

4.5V ≤DVDD5=AVDD5≤ 5.5V

Parameter	Symbol	Equation		fsys= 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK Output Frequency	f_{CYC}	-	20	-	20	MHz
TSPIxSCK Output cycle	t_{CYC}	50	-	50	-	ns
TSPIxSCK Low level Output pulse width	t_{WL}	(t_{CYC}/2)-13	-	12	-	
TSPIxSCK High level Output pulse width	t_{WH}	(t_{CYC}/2)-13	-	12	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	35-2×T (Note1)	-	10	-	
		35-T (Note2)	-	10		
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	2×T-10.5 (Note1)	-	14.5	-	
		T -10.5 (Note2)	-	14.5		
TSPIxSCK rise/ fall → TSPIxTXD delay time	t_{ODLY1}	-18	-	-18	-	
TSPIxSCK Rise/ fall → TSPIxTXD delay time	t_{ODLY2}	-	16	-	16	

Note 1: In this case ***[TSPIxCR2]***<RXDLY>=1, fsys=80MHz

Note 2: In this case ***[TSPIxCR2]***<RXDLY>=0, fsys=40MHz

2.7V≤DVDD5=AVDD5<4.5V

Parameter	Symbol	Equation		fsys= 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK Output Frequency	f_{CYC}	-	20	-	20	MHz
TSPIxSCK Output cycle	t_{CYC}	50	-	50	-	ns
TSPIxSCK Low level output pulse width	t_{WL}	(t_{CYC}/2)-16	-	9	-	
TSPIxSCK High level output pulse width	t_{WH}	(t_{CYC}/2)-16	-	9	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	45-2×T (Note1)	-	20	-	
		45-T (Note2)	-	20		
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	2×T-10.5 (Note1)	-	14.5	-	
		T- 10.5 (Note2)	-	14.5		
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	-18	-	-18	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	16	-	16	

Note 1: In this case ***[TSPIxCR2]***<RXDLY>=1, fsys=80MHz

Note 2: In this case ***[TSPIxCR2]***<RXDLY>=0, fsys=40MHz

Not Recommended for New Design

(5) Slave in SIO mode (TSPI0/1/2/3/4)

4.5V ≤ DVDD5=AVDD5 ≤5.5V

Parameter	Symbol	Equation		fsys= 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK Input Frequency	f_{CYC}	-	10	-	10	MHz
TSPIxSCK Input Cycle	t_{CYC}	100	-	100	-	ns
TSPIxSCK Low level Input Pulse Width	t_{WL}	37	-	37	-	
TSPIxSCK High level Input Pulse Width	t_{WH}	37	-	37	-	
TSPIxSCK rise/fall → TSPIxCSIN hold time	t_{CHD}	7	-	7	-	
TSPIxRXD Input ← SPIxSCK rise/fall time	t_{DSU}	7	-	7	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	10	-	10	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	0	-	0	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	49	-	49	

2.7V ≤ DVDD5=AVDD5<4.5V

Parameter	Symbol	Equation		fsys= 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK Input Frequency	f_{CYC}	-	10	-	10	MHz
TSPIxSCK Input Cycle	t_{CYC}	100	-	100	-	ns
TSPIxSCK Low level Input Pulse Width	t_{WL}	37	-	37	-	
TSPIxSCK High level Input Pulse Width	t_{WH}	37	-	37	-	
TSPIxSCK rise/fall → TSPIxCSIN hold time	t_{CHD}	7	-	7	-	
TSPIxRXD Input ← SPIxSCK rise/fall time	t_{DSU}	7	-	7	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	10	-	10	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	0	-	0	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	55	-	55	

Not Recommended for New Design

(1) 1st clock edge sampling (Master)

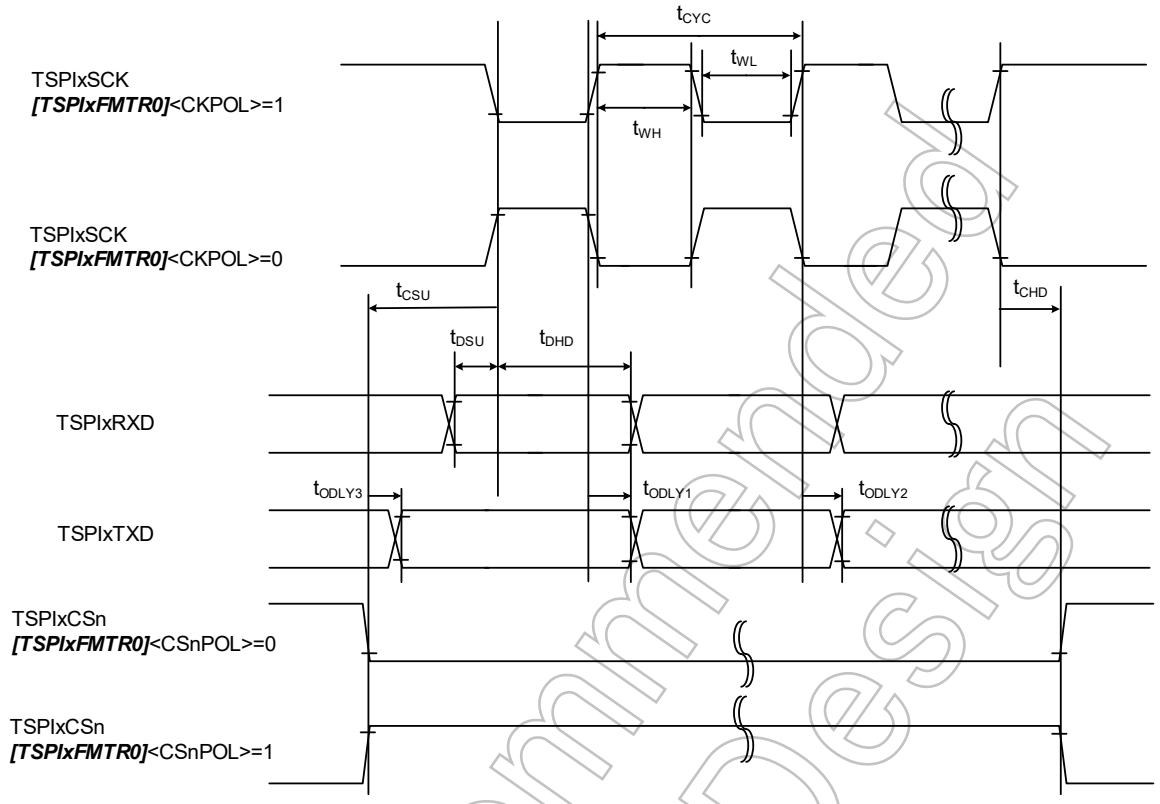


Figure 7.1 1st clock edge sampling (Master)

(2) 2nd clock edge sampling (Master)

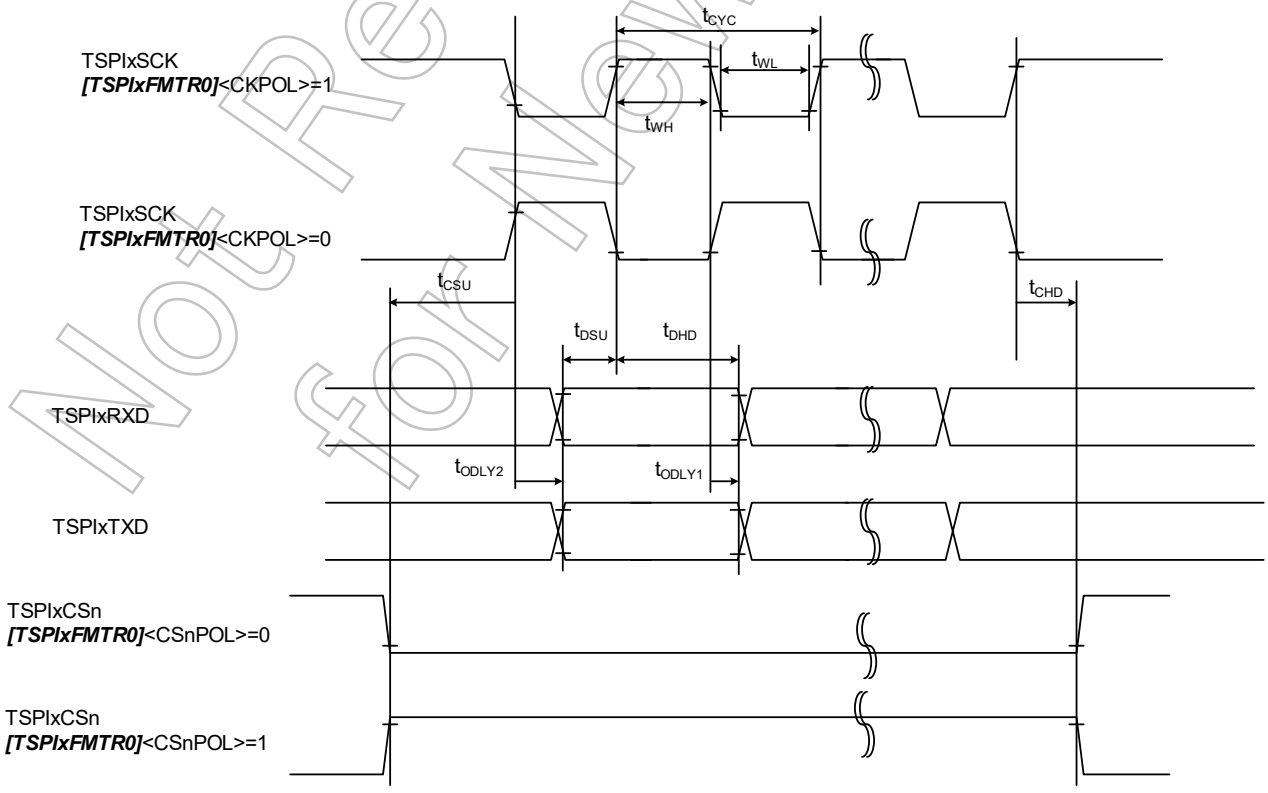


Figure 7.2 2nd clock edge sampling (Master)

Not Recommended for New Design

(3) 2nd clock edge sampling (slave)

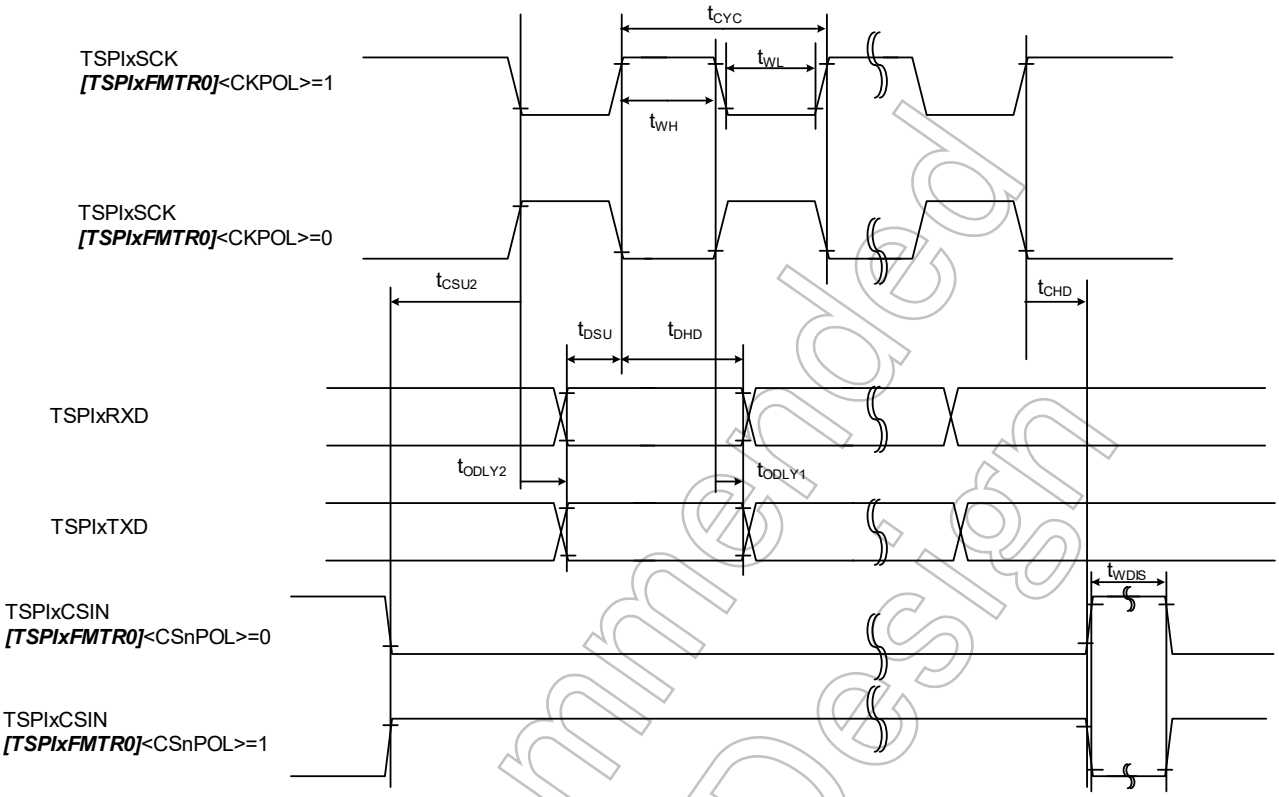


Figure 7.3 2nd clock edge sampling (Slave)

Not Recommended for New Design

7.10.2. I²C Interface (I²C)

7.10.2.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5=2.7v to 5.5V
- Ta = -40 to 85°C
- Output level: Low = 0.4V
- Input level: High = 0.7 × DVDD5, Low = 0.3 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.10.2.2. AC Electrical Characteristics

T indicates the Operation clock cycle of I²C.

The value of **n** is the SCL output clock frequency specified with ***[I2CxCR]***<SCK>.

The value of **p** is the prescaler dividing ratio specified with ***[I2CxPRS]***<PRSCK>.

Parameter		Symbol	Standard mode		Fast mode		Unit
			Min	Max	Min	Max	
SCL clock frequency		f_{SCL}	0	100	0	400	kHz
Start condition hold time		$t_{HD;STA}$	4.0	-	0.6	-	μs
SCL clock Low width (Input) (Note 1)		t_{LOW}	4.7	-	1.3	-	
SCL clock High width (Input) (Note 2)		t_{HIGH}	4.0	-	0.6	-	
Re-start condition setup time	<SREN>=0	$t_{SU;STA}$	4.7(Note5)	-	0.6(Note5)	-	
	<SREN>=1		4.7(Note5)	-	0.6		
Data hold time (Input) (Note 3, 4)		$t_{HD;DAT}$	0	-	0	-	
Data setup time		$t_{SU;DAT}$	250	-	100	-	ns
Stop condition setup time		$t_{SU;STO}$	4.0	-	0.6	-	μs
Bus free time between stop condition and start condition (Note 5)		t_{BUF}	4.7	-	1.3	-	
pulse width of spikes that must be suppressed by the input filter		t_{SP}	-	-	0	50	ns
rise time of both SDA and SCL signals		t_r	-	1000	20	300	
fall time of both SDA and SCL signals		t_f	-	300	20 × (V_{DD}/5.5V)	300	

Note1: SCL clock low level width (output): $p \times (2^{n+1}+10)/T$ (***[I2CxOP]***<NFSEL>=0)

Note2: SCL clock high level width (output): $p \times (2^{n+1}+6)/T$ (***[I2CxOP]***<NFSEL>=0)
On I²C bus standard, the maximum speed of standard mode/fast mode is 100kHz/400 kHz respectively. Note that an internal SCL clock frequency is determined by the fsys and the calculation of Note 1 and Note 2 above-mentioned.

Note3: The data hold time (output) is equal to four cycles of the prescaler clock (Tprsck) started from the internal SCL.

Note4: On I²C bus standard, it is described that a data internal hold time should be set at least 300 ns to avoid unstable condition on the falling of the SCL when the SDA is input; however, this precaution is not supported in this MCU. Also, the edge slope control function for the SCL is not available. Therefore, when the customer designs the MCU, make sure to follow the data hold time (input) in the table above. Note that tr/tf on the SCL/SDA should be included in the data hold time.

Note5: To keep the time by software.

Not Recommended for New Design

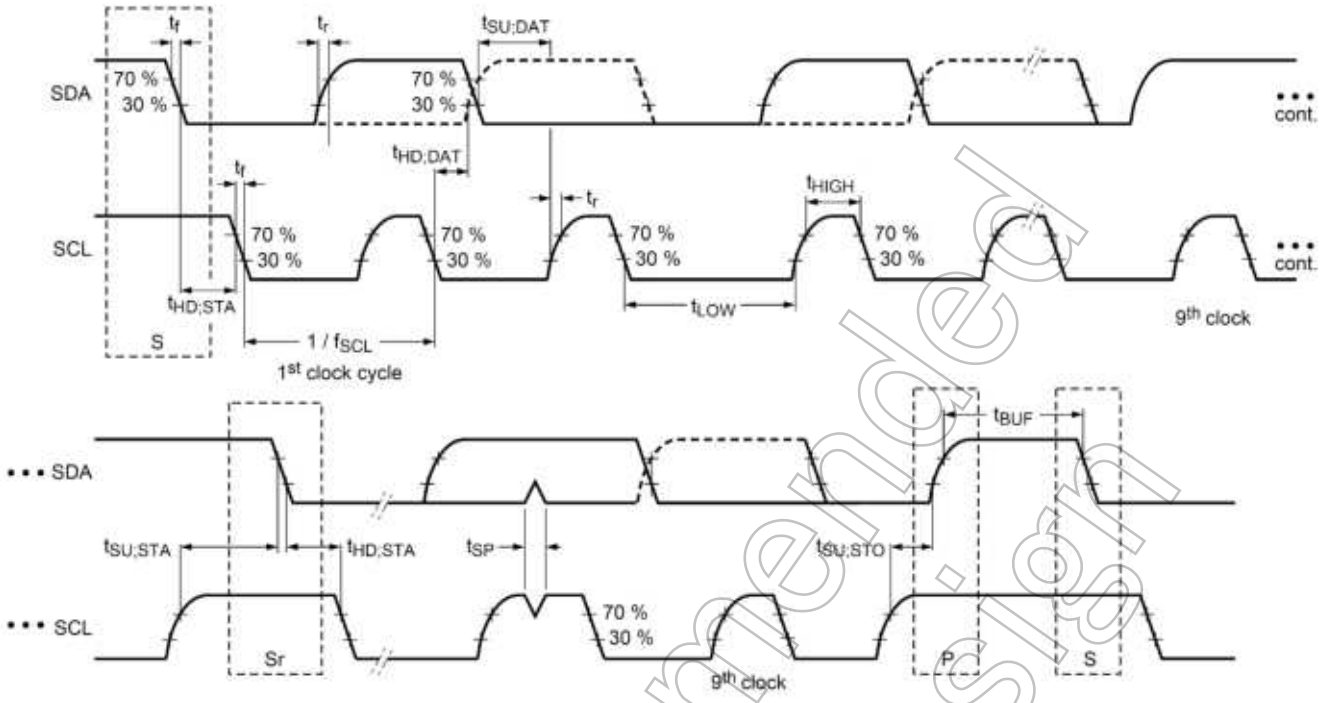


Figure 7.4 AC timing of I²C

Not Recommended for New Design

7.10.3. 32-bit Timer Event Counter (T32A)

This section describes the AC characteristics of T32AxINA0/A1, T32AxINB0/B1, and T32AxINC0/C1.

7.10.3.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5=2.7V to 5.5V
- Ta = -40 to 85°C
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.10.3.2. AC Characteristics

"T" in the table below indicates the operation clock cycle of the T32A. The operation clock of the T32A is the same cycle as the ΦT0 clock. This cycle is depending on the Prescaler Clock setting.

(1) Operation other than the pulse count

Parameter	Symbol	Equation		ΦT0 =80 MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{VCKL}	2T + 20	-	45	-	ns
High level pulse width	t_{VCKH}	2T + 20	-	45	-	

(2) At the pulse count

Parameter	Symbol	Equation		ΦT0 =80 MHz NF=4		Unit
		Min	Max	Min	Max	
Pulse cycle	t_{DCYC}	1000	-	1000	-	ns
Low level pulse width	t_{PWL}	500	-	500	-	
High level pulse width	t_{PWH}	500	-	500	-	
Input setup	t_{ABS}	(NF+1)×T+20	-	82.5	-	
Input hold	t_{ABH}	(NF+1)×T+20	-	82.5	-	

NF Value is depending on the ***[T32AxPLSCR]***<NF[1:0]> setting as follows.

[T32AxPLSCR]<NF[1:0]>	NF Value of Formula
00	0
01	2
10	4
11	8

Not Recommended for New Design

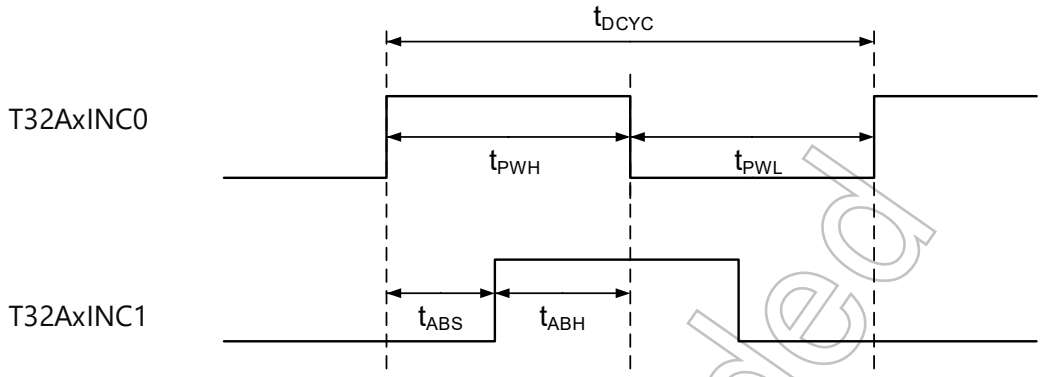


Figure 7.5 Count Pulse input

7.10.4. External Interrupt

7.10.4.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5=2.7V to 5.5V
- Ta = -40 to 85°C
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.10.4.2. AC Electrical Characteristics

"T" in the table below indicates the cycle of the system clock (fsys).

(1) NORMAL, IDLE mode

Parameter	Symbol	Equation		fsys=80 MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{INTAL1}	T + 100	-	112.5	-	ns
High level pulse width	t_{INTAH1}	T + 100	-	112.5	-	

(4) STOP1, STOP2 mode

Parameter	Symbol	Equation		fsys=80 MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{INTCL2}	125	-	125	-	ns
High level pulse width	t_{INTCH2}	125	-	125	-	

Not Recommended for New Design

7.10.5. Trigger Input (TRGINx)

7.10.5.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5 = 2.7V to 5.5V
- Ta = -40 to 85°C
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.10.5.2. AC Electrical Characteristics

"T" in the table below indicates the cycle of the system clock (fsys).

Parameter	Symbol	Equation		fsys=80 MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{ADL}	2T + 20	-	45	-	ns
High level pulse width	t_{ADH}	2T + 20	-	45	-	

Not Recommended for New Design

7.10.6. Debug Communication

7.10.6.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7V to 5.5V
- Ta = -40 to 85°C
- Output level: High = 0.8 ×DVDD5, Low = 0.2×DVDD5
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.10.6.2. SWD Interface

4.5V ≤DVDD5=AVDD5≤ 5.5V

Parameter	Symbol	Min	Max	Unit
CLK cycle	t_{dck}	100	-	ns
Output data hold time from the rising edge of CLK	t_{d1}	4	-	
Output data valid time from the rising edge of CLK	t_{d2}	-	33	
Input data valid time from the rising edge of CLK	t_{ds}	20	-	
Input data hold time from the rising edge of CLK	t_{dh}	15	-	

2.7V ≤DVDD5=AVDD5< 4.5V

Parameter	Symbol	Min	Max	Unit
CLK cycle	t_{dck}	100	-	ns
Output data hold time from the rising edge of CLK	t_{d1}	4	-	
Output data valid time from the rising edge of CLK	t_{d2}	-	45	
Input data valid time from the rising edge of CLK	t_{ds}	20	-	
Input data hold time from the rising edge of CLK	t_{dh}	15	-	

Not Recommended for New Design

7.10.6.3. JTAG Interface

4.5V ≤DVDD5=AVDD5≤ 5.5V

Parameter	Symbol	Min	Max	Unit
CLK cycle	t_{dck}	100	-	ns
Output data hold time from the rising edge of CLK	t_{d3}	4	-	
Output data valid time from the rising edge of CLK	t_{d4}	-	33	
Input data valid time from the rising edge of CLK	t_{ds}	20	-	
Input data hold time from the rising edge of CLK	t_{dh}	15	-	

2.7V ≤DVDD5=AVDD5< 4.5V

Parameter	Symbol	Min	Max	Unit
CLK cycle	t_{dck}	100	-	ns
Output data hold time from the rising edge of CLK	t_{d3}	4	-	
Output data valid time from the rising edge of CLK	t_{d4}	-	45	
Input data valid time from the rising edge of CLK	t_{ds}	20	-	
Input data hold time from the rising edge of CLK	t_{dh}	15	-	

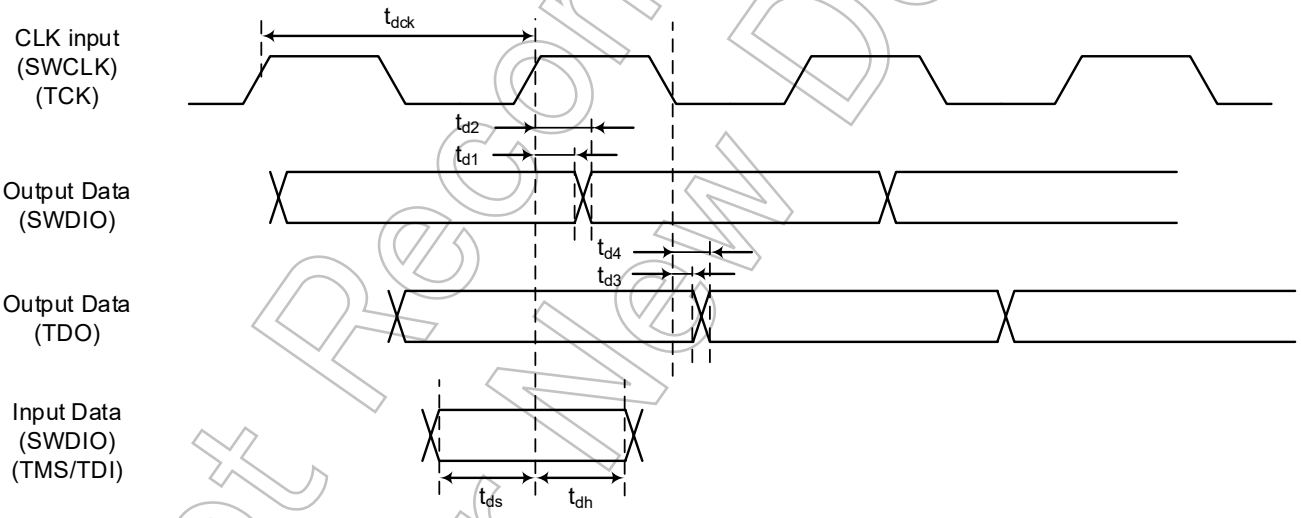


Figure 7.6 JTAG/SWD waveform

Not Recommended for New Design

7.10.6.4. ETM Trace

4.5V≤DVDD5=AVDD5≤ 5.5V

Parameter	Symbol	Min	Max	Unit
TRACECLK cycle	t_{tclk}	50	-	ns
Data valid time from rising on TRACECLK	t_{setupr}	2	-	
TRACEDATA hold time from the rising edge of TRACECLK	t_{holdr}	1	-	
TRACEDATA valid time from the falling edge of TRACECLK	t_{setupf}	2	-	
TRACEDATA hold time from the falling edge of TRACECLK	t_{holdf}	1	-	

2.7V ≤DVDD5=AVDD5< 4.5V

Parameter	Symbol	Min	Max	Unit
TRACECLK cycle	t_{tclk}	100	-	ns
Data valid time from rising on TRACECLK	t_{setupr}	2	-	
TRACEDATA hold time from the rising edge of TRACECLK	t_{holdr}	1	-	
TRACEDATA valid time from the falling edge of TRACECLK	t_{setupf}	2	-	
TRACEDATA hold time from the falling edge of TRACECLK	t_{holdf}	1	-	

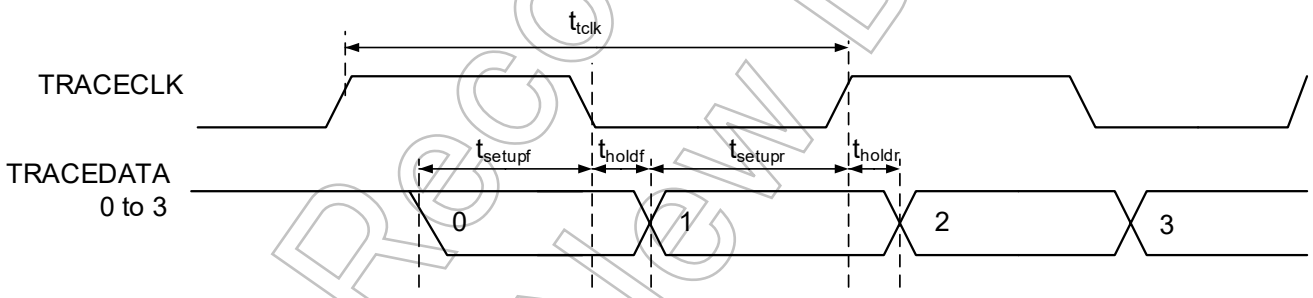


Figure 7.7 Trace signal waveform

Not Recommended for New Design

7.10.7. SCOUT Pin

7.10.7.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5= AVDD5= 2.7V to 5.5V
- Ta = -40 to 85°C
- Output level: High = 0.8 × DVDD5, Low = 0.2 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.10.7.2. AC Electrical Characteristics

"T" in the table indicates the cycle of the SCOUT output waveform.

Parameter	Symbol	Equation		SCOUT = 20MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{SCL}	0.5T- 10	-	15	-	ns
High level pulse width	t_{SCH}	0.5T- 10	-	15	-	

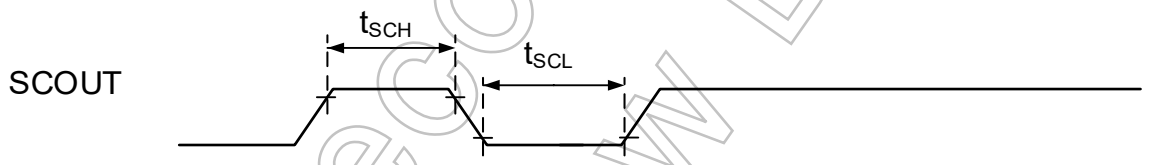


Figure 7.8 SCOUT wave output

7.10.8. Noise Filter Characteristics

Parameter	Condition	Min	Typ.	Max	Unit
Noise cancel width	-	15	30	60	ns

Not Recommended for New Design

7.10.9. External Clock Input

7.10.9.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7V to 5.5V
- Ta = -40 to 85°C
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.10.9.2. AC Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit
Clock frequency($1/t_{ehcin}$)	$f_{EHCLKIN}$	6	-	20	MHz
Clock duty	-	45	-	55	%
Clock rise time	t_r	-	-	10	ns
Clock fall time	t_f	-	-	10	ns

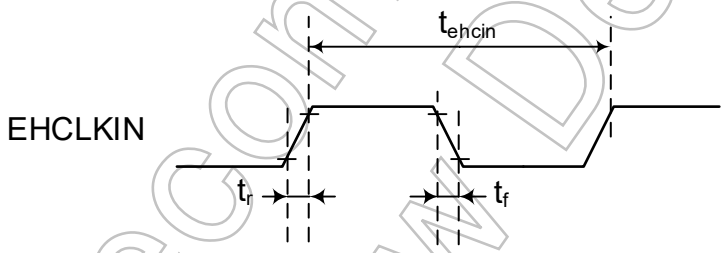


Figure 7.9 External clock input waveform

Not Recommended for New Design

7.11. Flash Memory Characteristics

7.11.1. Code Flash

DVDD5=2.7V to 5.5V
Ta=-40 to 85°C

Parameter	Condition	Min	Typ.	Max	Unit
Endurance	-	-	-	10,000	cycles
Programming time	Word Program time	-	29.5	-	μs
Erase time	Page Erase time	1.1	-	4.3	ms
	Block Erase time	8.6	-	34	
	Area Erase time(Note2)	-	9.2	-	

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B.
Note2: No block with effective protection.

7.11.2. Data Flash

DVDD5=2.7V to 5.5V
Ta=-40 to 85°C

Parameter	Condition	Min	Typ.	Max	Unit
Endurance	-	-	-	100,000	cycles
Programing time	-	-	64.7	-	μs
Erase time	Page Erase time	1	-	3.9	ms
	Block Erase time	15.4	-	62.1	
	Area Erase time(Note2)	-	9.2	-	

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B.
Note2: No block with effective protection.

7.11.3. Chip Erase

DVDD5= 2.7V to 5.5V
Ta= -40 to 85°C

Parameter	Condition	Min	Typ.	Max	Unit
Chip Erase time	Erasing of Code Flash, Data Flash, Protect Bits(Code), Protect Bits(Data), User Information Area and Security bits	23.4	-	62.7	ms

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B.
Note2: When Chip Erase command executes, no block with effective protection.

Not Recommended for New Design

7.12. Regulator

Parameter	Condition	Min	Typ.	Max	Unit
Capacitance of REGOUT1 capacitor	DVDD5=2.7Vto 5.5V Ta=-40 to 85°C	-	4.7	-	μF
Capacitance of REGOUT2 capacitor		-	4.7	-	

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.13. Oscillation Circuit

7.13.1. Internal Oscillator

DVDD5= 2.7V to 5.5V
Ta= -40 to 85°C

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Oscillation frequency	f_{IHOSC1}	Factory out, IC data (Note2)	-	10	-	MHz
	f_{IHOSC2}		-	10	-	

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B.

Note2: Not included the influence depend on the variations after Factory shipping. Please execute IHOSC1 oscillator adjustment by the trimming register, if it is required. IHOSC2 oscillator cannot be adjusted.

7.13.2. External Oscillator

DVDD5= 2.7V to 5.5V
Ta= -40 to 85°C

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Oscillation frequency	f_{EHOSC}	-	6	-	12	MHz
	f_{ELOSC}		30	-	34	kHz

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B.

Note2: Please contact the oscillator vendor, regarding the matching data of the device and the oscillator.

Not Recommended for New Design

7.13.3. Oscillation Circuit

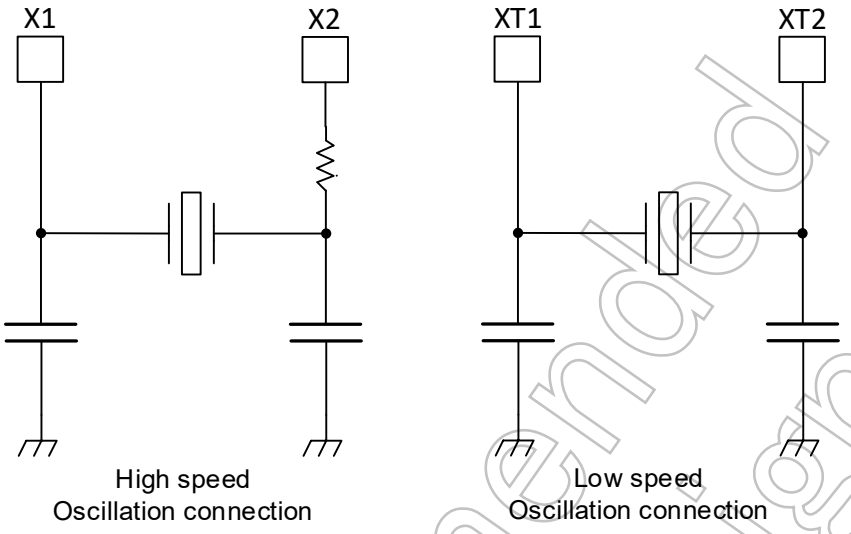


Figure 7.10 Oscillation circuit sample

To obtain a stable oscillation, load capacity and the position of the oscillator must be configured properly.

Since these factors are strongly affected by substrate patterns, please evaluate oscillation stability using the substrate you use.

This product has been evaluated by the oscillator vendor below. Please refer to this information when selecting external parts.

7.13.4. Ceramic resonator

This product has been evaluated by the ceramic resonator by Murata Manufacturing Co., Ltd.

Please refer to the Murata Website for details.

7.13.5. Crystal unit

This product has been evaluated by the crystal unit by KYOCERA Corporation.

Please refer to the KYOCERA Website for details.

7.13.6. Precautions for designing printed circuit board

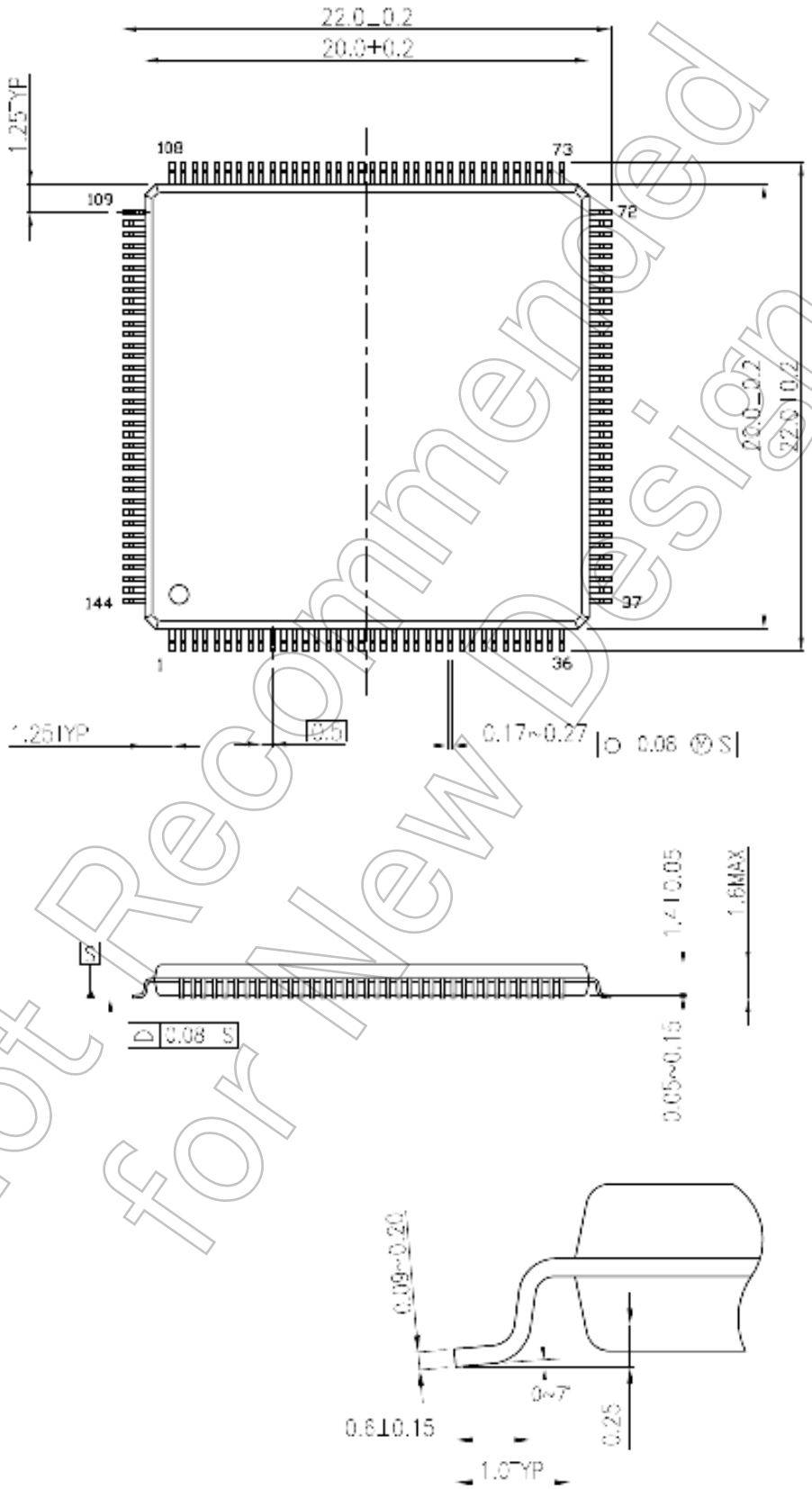
Be sure to design printed circuit board patterns that connect a crystal unit with other oscillation elements so that the length of such patterns become shortest possible to prevent deterioration of characteristics due to stray capacitances and wiring inductance. For multi-layer circuit boards, it is important not to wire the ground and other signal patterns right beneath the oscillation circuit. For more information, please refer to the URL of the crystal unit vendor.

Not Recommended for New Design

8. Package Dimensions

8.1. P-LQFP144-2020-0.50-002

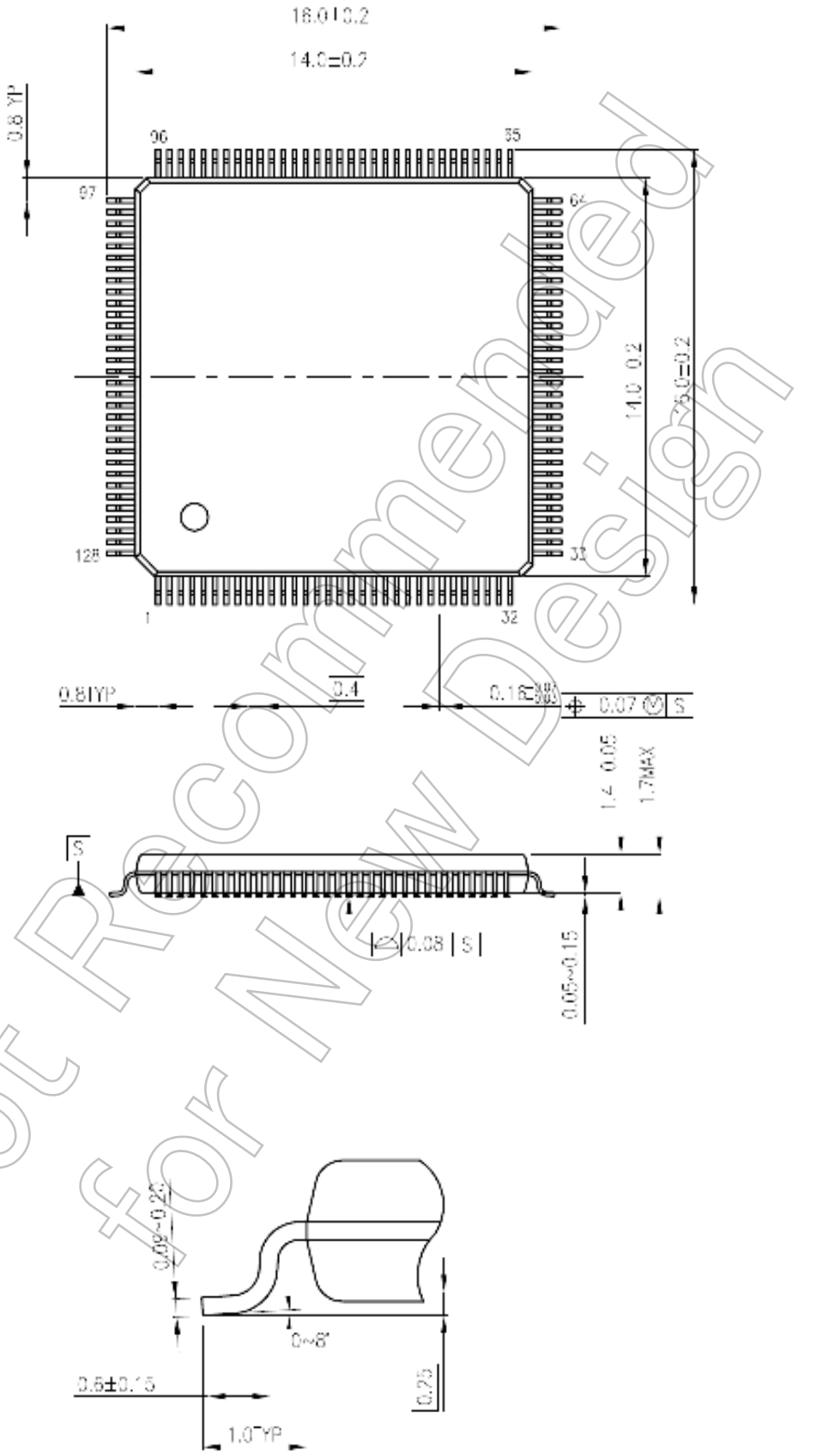
Unit: mm



Not Recommended for New Design

8.2. P-LQFP128-1414-0.40-001

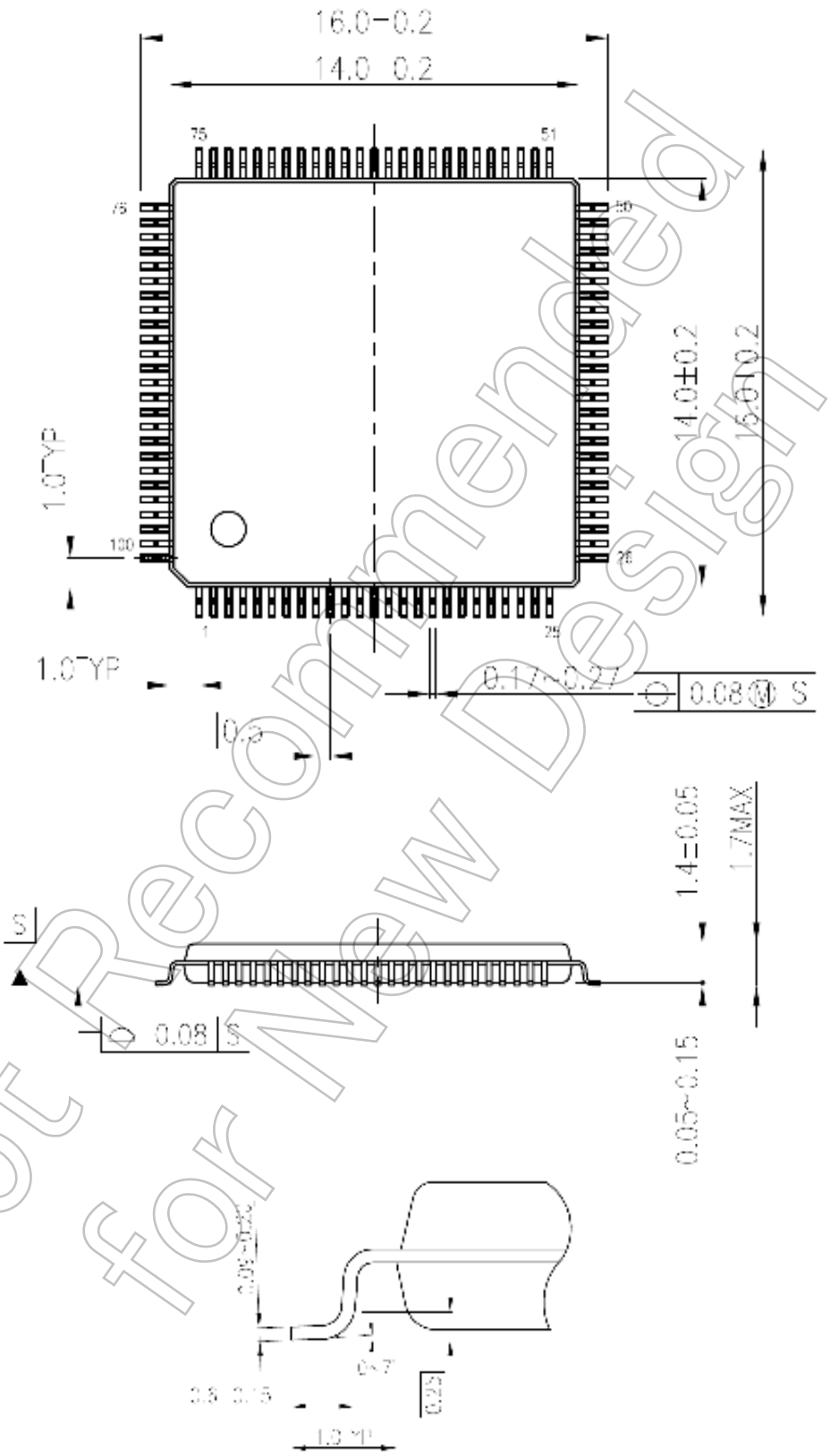
Unit: mm



Not Recommended for New Design

8.3. P-LQFP100-1414-0.50-002

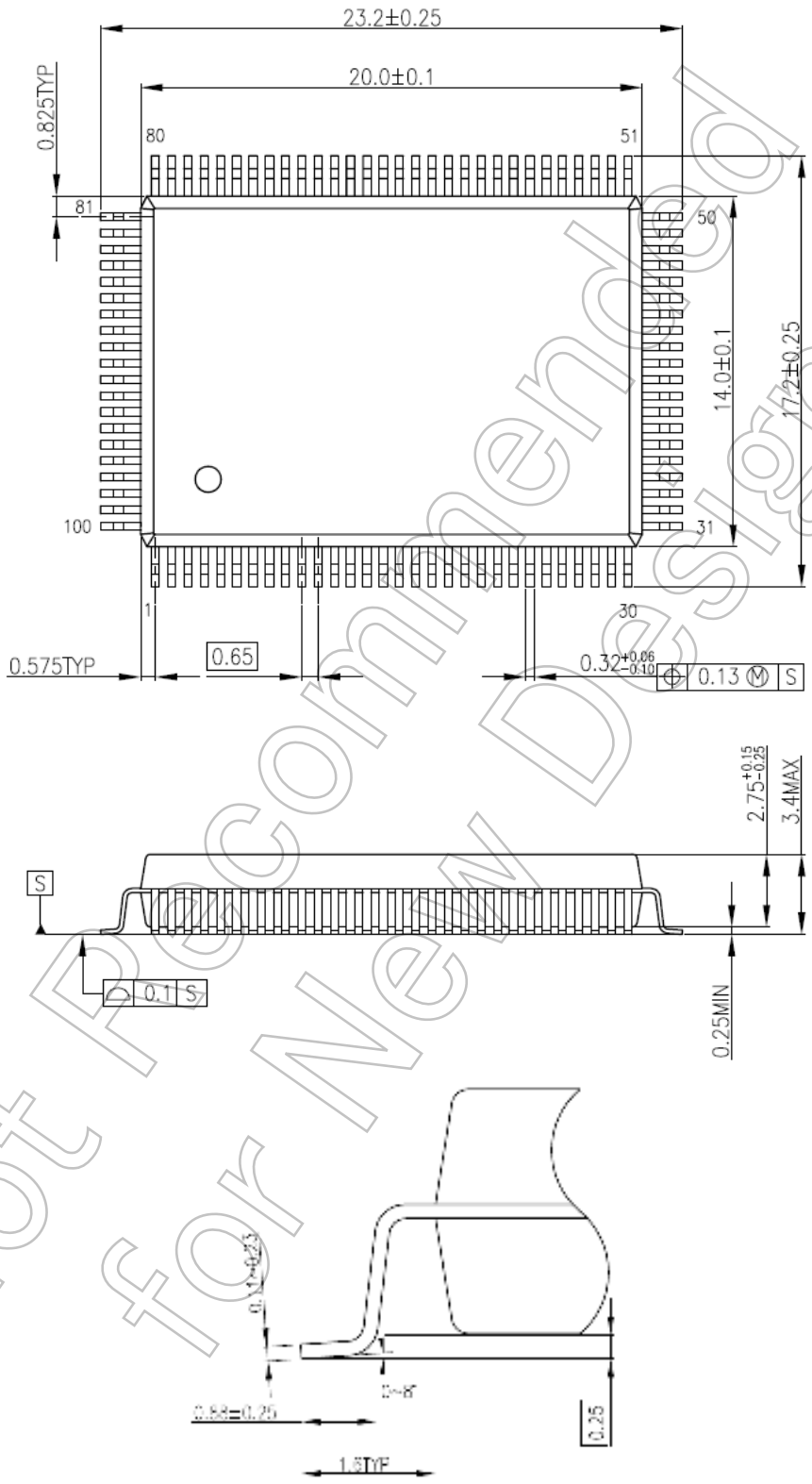
Unit: mm



Not Recommended for New Design

8.4. P-QFP100-1420-0.65-001

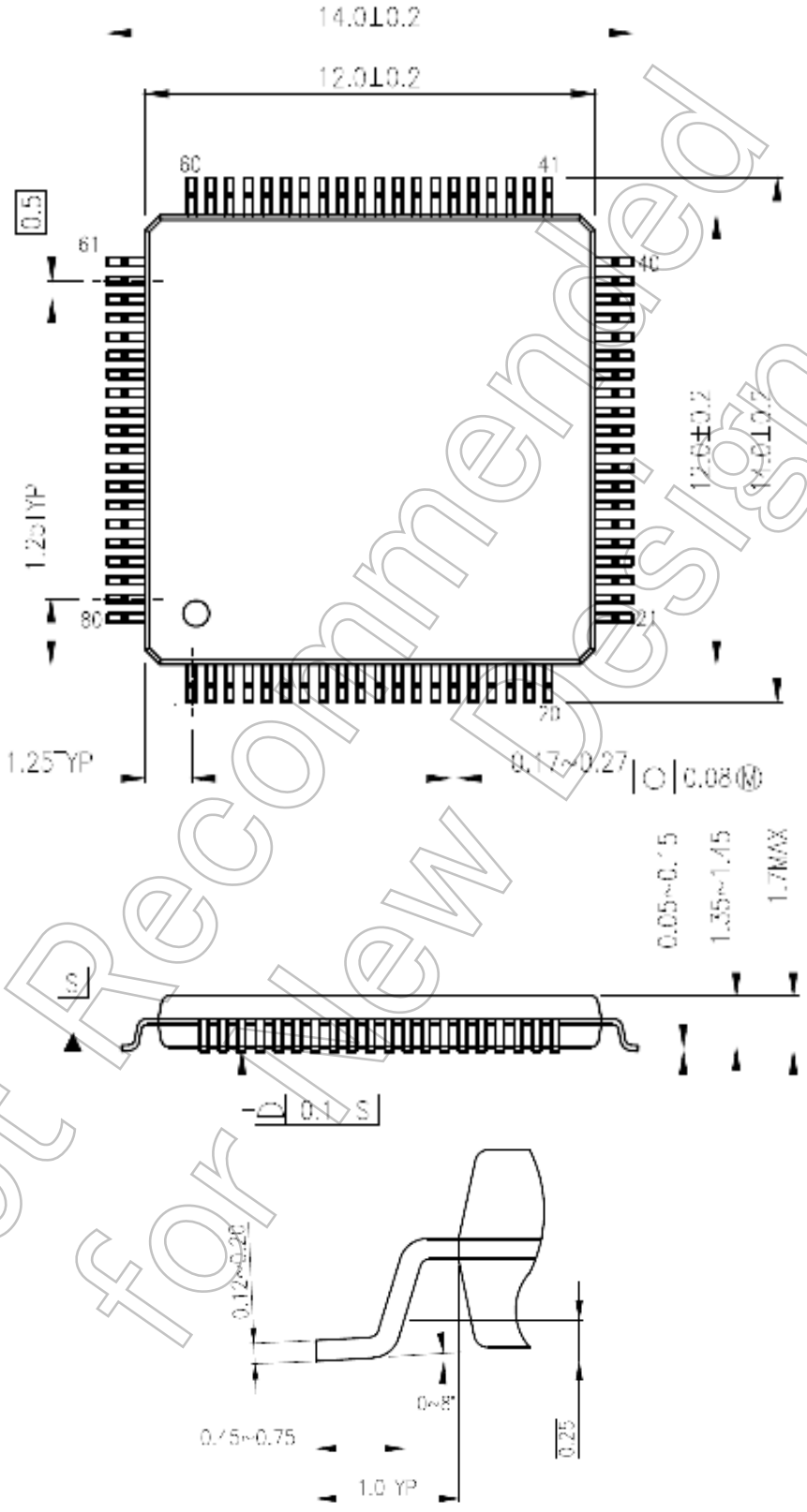
Unit: mm



Not Recommended for New Design

8.5. P-LQFP80-1212-0.50-003

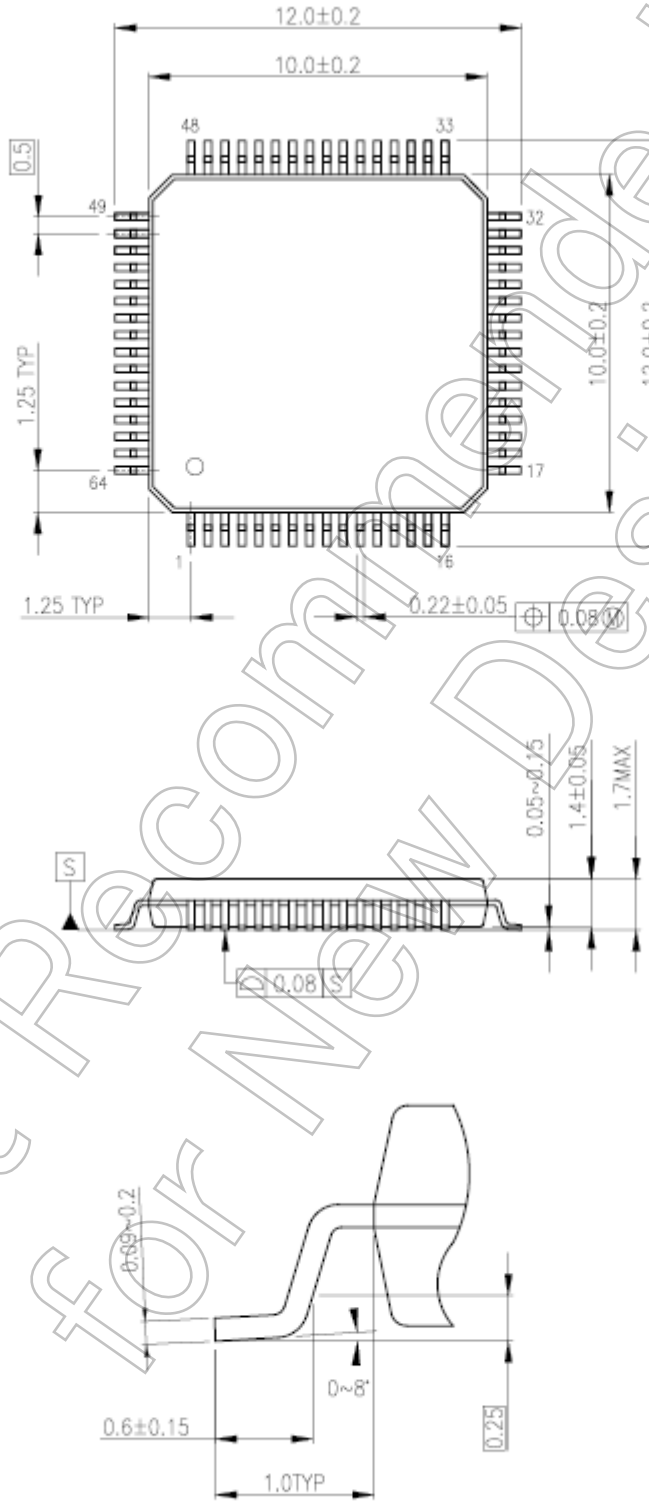
Unit: mm



Not Recommended for New Design

8.6. P-LQFP64-1010-0.50-003

Unit : mm



Not Recommended for New Design

9. Precautions

This Page explains general precautions on the use of Toshiba MCUs.

Note that if there is a difference between the general precautions and the description in the body of the document, the description in the body of the document has higher priority.

(1) The MCUs' operation at power-on

At power-on, the internal state of the MCUs is unstable. Therefore, the state of the pins is undefined until the reset operation is completed.

When a reset is performed by an external reset pin, pins of the MCUs that use the reset pin are undefined until reset operation by the external pin is completed.

Also, when a reset is performed by the internal power-on reset, pins of the MCUs that use the internal power-on reset are undefined until power supply voltage reaches the voltage at which power- on reset is valid.

(2) Unused pins

Unused input/output ports of the MCUs are prohibited to use. The pins are high-impedance.

Generally, if MCUs operate while the high-impedance pins left open, electrostatic damage or latch- up may occur in the internal LSI due to induced voltage influenced from external noise.

We recommend that each unused pin should be connected to the power supply pins or GND pins via resistors.

(3) Clock oscillation stability

A reset state must be released after the clock oscillation becomes stable. If the clock is changed to another clock while the program is in progress, wait until the clock is stable.

Not Recommended for New Design

10. Revision History

Table 10.1 Revision History

Revision	Date	Description
1.0	2018-10-25	New Release
2.0	2018-03-27	-General Description Modified “ARM” to “Arm”“256K to 512K bytes” to “256 to 512KB” and “32K bytes” to “32KB”, Deleted “(14x14mm,0.65mm pitch)” in the figure. -Features OFD: Corrected “detection” to “detector”, LVD: Deleted "low", added “circuit”. UART:Corrected to “Asynchronous Serial Communication Circuit”, "2.4Mbps" to "2.5Mbps". RMC: Corrected to “control signal preprocessor”. -Products Lists Categorized by Functions Table1: Modified "Products lists(1)" to "Products List", Deleted TMPM3HMF…TMPM3HMFYDFG. -Preface: Modified description about Arm. -Terms and Abbreviations Corrected A-PMD,DMAC,EHOSC,ELOSC,IHOSC,I2CS,POR,RAMP,RMC,SIWDT, T32A -1.Block Diagram: Added RAMP and modified DMAC,PORT,I2CS in Figure1.1. -2.5.LQFP80: Deleted TMPM3HMF…TMPM3HMFYDFG. -3.1.List of Memory Sizes: Deleted TMPM3HMF…TMPM3HMFYDFG in Table3.1. -4.1.1.Function Pins of Peripheral Corrected "timer" to "timer A" at T32AxOUTA in Table4.1. -4.1.2.Debug Pins: Modified "Function" to "Debug Port" in Table4.2. -4.1.3.Control Pins./ 4.1.4. Power Supply Pins: Deleted "Function" in Table4.3./4.4 -4.2.Functional Pin and Ports Assignment Modified description “terminal” to “pin”, Corrected "conection" to "connection" of Table4.5, Added and modified in table4.17. -4.3.Ports: Delete “State” about reset state. -5.1.Reference Manuals Deleted "(Version x)" in Table5.1, Corrected “Driver” to “Control Circuit” at A-PMD-B. -5.7.Oscillation Frequency Detector: Corrected to “Oscillation Frequency Detector”. -5.14. I^2C Interface: Corrected -5.15.8-bit Digital to Analog Converter: Modified to “Digital to Analog”. -5.16.12-bit Analog to Digital Converter: Modified to “Analog to Digital”. - 5.17.Comparator (COMP): Corrected. - 5.22.Clock Selective Watchdog Timer Corrected “internal oscillator“ to “internal oscillator1“, “oscillator for the OFD” to “oscillator2”. -5.23.Remote control signal preprocessor: Corrected. -6.1.PORT:Corrected Figure PA6,PA7...PV3, PH0 to PH3. -6.3.Control Pin: Added “MODE pin….” Figure MODE -6.4.Clock control:Modified Figure X1,X2 and XT1,XT2 -7.1.Absolute Maximum Ratings Table7.1:Modified port description.,modified Rating of AVDD5 and added “(Note1)”, Added Note1. -7.2.DC Electrical Characteristics (1/2): Corrected Condition of VDD Modified port description in table. -7.3.DC Electrical Characteristics (2/2): Corrected “detai” to “detail” STOP1,STOP2 Typ. value in table. Table7.2: Corrected “High-speed frequency” to “High speed”, "oscillator(IHOSC)" to "oscillator1 (IHOSC1)", “Low-speed” to “External low speed”, "LOSC" to "ELOSC". Deleted "LOSC=…" under Table7.2. -7.4.12-bit AD Converter Characteristics: Modified Condition and Specification in table. Added “(Note3)” in “Conversion time”. Added Note3. 7.5.8-bit DA Converter Characteristics: Corrected "=4MΩ" to "=10MΩ" in table. -7.7.Characteristics of Internal processing at RESET Modified “4” to “0.01” in V_{PON}(Min) of the table. -7.8.Characteristics of Power On Reset: Corrected. -7.9.Characteristics of Voltage Detection Circuit Corrected “250” to “200” in t_{VDDT1}(Max) of the table. -7.10.1.2.AC Electrical Characteristics: Corrected “***[TSPIxSCK]***” to “TSPIxSCK”. -7.10.2. I^2C Interface: Corrected. -7.10.2.1.AC Measurement Conditions: Deleted “Pull-up resistor: 200Ω” in condition.

Not Recommended for New Design

		-7.10.3. 32-bit Timer Event Counter: Corrected. -7.10.3.2. AC Characteristics: Corrected Symbol in table “(2)At the puls count” and signal name in Figure7.6. - 7.13.3.Oscillation Circuit: Modified “frequency” to “speed”. -7.13.4.Ceramic Oscillator/7.13.5.Crystal Oscillator Modified description, Deleted "the URL". - 8.6.: Deleted P-LQFP80-1414-0.65-001 -List of All pins: Corrected “PU” to “Pull-up/Pull-down” in the table(1)/(2) -Part Naming Conventions: “ARM” to “Arm”, “Cortex-M4” to ”Cortex-M4 with FPU”.
3.0	2018-07-10	- Footer: added Production Date - General Description added 64-pin Package - Features: Modified the value of Interruption, I^2C and TSPI channels number Modified Number of Interruption and I/O Ports - Products Lists: added M3HL to Product List - Preface sentence of registered trademark of SST was modified -1 Block Diagram: added RAMP block, Modified DMAC, PORT and TSPI in the block - 2. Pin Assignment: added the 2.6 of M3HL. -3.1 added M3HL to Memory Size and Address table. -4.2 added M3HL to Signal connection List. - 5.2 & 5.2.1 changed the word from ARM to Arm - 5.5 From to 5.25 added M3HL to supported product table. - 5.12 Section title modified - 5.14 Note2 modified - 7.3 Table 7.3 modified UART Transmission(2.4Mbps) → Transmission(2.5Mbps) - 7.4 Note2 modified. - 7.10.1.2 TSPI Deleted Fig 7.2. (1st Clock edge sampling(Slave)) Parameter modified of t_{ODLY1} in (1),(2),(3),(4)and(5) -8. Package Dimensions: added the PKG of M3HL in 8.6 -Appendix List of All pins: added the list of M3HL.
3.1	2018-07-25	-5.10 Table 5.9 modified Port Name(PK3→PL3, PK4→PL2,PK5→PL1,PK6→PL0)
3.2	2019-08-19	- Layout changed about the Date and the Copyright - Table 1 DMC ch 54 → 53 in M3HL, changed RMC into other peripherals, added RAMP in system function - 1. Figure 1.1 modified "54" → "53" in DMAC - 2.6 LQFP64 Pin Assigment is modified(57pin: deleted TSPI3RXD) - 4.1.5 Added the section about "Capacitors between power supply pins". - 5.14. Note2 modified "The Slave address match" →"The address match". - 6.1 Port changed from "PP0 to PP7" to "PP0 to PP2,PP4 to PP7". - 7.7 changed from "T" to "t". - 7.10.1.2 (1) ,(2) added "k1=k2=1" parameter. (3) added "k1=1" parameter. modified t_{CSU1}: "(t_{CYC} x (k1 + 0.5)) +15" →"(t_{CYC} x (k1 + 0.5)) +20", t_{CSU2} : " (t_{CYC} x k1) - 15" →"(t_{CYC} x k1) - 20". - 7.10.2.2 Revised the table(Changed $t_{SU,STA}$, Added t_{SP},t_r,t_f)and the Figure. - 7.10.3.2 (1) &(2) changed "fsys" to "ΦT0" , (2) added "NF=4" parameter. - Appendix The List of All pins(4) is modified. (TSPI ch3 is deleted) - Revised "Part Naming Conventions" - RESTRICTIONS ON PRODUCT USE Modified contents
3.3	2021-01-21	- Footer modified (Copyright & boundary Line) - Features TSPI: Unit correction ("bps" to "MHz") - Terms and Abbreviations :modified of TSPI - 5.14 I2C: Unit correcttion ("bps" to "kHz")

Not Recommended for New Design

Appendix

List of All pins

Combination Function A to B: These are the functions which become effective without setting up port function registers.
Combination Function 1 to 6: These are the functions which become effective with setting up port function registers.

List of All pins (1)

M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	Pin Name	Combination Function A	Combination Function B	Combination Function 1	Combination Function 2	Combination Function 3	Combination Function 4	Combination Function 5	Combination Function 6	Input/Output	Pull-up/ Pull-down	5V_T	SMT/ CMOS	Under Reset	After Reset
1	1	1	3	1	PE1	AINA05								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
2	2	2	4	2	PE0	AINA04								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
3	3	3	5	–	PD3	AINA03								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
4	4	4	6	3	PD2	AINA02								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
5	5	5	7	4	PD1	AINA01								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
6	6	6	8	5	PD0	AINA00								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
7	7	7	9	6	AVDD5									–	–	–	–	–	–
8	8	8	10	7	AVSS									–	–	–	–	–	–
9	9	9	11	8	PG0	DAC0								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
10	10	10	12	9	PG1	DAC1								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
11	–	–	–	–	PU5									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
12	–	–	–	–	PU4									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
13	–	–	–	–	PU3									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
14	–	–	–	–	PU2									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
15	11	–	–	–	PG2		INT27	UT3RXD	UT3TXDA	T32A07OUTA	T32A07OUTC			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
16	12	–	–	–	PG3		INT28	UT3TXDA	UT3RXD	T32A07INA0	T32A07INC0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
17	13	–	–	–	PG4			UT3TXDB		T32A07INA1	T32A07INC1			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
18	14	–	–	–	PG5					T32A07OUTB				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
19	15	–	–	–	PG6					T32A07INB0				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
20	16	–	–	–	PG7					T32A07INB1				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
21	17	11	13	10	PA7		INT11	UT3TXDA	UT3RXD					I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
22	18	12	14	11	PA6		INT07	UT3RXD	UT3TXDA					I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
23	19	13	15	12	PA5			I2C1SDA			T32A00INB1			I/O	PU/PD	T	SMT	Hi-z	Hi-z
24	20	14	16	13	PA4			I2C1SCL		TSPI0CS1	T32A00INB0			I/O	PU/PD	T	SMT	Hi-z	Hi-z
25	21	15	17	14	PA3				TSPI0CSIN	TSPI0CS0	T32A00OUTB		TRGIN1	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
26	22	16	18	15	PA2			UT0RXD	UT0TXDA	TSPI0RXD	T32A00INA1	T32A00INC1	ENC0Z	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
27	23	17	19	16	PA1			UT0TXDA	UT0RXD	TSPI0TXD	T32A00INA0	T32A00INC0	ENC0B	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
28	24	18	20	17	PA0			UT0TXDB		TSPI0SCK	T32A00OUTA	T32A00OUTC	ENC0A	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
29	25	–	–	–	PM7									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
30	26	19	21	–	PM6		INT15							I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
31	27	20	22	–	PM5						T32A00INB1			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
32	28	21	23	–	PM4			UT0RTS_N	UT0CTS_N	TSPI0CS1	T32A00INB0		TRACEDATA3	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
33	29	22	24	–	PM3			UT0CTS_N	UT0RTS_N	TSPI0CS0	T32A00OUTB	TSPI0CSIN	TRACEDATA2	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
34	30	23	25	18	PM2		INT09	UT0RXD	UT0TXDA	TSPI0RXD	T32A00INA1	T32A00INC1	TRACEDATA1	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
35	31	24	26	19	PM1			UT0TXDA	UT0RXD	TSPI0TXD	T32A00INA0	T32A00INC0	TRACEDATA0	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
36	32	25	27	20	PM0			UT0TXDB		TSPI0SCK	T32A00OUTA	T32A00OUTC	TRACECLK	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
37	33	26	28	21	PB0	BOOT_N					T32A01OUTA	T32A01OUTC	SCOUT	Output	PU/PD	N/A	SMT	Hi-z(Note1)	Hi-z
38	34	27	29	22	PB1		INT03	RXIN0			T32A01INA0	T32A01INC0	TRGIN0	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
39	35	28	30	23	PB2			UT2TXDA	UT2RXD	TSPI1SCK	T32A01INA1	T32A01INC1		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
40	36	29	31	24	PB3			UT2RXD	UT2TXDA	TSPI1TXD	T32A01OUTB			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
41	37	30	32	25	PB4			UT2CTS_N	UT2RTS_N	TSPI1RXD	T32A01INB0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
42	38	31	33	–	PB5			UT2RTS_N	UT2CTS_N	TSPI1CS0	T32A01INB1	TSPI1CSIN		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
43	39	32	34	–	PB6					TSPI1CS1				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
44	40	33	35	–	PB7		INT16							I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
45	–	–	–	–	PU0		INT30							I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
46	–	–	–	–	PU1		INT31							I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
47	41	34	36	26	PL0			UT2TXDA	UT2RXD	I2C2SCL		TRST_N		I/O	PU/PD	N/A	SMT	PU(Note2)	PU(Note2)
48	42	35	37	27	PL1			UT2RXD	UT2TXDA	I2C2SDA		TDI		I/O	PU/PD	N/A	SMT	PU(Note2)	PU(Note2)
49	43	36	38	28	PL2			UT2CTS_N	UT2RTS_N	T32A06OUTB		TDO/SWV		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
50	44	37	39	29	PL3		INT08	UT2RTS_N	UT2CTS_N	T32A06INB0		TCK/SWCLK		I/O	PU/PD	N/A	SMT	PD(Note2)	PD(Note2)
51	45	38	40	30	PL4		INT12			T32A06INB1		TMS/SWDIO		I/O	PU/PD	N/A	SMT	PU(Note2)	PU(Note2)
52	46	39	41	–	PL5					T32A06OUTA	T32A06OUTC			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
53	47	40	42	–	PL6					T32A06INA0	T32A06INC0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
54	48	–	–	–	PL7					T32A06INA1	T32A06INC1			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
55	–	–	–	–	PT7		INT29			T32A06INA1	T32A06INC1			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
56	–	–	–	–	PT6					T32A06INA0	T32A06INC0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
57	–	–	–	–	PT5					T32A06OUTA	T32A06OUTC			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
58	–	–	–	–	PT4			TSPI2RXD		T32A06INB1				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
59	49	–	–	–	PT3		INT26	TSPI2TXD		T32A06INB0				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
60	50	–	–	–	PT2		INT25	TSPI2SCK		T32A06OUTB				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
61	51	–	–	–	PT1		INT24	I2C3SCL	TSPI2CS0	TSPI2CSIN				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
62	52	–	–	–	PT0		INT23	I2C3SDA	TSPI2CS1					I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
63	53	41	43	31	PP0				TSPI2SCK	T32A01OUTA	T32A01OUTC			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
64	54	42	44	32	PP1				TSPI2TXD	T32A01INA0	T32A01INC0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
65	55	43	45	33	PP2				TSPI2RXD	T32A01INA1	T32A01INC1			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
66	56	44	46	34	DVDD5A									–	–	–	–	–	–
67	57	45	47	35	REGOUT2									–	–	–	–	–	–
68	58	46	48	36	REGOUT1									–	–	–	–	–	–
69	59	47	49	37	DVSSA									–	–	–	–	–	–
70	60	48	50	38	PH0	X1	EHCLKIN							Input	PD	N/A	SMT	Hi-z	Hi-z
71	61	49	51	39	PH1	X2								Input	PD	N/A	SMT	Hi-z	Hi-z
72	62	50	52	40	RESET_N										PU		SMT	–	–
73	63	51	53	41	PH2	XT1								Input	PD	N/A	SMT	Hi-z	Hi-z
74	64	52	54	42	PH3	XT2	INT06							Input	PD	N/A	SMT	Hi-z	Hi-z
75	65	53	55	43	MODE									–	PD	–	SMT	–	–
76	66	–	–	–	PH4		INT19	TSPI4SCK						I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
77	67	–	–	–	PH5		INT20	TSPI4TXD						I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
78	68	–	–	–	PH6		INT21	TSPI4RXD						I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
79	69	–	–	–	PH7		INT22							I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
80	–	–	–	–	PV5			UT4TXDB						I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
81	–	–	–	–	PV6			UT4TXDA	UT4RXD					I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
82	–	–	–	–	PV7			UT4RXD	UT4TXDA					I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
83	70	54	56	44	PC0		INT00	I2C0SCL		T32A02OUTA	T32A02OUTC			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
84	71	55	57	45	PC1		INT01	I2C0SDA		T32A02INA0	T32A02INC0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
85	72	56	58	46	PC2		INT02	UT4TXDB		T32A02INA1	T32A02INC1	RTCOUT		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
86	73	57	59	47	PC3			UT4TXDA	UT4RXD	T32A02OUTB				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
87	74	58	60	48	PC4			UT4RXD	UT4TXDA	T32A02INB0				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
88	75	59	61	49	PC5			UT4CTS_N	UT4RTS_N	T32A02INB1				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
89	76	60	62	50	PC6			UT4RTS_N	UT4CTS_N					I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
90	77	61	63	–	PR0					T32A02OUTA	T32A02OUTC			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
91	78	62	64	–	PR1					T32A02INA0	T32A02INC0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
92	79	63	65	–	PR2					T32A02INA1	T32A02INC1			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
93	80	64	66	–	PR3									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
94	81	–	–	–	PR4									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
95	82	–	–	–	PR5									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
96	83	–	–	–	PR6									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
97	84	–	–	–	PR7									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
98	85	65	67	–	PN5					T32A05INB1				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
99	86	66	68	51	PN4			UT5TXDB		T32A05INB0				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
100	87	67	69	52	PN3		INT10	UT5TXDA	UT5RXD	T32A05OUTB		TRGIN2		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z

Note1: When the RESET_N pin is "Low", a built-in pull-up resistor becomes effective.

Note2: The Initial value of built-in Pull-up/Pull-down resistor is effective.

TOSHIBA CONFIDENTIAL

List of All pins (2)

M3HQ (LQFP144)	M3HP (LQFP128)	M3HN (LQFP100)	M3HN (QFP100)	M3HM (LQFP80)	Pin Name	Combination Function A	Combination Function B	Combination Function 1	Combination Function 2	Combination Function 3	Combination Function 4	Combination Function 5	Combination Function 6	Input/Output	Pull-up/ Pull-down	5V_T	SMT/ CMOS	Under Reset	After Reset
101	88	68	70	53	PN2			UT5RXD	UT5TXDA	T32A05INA1	T32A05INC1			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
102	89	69	71	54	PN1			UT5CTS_N	UT5RTS_N	T32A05INA0	T32A05INC0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
103	90	70	72	55	PN0			UT5RTS_N	UT5CTS_N	T32A05OUTA	T32A05OUTC			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
104	91	71	73	56	PJ0			UT1TXDB		T32A03OUTA	T32A03OUTC	UO0		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
105	92	72	74	57	PJ1			UT1TXDA	UT1RXD	T32A03INA0	T32A03INC0	XO0		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
106	93	73	75	58	PJ2			UT1RXD	UT1TXDA	T32A03INA1	T32A03INC1	VO0		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
107	94	74	76	59	PJ3			UT1CTS_N	UT1RTS_N	T32A03OUTB		YO0		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
108	95	75	77	60	PJ4		INT04	UT1RTS_N	UT1CTS_N	T32A03INB0		WO0		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
109	96	76	78	61	PJ5					T32A03INB1		ZO0		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
110	97	77	79	62	PK0			UT1TXDB				EMG0		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
111	98	78	80	63	PK1		INT05	UT1TXDA	UT1RXD			OVV0		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
112	99	79	81	64	PK2			UT1RXD	UT1TXDA	T32A04OUTA	T32A04OUTC			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
113	100	80	82	65	PK3			UT1CTS_N	UT1RTS_N	T32A04INA0	T32A04INC0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
114	101	81	83	66	PK4			UT1RTS_N	UT1CTS_N	T32A04INA1	T32A04INC1			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
115	102	82	84	67	PK5					T32A04OUTB				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
116	103	83	85	68	PK6					T32A04INB0				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
117	104	84	86	69	PK7		INT13			T32A04INB1				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
118	105	85	87	70	PP3		INT14	TSPI3RXD						I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
119	106	86	88	71	PP4			TSPI3TXD						I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
120	107	87	89	72	PP5			TSPI3SCK						I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
121	108	88	90	73	PP6			TSPI3CS0	TSPI3CSIN	PMD0DBG				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
122	109	89	91	–	PP7			TSPI3CS1						I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
123	110	90	92	74	PV0									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
124	111	91	93	75	PV1									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
125	112	92	94	–	PV2		INT17							I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
126	113	93	95	–	PV3		INT18							I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
127	–	–	–	–	PV4									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
128	114	–	–	–	DVDD5B									–	–		–	–	–
129	115	–	–	–	DVSSB									–	–		–	–	–
130	–	–	–	–	PD5	AINA20								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
131	–	–	–	–	PD4	AINA19								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
132	116	–	–	–	PF7	AINA18								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
133	117	–	–	–	PF6	AINA17								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
134	118	–	–	–	PF5	AINA16								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
135	119	–	–	–	PF4	AINA15								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
136	120	–	–	–	PF3	AINA14								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
137	121	–	–	–	PF2	AINA13								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
138	122	94	96	–	PF1	AINA12								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
139	123	95	97	–	PF0	AINA11								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
140	124	96	98	76	PE6	AINA10								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
141	125	97	99	77	PE5	AINA09								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
142	126	98	100	78	PE4	AINA08								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
143	127	99	1	79	PE3	AINA07								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
144	128	100	2	80	PE2	AINA06								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z

Not Recommended for New Design

List of All pins (3)

M3HL (LQFP64)	Pin Name	Combination Function A	Combination Function B	Combination Function 1	Combination Function 2	Combination Function 3	Combination Function 4	Combination Function 5	Combination Function 6	Input/Output	Pull-up/ Pull-down	5V_T	SMT/ CMOS	Under Reset	After Reset
1	PE1	AINA05								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
2	PE0	AINA04								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PD3	AINA03								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
3	PD2	AINA02								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
4	PD1	AINA01								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
5	PD0	AINA00								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
6	AVDD5									-	-	-	-	-	-
7	AVSS									-	-	-	-	-	-
8	PG0	DAC0								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
9	PG1	DAC1								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PJ5									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PJ4									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PJ3									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PJ2									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PG2		INT27	UT3RXD	UT3TXDA	T32A07OUTA	T32A07OUTC			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PG3		INT28	UT3TXDA	UT3RXD	T32A07INA0	T32A07INC0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PG4			UT3TXDB		T32A07INA1	T32A07INC1			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PG5					T32A07OUTB				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PG6					T32A07INB0				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PG7					T32A07INB1				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
10	PA7		INT11	UT3TXDA	UT3RXD					I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
11	PA6		INT07	UT3RXD	UT3TXDA					I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PA5			I2C1SDA			T32A00INB1			I/O	PU/PD	T	SMT	Hi-z	Hi-z
-	PA4			I2C1SCL		TSPI0CS1	T32A00INB0			I/O	PU/PD	T	SMT	Hi-z	Hi-z
12	PA3				TSPI0CSIN	TSPI0CS0	T32A00OUTB		TRGIN1	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
13	PA2			UT0RXD	UT0TXDA	TSPI0RXD	T32A00INA1	T32A00INC1	ENC0Z	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
14	PA1			UT0TXDA	UT0RXD	TSPI0TXD	T32A00INA0	T32A00INC0	ENC0B	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
15	PA0			UT0TXDB		TSPI0SCK	T32A00OUTA	T32A00OUTC	ENC0A	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PM7									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PM6		INT15							I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PM5						T32A00INB1			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PM4			UT0RTS_N	UT0CTS_N	TSPI0CS1	T32A00INB0		TRACEDATA3	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PM3			UT0CTS_N	UT0RTS_N	TSPI0CS0	T32A00OUTB	TSPI0CSIN	TRACEDATA2	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PM2		INT09	UT0RXD	UT0TXDA	TSPI0RXD	T32A00INA1	T32A00INC1	TRACEDATA1	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PM1			UT0TXDA	UT0RXD	TSPI0TXD	T32A00INA0	T32A00INC0	TRACEDATA0	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
16	PM0			UT0TXDB		TSPI0SCK	T32A00OUTA	T32A00OUTC		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
17	PB0	BOOT_N					T32A01OUTA	T32A01OUTC	SCOUT	Output	PU/PD	N/A	SMT	Hi-z(Note1)	Hi-z
18	PB1		INT03	RXIN0			T32A01INA0	T32A01INC0	TRGIN0	I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
19	PB2			UT2TXDA	UT2RXD		T32A01INA1	T32A01INC1		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
20	PB3			UT2RXD	UT2TXDA		T32A01OUTB			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PB4			UT2CTS_N	UT2RTS_N	TSPI1RXD	T32A01INB0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PB5			UT2RTS_N	UT2CTS_N	TSPI1CS0	T32A01INB1	TSPI1CSIN		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PB6					TSPI1CS1				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PB7		INT16							I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PJ0		INT30							I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PJ1		INT31							I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
21	PL0			UT2TXDA	UT2RXD	I2C2SCL		TRST_N		I/O	PU/PD	N/A	SMT	PU(Note2)	PU(Note2)
22	PL1			UT2RXD	UT2TXDA	I2C2SDA		TDI		I/O	PU/PD	N/A	SMT	PU(Note2)	PU(Note2)
23	PL2			UT2CTS_N	UT2RTS_N	T32A06OUTB		TDO/SWV		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
24	PL3		INT08	UT2RTS_N	UT2CTS_N	T32A06INB0		TCK/SWCLK		I/O	PU/PD	N/A	SMT	PD(Note2)	PD(Note2)
25	PL4		INT12			T32A06INB1		TMS/SWDIO		I/O	PU/PD	N/A	SMT	PU(Note2)	PU(Note2)
-	PL5					T32A06OUTA	T32A06OUTC			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PL6					T32A06INA0	T32A06INC0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PL7					T32A06INA1	T32A06INC1			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PT7		INT29			T32A06INA1	T32A06INC1			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PT6					T32A06INA0	T32A06INC0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PT5					T32A06OUTA	T32A06OUTC			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PT4			TSPI2RXD		T32A06INB1				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PT3		INT26	TSPI2TXD		T32A06INB0				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PT2		INT25	TSPI2SCK		T32A06OUTB				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PT1		INT24	I2C3SCL	TSPI2CS0	TSPI2CSIN				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PT0		INT23	I2C3SDA	TSPI2CS1					I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PP0				TSPI2SCK	T32A01OUTA	T32A01OUTC			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PP1				TSPI2TXD	T32A01INA0	T32A01INC0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PP2				TSPI2RXD	T32A01INA1	T32A01INC1			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
26	DVDD5A									-	-	-	-	-	-
27	REGOUT2									-	-	-	-	-	-
28	REGOUT1									-	-	-	-	-	-
29	DVSSA									-	-	-	-	-	-
30	PH0	X1	EHCLKIN							Input	PD	N/A	SMT	Hi-z	Hi-z
31	PH1	X2								Input	PD	N/A	SMT	Hi-z	Hi-z
32	RESET_N									-	PU	-	SMT	-	-
33	PH2	XT1								Input	PD	N/A	SMT	Hi-z	Hi-z
34	PH3	XT2	INT06							Input	PD	N/A	SMT	Hi-z	Hi-z
35	MODE									-	PD	-	SMT	-	-
-	PH4		INT19	TSPI4SCK						I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PH5		INT20	TSPI4TXD						I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PH6		INT21	TSPI4RXD						I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PH7		INT22							I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PV5			UT4TXDB						I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PV6			UT4TXDA	UT4RXD					I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PV7			UT4RXD	UT4TXDA					I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
36	PC0		INT00	I2C0SCL		T32A02OUTA	T32A02OUTC			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
37	PC1		INT01	I2C0SDA		T32A02INA0	T32A02INC0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PC2		INT02	UT4TXDB		T32A02INA1	T32A02INC1	RTCOUT		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
38	PC3			UT4TXDA	UT4RXD	T32A02OUTB				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
39	PC4			UT4RXD	UT4TXDA	T32A02INB0				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PC5			UT4CTS_N	UT4RTS_N	T32A02INB1				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PC6			UT4RTS_N	UT4CTS_N					I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PR0					T32A02OUTA	T32A02OUTC			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PR1					T32A02INA0	T32A02INC0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PR2					T32A02INA1	T32A02INC1			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PR3									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PR4									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PR5									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PR6									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PR7									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PN5					T32A05INB1				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
40	PN4			UT5TXDB		T32A05INB0				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
41	PN3		INT10	UT5TXDA	UT5RXD	T32A05OUTB		TRGIN2		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
42	PN2			UT5RXD	UT5TXDA	T32A05INA1	T32A05INC1			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
43	PN1			UT5CTS_N	UT5RTS_N	T32A05INA0	T32A05INC0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z

Note1: When the RESET_N pin is "Low", a built-in pull-up resistor becomes effective.
Note2: The Initial value of built-in Pull-up/Pull-down resistor is effective.

Not to be copied without permission

List of All Pins(4)

M3HL (LQFP64)	Pin Name	Combination Function A	Combination Function B	Combination Function 1	Combination Function 2	Combination Function 3	Combination Function 4	Combination Function 5	Combination Function 6	Input/Output	Pull-up/ Pull-down	5V_T	SMT/ CMOS	Under Reset	After Reset
44	PJ0			UT1TXDB		T32A03OUTA	T32A03OUTC	UO0		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
45	PJ1			UT1TXDA	UT1RXD	T32A03INA0	T32A03INC0	XO0		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
46	PJ2			UT1RXD	UT1TXDA	T32A03INA1	T32A03INC1	VO0		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
47	PJ3			UT1CTS_N	UT1RTS_N	T32A03OUTB		YO0		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
48	PJ4		INT04	UT1RTS_N	UT1CTS_N	T32A03INB0		WO0		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
49	PJ5					T32A03INB1		ZO0		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
50	PK0			UT1TXDB				EMG0		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
51	PK1		INT05	UT1TXDA	UT1RXD			OVV0		I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
52	PK2			UT1RXD	UT1TXDA	T32A04OUTA	T32A04OUTC			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
53	PK3			UT1CTS_N	UT1RTS_N	T32A04INA0	T32A04INC0			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
54	PK4			UT1RTS_N	UT1CTS_N	T32A04INA1	T32A04INC1			I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
55	PK5					T32A04OUTB				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
56	PK6					T32A04INB0				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PK7		INT13			T32A04INB1				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
57	PP3		INT14							I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
	PP4									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
	PP5									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PP6					PMD0DBG				I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PP7									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
58	PV0									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
59	PV1									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PV2		INT17							I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PV3		INT18							I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PV4									I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	DVDD5B									-	-	-	-	-	-
-	DVSSB									-	-	-	-	-	-
-	PD5	AINA20								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PD4	AINA19								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PF7	AINA18								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PF6	AINA17								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PF5	AINA16								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PF4	AINA15								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PF3	AINA14								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PF2	AINA13								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PF1	AINA12								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
-	PF0	AINA11								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
60	PE6	AINA10								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
61	PE5	AINA09								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
62	PE4	AINA08								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
63	PE3	AINA07								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z
64	PE2	AINA06								I/O	PU/PD	N/A	SMT	Hi-z	Hi-z

Not Recommended for New Design

Part Naming Conventions

TMP M3H Q F D x FG

The identification of Toshiba microcontrollers

Core

Symbol	Core
M4	Arm Cortex-M4 processor with FPU
M3	Arm Cortex-M3
M0	Arm Cortex-M0

Product Group

Family	Group	Application
TXZ	H	For General-purpose/Consumer electronic equipment
	K	For Motor/Inverter control industrial equipment(MCU+AMP/COMP)
	G	For OA/Digital equipment/industrial equipment
	E	For Precision instruments control
	P	For Healthcare/ Battery equipment
	J	For FA / Robotics

Pin Count

Symbol		Pin Count	Symbol		Pin Count
0	G	Under 32pin	8	Q	129pin to 144pin
1	H	33pin to 44pin	9	R	145pin to 176pin
2	J	45pin to 48pin	A	S	177pin to 200pin
3	K	49pin to 52pin	B	T	201pin to 224pin
4	L	53pin to 64pin	C	U	225pin to 250pin
5	M	65pin to 80pin	D	V	251pin to 300pin
6	N	81pin to 100pin			
7	P	101pin to 128pin			

Revision

Package

Symbol	Package
QG	Plastic shrink quad outline non-leaded package; dry-packed
UG.DUG, FG,DFG	Plastic quad flat package; dry-packed
MG,DMG	Plastic small-outline package; dry-packed
XBG	Plastic ball grid array; dry-packed

ROM Size

Symbol	Size[KB]
M	32
P	48
S	64
U	96
W	128
Y	256
Z	384
D	512
E	768
10	1,024
15	1,536
20	2,048
40	4,096
80	8,192

ROM Type

Symbol	Type
F	Flash
C	Mask

Not Recommended for New Design

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as “TOSHIBA”.
Hardware, software and systems described in this document are collectively referred to as “Product”.

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, lifesaving and/or life supporting medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, and devices related to power plant. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative or contact us via our website.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**

Not Recommended for New Design