TP2104

P-Channel Enhancement-Mode Vertical DMOS FET

Features

- High Input Impedance and High Gain
- Low-Power Drive Requirement
- Ease of Paralleling
- Low C_{ISS} and Fast Switching Speeds
- Excellent Thermal Stability
- Integral Source-Drain Diode
- Free from Secondary Breakdown

Applications

- Logic-Level Interfaces (Ideal for TTL and CMOS)
- Solid-State Relays
- Analog Switches
- Power Management
- Telecommunication Switches

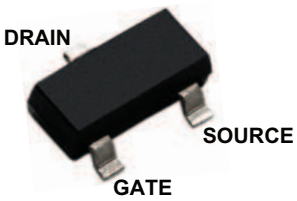
General Description

The TP2104 low-threshold, Enhancement-mode (normally-off) transistor uses a vertical DMOS structure and a well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

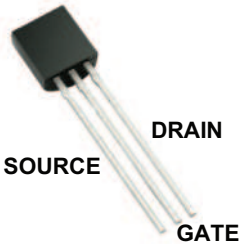
Microchip's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance and fast switching speeds are desired.

Package Types

3-lead SOT-23
(Top view)



3-lead TO-92
(Top view)



See Table 3-1 and Table 3-2 for pin information.

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Drain-to-Source Voltage ..... BV_{DSS}
Drain-to-Gate Voltage ..... BV_{DGS}
Gate-to-Source Voltage ..... ±20V
Operating Ambient Temperature, T_A ..... –55°C to +150°C
Storage Temperature, T_S ..... –55°C to +150°C

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_A = 25°C unless otherwise specified. All DC parameters are 100% tested at 25°C unless otherwise stated. Pulse test: 300 µs pulse, 2% duty cycle

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	BV_{DSS}	–40	—	—	V	V_{GS} = 0V, I_D = –1 mA
Gate Threshold Voltage	$V_{GS(th)}$	–1	—	–2	V	V_{GS} = V_{DS}, I_D = –1 mA
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	5.8	6.5	mV/°C	V_{GS} = V_{DS}, I_D = –1 mA (**Note 1**)
Gate Body Leakage Current	I_{GSS}	—	–1	–100	nA	V_{GS} = ± 20V, V_{DS} = 0V
Zero-Gate Voltage Drain Current	I_{DSS}	—	—	–10	µA	V_{GS} = 0V, V_{DS} = Maximum rating
		—	—	–1	mA	V_{DS} = 0.8 Maximum rating, V_{GS} = 0V, T_A = 125°C (**Note 1**)
On-State Drain Current	$I_{D(ON)}$	–0.6	—	—	A	V_{GS} = –10V, V_{DS} = –25V
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	—	10	Ω	V_{GS} = –4.5V, I_D = –50 mA
		—	—	6	Ω	V_{GS} = –10V, I_D = –500 mA
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	0.55	1	%/°C	V_{GS} = –10V, I_D = –500 mA (**Note 1**)

Note 1: Specification is obtained by characterization and is not 100% tested.

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AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_A = 25°C unless otherwise specified. Specification is obtained by characterization and is not 100% tested.						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Forward Transconductance	G_{FS}	150	200	—	mmho	V_{DS} = –25V, I_D = –500 mA
Input Capacitance	C_{ISS}	—	35	60	pF	V_{GS} = 0V, V_{DS} = –25V, f = 1 MHz
Common Source Output Capacitance	C_{OSS}	—	22	30	pF	
Reverse Transfer Capacitance	C_{RSS}	—	8	10	pF	
Turn-On Delay Time	$t_{d(ON)}$	—	4	6	ns	V_{DD} = –25V, I_D = –500 mA, R_{GEN} = 25Ω
Rise Time	t_r	—	4	8	ns	
Turn-Off Delay Time	$t_{d(OFF)}$	—	5	9	ns	
Fall Time	t_f	—	5	8	ns	
DIODE PARAMETER						
Diode Forward Voltage Drop	V_{SD}	—	–1.2	–2	V	V_{GS} = 0V, I_{SD} = –500 mA (**Note 1**)
Reverse Recovery Time	t_{rr}	—	400	—	ns	V_{GS} = 0V, I_{SD} = –500 mA

Note 1: Unless otherwise stated, all DC parameters are 100% tested at 25°C. Pulse test: 300 µs pulse, 2% duty cycle

TEMPERATURE SPECIFICATIONS

Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	–55	—	+150	°C	
Storage Temperature	T_S	–55	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
3-lead SOT-23	θ_{JA}	—	203	—	°C/W	
3-lead TO-92	θ_{JA}	—	132	—	°C/W	

THERMAL CHARACTERISTICS

Package	**I_D (Note 1) (Continuous) (mA)**	**I_D (Pulsed) (mA)**	**Power Dissipation at T_A = 25°C (W)**	**I_{DR} (Note 1) (mA)**	**I_{DRM} (mA)**
3-lead SOT-23	–160	–800	0.36	–160	–800
3-lead TO-92	–175	–1000	0.74	–175	–1000

Note 1: I_D (continuous) is limited by maximum rated T_J.

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

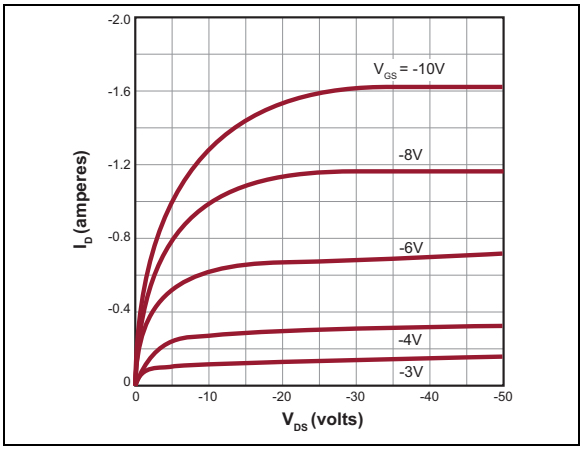


FIGURE 2-1: *Output Characteristics.*

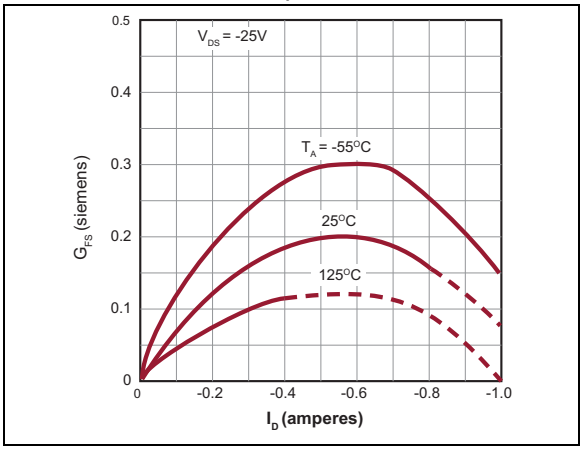


FIGURE 2-2: *Transconductance vs. Drain Current.*

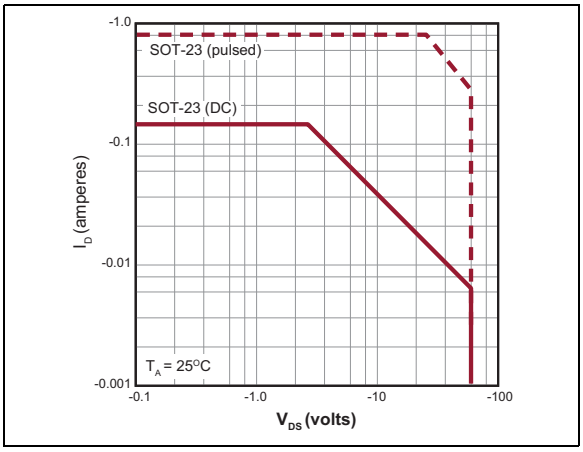


FIGURE 2-3: *Maximum Rated Safe Operating Area.*

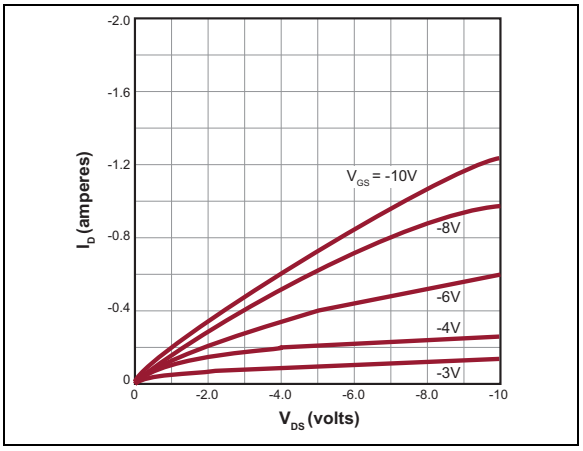


FIGURE 2-4: *Saturation Characteristics.*

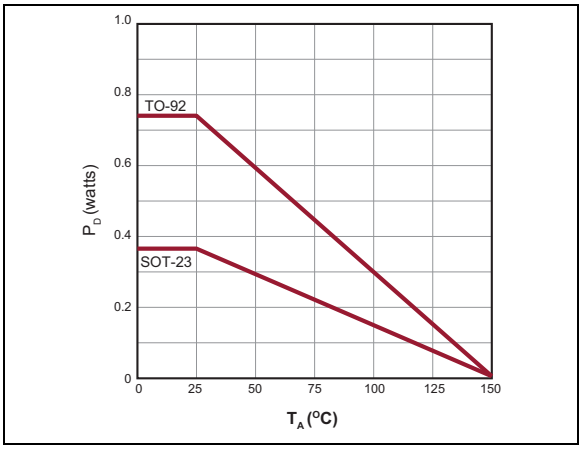


FIGURE 2-5: *Power Dissipation vs. Case Temperature.*

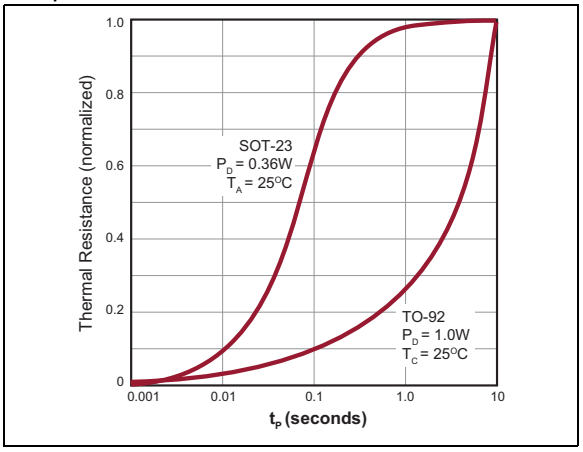


FIGURE 2-6: *Thermal Response Characteristics.*

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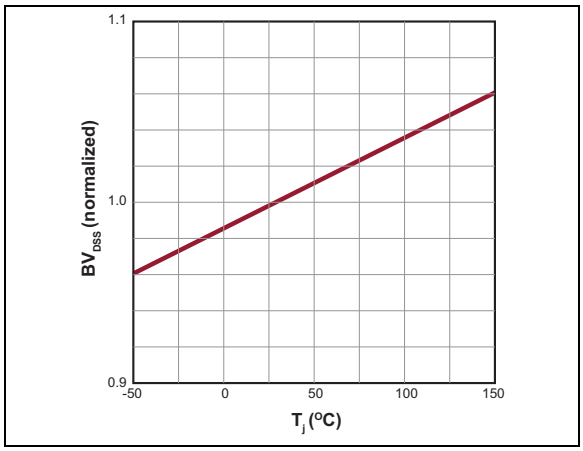


FIGURE 2-7: *BV_{DSS} Variation with Temperature.*

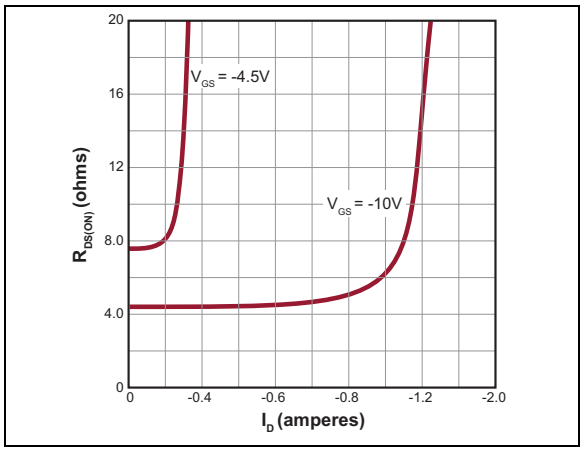


FIGURE 2-10: *On-Resistance vs. Drain Current.*

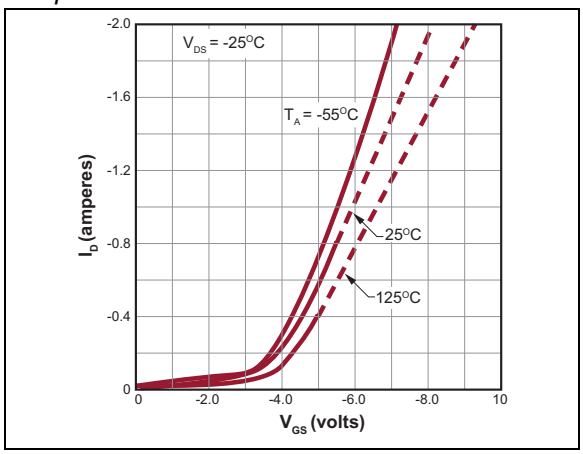


FIGURE 2-8: *Transfer Characteristics.*

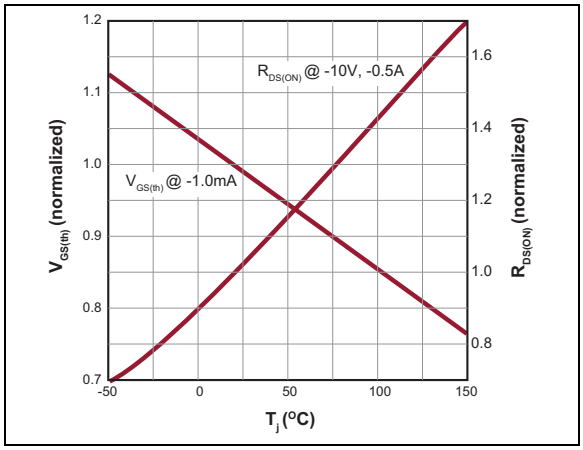


FIGURE 2-11: *$V_{(th)}$ and R_{DS} Variation with Temperature.*

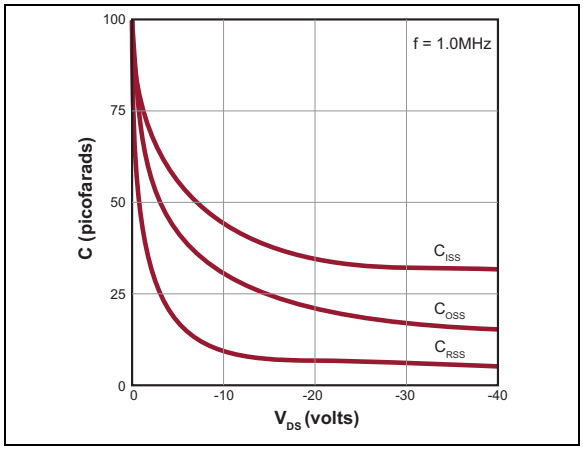


FIGURE 2-9: *Capacitance vs. Drain-to-Source Voltage.*

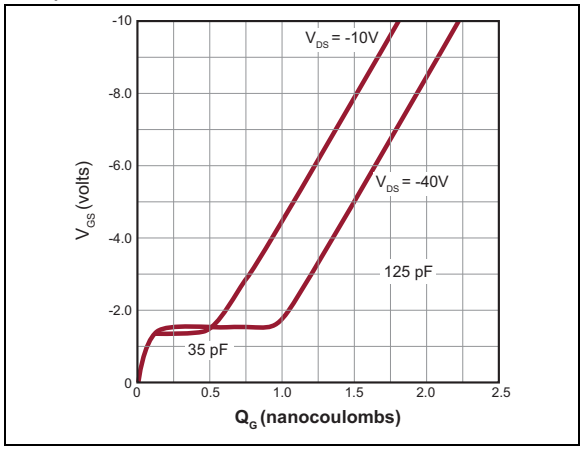


FIGURE 2-12: *Gate Drive Dynamic Characteristics.*

3.0 PIN DESCRIPTION

The details on the pins of 3-lead-SOT-23 and 3-lead TO-92 are listed in Table 3-1 and Table 3-2, respectively. Refer to **Package Types** for the location of pins.

TABLE 3-1: 3-LEAD SOT-23 PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Gate	Gate
2	Source	Source
3	Drain	Drain

TABLE 3-2: 3-LEAD TO-92 PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Source	Source
2	Gate	Gate
3	Drain	Drain

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4.0 FUNCTIONAL DESCRIPTION

Figure 4-1 illustrates the switching waveforms and test circuit for TP2104.

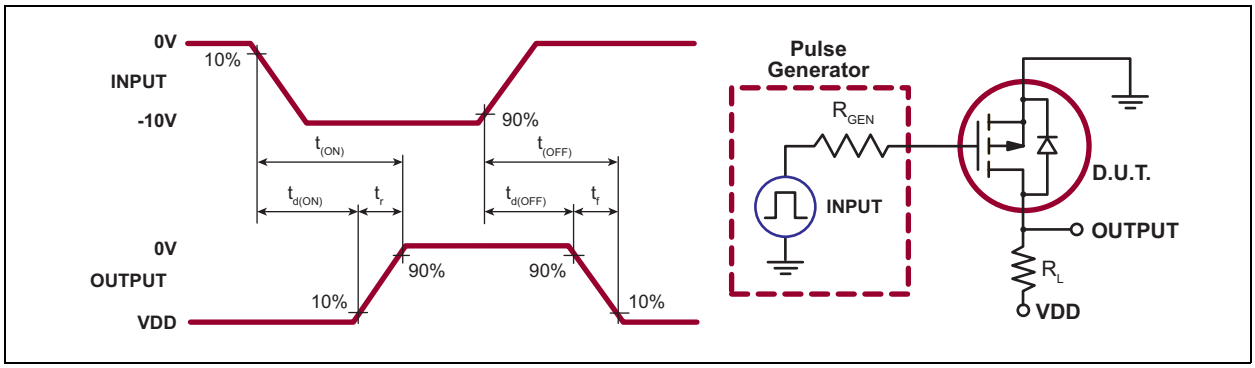


FIGURE 4-1: *Switching Waveforms and Test Circuit.*

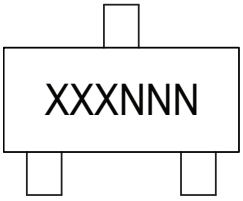
TABLE 4-1: PRODUCT SUMMARY

BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (Maximum) (Ω)	$V_{GS(TH)}$ (Maximum) (V)
–40V	6	–2

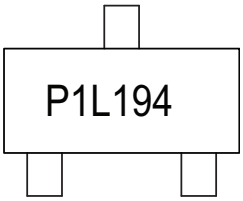
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

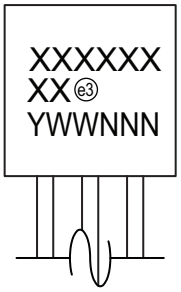
3-lead SOT-23



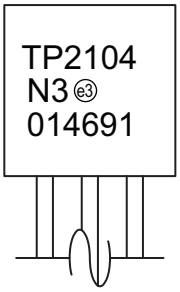
Example



3-lead TO-92



Example



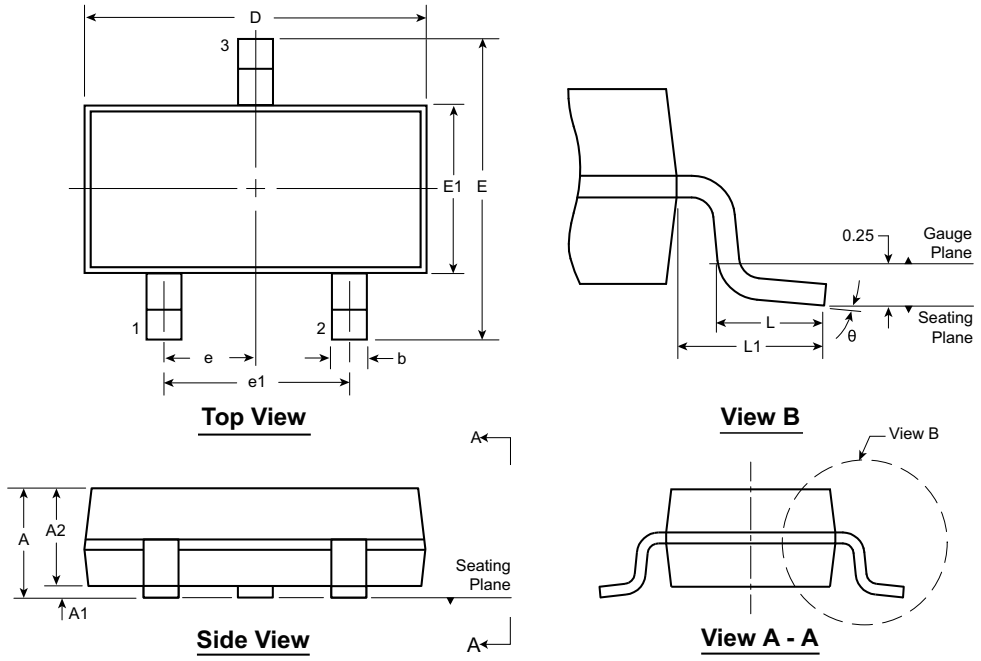
Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

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3-Lead TO-236AB (SOT-23) Package Outline (K1/T)

2.90x1.30mm body, 1.12mm height (max), 1.90mm pitch

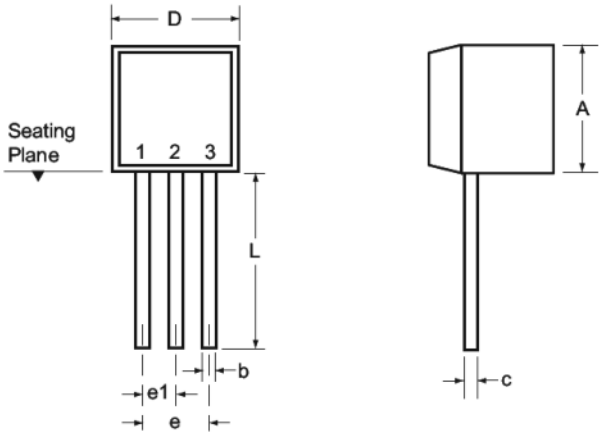


Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

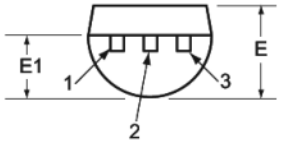
Symbol		A	A1	A2	b	D	E	E1	e	e1	L	L1	θ
Dimension (mm)	MIN	0.89	0.01	0.88	0.30	2.80	2.10	1.20	0.95 BSC	1.90 BSC	0.20†	0.54 REF	0°
	NOM	-	-	0.95	-	2.90	-	1.30			0.50		-
	MAX	1.12	0.10	1.02	0.50	3.04	2.64	1.40			0.60		8°

JEDEC Registration TO-236, Variation AB, Issue H, Jan. 1999.
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

3-Lead TO-92 Package Outline (L/LL/N3)



Front View **Side View**



Bottom View

Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014†	.014†	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022†	.022†	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

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APPENDIX A: REVISION HISTORY

Revision A (April 2020)

- Converted Supertex Doc# DSFP-TP2104 to Microchip DS20005958A
- Added pin function tables
- Changed the package marking format
- Removed the TO-92 P002, P005, P013 and P014 media types
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	TP2104	=	P-Channel Enhancement-Mode Vertical DMOS FET
Packages:	N3	=	3-lead TO-92
	K1	=	3-lead SOT-23
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Types:	(blank)	=	1000/Bag for an N3 Package
	(blank)	=	3000/Reel for a K1 Package
	P003	=	2000/Reel for an N3 Package

Examples:

a) TP2104N3-G:	P-Channel Enhancement-Mode, Vertical DMOS FET, 3-lead TO-92, 1000/Bag
b) TP2104N3-G-P003:	P-Channel Enhancement-Mode, Vertical DMOS FET, 3-lead TO-92, 2000/Reel
c) TP2104K1-G:	P-Channel Enhancement-Mode, Vertical DMOS FET, 3-lead SOT-23, 3000/Reel

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