# Extended Temperature Serial Interface CODEC/Filter COMBO Family

**Check for Samples: TP3054-X, TP3057-X**

## FEATURES

- **−40°C to +85°C Operation**
- **Complete CODEC and Filtering System (COMBO) Including:**
  - **Transmit High-Pass and Low-Pass Filtering**
  - **Receive Low-Pass Filter with Sin x/x Correction**
  - **Active RC Noise Filters**
  - **µ-Law or A-Law Compatible COder and DECoder**
  - **Internal Precision Voltage Reference**
  - **Serial I/O Interface**
  - **Internal Auto-Zero Circuitry**
- **µ-Law, 16-Pin - TP3054**
- **A-Law, 16-Pin - TP3057**
- **Designed for D3/D4 and CCITT Spplications**
- **±5V Operation**
- **Low Operating Power - Typically 50 mW**
- **Power-Down Standby Mode - Typically 3 mW**
- **Automatic Power-Down**
- **TTL or CMOS Compatible Digital Interfaces**
- **Maximizes Line Interface Card Circuit Density**
- **Dual-In-Line or PCC Surface Mount Packages**
- **See also AN-370, “Techniques for Designing with CODEC/Filter COMBO Circuits” (SNLA136)**

## DESCRIPTION

The TP3054, TP3057 family consists of µ-law and A-law monolithic PCM CODEC/filters utilizing the A/D and D/A conversion architecture shown in Figure 3, and a serial PCM interface. The devices are fabricated using TI's advanced double-poly CMOS process (microCMOS).

The encode portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded µ-law or A-law PCM format. The decode portion of each device consists of an expanding decoder, which reconstructs the analog signal from the companded µ-law or A-law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz followed by a single-ended power amplifier capable of driving low impedance loads. The devices require two 1.536 MHz, 1.544 MHz or 2.048 MHz transmit and receive master clocks, which may be asynchronous; transmit and receive bit clocks, which may vary from 64 kHz to 2.048 MHz; and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.

## Connection Diagram

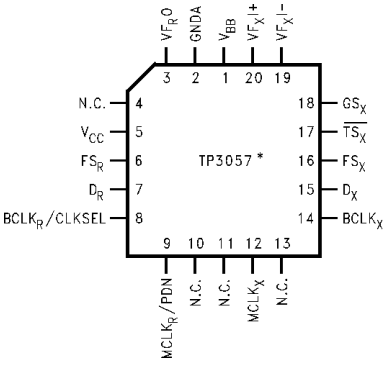



**Figure 1. Plastic Chip Carriers (Top View)**
**Package Number FN0020A**

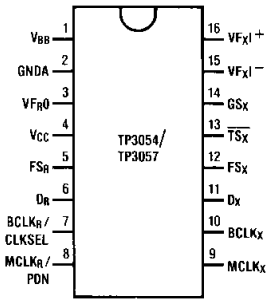



**Figure 2. Dual-In-Line Package (Top View)**
**Package Number NFG001E & DW0016B**

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## Block Diagram

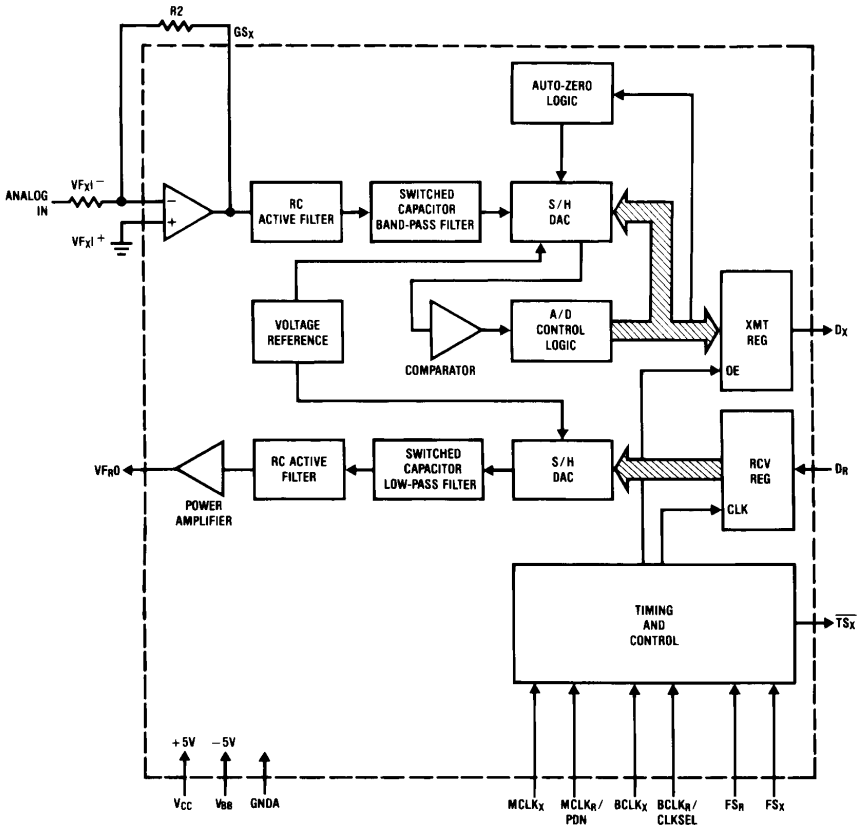



**Figure 3.**

### PIN DESCRIPTIONS

| Symbol | Function |
|---|---|
| $V_{BB}$ | Negative power supply pin. |
| | $V_{BB}$ = −5V ±5%. |
| GNDA | Analog ground. All signals are referenced to this pin. |
| $VF_RO$ | Analog output of the receive power amplifier. |
| $V_{CC}$ | Positive power supply pin. |
| | $V_{CC}$ = +5V ±5%. |
| $FS_R$ | Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into $D_R$. $FS_R$ is an 8 kHz pulse train. See Figure 4 and Figure 5 for timing details. |
| $D_R$ | Receive data input. PCM data is shifted into $D_R$ following the $FS_R$ leading edge. |
| $BCLK_R$/CLKSEL | The bit clock which shifts data into $D_R$ after the $FS_R$ leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see Table 1). |
| $MCLK_R$/PDN | Receive master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down. |
| $MCLK_X$ | Transmit master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$. Best performance is realized from synchronous operation. |
| $FS_X$ | Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on $D_X$. $FS_X$ is an 8 kHz pulse train, see Figure 4 and Figure 5 for timing details. |
| $BCLK_X$ | The bit clock which shifts out the PCM data on $D_X$. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$. |


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**PIN DESCRIPTIONS (continued)**

| Symbol | Function |
|---|---|
| $D_X$ | The TRI-STATE PCM data output which is enabled by $FS_X$. |
| $\overline{TS_X}$ | Open drain output which pulses low during the encoder time slot. |
| $GS_X$ | Analog output of the transmit input amplifier. Used to externally set gain. |
| $VF_XI^-$ | Inverting input of the transmit input amplifier. |
| $VF_XI^+$ | Non-inverting input of the transmit input amplifier. |

## Functional Description

### POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into a power-down state. All non-essential circuits are deactivated and the $D_X$ and $VF_RO$ outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin *and* $FS_X$ and/or $FS_R$ pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high; the alternative is to hold both $FS_X$ and $FS_R$ inputs continuously low—the device will power-down approximately 1 ms after the last $FS_X$ or $FS_R$ pulse. Power-up will occur on the first $FS_X$ or $FS_R$ pulse. The TRI-STATE PCM data output, $D_X$, will remain in the high impedance state until the second $FS_X$ pulse.

### SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

With a fixed level on the $BCLK_R$/CLKSEL pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R$/CLKSEL. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

Each $FS_X$ pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled $D_X$ output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE $D_X$ output is returned to a high impedance state. With an $FS_R$ pulse, PCM data is latched via the $D_R$ input on the negative edge of $BCLK_X$ (or $BCLK_R$ if running). $FS_X$ and $FS_R$ must be synchronous with $MCLK_{X/R}$.

**Table 1. Selection of Master Clock Frequencies**

| $BCLK_R$/CLKSEL | Master Clock Frequency Selected | |
|---|---|---|
| | TP3057 | TP3054 |
| Clocked | 2.048 MHz | 1.536 MHz or 1.544 MHz |
| 0 | 1.536 MHz or 1.544 MHz | 2.048 MHz |
| 1 | 2.048 MHz | 1.536 MHz or 1.544 MHz |

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## ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 2.048 MHz for the TP3057, or 1.536 MHz, 1.544 MHz for the TP3054, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see Pin Description above). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. $FS_X$ starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. $FS_R$ starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in Table 1 are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64 kHz to 2.048 MHz.

## SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, $FS_X$ and $FS_R$, must be one bit clock period long, with timing relationships specified in Figure 4. With $FS_X$ high during a falling edge of $BCLK_X$, the next rising edge of $BCLK_X$ enables the $D_X$ TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the $D_X$ output. With $FS_R$ high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. All four devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

## LONG FRAME SYNC OPERATION

To use the long frame mode, both the frame sync pulses, $FS_X$ and $FS_R$, must be three or more bit clock periods long, with timing relationships specified in Figure 5. Based on the transmit frame sync, $FS_X$, the COMBO will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The $D_X$ TRI-STATE output buffer is enabled with the rising edge of $FS_X$ or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The $D_X$ output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by $FS_X$ going low, whichever comes later. A rising edge on the receive frame sync pulse, $FS_R$, will cause the PCM data at $D_R$ to be latched in on the next eight falling edges of $BCLK_R$ ($BCLK_X$ in synchronous mode). All four devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

In applications where the LSB bit is used for signalling, with $FS_R$ two bit clock periods long, the decoder will interpret the lost LSB as "½" to minimize noise and distortion.

## TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see Figure 8. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to μ-law (TP3054) or A-law (TP3057) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload ($t_{MAX}$) of nominally 2.5V peak (see Transmission Characteristics). The $FS_X$ frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through $D_X$ at the next $FS_X$ pulse. The total encoding delay will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which totals 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.


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## RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (TP3057) or μ-law (TP3054) and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter/power amplifier capable of driving a 600Ω load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurrence of $FS_R$, the data at the $D_R$ input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μs later the decoder DAC output is updated. The total decoder delay is ~10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (½ frame), which gives approximately 180 μs.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings(1)(2)

| | | |
|---|---|---|
| $V_{CC}$ to GNDA | | 7V |
| $V_{BB}$ to GNDA | | −7V |
| Voltage at any Analog Input or Output | | $V_{CC}$+0.3V to $V_{BB}$−0.3V |
| Voltage at any Digital Input or Output | | $V_{CC}$+0.3V to GNDA−0.3V |
| Operating Temperature Range | | −55°C to + 125°C |
| Storage Temperature Range | | −65°C to +150°C |
| Lead Temperature | (Soldering, 10 sec.) | 300°C |

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

### Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are ensured for $V_{CC}$ = +5.0V ±5%, $V_{BB}$ = −5.0V ±5%; $T_A$ = −40°C to +85°C by correlation with 100% electrical testing at $T_A$ = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GNDA. Typicals specified at $V_{CC}$ = +5.0V, $V_{BB}$ = −5.0V, $T_A$ = 25°C.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **DIGITAL INTERFACE** | | | | | | |
| $V_{IL}$ | Input Low Voltage | | | | **0.6** | V |
| $V_{IH}$ | Input High Voltage | | **2.2** | | | V |
| $V_{OL}$ | Output Low Voltage | $D_X$, $I_L$=3.2 mA | | | **0.4** | V |
| | | $SIG_R$, $I_L$=1.0 mA | | | **0.4** | V |
| | | $\overline{TS_X}$, $I_L$=3.2 mA, Open Drain | | | **0.4** | V |
| $V_{OH}$ | Output High Voltage | $D_X$, $I_H$=−3.2 mA | **2.4** | | | V |
| | | $SIG_R$, $I_H$=−1.0 mA | **2.4** | | | V |
| $I_{IL}$ | Input Low Current | GNDA≤$V_{IN}$≤$V_{IL}$, All Digital Inputs | **−10** | | **10** | μA |
| $I_{IH}$ | Input High Current | $V_{IH}$≤$V_{IN}$≤$V_{CC}$ | **−10** | | **10** | μA |
| $I_{OZ}$ | Output Current in High Impedance State (TRI-STATE) | $D_X$, GNDA≤$V_O$≤$V_{CC}$ | **−10** | | **10** | μA |
| **ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (ALL DEVICES)** | | | | | | |
| $I_I$XA | Input Leakage Current | −2.5V≤V≤+2.5V, $VF_XI^+$ or $VF_XI^-$ | **−200** | | **200** | nA |
| $R_I$XA | Input Resistance | −2.5V≤V≤+2.5V, $VF_XI^+$ or $VF_XI^-$ | 10 | | | MΩ |
| $R_O$XA | Output Resistance | Closed Loop, Unity Gain | | 1 | 3 | Ω |
| $R_L$XA | Load Resistance | $GS_X$ | 10 | | | kΩ |
| $C_L$XA | Load Capacitance | $GS_X$ | | | 50 | pF |
| $V_O$XA | Output Dynamic Range | $GS_X$, $R_L$ ≥ 10 kΩ | **−2.8** | | **2.8** | V |
| $A_V$XA | Voltage Gain | $VF_XI^+$ to $GS_X$ | **5000** | | | V/V |

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## Electrical Characteristics (continued)

Unless otherwise noted, limits printed in **BOLD** characters are ensured for $V_{CC}$ = +5.0V ±5%, $V_{BB}$ = −5.0V ±5%; $T_A$ = −40°C to +85°C by correlation with 100% electrical testing at $T_A$ = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GNDA. Typicals specified at $V_{CC}$ = +5.0V, $V_{BB}$ = −5.0V, $T_A$ = 25°C.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_UXA$ | Unity Gain Bandwidth | | 1 | 2 | | MHz |
| $V_{OS}XA$ | Offset Voltage | | **−20** | | **20** | mV |
| $V_{CM}XA$ | Common-Mode Voltage | CMRRXA > 60 dB | −2.5 | | 2.5 | V |
| CMRRXA | Common-Mode Rejection Ratio | DC Test | **60** | | | dB |
| PSRRXA | Power Supply Rejection Ratio | DC Test | 60 | | | dB |
| **ANALOG INTERFACE WITH RECEIVE FILTER (ALL DEVICES)** | | | | | | |
| $R_ORF$ | Output Resistance | Pin $VF_RO$ | | 1 | 3 | Ω |
| $R_LRF$ | Load Resistance | $VF_RO$=±2.5V | 600 | | | Ω |
| $C_LRF$ | Load Capacitance | | | | 500 | pF |
| $VOS_RO$ | Output DC Offset Voltage | | **−200** | | **200** | mV |
| **POWER DISSIPATION (ALL DEVICES)** | | | | | | |
| $I_{CC}0$ | Power-Down Current | No Load(1) | | 0.65 | **2.0** | mA |
| $I_{BB}0$ | Power-Down Current | No Load(1) | | 0.01 | **0.33** | mA |
| $I_{CC}1$ | Power-Up (Active) Current | No Load | | 5.0 | **11.0** | mA |
| $I_{BB}1$ | Power-Up (Active) Current | No Load | | 5.0 | **11.0** | mA |

(1) $I_{CC0}$ and $I_{BB0}$ are measured after first achieving a power-up state.


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## Timing Specifications

Unless otherwise noted, limits printed in **BOLD** characters are ensured for $V_{CC}$ = +5.0V ±5%, $V_{BB}$ = −5.0V ±5%; $T_A$ = −40°C to +85°C by correlation with 100% electrical testing at $T_A$ = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GNDA. Typicals specified at $V_{CC}$ = +5.0V, $V_{BB}$ = –5.0V, $T_A$ = 25°C. All timing parameters are assured at $V_{OH}$ = 2.0V and $V_{OL}$ = 0.7V. See Definitions and Timing Conventions section for test methods information.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $1/t_{PM}$ | Frequency of Master Clocks | Depends on the Device Used and the | | 1.536 | | MHz |
| | | $BCLK_R$/CLKSEL Pin. | | 1.544 | | MHz |
| | | $MCLK_X$ and $MCLK_R$ | | **2.048** | | MHz |
| $t_{RM}$ | Rise Time of Master Clock | $MCLK_X$ and $MCLK_R$ | | | 50 | ns |
| $t_{FM}$ | Fall Time of Master Clock | $MCLK_X$ and $MCLK_R$ | | | 50 | ns |
| $t_{PB}$ | Period of Bit Clock | | 485 | **488** | 15725 | ns |
| $t_{RB}$ | Rise Time of Bit Clock | $BCLK_X$ and $BCLK_R$ | | | 50 | ns |
| $t_{FB}$ | Fall Time of Bit Clock | $BCLK_X$ and $BCLK_R$ | | | 50 | ns |
| $t_{WMH}$ | Width of Master Clock High | $MCLK_X$ and $MCLK_R$ | **160** | | | ns |
| $t_{WML}$ | Width of Master Clock Low | $MCLK_X$ and $MCLK_R$ | **160** | | | ns |
| $t_{SBFM}$ | Set-Up Time from $BCLK_X$ High to $MCLK_X$ Falling Edge | First Bit Clock after the Leading Edge of $FS_X$ Short Frame | **100** | | | ns |
| | | Long Frame | **125** | | | |
| $t_{SFFM}$ | Setup Time from $FS_X$ High to $MCLK_X$ Falling Edge | Long Frame Only | **100** | | | ns |
| $t_{WBH}$ | Width of Bit Clock High | $V_{IH}$=2.2V | **160** | | | ns |
| $t_{WBL}$ | Width of Bit Clock Low | $V_{IL}$=0.6V | **160** | | | ns |
| $t_{HBFL}$ | Holding Time from Bit Clock Low to Frame Sync | Long Frame Only | **0** | | | ns |
| $t_{HBFS}$ | Holding Time from Bit Clock High to Frame Sync | Short Frame Only | **0** | | | ns |
| $t_{SFB}$ | Set-Up Time from Frame Sync to Bit Clock Low | Long Frame Only | **115** | | | ns |
| $t_{DBD}$ | Delay Time from $BCLK_X$ High to Data Valid | Load=150 pF plus 2 LSTTL Loads | 0 | | 140 | ns |
| $t_{DBTS}$ | Delay Time to $\overline{TS_X}$ Low | Load=150 pF plus 2 LSTTL Loads | | | 140 | ns |
| $t_{DZC}$ | Delay Time from $BCLK_X$ Low to Data Output Disabled | $C_L$=0 pF to 150 pF | 50 | | 165 | ns |
| $t_{DZF}$ | Delay Time to Valid Data from $FS_X$ or $BCLK_X$, Whichever Comes Later | $C_L$=0 pF to 150 pF | 20 | | 165 | ns |
| $t_{SDB}$ | Set-Up Time from $D_R$ Valid to $BCLK_{R/X}$ Low | | **50** | | | ns |
| $t_{HBD}$ | Hold Time from $BCLK_{R/X}$ Low to $D_R$ Invalid | | **50** | | | ns |
| $t_{SF}$ | Set-Up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low | Short Frame Sync Pulse (1 Bit Clock Period Long) | **50** | | | ns |
| $t_{HF}$ | Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low | Short Frame Sync Pulse (1 Bit Clock Period Long) | **100** | | | ns |
| $t_{HBFI}$ | Hold Time from 3rd Period of Bit Clock Low to Frame Sync ($FS_X$ or $FS_R$) | Long Frame Sync Pulse (from 3 to 8 Bit Clock Periods Long) | **100** | | | ns |
| $t_{WFL}$ | Minimum Width of the Frame Sync Pulse (Low Level) | 64k Bit/s Operating Mode | **160** | | | ns |

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## Timing Diagrams

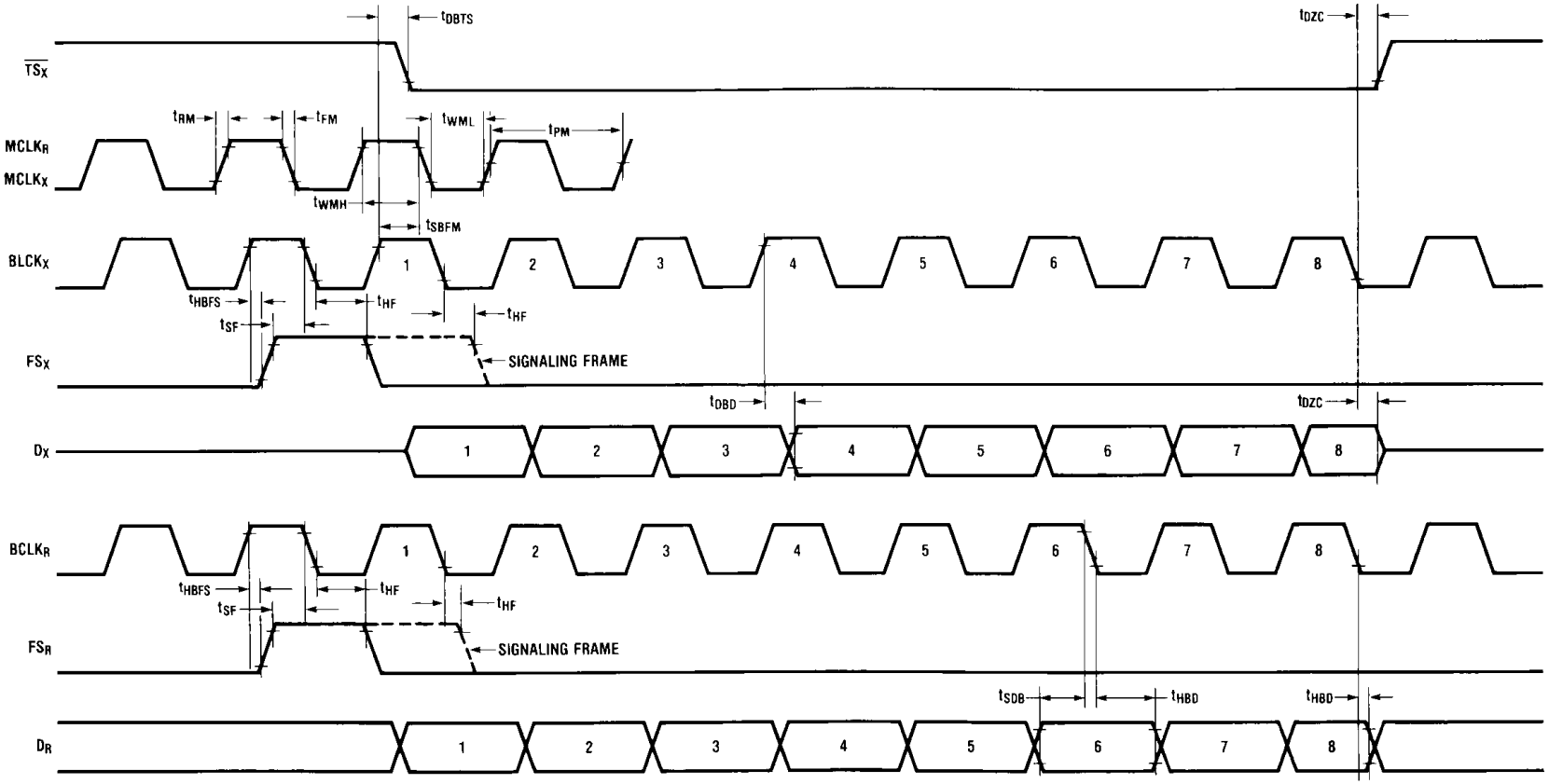



**Figure 4. Short Frame Sync Timing**


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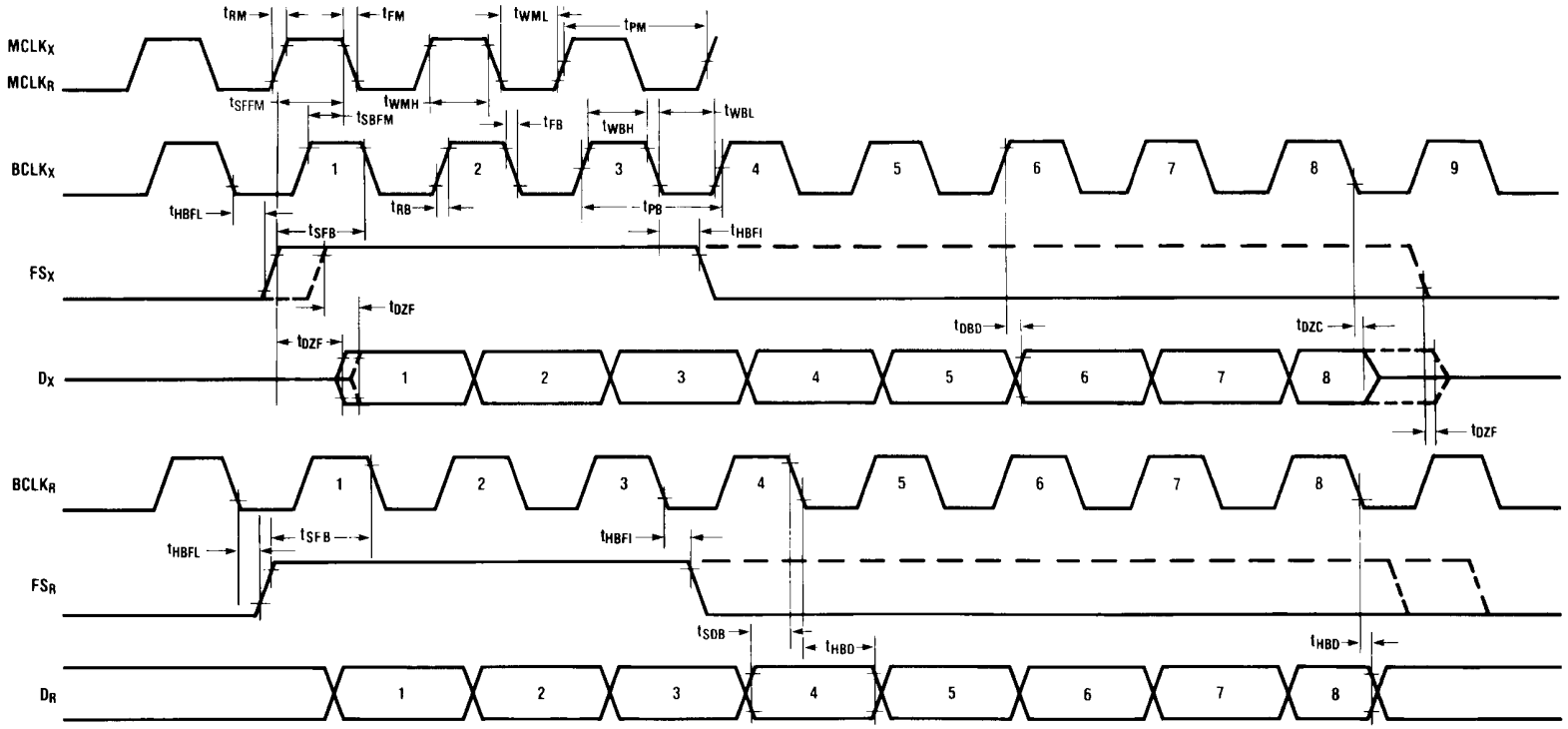



**Figure 5. Long Frame Sync Timing**

## Transmission Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are ensured for $V_{CC}$ = +5.0V ±5%, $V_{BB}$ = −5.0V ±5%; $T_A$ = −40°C to +85°C by correlation with 100% electrical testing at $T_A$ = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, $V_{IN}$ = 0 dBm0, transmit input amplifier connected for unity gain non inverting. Typicals are specified at $V_{CC}$ = +5.0V, $V_{BB}$ = −5.0V, $T_A$ = 25°C.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **AMPLITUDE RESPONSE** | | | | | | |
| | Absolute Levels (Definition of nominal gain) | Nominal 0 dBm0 Level is 4 dBm (600Ω) 0 dBm0 | | 1.2276 | | Vrms |
| $t_{MAX}$ | | Max Overload Level | | | | |
| | | TP3054 (3.17 dBm0) | | 2.501 | | $V_{PK}$ |
| | | TP3057 (3.14 dBm0) | | 2.492 | | $V_{PK}$ |
| $G_{XA}$ | Transmit Gain, Absolute | $T_A$=25°C, $V_{CC}$=5V, $V_{BB}$=−5V Input at $GS_X$=0 dBm0 at 1020 Hz | **−0.15** | | **0.15** | dB |
| $G_{XR}$ | Transmit Gain, Relative to $G_{XA}$ | f=16 Hz | | | −40 | dB |
| | | f=50 Hz | | | −30 | dB |
| | | f=60 Hz | | | **−26** | dB |
| | | f=200 Hz | **−1.8** | | **−0.1** | dB |
| | | f=300 Hz–3000 Hz | **−0.15** | | **0.15** | dB |
| | | f=3152 Hz | **−0.15** | | **0.20** | dB |
| | | f=3300 Hz | **−0.35** | | **0.1** | dB |
| | | f=3400 Hz | **−0.7** | | **0** | dB |
| | | f=4000 Hz | | | **−14** | dB |
| | | f=4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz | | | **−32** | dB |
| $G_{XAT}$ | Absolute Transmit Gain Variation with Temperature | Relative to $G_{XA}$ | −0.15 | | 0.15 | dB |
| $G_{XAV}$ | Absolute Transmit Gain Variation with Supply Voltage | Relative to $G_{XA}$ | **−0.05** | | **0.05** | dB |
| $G_{XRL}$ | Transmit Gain Variations with Level | Sinusoidal Test Method Reference Level=−10 dBm0 | | | | |
| | | $VF_XI^+$=−40 dBm0 to +3 dBm0 | **−0.2** | | **0.2** | dB |
| | | $VF_XI^+$=−50 dBm0 to −40 dBm0 | **−0.4** | | **0.4** | dB |
| | | $VF_XI^+$=−55 dBm0 to −50 dBm0 | **−1.2** | | **1.2** | dB |
| $G_{RA}$ | Receive Gain, Absolute | $T_A$=25°C, $V_{CC}$=5V, $V_{BB}$=−5V Input=Digital Code Sequence for 0 dBm0 Signal at 1020 Hz | **−0.20** | | **0.20** | dB |
| $G_{RR}$ | Receive Gain, Relative to $G_{RA}$ | f=0 Hz to 3000 Hz | **−0.15** | | **0.15** | dB |
| | | f=3300 Hz | **−0.35** | | **0.1** | dB |
| | | f=3400 Hz | **−0.7** | | **0** | dB |
| | | f=4000 Hz | | | **−14** | dB |
| $G_{RAT}$ | Absolute Receive Gain Variation with Temperature | Relative to $G_{RA}$ | −0.15 | | 0.15 | dB |
| $G_{RAV}$ | Absolute Receive Gain Variation with Supply Voltage | Relative to $G_{RA}$ | **−0.05** | | **0.05** | dB |
| $G_{RRL}$ | Receive Gain Variations with Level | Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded | | | | |
| | | PCM Level =−40 dBm0 to +3 dBm0 | **−0.2** | | **0.2** | dB |
| | | PCM Level =−50 dBm0 to −40 dBm0 | **−0.4** | | **0.4** | dB |
| | | PCM Level =−55 dBm0 to −50 dBm0 | **−1.2** | | **1.2** | dB |
| $V_{RO}$ | Receive Output Drive Level | $R_L$=600Ω | −2.5 | | 2.5 | V |


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## Transmission Characteristics (continued)

Unless otherwise noted, limits printed in **BOLD** characters are ensured for $V_{CC}$ = +5.0V ±5%, $V_{BB}$ = −5.0V ±5%; $T_A$ = −40°C to +85°C by correlation with 100% electrical testing at $T_A$ = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, $V_{IN}$ = 0 dBm0, transmit input amplifier connected for unity gain non inverting. Typicals are specified at $V_{CC}$ = +5.0V, $V_{BB}$ = −5.0V, $T_A$ = 25°C.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **ENVELOPE DELAY DISTORTION WITH FREQUENCY** | | | | | | |
| $D_{XA}$ | Transmit Delay, Absolute | f=1600 Hz | | 290 | 315 | µs |
| $D_{XR}$ | Transmit Delay, Relative to $D_{XA}$ | f=500 Hz−600 Hz | | 195 | 220 | µs |
| | | f=600 Hz−800 Hz | | 120 | 145 | µs |
| | | f=800 Hz−1000 Hz | | 50 | 75 | µs |
| | | f=1000 Hz−1600 Hz | | 20 | 40 | µs |
| | | f=1600 Hz−2600 Hz | | 55 | 75 | µs |
| | | f=2600 Hz−2800 Hz | | 80 | 105 | µs |
| | | f=2800 Hz−3000 Hz | | 130 | 155 | µs |
| $D_{RA}$ | Receive Delay, Absolute | f=1600 Hz | | 180 | 200 | µs |
| $D_{RR}$ | Receive Delay, Relative to $D_{RA}$ | f=500 Hz−1000 Hz | −40 | −25 | | µs |
| | | f=1000 Hz−1600 Hz | −30 | −20 | | µs |
| | | f=1600 Hz−2600 Hz | | 70 | 90 | µs |
| | | f=2600 Hz−2800 Hz | | 100 | 125 | µs |
| | | f=2800 Hz−3000 Hz | | 145 | 175 | µs |
| **NOISE** | | | | | | |
| $N_{XC}$ | Transmit Noise, C Message Weighted | TP3054 (1) | | 12 | **16** | dBrnC0 |
| $N_{XP}$ | Transmit Noise, P Message Weighted | TP3057 (1) | | −74 | **−67** | dBm0p |
| $N_{RC}$ | Receive Noise, C Message Weighted | PCM Code is Alternating Positive and Negative Zero - TP3054 | | 8 | **11** | dBrnC0 |
| $N_{RP}$ | Receive Noise, P Message Weighted | TP3057 PCM Code Equals Positive Zero | | −82 | **−79** | dBm0p |
| $N_{RS}$ | Noise, Single Frequency | f=0 kHz to 100 kHz, Loop Around Measurement, $VF_XI^+$=0 Vrms | | | −53 | dBm0 |
| $PPSR_X$ | Positive Power Supply Rejection, Transmit | $V_{CC}$=5.0 $V_{DC}$+100 mVrms<br>f=0 kHz−50 kHz (2) | **40** | | | dBC |
| $NPSR_X$ | Negative Power Supply Rejection, Transmit | $V_{BB}$=−5.0 $V_{DC}$+ 100 mVrms<br>f=0 kHz−50 kHz (2) | **40** | | | dBC |
| $PPSR_R$ | Positive Power Supply Rejection, Receive | PCM Code Equals Positive Zero<br>$V_{CC}$=5.0 $V_{DC}$+100 mVrms<br>Measure $VF_R0$ | | | | |
| | | f=0 Hz−4000 Hz | **38** | | | dBC |
| | | f=4 kHz−25 kHz | **38** | | | dB |
| | | f=25 kHz−50 kHz | **35** | | | dB |
| $NPSR_R$ | Negative Power Supply Rejection, Receive | PCM Code Equals Positive Zero<br>$V_{BB}$=−5.0 $V_{DC}$+100 mVrms<br>Measure $VF_R0$ | | | | |
| | | f=0 Hz−4000 Hz | **38** | | | dBC |
| | | f=4 kHz−25 kHz | **38** | | | dB |
| | | f=25 kHz−50 kHz | **35** | | | dB |

(1) Measured by extrapolation from the distortion test result at −50 dBm0.
(2) $PPSR_X$, $NPSR_X$, and $CT_{R-X}$ are measured with a −50 dBm0 activation signal applied to $VF_XI^+$.

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## Transmission Characteristics (continued)

Unless otherwise noted, limits printed in **BOLD** characters are ensured for $V_{CC}$ = +5.0V ±5%, $V_{BB}$ = −5.0V ±5%; $T_A$ = −40°C to +85°C by correlation with 100% electrical testing at $T_A$ = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, $V_{IN}$ = 0 dBm0, transmit input amplifier connected for unity gain non inverting. Typicals are specified at $V_{CC}$ = +5.0V, $V_{BB}$ = −5.0V, $T_A$ = 25°C.

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| SOS | Spurious Out-of-Band Signals at the Channel Output | Loop Around Measurement, 0 dBm0, 300 Hz to 3400 Hz Input PCM Code Applied at $D_R$. | | | | −30 | dB |
| | | 4600 Hz–7600 Hz | | | | −30 | dB |
| | | 7600 Hz–8400 Hz | | | | −40 | dB |
| | | 8400 Hz–100,000 Hz | | | | −30 | dB |
| **DISTORTION** | | | | | | | |
| $STD_X$, $STD_R$ | Signal to Total Distortion Transmit or Receive Half-Channel | Sinusoidal Test Method[3] | | | | | |
| | | Level=3.0 dBm0 | | **33** | | | dBC |
| | | =0 dBm0 to −30 dBm0 | | **36** | | | dBC |
| | | =−40 dBm0 | XMT | **28** | | | dBC |
| | | | RCV | **29** | | | dBC |
| | | =−55 dBm0 | XMT | **13** | | | dBC |
| | | | RCV | **14** | | | dBC |
| $SFD_X$ | Single Frequency Distortion, Transmit | | | | | **−43** | dB |
| $SFD_R$ | Single Frequency Distortion, Receive | | | | | **−43** | dB |
| IMD | Intermodulation Distortion | Loop Around Measurement, $VF_XI^+$=−4 dBm0 to −21 dBm0, Two Frequencies in the Range 300 Hz−3400 Hz | | | | **−41** | dB |
| **CROSSTALK** | | | | | | | |
| $CT_{X-R}$ | Transmit to Receive Crosstalk, 0 dBm0 Transmit Level | f=300 Hz−3400 Hz | | | −90 | **−70** | dB |
| | | $D_R$=Quiet PCM Code[4] | | | | | |
| $CT_{R-X}$ | Receive to Transmit Crosstalk, 0 dBm0 Receive Level | f=300 Hz−3400 Hz, $VF_XI$=Multitone[5] | | | −90 | **−70** | dB |

(3) TP3054/57 are measured using C message weighted filter for μ-law and psophometric weighted filter for A-law.
(4) $CT_{X-R}$ @ 1.544 MHz $MCLK_X$ freq. is −70 dB max. 50% ±5% $BCLK_X$ duty cycle.
(5) $PPSR_X$, $NPSR_X$, and $CT_{R-X}$ are measured with a −50 dBm0 activation signal applied to $VF_XI^+$.


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### Encoding Format at $D_X$ Output

| | TP3054 μ-Law | | | | | | | | TP3057 A-Law (Includes Even Bit Inversion) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IN}$ (at $GS_X$)=+Full-Scale | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| $V_{IN}$ (at $GS_X$)=0V | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| $V_{IN}$ (at $GS_X$)=−Full-Scale | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |

## APPLICATIONS INFORMATION

### POWER SUPPLIES

While the pins of the TP3050 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a “hot” socket with power and clocks already present, an extra long ground pin in the connector should be used.

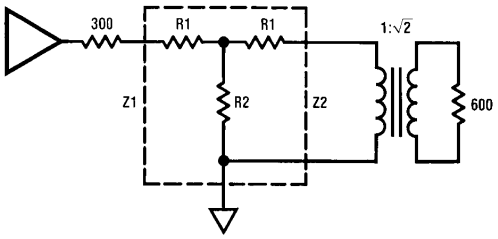
All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to $V_{CC}$ and $V_{BB}$, as close to device pins as possible.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus.

This common ground point should be decoupled to $V_{CC}$ and $V_{BB}$ with 10 μF capacitors.

### RECEIVE GAIN ADJUSTMENT

For applications where a TP3050 family CODEC/filter receive output must drive a 600Ω load, but a peak swing lower than ±2.5V is required, the receive gain can be easily adjusted by inserting a matched T-pad or π-pad at the output. Table 2 lists the required resistor values for 600Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest practical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30 dB return loss against 600Ω is obtained if the output impedance of the attenuator is in the range 282Ω to 319Ω (assuming a perfect transformer).




$$R1 = Z1\left(\frac{N^2+1}{N^2-1}\right) - 2\sqrt{Z1 \cdot Z2}\left(\frac{N}{N^2-1}\right)$$

$$R2 = 2\sqrt{Z1 \cdot Z2}\left(\frac{N}{N^2-1}\right)$$

$$\text{Where: } N = \sqrt{\frac{\text{POWER IN}}{\text{POWER OUT}}}$$

and

$$S = \sqrt{\frac{Z1}{Z2}}$$

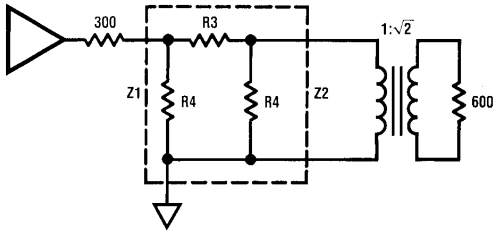
$$\text{Also: } Z = \sqrt{Z_{SC} \bullet Z_{OC}}$$

Where $Z_{SC}$ = impedance with short circuit termination

and $Z_{OC}$ = impedance with open circuit termination

**Figure 6. T-Pad Attenuator**

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$$R3 = \sqrt{\frac{Z1 \cdot Z2}{2}}\left(\frac{N^2 - 1}{N}\right)$$

$$R3 = Z1\left(\frac{N^2 - 1}{N^2 - 2NS + 1}\right)$$

**Note:** See Application Note 370 for further details.

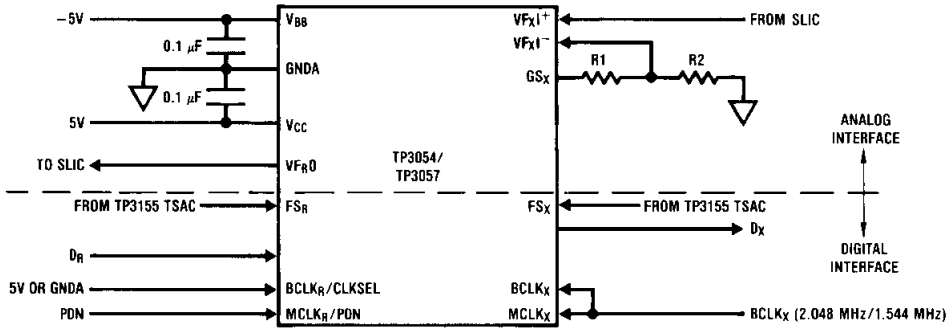
**Figure 7. π-Pad Attenuator**

**Table 2. Attentuator Tables for Z1=Z2=300Ω (All Values in Ω)**

| dB | R1 | R2 | R3 | R4 |
|---|---|---|---|---|
| 0.1 | 1.7 | 26k | 3.5 | 52k |
| 0.2 | 3.5 | 13k | 6.9 | 26k |
| 0.3 | 5.2 | 8.7k | 10.4 | 17.4k |
| 0.4 | 6.9 | 6.5k | 13.8 | 13k |
| 0.5 | 8.5 | 5.2k | 17.3 | 10.5k |
| 0.6 | 10.4 | 4.4k | 21.3 | 8.7k |
| 0.7 | 12.1 | 3.7k | 24.2 | 7.5k |
| 0.8 | 13.8 | 3.3k | 27.7 | 6.5k |
| 0.9 | 15.5 | 2.9k | 31.1 | 5.8k |
| 1.0 | 17.3 | 2.6l | 34.6 | 5.2k |
| 2 | 34.4 | 1.3k | 70 | 2.6k |
| 3 | 51.3 | 850 | 107 | 1.8k |
| 4 | 68 | 650 | 144 | 1.3k |
| 5 | 84 | 494 | 183 | 1.1k |
| 6 | 100 | 402 | 224 | 900 |
| 7 | 115 | 380 | 269 | 785 |
| 8 | 379 | 284 | 317 | 698 |
| 9 | 143 | 244 | 370 | 630 |
| 10 | 156 | 211 | 427 | 527 |
| 11 | 168 | 184 | 490 | 535 |
| 12 | 180 | 161 | 550 | 500 |
| 13 | 190 | 142 | 635 | 473 |
| 14 | 200 | 125 | 720 | 450 |
| 15 | 210 | 110 | 816 | 430 |
| 16 | 218 | 98 | 924 | 413 |
| 18 | 233 | 77 | 1.17k | 386 |
| 20 | 246 | 61 | 1.5k | 366 |


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## Typical Synchronous Application




**Note 1:** XMIT gain $= 20 \times \log\left(\frac{R1+R2}{R2}\right)$, $(R1+R2) > 10\ K\Omega$.

**Figure 8.**

## REVISION HISTORY

| Changes from Revision B (April 2013) to Revision C | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 15 |


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TP3054WM-X/63 | NRND | SOIC | DW | 16 | 1000 | TBD | Call TI | Call TI | | TP3054WM-X COMBO$R | |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

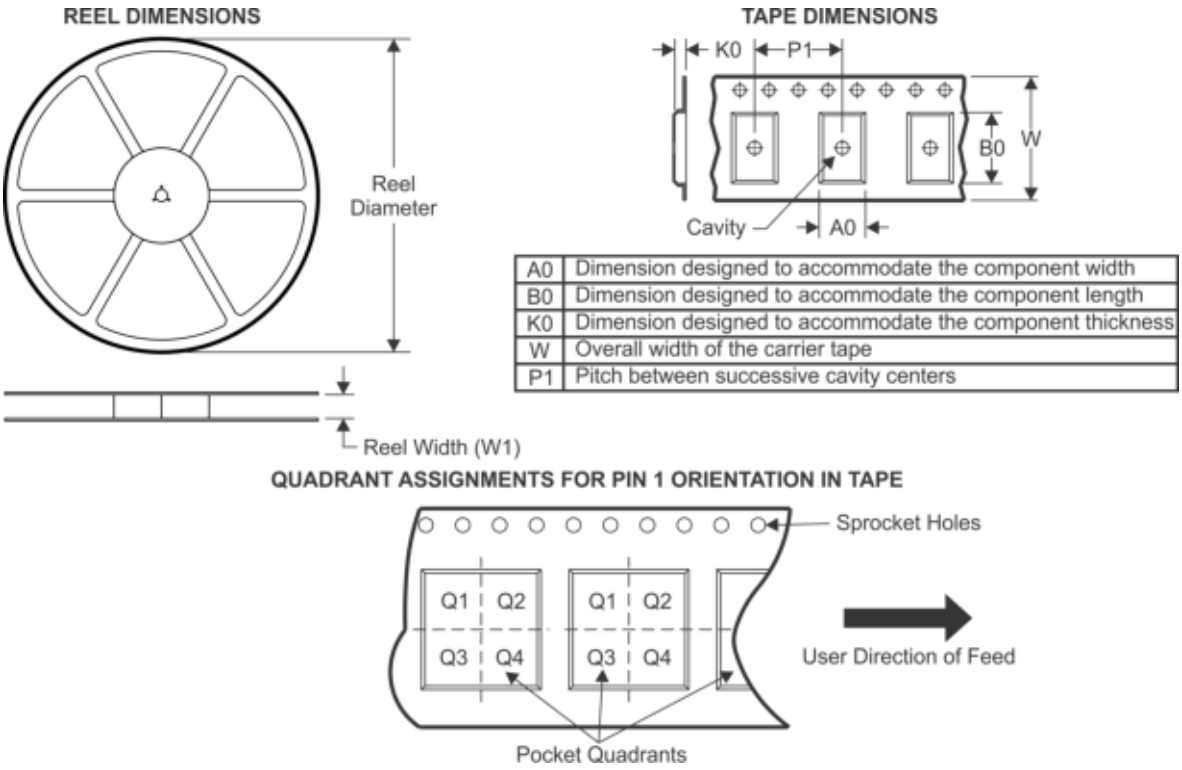
**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION

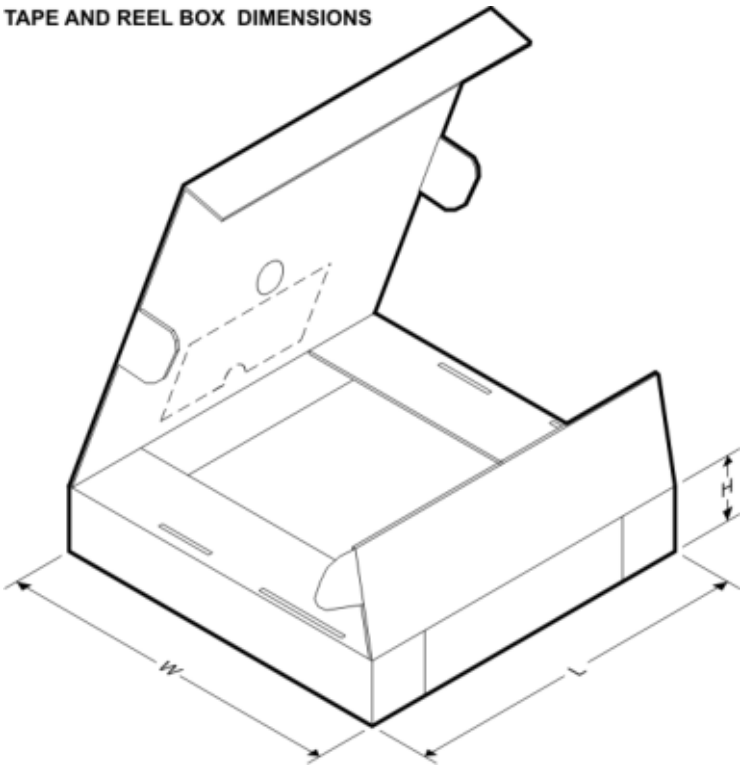



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TP3054WM-X/63 | SOIC | DW | 16 | 1000 | 330.0 | 16.4 | 10.9 | 10.7 | 3.2 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

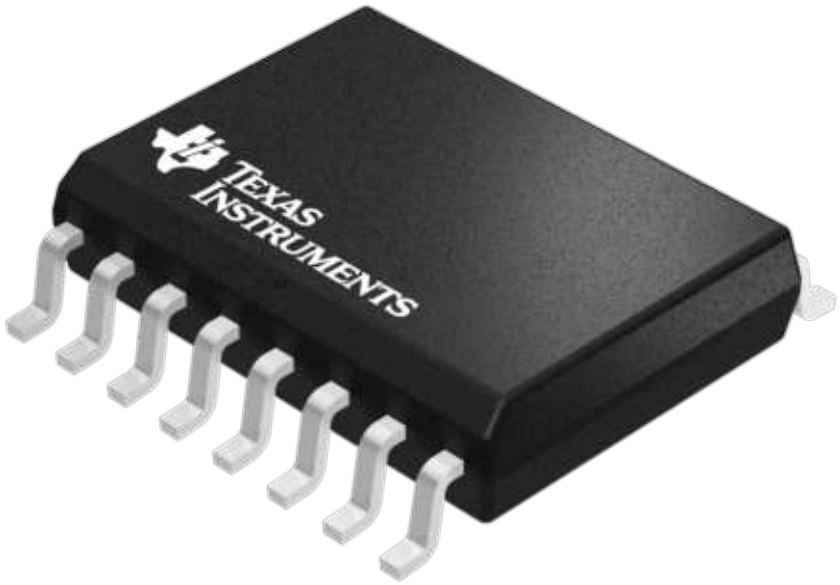



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TP3054WM-X/63 | SOIC | DW | 16 | 1000 | 367.0 | 367.0 | 38.0 |

# DW 16 SOIC - 2.65 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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