transphorm

TPH3206LS

600V Cascode GaN FET in PQFN88 (source tab)

Not recommended for new designs—see TPH3206LSB

Description

The TPH3206LS 600V, 150mΩ gallium nitride (GaN) FET is a normally-off device. Transphorm GaN FETs offer better efficiency through lower gate charge, faster switching speeds, and smaller reverse recovery charge, delivering significant advantages over traditional silicon (Si) devices.

Transphorm is a leading-edge wide band gap supplier with world-class innovation and a portfolio of fully-qualified GaN transistors that enables increased performance and reduced overall system size and cost.

Related Literature

- AN0009: Recommended External Circuitry for GaN FETs
- AN0003: Printed Circuit Board Layout and Probing

Ordering Information

Part Number*	Package	Package Configuration
TPH3206LS	8 x 8mm PQFN	Common Source

* Add "-TR" suffix for tape and reel; see page 9

TPH3206LS
8x8 PQFN
(bottom view)



Features

- Easy to drive—compatible with standard gate drivers
- Low conduction and switching losses
- Low Qrr of 52nC—no free-wheeling diode required
- JEDEC-qualified GaN technology
- RoHS compliant and Halogen-free

Benefits

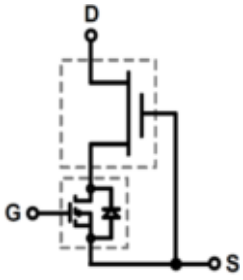
- Increased efficiency through fast switching
- Increased power density
- Reduced system size and weight
- Enables more efficient topologies—easy to implement bridgeless totem-pole designs
- Lower BOM cost

Applications

- Renewable energy
- Industrial
- Telecom and datacom
- Servo motors

Key Specifications	
V_{DS} (V) min	600
V_{TDS} (V) max	750
$R_{DS(on)}$ (mΩ) max*	180
Q_{rr} (nC) typ	52
Qg (nC) typ	6

* Dynamic $R_{(on)}$



Cascode Device Structure

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Absolute Maximum Ratings (T_C=25°C unless otherwise stated)

Symbol	Parameter		Limit Value	Unit
$I_{D25°C}$	Continuous drain current @T_C=25°C [a]		17	A
$I_{D100°C}$	Continuous drain current @T_C=100°C [a]		12	A
I_{DM}	Pulsed drain current (pulse width: 100µs)		60	A
V_{DSS}	Drain to source voltage		600	V
V_{TDS}	Transient drain to source voltage [b]		750	V
V_{GSS}	Gate to source voltage		±18	V
$P_{D25°C}$	Maximum power dissipation		96	W
T_C	Operating temperature	Case	-55 to +150	°C
T_J		Junction	-55 to +175	°C
T_S	Storage temperature		-55 to +150	°C
T_{CSOLD}	Soldering peak temperature [c]		260	°C

Thermal Resistance

Symbol	Parameter	Typical	Unit
$R_{\Theta JC}$	Junction-to-case	1.55	°C/W
$R_{\Theta JA}$	Junction-to-ambient [d]	45	°C/W

Notes:
a. For high current operation, see application note AN0009
b. In off-state, spike duty cycle D<0.1, spike duration <1µs
c. Reflow MSL3
d. Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling; with 6cm² copper area and 70µm thickness)

Electrical Parameters (T_C=25°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
$V_{DSS-MAX}$	Maximum drain-source voltage	600	—	—	V	V_{GS}=0V
$V_{GS(th)}$	Gate threshold voltage [e]	1.65	2.1	2.6	V	V_{DS}=V_{GS}, I_D=500μA
$R_{DS(on)}$	Drain-source on-resistance (T_J=25°C) [a]	—	150	180	mΩ	V_{GS}=8V, I_D=11A, T_J=25°C
	Drain-source on-resistance (T_J=175°C) [a]	—	340	—		V_{GS}=8V, I_D=11A, T_J=175°C
I_{DSS}	Drain-to-source leakage current (T_J=25°C)	—	2.5	30	μA	V_{DS}=600V, V_{GS}=0V, T_J=25°C
	Drain-to-source leakage current (T_J=150°C)	—	8	—		V_{DS}=600V, V_{GS}=0V, T_J=150°C
I_{GSS}	Gate-to-source forward leakage current	—	—	100	nA	V_{GS}=18V
	Gate-to-source reverse leakage current	—	—	-100		V_{GS}=-18V
C_{ISS}	Input capacitance	—	760	—	pF	V_{GS}=0V, V_{DS}=480V, *f*=1MHz
C_{OSS}	Output capacitance	—	44	—		
C_{RSS}	Reverse transfer capacitance	—	5	—		
$C_{O(er)}$	Output capacitance, energy related [b]	—	64	—	pF	V_{GS}=0V, V_{DS}=0V to 480V
$C_{O(tr)}$	Output capacitance, time related [c]	—	105	—		
Q_g	Total gate charge [d]	—	6.2	9.3	nC	V_{DS}=100V, V_{GS}=0V to 4.5V, I_D=11A
Q_{gs}	Gate-source charge	—	2.1	—		
Q_{gd}	Gate-drain charge	—	2.2	—		
$t_{d(on)}$	Turn-on delay	—	6	—	ns	V_{DS}=480V, V_{GS}=0V to 10V, I_D=11A, R_G=2Ω
t_r	Rise time	—	4.5	—		
$T_{d(off)}$	Turn-off delay	—	9.7	—		
t_f	Fall time	—	4	—		
Reverse Device Characteristics						
I_S	Reverse current	—	—	12	A	V_{GS}=0V, T_C=100°C, ≤50% Duty Cycle
V_{SD}	Reverse voltage [a]	—	2.6	—	V	V_{GS}=0V, I_S=12A, T_J=25°C
		—	4.6	—		V_{GS}=0V, I_S=12A, T_J=175°C
		—	1.8	—		V_{GS}=0V, I_S=6A, T_J=25°C
t_{rr}	Reverse recovery time	—	17	—	ns	I_S=11A, V_{DD}=400V, di/dt=2000A/μs, T_J=25°C
Q_{rr}	Reverse recovery charge	—	52	—	nC	

Notes:
a. Dynamic value
b. Equivalent capacitance to give same stored energy from 0V to 480V
c. Equivalent capacitance to give same charging time from 0V to 480V
d. Q_g does not change for V_{DS}>100V
e. Recommended gate drive: Turn on +8V, turn off 0 or -5V. For half bridge, use isolated driver ICs with 5V UVLO.

Typical Characteristics (25°C unless otherwise stated)

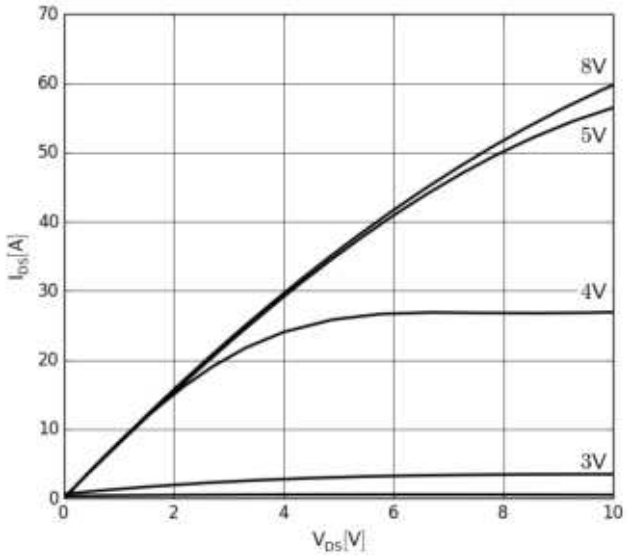


Figure 1. Typical Output Characteristics T_J=25°C
Parameter: V_{GS}

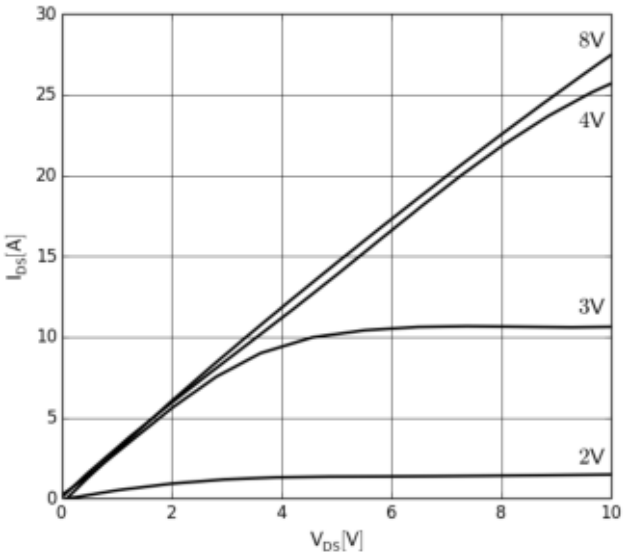


Figure 2. Typical Output Characteristics T_J=175°C
Parameter: V_{GS}

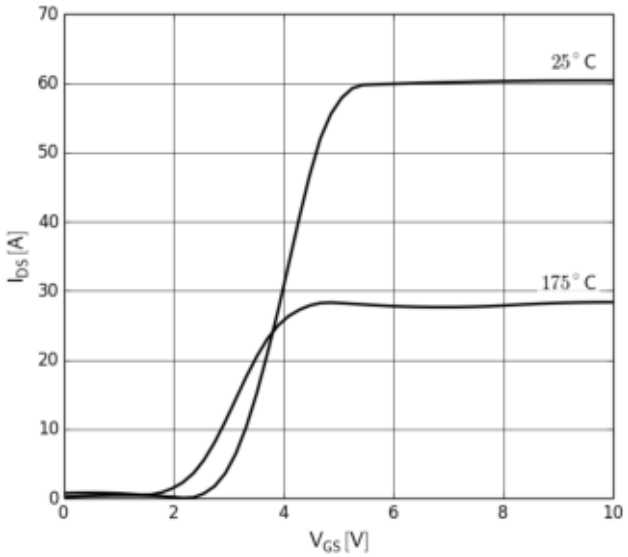


Figure 3. Typical Transfer Characteristics
V_{DS}=10V, Parameter: T_J

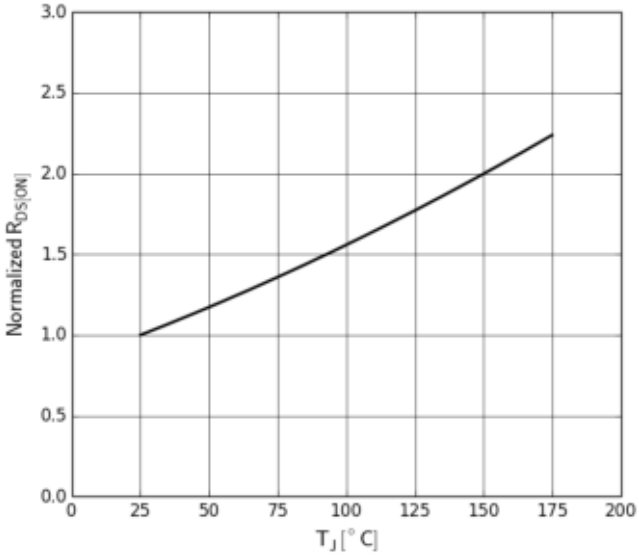


Figure 4. Normalized On-Resistance
I_D=12A, V_{GS}=8V

Typical Characteristics (25 °C unless otherwise stated)

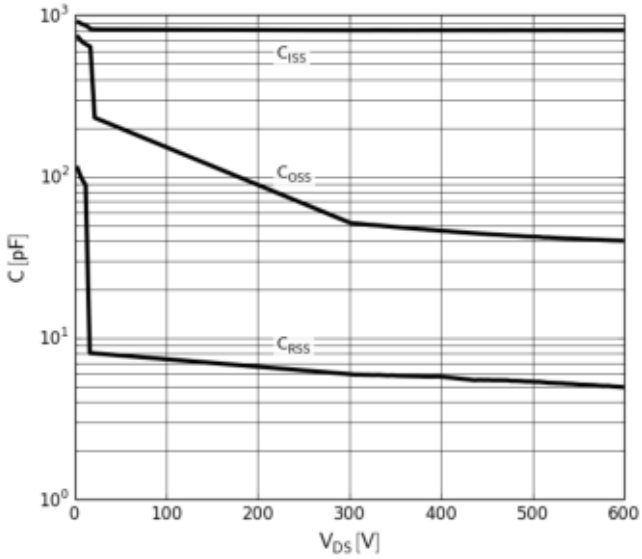


Figure 5. Typical Capacitance
V_{GS}=0V, f=1MHz

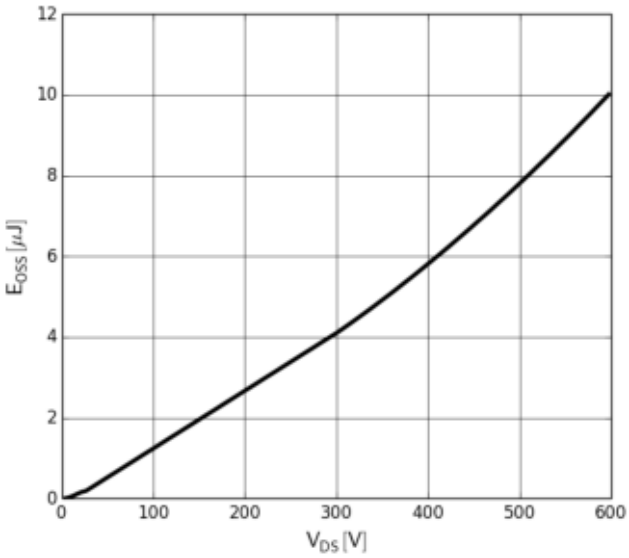


Figure 6. Typical C_{oss} Stored Energy

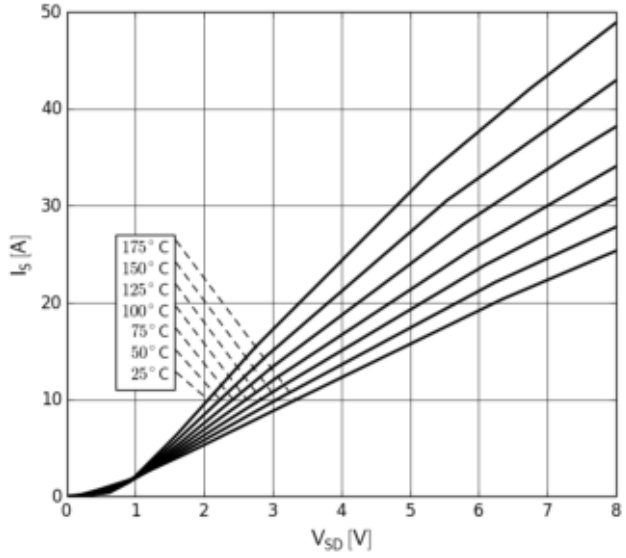


Figure 7. Forward Characteristics of Rev. Diode
$I_S=f(V_{SD})$, Parameter T_J

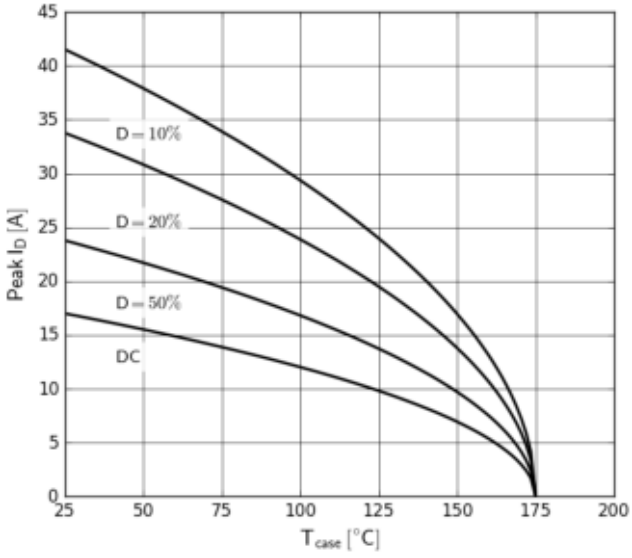


Figure 8. Current Derating
Pulse width ≤ 100µs

Typical Characteristics (25 °C unless otherwise stated)

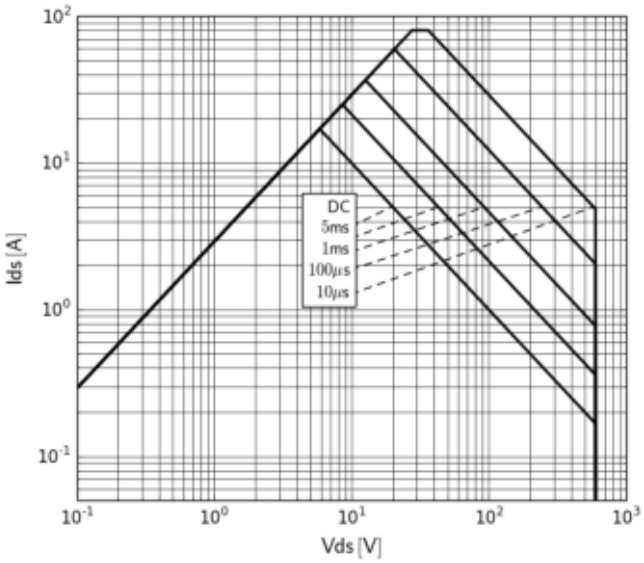


Figure 9. Safe Operating Area T_C=25 °C (calculated based based on thermal limit)

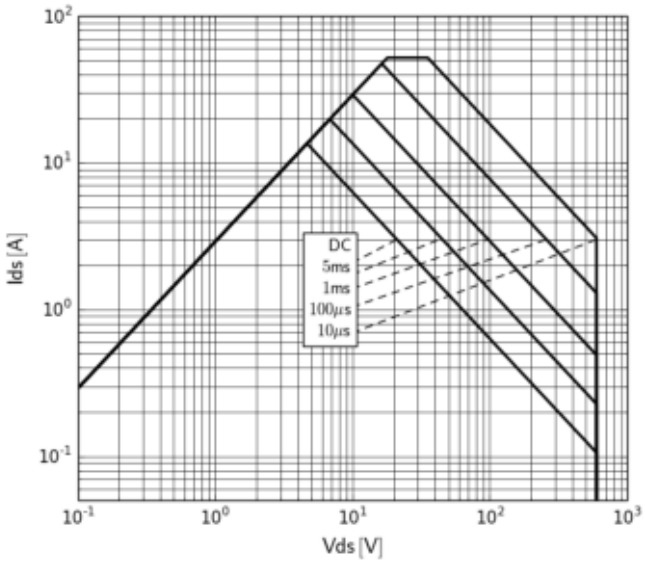


Figure 10. Safe Operating Area T_C=80 °C (calculated based on thermal limit)

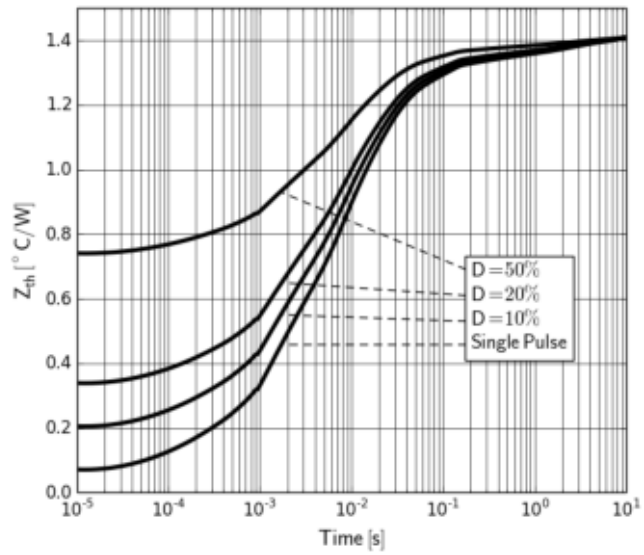


Figure 11. Transient Thermal Resistance

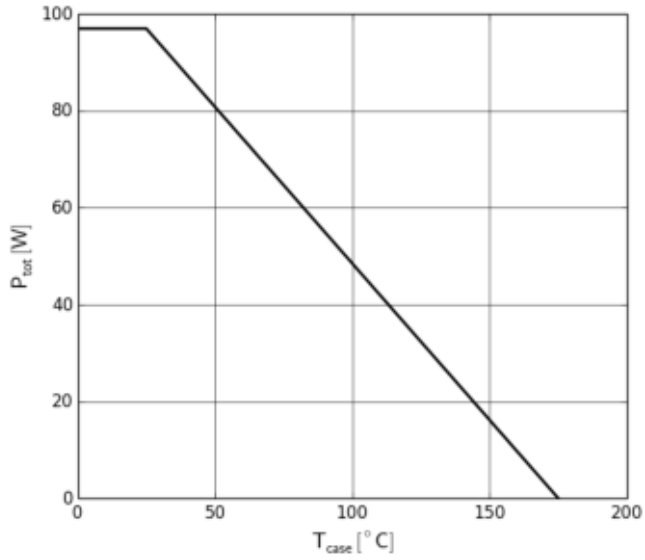


Figure 12. Power Dissipation

Test Circuits and Waveforms

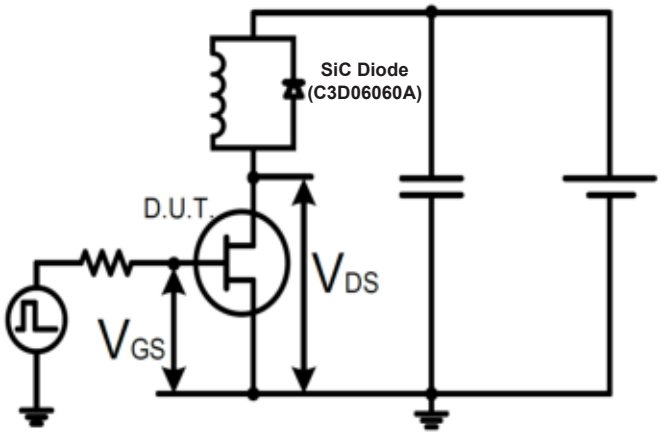


Figure 13. Switching Time Test Circuit
***See app note AN0009 for methods to ensure clean switching**

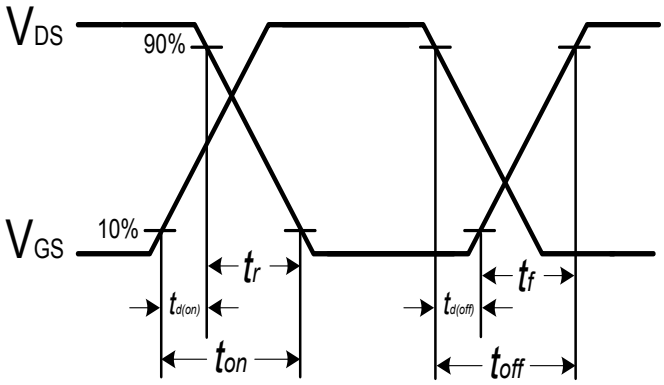


Figure 14. Switching Time Waveform

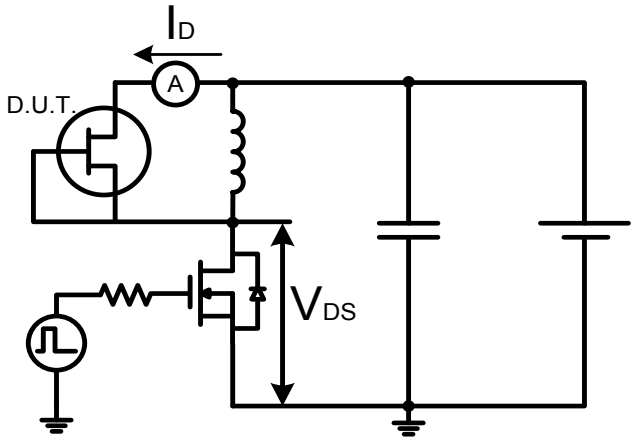


Figure 15. Test Circuit for Diode Characteristics

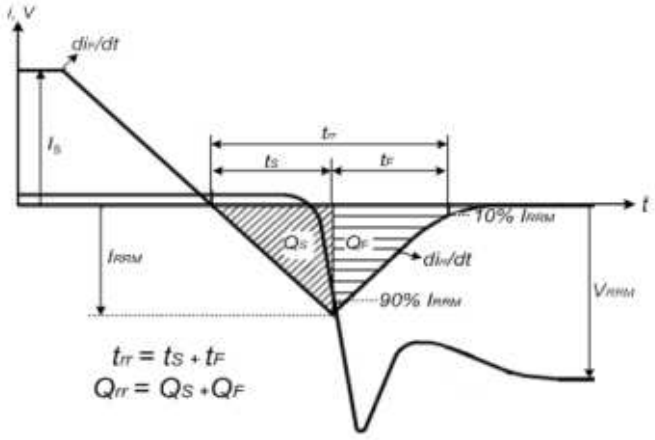


Figure 16. Diode Recovery Waveform

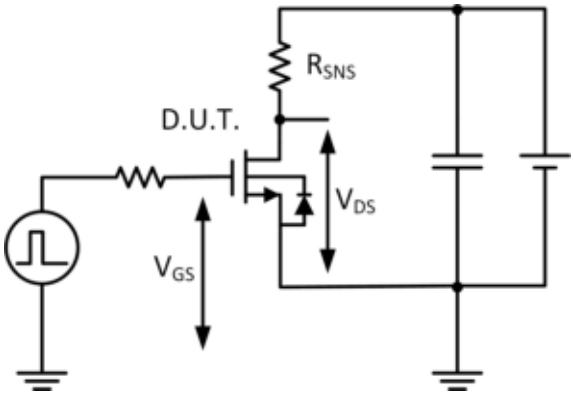


Figure 17. Test Circuit for Dynamic $R_{DS(on)}$

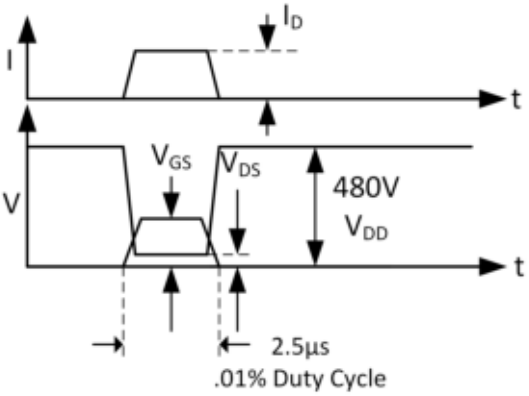
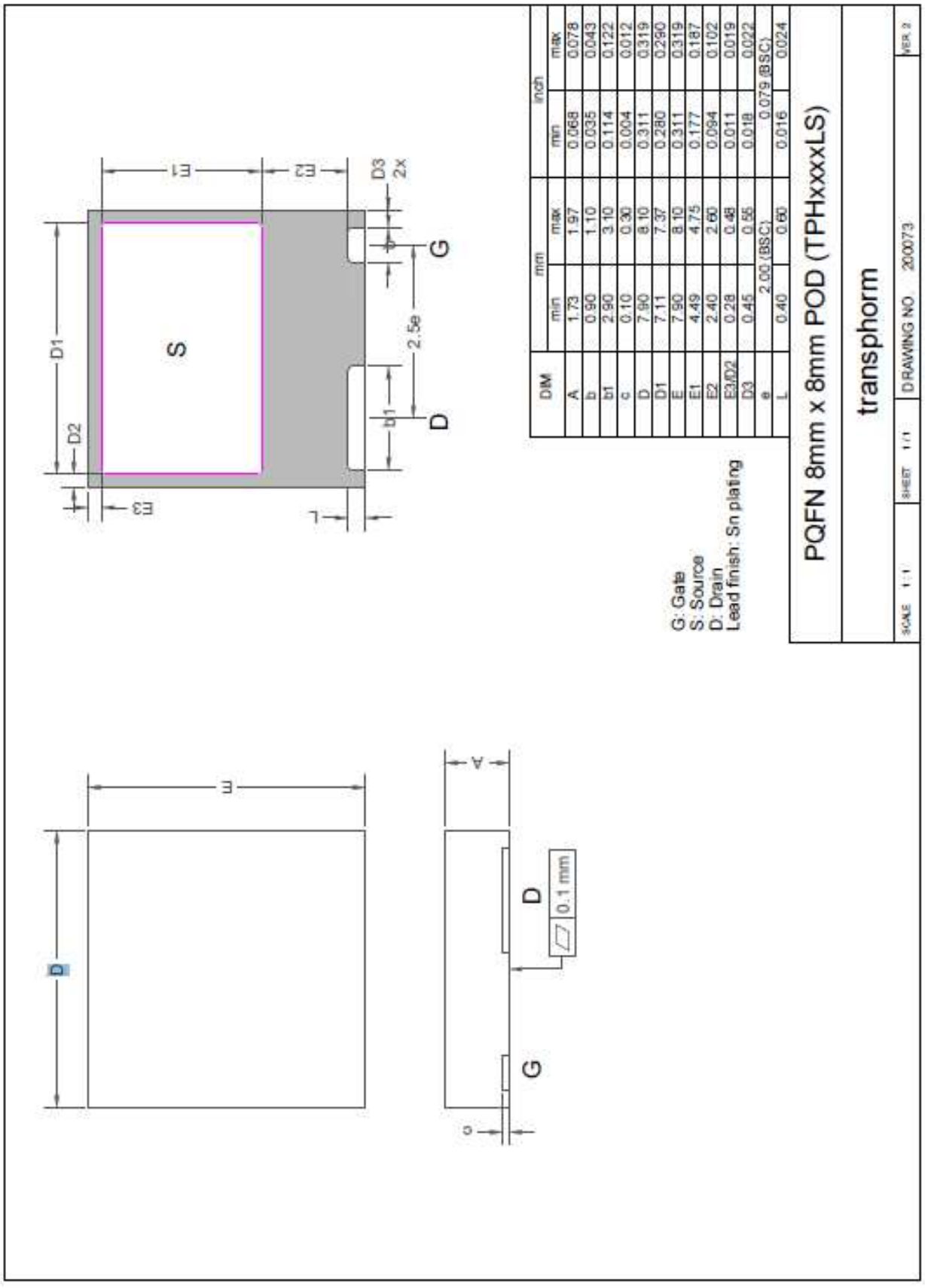


Figure 18. Dynamic $R_{DS(on)}$ Waveform

8x8 PQFN (LS) Package

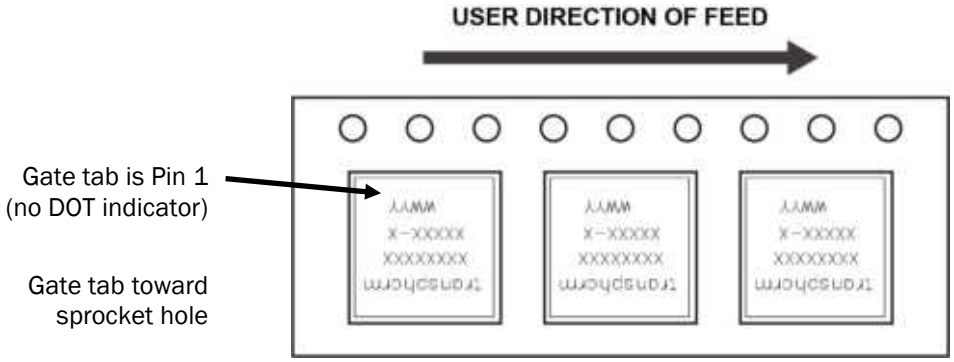
Mechanical



DIM	mm		inch	
	min	max	min	max
A	1.73	1.97	0.068	0.078
b	0.90	1.10	0.035	0.043
b1	2.90	3.10	0.114	0.122
c	0.10	0.30	0.004	0.012
D	7.90	8.10	0.311	0.319
D1	7.11	7.37	0.280	0.290
E	7.90	8.10	0.311	0.319
E1	4.49	4.75	0.177	0.187
E2	2.40	2.60	0.094	0.102
E3/D2	0.28	0.48	0.011	0.019
D3	0.45	0.55	0.018	0.022
e	2.00 (BSC)		0.079 (BSC)	
L	0.40	0.60	0.016	0.024

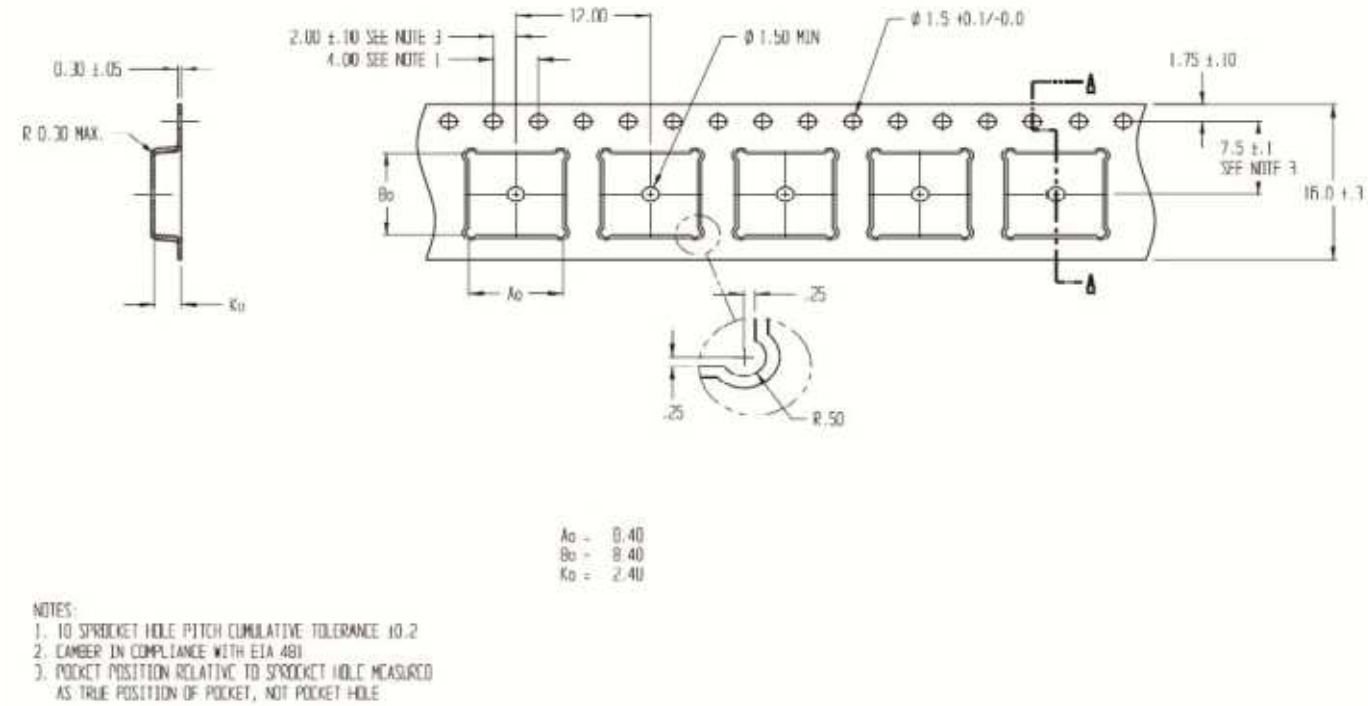
PQFN88 Tape and Reel Information

Product Orientation



- Leader empty pockets: 400mm/15.75” min
- Trailer empty pickets: 160mm/6.3” min
- Quantity per reel: 500 pcs

Carrier Tape Dimension



Design Considerations

The fast switching of GaN devices reduces current-voltage cross-over losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Transphorm GaN devices, see application note Printed Circuit Board Layout and Probing for GaN Power Switches. The table below provides some practical rules that should be followed during the evaluation.

When Evaluating Transphorm GaN Devices:

DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See AN0003: Printed Circuit Board Layout and Probing	

Application Notes

- AN0002: Characteristics of Transphorm GaN Power Switches
- AN0003: Printed Circuit Board Layout and Probing
- AN0004: Designing Hard-switched Bridges with GaN
- AN0007: PQFN Lead-Free 2nd Level Soldering Recommendations for Vapor Phase Reflow
- AN0008: Drain Voltage and Avalanche Ratings for GaN FETs
- AN0009: Recommended External Circuitry for GaN FETs

Evaluation Boards

- TDPV1000E0C1-KIT: 1kW inverter evaluation platform
- TDPS1000E0E10-KIT: 1kW hard-switched half-bridge, buck, or boost evaluation platform

Revision History

Version	Date	Change(s)
7	11/15/2016	Added application note AN0009
8	12/12/2016	Formatting Changes to p. 3, revision of dynamic measurement verbiage
9	2/20/2017	Updated ordering info, updated evaluation board list, added gate drive suggestion, marked NRND—see TPH3206LSB