# TPS2090, TPS2091, TPS2092 DUAL
# TPS2095, TPS2096, TPS2097 QUAD

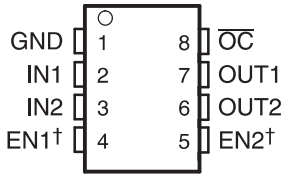
SLVS245C–SEPTEMBER 2000–REVISED OCTOBER 2007

## POWER-DISTRIBUTION SWITCHES

## FEATURES

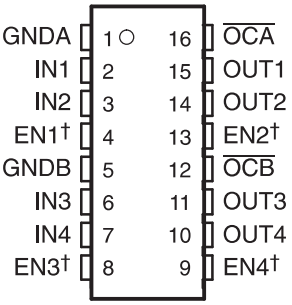
- **80-mΩ High-Side MOSFET Switch**
- **250 mA Continuous Current per Channel**
- **Independent Thermal and Short-Circuit Protection With Overcurrent Logic Output**
- **Operating Range: 2.7-V to 5.5-V**
- **CMOS- and TTL-Compatible Enable Inputs**
- **2.5-ms Typical Rise Time**
- **Undervoltage Lockout**
- **10 µA Maximum Standby Supply Current**
- **Bidirectional Switch**
- **Available in 8-Pin and 16-Pin SOIC Packages**
- **Ambient Temperature Range, 0°C to 85°C**
- **ESD Protection**

**TPS2090, TPS2091, AND TPS2092**
**D PACKAGE**
**(TOP VIEW)**




† See Available Options table

**TPS2095, TPS2096 AND TPS2097**
**D PACKAGE**
**(TOP VIEW)**




† See Available Options table

## DESCRIPTION

The TPS2090, TPS2091, and TPS2092 dual and the TPS2095, TPS2096 and TPS2097 quad power-distribution switches are intended for applications where heavy capacitive loads and short circuits are likely to be encountered. The TPS209x devices incorporate 80-mΩ N-channel MOSFET high-side power switches for power-distribution systems that require multiple power switches in a single package. Each switch is controlled by an independent logic enable input. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

**GENERAL SWITCH CATALOG**

| 33 mΩ, Single | 80 mΩ, Single | 80 mΩ, Dual | 80 mΩ, Dual | 80 mΩ, Triple | 80 mΩ, Quad | 80 mΩ, Quad |
|---|---|---|---|---|---|---|
| TPS201xA 0.2 A to 2 A<br>TPS202x 0.2 A to 2 A<br>TPS203x 0.2 A to 2 A | TPS2014 600 mA<br>TPS2015 1 A<br>TPS2041B 500 mA<br>TPS2051B 500 mA<br>TPS2045A 250 mA<br>TPS2049 100 mA<br>TPS2055A 250 mA<br>TPS2061 1 A<br>TPS2065 1 A<br>TPS2068 1.5 A<br>TPS2069 1.5 A | TPS2042B 500 mA<br>TPS2052B 500 mA<br>TPS2046B 250 mA<br>TPS2056 250 mA<br>TPS2062 1 A<br>TPS2066 1 A<br>TPS2060 1.5 A<br>TPS2064 1.5 A | TPS2080 500 mA<br>TPS2081 500 mA<br>TPS2082 500 mA<br>TPS2090 250 mA<br>TPS2091 250 mA<br>TPS2092 250 mA | TPS2043B 500 mA<br>TPS2053B 500 mA<br>TPS2047B 250 mA<br>TPS2057A 250 mA<br>TPS2063 1 A<br>TPS2067 1 A | TPS2044B 500 mA<br>TPS2054B 500 mA<br>TPS2048A 250 mA<br>TPS2058 250 mA | TPS2085 500 mA<br>TPS2086 500 mA<br>TPS2087 500 mA<br>TPS2095 250 mA<br>TPS2096 250 mA<br>TPS2097 250 mA |

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2000–2007, Texas Instruments Incorporated



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## DESCRIPTION (CONTINUED)

When the output load exceeds the current-limit threshold or a short is present, the TPS209x limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{OC}$x) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until valid input voltage is present. The TPS209x devices are designed to current limit at 0.5-A load.

### AVAILABLE OPTIONS(1)

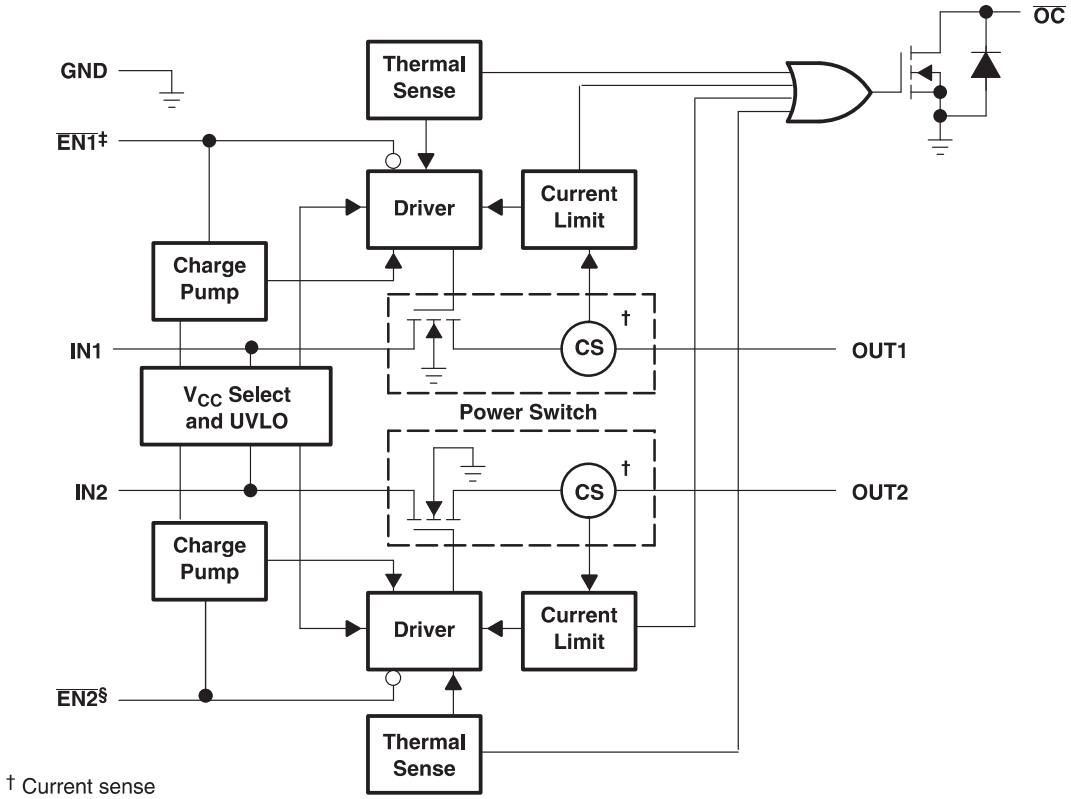
| DUAL POWER DISTRIBUTION SWITCHES | | | | | |
|---|---|---|---|---|---|
| $T_A$ | ENABLE | | RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A) | TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (A) | PACKAGED DEVICES |
| | EN1 | EN2 | | | SMALL OUTLINE (D)(2) |
| 0°C to 85°C | Active high | Active high | 0.25 | 0.5 | TPS2090D |
| | Active high | Active low | | | TPS2091D |
| | Active low | Active low | | | TPS2092D |

| QUAD POWER DISTRIBUTION SWITCHES | | | | | | | |
|---|---|---|---|---|---|---|---|
| $T_A$ | ENABLE | | | | RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A) | TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (A) | PACKAGED DEVICES |
| | EN1 | EN2 | EN3 | DN4 | | | SMALL OUTLINE (D)(2) |
| 0°C to 85°C | Active high | Active high | Active high | Active high | 0.25 | 0.5 | TPS2095D |
| | Active high | Active low | Active high | Active low | | | TPS2096D |
| | Active low | Active low | Active low | Active low | | | TPS2097D |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2091DR).

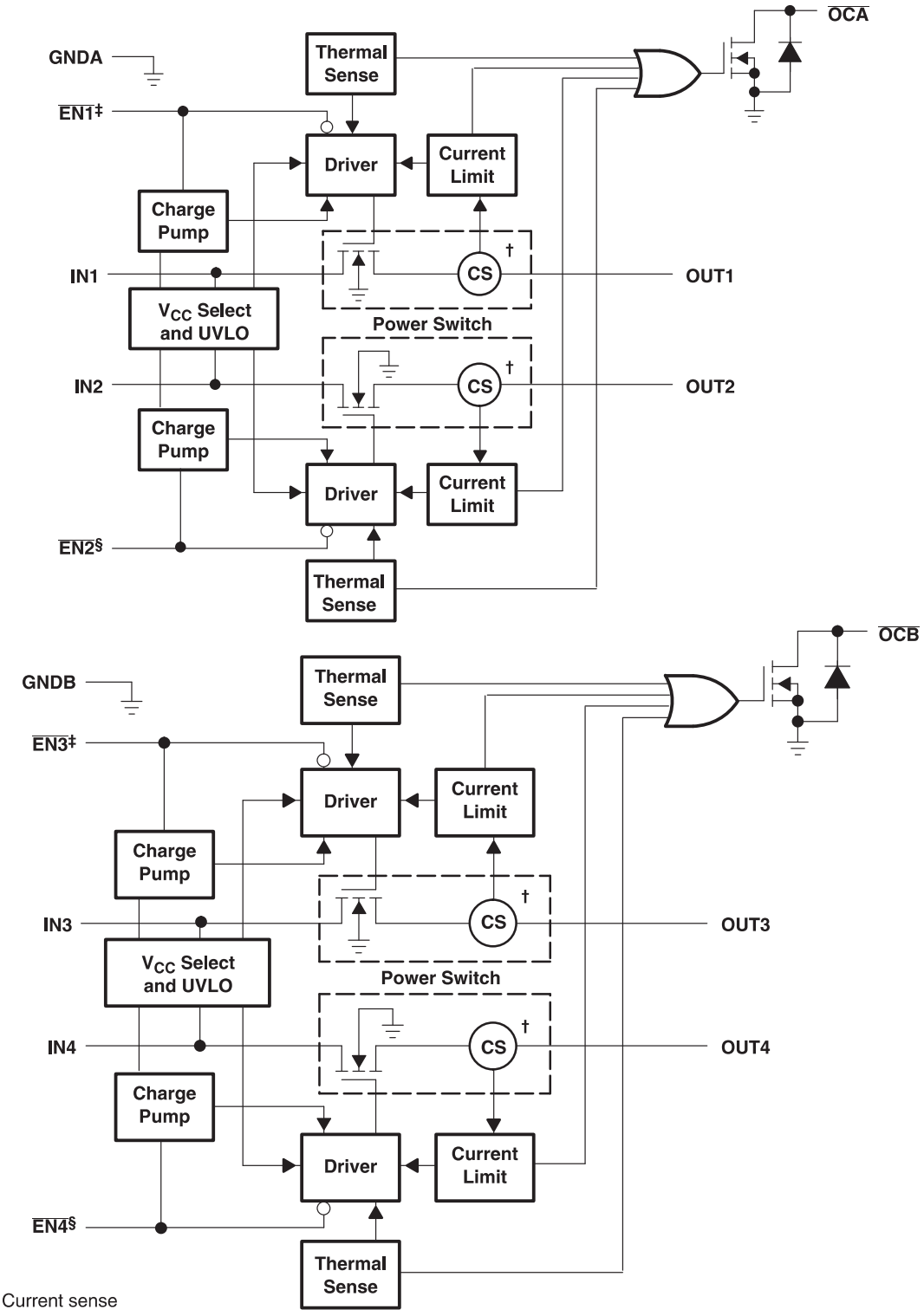

Copyright © 2000–2007, Texas Instruments Incorporated

## TPS2092 FUNCTIONAL BLOCK DIAGRAM




† Current sense
‡ Active high for TPS2090 and TPS2091
§ Active high for TPS2090

## TPS2097 FUNCTIONAL BLOCK DIAGRAM




† Current sense
‡ Active high for TPS2095 and TPS2096
§ Active high for TPS2095


Copyright © 2000–2007, Texas Instruments Incorporated

## TERMINAL FUNCTIONS

| DUAL POWER-DISTRIBUTION SWITCHES | | | | | |
|---|---|---|---|---|---|
| TERMINAL | | | | I/O | DESCRIPTION |
| NAME | NO. | | | | |
| | TPS2090 | TPS2091 | TPS2092 | | |
| $\overline{EN1}$ | | | 4 | I | Enable input. Active low turns on power switch. |
| $\overline{EN2}$ | | 5 | 5 | I | Enable input. Active low turns on power switch. |
| EN1 | 4 | 4 | | I | Enable input. Active high turns on power switch. |
| EN2 | 5 | | | I | Enable input. Active high turns on power switch. |
| GND | 1 | 1 | 1 | I | Ground |
| IN1 | 2 | 2 | 2 | I | N-Channel MOSFET Drain |
| IN2 | 3 | 3 | 3 | I | N-Channel MOSFET Drain |
| $\overline{OC}$ | 8 | 8 | 8 | O | Overcurrent. Open drain output active low |
| OUT1 | 7 | 7 | 7 | O | Power-switch output |
| OUT2 | 6 | 6 | 6 | O | Power-switch output |

| QUAD POWER-DISTRIBUTION SWITCHES | | | | | |
|---|---|---|---|---|---|
| TERMINAL | | | | I/O | DESCRIPTION |
| NAME | NO. | | | | |
| | TPS2095 | TPS2096 | TPS2097 | | |
| $\overline{EN1}$ | | | 4 | I | Enable input. Active low turns on power switch. |
| $\overline{EN2}$ | | 13 | 13 | I | Enable input. Active low turns on power switch. |
| $\overline{EN3}$ | | | 8 | I | Enable input. Active low turns on power switch. |
| $\overline{EN4}$ | | 9 | 9 | I | Enable input. Active low turns on power switch. |
| EN1 | 4 | 4 | | I | Enable input. Active high turns on power switch. |
| EN2 | 13 | | | I | Enable input. Active high turns on power switch. |
| EN3 | 8 | 8 | | I | Enable input. Active high turns on power switch. |
| EN4 | 9 | | | I | Enable input. Active high turns on power switch. |
| GNDA | 1 | 1 | 1 | | Ground for IN1 and IN2 switch and circuitry |
| GNDB | 5 | 5 | 5 | | Ground for IN3 and IN4 switch and circuitry |
| IN1 | 2 | 2 | 2 | I | N-channel MOSFET drain |
| IN2 | 3 | 3 | 3 | I | N-channel MOSFET drain |
| IN3 | 6 | 6 | 6 | I | N-channel MOSFET drain |
| IN4 | 7 | 7 | 7 | I | N-channel MOSFET drain |
| $\overline{OCA}$ | 16 | 16 | 16 | O | Overcurrent indicator for switch 1 and switch 2. Active-low open drain output. |
| $\overline{OCB}$ | 12 | 12 | 12 | O | Overcurrent indicator for switch 3 and switch 4. Active low open drain output |
| OUT1 | 15 | 15 | 15 | O | Power-switch output |
| OUT2 | 14 | 14 | 14 | O | Power-switch output |
| OUT3 | 11 | 11 | 11 | O | Power-switch output |
| OUT4 | 10 | 10 | 10 | O | Power-switch output |

Copyright © 2000–2007, Texas Instruments Incorporated

# DETAILED DESCRIPTION

## POWER SWITCH

The power switch is an N-channel MOSFET with a maximum on-state resistance of 135 mΩ ($V_{I(IN)}$ = 5V). Configured as a high-side switch, the power switch prevents current flow from OUTx to IN and IN to OUTx when disabled. The power switch supplies a minimum of 250mA per switch.

## CHARGE PUMP

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7V and requires very little supply current.

## DRIVER

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 4-ms range.

## ENABLE ($\overline{\text{ENx}}$ or ENx)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10 µA when a logic high is present on $\overline{\text{ENx}}$ or a logic low is present on ENx. A logic low input on $\overline{\text{ENx}}$ or logic high on ENx restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

## OVERCURRENT ($\overline{\text{OCx}}$)

The $\overline{\text{OCx}}$ open drain output is asserted (active low) when an overcurrent or over temperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed.

## CURRENT SENSE

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant current mode and holds the current constant while varying the voltage on the load.

## THERMAL SENSE

The TPS209x implements a dual thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition the junction temperature rises. When the die temperature rises to approximately 140°C, the internal thermal sense circuitry checks to determine which power switch is in an overcurrent condition and turns off that switch, thus isolating the fault without interrupting operation of the adjacent power switch. Hysteresis is built into the thermal sense, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed. The ($\overline{\text{OCx}}$) open-drain output is asserted (active low) when overtemperature or overcurrent occurs.

## UNDERVOLTAGE LOCKOUT

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.


Copyright © 2000–2007, Texas Instruments Incorporated

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{I(IN)}$ | Input voltage range(2) | | –0.3 to 6 | V |
| $V_{O(OUTx)}$ | Output voltage range(2) | | –0.3 to $V_{I(IN)}$ + 0.3 | V |
| $V_{I(\overline{ENx})}$ or $V_{I(ENx)}$ | Input voltage range | | –0.3 to 6 | V |
| $I_{O(OUTx)}$ | Continuous output current | | Internally Limited | |
| | Continuous total power dissipation | | See Dissipation Rating Table | |
| $T_J$ | Operating virtual junction temperature range | | 0 to 125 | °C |
| $T_{stg}$ | Storage temperature range | | –65 to 150 | °C |
| ESD | Electrostatic discharge protection | Human body model | 2 | kV |
| | | Machine model | 200 | V |
| | | Charged device model (CDM) | 750 | V |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND.

## DISSIPATION RATINGS TABLE

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING= |
|---|---|---|---|---|
| D-8 | 725 mW | 5.8 mW/°C | 464 mW | 377 mW |
| D-16 | 1123 mW | 9 mW/°C | 719 mW | 584 mW |

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{I(IN)}$ | Input voltage | 2.7 | 5.5 | V |
| $V_{I(\overline{ENx})}$ or $V_{I(ENx)}$ | Input voltage | 0 | 5.5 | V |
| $I_O$ | Continuous output current (per switch) | 0 | 250 | mA |
| $T_J$ | Operating virtual junction temperature | 0 | 125 | °C |

## ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, $I_O$ = rated current, $V_{I(\overline{ENx})}$ = 0 V, $V_{I(ENx)} = V_{I(INx)}$ (unless otherwise noted)

| SUPPLY CURRENT | | | | | | | |
|---|---|---|---|---|---|---|---|
| PARAMETER | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
| Supply current, low-level output | No Load on OUT | $V_{I(\overline{ENx})} = V_{I(IN)}$, $V_{I(ENx)} = 0$ V | $T_J$ = 25°C | | 0.025 | 1 | µA |
| | | | –40°C ≤ $T_J$ ≤ 125°C | | | 10 | |
| Supply current, high-level output | No Load on OUT | $V_{I(\overline{ENx})}$ = 0 V, $V_{I(ENx)} = V_{I(IN)}$ | $T_J$ = 25°C | | 85 | 110 | µA |
| | | | –40°C ≤ $T_J$ ≤ 125°C | | 100 | | |
| Leakage current | OUT connected to ground | $V_{I(\overline{ENx})} = V_{I(IN)}$, $V_{I(ENx)} = 0$ V | –40°C ≤ $T_J$ ≤ 125°C | | 100 | | µA |
| Reverse leakage current | INx = high impedance | $V_{I(\overline{ENx})}$ = 0 V, $V_{I(ENx)} = V_{I(IN)}$ | $T_J$ = 25°C | | 0.3 | | µA |

Copyright © 2000–2007, Texas Instruments Incorporated

## ELECTRICAL CHARACTERISTICS (Continued)

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, $I_O$ = rated current, $V_{I(\overline{ENx})}$ = 0 V, $V_{I(ENx)}$ = $V_{I(INx)}$ (unless otherwise noted)

| POWER SWITCH | | | | | | | |
|---|---|---|---|---|---|---|---|
| PARAMETER | | TEST CONDITIONS(1) | | | MIN | TYP | MAX | UNIT |
| $r_{DS(on)}$ | Static drain-source on-state resistance | $V_{I(IN)}$ = 5 V, | $T_J$ = 25°C, | $I_O$ = 0.25 A | | 80 | 100 | mΩ |
| | | $V_{I(IN)}$ = 5 V, | $T_J$ = 85°C, | $I_O$ = 0.25 A | | 90 | 120 | |
| | | $V_{I(IN)}$ = 5 V, | $T_J$ = 125°C, | $I_O$ = 0.25 A | | 100 | 135 | |
| | | $V_{I(IN)}$ = 3.3 V, | $T_J$ = 25°C, | $I_O$ = 0.25 A | | 90 | 125 | |
| | | $V_{I(IN)}$ = 3.3 V, | $T_J$ = 85°C, | $I_O$ = 0.25 A | | 110 | 145 | |
| | | $V_{I(IN)}$ = 3.3 V, | $T_J$ = 125°C, | $I_O$ = 0.25 A | | 120 | 165 | |
| $t_r$ | Rise time, output | $V_{I(IN)}$ = 5.5 V, $R_L$ = 20 Ω, | $T_J$ = 125°C, | $C_L$ = 1 µF | | 2.5 | | ms |
| | | $V_{I(IN)}$ = 2.7 V, $R_L$ = 20 Ω, | $T_J$ = 125°C, | $C_L$ = 1 µF | | 3 | | |
| $t_f$ | Fall time, output | $V_{I(IN)}$ = 5.5 V, $R_L$ = 20 Ω, | $T_J$ = 125°C, | $C_L$ = 1 µF | | 4.4 | | ms |
| | | $V_{I(IN)}$ = 2.7 V, $R_L$ = 20 Ω, | $T_J$ = 125°C, | $C_L$ = 1 µF | | 2.5 | | |

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

| ENABLE INPUT $V_{I(\overline{ENx})}$ or $V_{I(ENx)}$ | | | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| $V_{IH}$ | High-level input voltage | 2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | 4.5 V ≤ $V_{I(IN)}$ ≤ 5.5 V | | | 0.8 | V |
| | | 2.7 V ≤ $V_{I(IN)}$ ≤ 4.5 V | | | 0.4 | |
| $I_I$ | Input current | $V_{I(\overline{ENx})}$ = 0 V and $V_{I(ENx)}$ = $V_{I(IN)}$, or $V_{I(\overline{ENx})}$ = $V_{I(IN)}$ and $V_{I(ENx)}$ = 0 V | –0.5 | | 0.5 | µA |
| $t_{on}$ | Turnon time | $C_L$ = 100 µF, $R_L$ = 20 µF | | | 20 | ms |
| $t_{off}$ | Turnon time | $C_L$ = 100 µF, $R_L$ = 20 µF | | | 40 | ms |

| CURRENT LIMIT | | | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | | TEST CONDITIONS(1) | MIN | TYP | MAX | UNIT |
| $I_{OS}$ | Short-circuit output current | $V_{I(IN)}$ = 5 V, OUT connected to GND, Device enabled into short circuit | 0.3 | 0.5 | 0.7 | A |

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

| UNDERVOLTAGE LOCKOUT | | | | | |
|---|---|---|---|---|---|
| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| Low-level input voltage | | 2 | | 2.5 | V |
| Hysteresis | $T_J$ = 25°C | | 100 | | mV |

| OVERCURRENT $\overline{OCx}$ | | | | | |
|---|---|---|---|---|---|
| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| Sink current(1) | $V_O$ = 5 V | | | 10 | mA |
| Output low voltage | $I_O$ = 5 mA, $V_{OL(\overline{OCx})}$ | | | 0.5 | V |
| Off-state current(1) | $V_O$ = 5 V, $V_O$ = 3.3 V | | | 1 | µA |

(1) Specified by design, not production tested.


Copyright © 2000–2007, Texas Instruments Incorporated

## PARAMETER MEASUREMENT INFORMATION

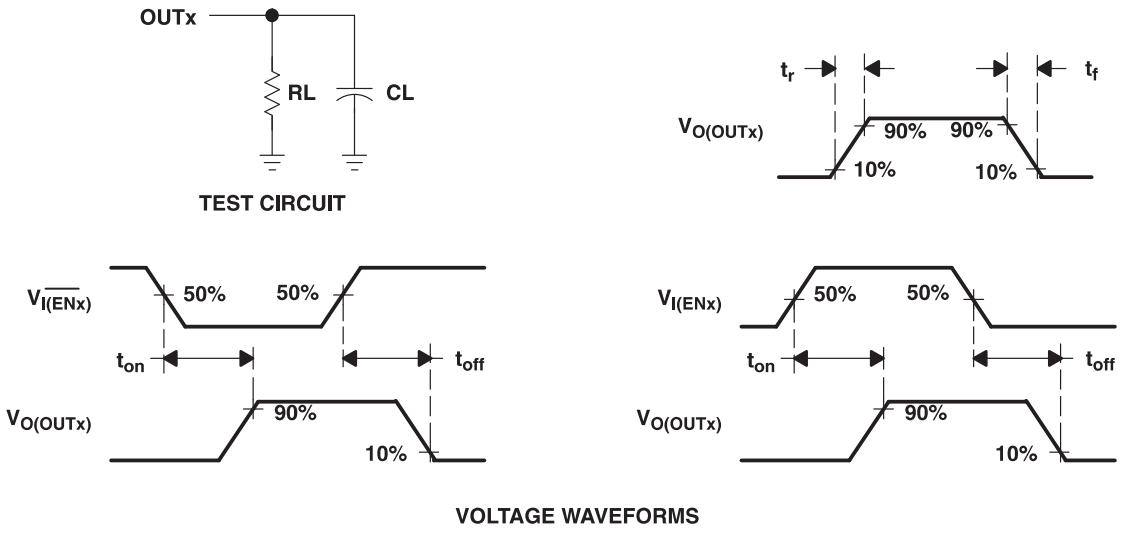



**Figure 1. Test Circuit and Voltage Waveforms**

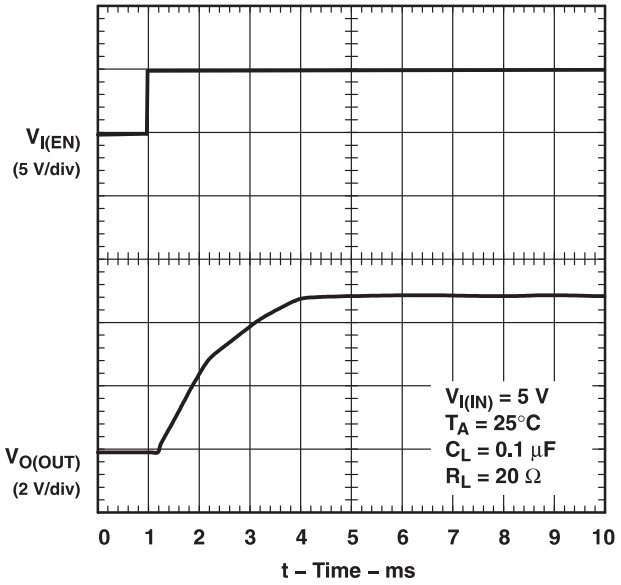



**Figure 2. Turnon Delay and Rise Time With 0.1-µF Load**

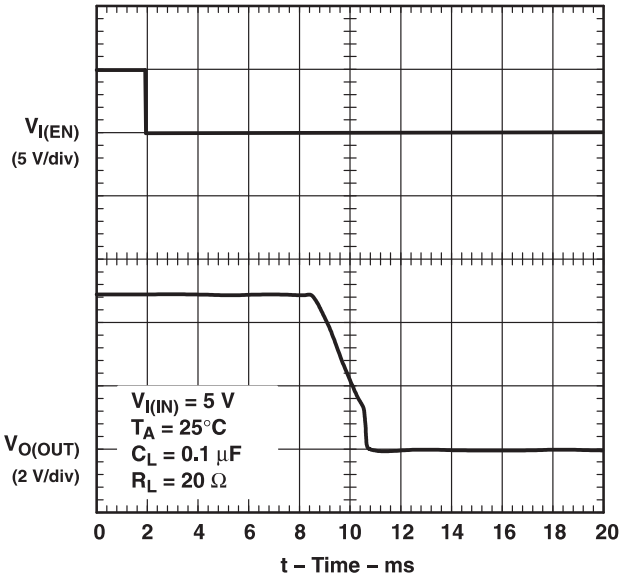



**Figure 3. Turnoff Delay and Fall Time With 0.1-µF Load**

Copyright © 2000–2007, Texas Instruments Incorporated

## PARAMETER MEASUREMENT INFORMATION (continued)

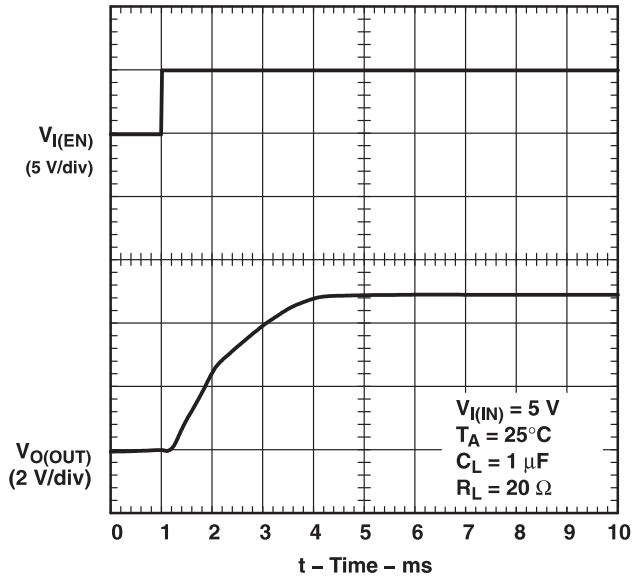



Figure 4. Turnon Delay and Rise Time With 1-μF Load

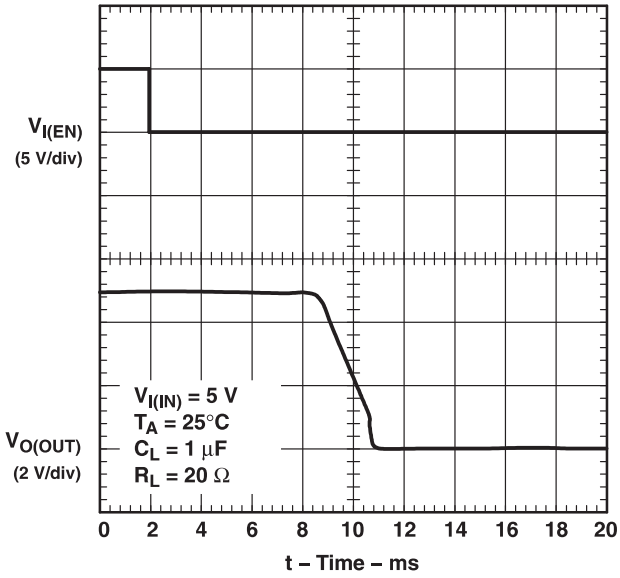



Figure 5. Turnoff Delay and Fall Time With 1-μF Load

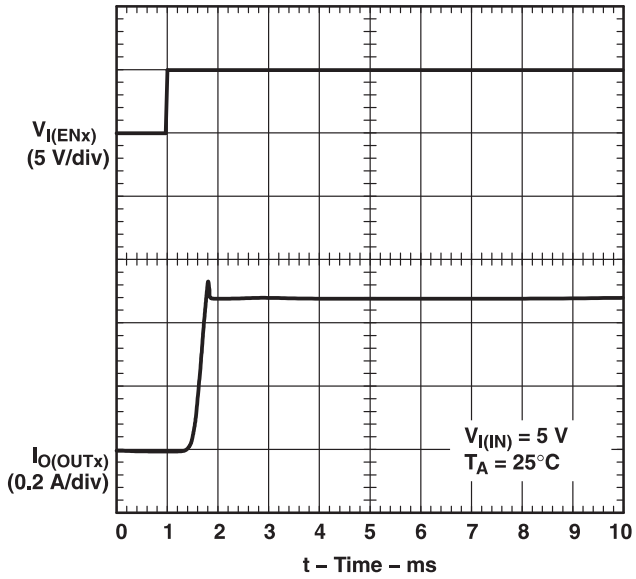



Figure 6. TPS2090, Short-Circuit Current, Device Enabled Into Short

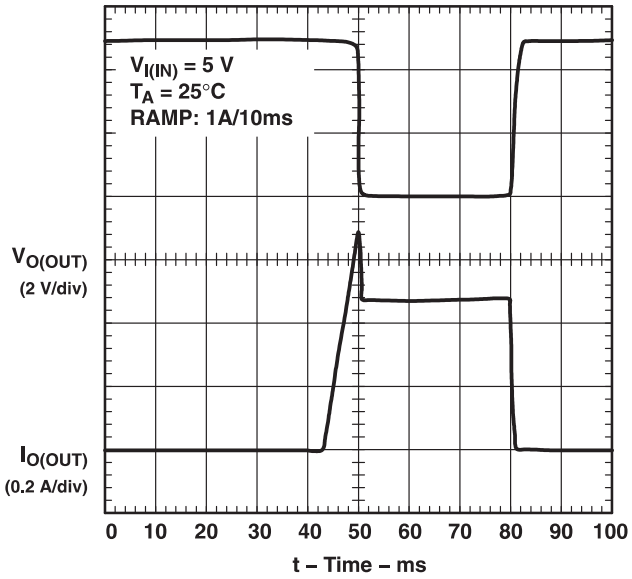



Figure 7. TPS2090, Threshold Trip Current With Ramped Load on Enabled Device


Copyright © 2000–2007, Texas Instruments Incorporated

## PARAMETER MEASUREMENT INFORMATION (continued)

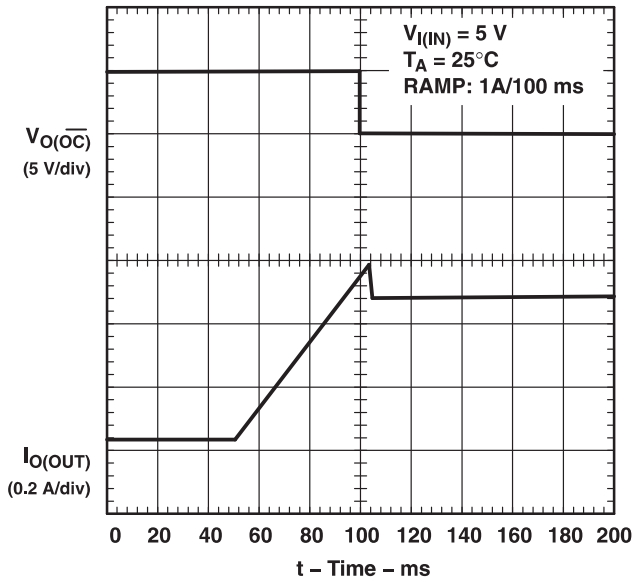



Figure 8. Ramped Load on Enabled Device

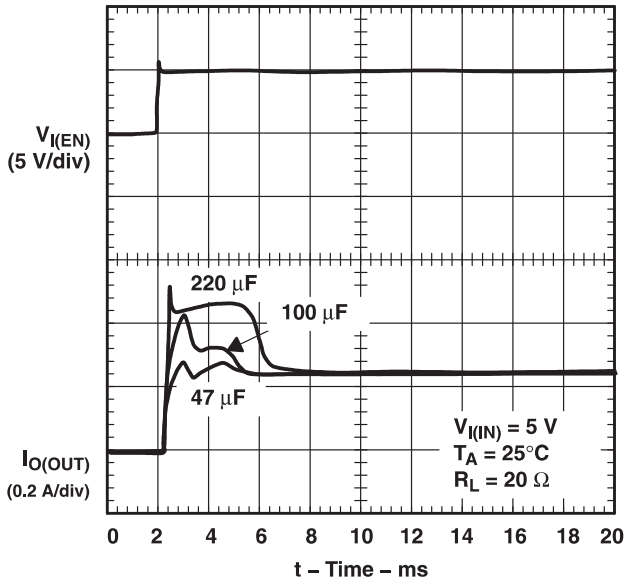



Figure 9. Inrush Current With 47-µF, 100-µF and 220-µF Load Capacitance

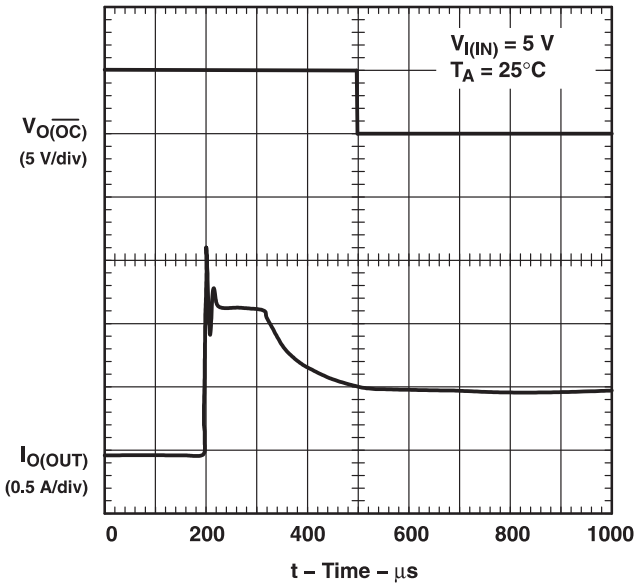



Figure 10. 4-Ω Load Connected to Enabled Device

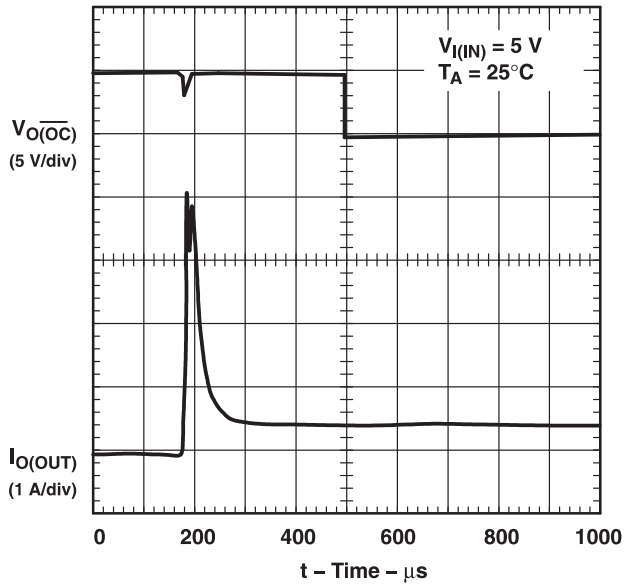



Figure 11. 1-Ω Load Connected to Enabled Device

Copyright © 2000–2007, Texas Instruments Incorporated

## TYPICAL CHARACTERISTICS

TURNON DELAY TIME
vs
INPUT VOLTAGE

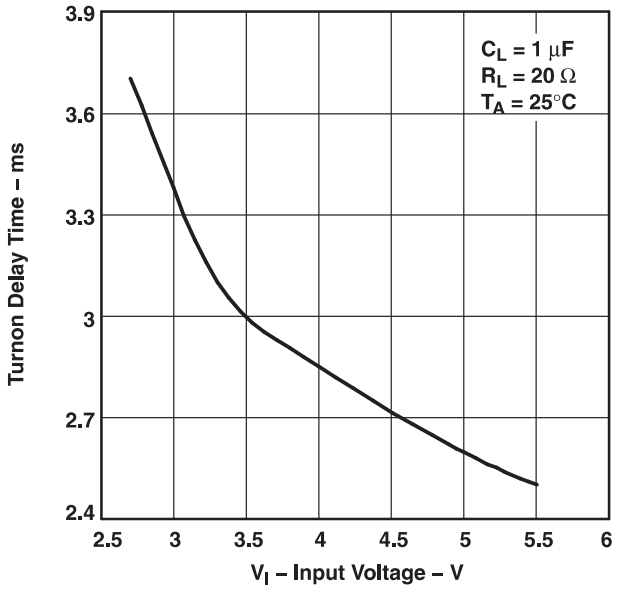



Figure 12.

TURNOFF DELAY TIME
vs
INPUT VOLTAGE

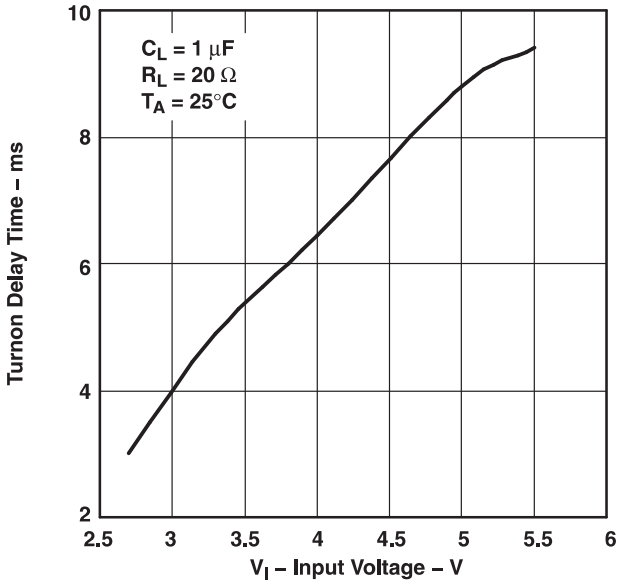



Figure 13.

RISE TIME
vs
INPUT VOLTAGE

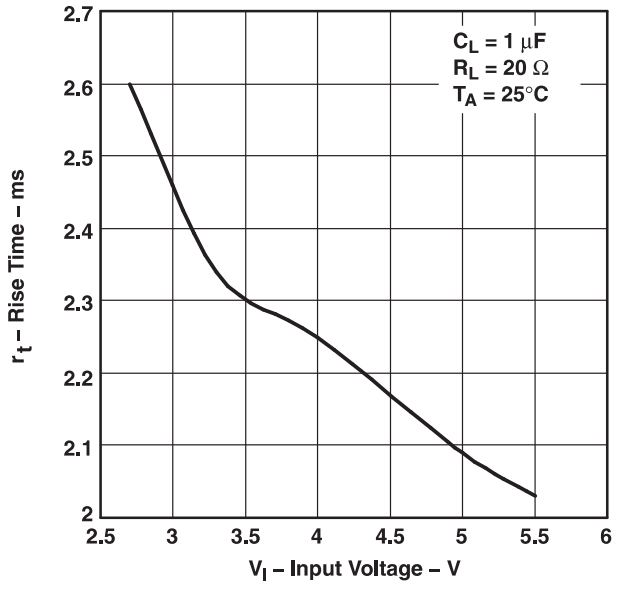



Figure 14.

FALL TIME
vs
INPUT VOLTAGE

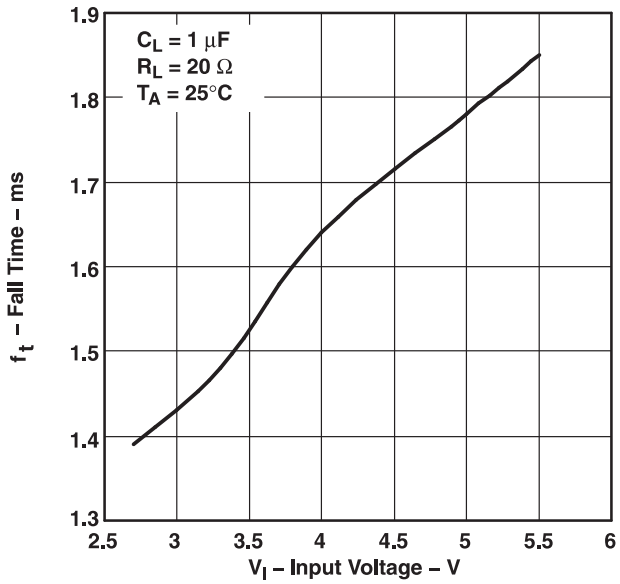



Figure 15.


Copyright © 2000–2007, Texas Instruments Incorporated

## TYPICAL CHARACTERISTICS (continued)

SUPPLY CURRENT, OUTPUT ENABLED
vs
JUNCTION TEMPERATURE

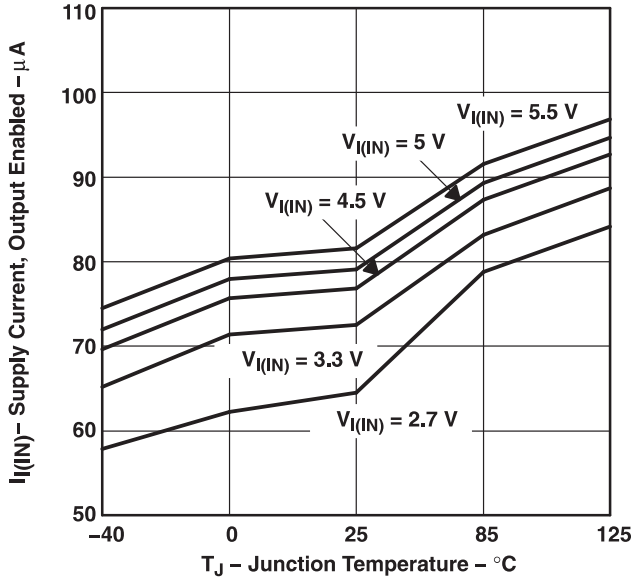



Figure 16.

SUPPLY CURRENT, OUTPUT DISABLED
vs
JUNCTION TEMPERATURE

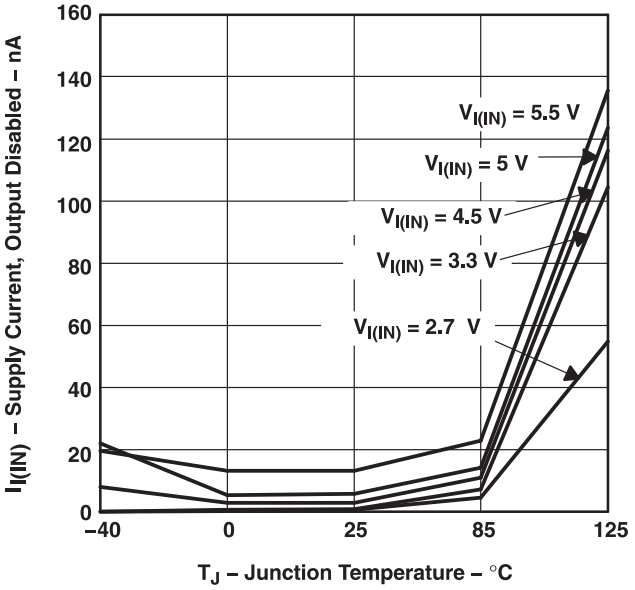



Figure 17.

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

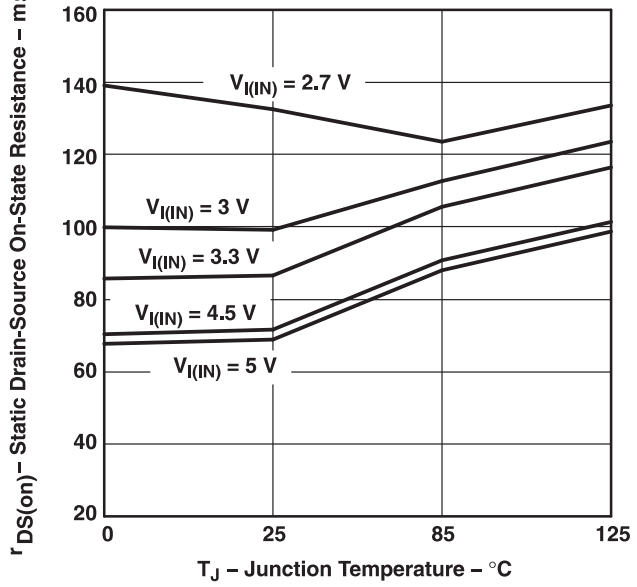



Figure 18.

INPUT-TO-OUTPUT VOLTAGE
vs
LOAD CURRENT

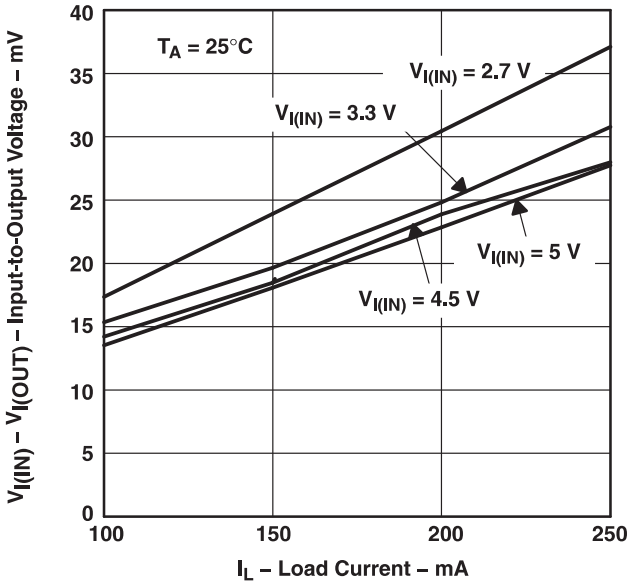



Figure 19.

Copyright © 2000–2007, Texas Instruments Incorporated

## TYPICAL CHARACTERISTICS (continued)

**SHORT-CIRCUIT OUTPUT CURRENT vs JUNCTION TEMPERATURE**

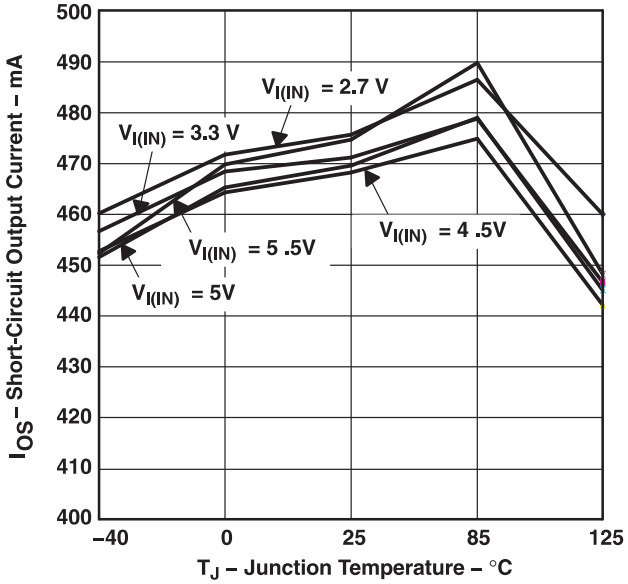



Figure 20.

**THRESHOLD TRIP CURRENT vs INPUT VOLTAGE**

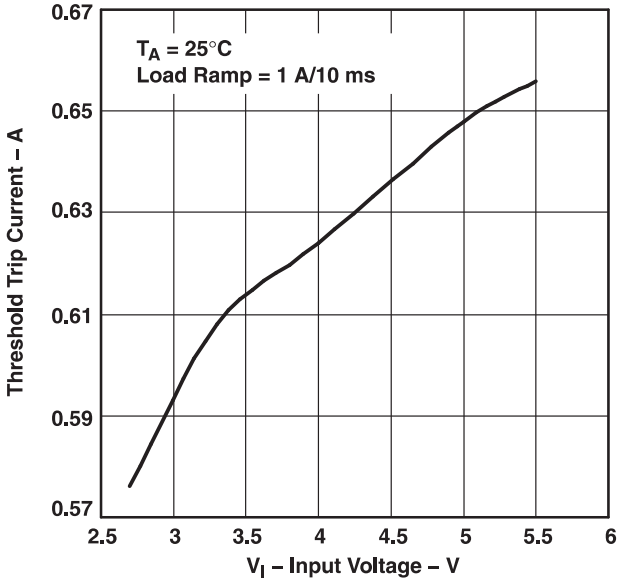



Figure 21.

**UNDERVOLTAGE LOCKOUT vs JUNCTION TEMPERATURE**

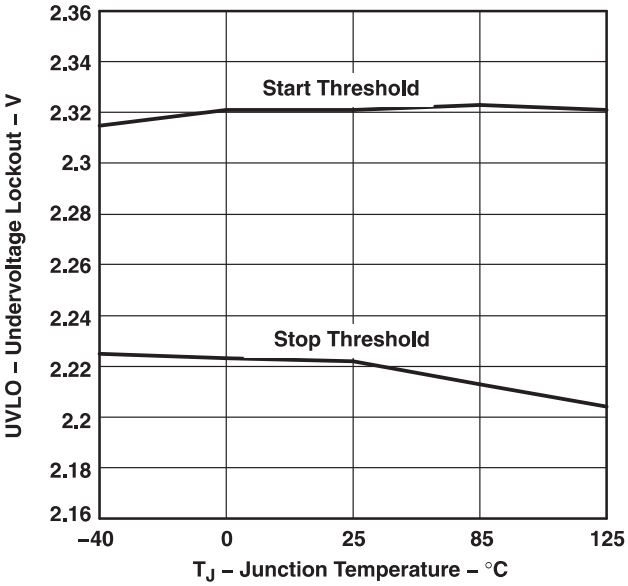



Figure 22.

**CURRENT LIMIT RESPONSE vs PEAK CURRENT**

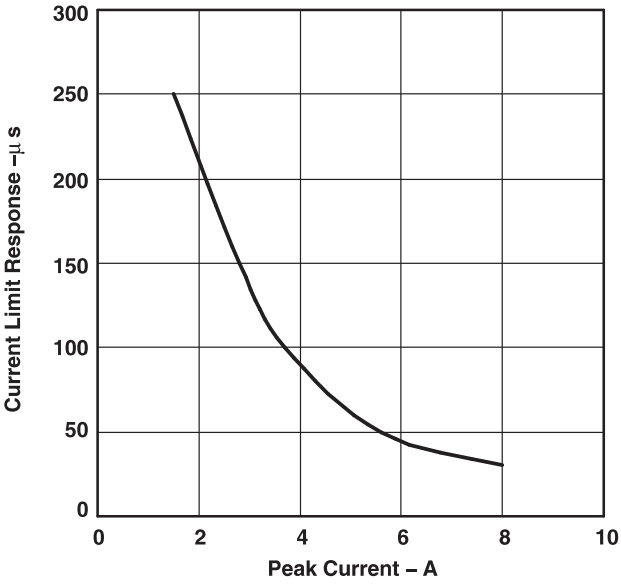



Figure 23.


Copyright © 2000–2007, Texas Instruments Incorporated

## APPLICATION INFORMATION

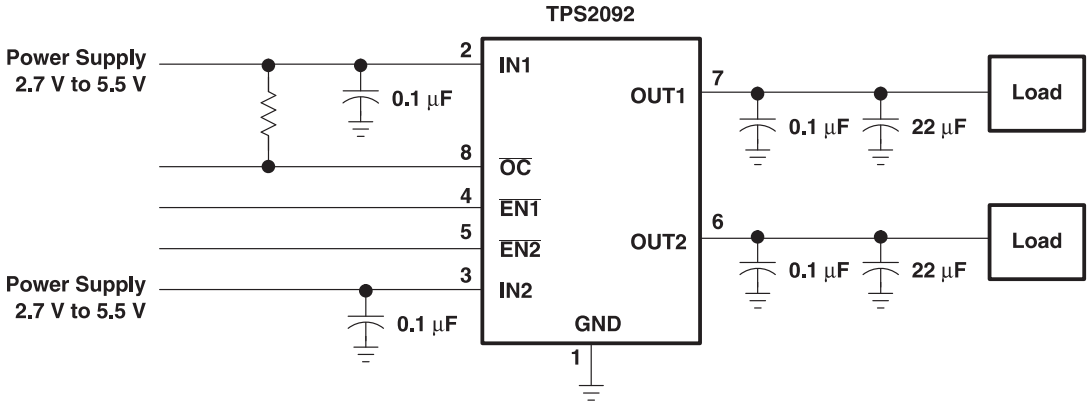



**Figure 24. Typical Application**

## POWER-SUPPLY CONSIDERATIONS

A 0.01-µF to 0.1-µF ceramic bypass capacitor between INx and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-µF to 0.1-µF ceramic capacitor improves the immunity of the device to short-circuit transients.

## OVERCURRENT

A sense FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 6). The TPS209x senses the short and immediately switches into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, very high currents may flow for a short time before the current-limit circuit can react (see Figure 10 and Figure 11). After the current-limit circuit has tripped (reached the overcurrent trip threshold) the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figure 8). The TPS209x is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

## $\overline{\text{OC}}$ RESPONSES

The $\overline{\text{OC}}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false overcurrent reporting from the inrush current flowing through the device, charging the downstream capacitor. The TPS209x devices are designed to reduce false overcurrent reporting. An internal overcurrent transient filter eliminates the need to use external components to remove unwanted pulses. Using low-ESR electrolytic capacitors on the output lowers the inrush current flow through the device during hot-plug events by providing a low impedance energy source, thereby reducing erroneous overcurrent reporting.

Copyright © 2000–2007, Texas Instruments Incorporated

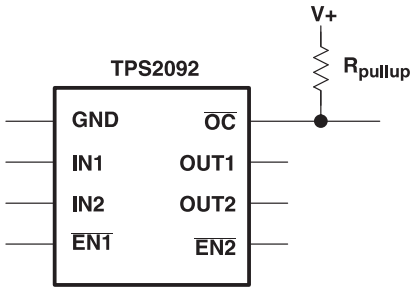



**Figure 25. Typical Circuit for $\overline{OC}$ Pin**

## POWER DISSIPATION AND JUNCTION TEMPERATURE

The low on-resistance on the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistances of these packages are high compared to that of power packages; it is good design practice to check power dissipation and junction temperature. Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figure 18. Using this value, the power dissipation per switch can be calculated by:

$$P_D = r_{DS(on)} \times I^2$$

Multiply this number by the total number of switches being used, to get the total power dissipation coming from the N-channel MOSFETs.

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

$T_A$ = Ambient Temperature °C

$R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W (for 8 pin), 111°C/W (for 16 pin)

$P_D$ = Total power dissipation based on number of switches being used.

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

## THERMAL PROTECTION

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS209x into constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels. The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

The TPS209x implements a dual thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition the junction temperature will rise. Once the die temperature rises to approximately 140°C, the internal thermal sense circuitry checks which power switch is in an overcurrent condition and turns that power switch off, thus isolating the fault without interrupting operation of the adjacent power switch. Should the die temperature exceed the first thermal trip point of 140°C and reach 160°C, both switches turn off. The $\overline{OC}$ open-drain output is asserted (active low) when overtemperature or overcurrent occurs.


Copyright © 2000–2007, Texas Instruments Incorporated

## UNDERVOLTAGE LOCKOUT (UVLO)I

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch will be quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO will also keep the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. Upon reinsertion, the power switch will be turned on with a controlled rise time to reduce EMI and voltage overshoots.

## GENERIC HOT-PLUG APPLICATIONS (see Figure 26)

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS209x, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS209x also ensures the switch will be off after the card has been removed, and the switch will be off during the next insertion. The UVLO feature insures a soft start with a controlled rise time for every insertion of the card or module.

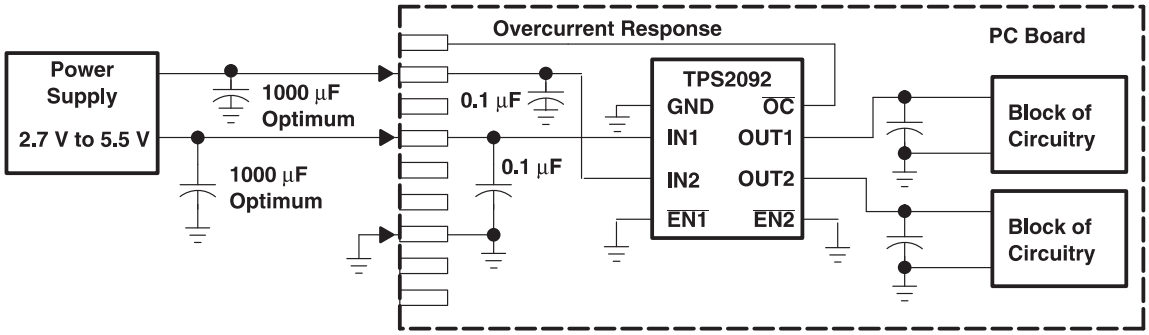



**Figure 26. Typical Hot-Plug Implementation**

By placing the TPS209x between the $V_{CC}$ input and the rest of the circuitry, the input power will reach these devices first after insertion. The typical rise time of the switch is approximately 2.5 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

Copyright © 2000–2007, Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS2090D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 85 | 2090 | Samples |
| TPS2090DG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 85 | 2090 | Samples |
| TPS2090DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 85 | 2090 | Samples |
| TPS2091D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 85 | 2091 | Samples |
| TPS2091DG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 85 | 2091 | Samples |
| TPS2092D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 85 | 2092 | Samples |
| TPS2092DG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 85 | 2092 | Samples |
| TPS2092DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 85 | 2092 | Samples |
| TPS2095D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 85 | 2095 | Samples |
| TPS2095DG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 85 | 2095 | Samples |
| TPS2095DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 85 | 2095 | Samples |
| TPS2096D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 85 | 2096 | Samples |
| TPS2096DG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 85 | 2096 | Samples |
| TPS2097D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 85 | 2097 | Samples |
| TPS2097DG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 85 | 2097 | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

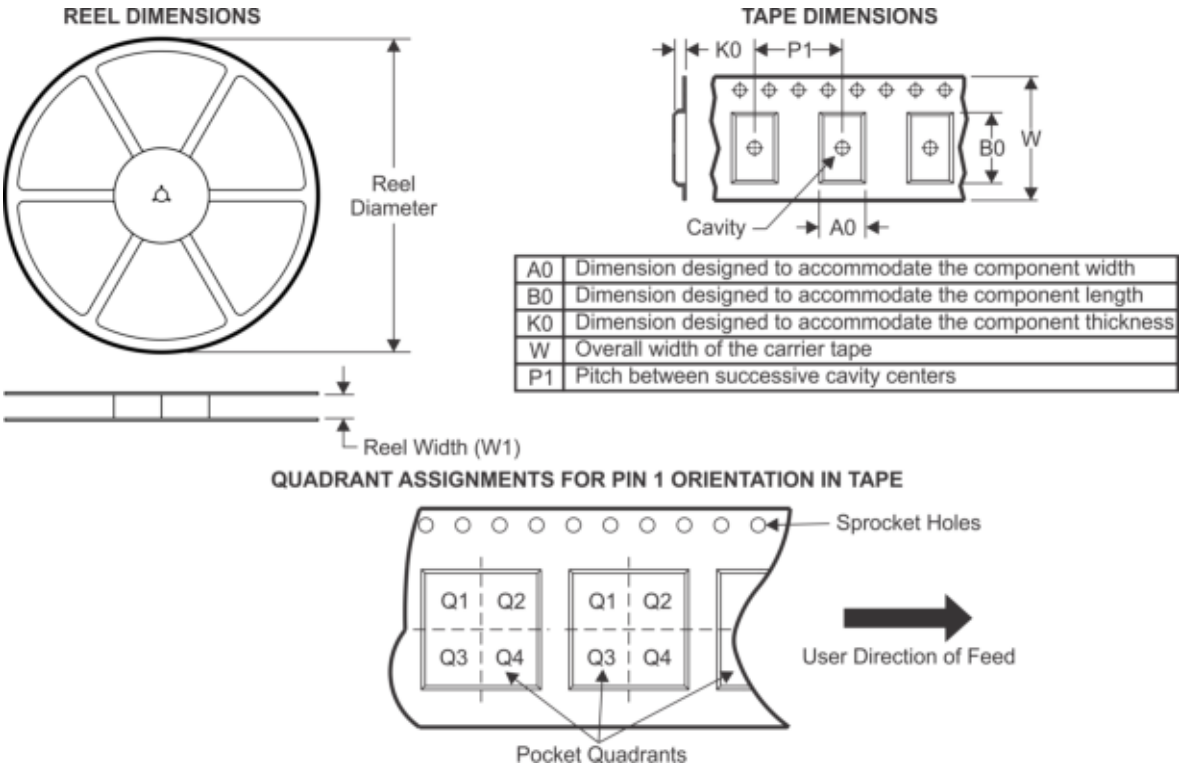
**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

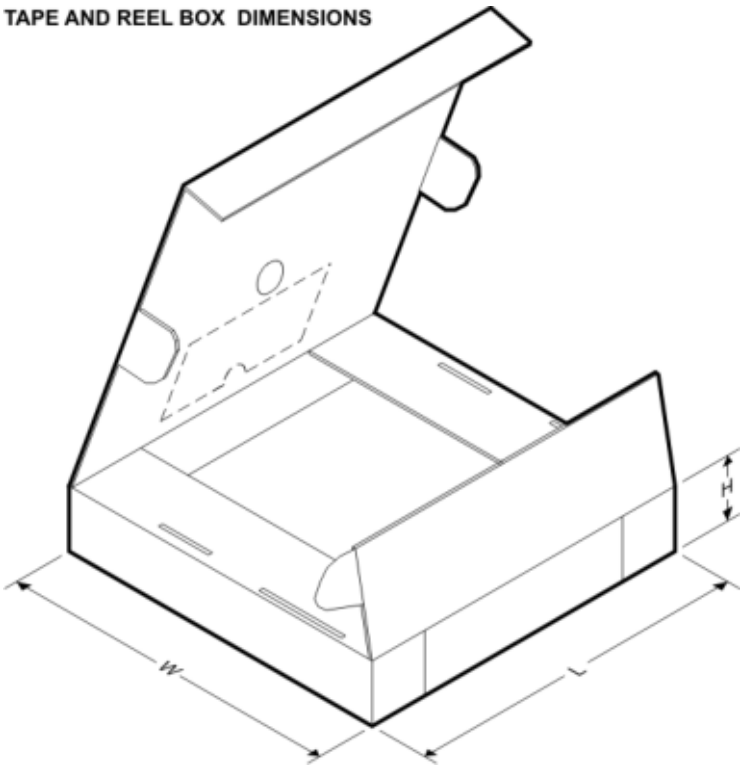



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS2090DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS2092DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS2095DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

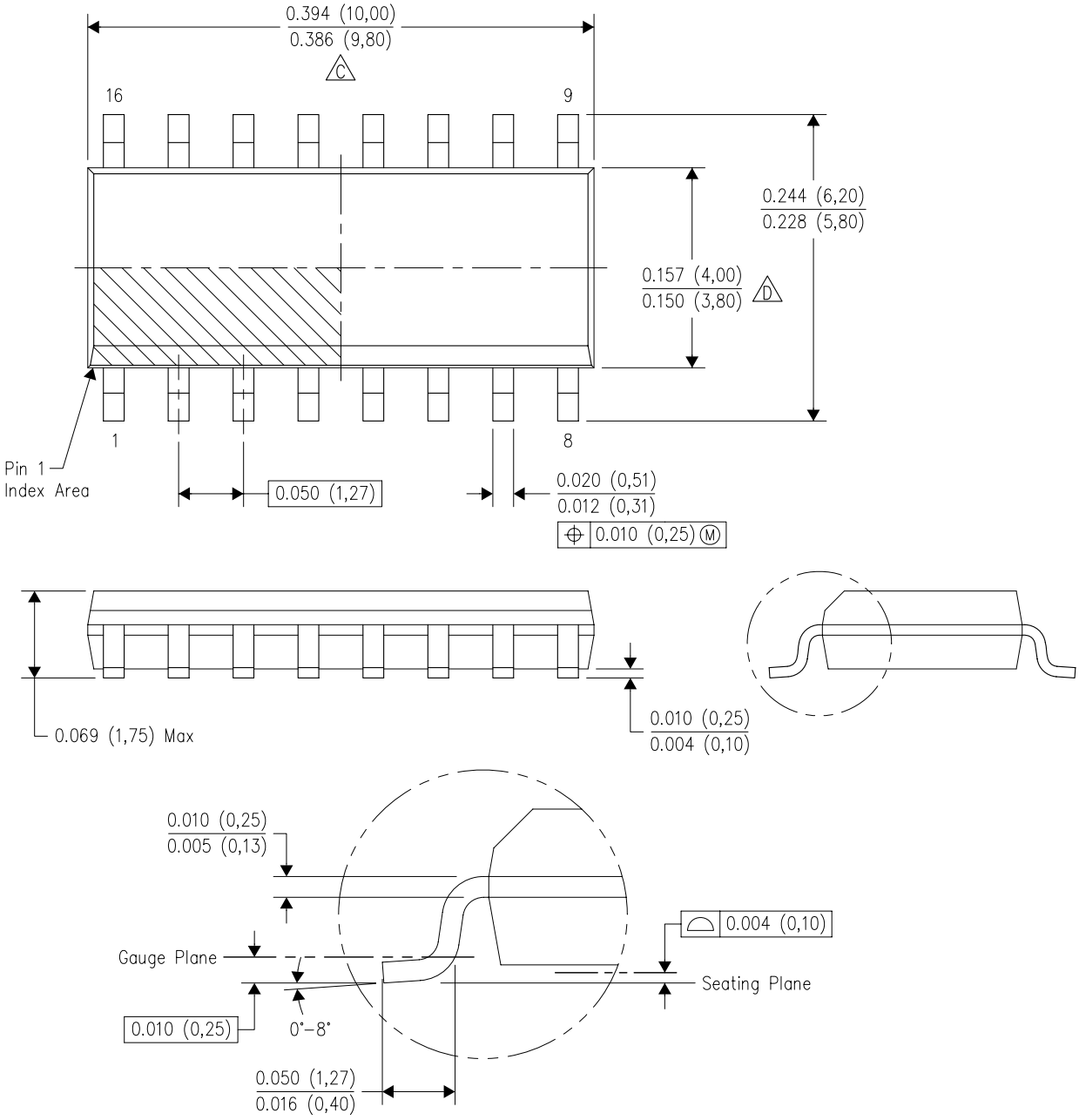
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

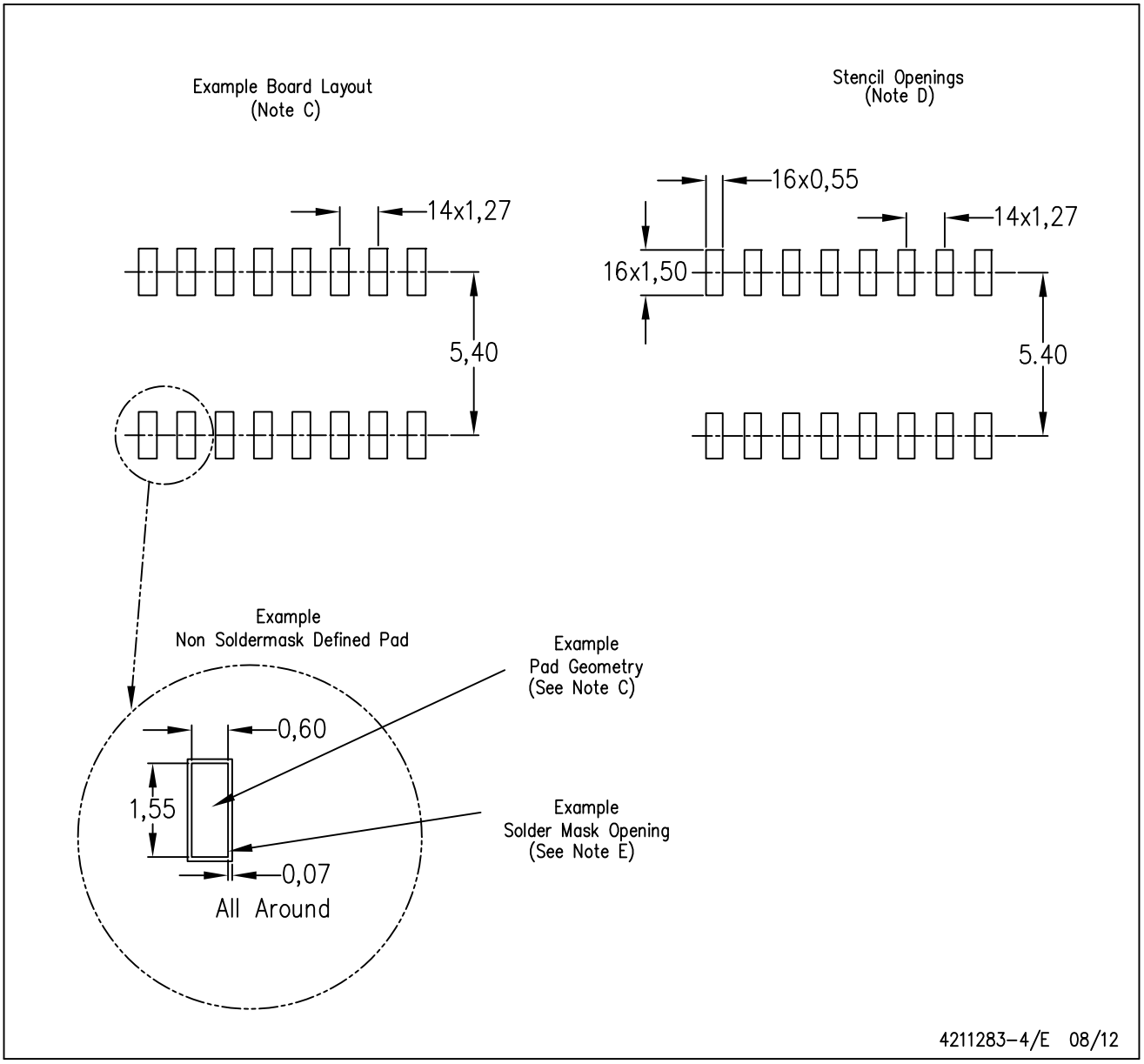
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS2090DR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TPS2092DR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TPS2095DR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



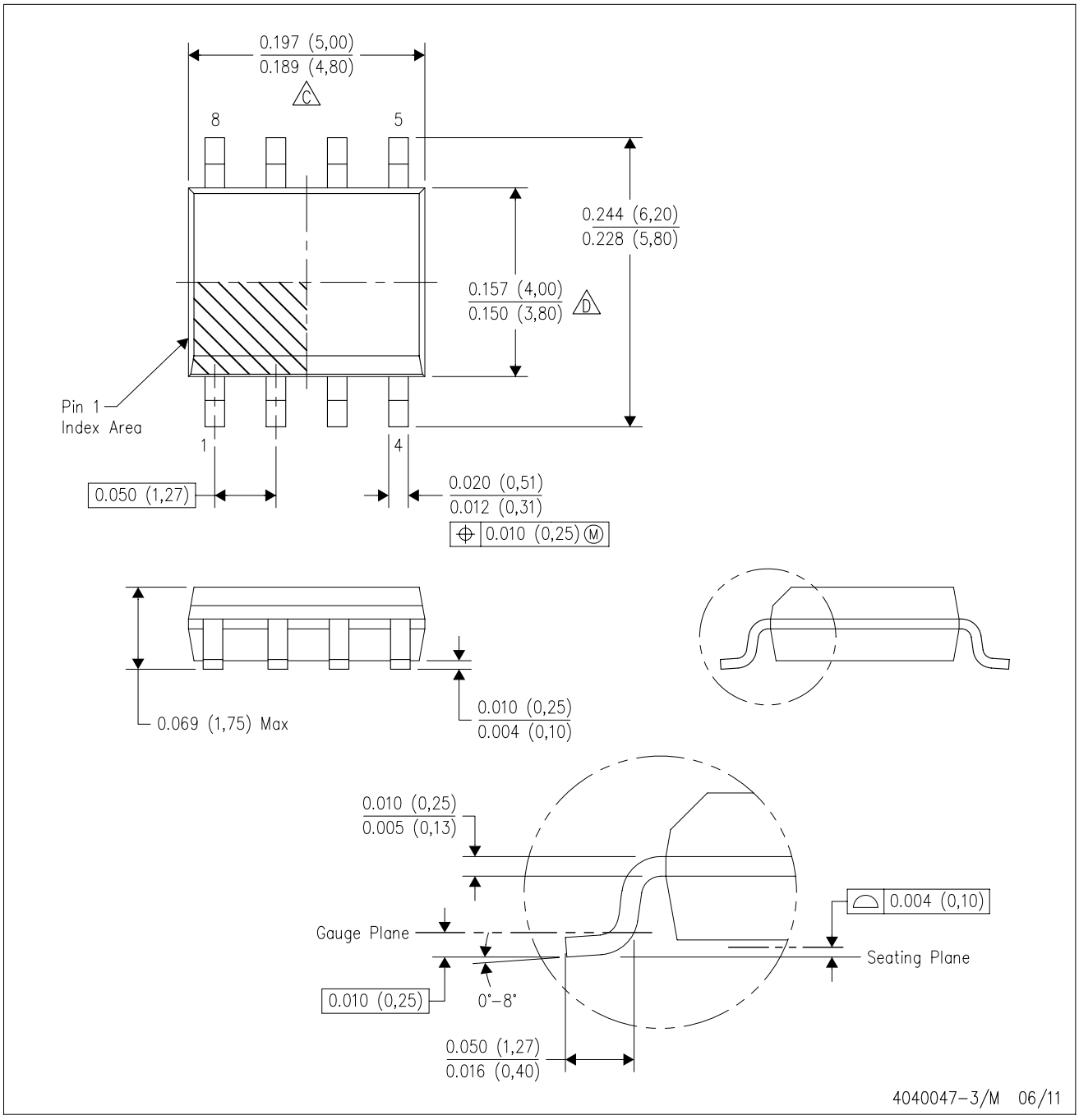

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



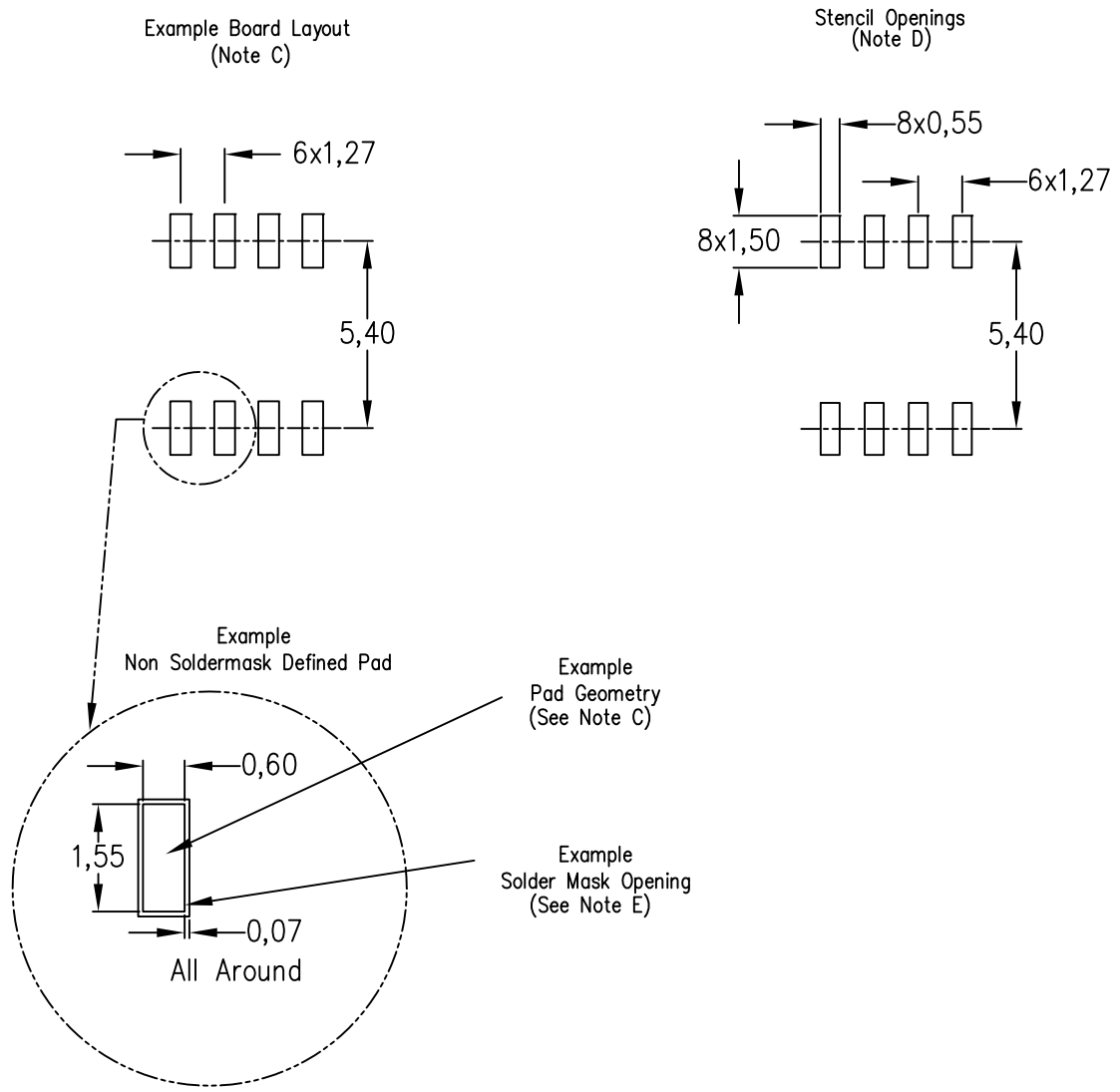

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

| **Products** | | **Applications** | |
|---|---|---|---|
| Audio | www.ti.com/audio | Automotive and Transportation | www.ti.com/automotive |
| Amplifiers | amplifier.ti.com | Communications and Telecom | www.ti.com/communications |
| Data Converters | dataconverter.ti.com | Computers and Peripherals | www.ti.com/computers |
| DLP® Products | www.dlp.com | Consumer Electronics | www.ti.com/consumer-apps |
| DSP | dsp.ti.com | Energy and Lighting | www.ti.com/energy |
| Clocks and Timers | www.ti.com/clocks | Industrial | www.ti.com/industrial |
| Interface | interface.ti.com | Medical | www.ti.com/medical |
| Logic | logic.ti.com | Security | www.ti.com/security |
| Power Mgmt | power.ti.com | Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Microcontrollers | microcontroller.ti.com | Video and Imaging | www.ti.com/video |
| RFID | www.ti-rfid.com | | |
| OMAP Applications Processors | www.ti.com/omap | **TI E2E Community** | e2e.ti.com |
| Wireless Connectivity | www.ti.com/wirelessconnectivity | | |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2016, Texas Instruments Incorporated