

SLUS572F − OCTOBER, 2003 − REVISED JANUARY 2007

DUAL SLOT PCI-X 2.0 HOT PLUG POWER CONTROLLER

FEATURES

- **Supports PCI, PCI−X 1.0 and PCI−X 2.0**
- **Internal Power Switches for –12 V, 12 V, 3.3 V Aux**
- **Control for External Power Switches for 5 V, 3.3 V, and V_{IO}**
- **Overload Protection on All Supplies**
- **Input Under-Voltage Protection for 3.3 V, 5 V, 12 V and V_{AUX} Supplies**
- **Soft Start to Minimize Inrush Current**
- **Programmable Slew Rate for 3.3 V, 5 V, 12 V, V_{IO} and V_{AUX} Supplies**
- **Multi-Slot or Single-Slot Serial Operating Mode**
- **Direct Operating Mode**
- **V_{IO} Selection Based on Card Type**
- **80-Lead PowerPad™ TQFP Package**

APPLICATIONS

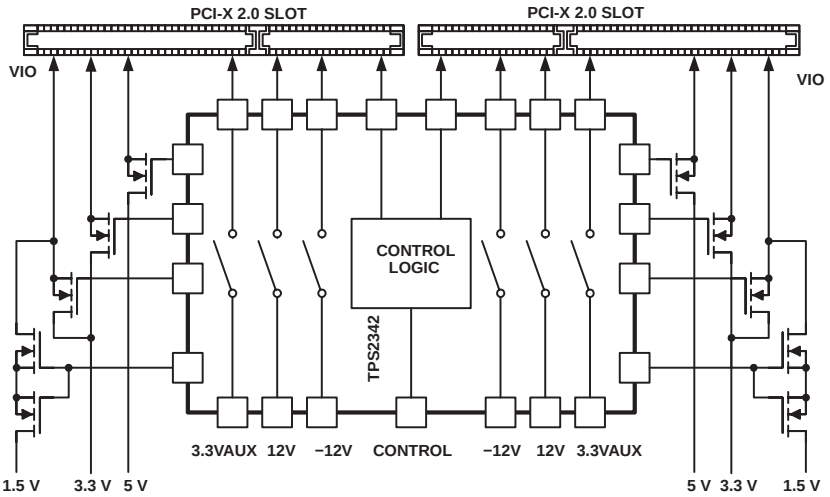
- **Hot Plug Slots in Servers**

DESCRIPTION

The TPS2342 contains main supply power control, auxiliary supply power control, power FETs for 12-V, −12-V and auxiliary 3.3-V supplies, V_{IO} control, and digital control of slots. Each TPS2342 contains supply control and switching for two slots. The TPS2342 supports both serial and direct communication to the slots.

The main power control circuits start with all supplies off and all outputs are held off until all power supplies to the TPS2342 are valid. When power is requested via the serial interface or by direct control, the control circuit applies constant current to the gates of the power FETs, allowing each FET to ramp load voltage linearly. Each supply can be programmed for a desired ramp rate by selecting the appropriate gate capacitor. The power control circuits monitor load current and latch off that slot if the load current exceeds a programmed maximum value. Once the 12-V, the 5-V, and the 3.3-V FETs are fully enhanced, the load voltage is monitored. If the load voltage drops out of specification after these FETs are fully enhanced, the slot latches off.

SIMPLIFIED APPLICATION DIAGRAM



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DESCRIPTION (CONT.)

The auxiliary power control circuit switches, ramps, and monitors 3.3-V auxiliary power to each slot. The auxiliary control circuit controls data switches that connect slot interrupts power management event (PME) outputs to the main interrupt PME bus after 3.3-V auxiliary supply is connected. PME is disconnected when a board is turned off or a fault occurs on the board's auxiliary power.

V_{IO} control consists of gate drivers to select between 3.3 V and 1.5 V in response to command over the interface, as well as a regulator for when the 1.5-V supply is greater than 1.575 V and current limiting circuitry to shut down a slot in the event of over current.

Each TPS2342 contains power FETs for 12 V, −12 V, and auxiliary 3.3 V for each slot. These power FETs are short-circuit protected, slew rate controlled, and over-temperature protected.

The serial interface communicates with a slot controller using a synchronous serial protocol. The interface communicates with the slot, status LEDs, and mechanical switches with individual, dedicated lines. The interface operates from 3.3-V power but inputs are 5-V tolerant. Status LED drivers are capable of driving 24-mA LEDs via integrated open-drain MOSFETs. Mechanical switch inputs have internal pull-up and hysteresis buffers. The serial interface controls slot power, bus connection, LED outputs, and V_{IO} control, and monitors board capability, power fault, and switch input status.

The serial interface operates in one of two modes: multi-slot mode and single-slot mode. In multi-slot mode, the data from two or more slots is cascaded on one serial interface. In single-slot mode, each slot has its own independent serial interface. Single-slot mode is preferred when the bandwidth of the bus is so high that the bridge/controller can only manage one slot per bus.

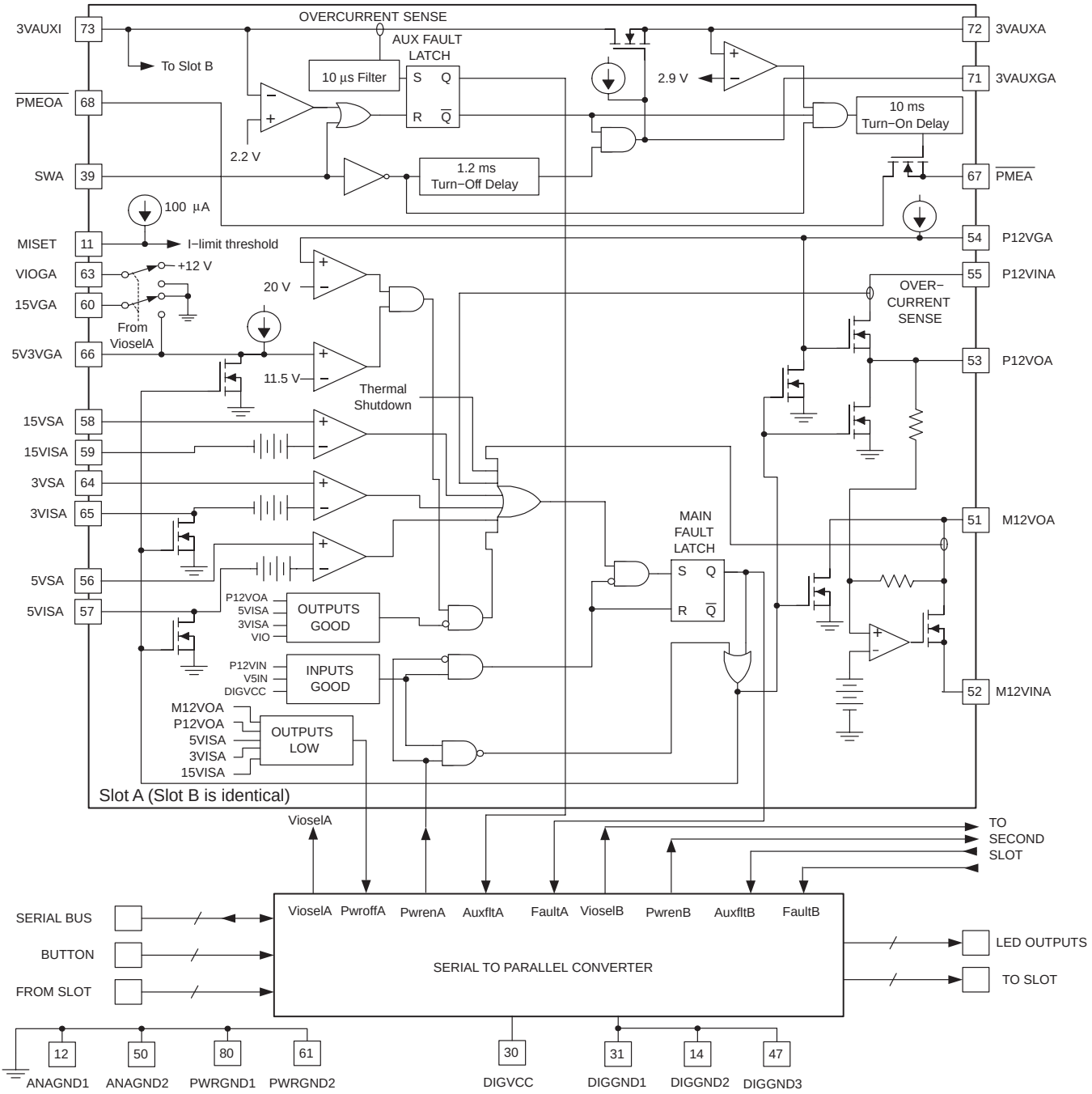
The TPS2342 can be configured for a conventional direct mode to access the slot directly over parallel lines.

ORDERING INFORMATION

T_A	PACKAGE(1)
	HTQFP (PFP)
−40°C to +85°C	TPS2342PFP

(1) Add suffix R to device type (e.g. TPS2342PFPR) to specify taped and reeled.

BLOCK DIAGRAM



In this drawing, circuits related to the VIO function are oversimplified. See the VIO section of the datasheet (pages 43−44) for a more accurate representation of this section.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)†‡

PARAMETER	TPS2342	UNIT
Input voltage range, P12VIN, $\overline{\text{BUTTONA}}$	−0.5 to 15	V
M12VIN	−15.0 to 0.5	
All others	−0.5 to 7	
Output voltage range, P12VO, 5V3VG, 15VG, VIOG	−0.5 to V_{P12VIN} + 0.5	
P12VG	−0.5 to 28	
M12VO	−15 to 0.5	
Output current pulse, P12VO (dc internally limited)	3	A
M12VO	0.8	
3VAUX	2	
Operating junction temperature range, T_J	−40 to 100	°C
Storage temperature range, T_{stg}	−65 to 150	
Lead temperature soldering 1.6 mm (1/16 inch) from case for 10 seconds	260	

† Stresses beyond those listed under ”absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under ”recommended operating conditions” is not implied. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability

‡ All voltages are with respect to DIGGND.

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

TEST METHOD	MIN	UNIT
Human body model (HBM)	2	kV
Charged device model (CDM)	1	kV

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	TYP	MAX	UNIT
Input supply,	M12VINA, M12VINB	−10.8	−12	−13.2	V
	P12VINA, P12VINB	10.8	12	13.2	
	DIGVCC, 3VAUXI	3.0	3.3	3.6	
	V5IN	4.75	5.00	5.25	
Load current,	PWRLEDA, PWRLEDB, ATTLEDA, ATTLEDB	0		24	mA
	P12VOA, P12VOB	0		500	
	M12VOA, M12VOB	0		−100	
	3VAUXA, 3VAUXB	0		375	

THERMAL SHUTDOWN

PARAMETER	TYP	UNIT
Junction temperature shutdown	150	°C
Junction temperature − cooldown restart	140	°C

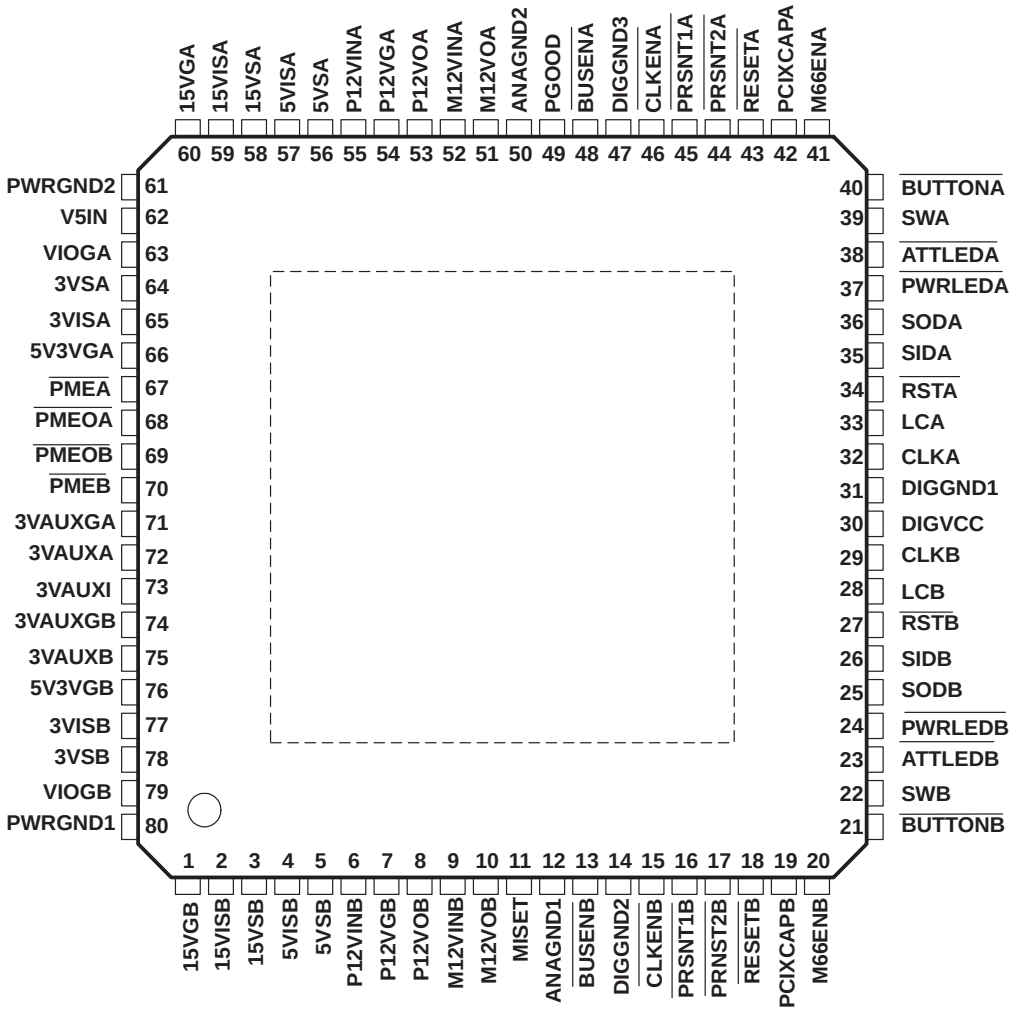
DISSIPATION RATING TABLE

PACKAGE	T_A	THERMAL RESISTANCE JUNCTION TO CASE Θ_{JC}	THERMAL RESISTANCE JUNCTION TO AMBIENT (NOTE 1) Θ_{JA}	THERMAL RESISTANCE JUNCTION TO AMBIENT (NOTE 2) Θ_{JA}
HTQFP−80 (PFP)	−40 °C to 85 °C	1.1 °C/W	19.3 °C/W	29.4 °C/W

Note 1: Thermal resistance measured using an 8-layer PC board following the layout recommendations in TI Publication *PowerPAD Thermally Enhanced Package* Technical Brief SLMA002.
Note 2: Thermal resistance measured using an 8-layer PC board using only top PC board copper to spread the heat.

SERIAL MODE PINOUT

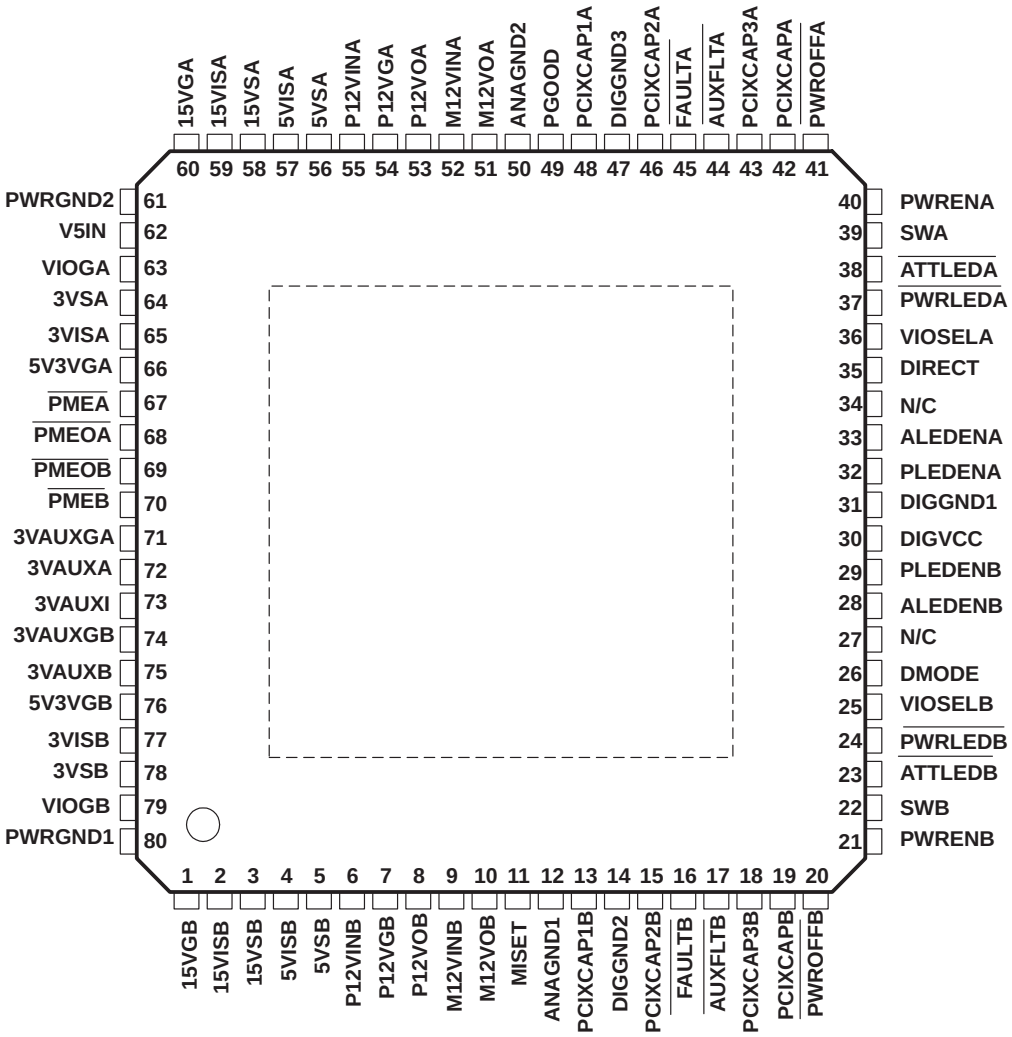
PFP PACKAGE
(TOP VIEW)



The heat-conducting pad on the underside of the package is electrically connected to M12VINA. Either connect the heat-conducting pad to −12 V_{IN} or leave this unconnected. Do not connect the heat-conducting pad to any other power plane or to ground.

DIRECT MODE PINOUT

PFP PACKAGE
(TOP VIEW)



The heat-conducting pad on the underside of the package is electrically connected to M12VINA. Either connect the heat-conducting pad to −12 V_{IN} or leave this unconnected. Do not connect the heat-conducting pad to any other power plane or to ground.

ELECTRICAL CHARACTERISTICS,

P12VIN = 12 V, DIGVCC = 3.3 V, M12VIN = −12 V, 3VAUXI = 3.3 V, V5IN = 5 V, R_{MISET} = 6.04 kΩ, all outputs unloaded, T_A = −40 °C to 85 °C, (unless otherwise noted) (1)(2)(3)

12-V Main Supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
12-V internal switch on resistance	$T_A = T_J$ = 25°C, P12VG > 18 V		0.18	0.30	Ω
	T_A = −40 °C to 85 °C, P12VG > 18 V			0.4	
12-V overcurrent threshold		0.83	1.00	1.17	A
P12VIN start threshold voltage		10.2	10.5	11.2	V
P12VIN stop threshold voltage		9.25	9.8	10.35	
P12VIN supply current, outputs off	PWREN = low		1.4	3	mA
P12VG gate good threshold to enable P12VO fault comparator		17.5	19.0	20.5	V
P12VO fault threshold	After P12VG and 5V3VG good	9.75	10.15	10.45	
P12VG gate charge current	PWREN = high	−5	−12	−20	µA
P12VG gate discharge resistance	0.1 V < V_{P12VG} < 0.5V	1.5	4	15	Ω
Turn-on time	PWREN = high to P12VO = 11.4 V, C_{P12VG} = 22 nF		25	40	ms
	PWREN = high to P12VO = 11.4 V, C_{P12VG} = 0 nF		0.5	2.0	
Turn-off time	PWREN = low to P12VO low comparator trip, C_{P12VG} = 22 nF		1.5	3.5	µs
P12VO bleed current	PWREN = low	8	50		mA
P12VO low comparator threshold	PWREN = low	0.075	0.100	0.150	V
P12VO turn-on slew rate	C_{P12VG} = 0 pF, 10% to 90% measurement	2			V/ms

−12-V Main Supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
−12-V internal switch on-resistance	$T_A = T_J$ = 25°C, steady state		0.50	0.75	Ω
	T_A = −40 °C to 85 °C, steady state			0.9	
−12-V overcurrent threshold		0.15	0.20	0.25	A
M12VIN supply current, outputs off	PWREN = low		2	6	mA
M12VO turn-on slew rate(4)	C_{P12VG} = 22 nF, 10% to 90% measurement	0.30	0.68	1.10	V/ms
Turn-on time	C_{P12VG} = 22 nF, PWREN = high to M12VO = −10.4 V, R_L = 120 Ω	5	20	35	ms
Turn-off time	PWREN = low to M12VO low comparator trip		0.5	2.0	µs
M12VO bleed current	PWREN = low	−8	−20		mA
M12VO low comparator threshold	PWREN = low	−0.075	−0.100	−0.150	V

NOTES: (1). All voltages are with respect to DIGGND unless otherwise stated.
(2) Currents are positive into and negative out of the specified terminal.
(3) When references to lines of individual slots are given without the slot identifier, the statement applies to lines on each slot.
(4) −12-V main supply turn on is controlled by the +12-V main supply turn on, so the –12-V main supply slew rate is a function of C_{P12VG}.

ELECTRICAL CHARACTERISTICS,

P12VIN = 12 V, DIGVCC = 3.3 V, M12VIN = −12 V, 3VAUXI = 3.3 V, V5IN = 5 V, R_{MISET} = 6.04 kΩ, all outputs unloaded, T_A = −40 °C to 85 °C, (unless otherwise noted) (1)(2)(3)

5-V/3.3-V Main Supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
5VS−5VIS overcurrent threshold (5 V)		43	53	63	mV
5VIS voltage fault threshold	After P12VG and 5V3VG good	4.25	4.5	4.65	V
5VS input bias current	PWREN = high	−100		100	μA
5VIS input bias current	PWREN = high	100	250	400	
5VIS bleed current	PWREN = low	8	60		mA
3VS−3VIS overcurrent threshold (3.3 V)		53	63	72	mV
3VIS voltage fault threshold	After P12VG and 5V3VG good	2.5	2.7	2.9	V
3VS input bias current	PWREN = high	−100		100	μA
3VIS input bias current	PWREN = high	100	250	400	
3VIS bleed current	PWREN = low	8	40		mA
5V3VG charge current	PWREN = high, 5V3VG = 5 V	−70	−100	−130	μA
5V3VG discharge resistance	0.1 V < V_{5V3VG} < 0.5 V	1.5	4	15	Ω
5V3VG good threshold		11	11.5	12	V
V5IN supply current			2	6	mA
V5IN start threshold voltage		4.2	4.4	4.6	V
V5IN stop threshold voltage		3.7	4.1	4.4	
DIGVCC supply current			1.2	3	mA
DIGVCC start threshold voltage		2.60	2.80	2.95	V
DIGVCC stop threshold voltage		2.40	2.55	2.80	
5VIS low comparator threshold	PWREN = low	0.075	0.100	0.150	
3VIS low comparator threshold	PWREN = low	0.075	0.100	0.150	

Noise Filter

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output undervoltage sensitivity threshold	12 V, 5 V, 3.3 V	50		200	ns
Output undervoltage sensitivity threshold	V_{IO}	80		250	ns
Output voltage fault captured pulse	12 V, 5 V, 3.3 V	200			ns
Output voltage fault captured pulse	V_{IO}	250			ns
Output undervoltage fault response time, from output falling to FAULT asserting	12 V, 5 V, 3.3 V, Vio			480	ns
Overcurrent sensitivity threshold	12 V, 5 V, 3.3 V, Vio	1.5		5.5	μs
	−12 V	2		10	
Overcurrent fault captured pulse	12 V, 5 V, 3.3 V, Vio	5			
	−12 V	10			
Overcurrent fault response time, from overcurrent to FAULT asserting	12 V, 5 V, 3.3 V, Vio	2.0		6.5	
	−12 V	2.5		12	

NOTES: (1). All voltages are with respect to DIGGND unless otherwise stated.
(2) Currents are positive into and negative out of the specified terminal.
(3) When references to lines of individual slots are given without the slot identifier, the statement applies to lines on each slot.

ELECTRICAL CHARACTERISTICS,

P12VIN = 12 V, DIGVCC = 3.3 V, M12VIN = −12 V, 3VAUXI = 3.3 V, V5IN = 5 V, R_{MISET} = 6.04 kΩ, all outputs unloaded, T_A = −40 °C to 85 °C, (unless otherwise noted) (1)(2)(3)

3.3 VAUX and PME

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
3VAUX overcurrent threshold		0.8	1.1	1.45	A
3VAUXI to 3VAUX switch on resistance	SW = low, 3VAUXG = 10 V		300	400	mΩ
3VAUXI undervoltage threshold	SW = low	1.9	2.2	2.9	V
3VAUXI supply current, $3V_{AUX}$ off	SW = high		1000	2000	µA
3VAUXG turn-on current	SW = low, 3VAUXG = 3.3 V	−3	−5	−7	
3VAUXG turn-off resistance	SW = high, 0.1 V < 3VAUXG < 0.5 V	3	8	30	Ω
3VAUX turn-on time with no gate capacitor	C_{3VAUXG} = 0 pF, 10% to 90% measurement		200	350	µs
3VAUX turn-on slew rate with gate capacitor	C_{3VAUXG} = 27 nF, 10% to 90% measurement	0.11	0.16	0.22	V/ms
3VAUXB bleed current	SW = high, 3VAUXG = 1 V	8	28		mA
3VAUX turn-off time from SW	From SW > 2.0 V to 3VAUX < 0.5 V, C_{3VAUXG} = 27 nF		1.2	5.0	ms
3VAUX turn-off time from Fault	From 3VAUX overcurrent fault		17	25	µs
PME turn-on time from 3VAUX	From 3VAUX > 3.0 V, C_{3VAUX} = 150 µF	6	10	17	ms
PME turn-off time from SW	From SW > 2.0 V			4	µs
PME turn-off time from Fault	From 3VAUX overcurrent fault			4	
PME switch on resistance	SW = low		10	20	Ω
3VAUX output rising threshold to PME switch closed		2.5		3.0	V

V_{IO} Supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
15VG, VIOG output voltage high	$V_{IO(in)}$ = 1.5 V	11.5	11.9		V
15VIS regulation voltage	$V_{IO(in)}$ = 1.8 V	1.450	1.500	1.545	V
15VS – 15VIS overcurrent threshold (1.5 V operation)		20.0	23.5	27.0	mV
15VG, VIOG turn-off resistance	PWREN = low, 0.1 V < V_{15VG}, V_{VIOG} < 0.5 V	10	50	100	Ω
15VS input bias current	PWREN = high, VIOSEL = low, test circuit Figure 7	−100		100	µA
15VIS input bias current	PWREN = high, VIOSEL = low, test circuit Figure 7	−100	150	200	
15VIS bleed current	PWREN = low	8	20		mA
15VIS low comparator threshold	PWREN = low	0.075	0.100	0.150	V
15VIS fault threshold	After P12VG and 5V3VG good	1.275	1.325	1.375	
VIOG falling threshold	5V3VG where VIOG starts falling	0.6	0.8	1.0	
15VG low voltage	PWREN = low		0.1	1.0	

NOTES: (1) All voltages are with respect to DIGGND unless otherwise stated.
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(3) When references to lines of individual slots are given without the slot identifier, the statement applies to lines on each slot.

ELECTRICAL CHARACTERISTICS,

P12VIN = 12 V, DIGVCC = 3.3 V, M12VIN = −12 V, 3VAUXI = 3.3 V, V5IN = 5 V, R_{MISET} = 6.04 kΩ, all outputs unloaded, T_A = −40 °C to 85 °C, (unless otherwise noted) (1)(2)(3)

Logic

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input high voltage (all digital inputs)		2.1			V
Input low voltage (all digital inputs)				0.8	
$\overline{\text{BUTTONA}}$ test mode input voltage	Mode is only sensed on the rising edge of PGOOD	10.0			
$\overline{\text{BUTTONA}}$ run mode input voltage	Mode is only sensed on the rising edge of PGOOD			5.5	
Input hysteresis (M66EN, SW, $\overline{\text{BUTTONA}}$, $\overline{\text{PRSNT}}$)		0.4		1.0	
Input hysteresis (PGOOD)		0.15		0.60	
Output high voltage (all push-pull outputs)	I_L = 4 mA	2.4	2.8		
Output low voltage ($\overline{\text{ATTLED}}$, $\overline{\text{PWRLED}}$)	I_L = 8 mA			0.5	
	I_L = 24 mA		0.4	0.8	
Output low voltage (all other outputs)	I_L = 4 mA		0.2	0.5	
Input pull-up resistor impedance	For inputs with pull-up resistors (see pin descriptions)	30		200	kΩ
Input pull-down resistor impedance	For inputs with pull-down resistors (see pin descriptions)	30		200	
PCIXCAP threshold between 33 MHz and 533 MHz		0.3	0.4	0.5	V
PCIXCAP threshold between 533 MHz and 266 MHz		1.1	1.2	1.3	
PCIXCAP threshold between 266 MHz and 66 MHz		1.95	2.05	2.15	
PCIXCAP threshold between 66 MHz and 133 MHz		2.8	2.9	3.0	

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Logic Switching(7)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
FCLK	Operating CLK frequency		0		10	MHz
TCLKH TCLKL	CLK high and low time		45			ns
TRF	Digital input rise and fall time, 10% to 90%	Recommended input rates for all non-hysteretic inputs	1		10	ns
TCOCLK	CLK to SID delay	C_L = 15 pF	5		15	ns
TCOLC	LC rising to output delay	All C_L = 15 pF except $\overline{BUSEN}$ C_L = 50 pF			20	ns
TSUSOD	SOD and SID setup time to CLK		15			ns
THSOD	SOD and SID hold time from CLK		4			ns
TSUPG	MSMODE, DMODE, TEST, and $\overline{PWRLED}$ setup time to PGOOD		15			ns
THPG	MSMODE, DMODE, TEST, and $\overline{PWRLED}$ hold time from PGOOD		0			ns
TZHL	PGOOD asserted to SID enable time				10	ns
THLZ	PGOOD deasserted to SID float time				15	ns
TND	NAND tree input to NT_OUT delay	NAND tree mode, C_L = 15 pF			200	ns
TFLRL	Fault asserted to bus disconnect(5)	Run-time test mode			20	ns
TRLRL	$\overline{RST}$ asserted to $\overline{RESET}$ asserted	C_L = 15 pF			20	ns
TRLCO	$\overline{RST}$ asserted and LCA low to output change	All C_L = 15 pF except $\overline{BUSEN}$ C_L = 50 pF			20	ns
TRHLCH	$\overline{RST}$ rising to LC rising		15			ns
TPGLD	PGOOD deasserted to bus disconnect	All C_L = 15 pF except $\overline{BUSEN}$ C_L = 50 pF			15	ns
TRPW, TLCPW	$\overline{RST}$ and LC low pulse width		45			ns
TGCLC	Delay from end of GLOBAL command to LC rising edge(6)		6n			$1/F_{CLK}$
TDPD	Direct mode signal propagation delay from input to output	All signals except PCIXCAP			20	ns

NOTES: (1). All voltages are with respect to DIGGND unless otherwise stated.
(2) Currents are positive into and negative out of the specified terminal.
(3) When references to lines of individual slots are given without the slot identifier, the statement applies to lines on each slot.
(5) $\overline{ATTLED}$ (Fault) asserted to $\overline{RESET}$ asserted; $\overline{ATTLED}$ (Fault) asserted to $\overline{CLKEN}$ or $\overline{BUSEN}$ deasserted.
(6) The delay allowance is measured in CLK periods and is a function of the number of slots (n) supported by the platform. The parameter specified must be multiplied by the number of slots to determine the total number of clocks that must be allowed.
(7) All logic switching characteristics tested with Tr = Tf = 2 ns.

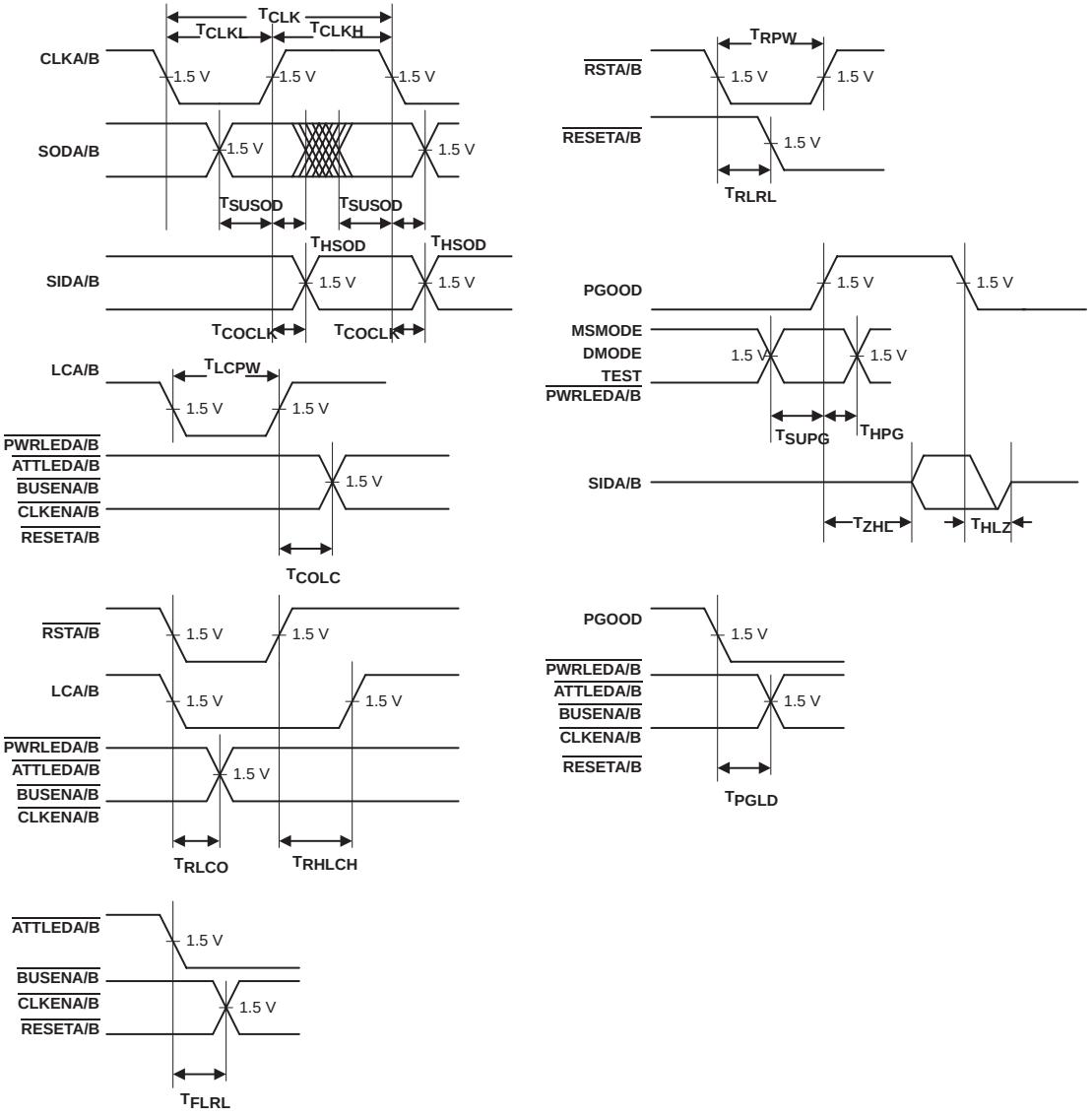


Figure 1. AC Logic Switching Characteristic Timing Diagrams

Terminal Functions

Terminal names in (parenthesis) indicate alternate terminal names for functions applicable when the device is operating in Direct Mode.

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	15VGB	I/O	Gate drive for the 1.5-V V_{IO} slot B FET switches. Ramp rate is programmed by the external capacitor connected from 5V3VGB to PWRGND. The voltage on 15VGB self-limits to regulate 1.5-V V_{IO} to 1.5 V. If VIO is switched and not regulated, leave this pin open.
2	15VISB	I	This pin in conjunction with the 15VSB pin senses the current to 1.5-V V_{IO} slot B. Connect to the load side of the 1.5-V V_{IO} current sense resistor to this pin. This pin is used as the regulator input to limit 1.5-V V_{IO} for slot B to 1.5 V. V_{IO} bleed is connected to this pin. The recommended current sense resistor value is 6 mΩ. A 0.01-µF capacitor from this pin to ANAGND is recommended.
3	15VSB	I	This pin in conjunction with the 15VISB pin senses the current to 1.5-V V_{IO} slot B. Connect to the current sense resistor at the 1.5-V Vio FET source. A 0.01-µF capacitor from this pin to ANAGND is recommended.
4	5VISB	I	This pin in conjunction with the 5VSB pin senses the current to the 5-V slot B main power load. This pin is used for output voltage sense, output bleed, and as the input to the output good and output low comparator (see Block Diagram). Connect to the load side of the 5-V current sense resistor. The recommended current sense resistor value is 6 mΩ. A 0.01-µF capacitor from this pin to ANAGND is recommended.
5	5VSB	I	This pin in conjunction with the 5VISB pin senses the current to the 5-V slot B main power load. Connect to the source of the 5-V FET switch. A 0.01-µF capacitor from this pin to ANAGND is recommended.
6	P12VINB	I	The 12-V power input to the internal FET for slot B. This input must be connected to P12VINA. Connect a 0.1-µF capacitor from this pin to PWRGND.
7	P12VGB	I/O	This pin is connected to the gate of the slot B 12-V internal power FET. Connect a capacitor from this pin to PWRGND to program the slot B 12-V and –12-V power ramp rate. The recommended capacitor value is 33 nF for 0.3 V/ms ramp rate on 12 V and a 0.45-V/ms ramp rate on –12-V power. Output under-voltage comparators are disabled until this pin and 5V3VG are high.
8	P12VOB	O	This output delivers 12-V power to slot B when enabled and is pulled to PWRGND with a bleed current when disabled. A 2.2-µF capacitor from this pin to ANAGND is recommended.
9	M12VINB	I	Connect this power input to –12-V power to drive slot B. This input must be connected to M12VINA. Connect a 0.1-µF capacitor from this pin to PWRGND.
10	M12VOB	O	This output delivers –12-V power to slot B when enabled and is pulled to PWRGND with a bleed current when disabled. Turn on of –12-V power tracks turn on of 12-V power and is controlled by the capacitor on P12VGB. A 0.01-µF capacitor from this pin to ANAGND is recommended.
11	MISET	I/O	This pin programs current limit for 12-V, 5-V, 3.3-V, and –12-V main supplies. MISET does not control 3.3 VAUX or V_{IO} current limit. The recommended resistor from MISET to ANAGND is 6.04kΩ ±1%. Increasing the value of this resistor raises the current-limit thresholds for the supplies listed above proportionately. The maximum value of the MISET resistor is 12 kΩ.
12	ANAGND1	GND	Ground for low-level signals including the current sense circuits and the under voltage comparators.
13	$\overline{\text{BUSENB}}$	O	In serial mode, this output enables the bus switches that connect the bus to slot B. This output is a totem pole that switches between DIGVCC and DIGGND.
	(PCIXCAP1B)	O	In direct mode, this pin indicates bit 1 of the PCIXCAPB state.
14	DIGGND2	GND	This pin is the ground return for the digital circuits in the TPS2342.
15	$\overline{\text{CLKENB}}$	O	In serial mode, this output enables the bus switches that connect the bus CLK to the slot B clock. This output is a totem pole that switches between DIGVCC and DIGGND.
	(PCIXCAP2B)	O	In direct mode, this pin indicates bit 2 of the PCIXCAPB state.

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
16	$\overline{\text{PRSNT1B}}$	I	In serial mode, this input connects to the PCI presence detect bit 1 on slot B. This pin has an internal 100-kΩ pull-up resistor to DIGVCC and hysteresis.
	($\overline{\text{FAULTB}}$)	O	In direct mode, this is an open-drain output that indicates a main or aux power fault when PGOOD is asserted.This pin has an internal 100-kΩ pull-up resistor to DIGVCC and hysteresis.
17	$\overline{\text{PRSNT2B}}$	I	In serial mode, this input connects to the PCI presence detect bit 2 on slot B. This pin has an internal 100-kΩ pull-up resistor to DIGVCC and hysteresis.
	($\overline{\text{AUXFLTB}}$)	O	In direct mode, this is an open-drain output that indicates an aux power fault. This pin has an internal 100-kΩ pull-up resistor to DIGVCC. When DIGVCC is off this output is not valid and a VAUX FAULT is indicated on the ATTLEDB.
18	$\overline{\text{RESETB}}$	O	In serial mode, this output drives the slot B $\overline{\text{RESET}}$ signal. This output is a totem pole that switches between DIGVCC and DIGGND.
	(PCIXCAP3B)	O	In direct mode, this pin indicates bit 3 of the PCIXCAPB state.
19	PCIXCAPB	I	This pin is the input to a 5-level A/D converter that determines the speed and mode of the inserted B slot card based on the impedance from this pin to ANAGND. The operation of this pin meets the PCI−X local bus specification, revision 2.0.
20	M66ENB	I/O	In serial mode, this pin is an input with hysteresis that monitors the 66-MHz PCI mode of slot B. When $\overline{\text{CLKENB}}$ asserts, this becomes an open-drain output to drive the slot B M66EN pin with the appropriate mode. This pin has an internal 100-kΩ pull-up resistor to 3VISB and hysteresis.
	($\overline{\text{PWROFFB}}$)	O	In direct mode $\overline{\text{PWROFFB}}$ is a logic output that indicates the status of the slot. During turn-on of the slot main power, $\overline{\text{PWROFFB}}$ goes high after P12VGB and 5V3VGB ramphigh, indicating that the slot is fully powered. With slot main power on, $\overline{\text{PWROFFB}}$ asserts low if there is an over-current fault on 3.3 V_{AUX} or main for slot B. During turn-off of slot main power, $\overline{\text{PWROFFB}}$ asserts low after the voltage on all main power supplies are below the low comparator threshold, indicating the the slot is fully unpowered. This pin has an internal 100-kΩ pull-up resistor to 3VISA.
21	$\overline{\text{BUTTONB}}$	I	In serial mode, this input is normally high, 3.3 V, and is pulled low to request attention on slot B. A register bit is set to indicate a slot B button has been pressed. This pin has an internal 100-kΩ pull-up to DIGVCC and hysteresis.
	(PWRENB)	I	In direct mode, PWRENB is asserted to turn on slot B main power. $\overline{\text{FAULTB}}$ is cleared by de-asserting PWRENB. This pin has an internal 100-kΩ pull-up to DIGVCC and hysteresis.
22	SWB	I	When low, this input enables 3.3-V aux power to slot B. AUXFLTB is cleared by de-asserting SWB. This pin has an internal 100-kΩ pull-up resistor to 3VAUXI and hysteresis.
23	$\overline{\text{ATTLEDB}}$	O	This open-drain power output directly drives the slot B attention indicator LED. When serial mode is active, this pin defaults to deasserted. While PGOOD is asserted this pin indicates the slot B LED attention indicator output signal as received from the serial interface bus or dedicated direct mode input. While PGOOD is deasserted, this pin indicates the state of the AUXFLTB latch internal signal. This signal pulls low with up to 24 mA of drive when asserted and is pulled high by an on-chip 100-kΩ resistor to V5IN when deasserted.
24	$\overline{\text{PWRLEDB}}$	O	This open-drain active-low power output directly drives the slot B power indicator LED. When serial mode is active, this output defaults to deasserted. In direct mode, PWRLEDB follows PLEDENB. This signal pulls low with up to 24 mA of drive when asserted and is pulled high by an on-chip 100-kΩ resistor to V5IN when deasserted. If PWRLEDB is low, on the rising edge of PGOOD, the slot power enters the forced enable mode. See page 30 in the Operating Modes section.
25	SODB	I	In multi-slot serial mode, this pin is the serial data input, receiving data from another TPS2342 on each rising edge of CLKB. This data is passed to the next TPS2342 or controller via SIDA. In single-slot serial mode, this pin is the serial data input, receiving commands and data from the controller. Data is shifted into the TPS2342 on the rising edge of CLKB.
	(VIOSELB)	I	In direct mode, this pin selects between 1.5 V (when low) and 3.3 V VIO for slot B. Change VIOSELB level only when slot power is off.

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
26	SIDB	I/O	In multi-slot serial mode, this pin is the serial data output. Serial output data from slot A is driven out to the next TPS2342 on the rising edge of CLKB. In single-slot serial mode, this pin is the serial data output to provide slot B status to the PCI controller on the rising edge of CLKB. This pin has an internal 100-kΩ pull-down resistor to DIGGND.
	(DMODE)	I	This pin is the input to determine whether to operate in direct or serial mode. While PGOOD is low, this pin is high impedance. The state of this pin is stored on the rising edge of PGOOD. See interface Operating Modes section.This pin has an internal 100-kΩ pull-down resistor to DIGGND.
27	$\overline{\text{RSTB}}$	I	In serial mode, this pin controls the $\overline{\text{RESETB}}$ output. In multi-slot serial mode, $\overline{\text{RSTB}}$ is connected to $\overline{\text{RSTA}}$. This pin has an internal 100-kΩ pull-up resistor to DIGVCC.
	n/a		In direct mode, this pin has no function.This pin has an internal 100-kΩ pull-up resistor to DIGVCC.
28	LCB	I	In serial mode, this pin is the slot B serial bus latch clock. On the rising edge of this pin, data is transferred from the internal shift registers to the parallel output registers. This signal is synchronous with the bus segment PCI clock. The latch clock signal is described in more detail in the TPS2342 programming data, TI document sluu193. In multi-slot serial mode, LCB is connected to LCA.
	(ALEDENB)	I	In direct mode, this pin controls ATTLEDB. When this input is high, the LED is on (low). If the attention LED is not used, ground this input pin.
29	CLKB	I	In serial mode, this input is the serial clock for the slot A serial interface. Data is shifted on the rising edge of this clock. In multi-slot serial mode, CLKB is connected to CLKA.
	(PLEDENB)	I	In direct mode, this pin is the input that drives PWRLEDB. When this input is high, the LED is on (low). If the power LED is not used, ground this input pin.
30	DIGVCC	I	This pin is the 3.3-V main power input to the TPS2342. Bypass this pin to DIGGND with a 0.1-µF ceramic capacitor close to the TPS2342.
31	DIGGND1	GND	This pin is the ground return for the digital circuits in the TPS2342.
32	CLKA	I	In serial mode, this input is the serial clock for the slot A serial interface. Data is shifted on the rising edge of this clock. In multi-slot serial mode, CLKA is connected to CLKB
	(PLEDENA)	I	In direct mode, this pin is the input that drives PWRLEDA. When this input is high, the LED is on (low). If the power LED is not used, ground this input pin.
33	LCA	I	In serial mode, this pin is the slot A serial bus latch clock. On the rising edge of this pin, data is transferred from the internal shift registers to the parallel output registers. This signal is synchronous with the bus segment PCI clock. The latch clock signal is described in more detail in the TPS2342 programming data, TI document sluu193. In multi-slot serial mode, LCA is connected to LCB.
	(ALEDENA)	I	In direct mode, this pin controls ATTLEDA. When this input is high, the LED is on (low). If the attention LED is not used, ground this input pin.
34	$\overline{\text{RSTA}}$	I	In serial mode, this pin controls the $\overline{\text{RESETA}}$ output. In multi-slot serial mode, $\overline{\text{RSTA}}$ is connected to $\overline{\text{RSTB}}$. This pin has an internal 100-kΩ pull-up resistor to DIGVCC.
	n/a		In direct mode, this pin has no function. This pin has an internal 100-kΩ pull-up resistor to DIGVCC.
35	SIDA	I/O	In serial mode, this pin is the serial output data. Serial output data is driven out to the controller on the rising edge of CLKA. On the rising edge of PGOOD, if this pin is high, the TPS2342 enters multi-slot mode; if low, the TPS2342 enters single-slot mode. To use the TPS2342 in multi-slot mode, pull this pin to 3.3 V with a 10-kΩ resistor. To use the TPS2342 in single-slot mode, pull this pin to DIGGND with a 10-kΩ resistor. This pin has an internal 100-kΩ pull-down resistor to DIGGND.
	DIRECT	I	This pin is the input to determine whether to operate in direct or serial mode. WhilePGOOD is low, this pin is high impedance. The state of this pin is stored on the rising edge of PGOOD. (See Interface Operating Modes section. This pin has an internal 100-kΩ pull-down resistor to DIGGND.

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
36	SODA	I	In single-slot serial mode, this pin accepts slot A commands from the controller. Data is shifted in on the rising edge of CLKA. In multi-slot serial mode, this pin accepts slot A commands from the controller and passes them to the next slot and the next TPS2342.
	(VIOSELA)	I	In direct mode, this pin selects 1.5 V (when low) or 3.3 V V_{IO} for slot A. Only change VIOSELA level when slot power is off.
37	$\overline{\text{PWRLEDA}}$	O	This open-drain active-low power output directly drives the slot A power indicator LED. When serial mode is active, this output defaults to deasserted. In direct mode, PWRLEDA follows PLEDENA. This signal pulls low with up to 24 mA of drive when asserted and is pulled high by an on-chip 100-kΩ resistor to V5IN when deasserted. If PWRLEDA is low on the rising edge of PGOOD, the slot power enters the forced enable mode. See Interface Operating Modes.
38	$\overline{\text{ATTLEDA}}$	O	This open-drain power output directly drives the slot A attention indicator LED. When serial mode is active, this pin defaults to deasserted. While PGOOD is asserted this pin indicates the slot A LED attention indicator output signal as received from the serial interface bus or dedicated direct mode input. While PGOOD is deasserted, this pin indicates the state of the AUXFLTA latch.This signal pulls low with up to 24 mA of drive when asserted and is pulled high by an on-chip 100-kΩ resistor to V5IN when deasserted.
39	SWA	I	When low, this input enables 3.3-V Aux power to slot A. AUXFLTA is cleared by de-asserting SWA. This pin has an internal 100-kΩ pull-up resistor to 3VAUXI and hysteresis.
40	$\overline{\text{BUTTONA}}$	I	In serial mode, this input is normally high, 3.3 V, and is pulled low to request attention on slot A. A register bit is set to indicate a slot A button has been pressed. This pin has an internal 100-kΩ pull-up to DIGVCC and hysteresis.
	(PWRENA)	I	In direct mode, PWRENA is asserted to turn on slot A main power. $\overline{\text{FAULTA}}$ is cleared by de-asserting PWRENA. This pin has an internal 100-kΩ pull-up to DIGVCC and hysteresis.
41	M66ENA	I/O	In serial mode, this pin is an input that monitors the 66-MHz PCI mode of slot A. When $\overline{\text{CLKENA}}$ asserts, this pin becomes an open-drain output to drive the slot A M66EN pin with the appropriate mode. This pin has an internal 100-kΩ pull-up resistor to 3VISA and hysteresis.
	($\overline{\text{PWROFFA}}$)	O	In direct mode $\overline{\text{PWROFFA}}$ is a logic output that indicates the status of the slot. During turn-on of the slot main power, $\overline{\text{PWROFFA}}$ goes high after P12VGA and 5V3VGA ramphigh, indicating that the slot is fully powered. With slot main power on, $\overline{\text{PWROFFA}}$ asserts low if there is an over-current fault on 3.3 V_{AUX} or main for slot A. During turn-off of slot main power, $\overline{\text{PWROFFA}}$ asserts low after the voltage on all main power supplies are below the low comparator threshold, indicating the the slot is fully unpowered. This pin has an internal 100-kΩ pull-up resistor to 3VISA.
42	PCIXCAPA	I	This pin is the input to a 5-level A/D converter that determines the speed and mode of the inserted A slot card based on the impedance from this pin to ANAGND. The operation of this pin meets the PCI−X local bus specification, revision 2.0.
43	$\overline{\text{RESETA}}$	O	In serial mode, this output drives the slot A $\overline{\text{RESET}}$ signal. This output is a totem pole that switches between DIGVCC and DIGGND.
	(PCIXCAP3A)	O	In direct mode, this pin indicates bit 3 of the PCIXCAPA state.
44	$\overline{\text{PRSNT2A}}$	I/O	In serial mode, this input connects to the PCI presence detect bit 2 on slot A. This pin has an internal 100-kΩ pull-up resistor to DIGVCC and hysteresis.
	($\overline{\text{AUXFLTA}}$)	O	In direct mode, this open-drain output indicates an AUX power fault when DIGVCC is off. This output is not valid and VAUX fault is indicated on the ATTLED.This pin has an internal 100-kΩ pull-up resistor to DIGVCC.

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
45	$\overline{\text{PRSNT1A}}$	I/O	In serial mode, this input connects to the PCI presence detect bit 1 on slot A. This pin has an internal 100-kΩ pull-up resistor to DIGVCC and hysteresis.
	($\overline{\text{FAULTA}}$)	O	In direct mode, this open-drain output indicates an AUX or main power fault on SLOTA when PGOOD is asserted.This pin has an internal 100-kΩ pull-up resistor to DIGVCC and hysteresis.
46	$\overline{\text{CLKENA}}$	O	In serial mode, this output enables the bus switches that connect the bus CLK to the slot A clock. This output is a totem pole that switches between DIGVCC and DIGGND. By default, $\overline{\text{CLKENA}}$ is deasserted. $\overline{\text{CLKENA}}$ is changed by the SHIFTOUT command and LCA.
	(PCIXCAP2A)	O	In direct mode, this pin indicates bit 2 of the PCIXCAPA state.
47	DIGGND3	GND	This pin is the ground return for the digital circuits in the TPS2342.
48	$\overline{\text{BUSENA}}$	O	In serial mode, this output enables the bus switches that connect the bus to slot A. This output is a totem pole that switches between DIGVCC and DIGGND. By default, $\overline{\text{BUSENA}}$ is deasserted. $\overline{\text{BUSENA}}$ is changed by the SHIFTOUT command and LCA.
	(PCIXCAP1A)	O	In direct mode, this pin indicates bit 1 of the PCIXCAPA state.
49	PGOOD	I	This input is used for TPS2342 initialization. PGOOD should be asserted after power is good in the whole system preventing Input UVLO fault at power up. The operating mode is selected on the rising edge of PGOOD as described in the table under interface operating modes in the applications information section. This pin has an internal 100-kΩ pull-up to DIGVCC and hysteresis
50	ANAGND2	GND	Ground for low-level signals including the current sense circuits and the under voltage comparators.
51	M12VOA	O	This output delivers –12-V power to slot A when enabled and is pulled to PWRGND with a bleed current when disabled. Turn on of –12-V power tracks turn on of 12-V power and is controlled by the capacitor on P12VGA. A 0.01-µF capacitor from this pin to ANAGND is recommended.
52	M12VINA	I	Connect this power input to –12-V power to drive slot A. This input must be connected to M12VINB. Connect a 0.1-µF capacitor from this pin to PWRGND. The heat-conducting pad on the underside of the package is electrically connected to M12VINA.
53	P12VOA	O	This output delivers 12-V power to slot A when enabled and is pulled to PWRGND with a bleed current when disabled. A 2.2-µF capacitor from this pin to ANAGND is recommended.
54	P12VGA	I/O	This pin is connected to the gate of the slot A 12-V internal power FET. Connect a capacitor from this pin to PWRGND to program the slot A 12-V and –12-V power ramp rate. The recommended capacitor value is 33 nF for 0.3-V/ms ramp rate on 12 V and a 0.45-V/ms ramp rate on –12-V power. Output undervoltage comparators are disabled until this pin and 5V3VGA are high.
55	P12VINA	I	The 12-V power input to slot A. This input must be connected to P12VINB. Connect a 0.1-µF capacitor from this pin to PWRGND.
56	5VSA	I	This pin in conjunction with the 5VISA pin senses the current to the 5-V slot A main power load. Connect to the source of the 5-V FET switch. A 0.01-µF capacitor from this pin to ANAGND is recommended.
57	5VISA	I	This pin in conjunction with the 5VSA pin senses the current to the 5-V slot A main power load. This pin is used for output voltage sense, output bleed and as the input to the V_{IO} output good comparator. Connect to the load side of the 5-V current sense resistor. The recommended current sense resistor value is 6 mΩ. A 0.01-µF capacitor from this pin to ANAGND is recommended.
58	15VSA	I	This pin in conjunction with the 15VISA pin senses the current to 1.5-V V_{IO} slot A. Connect to the current sense resistor at the 1.5-V Vio FET switch A 0.01-µF capacitor from this pin to ANAGND is recommended.
59	15VISA	I	This pin in conjunction with the 15VSA pin senses the current to 1.5-V V_{IO} slot A. This pin is used as the regulator input to limit 1.5-V V_{IO} for slot A to 1.5 V and as the input to the V_{IO} output good comparator. V_{IO} bleed is connected to this pin. Connect to the load side of the 1.5-V V_{IO} current sense resistor. The recommended current sense resistor value is 6 mΩ. A 0.01-µF capacitor from this pin to ANAGND is recommended.
60	15VGA	I/O	Gate drive for the 1.5-V V_{IO} slot A FET switches. Ramp rate is programmed by the external capacitor connected from 5V3VGA to PWRGND. The voltage on 15VGA self-limits to regulate 1.5 V V_{IO} to 1.5 V.
61	PWRGND2	GND	Ground for high current paths including discharge current of external gate capacitors.
62	V5IN	I	Connect this power input to 5-V power. This input is used to bias analog circuits and to check the 5-V input supply limits. Connect a 0.1-µF capacitor from this pin to PWRGND.

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
63	VIOGA	I/O	Gate drive for the 3.3-V V_{IO} slot A FET switches. This drive is not slew rate controlled and relies on the main 3.3-V slew rate control for inrush control. VIOGA rises when power is enabled and falls after 5V3VGA drops below 1 V.
64	3VSA	I	This pin in conjunction with the 3VISA pin senses the current to the 3.3-V slot A main power load. Connect to the source of the 3.3-V FET switch. A 0.01-µF capacitor from this pin to ANAGND is recommended.
65	3VISA	I	This pin in conjunction with the 3VSA pin senses the current to the 3.3-V slot A main power load. Connect to the load side of the 3.3-V current sense resistor. The recommended current sense resistor value is 6 mΩ. A 0.01-µF capacitor from this pin to ANAGND is recommended.
66	5V3VGA	I/O	Gate drive for the 5-V and 3.3-V slot A FET switches. Ramp rate is programmed by an external capacitor in series with a 2.2-kΩ resistor connected from this pin to PWRGND. The recommended capacitor value is 270 nF for 0.425-V/ms ramp rate. Output undervoltage comparators are disabled until this pin and P12VGA are high.
67	$\overline{\text{PMEA}}$	I	This input connects to the slot A power management event (PME) signal. This pin is internally pulled up to 3VAUXA with a 100-kΩ resistor.
68	$\overline{\text{PMEOA}}$	O	This output is connected to $\overline{\text{PMEA}}$ by a bus switch that is closed after slot A 3VAUX voltage is good and opens immediately when there is a fault on slot A 3 V_{AUX} or SWA opens. This output requires a pull-up resistor to 3VAUXI.
69	$\overline{\text{PMEOB}}$	O	This output is connected to $\overline{\text{PMEB}}$ by a bus switch that is closed after slot B 3VAUX voltage is good and opens immediately when there is a fault on slot B 3 V_{AUX} or SWB opens. This output requires a pull-up resistor to 3VAUXI.
70	$\overline{\text{PMEB}}$	I	This input connects to the slot B power management event (PME) signal. This pin is internally pulled up to 3VAUXB with a 100-kΩ resistor.
71	3VAUXGA	I/O	This pin is connected to the gate of the slot A 3-V_{AUX} internal power FET. Connect a capacitor from this pin to PWRGND to program the slot A 3-V_{AUX} ramp rate. The recommended capacitor value is 22 nF for 0.45-V/ms ramp rate.
72	3VAUXA	O	This output supplies 3-V_{AUX} power to slot A when enabled and is pulled low by a bleed when there is a fault on slot A 3 V_{AUX} or when $\overline{\text{SWA}}$ is opened. A 0.01-µF capacitor from this pin to ANAGND is recommended.
73	3VAUXI	I	Connect this power input to 3.3-V power to drive 3-V_{AUX} loads. Connect a 0.1-µF capacitor from this pin to PWRGND.
74	3VAUXGB	I/O	This pin is connected to the gate of the slot B 3-V_{AUX} internal power FET. Connect a capacitor from this pin to PWRGND to program the slot B 3VAUX ramp rate. The recommended capacitor value is 22 nF for 0.45 V/ms ramp rate.
75	3VAUXB	O	This output supplies 3-V_{AUX} power to slot B when enabled and is pulled low by a bleed when there is a fault on slot B 3 V_{AUX}or when $\overline{\text{SWB}}$ is opened. A 0.01-µF capacitor from this pin to ANAGND is recommended.
76	5V3VGB	I/O	Gate drive for the 5-V and 3.3-V slot B FET switches. Ramp rate is programmed by an external capacitor in series with a 2.2-kΩ resistor connected from this pin to PWRGND. The recommended capacitor value is 270 nF for 0.425-V/ms ramp rate. Output undervoltage comparators are disabled until this pin and P12VGB are high.
77	3VISB	I	This pin in conjunction with the 3-VSB pin senses the current to the 3.3-V slot B main power load. Connect to the load side of the 3.3-V current sense resistor. The recommended current sense resistor value is 6 mΩ. A 0.01-µF capacitor from this pin to ANAGND is recommended.
78	3VSB	I	This pin in conjunction with the 3-VISB pin senses the current to the 3.3-V slot B main power load. Connect to the source of the 3.3-V FET switch. A 0.01-µF capacitor from this pin to ANAGND is recommended.
79	VIOGB	I/O	Gate drive for the 3.3-V V_{IO} slot B FET switches. This drive is not slew rate controlled and relies on the main 3.3-V slew control for inrush control. VIOGB rises when power is enabled and falls after 5V3VGB drops below 1 V.
80	PWRGND1	GND	Ground for high-current paths including discharge current of external gate capacitors.

APPLICATION INFORMATION

Turn-On Sequence

Main power to the slot turns on when all input supplies are above the input supply start thresholds and power is commanded, either by asserting PWRENx in direct mode or by the power enable command on the serial interface in serial mode. The charge pump combined with the P12VGx capacitor produces a linear voltage ramp on P12VGx, which produces a linear ramping of the 12-V output and the −12-V output. At the same time, a current source on 5V3VGx combined with the 5V3VGx capacitor from produces a linear voltage ramp on 5V3VG, which produces a linear ramping of the 3.3-V and 5-V main outputs.

During this time, if any main slot current exceeds the appropriate over-current threshold for more than the over-current sensitivity time, the slot latches off and remains off until the logic command is turned off and on again.

When P12VGx exceeds the 12-V gate good threshold and 5V3VGx exceeds the 5-V gate good threshold, outputs should be fully ramped and the power MOSFETs should be fully enhanced. After this point, output under-voltage comparators are enabled. If any main slot output drops below the appropriate voltage fault threshold for more than the under-voltage sensitivity time, the slot latches off and remains off until the logic command is turned off and on again.

+12-V Supply Control

The TPS2342 integrates an N-channel power MOSFET for the 12-V supply and a voltage multiplying charge pump to drive the gate of the power MOSFET to 20 V. Inrush current for the 12-V supply is controlled because the slew rate of the 12-V supply is limited. The slew rate for the 12-V supply is set by the capacitor from P12VG to AGND.

Slew rate can be estimated as:

$$\frac{dV}{dt} = \frac{I_{GATE}}{C_{P12VGx}}$$

where C_{P12VGx} is the capacitor from P12VGx to AGND and I_{GATE} is the P12VGx gate charge current.

PCI specifications allow for 12-V supply adapter card bulk capacitance of up to 300 μF. This load capacitance causes additional inrush current of:

$$I_{INRUSH} = C_{LOAD} \times \frac{dV}{dt} = 300\ \mu F \times \frac{I_{GATE}}{C_{P12VGx}}$$

Using the recommended value for C_{P12VGx} = 0.033 μF and the typical value for I_{GATE} = 10 μA, average inrush current can be estimated as:

$$I_{INRUSH} = 300\ \mu F \times \frac{10\ \mu A}{0.033\ \mu F} = 0.091\ A$$

An internal current−sense circuit monitors the 12-V supply. The over-current threshold for the 12-V supply is directly proportional to the resistor from MISET to AGND. Raising the MISET resistor simultaneously raises the current limit threshold for the 12-V, 5-V, 3.3-V and −12-V supplies. For example, to raise the nominal output current from the 12-V supply by 20%, increase the MISET resistor 20%. This resistor can be as high as 12 kΩ if necessary.

APPLICATION INFORMATION

−12-V Supply Control

The TPS2342 integrates an N-channel power MOSFET for the −12-V supply. This switch turns on when PWRENx is asserted and turns off when PWRENx is deasserted or when there is a fault on any main power supply to the slot.

Like the 12-V supply, inrush for the −12-V supply is controlled by controlling turn-on slew rate. The −12-V supply tracks the 12-V supply, so the slew rates of these supplies are directly related. To insure that the power MOSFET for the −12-V supply fully enhances, the tracking amplifier has a gain of approximately 1.4, producing a −12-V supply slew rate 40% higher than the 12-V supply slew rate.

PCI specifications allow for −12-V supply adapter card bulk capacitance of up to 150 μF. This load capacitance causes additional inrush current of:

$$I_{INRUSH} = C_{LOAD} \times \frac{dV}{dt} = 150\ \mu F \times \frac{I_{GATE}}{C_{P12VG}} \times 1.1$$

Using the recommended value for C_{P12VG} = 0.033 μF and the typical value for I_{GATE} = 10 μA, average inrush current can be estimated as:

$$I_{INRUSH} = 150\ \mu F \times \frac{10\ \mu A}{0.033\ \mu F} \times 1.1 = 0.05\ A$$

An internal current-sense circuit monitors the −12-V supply. The over-current threshold for the −12-V supply is directly proportional to the resistor from MISET to AGND. Raising the MISET resistor simultaneously raises the current limit threshold for the 12-V, 5-V, 3.3-V and −12-V supplies. For example, to raise the nominal output current from the −12-V supply by 20%, increase the MISET resistor 20%. This resistor can be as high as 12 kΩ if necessary.

APPLICATION INFORMATION

+5-V and +3.3-V Main Supply Control

The TPS2342 uses external N-channel power MOSFETs for the 3.3-V and 5-V supplies. Inrush current for these supplies is controlled because the slew rate of the supplies is limited. These slew rates are set by the capacitor from 5V3VGx to AGND. Slew rate can be estimated as:

$$\frac{dV}{dt} = \frac{I_{GATE}}{C_{5V3VGx}}$$

where C_{5V3VG} is the capacitor from 5V3VGx to AGND and I_{GATE} is the 5V3VGx gate charge current.

PCI specifications allow for 3.3-V and 5-V supply adapter card bulk capacitance of up to 3000 μF. This load capacitance causes additional inrush current of:

$$I_{INRUSH} = C_{LOAD} \times \frac{dV}{dt} = 3000\ \mu F \times \frac{I_{GATE}}{C_{5V3VGx}}$$

Using the recommended value for C_{5V3VGx} = 0.27 μF and the typical value for I_{GATE} = 100 μA, average inrush current can be estimated as:

$$I_{INRUSH} = 3000\ \mu F \times \frac{100\ \mu A}{0.27\ \mu F} = 1.11\ A$$

An external current-sense resistor monitors the 3.3-V and 5-V supplies. The calculation of external resistor values is shown in the determining component values section.The over-current thresholds for these supplies are directly proportional to the resistor from MISET to AGND and inversely proportional to the current-sense resistor. Raising the MISET resistor simultaneously raises the current limit threshold for the 12-V, 5-V, 3.3-V and −12-V supplies. This resistor can be as high as 12 kΩ if necessary.

+1.5-V and +3.3-V V_{IO} Supply Control

The TPS2342 uses external N-channel power MOSFETs for the 1.5-V and 3.3-V VIO supplies. Inrush current for these supplies is controlled because the slew rate of the supplies are limited. These slew rates are set by the capacitor from 5V3VGx to AGND. Slew rate can be estimated as:

$$\frac{dV}{dt} = \frac{I_{GATE}}{C_{5V3VGx}}$$

where C_{5V3VGx} is the capacitor from 5V3VGx to AGND and I_{GATE} is the 5V3VGx gate charge current.

PCI specifications allow for 1.5-V and 3.3-V V_{IO} supply adapter card bulk capacitance of up to 150 μF. This load capacitance causes additional inrush current of:

$$I_{INRUSH} = C_{LOAD} \times \frac{dV}{dt} = 150\ \mu F \times \frac{I_{GATE}}{C_{5V3VGx}}$$

Using the recommended value for C_{5V3VG} = 0.27 μF and the typical value for I_{GATE}=100 μA, maximum inrush current can be estimated as:

$$I_{INRUSH} = 150\ \mu F \times \frac{100\ \mu A}{0.27\ \mu F} = 0.056\ A$$

APPLICATION INFORMATION

V_{IO} is frequently used to power V_{IO} for both the slot and the bridge so that there is minimal drop between the slot and the bridge V_{IO} supplies. When calculating the current-limit threshold for V_{IO}, take into account the current consumption of the slot and the bridge.

The 3.3-V V_{IO} supply shares current limiting with the 3.3-V main supply. If higher current is required from the 3.3-V V_{IO} supply, the external current sense resistor for the 3.3-V main supply can be lowered or the MISET resistor can be raised as described in the paragraph on the 3.3-V main supply.

An external current-sense resistor monitors the 1.5-V V_{IO} supply. The calculation of external resistor values is shown in the Determining Component Values section. The over-current threshold for this supply is inversely proportional to this current-sense resistor.

3VAUX Supply Control

The TPS2342 3VAUX supply is completely independent of the main supply. Supply status and faults on main supplies have no effect on 3VAUX and faults on 3VAUX have no effect on main supply operation.

The TPS2342 uses internal power MOSFETs for the 3VAUX supply and voltage multiplying charge pumps to drive the gates of the power MOSFETs to 8 V. Inrush current for the 3VAUX supply is controlled because the slew rate of the 3VAUX supply is limited. This slew rate is set by the capacitor from 3VAUXGx to AGND. Slew rate can be estimated as:

$$\frac{dV}{dt} = \frac{I_{GATE}}{C_{3VAUXGx}}$$

where $C_{3VAUXGx}$ is the capacitor from 3VAUXGx to AGND and IGATE is the 3VAUXG gate charge current. Inrush current caused by this slewing and any adapter card load capacitance can be estimated as:

$$I_{INRUSH} = C_{LOAD} \times \frac{dV}{dt} = C_{LOAD} \times \frac{10\ \mu A}{C_{3VAUXGx}}$$

The 3VAUXx current-sense threshold is internally set and can not be adjusted.

When main power is applied to the TPS2342, all gates are actively held low. When main power is removed, leakage current can potentially raise gate voltage, but because main power is not applied, no malfunction occurs. This is noted here as floating gates may be observed during bench testing, but ths is not an application problem.

Gate Capacitance Effect on Turn On/Off +12 V

Increasing the gate capacitor increases the turn on time for the slot voltage. To a much smaller degree, it also effects the turn off time. When slot voltage is turned off by the PWRENx, an internal FET discharges the gate capacitors. See the chart of 12-V turn on/off time for various gate capacitors, Table 1.

Table 1. 12-V Turn On/Off Time for Various Gate Capacitors

Capacitor (μF)	Turn On Time (ms)	Turn Off Time (μs)
0.033	50	4.0
0.100	140	4.8
0.270	220	8.0
0.390	370	12.0
0.470	470	12.5

APPLICATION INFORMATION

Layout Considerations

It is important to use good layout practices regarding device placement and etch routing of the backplane/system board to optimize the performance of the hot plug circuit. Some of the key considerations are listed here:

- Decoupling capacitors should be located close to the device.
- Any protection devices (e.g. zener clamps) should be located close to the device.
- To reduce insertion loss across the hot plug interface, use wide traces for the supply and return current paths. A power plane can be used for the supply return or PWRGND nodes.
- Additional copper placed at the land patterns of the sense resistors and pass FETs can significantly reduce the thermal impedance of these devices, reducing temperature rise in the module and improving overall reliability.
- Because typical values for current sense resistors can be very low (6 mΩ typical), board trace resistance between elements in the supply current paths becomes significant. To achieve maximum accuracy of the overload thresholds, good Kelvin connections to the resistors should be used for the current sense inputs to the device. The current sense traces should connect symmetrically to the sense resistor land pattern, in close proximity to the element leads, not upstream or downstream from the device.

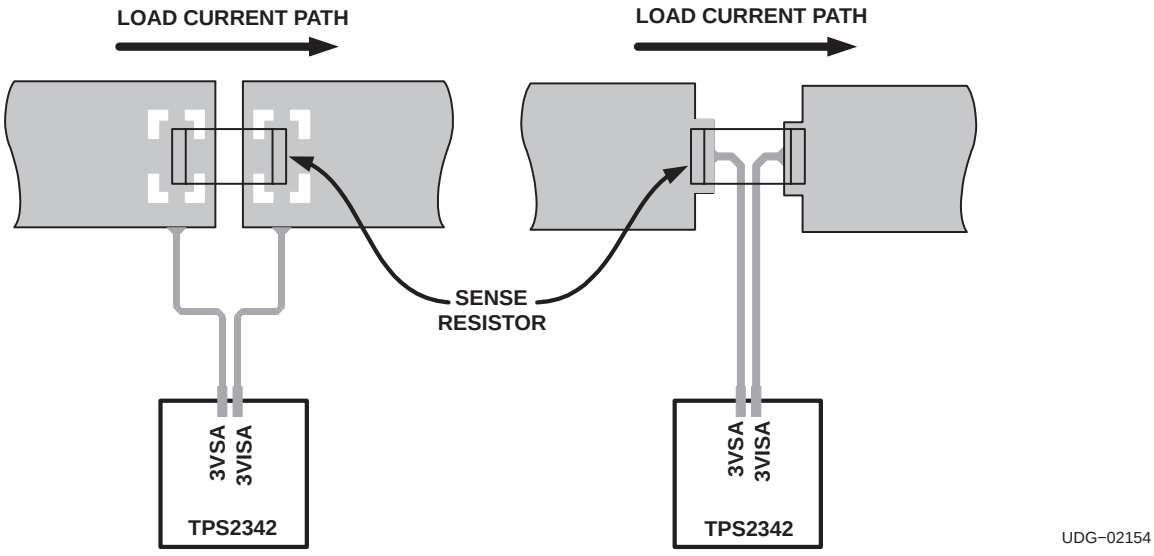


Figure 2. Connecting the Sense Resistors

These recommended layouts provide force-and-sense (Kelvin) connection to the current sense resistor to minimize circuit board trace resistance.

Power and Grounding

Connect all TPS2342 grounds directly to the digital ground plane on the circuit board through the shortest path possible. Also connect P12VINA, P12VINB, M12VINA and M12VINB directly to the appropriate power plane through the shortest path possible. A 0.1-µF decoupling capacitor is recommended on each of these power pins, as close to the pin as possible.

APPLICATION INFORMATION

Thermal Model

The TPS2342 is packaged in the HTQFP-80 PowerPad™ quad flat-pack package. The PowerPad™ package is a thermally enhanced standard size device package designed to eliminate the use of bulky heatsinks and slugs traditionally used in thermal packages. This package can be easily mounted using standard printed circuit board (PCB) assembly techniques, and can be removed and replaced using standard repair procedures.

The leadframe die pad is exposed on the bottom of the device. This provides an extremely low thermal resistance between the die and the thermal pad. The thermal pad can be soldered directly to the PCB for heatsinking. In addition, through the use of thermal vias, the thermal pad can be directly connected to a power plane or special heat sink structure designed into the PCB. On the TPS2342, the die substrate is internally connected to the −12-V input supply. Therefore the power plane or heatsink connected to the thermal pad on the bottom of the device must also connect to the −12-V input supply (recommended) or float independent of any supply (acceptable).

The thermal performance can be modeled by determining the thermal resistance between the die and the ambient environment. Thermal resistances are measures of how effectively an object dissipates heat. Typically, the larger the device, the more surface area available for power dissipation and the lower the object's thermal resistance. Figure 3 illustrates the thermal path and resistances from the die, T_J through the printed circuit board to the ambient air.

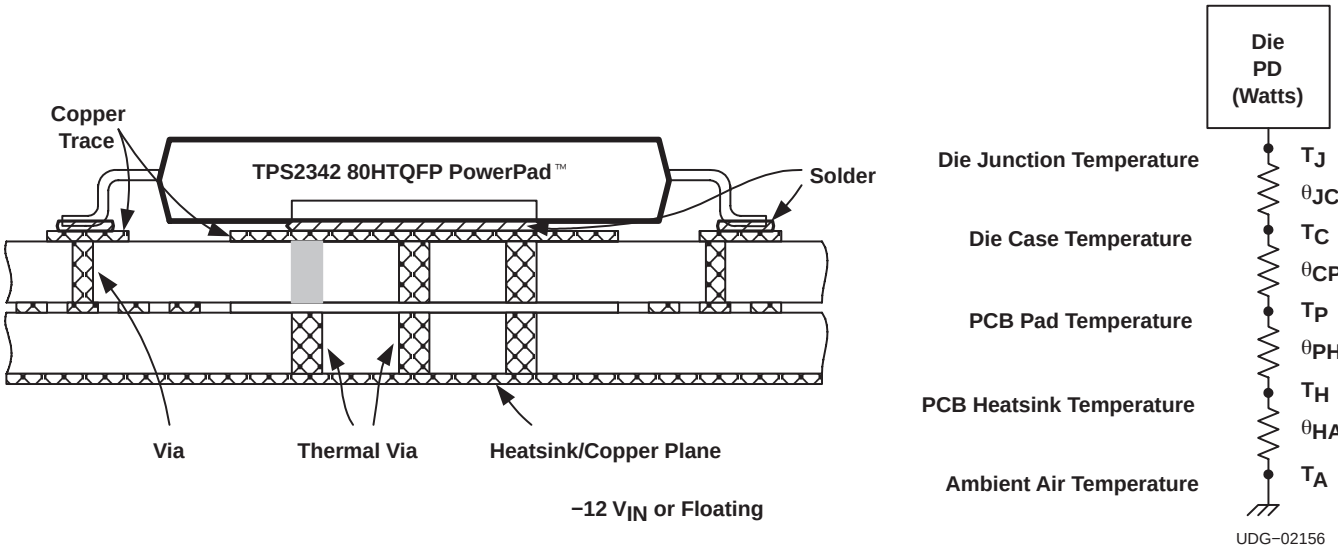


Figure 3. PowerPAD™ Thermal Model

Technical Brief *PowerPAD™ Thermally Enhanced Package* (SLMA002) can be used as a guide to model the TPS2342 thermal resistance.

When mounted to a copper pad with solder on a PCB with two ounce traces, the TPS2342 exhibits thermal resistance from junction to ambient of 29°C/W. When the TPS2342 is mounted to a conventional PCB with solder mask under the package and only the lead tips soldered to traces, the TPS2342 exhibits thermal resistance from junction to ambient of 35°C/W.

Refer to Technical Briefs: PowerPAD™ Thermally Enhanced Package SLMA003 and PowerPAD™ Made Easy SLMA004 for more information on using this PowerPad™ package.

APPLICATION INFORMATION

Thermal Shutdown

Under normal operating consitions, the power dissipation in the TS2342 is low enough that the junction temperature (T_J) is not more than 15°C above air temperature (T_A). However, in the case of a load that exceeds PCI specifications (but remains under the TPS2342 overcurrent threshold) power dissipation can be higher. To prevent any damage from an out-of-specification load or severe rise in ambient temperature, the TPS2342 contains two independent thermal shutdown circuits, one for each main supply slot. VAUX is not affected by the thermal shutdown.

The highest power dissipation in the TPS2342 is from the 12-V power FET so that TPS2342 temperature sense elements are integrated closely with these FETs. These sensors indicate when the temperature at these transistors exceeds approximately 150°C, due either to average device power dissipation, 12-V power FET power dissipation, or a combination of both.

When excessive junction temperature is detected in one slot, that slot's fault latch is set and remains set until the junction temperature drops by approximately 10°C and the slot is then restarted. The other slot is not affected by this event.

Determining Component Values

Load Conditions

Table 2. Load Conditions for Determining Component Values

SUPPLY DRIVER	I_{LOAD} (A)	I_{TRIP} (A)	C_{LOAD} (μF)	SR (V/s)
+12 V	0.5	0.94	300	250
+5 V	5	7.0	3000	200
+3.3 V	7.6	10.0	3000	200
−12 V	0.1	0.19	150	200
+3.3 Vaux	0.375	1.0	150	5000
+3.3 Vaux(1)	0.02	0.04	150	100
+1.5 VIO	1.5	4.0	150	200

(1) +3.3 Vaux turn-on from stand-by power.

APPLICATION INFORMATION

+3.3-V Supply

Overload Trip Point with MISET = 6.04 kΩ

Desired I_{TRIP} (nom) ≅ 10 A

$$R_{SENSE} = \frac{V_{RTRIP\ (nom)}}{I_{TRIP\ (nom)}} = \frac{63\ mV}{10\ A} = 0.0063\ \Omega \quad \therefore \text{Choose 6 m}\Omega,\ 2\%\ \text{sense resistor}$$

$$I_{TRIP(min)} = \frac{V_{TRIP\ (min)}}{R_{SENSE\ (max)}} = \frac{53\ mV}{6.12\ m\Omega} = 8.66\ A$$

$$I_{TRIP(max)} = \frac{V_{TRIP\ (max)}}{R_{SENSE\ (min)}} = \frac{72\ mV}{5.88\ m\Omega} = 12.24\ A$$

+5-V Supply

Overload Trip Point with MISET = 6.04 kΩ

Desired I_{TRIP} (nom) ≅ 7 A

$$R_{SENSE} = \frac{V_{RTRIP\ (nom)}}{I_{TRIP\ (nom)}} = \frac{53\ mV}{7\ A} = 0.00589\ \Omega \quad \therefore \text{Choose 6 m}\Omega,\ 2\%\ \text{sense resistor.}$$

$$I_{TRIP(min)} = \frac{V_{TRIP\ (min)}}{R_{SENSE\ (max)}} = \frac{43\ mV}{6.12\ m\Omega} = 7.03\ A$$

$$I_{TRIP(max)} = \frac{V_{TRIP\ (max)}}{R_{SENSE\ (min)}} = \frac{63\ mV}{5.88\ m\Omega} = 10.71\ A$$

1.55 Volt Supply for 1.5 V_{IO}

Overload trip point with MISET = 6.04 kΩ.

Desired $I_{TRIP(nom)}$ = 4 A

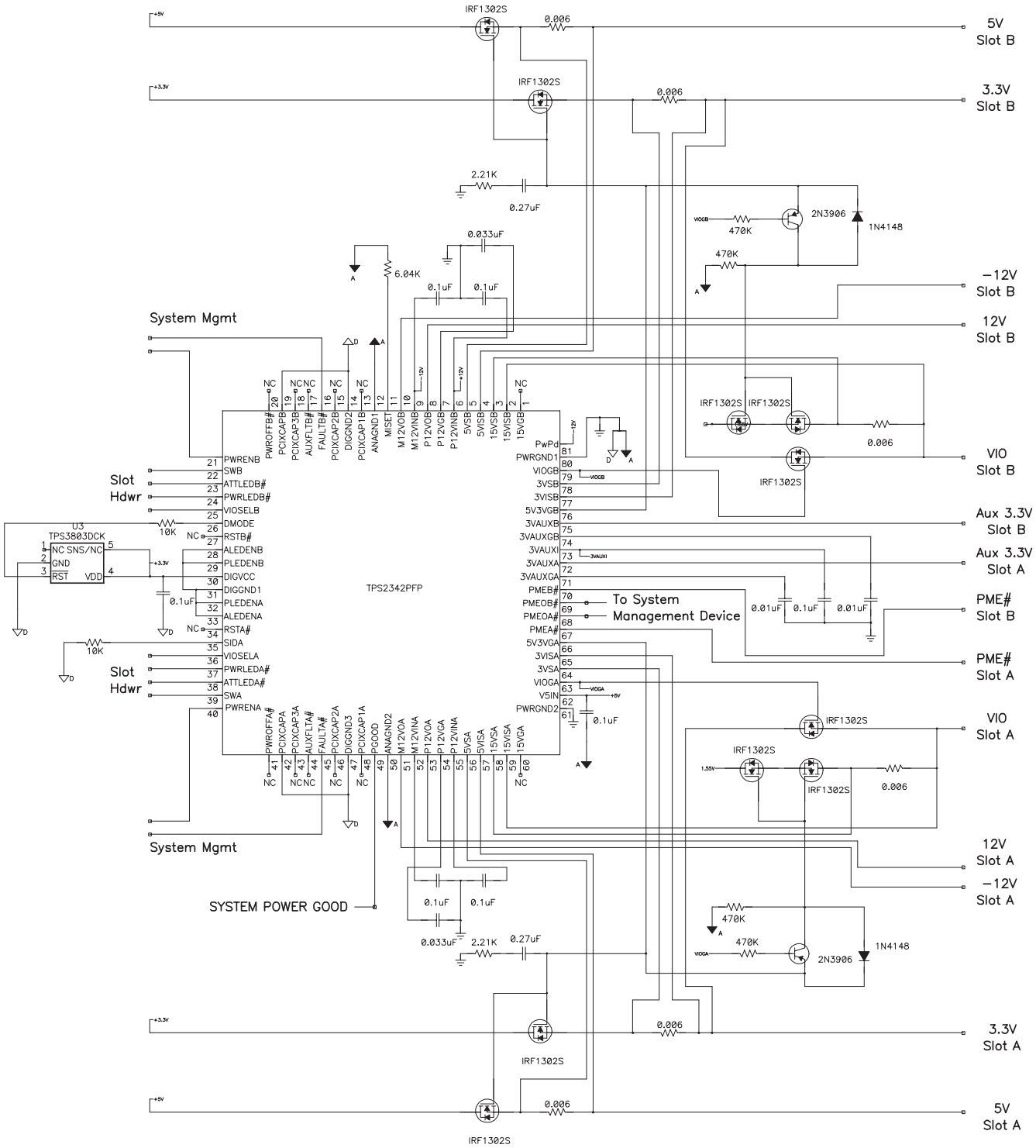
$$R_{SENSE} = \frac{V_{TRIP(nom)}}{I_{TRIP(nom)}} = \frac{23.5\ mV}{4.0\ A} = 0.00598\Omega$$

Choose 0.006 Ω

$$I_{TRIP(min)} = \frac{20\ mV}{0.00612\ \Omega} = 3.27\ A_{MIN}$$

$$I_{TRIP(max)} = \frac{27\ mV}{0.00588\ \Omega} = 4.594\ A_{MIN}$$

APPLICATION INFORMATION



APPLICATION INFORMATION

MOSFET Selection

All external power MOSFETs are N-channel devices. Gate resistors are not required.

Hot plug can cause excessive voltage spikes on the input and output of the FET. During a short circuit, an excessive current spike can occur before current limit turns off the output. Although the duration is usually very small, the energy can be large and cause big voltage fluctuations. The MOSFET will operate at high current and high drain to source voltage which could violate the safe operating area of the device and cause breakdown.

To ensure safe operation of the external MOSFET, the drain-to-source voltage rating should be reasonably higher than V_{IN}. A 2-to-1 or 3-to-1 ratio of the V_{DSS} to V_{IN} is recommended.

V_{DSS} > 2 x V_{IN}

The current rating of the FET at the maximum case temperature (usually 70°C − 100°C), I_D, should be at least 2 x $I_{TRIP(max)}$ (see R_{SENSE} Calculations Section).

I_D at $T_{C(max)}$ > 2 x $I_{TRIP(max)}$

The gate-to-source voltage rating, VGS of the FET should be at least 10 V because the TPS2342 gate voltages can be as high as 12 V and the source voltage as low as 3.3 V, a difference of 8.7 V.

VGS > 10 V

$R_{DS(on)}$ Calculation

Another important parameter in choosing a FET is the on-resistance, $R_{DS(on)}$. The lower the $R_{DS(on)}$, the smaller the power dissipation of the FET and the easier to maintain the PCI recommended bus voltage. The lowest $R_{DS(on)}$ FETs are the most expensive. To calculate the FET $R_{DS(on)}$, note the lower limit for each slot voltage specified in the PCI−X Electrical and Mechanical Addendum.

The difference between the lower limit of both the system power supply and the PCI specification slot voltage value is the system voltage budget. System power supplies specified with slightly high output voltage increases the system voltage budget making the FETs $R_{DS(on)}$ less critical. To calculate the $R_{DS(on)}$, sum the voltage drop due to contact resistance of the power input connector, the PCI connector, and the sense resistor. This sum is subtracted from the system voltage budget to give the $VR_{DS(on)}$ and ultimately the $R_{DS(on)}$.

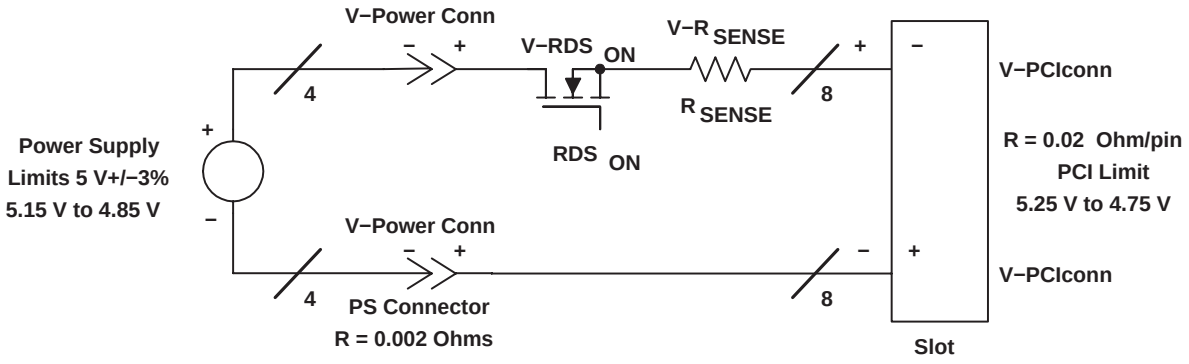


Figure 4.

APPLICATION INFORMATION

Terms

Terms are defined below referenced by an example calculation.

- System voltage budget = PCI lower limit − power supply lower limit
- System voltage drop= V power connector + V PCI connector + VR_{SENSE}

(For power and ground paths)

- $VR_{DS(on)}$ = system voltage budget − system voltage drop
- $R_{DS(on)}$ = $VR_{DS(on)}$/max operating current

Example Calculation of $R_{DS(on)}$ for the 5.0 V Main:

- PS low voltage 5.0 V − 3% = 4.85 V
- PCI spec lowest voltage to add in card = 4.75 V
- System voltage budget = 4.85 V − 4.75 V = 0.1 V
- PCI bus has 8 pins for 5.0 A, 5.0 A/8 pins = 0.625 A/pin
- Contact resistance = 20 mΩ, .625 A x 0.020 Ω = 12.5 mV
- V_{PCI} connector = 12.5 mV + 12.5 mV (return path) = 25 mV
- V power connector = 5.0 A/4 pins = 1.25 A/pin
- Pin contact resistance = 0.002 Ω,
- V power connector = 1.25A x 0.002 Ω = 2.5 mV, 2.5 mV x 2 = 5 mV
- V_{RSENSE} = 5.0 A x 0.006 Ω = 30 mV
- System voltage budget = V_{PCI} connector + V power connector + V_{RSENSE} +$VR_{DS(on)}$
- 100 = 25 + 5 + 30 + $VR_{DS(on)}$,
- $VR_{DS(on)}$ = 40 mV
- $R_{DS(on)}$ = 0.040 V/5 A = 8 mΩ

Systems have different parameters but calculating RDSon for the different voltages using these assumptions gives the following results.

Table 3.

VOLTAGE	$R_{DS(on)}$
+5 V	8 mΩ
+3.3 V	12 mΩ
+3.3 VIO	12 mΩ
+1.5 VIO	4 mΩ

APPLICATION INFORMATION

FET Heatsink

Place a layer of copper on the circuit board under the surface mount FET and solder the FET to the board for good thermal connection. Connect the copper to an inner voltage layer at the same potential or if possible, an area of copper on the other side of the board.

Decoupling Capacitors

Decoupling is required on the power inputs to the TPS2342. Use 0.1-µF capacitors on the 12 V, −12 V, 5 V, 3.3 V main and 3.3-V_{AUX} inputs and keep them close to the TPS2342 voltage input pins.

The pin descriptions for the TPS2342 signal outputs recommend 0.01-µF decoupling capacitors. These are not required.

Interface Operating Modes

The TPS2342 is initialized at power up into one of four available operating modes. The operation of the TPS2342 is controlled by the PGOOD, PWRLED, SIDB, and SIDA pins according to the following table:

PGOOD	SIDB/ DMODE	SIDA	$\overline{\text{PWRLEDx}}$	OPERATING MODE
↑	0	0	1	Single-slot serial mode: Using different hot-plug controllers for slot A and slot B.
↑	0	1	1	Multi-slot serial mode: Using the same hot-plug controller for slot A and slot B, and potentially cascading additional TPS2342.
↑	1	0	1	Direct mode.
↑	X	X	0	Force enable mode. The slot is forced enabled. (see Note 3)

NOTES: 1. X = do not care. The level on this signal does not affect the operating mode.
2. x = *a* or *b* as appropriate. For example, $\overline{\text{PWRLEDx}}$ refers to $\overline{\text{PWRLEDA}}$ or $\overline{\text{PWRLEDB}}$, depending on which slot is being discussed.
3. In force enable mode, the VIOSEL inputs have no effect. V_{IO} selection is directly controlled by the PCIXCAPx3 logic bit, derived from the programming in the PCIXCAPx input.

APPLICATION INFORMATION

Mode Initialization Timing

The input power supplies can be turned on in any sequence. The mode logic is powered from DIGVCC, pin 30, the 3.3-V main power supply. The 3.3-V main is connected to the 3VAUXI, pin 73, if V_{AUX} is not used on the system and there is no V_{AUX} power supply. The signal timing for initialization shown in Figure 5 is in relationship to DIGVCC and not VAUX when there is a separate V_{AUX} power supply.

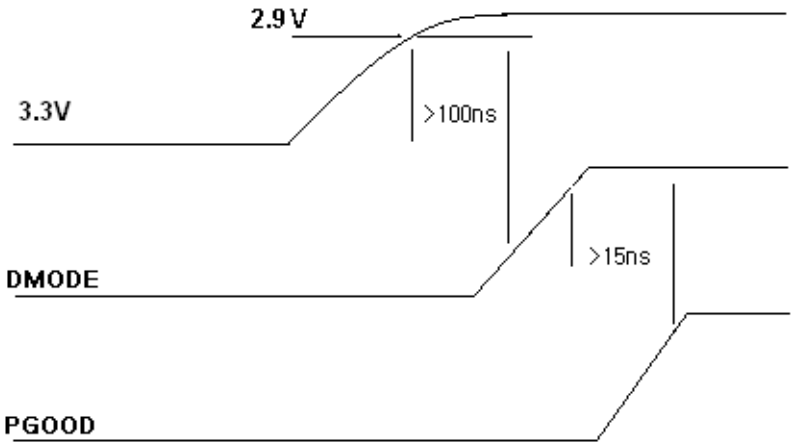


Figure 5. Mode Initialization Timing

APPLICATION INFORMATION

Initialization Methods

The mode initialization timing for either SIDA (DIRECT) or SIDB (DMODE) can be achieved though one of three different methods.

- An FPGA available in the system
- RC time constant
- Power supervisor, voltage detector circuit

Whichever method is used, the circuit output is applied to either SIDA (DIRECT) or SIDB (DMODE), whichever is high for entry to the desired mode shown in Table 1. For example, to enter direct mode, the circuit output is applied to SIDB (DMODE) while SIDA (DIRECT) is grounded. Note that no additional circuit is used for Single Slot serial mode since SIDA (DIRECT) and SIDB (DMODE) are both held low by external 10-kΩ pull-down resistors.

A single circuit can be used to initialize multiple TPS2342 power controllers. Each TPS2342 mode input pin has a resistor to the initialization circuit.

The following are examples of each initialization method:

FPGA

A spare output from an on-board FPGA programmed for the timing shown in Figure 6 is applied to SIDB (DMODE). The output of the FPGA is a push-pull type.

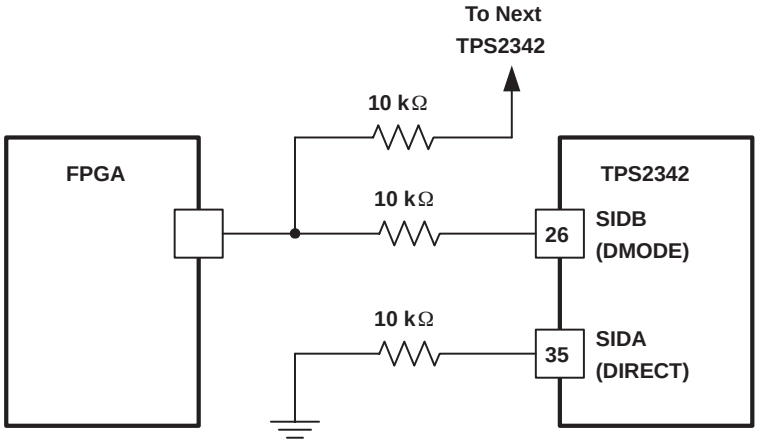


Figure 6. On-board FPGA

APPLICATION INFORMATION

RC Delay

The 10-kΩ resistor and 0.27-μF capacitor set up a delay between DIGVCC and SIDA (DMODE). The size of the capacitor can vary with the slew rate of the power supply. A 0.1-μF capacitor is sufficient for a power supply with a <20-ms slew rate and 0.27-μF for a 250-ms slew rate.

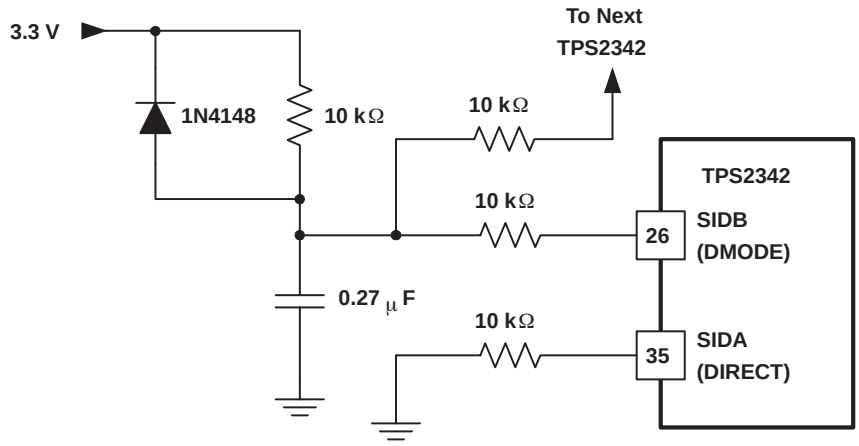


Figure 7. RC Delay

Power Supervisor

The TPS3805 is a power supervisor device. The reset output is low until the power supply reaches a 3.05 V level (typical). $\overline{\text{RST}}$ is a push-pull output.

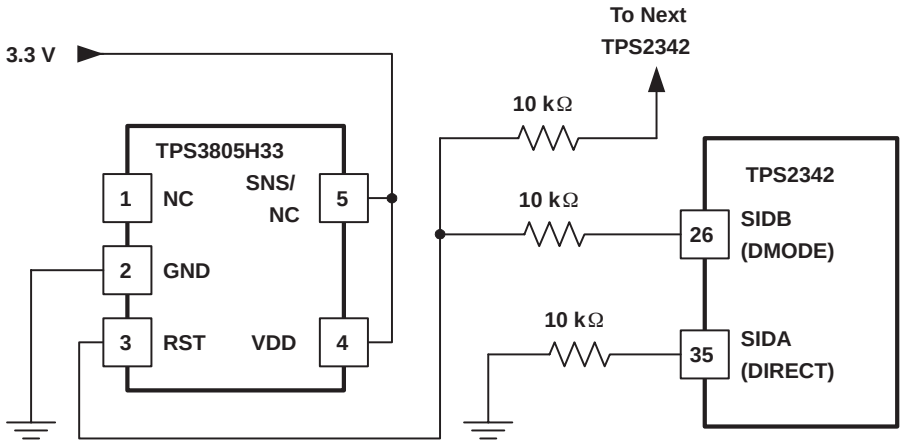


Figure 8. Power Supervisor Device

APPLICATION INFORMATION

Single-Slot Serial Mode

In single-slot serial mode, each TPS2342 has two independent serial interfaces. Control for slot A is completely independent of control for slot B.

To configure the TPS2342 for single-slot serial mode, pull SIDA to DIGGND through a 10-kΩ resistor. This insures that SIDA is low on the rising edge of PGOOD. Also, pull SIDB to DIGGND through a 10-kΩ resistor. This insures that SIDB is low on the rising edge of PGOOD.

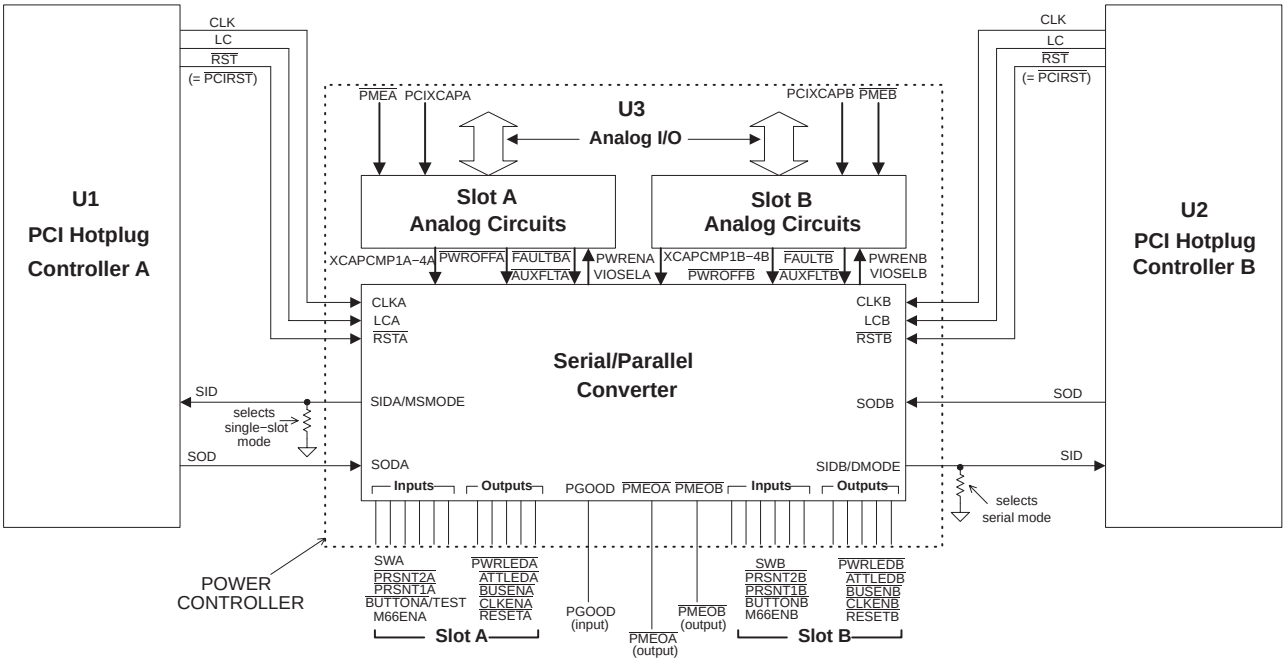


Figure 9. Single-Slot Serial Mode Equivalent Interface Block Diagram

BUSENx, CLKENx, and RESETx

The TPS2342 BUSENx and CLKENx signals connect to the PCI hot plug controller to switch bus and clock signals to the slot. The TPS2342 RESETx signal drives the slot reset.

APPLICATION INFORMATION

Multi-Slot Serial Mode

In multi-slot serial mode, one serial interface functions for both slots of the TPS2342. This serial interface can be cascaded to additional TPS2342 devices.

To configure the TPS2342 for multi-slot serial mode, pull SIDA to 3.3 V through a 10-kΩ resistor. This insures that SIDA is high on the rising edge of PGOOD. Also, pull SIDB to DIGGND through a 10-kΩ resistor. This insures that SIDB is low on the rising edge of PGOOD.

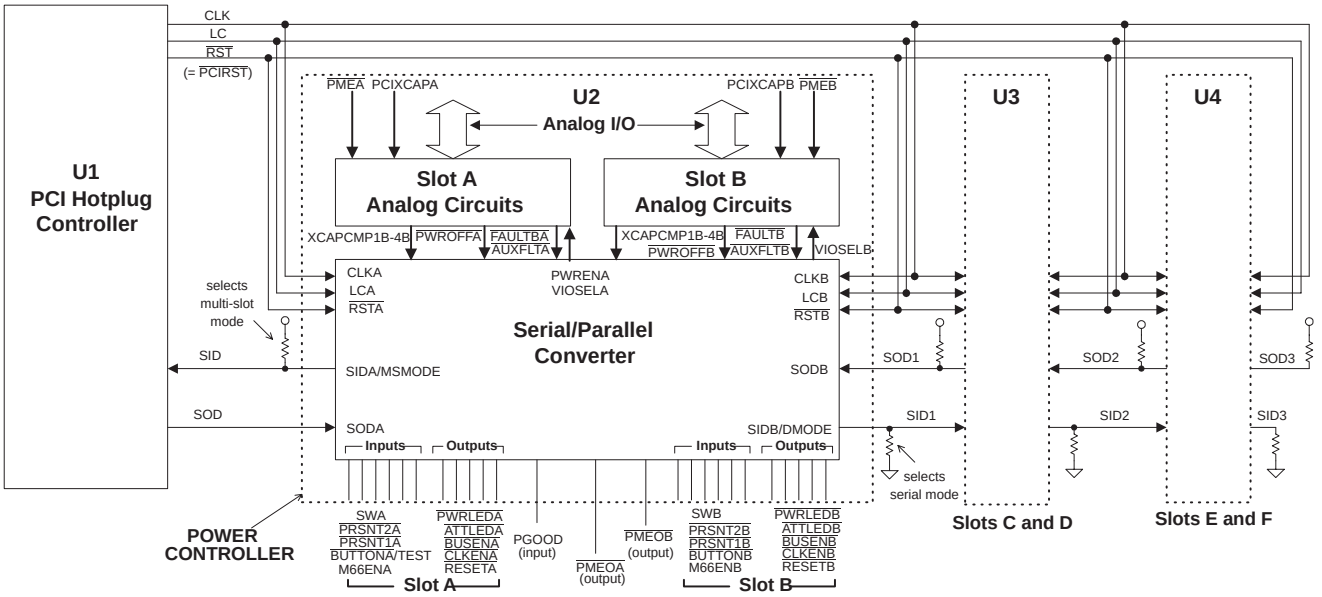


Figure 10. Multi-Slot Serial Mode Equivalent Interface Block Diagram

SID and SOD

SID and SOD are signals named for the hot plug controller functions, serial input data and serial output data. The TPS2342 slot controllers keep the same signal naming convention as the hot plug controllers so SID is the slot controller's output data and SOD is the slot controller's input data.

APPLICATION INFORMATION

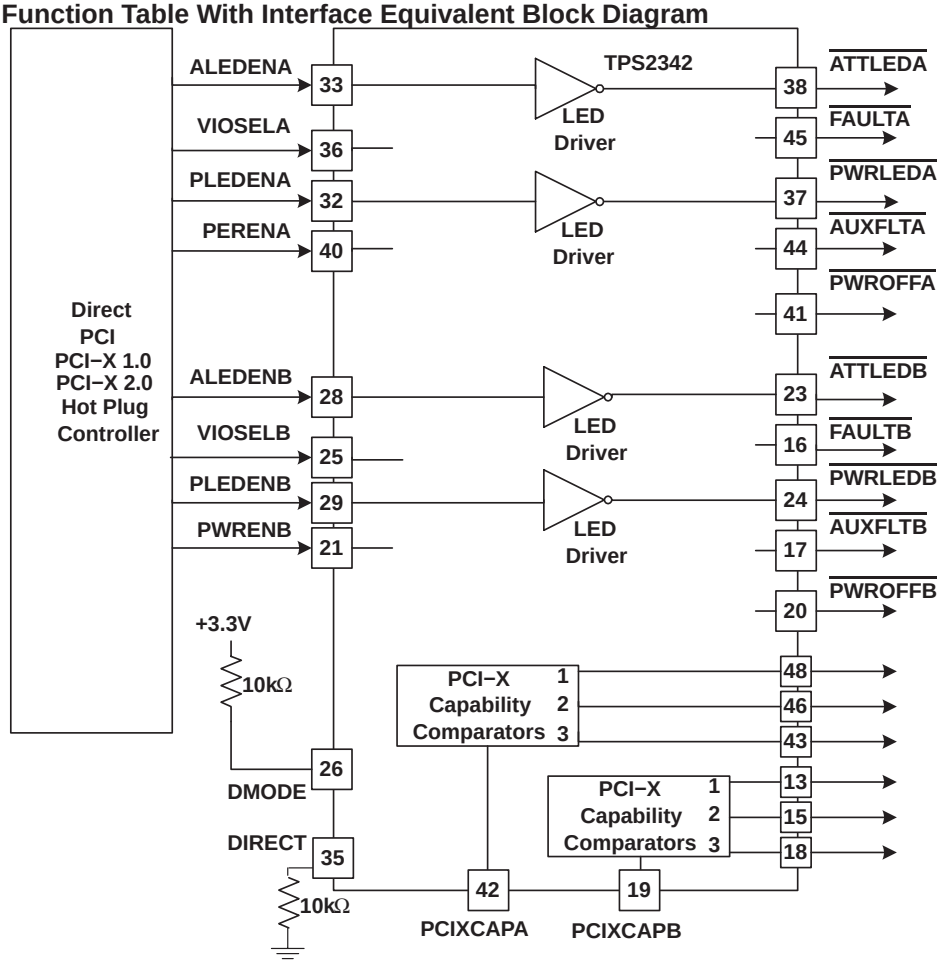
Direct Mode

In direct mode, all functions of the TPS2342 are performed by direct logic command to designated logic inputs.

To enter direct mode, SIDB must be high and SIDA must be low on the rising edge of PGOOD.To configure the TPS2342 for direct mode, pull SIDB/DMODE to 3.3 V through a 10-kΩ resistor and either ground or disconnect SIDA. An internal resistor pulls SIDA low if it is disconnected (floating).

Table 4. Direct Mode Pin Function Table With Interface Equivalent Block Diagram

PIN	FUNCTION
13	PCIXCAP1B
15	PCIXCAP2B
16	$\overline{\text{FAULTB}}$
17	$\overline{\text{AUXFLTB}}$
18	PCIXCAP3B
19	PCIXCAPB
20	$\overline{\text{PWROFFB}}$
21	PWRENB
23	$\overline{\text{ATTLEDB}}$
24	$\overline{\text{PWRLEDB}}$
25	VIOSELB
26	DMODE
27	N/A
28	ALEDENB
29	PLEDENB
32	PLEDENA
33	ALEDENA
34	N/C
35	DIRECT
36	VIOSELA
37	$\overline{\text{PWRLEDA}}$
38	$\overline{\text{ATTLEDA}}$
40	PWRENA
41	$\overline{\text{PWROFFA}}$
42	PCIXCAPA
43	PCIXCAP3A
44	$\overline{\text{AUXFLTA}}$
45	$\overline{\text{FAULTA}}$
46	PCIXCAP2A
48	PCIXCAP1A



APPLICATION INFORMATION

If the main power is on and a main power fault such as an over-current fault occurs, the $\overline{\text{FAULTx}}$ output asserts. If the main power is on and the 3.3 VAUX has an overcurrent fault, both $\overline{\text{AUXFLTx}}$ and $\overline{\text{FAULTx}}$ outputs assert. If the system requires separate main power and 3.3 AUX fault signals, 3.3-V main power to the slot can be ORed with $\overline{\text{FAULTx}}$ to produce a $\overline{\text{MAINFLTx}}$ output signal, as shown below. Power this logic from DIGVCC.

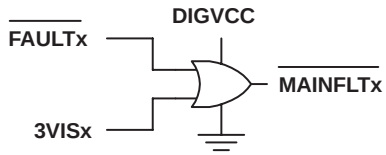


Figure 11. $\overline{\text{MAINFLT}}$ Output Signal

Force Enable Mode

In force enable mode, slots A and/or B can be forced to the enabled state. When in the force-enabled state and the associated SWA/B pin is low, V_{AUX} and the main power is enabled and the state of the VIOSEL signals are governed by the PCIXCAPA/B pin.

In this state, the slots cannot be controlled by other than SWx , but status (power controller outputs) is available from either the serial or parallel interface. Fault conditions cause the slot to be asynchronously powered down. Main power faults are cleared by deasserting the PWRENx signals. V_{AUX} power faults are cleared by deasserting SWA/B.

The force enable mode is typically used for manufacturing test or early product development when the hot-plug controller may not be functional due to software or hardware reasons. Force enable mode is selected by holding the PWRLEDA/B# pin low at the rising edge of PGOOD.

When the power controller is in serial mode, the BUSENA/B# and CLKENA/B# pins are asserted and the RESETA/B# pins follow the RSTA/B# signal. The M66EN pin is tri−stated and pulled up with 3.3V slot power. The ATTLEDA/B# pin is deasserted and the PWRLEDA/B# pin is asserted due to the external pulldown circuit. Should a power fault occur, power is shut down, the bus is disconnected (BUSENA/B# and CLKENA/B# pins are deasserted) and RESETA/B# is asserted.

APPLICATION INFORMATION

Possible Bus Condition

When the slot is powered off, there is the possibility that power from another part of the system could be applied to at least one of the slot voltages. External power applied to the slot holds the PWROFFx signal de-asserted. PWROFFx indicates that the slot power is off because slot voltages are below the comparator threshold. The PWRLED stays on signaling the operator that power has not been removed from the slot.

A parallel SCSI host bus adapter (HBA) without a TERMPOWER isolation diode is an example of a module that can cause this behavior. The parallel SCSI specification permits the host or other SCSI bus devices to supply TERMPOWER. In order to accommodate TERMPOWER supplied from multiple sources, each potential source is required (by parallel SCSI specifications) to have an isolation diode between the local power supply and the TERMPOWER signal. This prevents a direct wire connection between the system's different power supplies through the SCSI bus.

If the HBA manufacturer does not use the diode, and the slot is turned off, another SCSI device's TERMPOWER drives the slot's 3.3-V or more likely 5-V power.

A circuit like the timer Figure 12 can be used to indicate the module may be removed. $\overline{\text{PWROFFx}}$ is the TPS2342 $\overline{\text{PWROFFx}}$ signal and $\overline{\text{PWROFFx}}$ is the $\overline{\text{PWROFFx}}$ system destination. When PWRENx is off, the circuit waits two seconds. $\overline{\text{PWROFFx}}$ is de-asserted regardless of the condition of PWROFFx. The circuit should only be used if there is concern the slot may be exposed to a module that has a connection to other power supplies.

The feedback current through TPS2342 signal 5VIS is −90 mA or through 3VIS is −70 mA. This is less than a half watt which the TPS2342 is designed to dissipate during normal operation. If the slot is off and an operator is not available to remove the card no damage will result to the TPS2342.

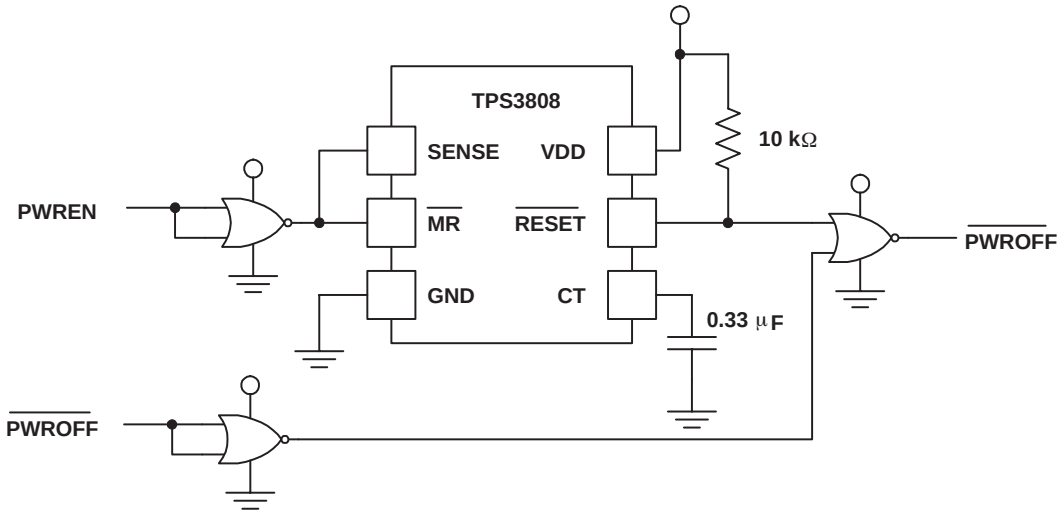


Figure 12. PWROFF Timeout Circuit

APPLICATION INFORMATION

−12 Volt Over-Current Response Time

For the −12-V supply only, a small over-current has a slower response time before turn off than a larger over-current. The comparator response time measured from the time the over-current is applied to the FAULT assertion is fixed at 4 μs typical. The turn off time of the −12 V is less than 10 μs at greater than 50% overload and approaches the comparator response time at 150% overload. Turn off time follows the graph Figure 13.

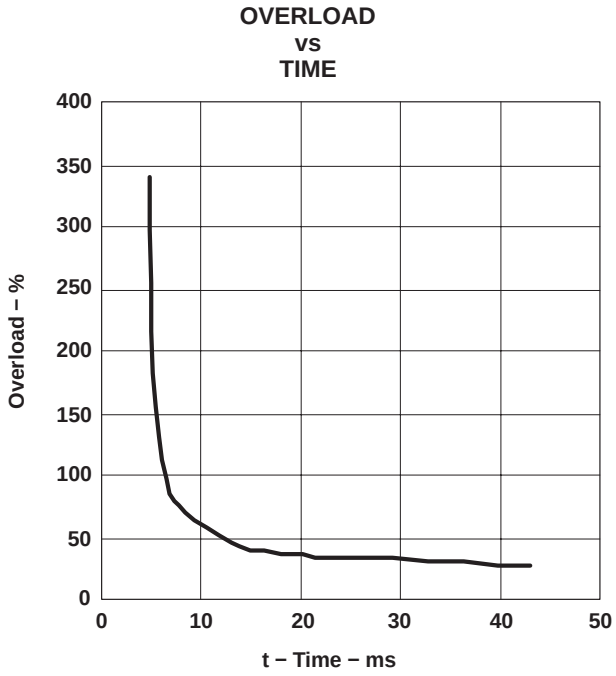


Figure 13

12−Volt Outputs

The 12-V and −12-V outputs share ramping circuits. In order to insure that the power MOSFET for the −12-V supply fully enhances, the tracking amplifier slews −12-V output 40% faster than the 12-V output. Reference the block diagram on page 3 and notice the resistor network between P12VOA/B and M12VOA/B. During the 12-V ramp delay, approximately 2 ms, there is 480-μA typical leakage current from the −12-V ramp to the positive output. With no load, the 12-V output is −0.7 V clamped by an internal ESD diode.

This condition is non destructive to the TPS2342. If desired, the 12-V output ramps from 0 V when the recommended 2.2-μF capacitor is connected between the 12-V output and GND.

APPLICATION INFORMATION

PCI−X Capability Selection

The PCI−X local bus 2.0 specification describes how the PCIXCAP pins program board operating mode using resistors on the board. The TPS2342 decodes the resistor values and communicates this to the slot controller using logic signals.

Five different operating modes are allowed under PCI−X 2.0. These modes are compatible with the three existing PCI and PCI−X 1.0 modes and add operation at 266 MHz and 533 MHz. The PCI−X 2.0 specification requires that PCIXCAP pins are pulled up to 3.3 V with a 3.3-kΩ, 5% resistor on the backplane or systemboard. This pull-up resistor combined with the resistor on the board creates a voltage divider as shown in the following table:

Table 5.

MODE	BUS SPEED	BOARD CONNECTION ON PCIXCAP PIN	PCIXCAP PIN NOMINAL VOLTAGE
PCI 2.2	33 MHz/66 MHz	ground	0 V
PCI−X 1.0	66 MHz	10 kΩ 1% to ground	2.481 V
PCI−X 1.0	133 MHz	open circuit	3.300 V
PCI−X 2.0	266 MHz	3.16 kΩ 1% to ground	1.614 V
PCI−X 2.0	533 MHz	1.02 kΩ 1% to ground	0.779 V

APPLICATION INFORMATION

The TPS2342 detects these five different modes using four comparators. These comparators have voltage thresholds between the nominal voltage points, as shown in the electrical characteristics table. These thresholds are proportional to DIGVCC voltage, so any supply variations are compensated by equivalent variation in the voltage thresholds. The voltage thresholds are far from the nominal voltage, so there is noise margin in mode selection. The table below shows these margins with a 3.3-kΩ, 5% pull-up resistor and the voltage threshold ranges shown in the electrical characteristic table.

Table 6.

MODE WINDOW	PCIXCAP VOLTAGE NOISE MARGIN
33 MHz to 533 MHz	0.279 V
533 MHz to 266 MHz	0.314 V
266 MHz to 66 MHz	0.331 V
66 MHz to 133 MHz	0.319 V

If the PCIXCAP feature is not used connect the PCIXCAPx input to the PCIXCAPx pin on slotx. The PCIXCAPx1,2,3 outputs can float. If the PCIXCAPx pin is not used on slotx, control the PCIXCAPx input to the TPS2342 by either pulling it up to DIGVCC with a 3.3-kΩ resistor or pulled down to ground with a 10-kΩ resistor or less.

In force enable mode, the PCIXCAPx level determines the VIO voltage selected.

PCIXCAP Outputs in Serial and Direct Mode

In serial mode, the serial interface communicates the state of the PCIXCAP resistances in six bits PCIXCAPxn, according to the table below. In direct mode PCIXCAPx1, PCIXCAPx2 and PCIXCAPx3 directly communicate the PCIXCAP resistances according to the table below.

Table 7.

MODE	BUS SPEED	PCIXCAPx1 (PINS 48, 13)	PCIXCAPx2 (PINS 46, 15)	PCIXCAPx3 (PINS 43, 18)
PCI 2.2	33 MHz/66 MHz	0	0	0
PCI−X 1.0	66 MHz	1	0	0
PCI−X 1.0	133 MHz	1	1	0
PCI−X 2.0	266 MHz	0	0	1
PCI−X 2.0	533 MHz	1	0	1

With PCIXCAPx = 0 V, the slot is operating in PCI 2.2 mode. In PCI 2.2 mode, the M66EN bit selects between 33 MHz and 66 MHz. Connect the slot M66EN signal to the TPS2342 M66EN signal.

APPLICATION INFORMATION

Power Stage Design

Adapter card current is a combination of static adapter card current consumption plus inrush current caused by the supply voltage ramping into the adapter card decoupling capacitance. The TPS2342 implements current limiting on each supply. For the 15VIO, 5 V and 3.3 V supplies, user-supplied 6-mΩ resistors sense current. For the other supplies, current sense resistors are integrated into the TPS2342. The current sense thresholds of the 5-V, 3.3-V, 12-V, and –12-V supplies are programmed by one user-supplied resistor connected from MISET to ground. The TPS2342 implements slew-rate control using on-chip current sources and user-supplied capacitors. On each slot, one capacitor sets the slew rate for the 5-V, 3.3-V, and Vio supplies, a second capacitor set the slew rate for the 12-V and –12-V supplies, and a third capacitor sets the slew rate for the 3.3-V_{AUX} supply.

Using the recommended current sense-resistors, current-threshold resistor, and slew-rate control capacitors implements a system with slew rates that meet PCI specifications and can deliver power to any adapter card that meets PCI specifications. If a unique adapter card produces premature current limiting with the recommended programming components, current-limit thresholds can be increased by increasing the value of the resistor connected to MISET or inrush current can be reduced by raising the value of the appropriate slew-rate control capacitors.

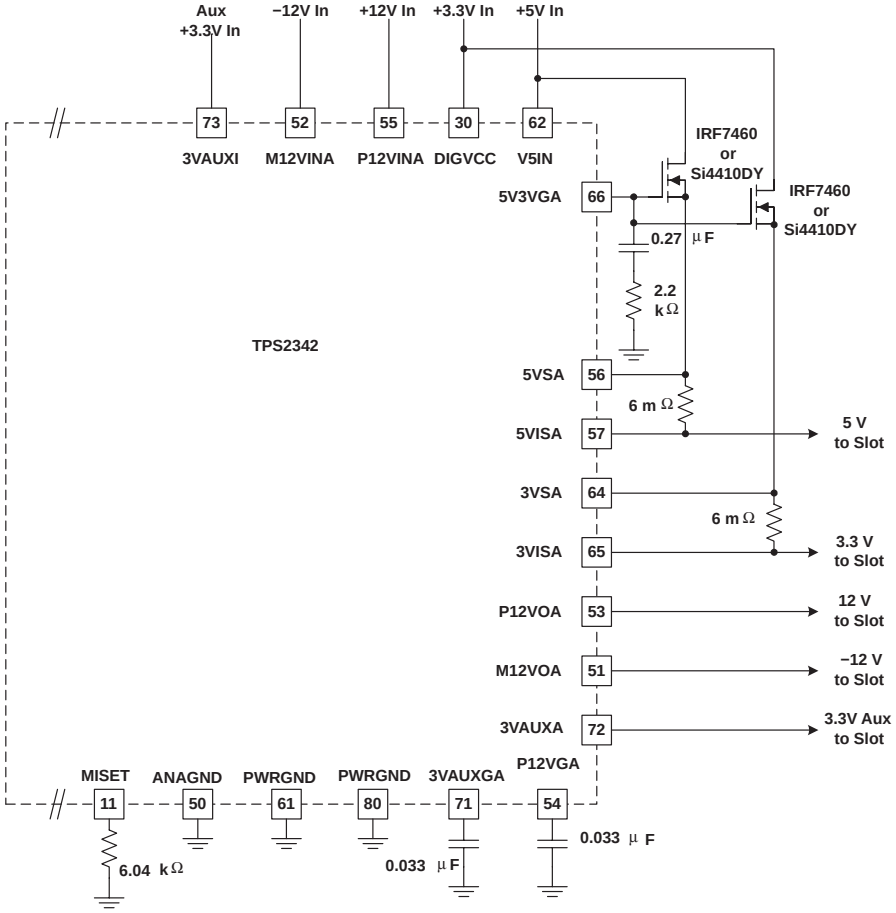


Figure 14. Typical TPS2342 Application Showing Power, Slew-Rate Control and Current-Limit Programming Components for One Slot

APPLICATION INFORMATION

V_{IO} Power Selection

PCI−X local bus specification revision 2.0 requires that V_{IO} be 3.3 V when the slot is operating in 33-MHz, 66-MHz, or 133-MHz modes and 1.5 V when the slot is operating in 266-MHz or 533-MHz modes. The TPS2342 provides signals to drive external power FETs to select between 3.3 V and 1.5 V for V_{IO}.

To prevent body-diode conduction from the 3.3-V supply to the 1.5-V supply when 3.3 V is delivered to V_{IO}, the 1.5-V V_{IO} switch must be implemented as two power FETs wired in blocking series connection, as shown below. To minimize voltage loss, very low on-resistance power FETs are required (IRF1302S or Si4430DY). It is helpful to anticipate the voltage drop in the power FETs and adjust the 1.5-V V_{IO} power source for slightly greater than 1.5 V, for example 1.55 V ±25 mV. This circuit shows how to generate drive to the two power FETs from the VIOG and 5V3VG signals.

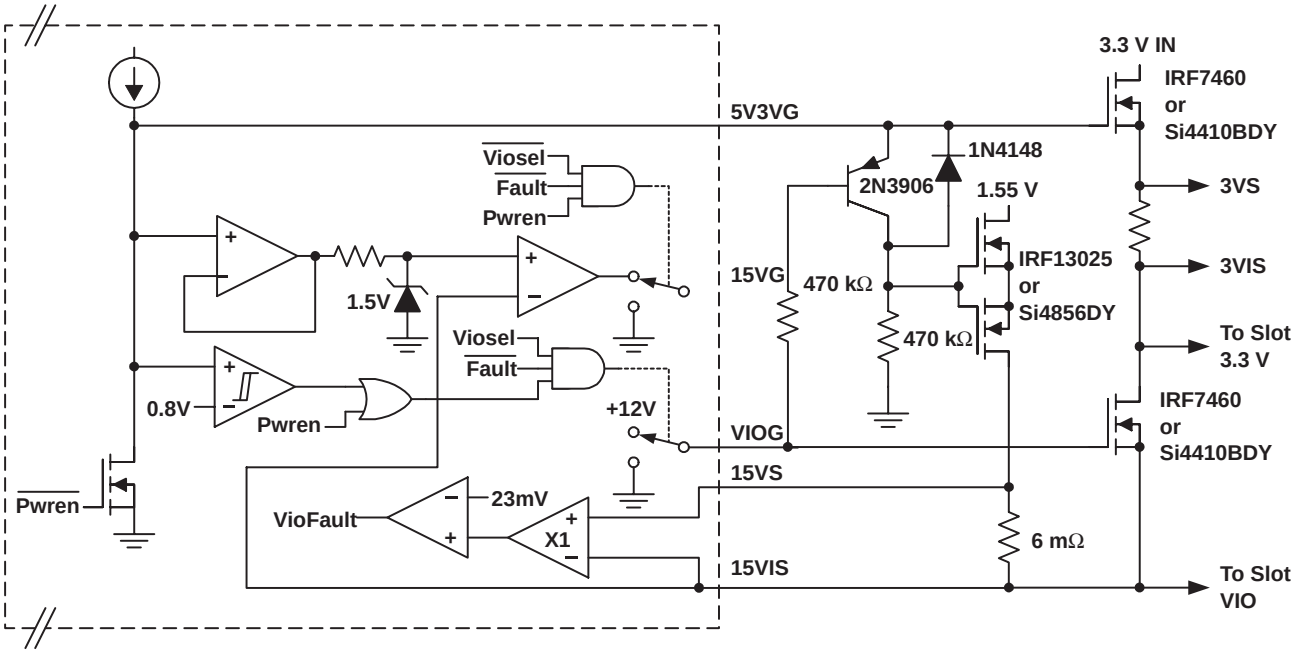


Figure 15. V_{IO} Block Diagram for Use With External FETs and $V_{IO(in)}$ = 1.55 V

Alternately, the 1.5-V V_{IO} input supply can be significantly higher than 1.5 V, for example, 1.8 V. If the power provided to the 1.5-V power FETs is greater than 1.54 V, the TPS2342 reduces the gate voltage to the 1.5-V power FETs to linearly regulate power to slot V_{IO} to approximately 1.5 V. The advantage of driving 1.5-V V_{IO} input with 1.8 V is that the power FET $R_{DS(on)}$ requirements are reduced and the total voltage drop budget is higher. The disadvantage is that the power dissipation in the 1.5-V V_{IO} power FETs is larger.

PCI specifications limit the adapter card V_{IO} capacitance to 150 µF. Depending on choice of power FETs and capacitance on the adapter card, it may improve transient response to add a 0.0047-µF capacitor from VIOG to PWRGND and/or to add a 10-µF capacitor from V_{IO} to ground on the system board.

APPLICATION INFORMATION

The 1.5-V V_{IO} drive is current limited by the 15VS/15VISx comparator while the 3.3-V V_{IO} drive is current limited by the main 3VS/3VISx comparator. This allows selection of the 1.5-V current limit point independently of the 3.3-V current limit point. The MISET programming resistor has no effect on the V_{IO} current limit threshold.

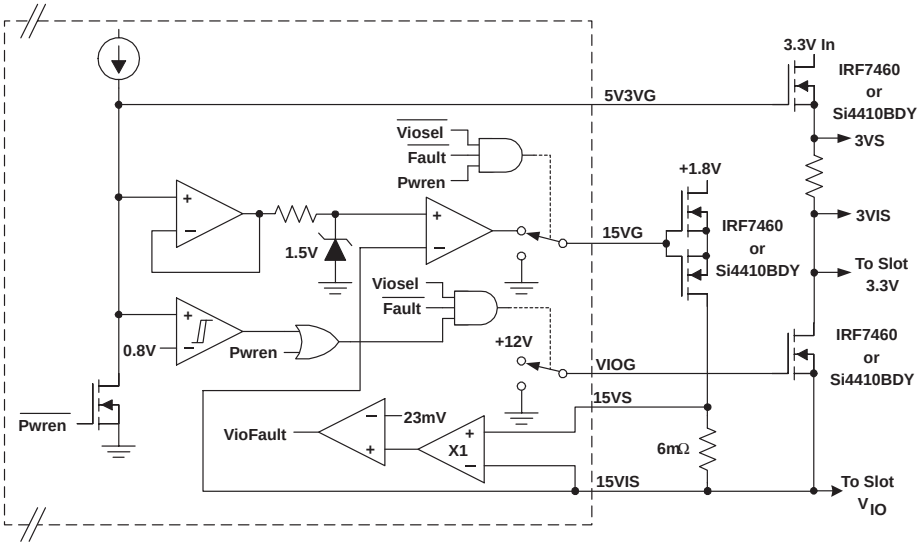


Figure 16. V_{IO} Block Diagram for use with External FETs and $V_{IO(in)}$ = 1.8 V

The TPS2342 can be used with an external V_{IO} voltage regulator module (VRM). This is valuable in cases where a low voltage power supply for V_{IO} is not available. One supply can be used to generate either 1.5 V or 3.3 V based on the output of the 15VG and VIOG signals. The exact configuration of this is dependent on the programming inputs of the VRM, but a typical implementation with the PTH05000W is shown below. The PTH05000W has a shutdown input and programming input, so the 15VG and VIOG signals are shown going to low cost transistors and diodes to drive these signals.

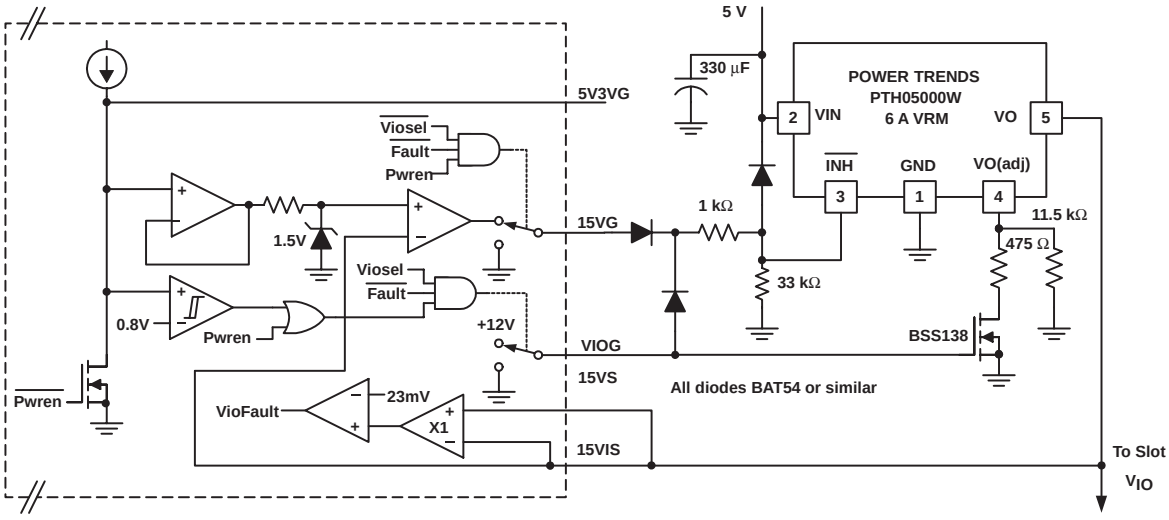


Figure 17. V_{IO} Block Diagram For Use With An External Voltage Regulator Module (VRM)

If 1.5-V VIO is not used, connect both 15VSx and 15VISx to 3.3 V. This prevents floating inputs and false over-current detection.

APPLICATION INFORMATION

Power Cycling and $\overline{PME}$

The PCI power management specification defines a signal called $\overline{PME}$ (power management event) to allow requests for power state changes to be communicated from the slot back to the system. The TPS2342 provides a slot-specific $\overline{PMEx}$ input and a gated $\overline{PMEOx}$ output that can be monitored by the system. The gated $\overline{PMEOx}$ output is enabled a delay after the SWx slot switch closes (SWx low) as shown in the timing diagram below. The purpose of the delay is to ensure that 3.3-V_{AUX} power is stable to the slot before connecting $\overline{PMEx}$ the signal.

> **NOTE:** If the $\overline{PMEx}$ signal was presented to the system while 3.3-V_{AUX} power was still ramping up, a false trigger could result.

The 3.3-V_{AUX} circuitry provides over current fault detection. In the event of an over current fault on V_{AUX}, the slot 3.3-V_{AUX} and $\overline{PME}$ signals are immediately disconnected. The fault state is latched internally in the TPS2342 and is cleared either by opening the SWx slot switch or by removing the 3.3-V_{AUX} power to the TPS2342.

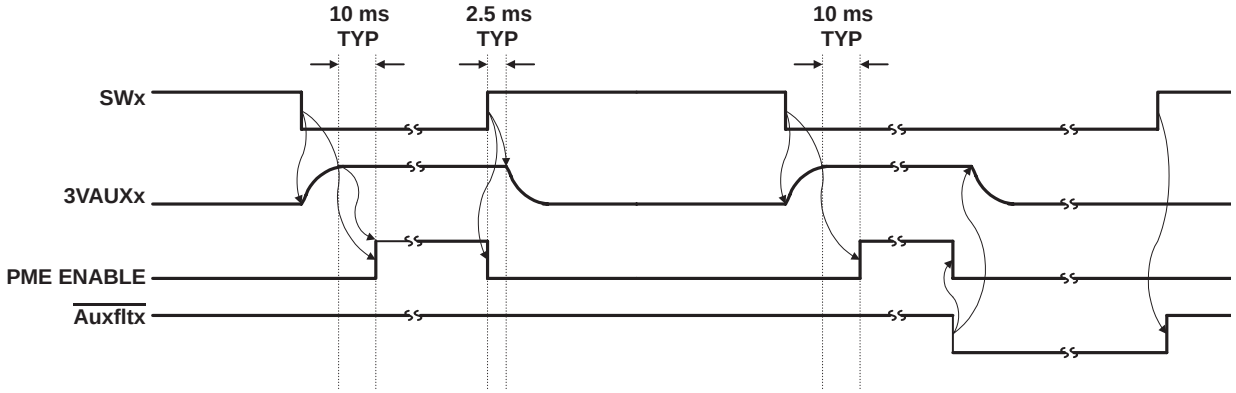


Figure 18.

V_{AUX} and PME Gating

When SWx is closed (low), 3VAUXx power is immediately applied to the slot with controlled slew rate, minimizing inrush current into 3VAUXx bypass capacitors. After 3VAUXx power completes ramping up, a delay timer starts. At the end of the delay timer cycle, the $\overline{PMEx}$ enable switches close, allowing connection of the $\overline{PMEx}$ signal to the $\overline{PMEOx}$ output. Multiple $\overline{PMEOx}$ output pins can be connected to the same node, creating a $\overline{PME}$ bus that can be connected to a master system interrupt input.

When SWx is opened (high) or if there is a power fault on slot x, the $\overline{PMEx}$ enable switch for that slot is immediately opened and the 3VAUXx power for that slot is removed. Although these events happen at approximately the same time, the 3VAUXx power should remain high until the $\overline{PMEx}$ switch is open so that falling 3VAUXx power does not cause a nuisance $\overline{PMEx}$ interrupt. To insure that 3VAUXx remains high during a power fault, 3VAUXx should have a bypass capacitance of at least 20 μF. If the capacitor is not available on the inserted card, it should be provided on the system board.

The PME circuit operates independently of any of the main power supplies.

TYPICAL CHARACTERISTICS

OUTPUT TURN OFF AND PWROFF

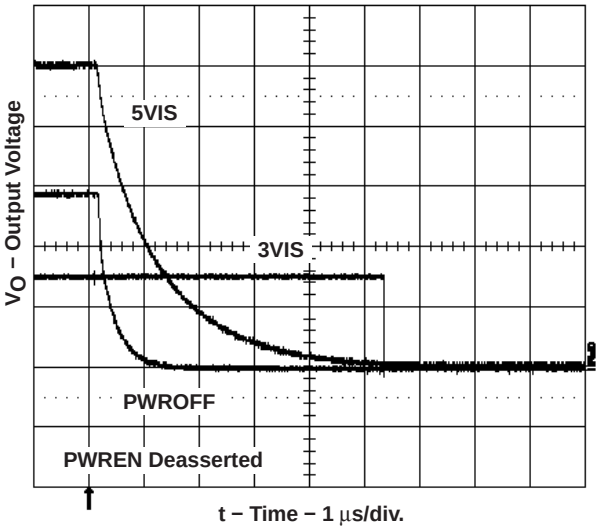


Figure 19

OUTPUT TURN ON AND PWREN

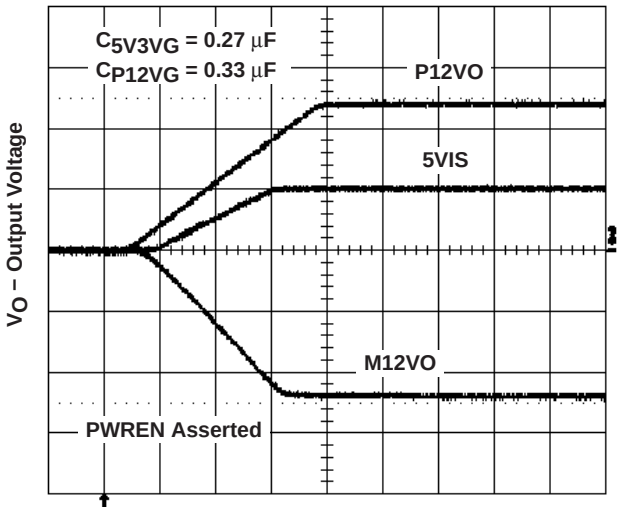


Figure 20

P12V0 ON 12 V OVER CURRENT CONDITION

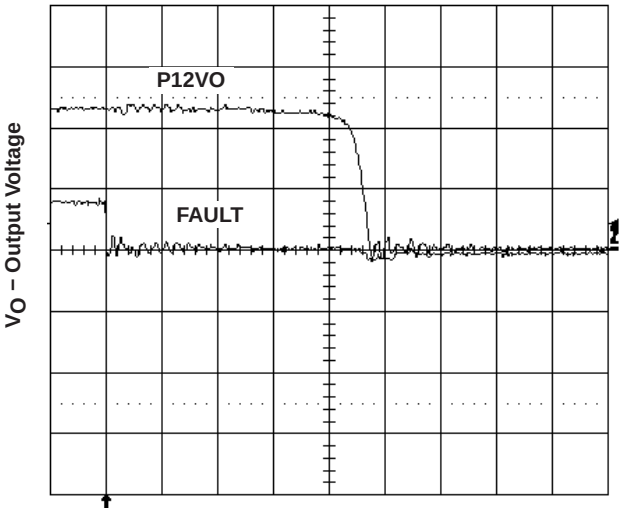


Figure 21

−12 OUTPUT AND FAULT ON P12V OVER CURRENT

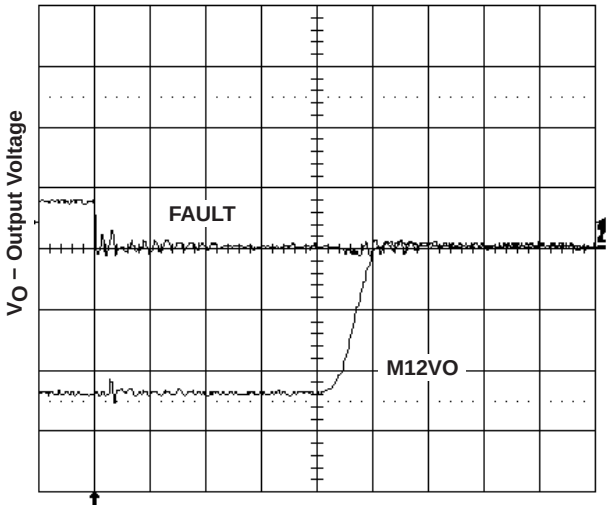


Figure 22

TYPICAL CHARACTERISTICS

12 V AND −12 V OUTPUT AND PWROFF FROM PWREN DEASSERTED

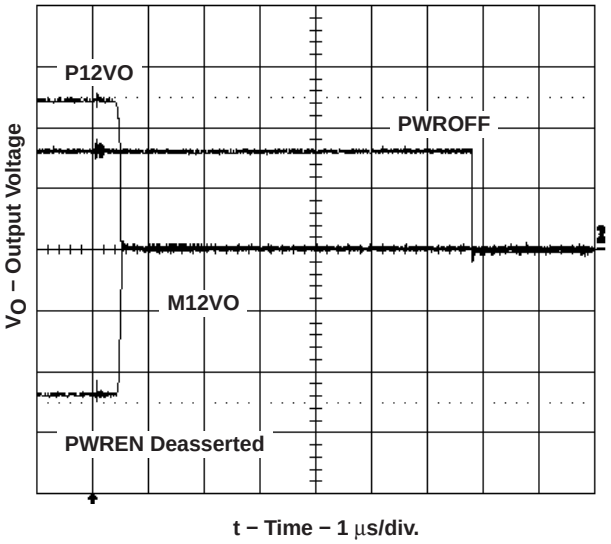


Figure 23

3.3 V AND FAULT RESPONSE TO P12V OVER CURRENT

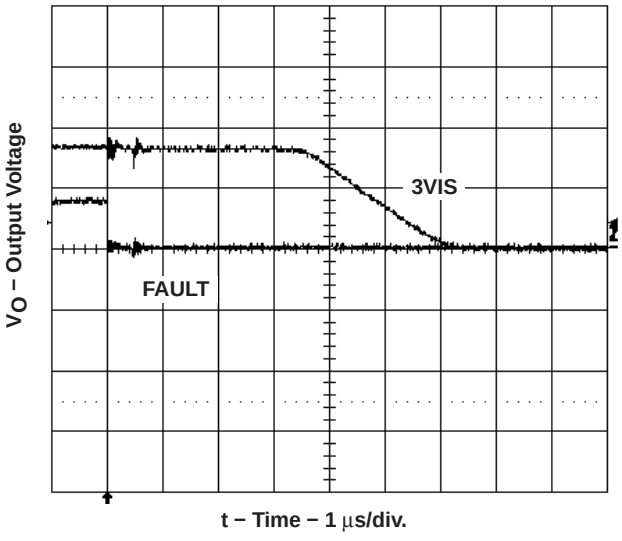


Figure 24

VAUXO AND VAUXG ON SW ASSERTED

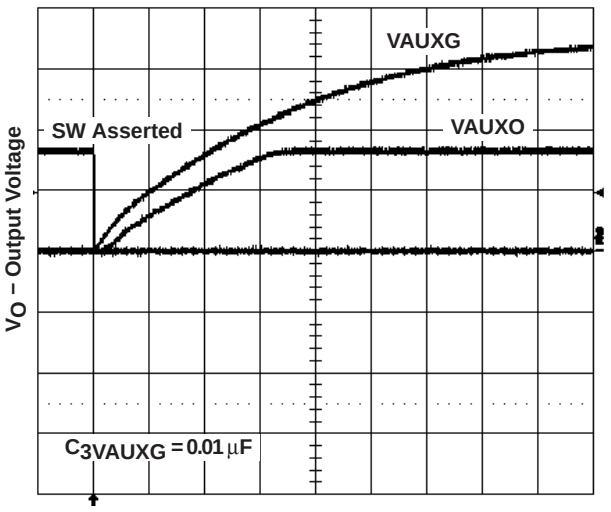


Figure 25

VAUX OUTPUT AND VAUXG ON VAUX FAULT

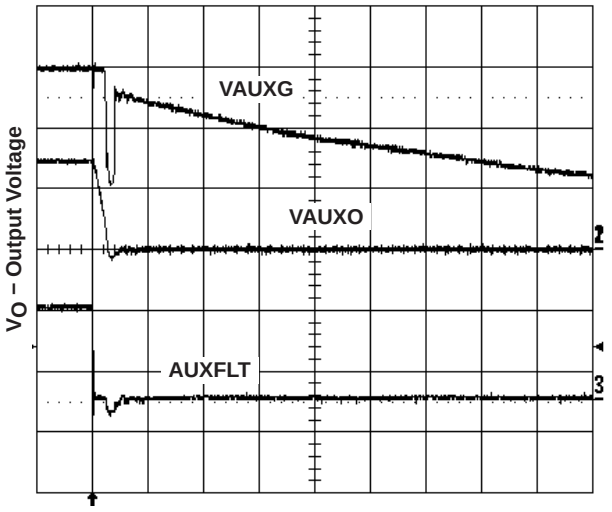


Figure 26

TYPICAL CHARACTERISTICS

5VIS UNDER VOLTAGE RESPONSE

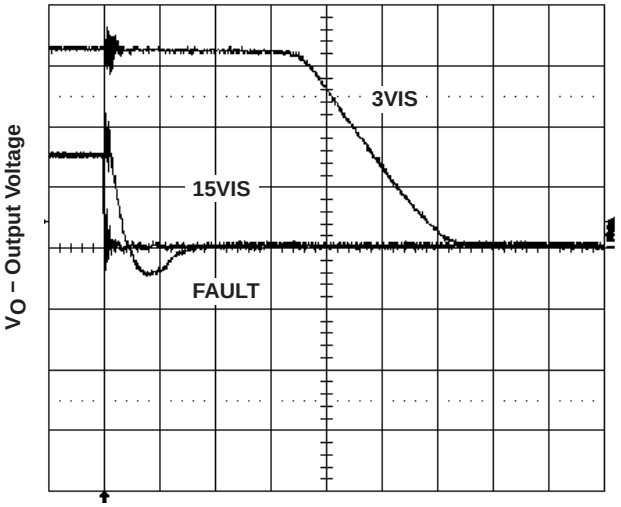


Figure 27

VAUXO AND VAUXG ON SW DE-ASSERTED

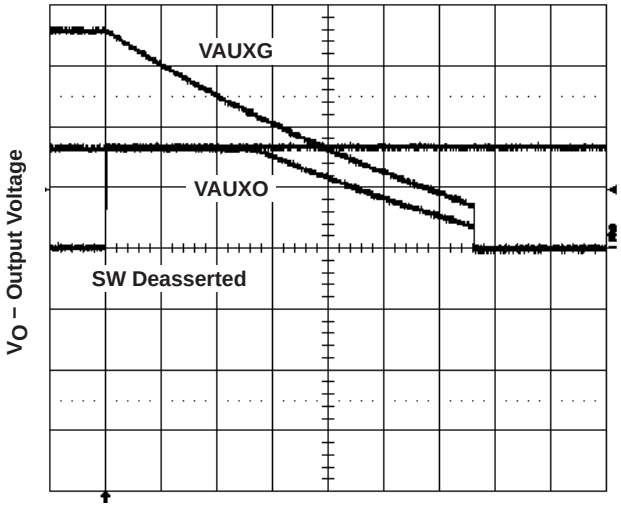


Figure 28

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2342PFP	OBSOLETE	HTQFP	PFP	80		TBD	Call TI	Call TI	-40 to 85	TPS2342PFP	
TPS2342PFPG4	OBSOLETE	HTQFP	PFP	80		TBD	Call TI	Call TI	-40 to 85		
TPS2342PFPR	ACTIVE	HTQFP	PFP	80		TBD	Call TI	Call TI	-40 to 85	TPS2342PFP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

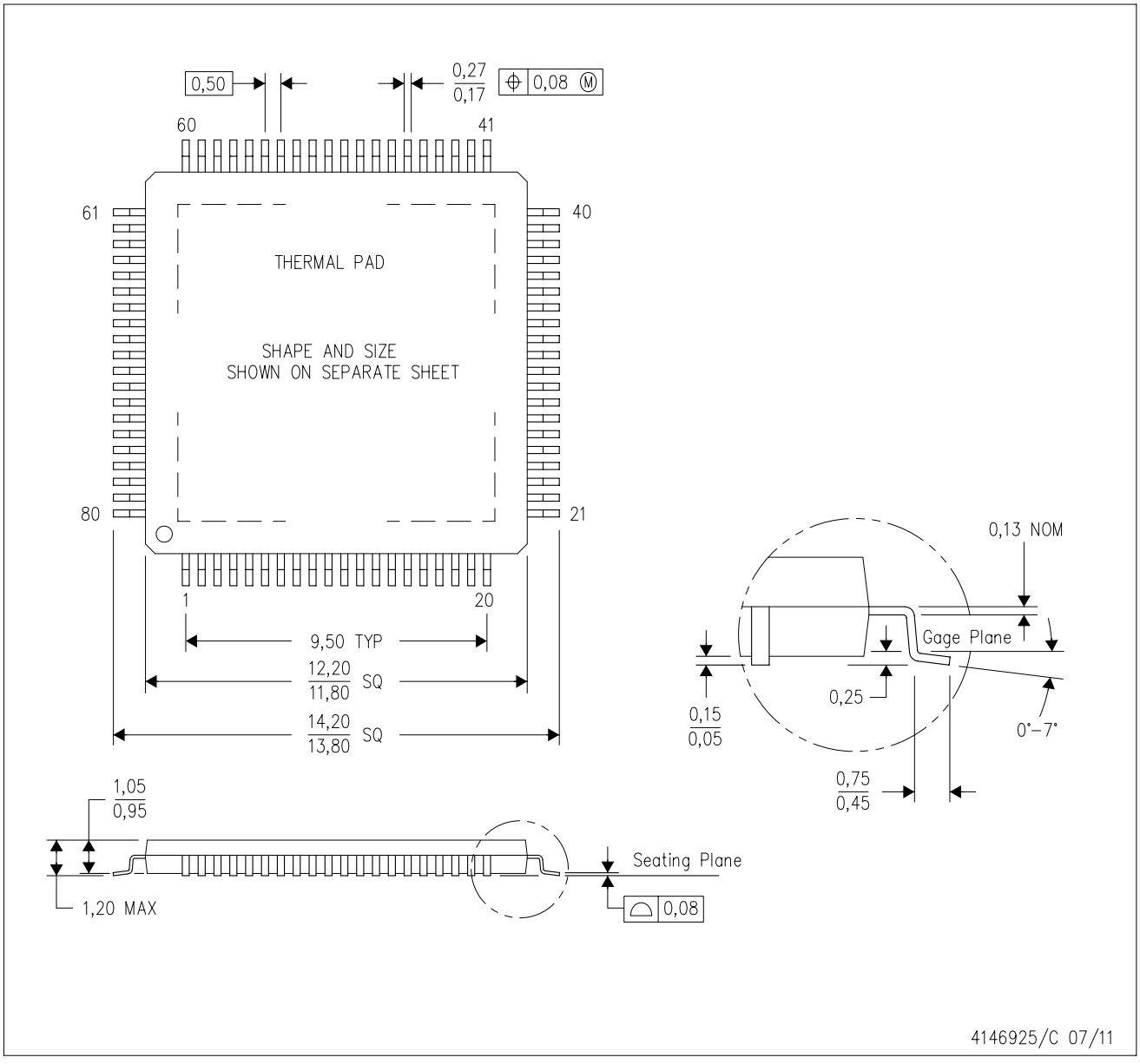
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS–026

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