TPS6105x High-Power White LED Driver 2-mHz Synchronous Boost Converter With Standard Logic Interface

1 Features

- Four Operational Modes
  - Torch and Flash up to I_{LED} = 700 mA
  - Voltage-Regulated Boost Converter: 5.0 V
  - Shutdown: 0.3 µA (Typical)
- Total Solution Circuit Area < 25 mm^2
- Up to 96% Efficiency
- Integrated LED Turnon Safety Timer
- Zero Latency TX-Masking Input
- Integrated Low Light Dimming Mode
- LED Disconnect During Shutdown
- Open/Shorted LED Protection
- Over-Temperature Protection
- Available in a 12-Pin NanoFree™ (CSP) and 10-Pin VSON Packaging

2 Applications

- Camera White LED Torch or Flash for Cell Phones, Smartphones and PDAs
- General Lighting Applications
- Audio Amplifier Power Supply

3 Description

The TPS6105x device uses a high-frequency synchronous-boost topology with constant current sink to drive single white LEDs. The device uses an inductive fixed-frequency PWM control scheme using small external components, minimizing input ripple current.

The 2-MHz switching frequency allows the use of small and low-profile 2.2-µH inductors. To optimize overall efficiency, the device operates with only a 250-mV LED feedback voltage.

The TPS6105x device not only operates as a regulated current source, but also as a standard voltage-boost regulator. This additional operating mode can be useful to supply other high-power devices in the system, such as a hands-free audio power amplifier, or any other component requiring a supply voltage higher than the battery voltage.

The LED current or the desired output voltage can be programmed through two logic signals (MODE0/1). To simplify flash synchronization with the camera module, the device offers a trigger pin (FLASH_SYNC) for fast LED turnon time.

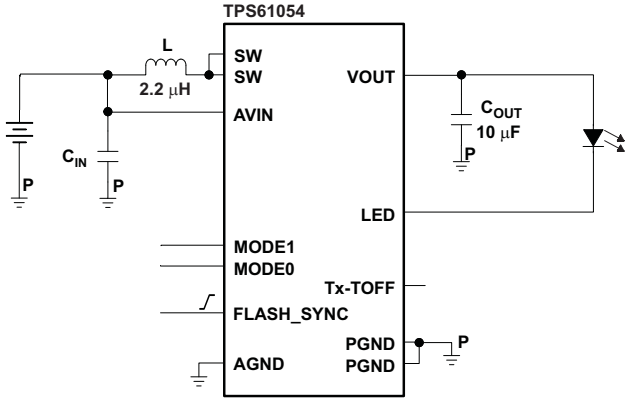
When the TPS6105x is not in use, it can be put into shutdown mode, reducing the input current to 0.3 µA (typical). During shutdown, the LED pin is high impedance to avoid leakage current through the LED.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61054, TPS61055	VSON (10)	3.00 mm × 3.00 mm
	DSBGA (12)	1.96 mm × 1.46 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2008) to Revision B **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Package Summary* section ... 21

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5 Device Options

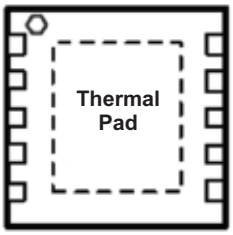
PART NUMBER(1)(2)	TORCH CURRENT(3)	FLASH CURRENT(3)	SAFETY TIMER MAXIMUM DURATION	CURRENT LIMIT
TPS61054DRC	75 mA	700 mA	820 ms	1500 mA (ILIM = 01)
TPS61055DRC	75 mA	500 mA	820 ms	1000 mA (ILIM = 00)

(1) All devices are specified for operation in the commercial temperature range, –40°C to 85°C
(2) The YZG package is available in tape and reel. Add R suffix (TPS6105xYZGR, TPS6105xDRCR) to order quantities of 3000 parts. Add T suffix (TPS6105xDRCT) to order quantities of 250 parts.
(3) For customized current settings, please contact the factory.

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6 Pin Configuration and Functions

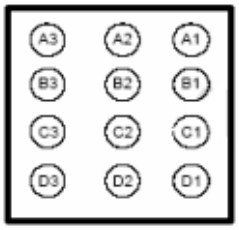
DRC Package
10-Pin VSON
Top View



YZG Package
12-Pin DSBGA
Top View



YZG Package
12-Pin DSBGA
Bottom View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	VSON	DSBGA		
AVIN	5	D3	I	This is the input voltage pin of the device. Connect directly to the input bypass capacitor.
VOUT	9	A2	O	Boost converter output.
LED	6	D2	I	LED return input. This feedback pin regulates the LED current through the internal sense resistor by regulating the voltage across it. The regulation operates with typically 250-mV dropout voltage. Connect to the cathode of the LED.
FLASH_SYNC	10	A1	I	Flash strobe pulse synchronization input.
				FLASH_SYNC = LOW (GND): The device is operating and regulating the LED current to the torch current level (TC).
				FLASH_SYNC = HIGH (VIN): The device is operating and regulating the LED current to the flash current level (FC).
MODE0	2	B3	I	Mode selection inputs. These pins must not be left floating and must be terminated.
				MODE0 = 0, MODE1 = 0: Device in shutdown mode
MODE1	1	A3		MODE0 = 1, MODE1 = 0: Device in torch only mode
				MODE0 = 0, MODE1 = 1: Device in torch and flash mode
				MODE0 = 1, MODE1 = 1: Device in constant voltage regulation mode
Tx-TOFF	3	C3	I	RF PA synchronization input.
				Tx-TOFF = LOW : The device is operating normally.
				Tx-TOFF = HIGH : The device is forced into torch mode.
SW	8	B1, B2	I/O	Inductor connection. Drain of the internal power MOSFET. Connect to the switched side of the inductor. SW is high impedance during shutdown.
PGND	7	C1, C2	—	Power ground. Connect to AGND underneath IC.
AGND	4	D1	—	Analog ground.
Thermal Pad	—	N/A	—	Internally connected to PGND.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
	Voltage on AVIN, VOUT, SW, LED(2)	–0.3	7	V
	Voltage on MODE0, MODE1, FLASH_SYNC, Tx-TOFF(2)	–0.3	7	V
T_A	Operating ambient temperature(3)	–40	85	°C
$T_{J\ (MAX)}$	Maximum operating junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A(max)} = T_{J(max)} - (R_{\theta JA} \times P_{D(max)})$.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±1000	
		Machine Model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.5	3.6	6	V
V_{OUT}	Output voltage range in current regulator mode	V_{IN}		5.5	V
	Output voltage range in voltage regulator mode	4.5	5	5.25	V
L	Inductance effective value range	1.3	2.2	2.9	µH
C_{IN}	Input capacitance range		10		µF
C_{OUT}	Input capacitance effective value range	3	10	50	µF
T_J	Operating junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS61054, TPS61055		UNIT
		DRC (VSON)	YZG (DSBGA)	
		10 PINS	12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48.5	82.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.4	0.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.0	35.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	2.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.1	19.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.3	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

Unless otherwise noted the specification applies for V_{IN} = 3.6 V over an operating junction temperature of –40°C ≤ T_J ≤ 125°C. Typical values are for T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage range		2.5		6	V
	Minimum input voltage for start-up	MODE0 = 1, MODE1 = 1, R_L = 10 Ω			2.5	V
I_Q	Operating quiescent current into AVIN	MODE0 = 1, MODE1 = 1		8.5		mA
I_{SD}	Shutdown current into AVIN	MODE0 = 0, MODE1 = 0, –40°C ≤ T_J ≤ 85°C		0.3	3	µA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling		2.3	2.4	V
OUTPUT						
V_{OUT}	Output voltage range	Current regulator mode	V_{IN}		5.5	V
		Voltage regulator mode		5		
OVP	OVP Output overvoltage protection	V_{OUT} rising	5.7	6	6.25	V
	Output overvoltage protection hysterisis			0.15		V
D	Minimum duty cycle			7.5%		
	LED current accuracy(1)	0.25 V ≤ V_{LED} ≤ 2.0 V, I_{LED} = I_{TORCH}, T_J = 50°C	–15%		15%	
		0.25 V ≤ V_{LED} ≤ 2.0 V, I_{LED} = I_{FLASH}, T_J = 50°C	–12%		12%	
	LED current temperature coefficient			0.08		%/°C
	DC output voltage accuracy	2.5 V ≤ V_{IN} ≤ 0.9 V_{OUT}, PWM operation	–3%		3%	
V_{LED}	LED sense voltage	Boost Mode		250		mV
	LED input leakage current	V_{LED} = V_{OUT} = 5 V, –40°C ≤ T_J ≤ 85°C		0.1	1	µA
POWER SWITCH						
$r_{DS(on)}$	Switch MOSFET on-resistance	V_{OUT} = V_{GS} = 3.6 V		80		mΩ
	Rectifier MOSFET on-resistance			80		
$I_{lkg(SW)}$	Switch MOSFET leakage	V_{DS} = 6.0 V, –40°C ≤ T_J ≤ 85°C		0.1	1	µA
	Rectifier MOSFET leakage			0.1	1	
I_{lim}	Switch current limit	2.5 V ≤ V_{IN} ≤ 6.0 V, ILIM = 00	850	1000	1150	mA
		2.5 V ≤ V_{IN} ≤ 6.0 V, ILIM = 01 (1)	1275	1500	1725	
	Thermal shutdown(1)		140	160		°C
	Thermal shutdown hysteresis(1)			20		°C
OSCILLATOR						
f_{SW}	Oscillator frequency		1.8	2.0	2.2	MHz
MODE0, MODE1, Tx-TOFF, FLASH_SYNC						
$V_{(IH)}$	High-level input voltage		1.2			V
$V_{(IL)}$	Low-level input voltage				0.4	V
$I_{(LKG)}$	Logic input leakage current	Input connected to V_{IN} or GND, –40°C ≤ T_J ≤ 85°C		0.01	0.1	µA
	Tx-TOFF pulldown resistance	Tx-TOFF ≤ 0.4 V		400		kΩ
	FLASH_SYNC pulldown resistance	FLASH_SYNC ≤ 0.4 V		400		kΩ
TIMING						
	Start-up time	From shutdown into flash mode I_{LED} = 700 mA		1.2		ms
		From shutdown into voltage mode MODE0 = 1, MODE1 = 1, I_{OUT} = 0 mA		650		µs
	LED current settling time(2) triggered by rising edge on FLASH_SYNC	MODE0 = 0, MODE1 = 1, I_{LED} = from 75mA to 700 mA		160		µs
	LED current settling time(2) triggered by rising edge on Tx-TOFF	MODE0 = 0, MODE1 = 1, I_{LED} = 700 mA to 75 mA		20		µs

(1) Assured by design. Not tested in production.
(2) Settling time to ±15% of the target value

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7.6 Typical Characteristics

Table 1. Table of Graphs

		FIGURE
LED Power Efficiency	vs. Input Voltage	Figure 1, Figure 2
DC Input Current	vs. Input Voltage	Figure 3
LED Current	vs. LED Pin Headroom Voltage	Figure 4
Voltage Mode Efficiency	vs. Output Current	Figure 5
DC Output Voltage	vs. Load Current	Figure 6
DC Output Voltage	vs. Input Voltage	Figure 7
Quiescent Current	vs. Input Voltage	Figure 8
Shutdown Current	vs. Input Voltage	Figure 9
Junction Temperature	vs. GPIO Voltage	Figure 10

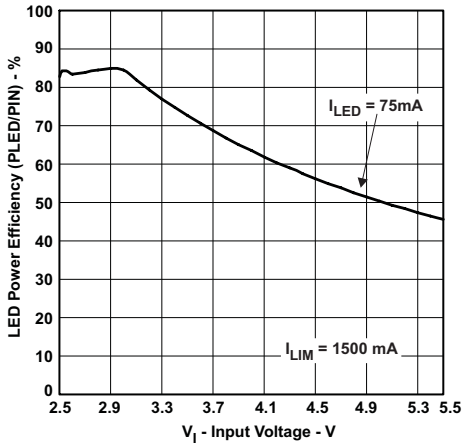


Figure 1. LED Power Efficiency vs Input Voltage

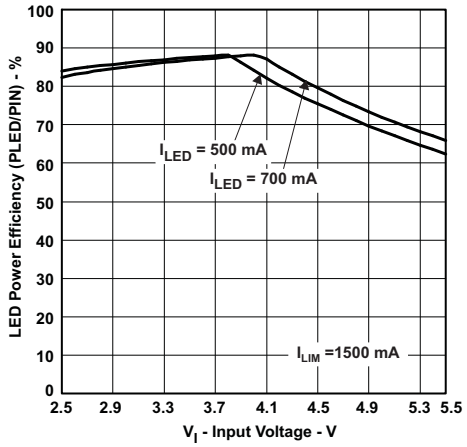


Figure 2. LED Power Efficiency vs Input Voltage

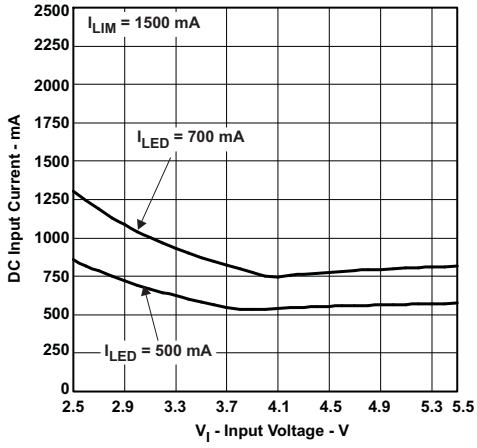


Figure 3. DC Input Current vs Input Voltage

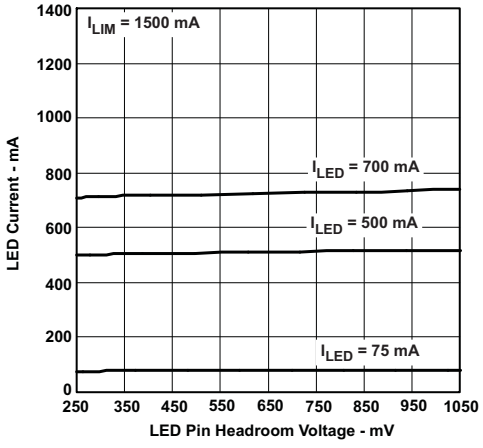


Figure 4. LED Current vs LED Pin Headroom Voltage

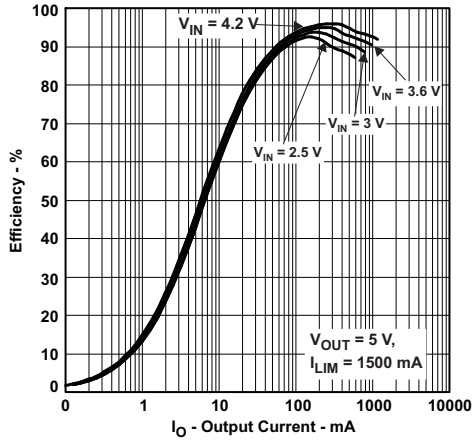


Figure 5. Voltage Mode Efficiency vs Load Current

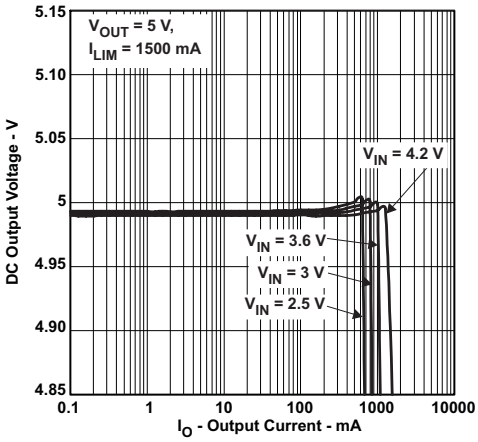


Figure 6. DC Output Voltage vs Output Current

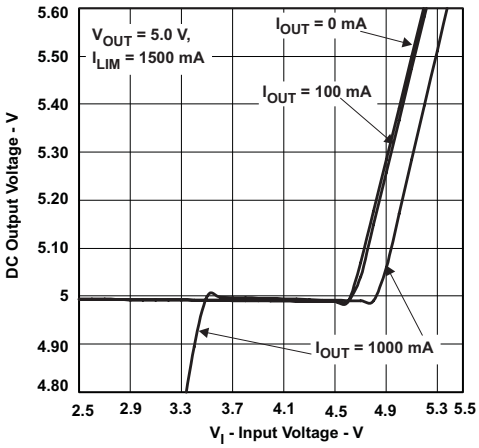


Figure 7. DC Output Voltage vs Input Voltage

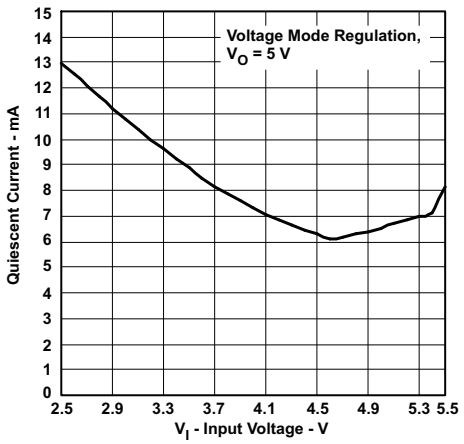


Figure 8. Quiescent Current Vs Input Voltage

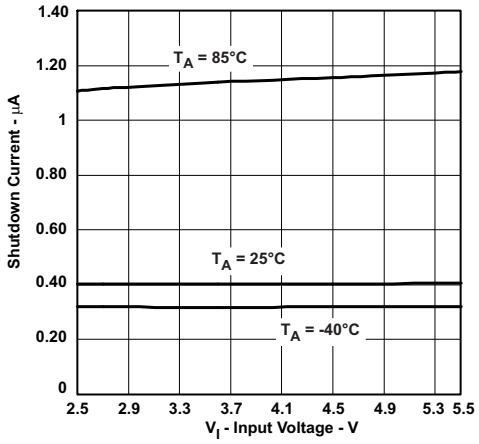


Figure 9. Shutdown Current vs Input Voltage

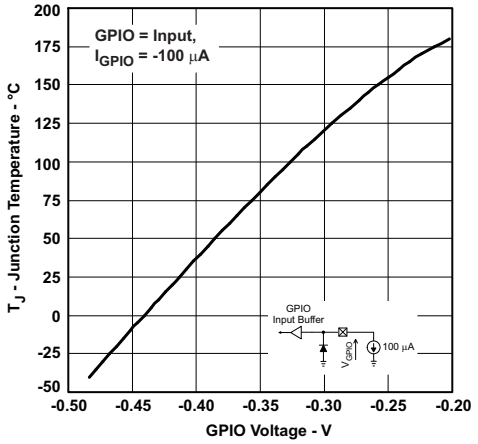
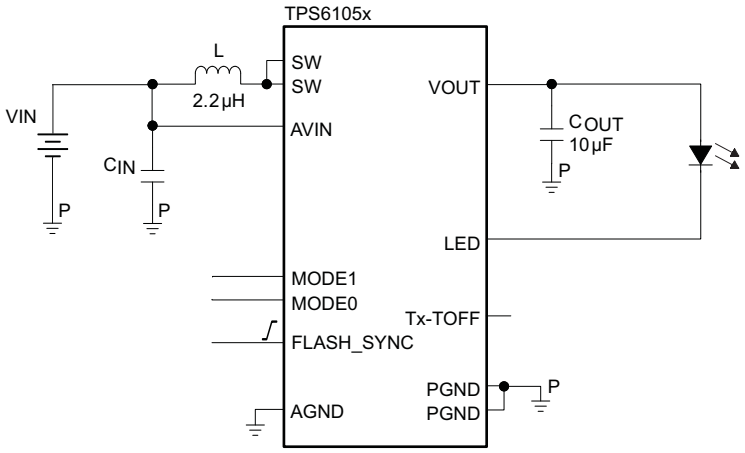


Figure 10. Junction Temperature vs GPIO Voltage

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8 Parameter Measurement Information



List Of Components:
- L = Wuerth Elektronik WE-PD S Series
- C_{IN} = C_{OUT} = TDK C1605X5R0J106MT

Figure 11. Parameter Measurement Circuit

9 Detailed Description

9.1 Overview

The TPS6105x family employs a 2-MHz constant-frequency, current-mode PWM converter to generate the output voltage required to drive high-power LEDs. The device integrates a power stage based on an NMOS switch and a synchronous NMOS rectifier. The device also implements a linear low-side current regulator to control the LED current when the battery voltage is higher than the diode forward voltage.

9.2 Functional Block Diagrams

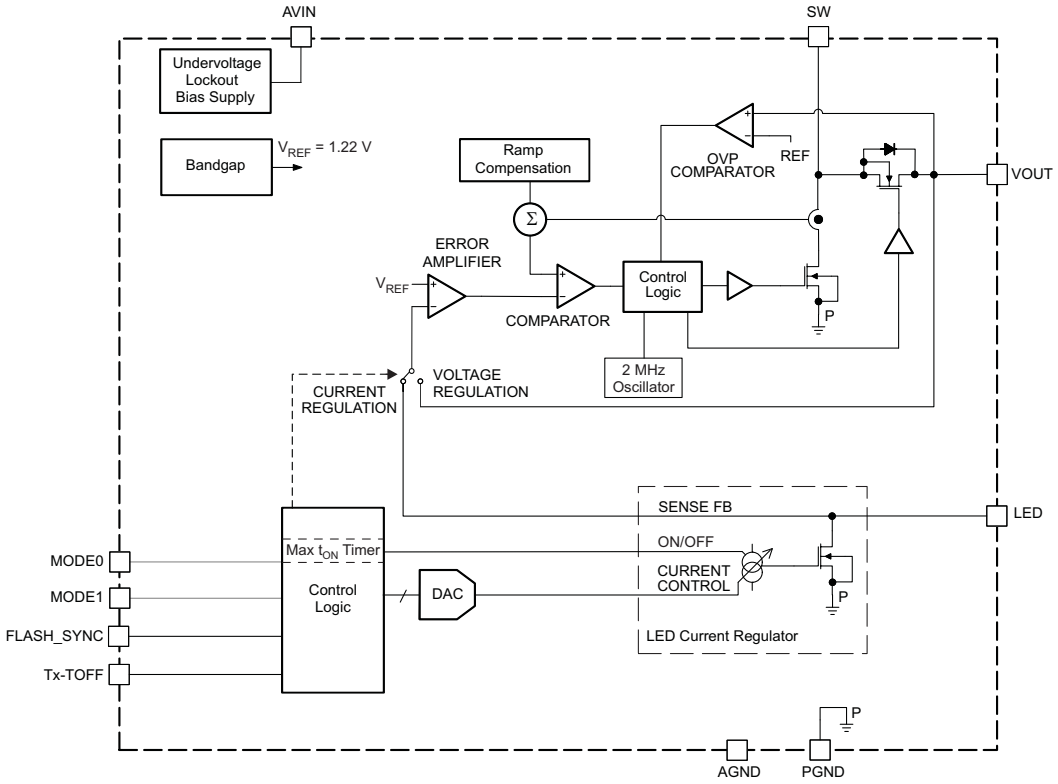


Figure 12. Functional Block Diagram of TPS6105x

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Functional Block Diagrams (continued)

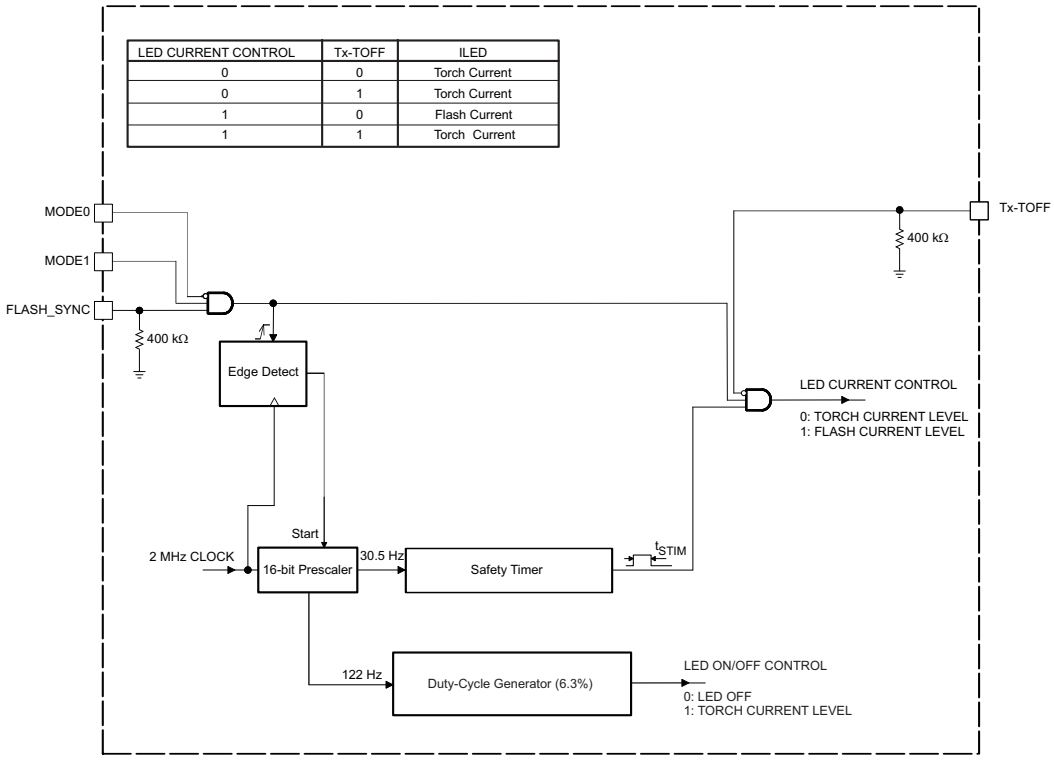


Figure 13. Timer Block Diagram of TPS6105x

9.3 Feature Description

9.3.1 Operation

In boost mode, the duty cycle of the converter is set by the error amplifier and the saw-tooth ramp applied to the comparator. Because the control architecture is based on a current-mode control, a compensation ramp is added to allow stable operation at duty cycles larger than 50%. The converter is a fully-integrated synchronous-boost converter, always operating in continuous-conduction mode. This allows low-noise operation, and avoids ringing on the switch pin, which would be seen on a converter when entering discontinuous-conduction mode.

The TPS6105x device not only operates as a regulated current source but also as a standard voltage-boost regulator. This additional operating mode can be useful to properly synchronize the converter when supplying other high-power devices in the system, such as a hands-free audio power amplifier, or any other component requiring a supply voltage higher than the battery voltage.

The mode of operation (shutdown, torch and flash modes, constant voltage regulation) selection is done through the MODE0/1 control inputs.

Table 2. TPS6105x Operating Modes

MODE1	MODE0	OPERATING MODES
0	0	Power stage is in shutdown. The output is either connected directly to the battery through the body diode of the rectifier.
0	1	LED is turned on for torch light operation. The converter is operating in the current regulation mode (CM). The output voltage is controlled by the forward voltage characteristic of the LED.
1	0	LED is turned on for flashlight operation. The converter is operating in the current regulation mode (CM). The output voltage is controlled by the forward voltage characteristic of the LED.
1	1	LED is turned off and the converter is operating in voltage regulation mode (VM). The output voltage is regulated to 5.0 V.

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9.3.2 Flash Synchronization

To simplify flash synchronization with the camera module, the device offers a FLASH_SYNC strobe input pin to switch (with zero latency) the LED current from flash to torch light. The LED is driven at the flashlight current level when a logic high signal is applied to the FLASH_SYNC pin.

The maximum duration of the flash pulse can be limited by means of an internal safety timer (820 ms). The safety timer starts on the rising edge of the FLASH_SYNC signal and stops either on its falling edge or after a time-out whatever occurs first.

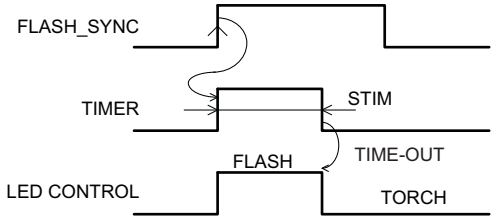


Figure 14. Level Sensitive Safety Timer (Time-Out)

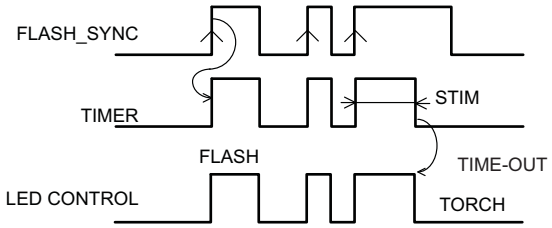


Figure 15. Level Sensitive Safety Timer (Normal Operation + Time-Out)

9.3.3 Efficiency

The sense voltage has a direct effect on the converter's efficiency. Because the voltage across the low-side current regulator does not contribute to the output power (LED brightness), the lower the sense voltage, the higher the efficiency will be.

When running in boost mode ($V_{F(LED)} > V_{IN}$), the voltage present at the LED pin of the low-side current regulator is typically 250 mV, which contributes to high power-conversion efficiency.

When running in the linear down-converter mode ($V_{F(LED)} < V_{IN}$), the low-side current regulator drops the voltage difference between the input voltage and the LED forward voltage. Depending on the input voltage and the LED forward voltage characteristic, the converter displays efficiency of approximately 80% to 90%.

9.3.4 Flash Blanking

The TPS6105x device also integrates a Tx-TOFF input that can be used as flash masking input. This blanking function turns the LED from flash to torch light, thereby reducing almost instantaneously the peak current loading from the battery. This function has no influence on the safety timer duration.

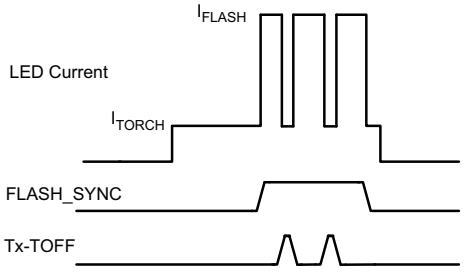


Figure 16. Synchronized Flash With Blanking Periods (MODE0 = 0, MODE1 = 1)

9.3.5 Soft-Start

Because the output capacitor always remains biased to the input voltage, the TPS6105x can immediately start switching once it has been enabled. The TPS6105x starts up by smoothly ramping up the internal reference voltage of the device, thus limiting the inrush current.

9.3.6 Shutdown

In shutdown mode, the regulator stops switching and the LED pin is high-impedance, thus eliminating any DC conduction path. The internal switch and rectifier MOSFET are turned off. VOUT is one body-diode drop below the input voltage and the device consumes only a shutdown current of 0.3 µA (typical). The output capacitor remains biased to the input voltage.

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9.3.7 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages. It prevents the converter from turning on the switch or rectifier MOSFET under undefined conditions.

9.3.8 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 160°C typical, the device goes into thermal shutdown. In this mode, the *boost* power stage and the low-side current regulator are turned off. To resume operation, the device needs to be cycled through a shutdown phase (MODE0 = 0, MODE1 = 0).

9.4 Device Functional Modes

9.4.1 Low-Light Dimming Mode

The TPS6105x device features white LED drive capability at very low-light intensity. To generate a reduced LED average current, the device employs a 122-Hz, fixed-frequency PWM modulation scheme. Operation is understood best by referring to the Figure 13.

The torch current is modulated with a 6.3% duty cycle. The low-light dimming mode can only be activated in the torch only mode (MODE1 = 0, MODE0 = 1) together with a logic level high applied to the FLASH_SYNC input.

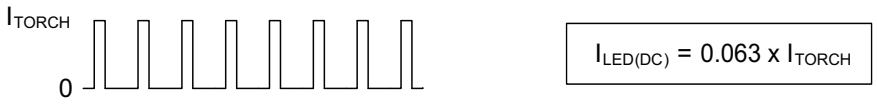


Figure 17. PWM Dimming Principle

White LED blinking can be achieved by turning on or off periodically the LED dimmer through the (DIM) bit, see Figure 18.

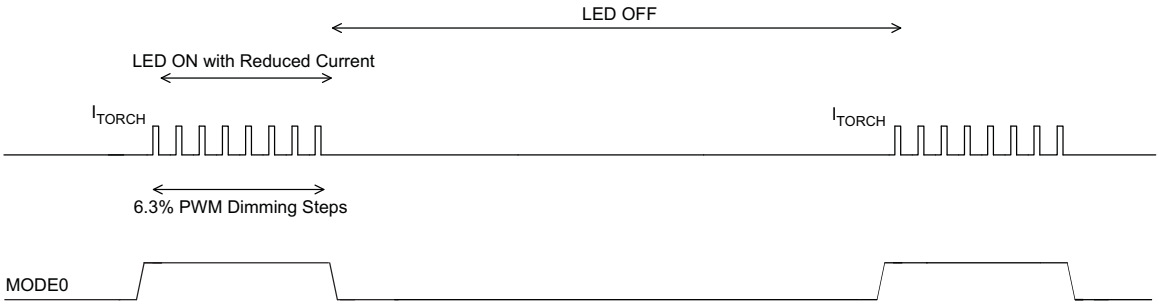


Figure 18. White LED Blinking Control (MODE1 = 0, FLASH_SYNC = 1)

9.4.2 LED Failure Modes

If the LED fails as a short circuit, the low-side current regulator limits the maximum output current.

If the LED fails as an open circuit, the control loop initially attempts to regulate off of its low-side current regulator feedback signal. This drives VOUT higher. Because the open-circuited LED will never accept its programmed current, VOUT must be voltage-limited by means of a secondary control loop. In this failure mode, the TPS6105x limits VOUT to 6.0 V (typical).

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS6105x device uses a high-frequency synchronous-boost topology with constant current sink to drive single white LEDs. The TPS6105x device not only operates as a regulated current source, but also as a standard voltage-boost regulator. This additional operating mode can be useful to supply other high-power devices in the system, such as a hands-free audio power amplifier, or any other component requiring a supply voltage higher than the battery voltage.

10.2 Typical Applications

10.2.1 High Power White LED Solution Featuring No-Latency Turn-Down through PA TX Signal

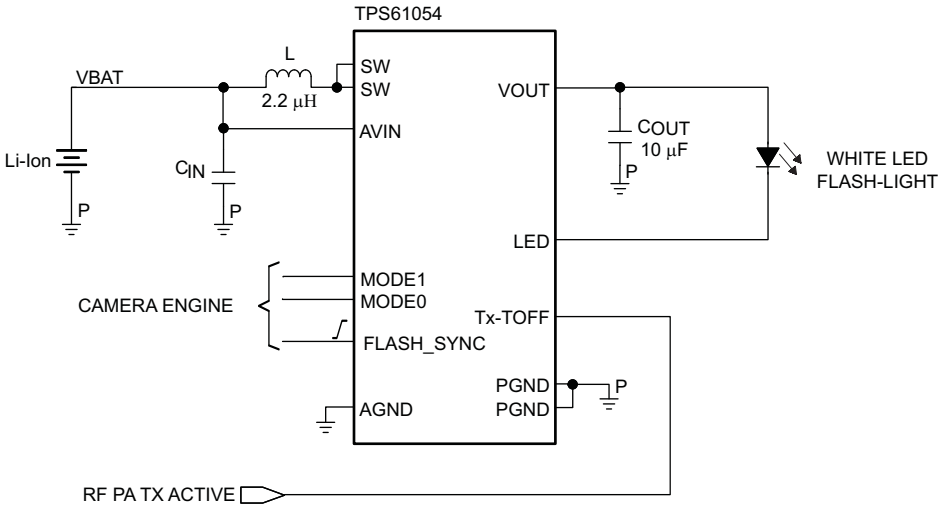


Figure 19. High Power White LED Solution Featuring No-Latency Turn-Down through PA TX Signal

10.2.1.1 Design Requirements

Table 3 shows how to use the TPS6105x to drive high power white LED.

Table 3. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	3.3 V to 4.2 V
Output voltage	5 V
Flash current	500 mA

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Inductor Selection

A boost converter requires two main passive components for storing energy during the conversion. A boost inductor and a storage capacitor at the output are required. The TPS6105x device integrates a current limit protection circuitry. The peak current of the NMOS switch is sensed to limit the maximum current flowing through the switch and the inductor (for example, 1000 mA or 1500 mA).

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To optimize solution size the TPS6105x device has been designed to operate with inductance values between a minimum of 1.3 µH and maximum of 2.9 µH. In typical high-current white LED applications a 2.2-µH inductance is recommended.

To select the boost inductor, TI recommends to keep the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. The highest peak current through the inductor and the power switch depends on the output load, the input and output voltages. Estimation of the maximum average inductor current and the maximum inductor peak current can be done using Equation 1 and Equation 2:

$$I_L \approx I_{OUT} = \frac{V_{OUT}}{\eta \times V_{IN}} \quad (1)$$

$$I_{L(PEAK)} = \frac{V_{IN} \times D}{2 \times f \times L} + \frac{I_{OUT}}{(1 - D) \times \eta} \text{ with } D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (2)$$

where

- f = switching frequency (2 MHz)
- L = inductance value (2.2 µH)
- η = estimated efficiency (85%)

For example, for an output current of 500 mA at 5 V, the TPS6105x device needs to be set for a 1000 mA current limit operation together with an inductor supporting this peak current.

The losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

Table 4. List of Inductors

MANUFACTURER	SERIES	DIMENSIONS	I_{LIM} SETTINGS
TDK	VLF3010AT	2.6 mm × 2.8 mm × 1.0 mm maximum height	1000 mA (typical)
TAIYO YUDEN	NR3010	3.0 mm × 3.0 mm × 1.0 mm maximum height	
FDK	MIPSA2520	2.5 mm × 2.0 mm × 1.2 mm maximum height	
TDK	VLF3014AT	2.6 mm × 2.8 mm × 1.4 mm maximum height	1500 mA (typical)
COILCRAFT	LPS3015	3.0 mm × 3.0 mm × 1.5 mm maximum height	
MURATA	LQH3NP	3.0 mm × 3.0 mm × 1.5 mm maximum height	
TOKO	FDSE0312	3.0 mm × 3.0 mm × 1.2 mm maximum height	

10.2.1.2.2 Capacitor Selection

10.2.1.2.2.1 Input Capacitor

For good input voltage filtering low ESR ceramic capacitors are recommended. A 10-µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. The input capacitor must be placed as close as possible to the input pin of the converter.

10.2.1.2.2.2 Output Capacitor

The primary parameter necessary to define the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance needed for the defined ripple, supposing that the ESR is zero, by using Equation 3:

$$C_{min} \approx \frac{I_{OUT} \times \left(V_{OUT} - V_{IN}\right)}{f \times \Delta V \times V_{OUT}} \quad (3)$$

where

- f is the switching frequency
- ΔV is the maximum allowed ripple.

With a chosen ripple voltage of 10 mV, a minimum capacitance of 10 µF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using Equation 4:

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$$\Delta V_{ESR} = I_{OUT} \times R_{ESR} \quad (4)$$

The total ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor. Additional ripple is caused by load transients. This means that the output capacitor has to completely supply the load during the charging phase of the inductor. A reasonable value of the output capacitance depends on the speed of the load transients and the load current during the load change.

For the high current white LED application, a minimum of 3-µF effective output capacitance is usually required when operating with 2.2-µH (typical) inductors. For solution size reasons, this is usually one or more X5R/X7R ceramic capacitors. For stable operation of the internally compensated control loop, a maximum of 50-µF effective output capacitance is tolerable.

Depending on the material, size and margin to the rated voltage of the used output capacitor, degradation on the effective capacitance can be observed. This loss of capacitance is related to the DC bias voltage applied. Therefore, TI always recommends to check that the selected capacitors are showing enough effective capacitance under real operating conditions.

10.2.1.2.3 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

The next step in regulation loop evaluation is to perform a load transient test. Output voltage settling time after the load transient event is a good estimate of the control loop bandwidth. The amount of overshoot and subsequent oscillations (ringing) indicates the stability of the control loop. Without any ringing, the loop has usually more than 45° of phase margin.

Because the damping factor of the circuitry is directly related to several resistive parameters (for example, MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, output current range, and temperature range.

10.2.1.3 Application Curves

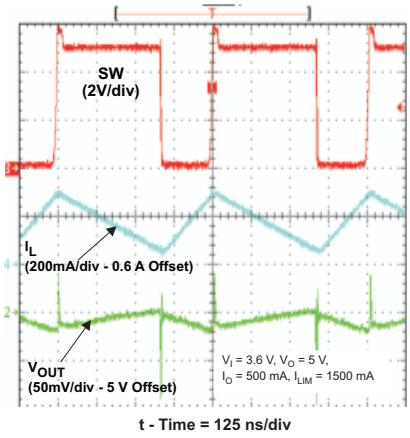


Figure 20. PWM Operation

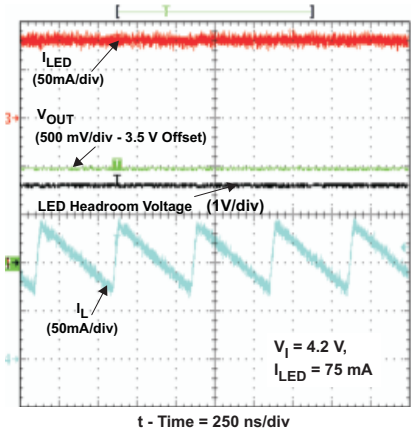


Figure 21. Down-Mode Operation

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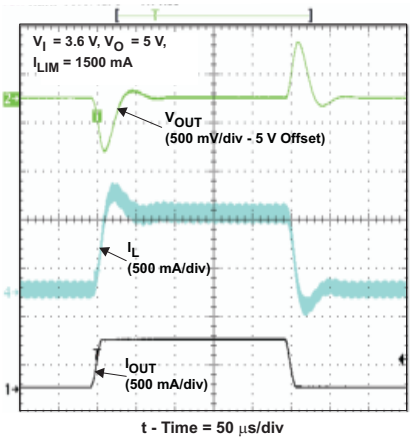


Figure 22. Voltage Mode Load Transient Response

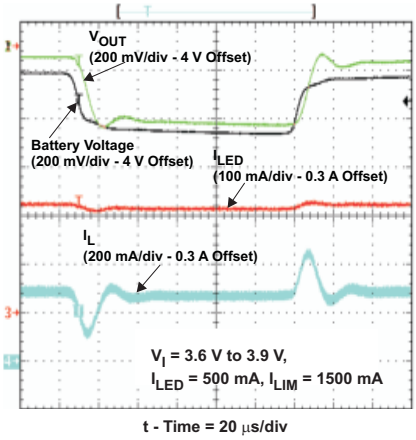


Figure 23. Down-Mode Line Transient Response

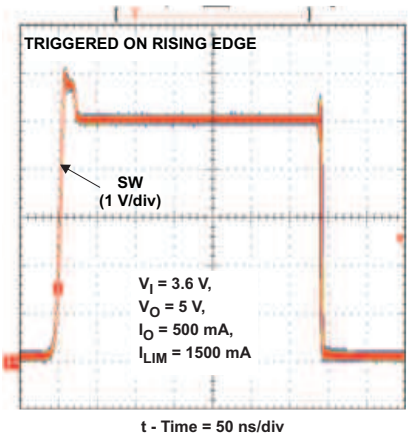


Figure 24. Duty Cycle Jitter

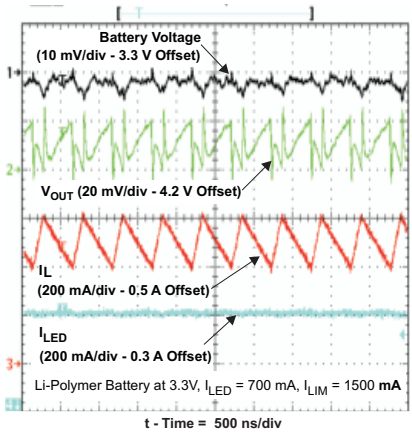


Figure 25. Input Ripple Voltage

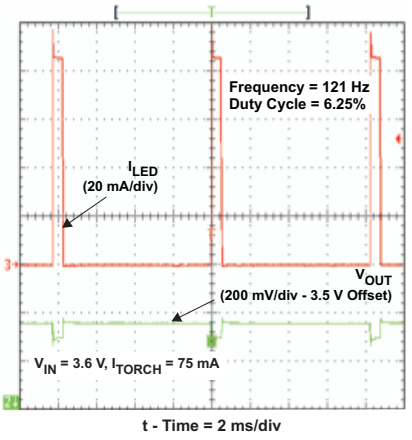


Figure 26. Low-Light Dimming Mode Operation

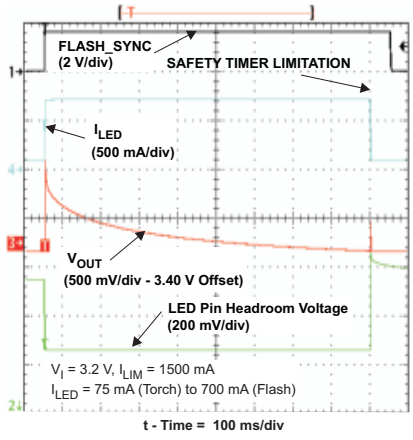


Figure 27. Torch and Flash Sequence

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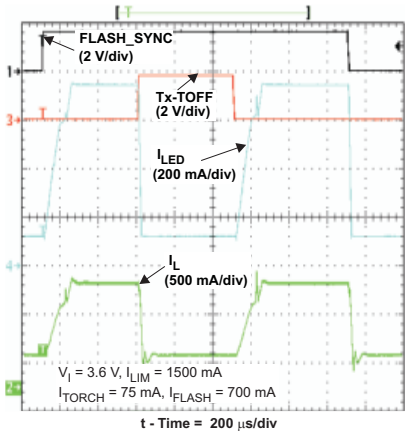


Figure 28. TX-Masking Operation

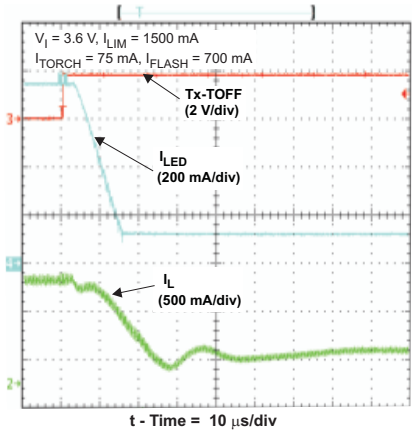


Figure 29. TX-Masking Operation

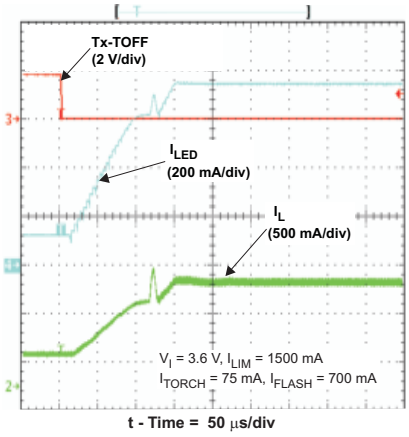


Figure 30. TX-Masking Operation

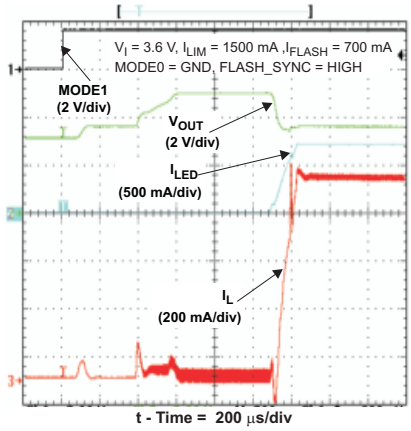


Figure 31. Start-Up in Flash Operation

10.2.2 2 × 350-mA Dual LED Camera Flash

Figure 32 shows the typical application where TPS61054 is used to drive dual LED camera flash (2 × 350-mA).

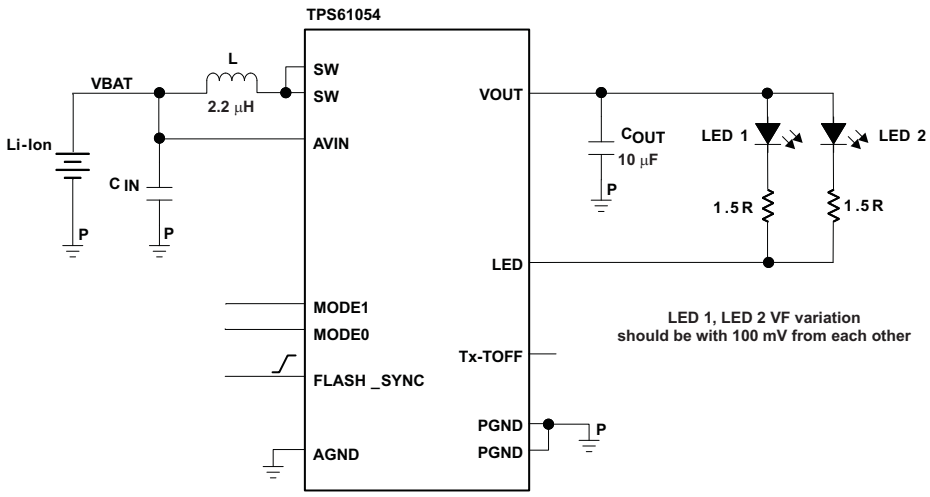


Figure 32. 2 × 350-mA Dual LED Camera Flash

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11 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.5 V to 6.0 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A typical choice is an electrolytic or tantalum capacitor with a value of 47 µF.

12 Layout

12.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks.

The input capacitor, output capacitor, and the inductor must be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

To lay out the control ground, TI recommends to use short traces, as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

12.2 Layout Example

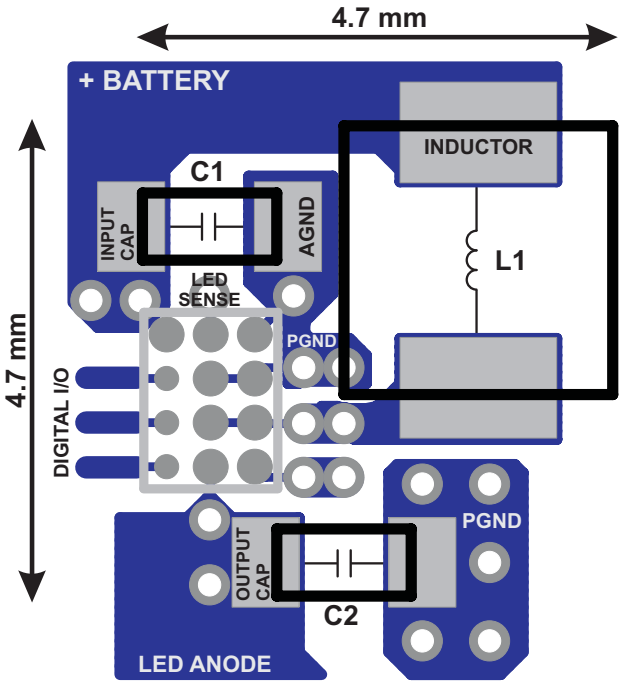


Figure 33. Typical PCB Layout

12.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, take special care to thermal dissipation issues in board design. The maximum junction temperature (T_J) of the TPS6105x is 150°C.

The maximum power dissipation gets especially critical when the device operates in the linear down mode at high LED current. For single-pulse power thermal analysis (for example, flash strobe), the allowable power dissipation for the device is given by Figure 34.

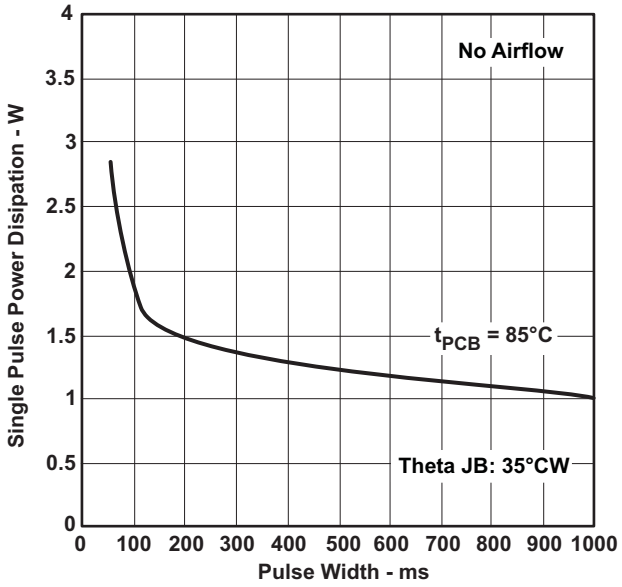


Figure 34. Single Pulse Power Capability (CSP Package)

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13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS61054	Click here	Click here	Click here	Click here	Click here
TPS61055	Click here	Click here	Click here	Click here	Click here

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61054DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BRX	Samples
TPS61054YZGR	ACTIVE	DSBGA	YZG	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS61054	Samples
TPS61055DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BRY	Samples
TPS61055DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BRY	Samples
TPS61055YZGR	ACTIVE	DSBGA	YZG	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS61055	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

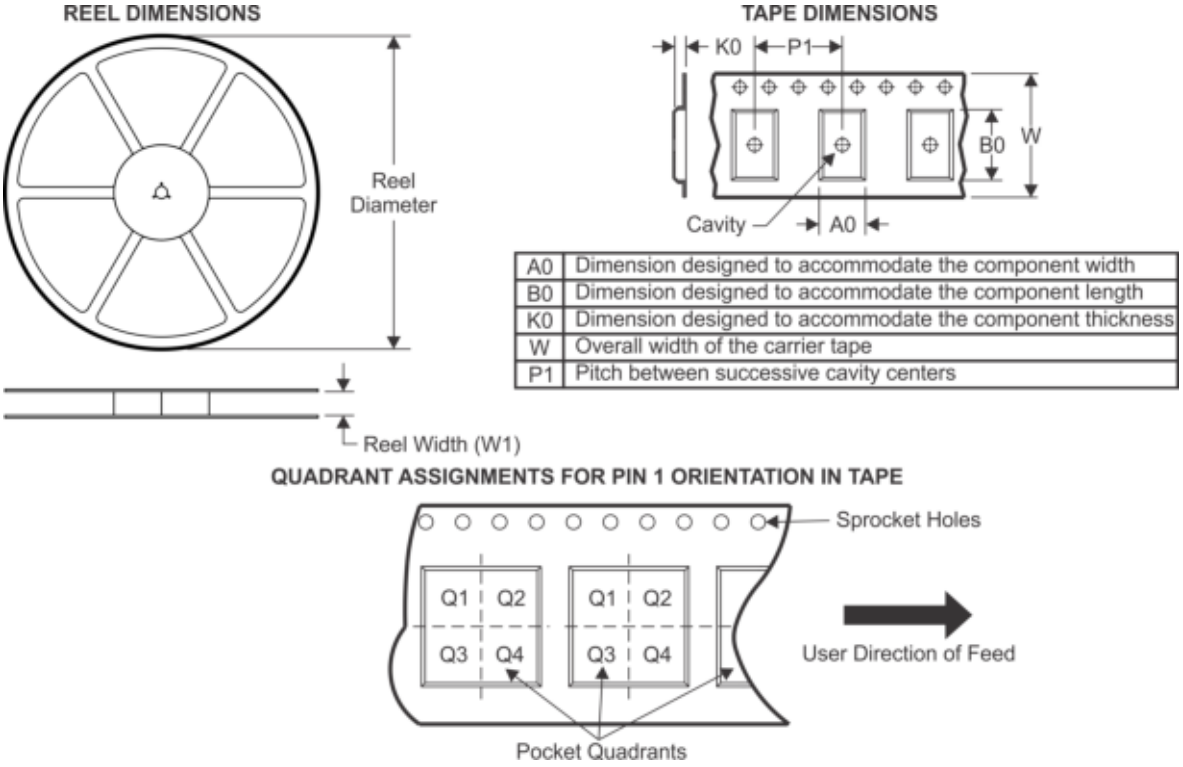
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

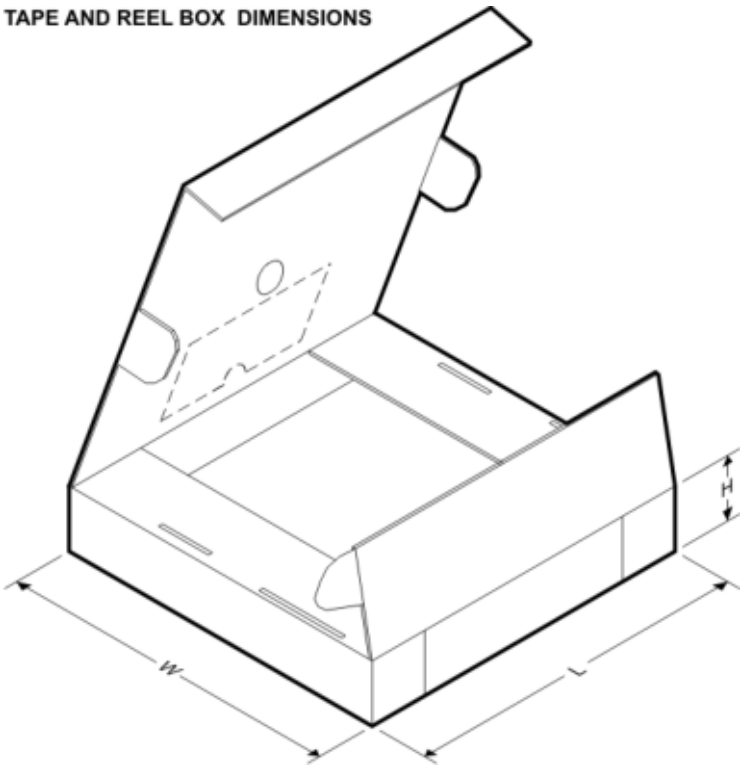


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61054DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61054YZGR	DSBGA	YZG	12	3000	180.0	8.4	1.75	2.25	0.81	4.0	8.0	Q1
TPS61055DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61055DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61055YZGR	DSBGA	YZG	12	3000	180.0	8.4	1.75	2.25	0.81	4.0	8.0	Q1

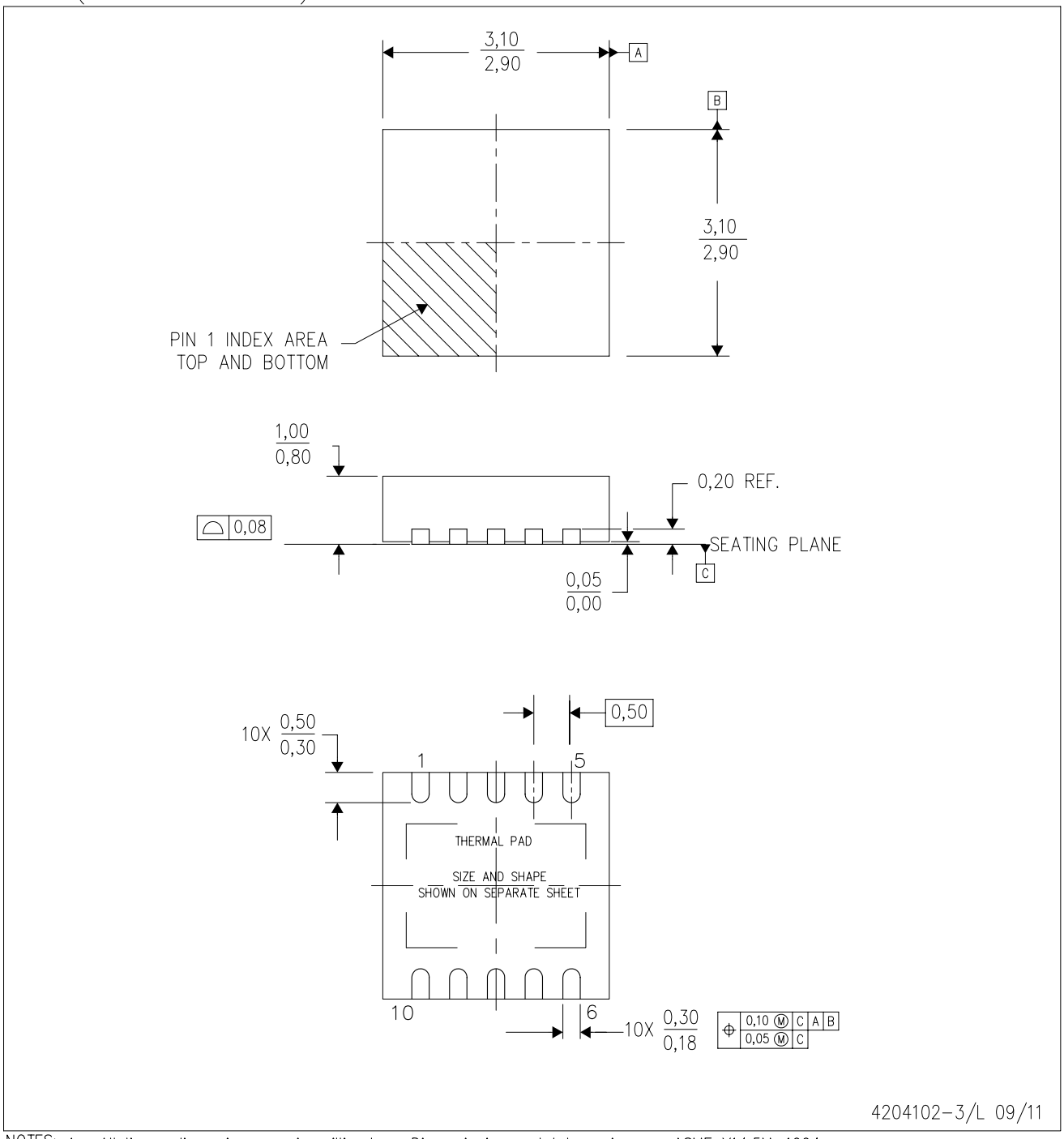
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61054DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS61054YZGR	DSBGA	YZG	12	3000	182.0	182.0	20.0
TPS61055DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS61055DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS61055YZGR	DSBGA	YZG	12	3000	182.0	182.0	20.0

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

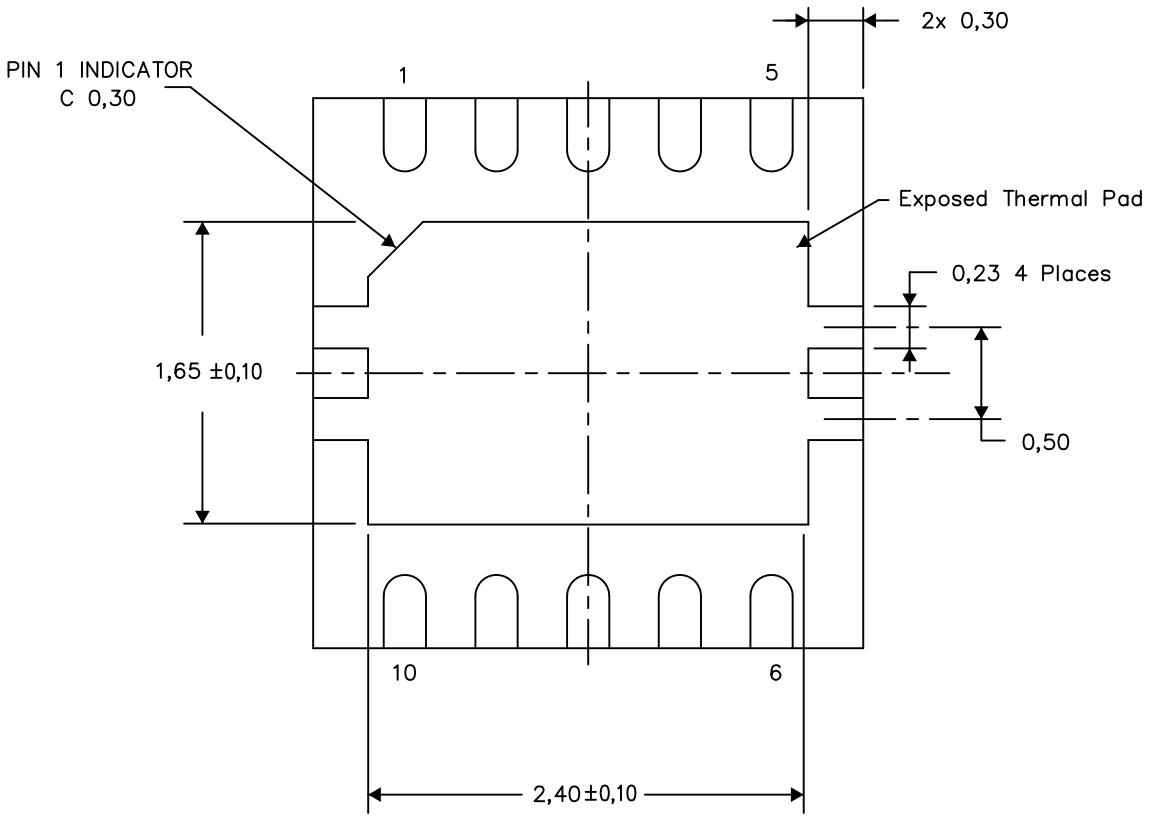
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



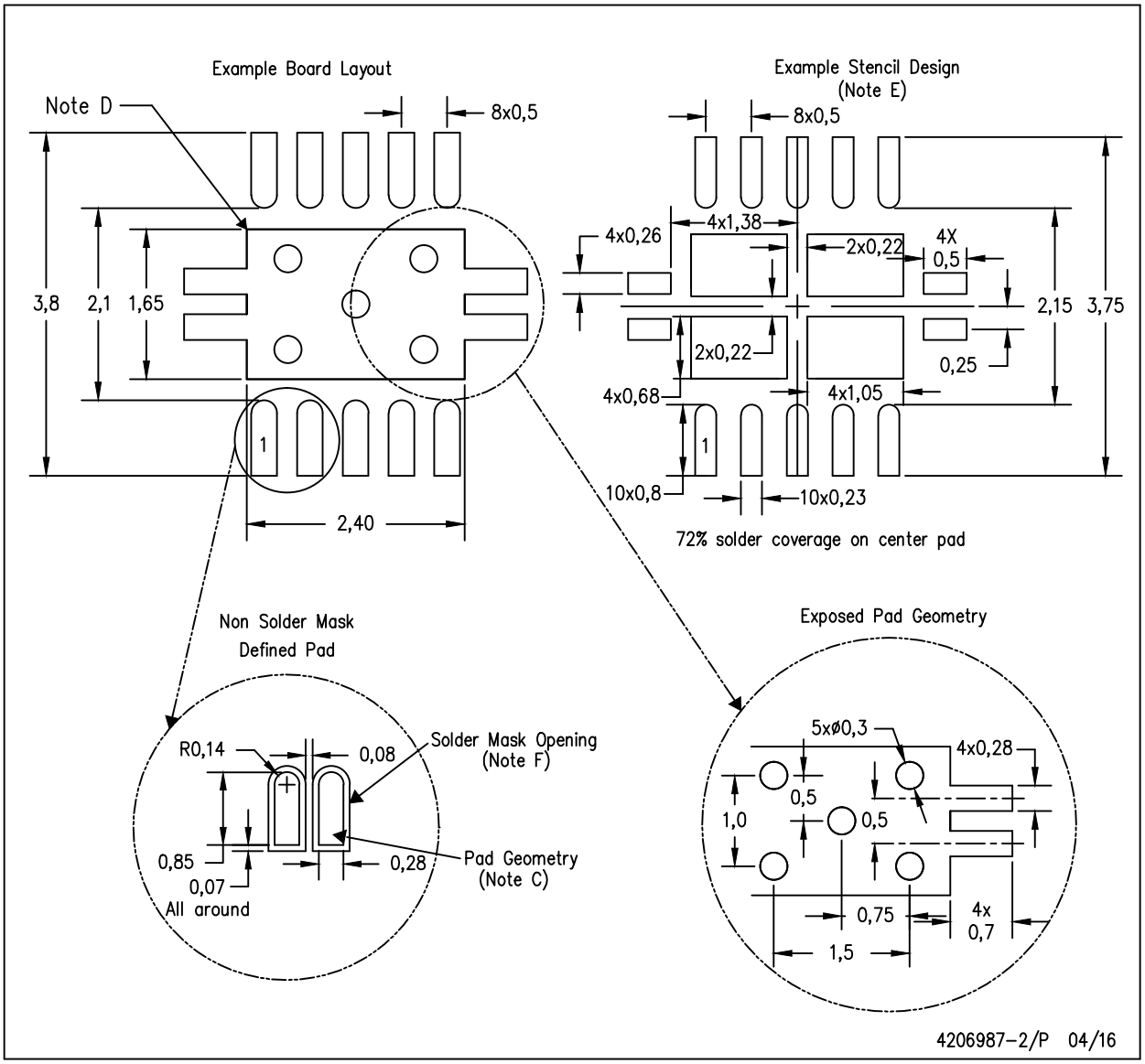
Bottom View

Exposed Thermal Pad Dimensions

4206565–3/Y 08/15

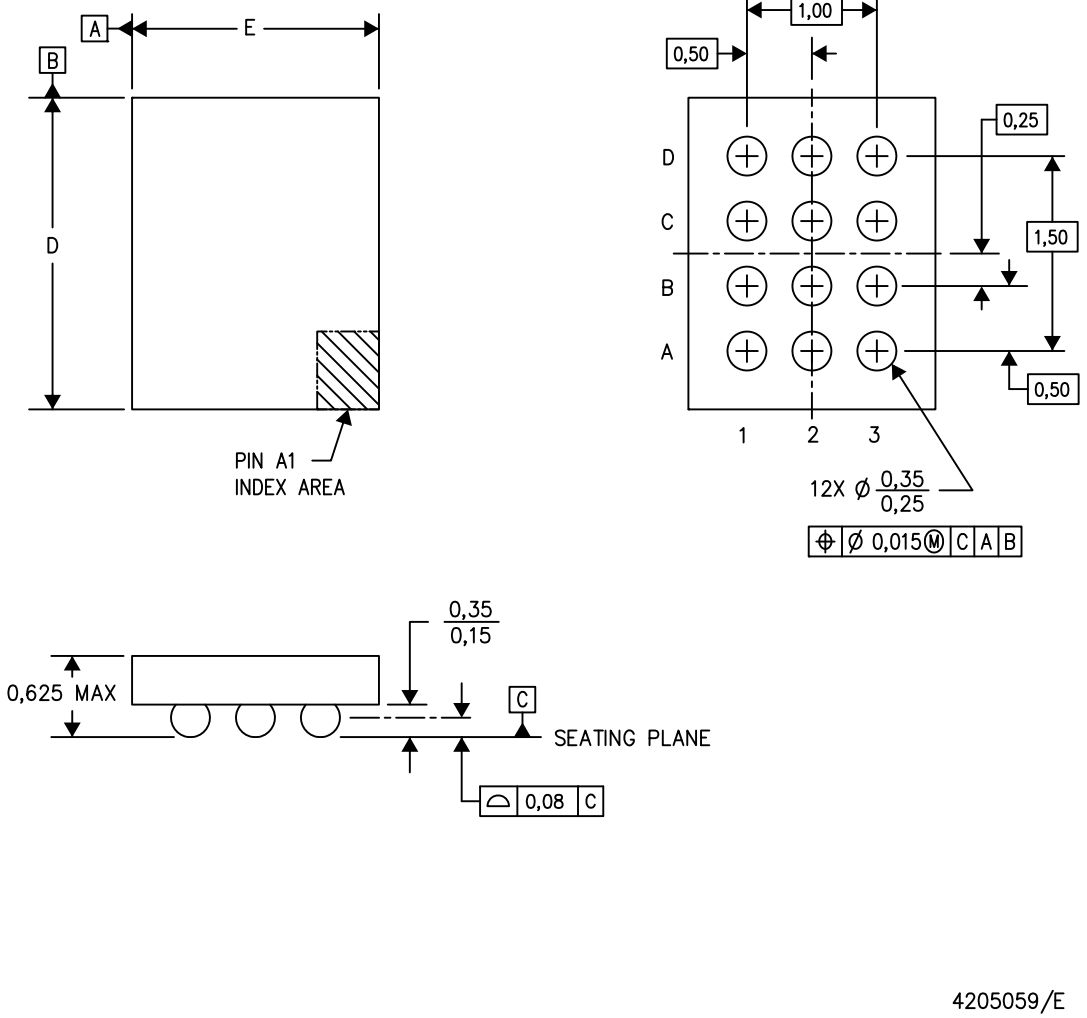
NOTE: A. All linear dimensions are in millimeters

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

YZG (R–XBGA–N12) DIE–SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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