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SLVS338P–MAY 2001–REVISED NOVEMBER 2008

50 mA, 24 V, 3.2-μA Supply Current Low-Dropout Linear Regulator in SC70 Package

FEATURES

- **24-V Maximum Input Voltage**
- **Low 3.2-μA Quiescent Current at 50 mA**
- **Stable With Any Capacitor (≥ 0.47 μF)**
- **50-mA Low-Dropout Regulator**
- **Available in 1.8 V, 1.9 V, 2.3 V, 2.5 V, 3.0 V, 3.3 V, 3.45 V, 5.0 V, and Adjustable (1.2 V to 15 V)**
- **Designed to Support MSP430 Families:**
  - **1.9-V version ensured to be higher than minimum V_{IN} of 1.8 V**
  - **2.3-V version ensured to meet 2.2-V minimum V_{IN} for FLASH on MSP430F2xx**
  - **3.45-V version ensured to be lower than maximum V_{IN} of 3.6 V**
  - **Wide variety of fixed output voltage options to match V_{IN} to the minimum required for desired MSP430 speed**
- **Minimum/Maximum Specified Current Limit**
- **5-Pin SC70/SOT-323 (DCK) Package**
- **–40°C to +125°C Specified Junction Temperature Range**
- **For 80-mA Rated Current and Higher Power Package, see TPS715Axx**

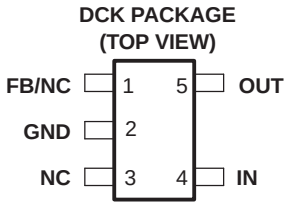
APPLICATIONS

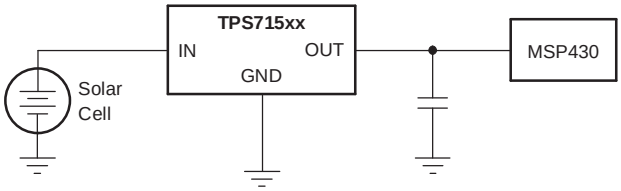
- **Ultra-Low Power Microcontrollers**
- **Cellular/Cordless Handsets**
- **Portable/Battery-Powered Equipment**

DESCRIPTION

The TPS715xx low-dropout (LDO) voltage regulators offer the benefits of high input voltage, low-dropout voltage, low-power operation, and miniaturized packaging. The devices, which operate over an input range of 2.5 V to 24 V, are stable with any capacitor (≥ 0.47 μF). The low dropout voltage and low quiescent current allow operations at extremely low power levels. Therefore, the devices are ideal for powering battery management ICs. Specifically, since the devices are enabled as soon as the applied voltage reaches the minimum input voltage, the output is quickly available to power continuously operating battery charging ICs.

The usual PNP pass transistor has been replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the low dropout voltage, typically 415 mV at 50 mA of load current, is directly proportional to the load current. The low quiescent current (3.2 μA typically) is stable over the entire range of output load current (0 mA to 50 mA).





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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT}(2)
TPS715**xx*yyy*z**	**XX** is nominal output voltage (for example, 28 = 2.8 V, 285 = 2.85 V, 01 = Adjustable). **YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Output voltages from 1.25 V to 5.4 V in 50-mV increments are available through the use of innovative factory EEPROM programming; minimum order quantities may apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Over operating temperature range (unless otherwise noted).

	UNIT
V_{IN} range	–0.3 V to +24 V
V_{OUT} range	–0.3 V to +16.5 V
Peak output current	Internally limited
ESD rating, HBM	2 kV
ESD rating, CDM	500 V
Continuous total power dissipation	See Dissipation Rating Table
Junction temperature range, T_J	–40°C to +150°C
Storage temperature range, T_{stg}	–65°C to +150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

BOARD	PACKAGE	$R_{\theta JC}$°C/W	$R_{\theta JA}$°C/W	DERATING FACTOR ABOVE T_A = +25°C	$T_A \le 25$°C POWER RATING	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
Low-K(1)	DCK	165	395	2.52 mW/°C	250 mW	140 mW	100 mW
High-K(2)	DCK	165	315	3.18 mW/°C	320 mW	175 mW	130 mW

(1) The JEDEC Low-K (1s) board design used to derive this data was a 3 inch × 3 inch, two-layer board with 2 ounce copper traces on top of the board.
(2) The JEDEC High-K (2s2p) board design used to derive this data was a 3 inch × 3 inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

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ELECTRICAL CHARACTERISTICS

Over operating junction temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(NOM)}$ + 1 V, I_{OUT} = 1 mA, and C_{OUT} = 1 µF, unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage(1)		V_{IN}	I_O = 10 mA	2.5		24	V
			I_O = 50 mA	3		24	
V_{OUT} voltage range (TPS71501)				1.2		15	V
V_{OUT} accuracy(1)	Over V_{IN}, I_{OUT}, and T		V_{IN} + 1.0 V ≤ V_{IN} ≤ 24 V 100 µA ≤ I_{OUT} ≤ 50 mA	–4.0		+4.0	%
Ground pin current(2)		I_{GND}	0 ≤ I_{OUT} ≤ 50 mA, T_J = –40°C to +85°C		3.2	4.2	µA
			0 mA ≤ I_{OUT} ≤ 50 mA		3.2	4.8	
			0 mA ≤ I_{OUT} ≤ 50 mA, V_{IN} = 24 V			5.8	
Load regulation	$\Delta V_{OUT}/\Delta I_{OUT}$		I_{OUT} = 100 µA to 50 mA		22		mV
Output voltage line regulation (1)	$\Delta V_{OUT}/\Delta V_{IN}$		V_{OUT} + 1 V < V_{IN} ≤ 24 V		20	60	mV
Output noise voltage		V_n	BW = 200 Hz to 100 kHz, C_{OUT} = 10 µF, I_{OUT} = 50 mA		575		µVrms
Output current limit		I_{CL}	V_{OUT} = 0 V, V_{IN} ≥ 3.5 V	125		750	mA
			V_{OUT} = 0 V, V_{IN} < 3.5 V	90		750	mA
Power-supply ripple rejection		PSRR	f = 100 kHz, C_{OUT} = 10 µF		60		dB
Dropout voltage V_{IN} = $V_{OUT(NOM)}$ – 0.1 V		V_{DO}	I_{OUT} = 50 mA		415	750	mV

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or the value shown for *Input voltage* in this table, whichever is greater.
(2) See Figure 1. The TPS715xx family employs a leakage null control circuit. This circuit is active only if output current is less than pass FET leakage current. The circuit is typically active when output load is less than 5 µA, V_{IN} is greater than 18 V, and die temperature is greater than +100°C.

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FUNCTIONAL BLOCK DIAGRAMS

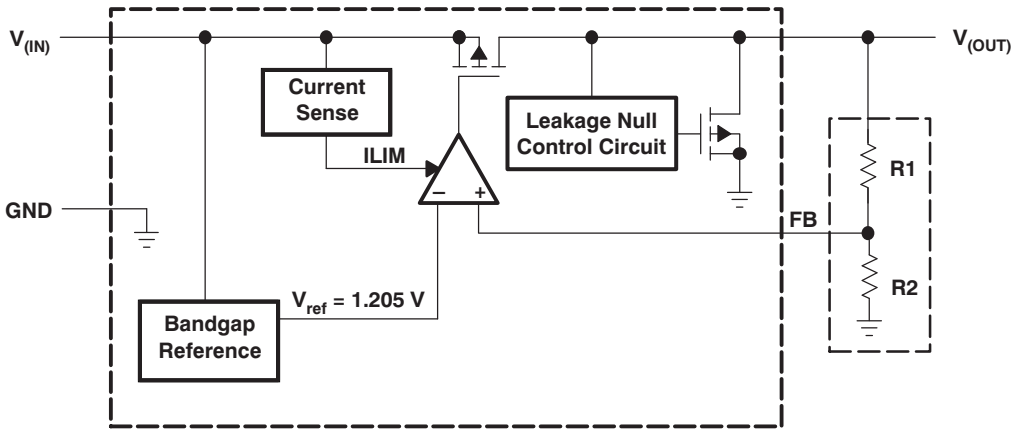


Figure 1. Functional Block Diagram—Adjustable Version

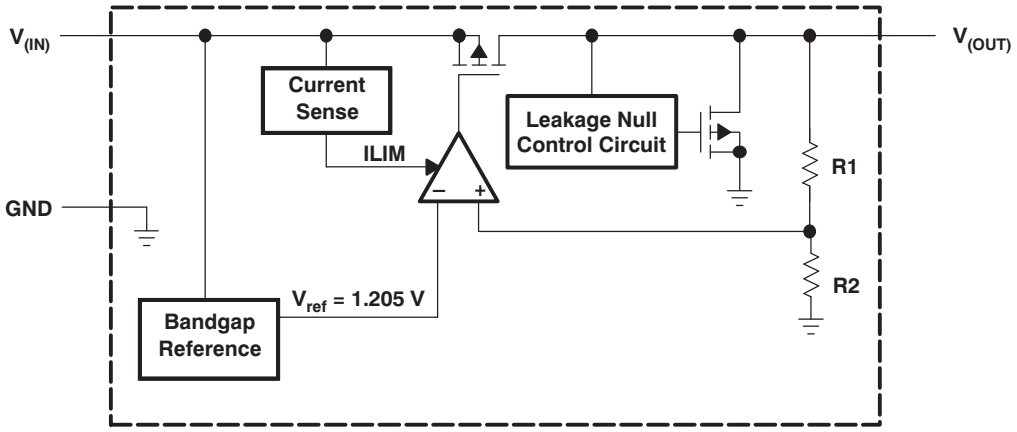


Figure 2. Functional Block Diagram—Fixed Version

Table 1. Terminal Functions

TERMINAL			DESCRIPTION
NAME	NO.		
	FIXED	ADJ.	
FB		1	Adjustable version only. This terminal is used to set the output voltage.
NC	1		No connection
GND	2	2	Ground
NC	3	3	No connection
IN	4	4	Input supply.
OUT	5	5	Output of the regulator, any output capacitor ≥ 0.47 µF can be used for stability.

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TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs OUTPUT CURRENT

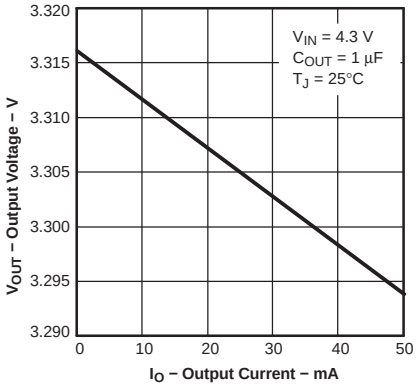


Figure 3.

OUTPUT VOLTAGE vs JUNCTION TEMPERATURE

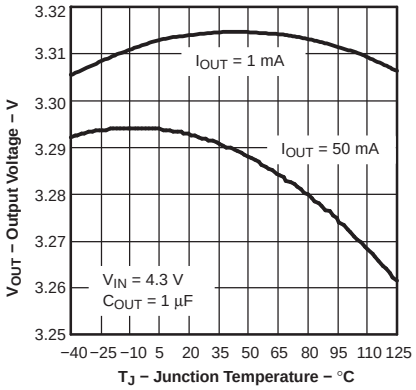


Figure 4.

QUIESCENT CURRENT vs JUNCTION TEMPERATURE

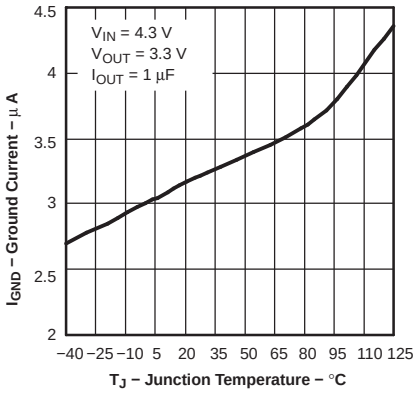


Figure 5.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

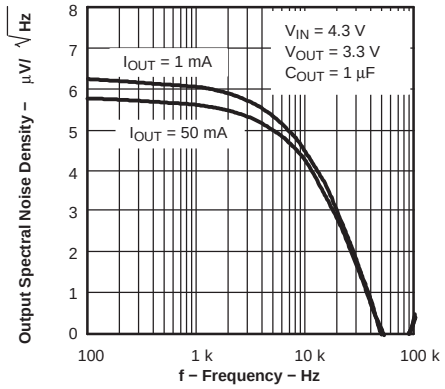


Figure 6.

OUTPUT IMPEDANCE vs FREQUENCY

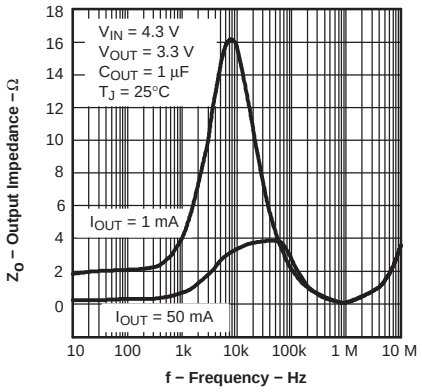


Figure 7.

DROPOUT VOLTAGE vs OUTPUT CURRENT

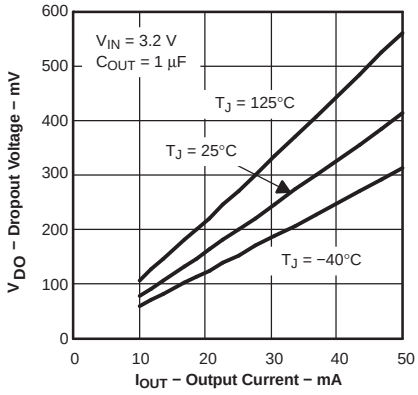


Figure 8.

TPS71501 DROPOUT VOLTAGE vs INPUT VOLTAGE

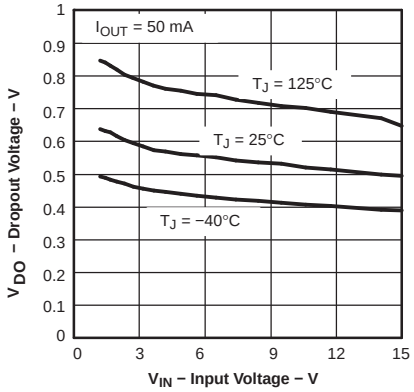


Figure 9.

DROPOUT VOLTAGE vs JUNCTION TEMPERATURE

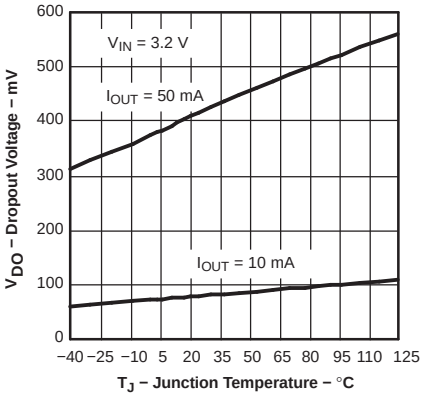


Figure 10.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY

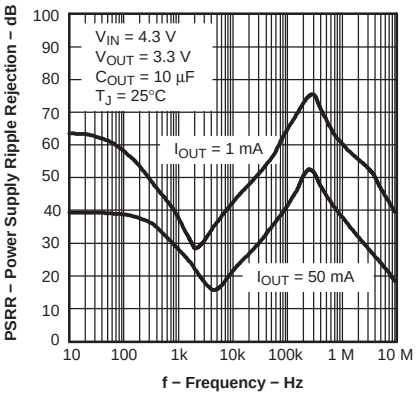


Figure 11.

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TYPICAL CHARACTERISTICS (continued)

POWER-UP / POWER-DOWN

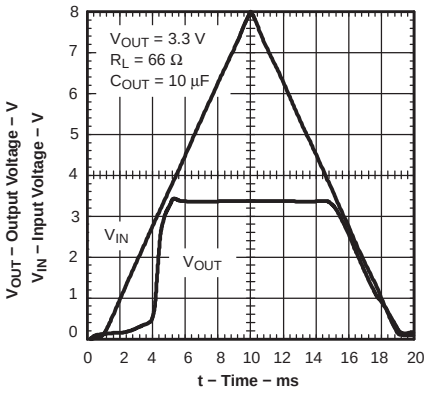


Figure 12.

LINE TRANSIENT RESPONSE

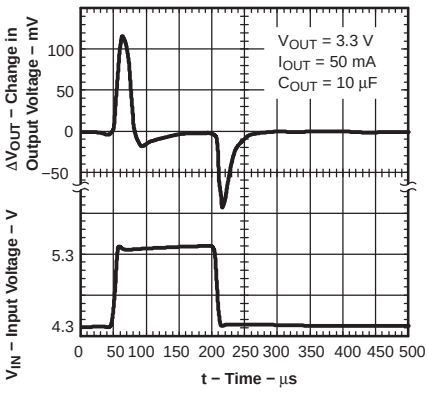


Figure 13.

LOAD TRANSIENT RESPONSE

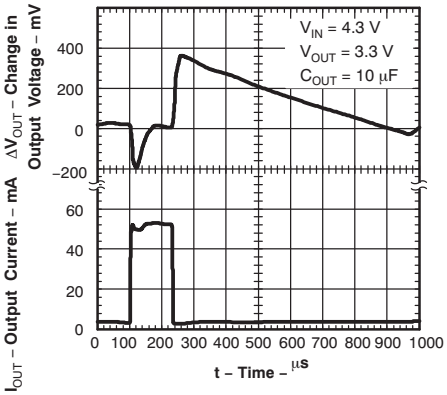


Figure 14.

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APPLICATION INFORMATION

The TPS715xx family of LDO regulators has been optimized for ultra-low power applications such as the MSP430 microcontroller. Its ultra-low supply current maximizes efficiency at light loads, and its high input voltage range makes it suitable for supplies such as unconditioned solar panels.

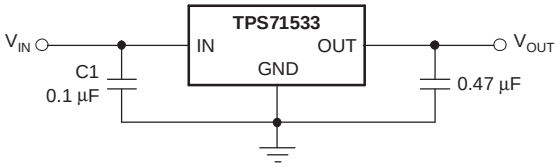


Figure 15. Typical Application Circuit (Fixed Voltage Version)

External Capacitor Requirements

Although not required, a 0.047-µF or larger input bypass capacitor, connected between IN and GND and located close to the device, is recommended to improve transient response and noise rejection of the power supply as a whole. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

The TPS715xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. Any capacitor (including ceramic and tantalum) greater than or equal to 0.47 µF properly stabilizes this loop. X7R type capacitors are recommended, but X5R and others may be used.

Power Dissipation and Junction Temperature

To ensure reliable operation, worst-case junction temperature should not exceed +125°C. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \quad (1)$$

where:

- $T_J$max is the maximum allowable junction temperature.
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the Dissipation Ratings table).
- T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

For a higher power package version of the TPS715xx, see the TPS715Axx.

Regulator Protection

The TPS715xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (e.g., during power-down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS715xx features internal current limiting. During normal operation, the TPS715xx limits output current to approximately 500 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. Take care not to exceed the power dissipation ratings of the package.

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Programming the TPS71501 Adjustable LDO Regulator

The output voltage of the TPS71501 adjustable regulator is programmed using an external resistor divider as shown in Figure 16. The output voltage operating range is 1.2 V to 15 V, and is calculated using:

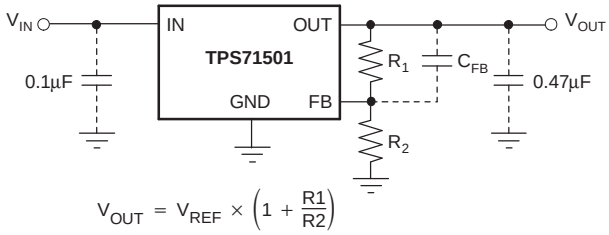
$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) \quad (3)$$

where:

- V_{REF} = 1.205 V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 1.5-µA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistor values should be avoided as leakage current into/out of FB across R1/R2 creates an offset voltage that artificially increases/decreases the feedback voltage and thus erroneously decreases/increases V_{OUT}. The recommended design procedure is to choose R2 = 1 MΩ to set the divider current at 1.5 µA, and then calculate R1 using Equation 4:

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R2 \quad (4)$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2
1.8 V	0.499 MΩ	1 MΩ
2.8 V	1.33 MΩ	1 MΩ
5.0 V	3.16 MΩ	1 MΩ

Figure 16. TPS71501 Adjustable LDO Regulator Programming

Power the MSP430 Microcontroller

Several versions of the TPS715xx are ideal for powering the MSP430 microcontroller. Table 2 shows potential applications of some voltage versions.

Table 2. Typical MSP430 Applications

DEVICE	V_{OUT} (TYP)	APPLICATION
TPS71519	1.9 V	$V_{OUT, MIN}$ > 1.800 V required by many MSP430s. Allows lowest power consumption operation.
TPS71523	2.3 V	$V_{OUT, MIN}$ > 2.200 V required by some MSP430s FLASH operation.
TPS71530	3.0 V	$V_{OUT, MIN}$ > 2.700 V required by some MSP430s FLASH operation.
TPS715345	3.45 V	$V_{OUT, MIN}$ < 3.600 V required by some MSP430s. Allows highest speed operation.

The TPS715xx family offers many output voltage versions to allow designers to minimize the supply voltage for the processing speed required of the MSP430. This minimizes the supply current consumed by the MSP430.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
BQ71525DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
BQ71525DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
BQ71533DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
BQ71533DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS71501DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS71501DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS71518DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS71518DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS71519DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS71519DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS71523DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS71523DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS71525DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS71525DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS71530DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS71530DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS71533DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS71533DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS715345DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS715345DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS71550DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS71550DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF TPS71501, TPS71525, TPS71530, TPS71533, TPS71550 :

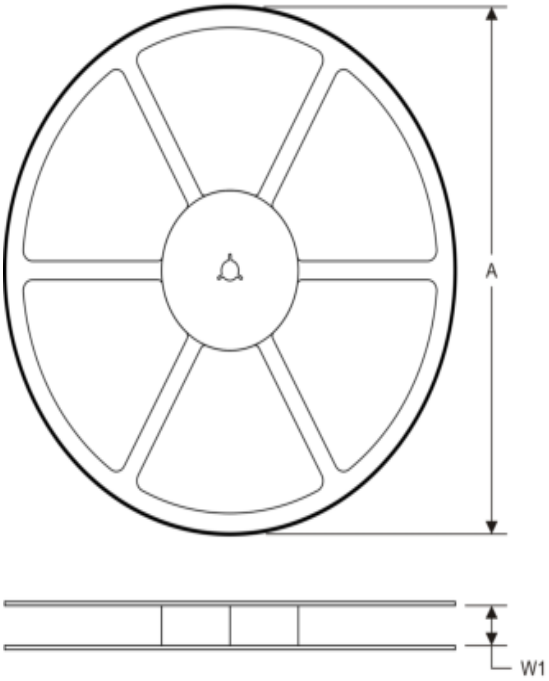
- Automotive: TPS71501-Q1, TPS71525-Q1, TPS71530-Q1, TPS71533-Q1, TPS71550-Q1
- Enhanced Product: TPS71501-EP

NOTE: Qualified Version Definitions:

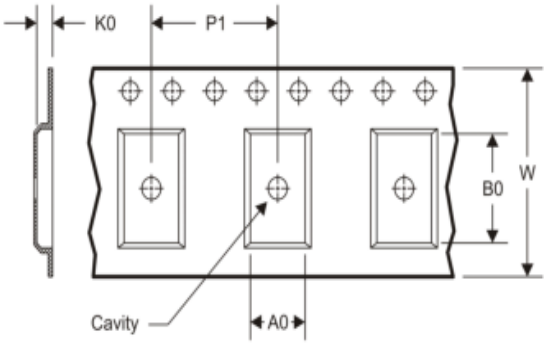
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



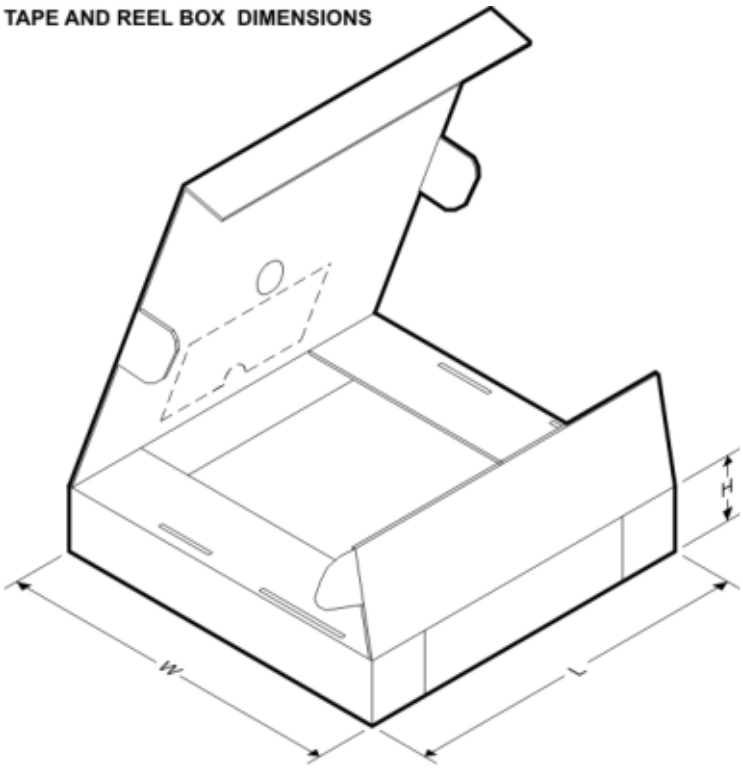
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ71525DCKR	SC70	DCK	5	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
BQ71533DCKR	SC70	DCK	5	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
TPS71501DCKR	SC70	DCK	5	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
TPS71518DCKR	SC70	DCK	5	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
TPS71519DCKR	SC70	DCK	5	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
TPS71523DCKR	SC70	DCK	5	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
TPS71525DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71530DCKR	SC70	DCK	5	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
TPS71533DCKR	SC70	DCK	5	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
TPS715345DCKR	SC70	DCK	5	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
TPS71550DCKR	SC70	DCK	5	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3

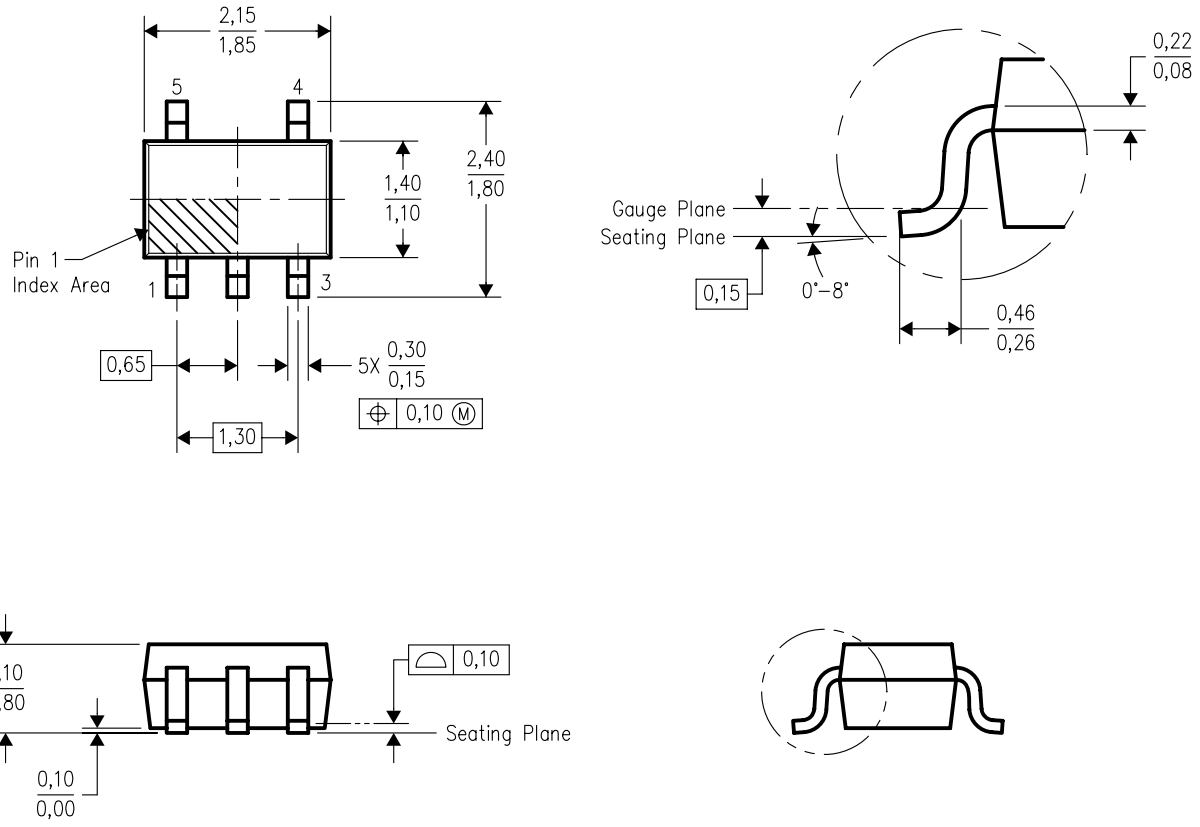
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ71525DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
BQ71533DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
TPS71501DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
TPS71518DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
TPS71519DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
TPS71523DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
TPS71525DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71530DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
TPS71533DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
TPS715345DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
TPS71550DCKR	SC70	DCK	5	3000	202.0	201.0	28.0

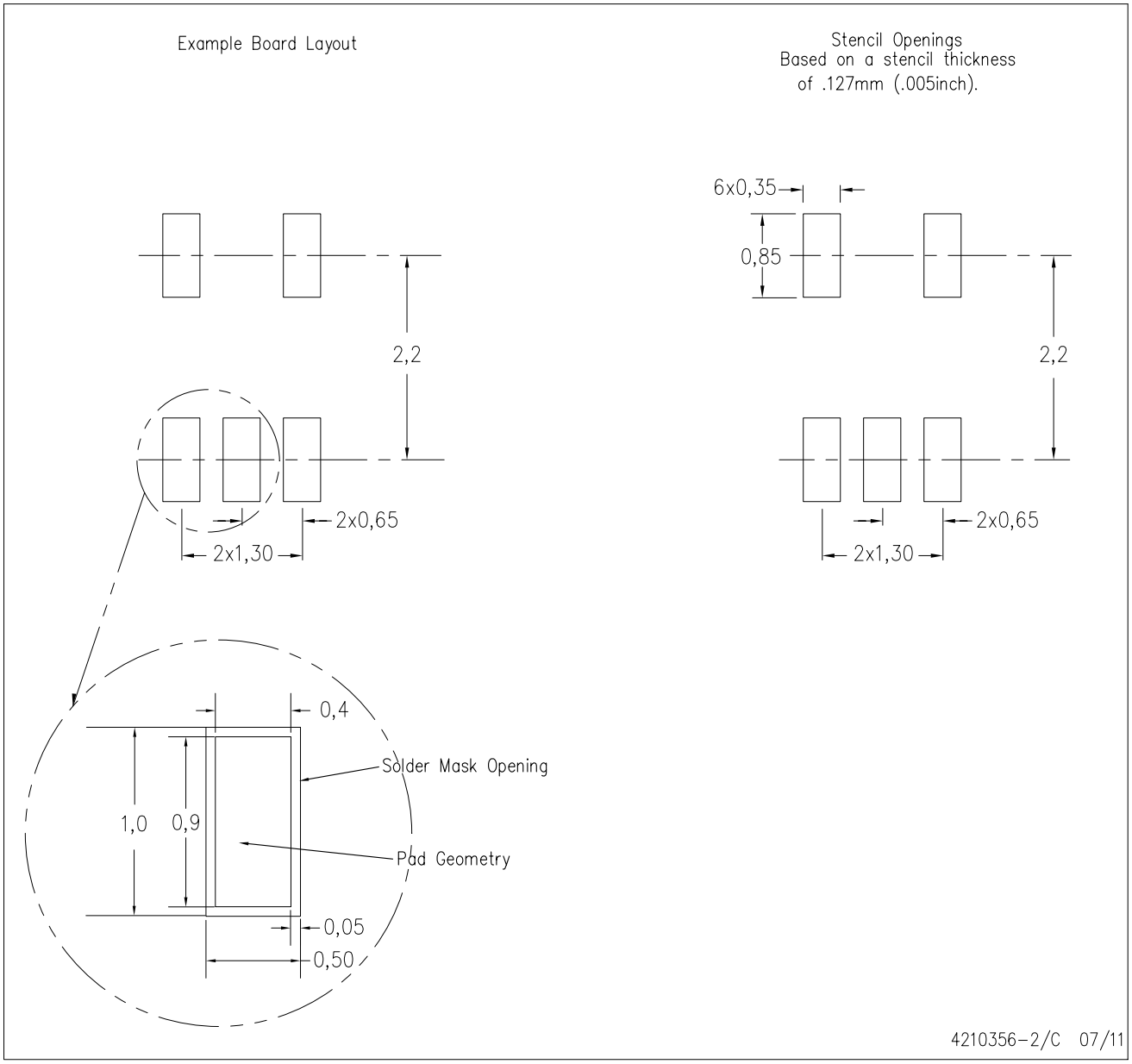
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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