

TE0803 TRM

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2 Overview

Refer to "https://shop.trenz-electronic.de/en/Download/?path=Trenz_Electronic/TE0803" for downloadable version of this manual and the rest of available documentation.The Trenz Electronic TE0803 is an industrial-grade MPSoC SoM integrating a Xilinx Zynq UltraScale+, max. 8 GByte DDR4 SDRAM with 64-Bit width data bus connection, max. 512 MByte SPI Boot Flash memory for configuration and operation, up to 8 Gigabit transceivers and powerful switch-mode power supplies for all on-board voltages. A large number of configurable I/O's is provided via rugged high-speed stacking connections.

All this in a compact 5.2 x 7.6 cm form factor, at the most competitive price

2.1 Key Features

- Xilinx Zynq UltraScale+ MPSoC 784 pin package (options: ZU2CG, ZU2EG, ZU3CG, ZU3EG, ZU4CG, ZU4EV)
- Memory
  - 64-Bit DDR4, 8 GByte maximum
  - Dual SPI boot Flash in parallel, 512 MByte maximum
- User I/O
  - 65 x MIO, 48 x HD (all), 156 x HP (3 banks)
  - Serial transceiver: 4 x GTR (+ 4 x GTH transceiver with ZU4CG or ZU4EV MPSoC)
  - Transceiver clocks inputs and outputs
  - PLL clock generator inputs and outputs
- Size: 52 x 76 mm, 3 mm mounting holes for skyline heat spreader
- B2B connectors: 4 x 160 pin
- Si5338A - 4 output PLL
- All power supplies on board, single 3.3V power source required
  - LP, FP, PL separately controlled power domains
- Support for all boot modes (except NAND) and scenarios
- Support for any combination of PS connected peripherals

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2.2 Block Diagram

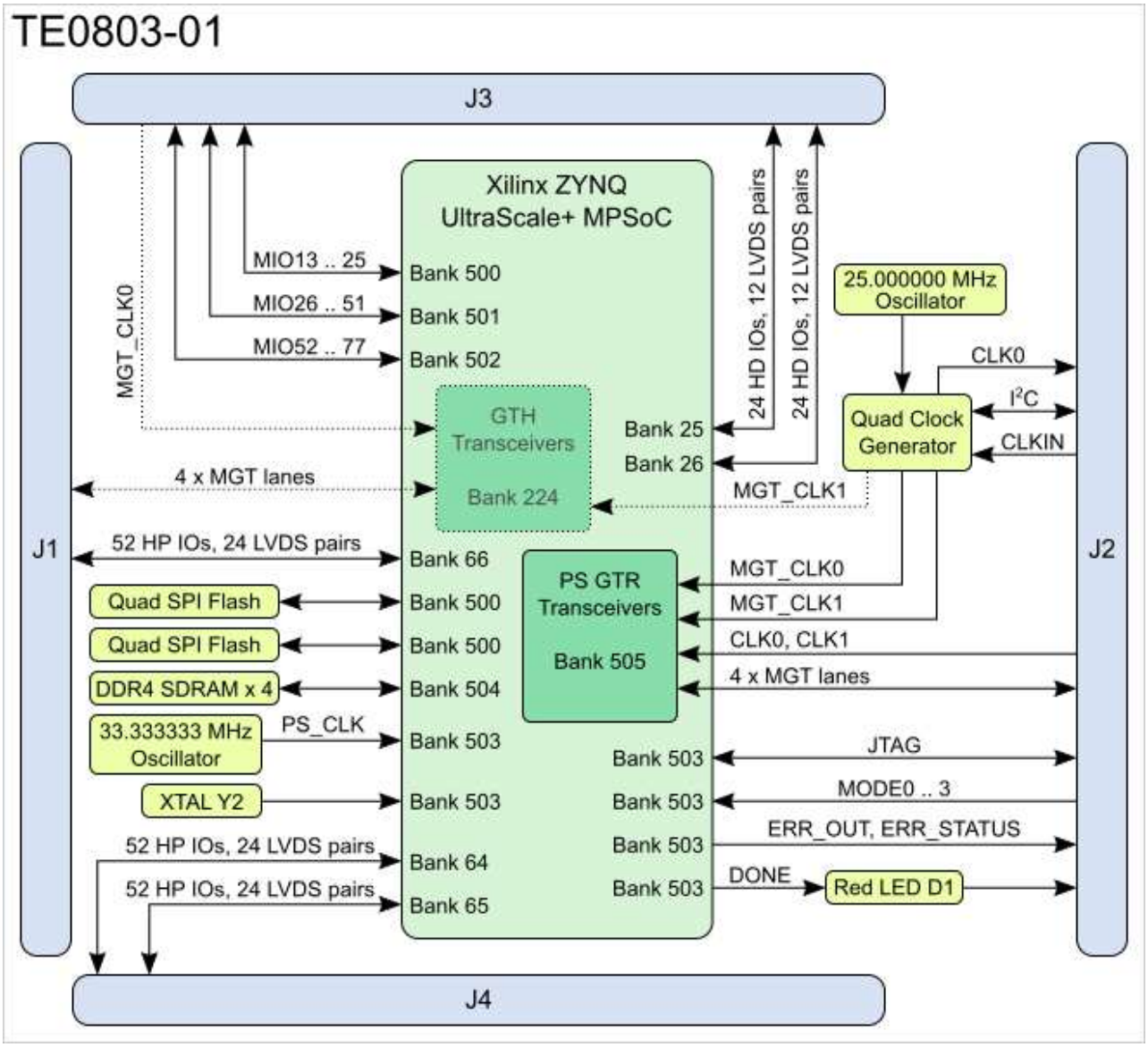


Figure 1: TE0803-01 Block Diagram

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2.3 Main Components

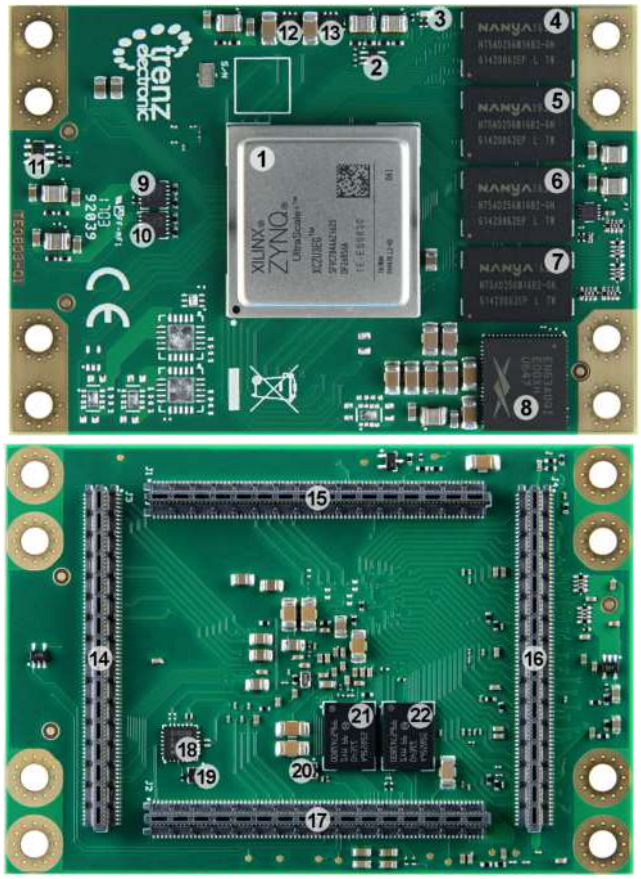


Figure 2: TE0803-01 MPSoC module

1. Xilinx ZYNQ UltraScale+ MPSoC, U1
2. 2-Input AND Gate, U39
3. Red LED (DONE), D1
4. 256Mx16 DDR4-2400 SDRAM, U12
5. 256Mx16 DDR4-2400 SDRAM, U9
6. 256Mx16 DDR4-2400 SDRAM, U2
7. 256Mx16 DDR4-2400 SDRAM, U3
8. 12A PowerSoC DC-DC converter, U4
9. 1.5A LDO DC-DC converter, U10
10. 1.5A LDO DC-DC converter, U8
11. Voltage monitor circuit, U41
12. 0.35A LDO DC-DC converter, U26
13. 0.35A LDO DC-DC converter, U27
14. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J3
15. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J1
16. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J4
17. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J2
18. 4-channel programmable PLL clock generator, U5
19. Low-power programmable oscillator @ 25.000000 MHz, U5
20. Low-power programmable oscillator @ 33.333333 MHz (PS_CLK), U32
21. 256 Mbit serial NOR Flash memory, U7
22. 256 Mbit serial NOR Flash memory, U17

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2.4 Initial Delivery State

Storage device name	Content	Notes
SPI Flash main array	Not programmed	-
eFUSE Security	Not programmed	-
Si5338A programmable PLL NVM OTP	Not programmed	-

Table 1: Initial Delivery State of the flash memories

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3 Signals, Interfaces and Pins

3.1 Board to Board (B2B) connectors

The TE0803 MPSoC SoM has four Board to Board (B2B) connectors with 160 contacts per connector.

Each connector has a specific arrangement of the signal-pins, which are grouped together in categories related to their functionalities and to their belonging to particular units of the Zynq UltraScale+ MPSoC like I/O-banks, interfaces and Gigabit transceivers
or to the on-board peripherals.

Following table lists the I/O-bank signals, which are routed from the MPSoC's PL and PS banks as LVDS pairs or single ended I/O's to the B2B connectors.

Bank	Type	B2B Connector	Schematic Names / Connector Pins	I/O Signal Count	LVDS Pairs Count	VCCO Bank Voltage	Notes
25[1)]	HD	J3	B25_L1_P ... B25_L12_P B25_L1_N ... B25_L12_N	24 I/O's	12	VCCO25 pins J3-15, J3-16	VCCO max. 3.3V usable as single-ended I/O's
26[2)]	HD	J3	B26_L1_P ... B26_L12_P B26_L1_N ... B26_L12_N	24 I/O's	12	VCCO26 pins J3-43, J3-44	VCCO max. 3.3V usable as single-ended I/O's
64	HP	J4	B64_L1_P ... B64_L24_P B64_L1_N ... B64_L24_N B64_T0 ... B64_T3	52 I/O's	24	VCCO64 pins J4-58, J4-106	VCCO max. 1.8V usable as single-ended I/O's
65	HP	J4	B65_L1_P ... B65_L24_P B65_L1_N ... B65_L24_N B65_T0 ... B65_T3	52 I/O's	24	VCCO65 pins J4-69, J4-105	VCCO max. 1.8V usable as single-ended I/O's
66	HP	J1	B66_L1_P ... B66_L24_P B66_L1_N ... B66_L24_N B66_T0 ... B66_T3	52 I/O's	24	VCCO66 pins J1-90, J1-120	VCCO max. 1.8V usable as single-ended I/O's
500	MIO	J3	MIO13 ... MIO25	13 I/O's	-	PS_1V8	user configurable I/O's on B2B

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Bank	Type	B2B Connector	Schematic Names / Connector Pins	I/O Signal Count	LVDS Pairs Count	VCCO Bank Voltage	Notes
501	MIO	J3	MIO26 ... MIO51	26 I/O's	-	PS_1V8	user configurable I/O's on B2B
502	MIO	J3	MIO52 ... MIO77	26 I/O's	-	PS_1V8	user configurable I/O's on B2B

Table 2: B2B connector pin-outs of available PL and PS banks of the TE0803-01 SoM

1) Bank 25 at XC**ZU2** / XC**ZU3**, else Bank 45 at XC**ZU4** / XC**ZU5**

2) Bank 26 at XC**ZU2** / XC**ZU3**, else Bank 46 at XC**ZU4** / XC**ZU5**

All MIO banks are powered from on-module DC-DC power rail. All PL I/O banks have separate VCCO input pins in the B2B connectors, valid VCCO should be supplied from the carrier board.

For detailed information about the B2B pin-out, please refer to the Pin-out table.

The configuration of the I/O's MIO13 - MIO77 are depending on the base-board peripherals connected to these pins.

3.2 MGT Lanes

The B2B connectors J1 and J2 provide also access to the MGT banks of the Zynq UltraScale+ MPSoC. There are 8 high-speed data lanes (Xilinx GTH / GTR transceiver) available composed as differential signaling pairs for both directions (RX/TX).

The MGT banks have also clock input-pins which are exposed to the B2B connectors J2 and J3. Following MGT lanes are available on the B2B connectors:

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Bank	Type	B2B Connector	Count of MGT Lanes	Schematic Names / Connector Pins	MGT Bank's Reference Clock Inputs
224 [1)]	GTH	J1	4 GTH lanes (4 RX / 4TX)	B224_RX3_P, B224_RX3_N, pins J1-51, J1-53 B224_TX3_P, B224_TX3_N, pins J1-50, J1-52 B224_RX2_P, B224_RX2_N, pins J1-57, J1-59 B224_TX2_P, B224_TX2_N, pins J1-56, J1-58 B224_RX1_P, B224_RX1_N, pins J1-63, J1-65 B224_TX1_P, B224_TX1_N, pins J1-62, J1-64 B224_RX0_P, B224_RX0_N, pins J1-69, J1-71 B224_TX0_P, B224_TX0_N, pins J1-68, J1-70	1 reference clock signal (B224_CLK0) from B2B connector J3 (pins J3-59/J3-61) to bank's pins Y6/Y5 1 reference clock signal (B224_CLK1) from programmable PLL clock generator U5 to bank's pins V6/V5
505	GTR	J2	4 GTR lanes (4 RX / 4TX)	B505_RX3_P, B505_RX3_N, pins J2-51, J2-49 B505_TX3_P, B505_TX3_N, pins J2-54, J2-52 B505_RX2_P, B505_RX2_N, pins J2-57, J2-55 B505_TX2_P, B505_TX2_N, pins J2-60, J2-58 B505_RX1_P, B505_RX1_N, pins J2-63, J2-61 B505_TX1_P, B505_TX1_N, pins J2-66, J2-64 B505_RX0_P, B505_RX0_N, pins J2-69, J2-67 B505_TX0_P, B505_TX0_N, pins J2-72, J2-70	2 reference clock signals (B505_CLK0, B505_CLK1) from B2B connector J2 (pins J2-16/J2-18, J2-10/J2-12) to bank's pins F23/F24, E21/E22 2 reference clock signals (B505_CLK2, B505_CLK3) from programmable PLL clock generator U5 to bank's pins C21/C22, A21/A22

Table 3: B2B connector pin-outs of available MGT lanes of the MPSoC

1) Bank 224 only available at XC**ZU4** / XC**ZU5** MPSoC.

3.3 JTAG Interface

JTAG access is provided through the MPSoC's PS configuration bank 503 with bank voltage 'PS_1V8'.

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JTAG Signal	B2B Connector Pin
TCK	J2-120
TDI	J2-122
TDO	J2-124
TMS	J2-126

Table 4: B2B connector pin-out of JTAG interface

3.4 Configuration Bank Control Signals

The Xilinx Zynq UltraScale+ MPSoC's PS configuration bank 503 control signal pins are accessible through B2B-connector J2.

For further information about the particular control signals and how to use and evaluate them, refer to the Xilinx Zynq UltraScale+ MPSoC TRM and UltraScale Architecture Configuration - User Guide.

Signal	B2B Connector Pin	Function
DONE	J2-116	PL configuration completed
PROG_B	J2-100	PL configuration reset signal
INIT_B	J2-98	PS is initialized after a power-on reset
SRST_B	J2-96	System reset
MODE0 ... MODE3	J2-109/J2-107/J2-105/ J2-103	4-bit boot mode pins For further information about the boot-modes refer to the Xilinx Zynq UltraScale+ MPSoC TRM section 'Boot and Configuration'.
ERR_STATUS / ERR_OUT	J2-86 / J2-88	ERR_OUT signal is asserted for accidental loss of power, an error, or an exception in the MPSoC's Platform Management Unit (PMU) ERR_STATUS indicates a secure lock-down state
PUDC_B	J2-127	Pull-up during configuration (pulled-up to 'PL_1V8')

Table 5: B2B connector pin-out of MPSoC's PS configuration bank

3.5 Analog Input

The Xilinx Zynq UltraScale+ MPSoC provides differential pairs for analog input values. The pins are exposed to B2B-connector J2.

Signal	B2B Connector Pin	Function
V_P, V_N	J2-113, J2-115	System Monitor
DX_P, DX_N	J2-119, J2-121	Temperature-sensing diode pins

Table 6: B2B connector pin-out of analog input pins

3.6 Quad SPI Interface

Quad SPI Flash memory ICs U7 and U17 are connected to the Zynq PS QSPI0 interface via PS MIO bank 500, pins MIO0..MIO5 and MIO7..MIO12.

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MIO	U7 Pin	Pin Name	MIO	U17 Pin	Pin Name
0	B2	CLK	7	C2	CS#
1	D2	DO/IO1	8	D3	DI/IO0
2	C4	WP#/IO2	9	D2	DO/IO1
3	D4	HOLD#/IO3	10	C4	WP#/IO2
4	D3	DI/IO0	11	D4	HOLD#/IO3
5	C2	CS#	12	B2	CLK

Table 7: MIO pin assignment of the Quad SPI Flash memory ICs

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4 Boot Process

The boot source of the Zynq UltraScale+ MPSoC can be selected via 4 dedicated pins, which generate a 4-bit code to select the boot mode. The pins are accessible on B2B connector J2:

Boot Mode Pin	B2B Pin
PS_MODE0	J2-109
PS_MODE1	J2-107
PS_MODE2	J2-105
PS_MODE3	J2-103

Table 8: Boot mode pins on B2B connector J2

Following boot modes are possible on the TE0803 UltraScale+ MPSoC module by generating the corresponding 4-bit code with pins 'PS_MODE0' ... 'PS_MODE3' (little-endian alignment):

Boot Mode	Mode Pins [3:0]	MIO Location	Description
JTAG	0x0	JTAG	Dedicated PS interface.
QSPI32	0x2	MIO[12:0]	Configured on module with dual QSPI Flash Memory. 32-bit addressing. Supports single and dual parallel configurations. Stack and dual stack is not supported.
SD0	0x3	MIO[25:13]	Supports SD 2.0.
SD1	0x5	MIO[51:38]	Supports SD 2.0.
eMMC_18	0x6	MIO[22:13]	Supports eMMC 4.5 at 1.8V.
USB 0	0x7	MIO[52:63]	Supports USB 2.0 and USB 3.0.
PJTAG_0	0x8	MIO[29:26]	PS JTAG connection 0 option.
SD1-LS	0xE	MIO[51:39]	Supports SD 3.0 with a required SD 3.0 compliant level shifter.

Table 9: Selectable boot modes by dedicated boot mode pins

For functional details see ug1085 - Zynq UltraScale+ TRM (Boot Modes Section).

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5 On-board Peripherals

5.1 Flash

The TE0803 SoM can be configured with max. 512 MByte Flash memory for configuration and operation.

Name	IC	Designator	PS7	MIO	Notes
SPI Flash	N25Q256A11E1240E	U7	QSPI0	MIO0 ... MIO5	Dual parallel booting possible, 32 MByte memory per Flash IC at standard configuration
SPI Flash	N25Q256A11E1240E	U17	QSPI0	MIO7 ... MIO12	As above

Table 10: Peripherals connected to the PS MIO pins

5.2 DDR4 SDRAM

The TE0803-01 SoM is equipped with with four DDR4-2400 SDRAM modules with up to 8 GByte of memory. The SDRAM modules are connected to the Zynq MPSoC's PS DDR controller (bank 504) via 64-bit wide data bus.

Refer to the Xilinx Zynq UltraScale+ datasheet DS925 for more information, if the specific Zynq UltraScale+ MPSoC chip on module supports the maximum data transmission rate of 2400 MByte/s.

5.3 Programmable PLL Clock Generator

Following table illustrates on-board Si5338A programmable clock multiplier chip inputs and outputs:

Input	Connected to	Frequency	Notes
IN1 / IN2	B2B Connector pins J2-4, J2-6 (differential pair)	User	AC decoupling required on base
IN3	On-board Oscillator (U6)	25.000000 MHz	-
Output	**Connected to**	**Frequency**	**Notes**
CLK0 A/B	B2B Connector pins J2-1, J2-3 (differential pair)	User	Default off
CLK1 A/B	B224 CLK1 (only available at ZU5EV MPSoC)	User	Default off
CLK2 A/B	B505 CLK3	User	Default off
CLK3 A/B	B505 CLK2	User	Default off

Table 11: Programmable PLL clock generator input/output

The Si5338A programmable clock generator's control interface pins are exposed to B2B connector J2. For further information refer to the Si5338A data sheet.

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Signal	B2B Connector pin	Function
PLL_SCL / PLL_SDA	J2-90 / J2-92	I^2C interface, external pull-ups needed for SCL/SDA line. I^2C address in current configuration: 1110000b

Table 12: B2B connector pin-out of Si5338A control interface

> ⚠ Si5338A OTP ROM is not programmed by default at delivery, so it is customers responsibility to either configure Si5338A during FSBL or then use Silicon Labs programmer and burn the OTP ROM with customer fixed clock setup.

Si5338A OTP can only be programmed two times, as different user configurations may require different setup, TE0803 is normally shipped with blank OTP.
Refer to Si5338A datasheet for more information.

5.4 Clocking

The TE0803-01 SoM is equipped with two on-board oscillators to provide the Zynq MPSoC's PS configuration bank 503 with reference clock signals.

Clock	Frequency	Bank 503 Pin	Connected to
PS_CLK	33.333333 MHz	R16	MEMS oscillator, U32
PS_PAD (RTC)	32.768 kHz	N17/N18	Quartz crystal, Y2

Table 13: Reference clock-signals to PS configuration bank 503

5.5 On-board LEDs

LED	Color	Connected to	Description and Notes
D1	Red	DONE signal (PS Configuration Bank 503)	This LED goes ON when power has been applied to the module and stays ON until MPSoC's programmable logic is configured properly.

Table 14: LED's description

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6 Power and Power-On Sequence

6.1 Power Consumption

The maximum power consumption of a module mainly depends on the design which is running on the FPGA.

Xilinx provide a power estimator excel sheets to calculate power consumption. It's also possible to evaluate the power consumption of the developed design with Vivado. See also Trenz Electronic Wiki FAQ.

Power Input Pin	Typical Current
DCDCIN	TBD*
LP_DCDC	TBD*
PL_DCIN	TBD*
PS_BATT	TBD*

Table 15: Maximum current of power supplies. *To Be Determined soon with reference design setup.

Power supply with minimum current capability of 3A for system startup is recommended. For the lowest power consumption and highest efficiency of on board DC/DC regulators it is recommended to powering the module from one single 3.3V supply. Except 'PS_BATT', all input power supplies have a nominal value of 3.3V. Although the input power supplies can be powered up in any order, it is recommended to power them up simultaneously.

The TE0803 module equipped with the Xilinx Zynq UltraScale+ MPSoC delivers a heterogeneous multi-processing system with integrated programmable logic and independently operable elements and is designed to meet embedded system power management requirement by advanced power management features. This features allow to offset the power and heat constraints against overall performance and operational efficiency.

This features allowing highly flexible power management are achieved by establishing Power Domains for power isolation. The Zynq UltraScale+ MPSoC has multiple power domains, whereby each power domain requires its own particular external DC-DC converters.

The Processing System contains three Power Domains:

- Battery Power Domain (BBRAM and RTC)
- Full-Power Domain (Application Processing Unit, DDR Controller, Graphics Processing Unit and High-Speed Connectivity)
- Low-Power Domain (Real-Time Processing Unit, Security and Configuration Unit, Platform Management Unit, System Monitor and General Connectivity)

The fourth Power Domain is for the Programmable Logic (PL). If individual Power Domain control is not required, power rails can be shared between domains.

On the TE0803 SoM, following Power Domains can be powered up individually with power rails available on the B2B connectors:

- Full-Power Domain, supplied by power rail **'DCDCIN'**
- Low-Power Domain, supplied by power rail **'LP_DCDC'**
- Programmable Logic, supplied by power rail **'PL_DCIN'**
- Battery Power Domain, supplied by power rail **'PS_BATT'**

Each Power Domain has its own "Enabling"- and "Power Good"-signals. The power rail **'GT_DCDC'** is only necessary for variants of the TE0803 module with the Xilinx Zynq UltraScale+ ZU4CG or ZU4EV MPSoC to generate the voltages for the available Xilinx GTH unit.

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6.2 Power Distribution Dependencies

The power rails 'DCDCIN', 'LP_DCDC', 'PL_DCIN', 'PS_BATT' have to be powered up on the assigned pins of the B2B connectors as listed on the section "Power Rails". Except 'PS_BATT' (see section "Recommended Operation Conditions"), all power-rails can be powered up, with 3.3V power sources, also shared, if Power Domain control is not required.

There are following dependencies how the initial voltages of the power rails on the B2B connectors are distributed to the on-board DC-DC converters, which power up further DC-DC converters and the particular on-board voltages:

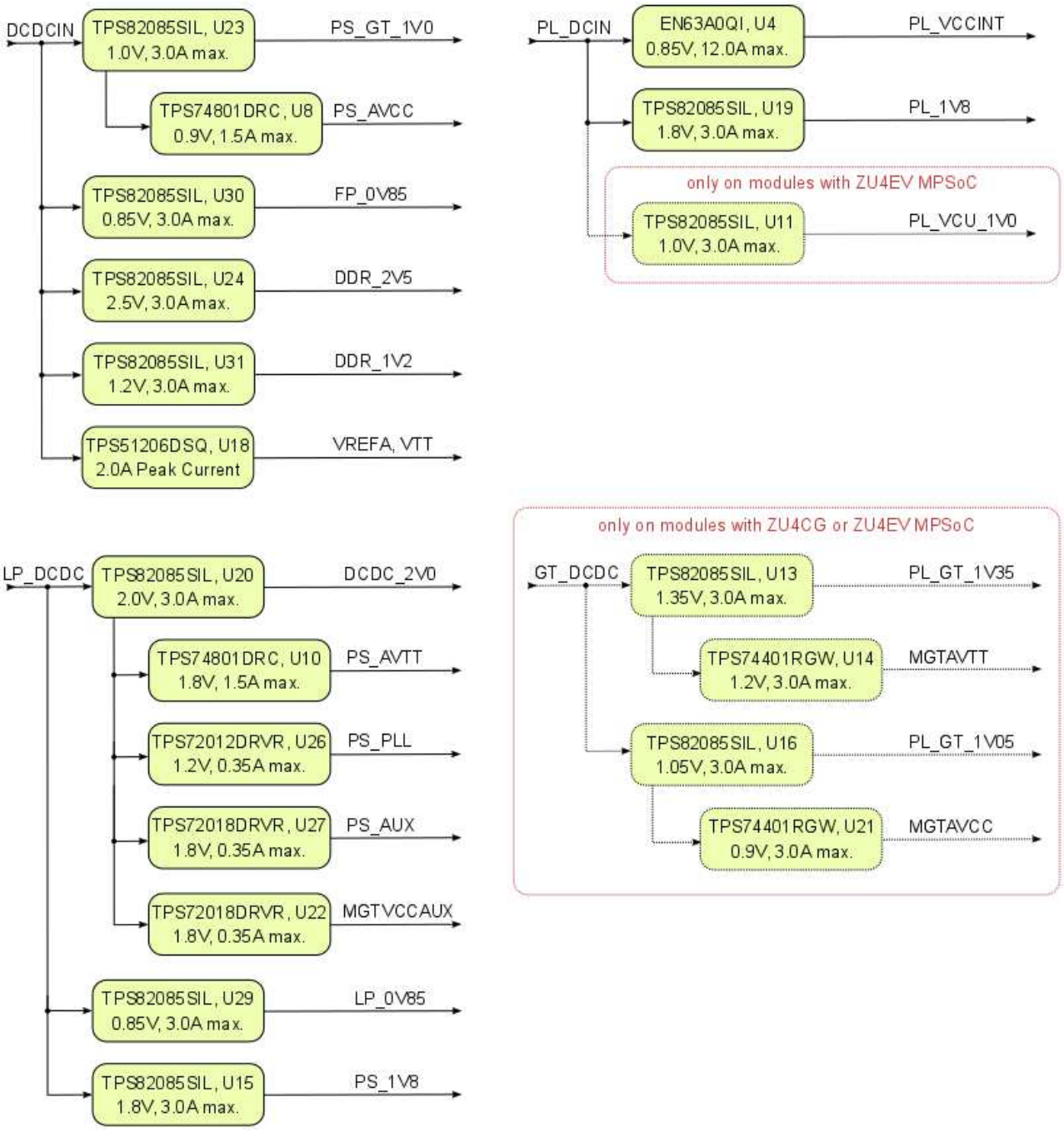


Figure 3: Power Distribution Diagram

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⚠ Current rating of Samtec Razor Beam LP Terminal/Socket Strip ST5/SS5 B2B connectors is 1.5 A per pin (1 pin powered per row).

6.3 Power-On Sequence Diagram

The TE0803 SoM meets the recommended criteria to power up the Xilinx Zynq UltraScale+ MPSoC properly by keeping a specific sequence of enabling the on-board DC-DC converters dedicated to the particular Power Domains and powering up the on-board voltages.

The on-board voltages of the TE0803 SoM will be powered-up in order of a determined sequence by activating the above-mentioned power rails and the Enable-Signals of the DC-DC converters. The on-board voltages will be powered up at three steps.

1. Low-Power Domain (LPD)
2. Programmable Logic (PL) and Full-Power Domain (FPD)
3. PS GTR transceiver and DDR memory (additionally GTH transceiver at modules with ZU5EV MPSoC)

Hence, those three power instances will be powered up consecutively and the Power-Good-Signals of the previous instance has to be asserted.

Following diagram clarifies the sequence of enabling the three power instances utilizing the DC-DC converter control signals ('Enable', 'Power-Good'), which will power-up in descending order as listed in the blocks of the diagram.

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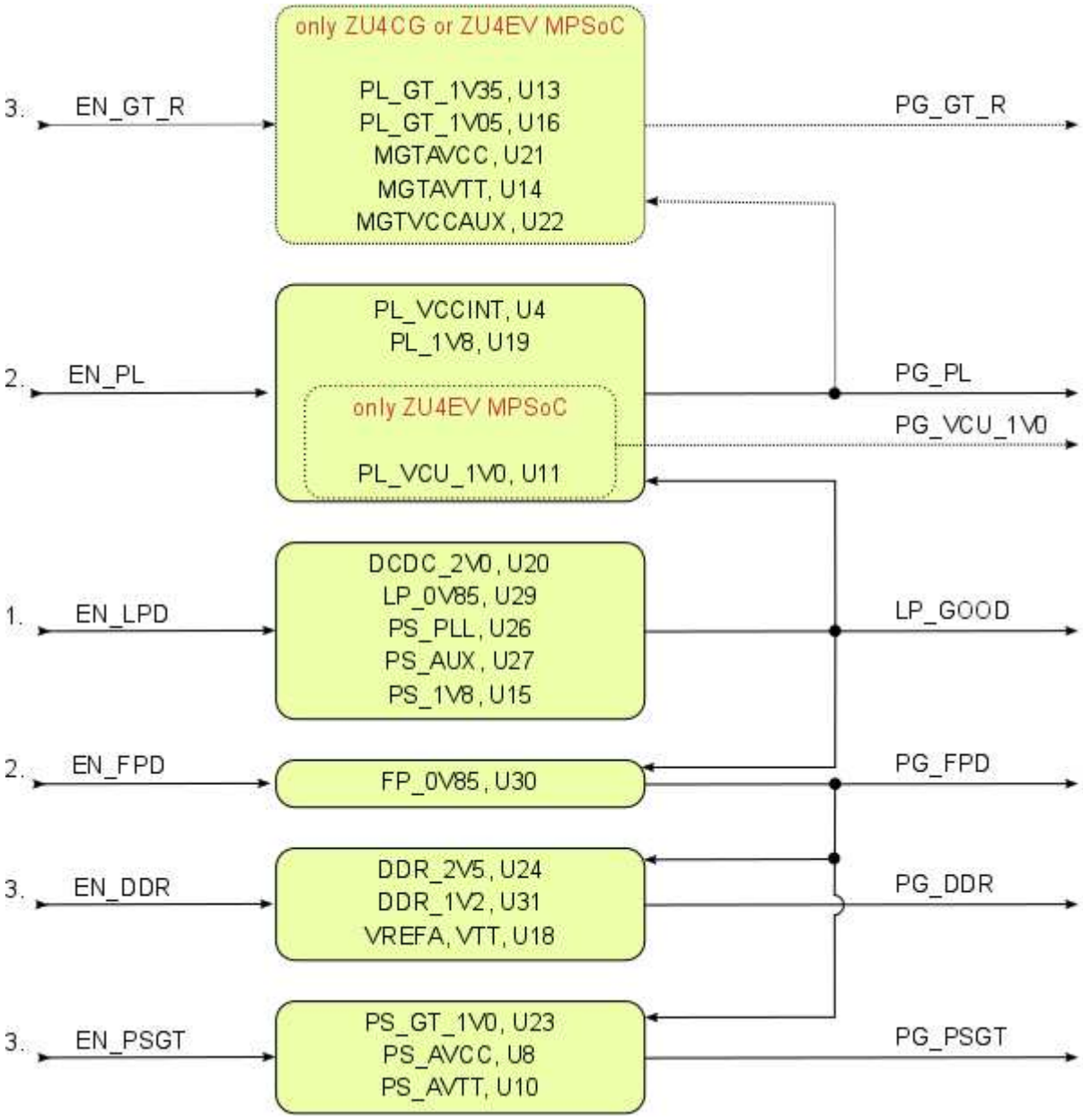


Figure 4: Power-On Sequence Utilizing DC-DC Converter Control Signals

6.4 Operation Conditions of the DC-DC Converter Control Signals

The control signals have to be asserted on the B2B connector J2, whereby some of the Power Good Signals need external pull-up resistors.

Enable-Signal	B2B Connector Pin	Max. Voltage	Note	Power-Good-Signal	B2B Connector Pin	Pull-up Resistor	Note
EN_LPD	J2-108	6V	TPS82085SIL data sheet	LP_GOOD	J2-106	4K7, pulled up to LP_DCDC	-
EN_FPD	J2-102	DCDCIN	NC7S08P5X data sheet	PG_FPD	J2-110	4K7, pulled up to DCDCIN	-

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EN_PL	J2-101	max PL_DCIN	Left floating for logic high (drive to GND for logic low)	PG_PL	J2-104	External pull-up needed (max. voltage 'GT_DCDC'), Max. sink current 1 mA	TPS82085SIL / NC7S08P5X datasheet
EN_DDR	J2-112	DCDCIN	NC7S08P5X data sheet	PG_DDR	J2-114	4K7, pulled up to DCDCIN	-
EN_PSGT	J2-84	DCDCIN	NC7S08P5X data sheet	PG_PSGT	J2-82	External pull-up needed (max. 5.5V), Max. sink current 1 mA	TPS74801 datasheet
EN_GT_R	J2-95	GT_DCDC	NC7S08P5X data sheet	PG_GT_R	J2-91	External pull-up needed (max. 5.5V), Max. sink current 1 mA	TPS74401 datasheet
-	-	-	-	PG_VCU_1V0	J2-97	External pull-up needed (max. 5.5V), Max. sink current 1 mA	TPS82085SIL datasheet

Table 16: Recommended operation conditions of DC-DC converter control signals

To avoid any damage to the MPSoC module, check for stabilized on-board voltages in steady state before powering up the MPSoC's I/O bank voltages VCCOx. All I/O's should be tri-stated during power-on sequence.

Core voltages and main supply voltages have to reach stable state and their "Power Good" signals have to be asserted before other voltages like bank I/O voltages (VCCOx) can be powered up.

It is important that all PS and PL I/Os are tri-stated at power-on until the "Power Good" signals are high, meaning that all on-module voltages have become stable and module is properly powered up.

See Xilinx datasheet DS925 for additional information. User should also check related base board documentation when intending base board design for TE0803 SoM.

6.5 Voltage Monitor Circuit

The voltages 'LP_DCDC' and 'LP_0V85' are monitored by the voltage monitor circuit U41, which generates the POR_B reset signal at Power-On. A manual reset is also possible by driving the MR-pin (J2-83) to GND. Leave this pin unconnected or connect to VDD (LP_DCDC) when unused.

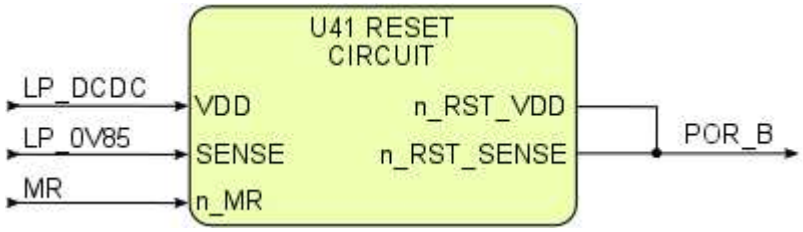


Figure 5: Voltage monitor circuit

6.6 Power Rails

Voltages on B2B Connectors	B2B J1 Pin	B2B J2 Pin	B2B J3 Pin	B2B J4 Pin	Input / Output	Note
PL_DCIN	J1-151, J1-153, J1-157, J1-159	-	-	-	Input	-
DCDCIN	-	J2-154, J2-156, J2-158, J2-160, J2-153, J2-155, J2-157, J2-159	-	-	Input	-
LP_DCDC	-	J2-138, J2-140, J2-142, J2-144	-	-	Input	-
PS_BATT	-	J2-125	-	-	Input	-
GT_DCDC	-	-	J3-157, J3-158, J3-159, J3-160	-	Input	-
PS_1V8	-	J2-99	J3-148	-	Output	Internal voltage level 1.8V nominal output
PL_1V8	J1-91, J1-121	-	-	-	Output	Internal voltage level 1.8V nominal output
DDR_1V2	-	J2-135	-	-	Output	Internal voltage level 1.2V nominal output

Table 17: Power rails of the MPSoC module on accessible connectors

6.7 Bank Voltages

Bank	Type	Schematic Name / B2B Connector Pins	Voltage	Reference Input Voltage	Voltage Range
25	HD	VCCO25, pins J3-15, J3-16	User	-	Max. 3.3V
26	HD	VCCO26, pins J3-43, J3-44	User	-	Max. 3.3V

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Bank	Type	Schematic Name / B2B Connector Pins	Voltage	Reference Input Voltage	Voltage Range
64	HP	VCCO64, J4-58, J4-106	User	VREF_64, pin J4-88	Max. 1.8V
65	HP	VCCO65, J4-69, J4-105	User	VREF_65, pin J4-15	Max. 1.8V
66	HP	VCCO66, J1-90, J1-120	User	VREF_66, pin J1-108	Max. 1.8V
500	MIO	PS_1V8	1.8V	-	-
501	MIO	PS_1V8	1.8V	-	-
502	MIO	PS_1V8	1.8V	-	-
503	CONFIG	PS_1V8	1.8V	-	-

Table 18: Range of MPSoC module's bank voltages

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7 B2B connectors

5.2 x 7.6 cm UltraSoM+ modules use four Samtec Razor Beam LP Terminal Strip (ST5) on the bottom side.

- 4x REF-192552-02 (160-pins)
  - ST5 Mates with SS5

5.2 x 7.6 cm UltraSoM+ carrier use four Samtec Razor Beam LP Socket Strip (SS5) on the top side.

- 4x REF192552-01 (160-pins)
  - SS5 Mates with ST5

7.1 Features

- Board-to-Board Connector 160-pins, 80 contacts per row
- Ultrafine .0197" (0.50 mm) pitch
- Narrow body design saves space on board
- Lead style -03.5
- Samtec 28+ Gbps Solution
- Mates with: ST5
- Insulator Material: Liquid Crystal Polymer, schwarz
- Operating Temperature Range: -55°C bis +125°C
- Lead-Free Solderable: Yes
- RoHS Konform: Yes

7.2 Connector Stacking height

When using the standard type on baseboard and module, the mating height is 5 mm.

Other mating heights are possible by using connectors with a different height:

Order number	REF number	Samtec Number	Type	Contribution to stacking height	Comment
27219	REF192552-01	SS5-80-3.50-L-D-K-TR	Baseboard connector	3.5mm	Standard connector used on modules
27018	REF-189545-02	SS5-80-3.00-L-D-K-TR	Baseboard connector	3 mm	Assembly option on request
27220	REF-192552-02	ST5-80-1.50-L-D-P-TR	Module connector	1.5 mm	Standard connector used on modules
27017	REF-189545-01	ST5-80-1.00-L-D-P-TR	Module connector	1 mm	Assembly option on request

The module can be manufactured using other connectors upon request.

7.3 Current Rating

Current rating of Samtec Razor Beam LP Terminal/Socket Strip ST5/SS5 B2B connectors is 1.5 A per pin (1 pin powered per row).

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7.4 Connector Speed Ratings

The connector speed rating depends on the stacking height:

Stacking height	Speed rating
4 mm, Single-Ended	13GHz/26Gbps
4 mm, Differential	13.5GHz/27Gbps
5 mm, Single-Ended	13.5GHz/27Gbps
5 mm, Differential	20GHz/40 Gbps

The SS5/ST5 series board-to-board spacing is currently available in 4mm (0.157"), 4.5mm (0.177") and 5mm (0.197") stack heights.

The data in the reports is applicable only to the 4mm and 5mm board-to-board mated connector stack height.

7.5 Manufacturer Documentation

Geändert
30 05, 2017 by Susanne Kunath
30 05, 2017 by Susanne Kunath
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8 Variants Currently In Production

Trenz shop TE0803 overview page	
English page	German page

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9 Technical Specifications

9.1 Absolute Maximum Ratings

Parameter	Min	Max	Unit	Notes / Reference Document
PL_DCIN	-0.3	7	V	TPS82085SIL / EN63A0QI data sheet
DCDCIN	-0.3	7	V	TPS82085SIL / TPS51206PSQ data sheet
LP_DCDC	-0.3	4	V	TPS3106K33DBVR data sheet
GT_DCDC	-0.3	7	V	TPS82085SIL data sheet
PS_BATT	-0.5	2	V	Xilinx DS925 data sheet
VCCO for HD I/O banks	-0.5	3.4	V	Xilinx DS925 data sheet
VCCO for HP I/O banks	-0.5	2	V	Xilinx DS925 data sheet
VREF	-0.5	2	V	Xilinx DS925 data sheet
I/O input voltage for HD I/O banks	-0.55	VCCO + 0.55	V	Xilinx DS925 data sheet
I/O input voltage for HP I/O banks	-0.55	VCCO + 0.55	V	Xilinx DS925 data sheet
PS I/O input voltage (MIO pins)	-0.5	VCCO_PSIO + 0.55	V	Xilinx DS925 data sheet, VCCO_PSIO 1.8V nominally
Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage	-0.5	1.2	V	Xilinx DS925 data sheet
Voltage on input pins of NC7S08P5X 2-Input AND Gate	-0.5	VCC + 0.5	V	NC7S08P5X data sheet, see schematic for VCC
Voltage on input pins (nMR) of TPS3106K33DBVR Voltage Monitor, U41	-0.3	VDD + 0.3	V	TPS3106 data sheet, VDD = LP_DCDC
"Enable"-signals on TPS82085SIL ('EN_LPD')	-0.3	7	V	TPS82085SIL data sheet
Storage temperature (ambient)	-40	100	°C	ROHM Semiconductor SML-P11 Series data sheet

⚠ Assembly variants for higher storage temperature range are available on request.

9.2 Recommended Operating Conditions

Parameter	Min	Max	Unit	Notes / Reference Document
PL_DCIN	2.5	6	V	EN63A0QI / TPS82085SIL data sheet

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Parameter	Min	Max	Unit	Notes / Reference Document
DCDCIN	3.1	6	V	TPS82085SIL / TPS51206PSQ data sheet
LP_DCDC	2.5	3.6	V	TPS82085SIL / TPS3106K33DBVR data sheet
GT_DCDC	2.5	6	V	TPS82085SIL data sheet
PS_BATT	1.2	1.5	V	Xilinx DS925 data sheet
VCCO for HD I/O banks	1.14	3.4	V	Xilinx DS925 data sheet
VCCO for HP I/O banks	0.95	1.9	V	Xilinx DS925 data sheet
I/O input voltage for HD I/O banks.	-0.2	VCCO + 0.2	V	Xilinx DS925 data sheet
I/O input voltage for HP I/O banks	-0.2	VCCO + 0.2	V	Xilinx DS925 data sheet
PS I/O input voltage (MIO pins)	-0.2	VCCO_PSIO + 0.2	V	Xilinx DS925 data sheet, VCCO_PSIO 1.8V nominally
Voltage on input pins of NC7S08P5X 2-Input AND Gate	0	VCC	V	NC7S08P5X data sheet, see schematic for connected VCCs
Voltage on input pins (MR) of TPS3106K33DBVR Voltage Monitor, U41	0	VDD	V	TPS3106 data sheet, VDD = LP_DCDC

⚠ Please check Xilinx datasheet DS925 for complete list of absolute maximum and recommended operating ratings.

9.3 Operating Temperature Ranges

Extended grade: 0°C to +100°C.

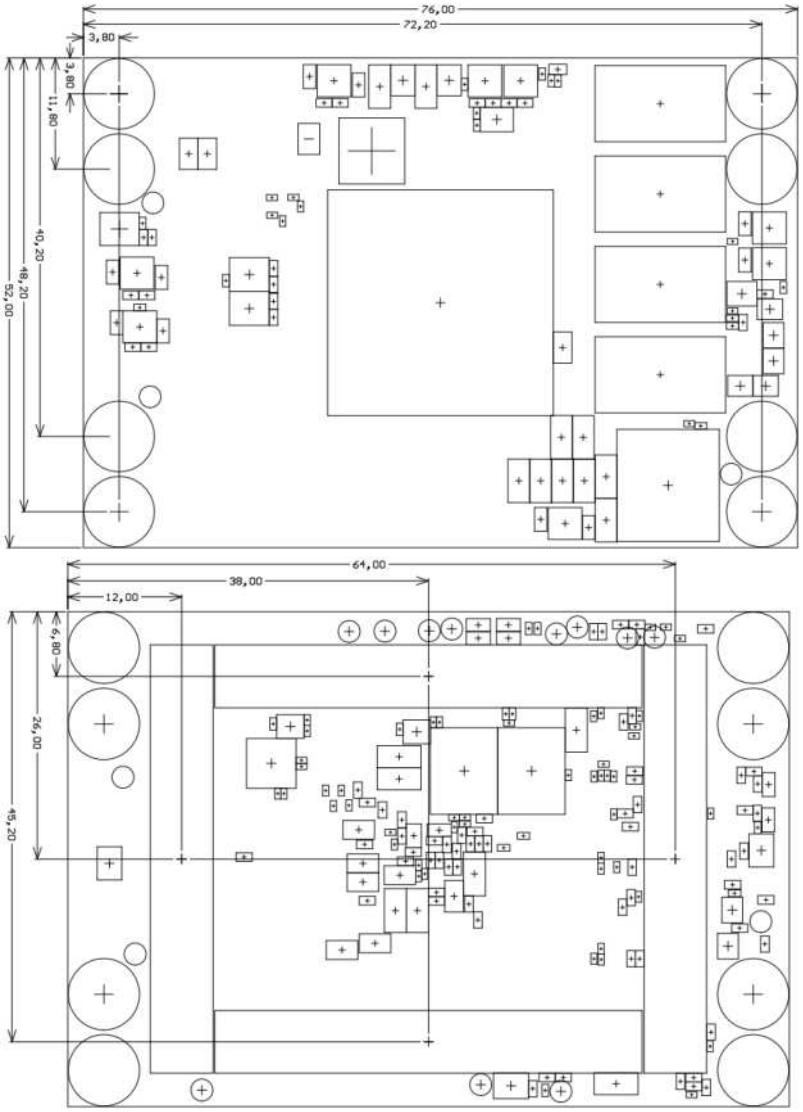
The module operating temperature range depends also on customer design and cooling solution. Please contact us for options.

9.4 Physical Dimensions

- Module size: 52 mm × 76 mm. Please download the assembly diagram for exact numbers
- Mating height with standard connectors: 4mm
- PCB thickness: 1.6mm
- Highest part on PCB: approx. 3mm. Please download the step model for exact numbers

All dimensions are given in millimeters.

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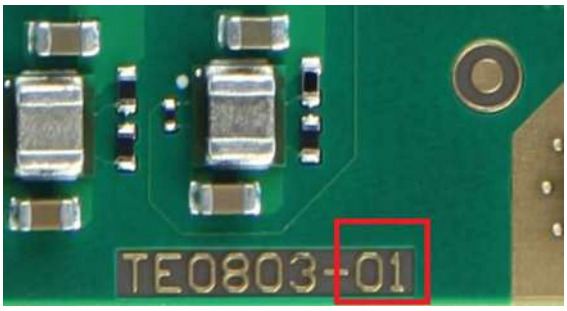
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10 Revision History

10.1 Hardware Revision History

Date	Revision	Notes	Link to PCN	Documentation Link
2016-12-23	01	First production release	-	TE0803-01

Hardware revision number is written on the PCB board together with the module model number separated by the dash.



10.2 Document Change History

Date	Revision	Contributors	Description
2018-08-06	v.28	John Hartfiel	• typo correction
2017-11-13	v.23	Ali Naseri	• updated B2B connector max. current rating per pin
2017-11-13	v.19	John Hartfiel	• rework B2B section
2017-10-19	v.18	John Hartfiel	• Removed ES1 Note
2017-08-15	v.17	Vitali Tsiukala	• Changed Signals Count in the table B2B-connectors
2017-08-07	v.14	Jan Kumann	• New smaller images. • New QSPI Flash MIO mapping table. • Temperature information changes. • Few corrections.
2017-05-17	V.4	Ali Naseri	Current TRM release.
2017-05-10	v.1	Ali Naseri	Initial document.

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