TRS3232E
3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH ±15-kV IEC ESD PROTECTION

SLLS790 – JUNE 2007

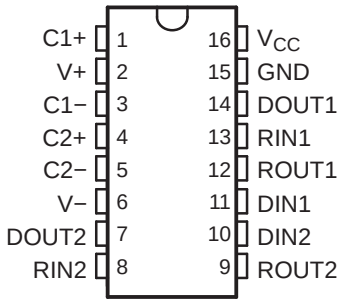
FEATURES

- **ESD Protection for RS-232 Bus Pins**
  - **±15-kV Human Body Model (HBM)**
  - **±8 kV (IEC61000-4-2, Contact Discharge)**
  - **±15 kV (IEC61000-4-2, Air-Gap Discharge)**
- **Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Operates With 3-V to 5.5-V V_{CC} Supply**
- **Operates up to 250 kbit/s**
- **Two Drivers and Two Receivers**
- **Low Supply Current . . . 300 µA Typ**
- **External Capacitors . . . 4 × 0.1 µF**
- **Accepts 5-V Logic Input With 3.3-V Supply**
- **Pin Compatible to Alternative High-Speed Device (1 Mbit/s)**
  - **TRSF3232E**

APPLICATIONS

- **Battery-Powered Systems**
- **PDAs**
- **Notebooks**
- **Laptops**
- **Palmtop PCs**
- **Hand-Held Equipment**

D, DB, DW, OR PW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC – D	Tube of 40	TRS3232ECD	TRS3232EC
		Reel of 2500	TRS3232ECDR	
	SOIC – DW	Tube of 40	TRS3232ECDW	TRS3232EC
		Reel of 2000	TRS3232ECDWR	
	SSOP – DB	Tube of 80	TRS3232ECDB	RS32EC
		Reel of 2000	TRS3232ECDBR	
	TSSOP – PW	Tube of 90	TRS3232ECPW	RS32EC
		Reel of 2000	TRS3232ECPWR	
–40°C to 85°C	SOIC – D	Tube of 40	TRS3232EID	TRS3232EI
		Reel of 2500	TRS3232EIDR	
	SOIC – DW	Tube of 40	TRS3232EIDW	TRS3232EI
		Reel of 2000	TRS3232EIDWR	
	SSOP – DB	Tube of 80	TRS3232EIDB	RS32EI
		Reel of 2000	TRS3232EIDBR	
	TSSOP – PW	Tube of 90	TRS3232EIPW	RS32EI
		Reel of 2000	TRS3232EIPWR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The TRS3232E device consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV IEC ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at data signaling rates up to 250 kbit/s and a maximum of 30-V/µs driver output slew rate.

FUNCTION TABLES

Each Driver(1)

INPUT DIN	OUTPUT DOUT
L	H
H	L

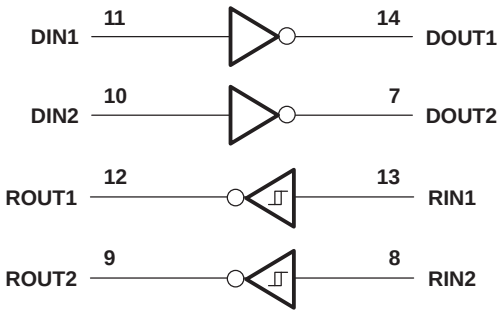
(1) H = high level, L = low level

Each Receiver(1)

INPUT RIN	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level,
Open = input disconnected or
connected driver off

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.3	6	V
V+	Positive output supply voltage range(2)		–0.3	7	V
V–	Negative output supply voltage range(2)		0.3	–7	V
V+ – V–	Supply voltage difference(2)			13	V
V_I	Input voltage range	Drivers	–0.3	6	V
		Receivers	–25	25	
V_O	Output voltage range	Drivers	–13.2	13.2	V
		Receivers	–0.3	V_{CC} + 0.3	
θ_{JA}	Package thermal impedance(3)(4)	D package		73	°C/W
		DB package		82	
		DW package		57	
		PW package		108	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.
(3) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)

See Figure 4

				MIN	NOM	MAX	UNIT
	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	
V_{IH}	Driver high-level input voltage	DIN	V_{CC} = 3.3 V	2		5.5	V
			V_{CC} = 5 V	2.4		5.5	
V_{IL}	Driver low-level input voltage	DIN		0		0.8	V
V_I	Receiver input voltage			–25		25	V
T_A	Operating free-air temperature		TRS3232EC	0		70	°C
			TRS3232EI	–40		85	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

Electrical Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
I_{CC}	Supply current	No load, V_{CC} = 3.3 V or 5 V		0.3	1	mA

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

DRIVER SECTION

Electrical Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = GND	5	5.4		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = V_{CC}	–5	–5.4		V
I_{IH}	High-level input current	V_I = V_{CC}			±0.01	±1	µA
I_{IL}	Low-level input current	V_I at GND			±0.01	±1	µA
I_{OS}(3)	Short-circuit output current	V_{CC} = 3.6 V,	V_O = 0 V		±35	±60	mA
		V_{CC} = 5.5 V,	V_O = 0 V		±35	±60	
r_o	Output resistance	V_{CC}, V+, and V– = 0 V,	V_O = ±2 V	300	10M		Ω

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

Switching Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
	Maximum data rate	C_L = 1000 pF, One DOUT switching,	R_L = 3 kΩ, See Figure 1	150	250		kbit/s
$t_{sk(p)}$	Pulse skew(3)	C_L = 150 pF to 2500 pF, See Figure 2	R_L = 3 kΩ to 7 kΩ,		300		ns
SR(tr)	Slew rate, transition region (see Figure 1)	R_L = 3 kΩ to 7 kΩ, V_{CC} = 3.3 V	C_L = 150 pF to 1000 pF	6		30	V/µs
			C_L = 150 pF to 2500 pF	4		30	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

RECEIVER SECTION

Electrical Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA	V_{CC} – 0.6	V_{CC} – 0.1		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3 V		1.5	2.4	V
		V_{CC} = 5 V		1.8	2.4	
$V_{IT–}$	Negative-going input threshold voltage	V_{CC} = 3.3 V	0.6	1.2		V
		V_{CC} = 5 V	0.8	1.5		
V_{hys}	Input hysteresis (V_{IT+} – $V_{IT–}$)			0.3		V
r_i	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

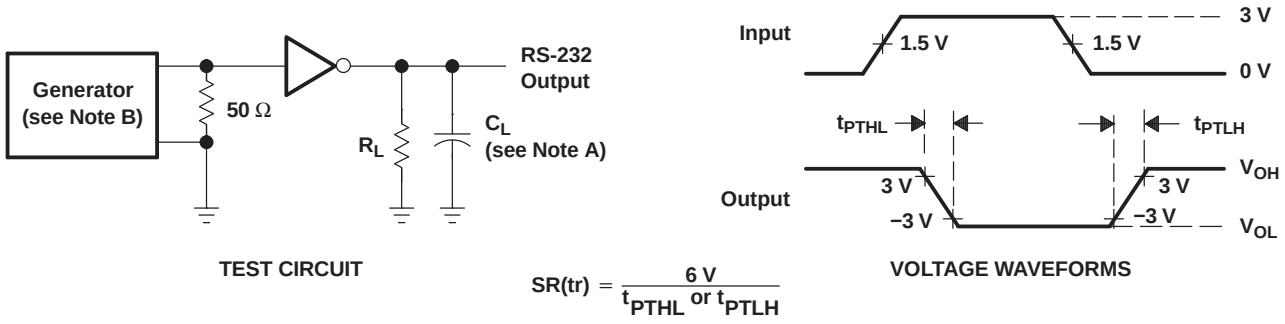
Switching Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 3)

PARAMETER		TEST CONDITIONS	TYP(2)	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF	300	ns
t_{PHL}	Propagation delay time, high- to low-level output		300	ns
$t_{sk(p)}$	Pulse skew(3)		300	ns

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} – t_{PHL}|$ of each channel of the same device.

PARAMETER MEASUREMENT INFORMATION



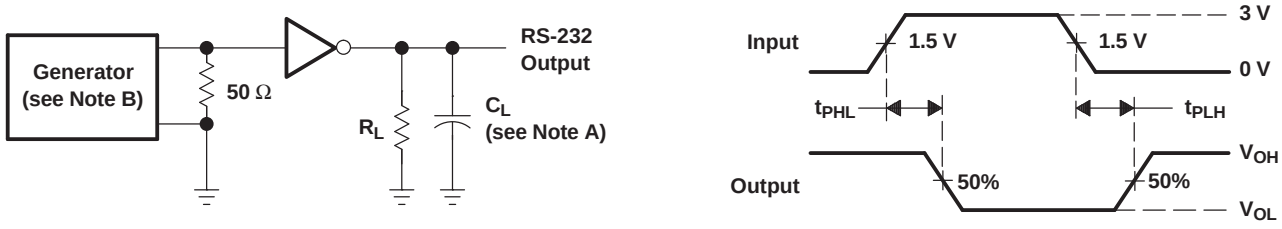
TEST CIRCUIT

$$SR(tr) = \frac{6\ V}{t_{PTHL} \text{ or } t_{PTLH}}$$

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 1. Driver Slew Rate

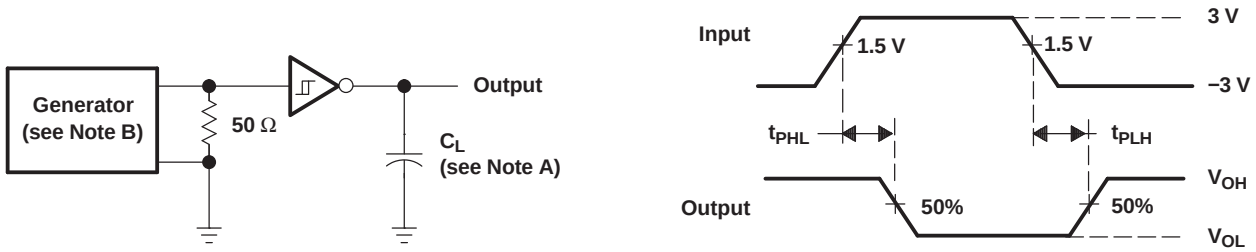


TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 2. Driver Pulse Skew



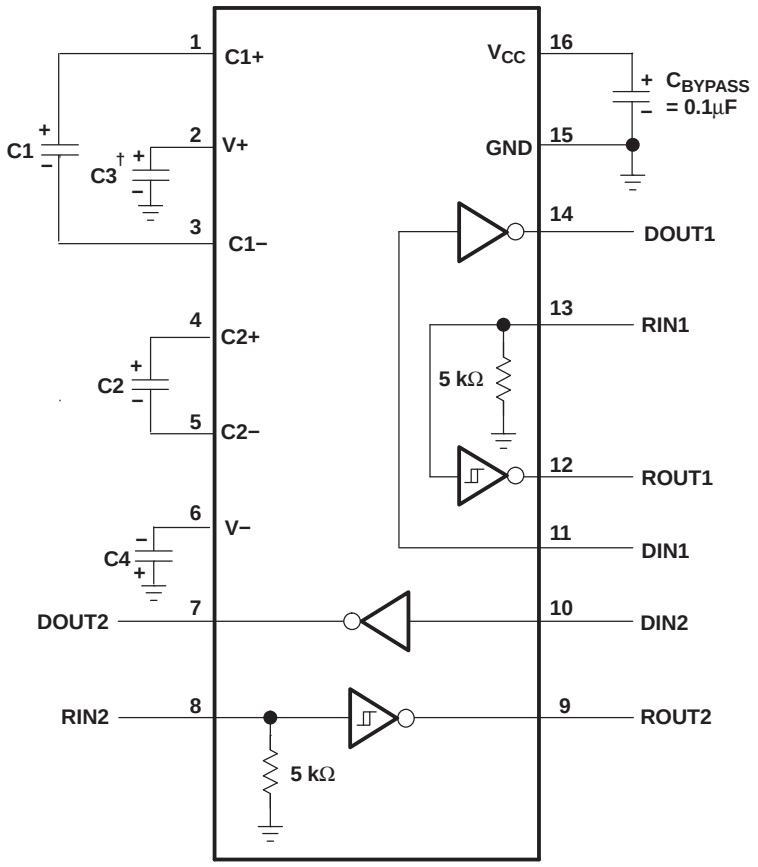
TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 3. Receiver Propagation Delay Times

APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

Figure 4. Typical Operating Circuit and Capacitor Values

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TRS3232ECD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232ECDB	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232ECDBG4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232ECDBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232ECDBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232ECDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232ECDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232ECDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232ECDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232ECDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232ECDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232ECDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232ECPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232ECPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232ECPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232ECPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232EID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232EIDB	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232EIDBG4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232EIDBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232EIDBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232EIDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232EIDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232EIDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232EIDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TRS3232EIDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232EIDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232EIDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232EIPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232EIPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232EIPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRS3232EIPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

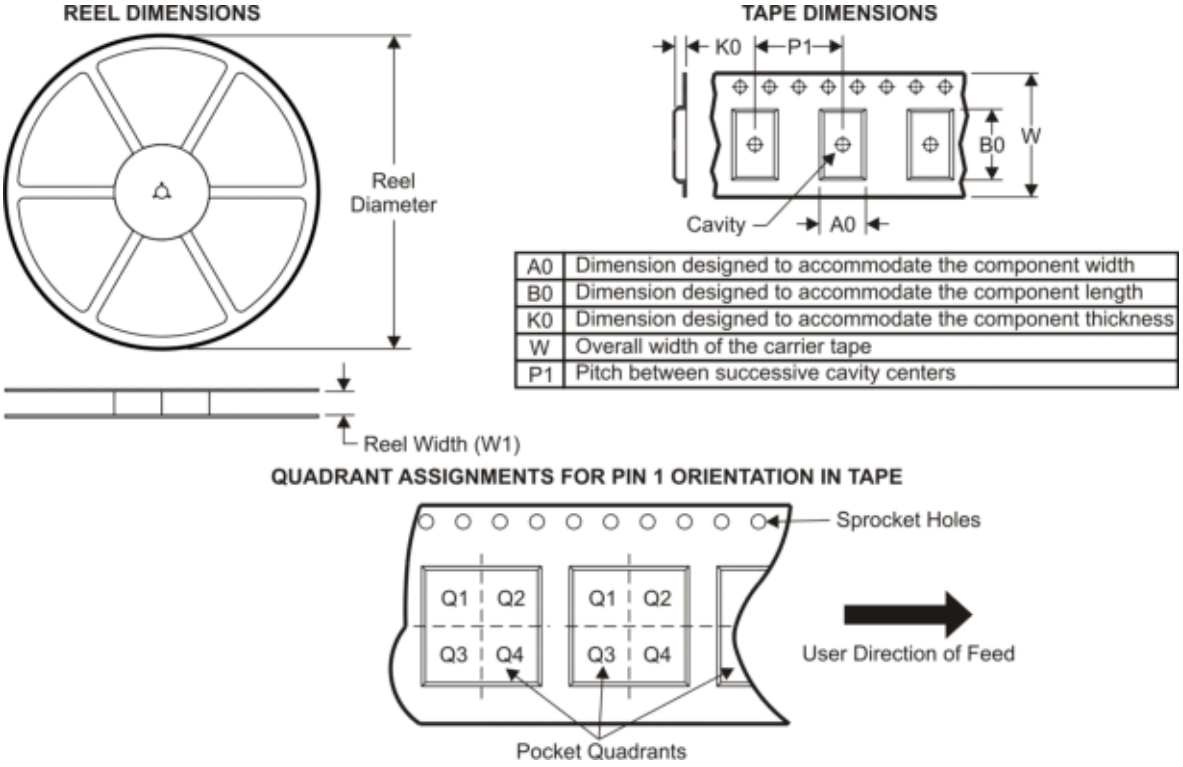
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

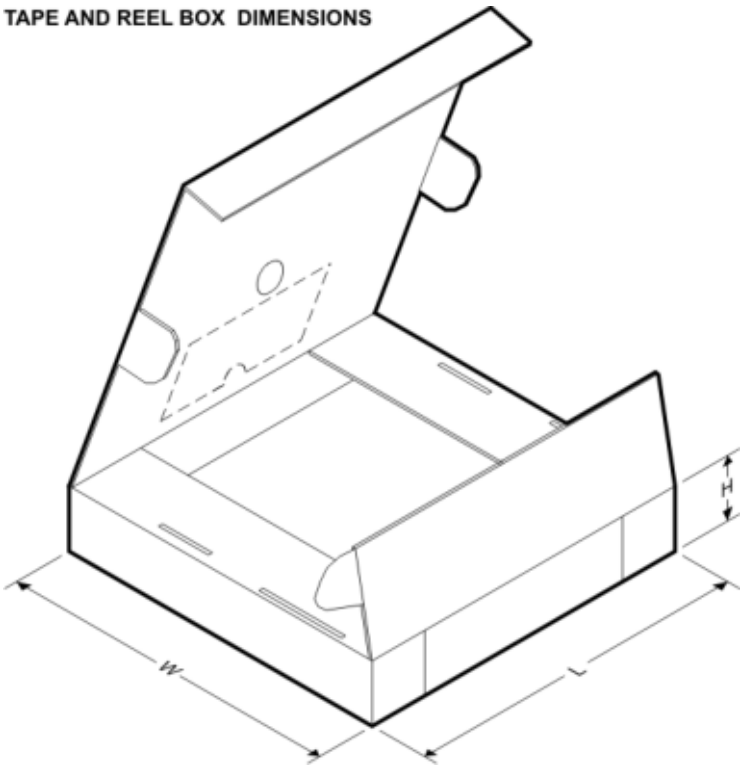


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS3232ECDBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TRS3232ECDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRS3232ECDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TRS3232ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRS3232EIDBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TRS3232EIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRS3232EIDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TRS3232EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

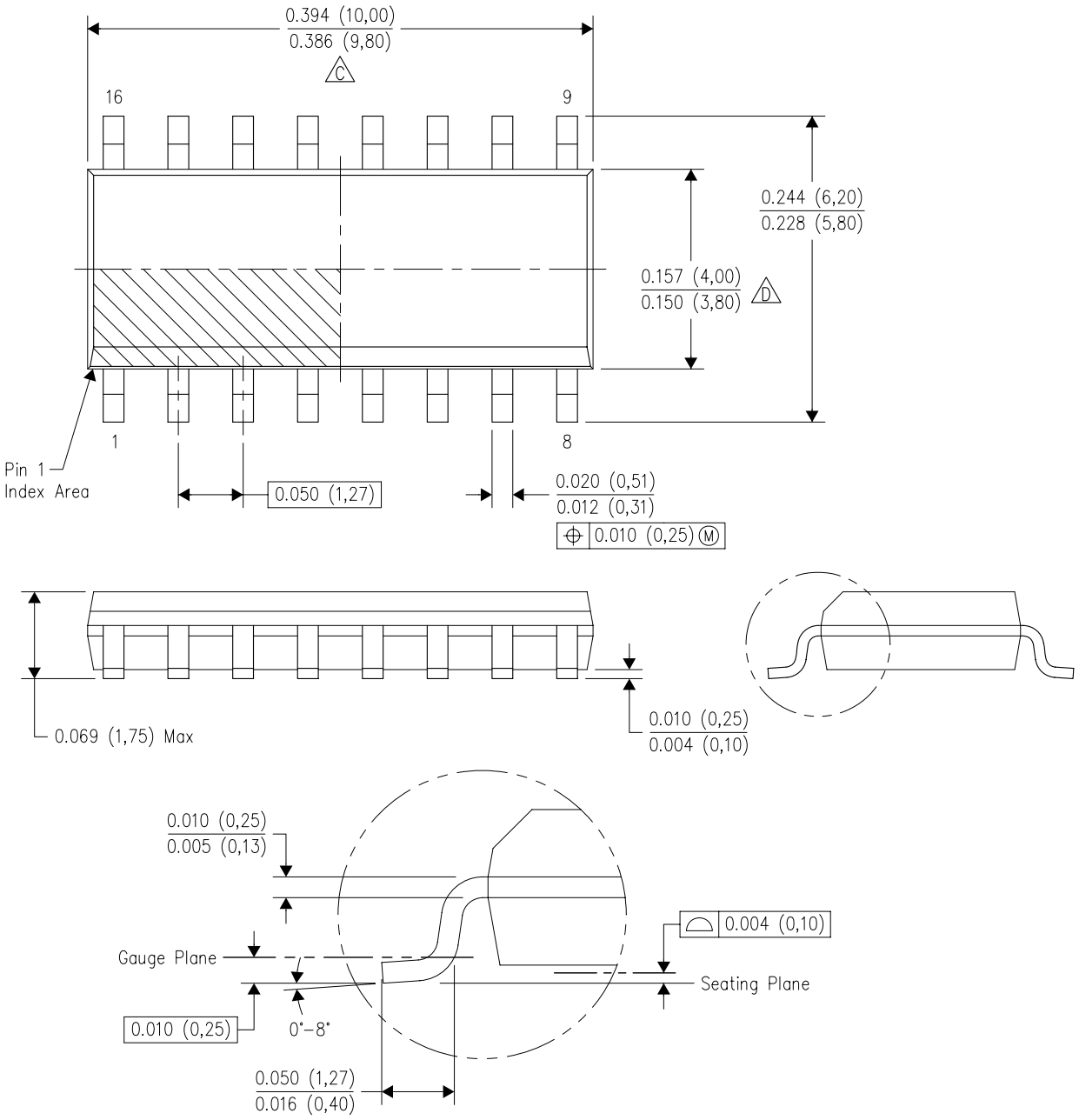
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

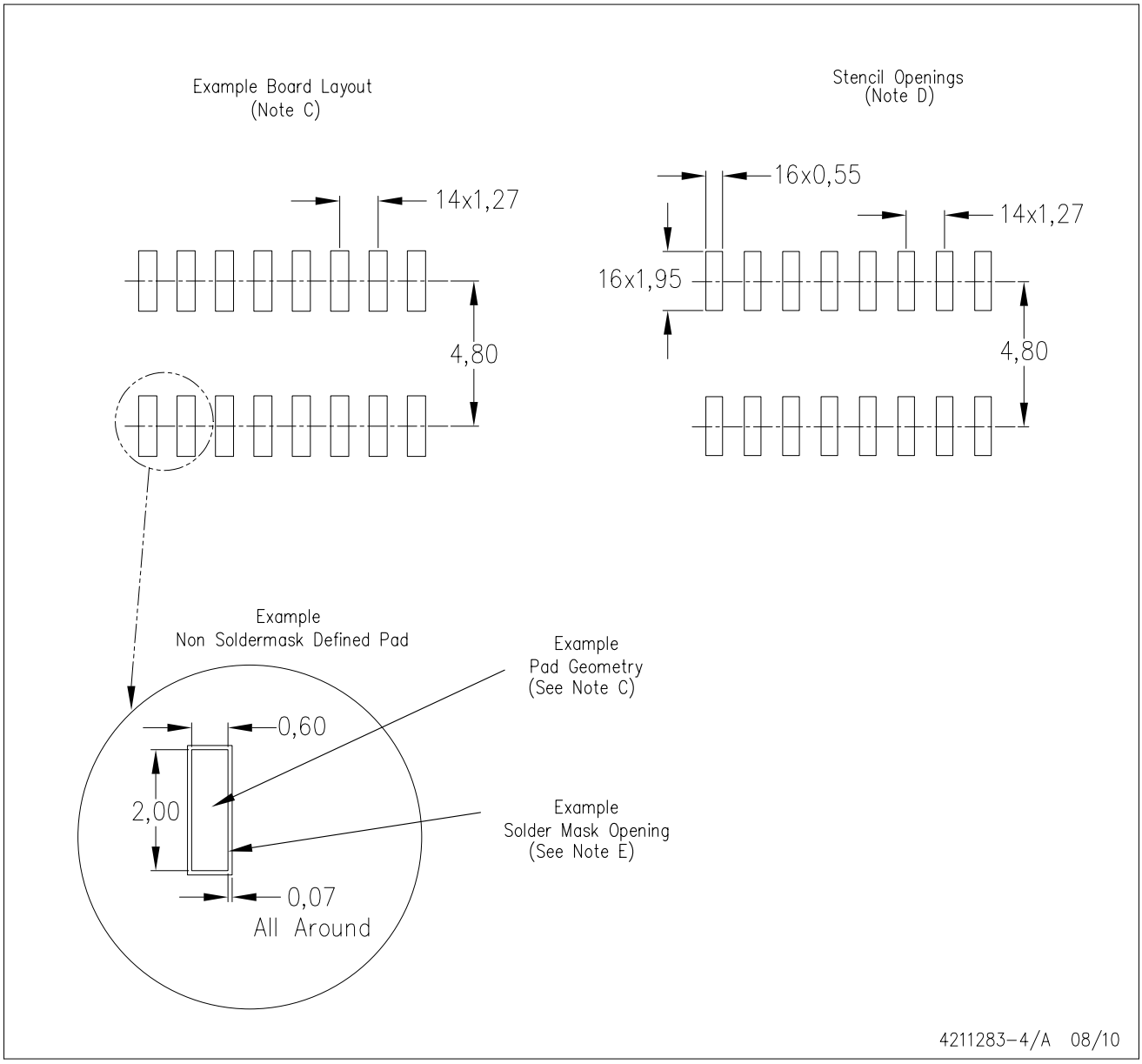
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS3232ECDBR	SSOP	DB	16	2000	346.0	346.0	33.0
TRS3232ECDR	SOIC	D	16	2500	346.0	346.0	33.0
TRS3232ECDWR	SOIC	DW	16	2000	346.0	346.0	33.0
TRS3232ECPWR	TSSOP	PW	16	2000	346.0	346.0	29.0
TRS3232EIDBR	SSOP	DB	16	2000	346.0	346.0	33.0
TRS3232EIDR	SOIC	D	16	2500	346.0	346.0	33.0
TRS3232EIDWR	SOIC	DW	16	2000	346.0	346.0	33.0
TRS3232EIPWR	TSSOP	PW	16	2000	346.0	346.0	29.0

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



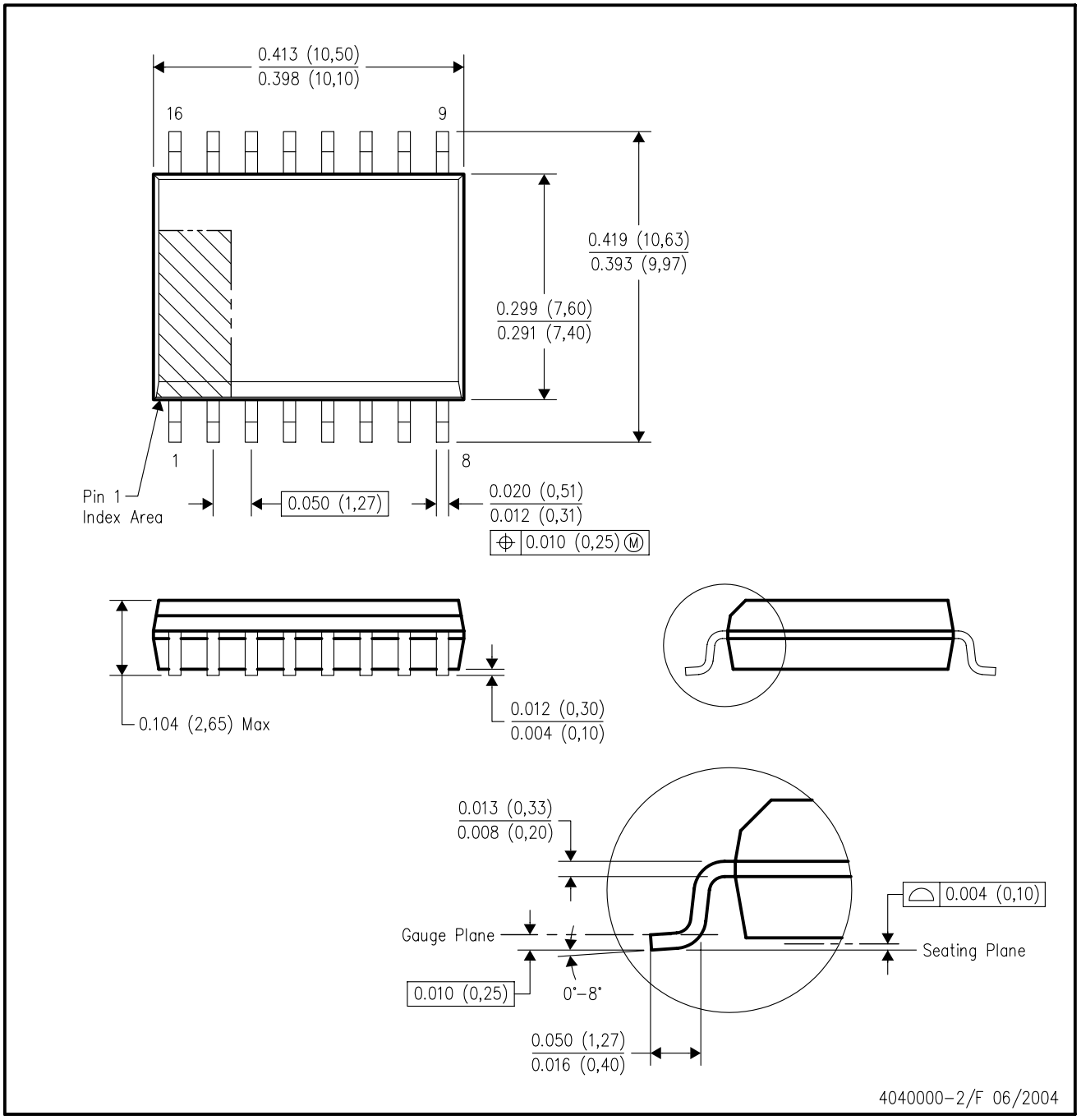
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DW (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE

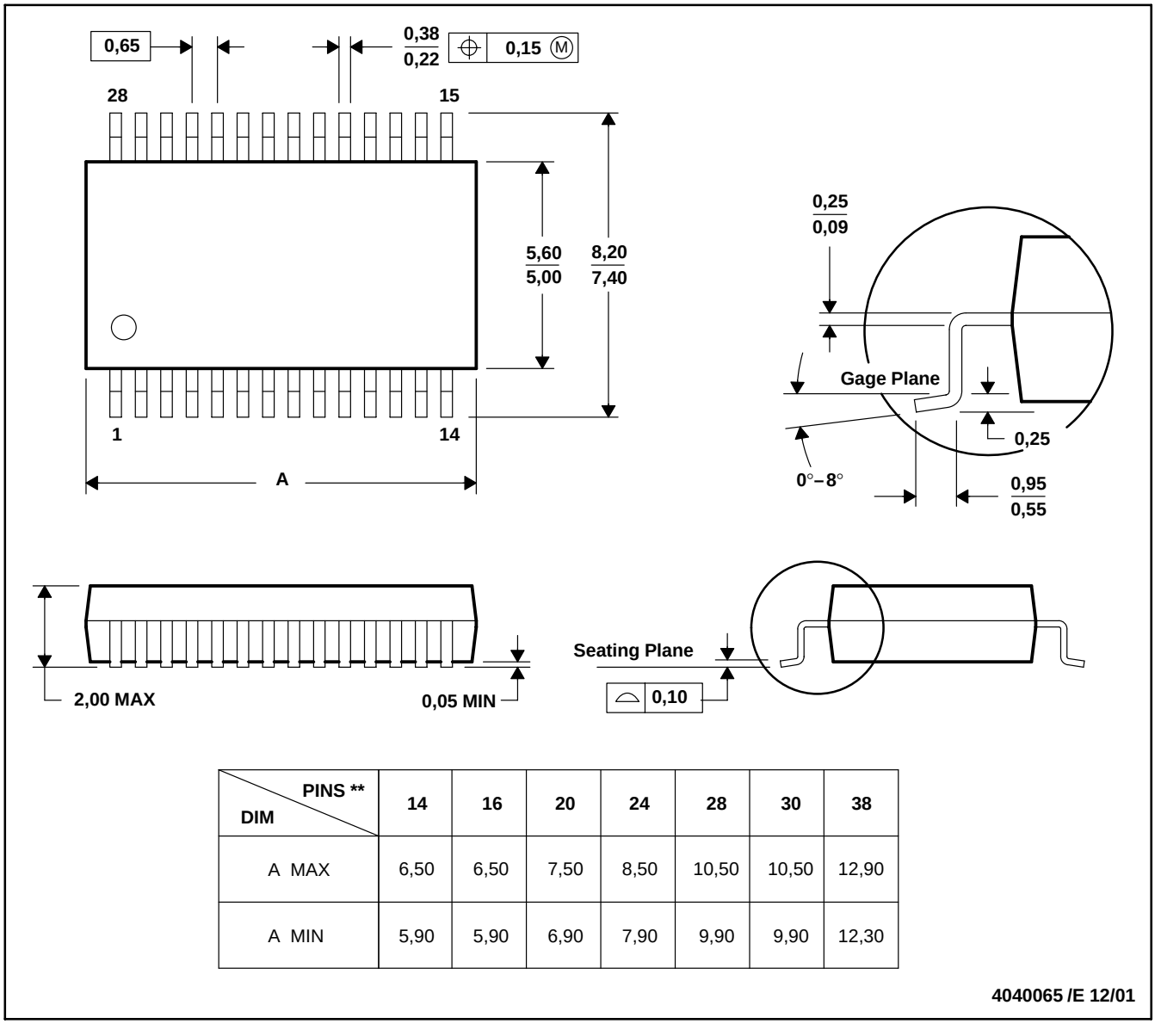


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



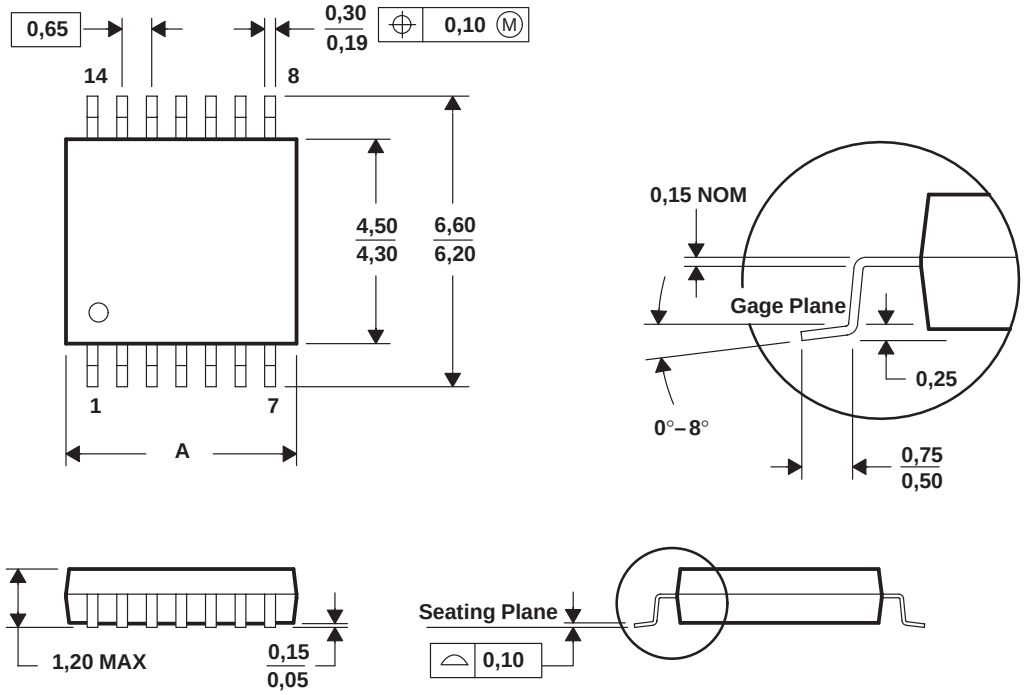
DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

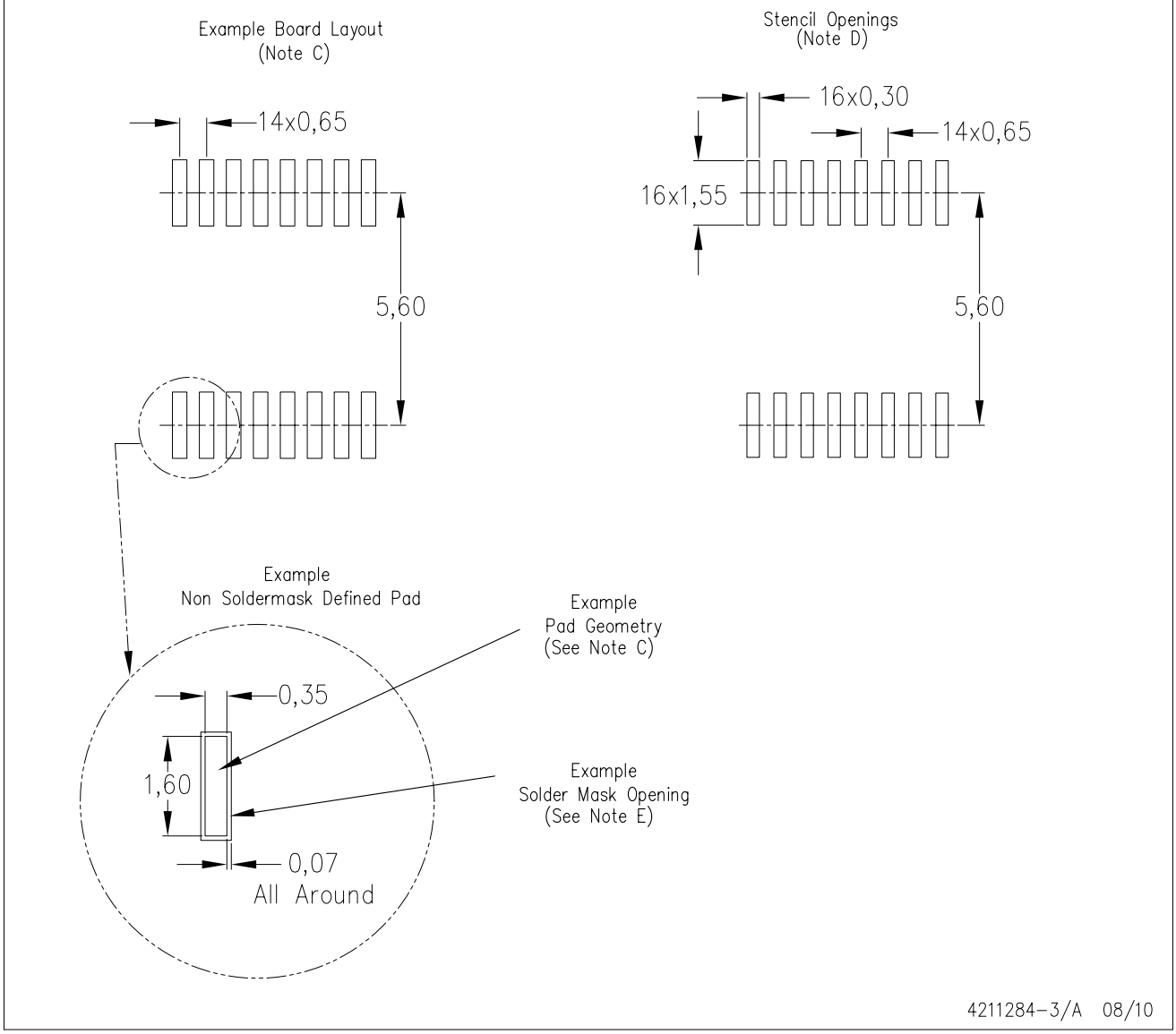


DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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