# 1A Low Dropout Positive Voltage Regulator

## DESCRIPTION

TS1117B are high performance positive voltage regulators are designed for use in applications requiring low dropout performance at full rated current. Additionally, TS1117B provides excellent regulation over variations due to changes in line, load and temperature. Outstanding features include low dropout performance at rated current, fast transient response, internal current limiting, and thermal shutdown protection of the output device. TS1117B are three terminal regulators with fixed and adjustable voltage options available in popular packages.

## FEATURES

- Low dropout performance 1.5V max.
- Fast transient response
- Built-in thermal shutdown
- Output current limit
- Line regulation typical 0.2%
- Load regulation typical 0.05%
- Low-ESR ceramic capacitor (MLCC) required for Stability.
- Good ripple rejection
- RoHS Compliant
- Halogen-free

## APPLICATION

- PC peripheral
- Communication
- Consumer equipment

**TO-252 (DPAK)**



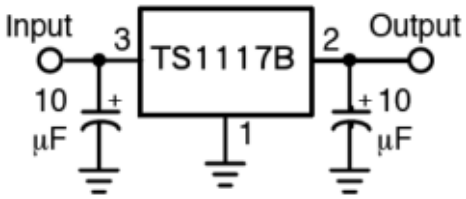
**SOT-223**



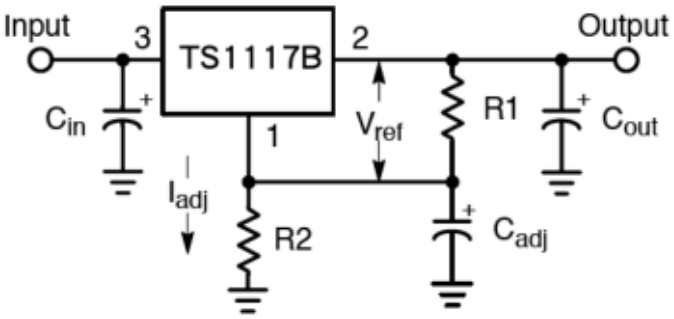
**Pin Definition:**
1. Fixed / Adj
2. Output (Tab)
3. Input

**Notes:** MSL 3 (Moisture Sensitivity Level) per J-STD-020

## TYPICAL APPLICATION CIRCUIT




**Fixed output voltage version**




**Adjustable output voltage version**

| ABSOLUTE MAXIMUM RATINGS | | | | |
|---|---|---|---|---|
| **PARAMETER** | | **SYMBOL** | **LIMIT** | **UNIT** |
| Input Supply Voltage | | $V_{IN}$ | 15 | V |
| Recommend Operation Input Supply Voltage | | $V_{IN\ (Opr.\ Typ.)}$ | 12 | V |
| Power Dissipation (Note 2) | | $P_D$ | Internal limited | |
| Operating Temperature Range | | $T_{OPER}$ | -40 ~ +125 | °C |
| Junction Temperature Range | | $T_J$ | +150 | °C |
| Storage Temperature Range | | $T_{STG}$ | -65 ~ +150 | °C |
| Lead Soldering Temperature (260°C) | TO-252 | | 5 | s |
| | SOT-223 | | | |

| THERMAL PERFORMANCE | | | | |
|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **LIMIT** | | **UNIT** |
| | | **SOT-223** | **TO-252** | |
| Junction to Ambient Thermal Resistance | $R_{\Theta JA}$ | 130 | 105 | °C/W |

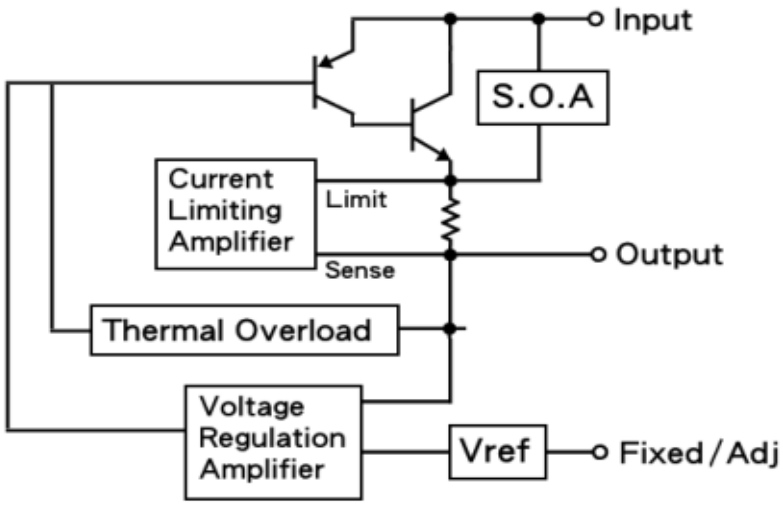
**Notes:** $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB in still air.

| ELECTRICAL SPECIFICATIONS ($T_A$=25°C, unless otherwise noted) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **CONDITIONS** | **SYMBOL** | **MIN** | **TYP** | **MAX** | **UNIT** |
| Reference Voltage | $V_{IN}$ = 2.75, $I_O$=1A | $V_{REF}$ | 1.225 | 1.25 | 1.275 | V |
| Output Voltage (Note 4) | $V_{IN}$ = 2.7V~12V, $I_O$=1A | $V_{OUT}$ | 1.176 | 1.2 | 1.224 | V |
| | $V_{IN}$ = 3V~12V, $I_O$=1A | | 1.470 | 1.5 | 1.530 | |
| | $V_{IN}$ = 4V~12V, $I_O$=1A | | 2.450 | 2.5 | 2.550 | |
| | $V_{IN}$ = 4.8V~12V, $I_O$=1A | | 3.235 | 3.3 | 3.366 | |
| | $V_{IN}$ = 6.5V~12V, $I_O$=1A | | 4.900 | 5.0 | 5.100 | |
| Line Regulation | $V_O$ +1.5V ≤ $V_{IN}$ ≤ 12V, $I_O$ = 10mA | $REG_{LINE}$ | -- | 0.2 | 0.5 | % |
| Load Regulation (Note 1,2) | $V_{IN}$ = $V_{OUT}$+1.5V, $I_O$ = 10mA~1A | $REG_{LOAD}$ | -- | 0.05 | 1.0 | % |
| Dropout Voltage | $I_O$ =1A, $\Delta V_{OUT}$ = 1% $V_{OUT}$ | $V_{DROP}$ | -- | 1.3 | 1.5 | V |
| Quiescent Current | $V_{IN}$ = 5V | $I_Q$ | -- | 5 | 10 | mA |
| Adjustable Pin Current | | $I_{ADJ}$ | -- | 90 | -- | µA |
| Output Current Limit | $V_{IN}$ - $V_{OUT}$ = 1.5V | $I_{LIMIT}$ | 1.1 | -- | -- | A |
| Temperature Stability | $I_O$ =10mA, | | -- | 0.5 | -- | % |
| Ripple Rejection | f= 120Hz, $I_O$= 1A, $C_{OUT}$ =25µF, $V_{IN}$ = $V_{OUT}$+3V | RR | -- | 60 | 70 | dB |

**Note:**

1. See thermal regulation specification for changes in output voltage due to heating effects. Line and load regulation are measured at a constant junction temperature by low duty cycle pulse testing. Load regulation is measured at the output lead = 1/18" from the package.
2. Line and load regulation are guaranteed up to the maximum power dissipation of 15W. Power dissipation is determined by the input / output voltage difference and the output current. Guaranteed maximum power dissipation will not be available over the full input / output voltage range.
3. Quiescent current is defined as the minimum output current required to maintain the regulation.
4. The Output Capacitor does not have a theoretical upper limit and increasing its value will increase stability. $C_{OUT}$=100uF or more is typical for high current regulator design.

## FUNCTION BLOCK




## ORDERING INFORMATION

| OUTPUT VOLTAGE | PART NO. | PACKAGE | PACKING | DEVICE MARKING |
|---|---|---|---|---|
| ADJ | TS1117BCP ROG | TO-252 (DPAK) | 2,500pcs / 13" Reel | TS1117B CP |
| | TS1117BCW RPG | SOT-223 | 2,500pcs / 13" Reel | TS1117B CW |
| 1.2V | TS1117BCW12 RPG | SOT-223 | 2,500pcs / 13" Reel | TS1117B 12 |
| 2.5V | TS1117BCW25 RPG | SOT-223 | 2,500pcs / 13" Reel | TS1117B 25 |
| 3.3V | TS1117BCP33 ROG | TO-252 (DPAK) | 2,500pcs / 13" Reel | TS1117B 33 |
| | TS1117BCW33 RPG | SOT-223 | 2,500pcs / 13" Reel | TS1117B 33 |
| 5.0V | TS1117BCP50 ROG | TO-252 (DPAK) | 2,500pcs / 13" Reel | TS1117B 50 |
| | TS1117BCW50 RPG | SOT-223 | 2,500pcs / 13" Reel | TS1117B 50 |

## CHARACTERISTICS CURVES

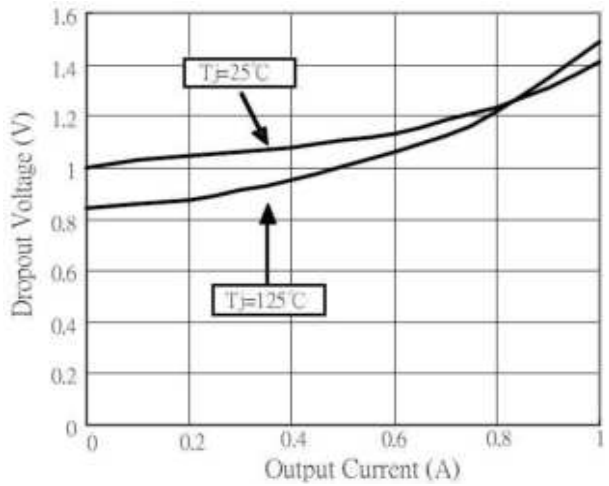



**Figure 1. $V_{DROP}$ vs. Output Current**

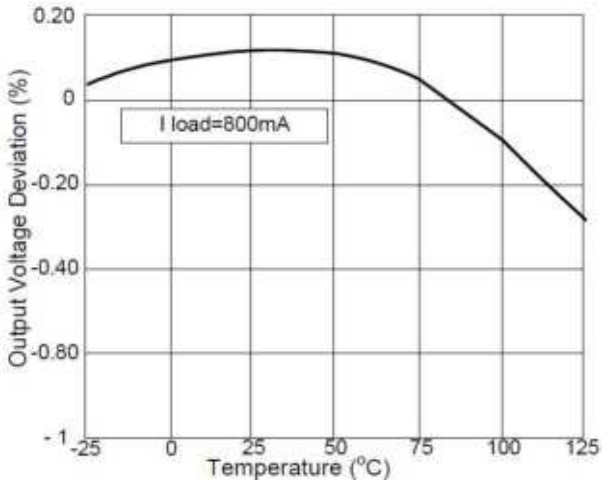



**Figure 2. Load Regulation vs. Temperature**

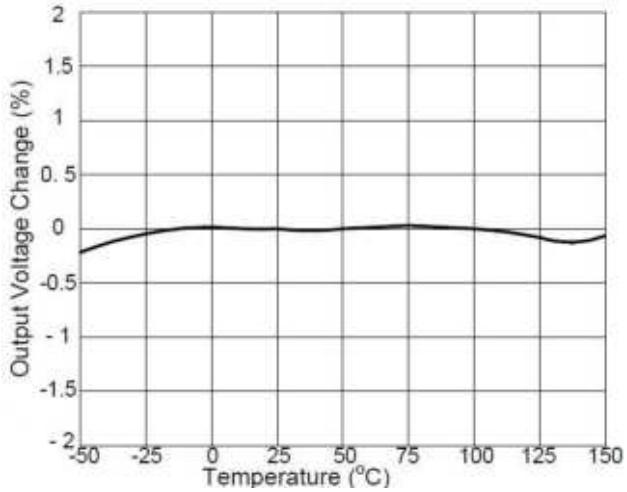



**Figure 3. $V_{OUT}$ Change vs. Temperature**

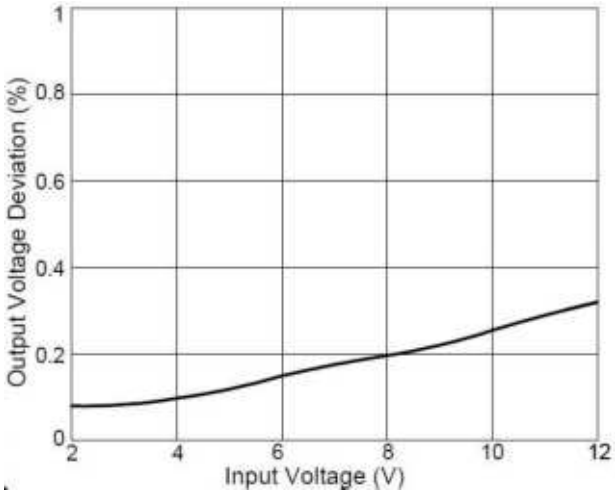



**Figure 4. $V_{OUT}$ Deviation vs. Temperature**

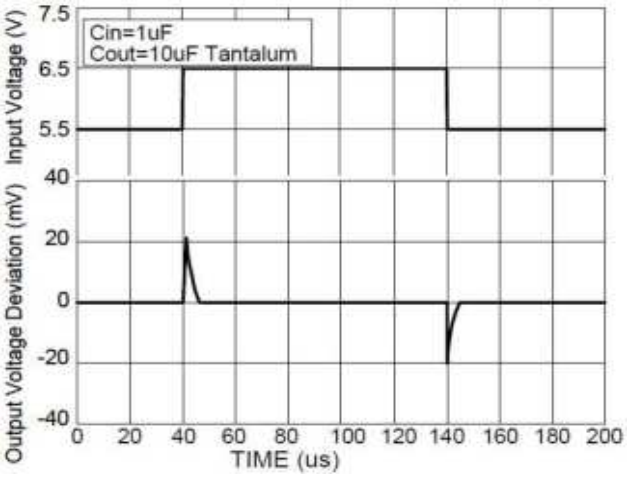



**Figure 5. Line Transient Response**

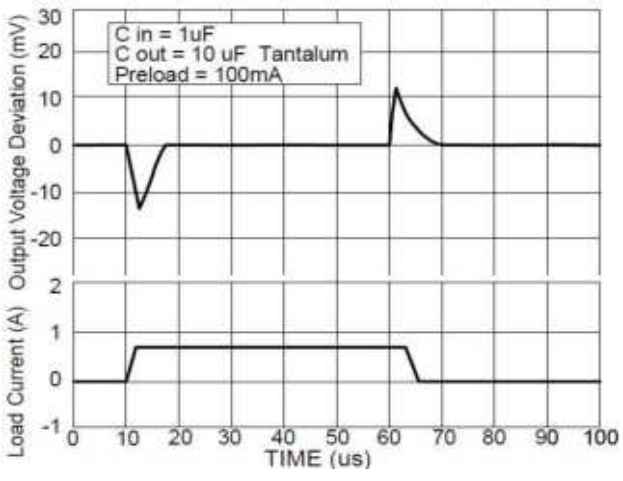
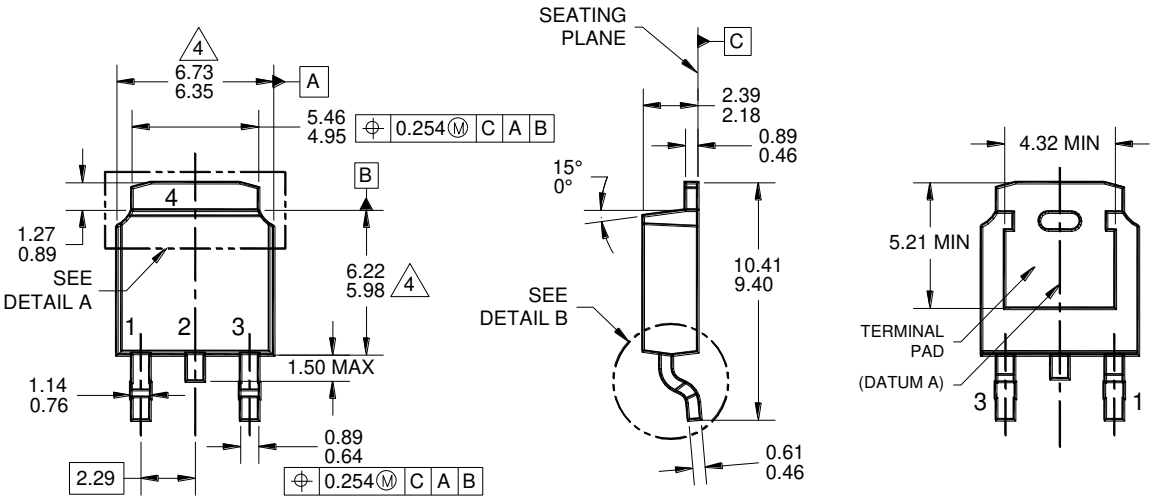
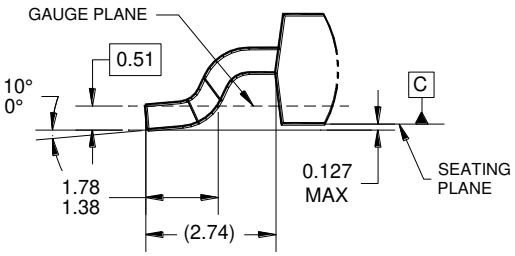



**Figure 6. Load Transient Response**

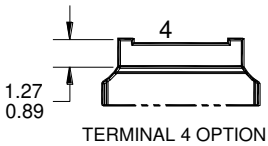
## PACKAGE OUTLINE DIMENSIONS

**TO-252**

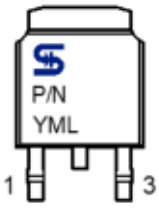


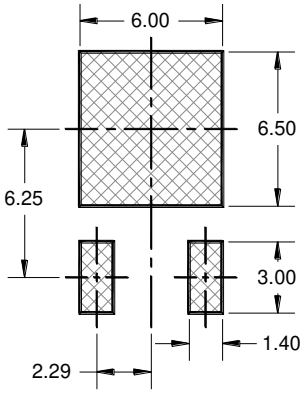

DETAIL B, ROTATED -90°
(SCALE 2:1)




TERMINAL 4 OPTION
DETAIL A




MARKING DIAGRAM




SUGGESTED PAD
LAYOUT

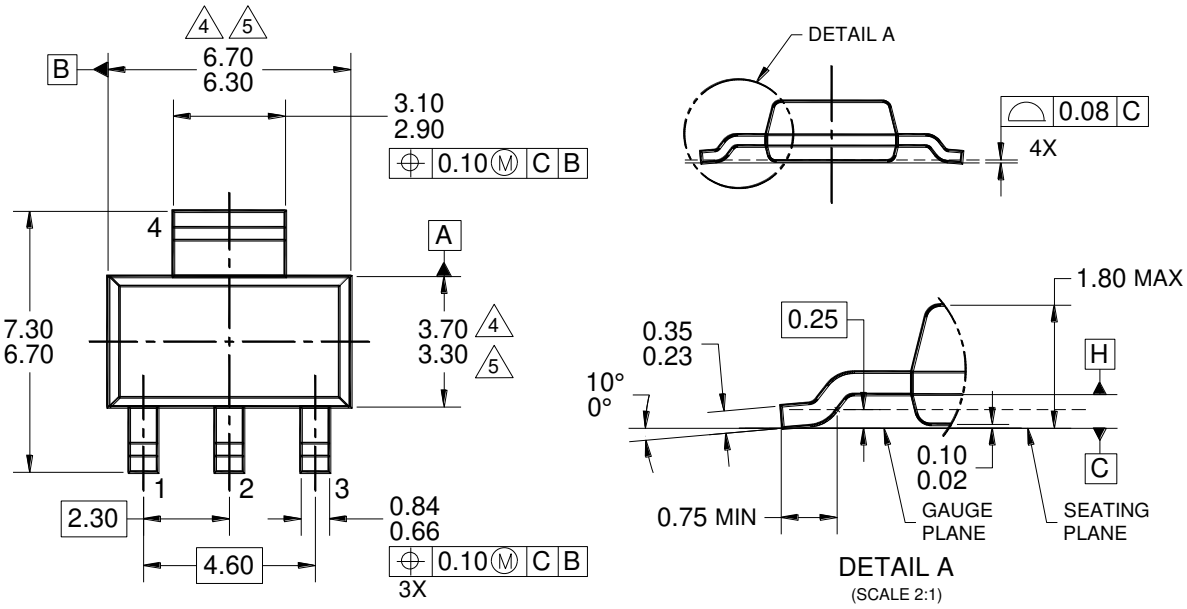
P/N = MARKING CODE
Y = YEAR CODE
M = MONTH CODE
O =JAN P =FEB Q =MAR R =APR
S =MAY T =JUN U =JUL V=AUG
W =SEP X =OCT Y =NOV Z =DEV
L = LOT CODE

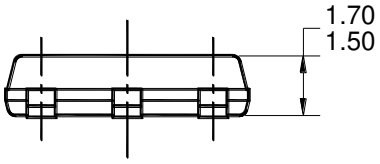
NOTES: UNLESS OTHERWISE SPECIFIED

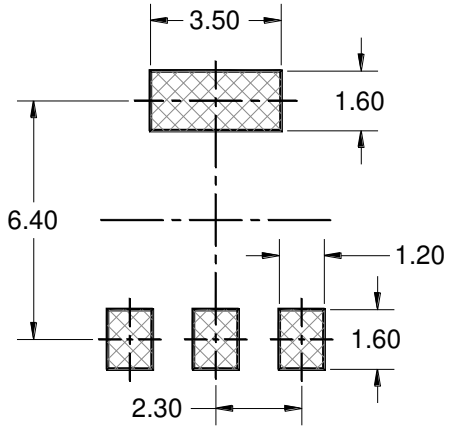
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: JEDEC TO-252, VARIATION AA, ISSUE F.
4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURRS.
5. DWG NO. REF: HQ2SD07-TO252AA-013 REV B.

## PACKAGE OUTLINE DIMENSIONS

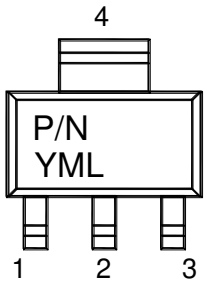
**SOT-223**




SUGGESTED PAD LAYOUT




MARKING DIAGRAM

P/N = MARKING CODE
Y = YEAR CODE
M = MONTH CODE
O =JAN P =FEB Q =MAR R =APR
S =MAY T =JUN U =JUL V=AUG
W =SEP X =OCT Y =NOV Z =DEV
L = LOT CODE

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE:TO-261, VARIATION AA.
4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH.
5. MOLDED PLASTIC BODY LATERAL DIMENSIONS TO BE DETERMINED AT DATUM PLANE H.
6. DWG NO. REF: HQ2SD07-SOT223-001 REV A

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