IEEE 1394a THREE-PORT CABLE TRANSCEIVER/ARBITER

FEATURES

- **Fully Supports Provisions of IEEE 1394-1995 Standard for High Performance Serial Bus[1] and the P1394a Supplement**
- **Fully Interoperable With FireWire™ and i.LINK™ Implementation of IEEE Std 1394**
- **Fully Compliant With OpenHCI Requirements**
- **Provides Three P1394a Fully Compliant Cable Ports at 100/200/400 Megabits per Second (Mbits/s)**
- **Full P1394a Support Includes: Connection Debounce, Arbitrated Short Reset, Multispeed Concatenation, Arbitration Acceleration, Fly-By Concatenation, Port Disable/Suspend/Resume**
- **Extended Resume Signaling for Compatibility With Legacy DV Devices**
- **Power-Down Features to Conserve Energy in Battery Powered Applications Include: Automatic Device Power-Down During Suspend, Device Power-Down Terminal, Link Interface Disable via LPS, and Inactive Ports Powered Down**
- **Ultralow-Power Sleep Mode**
- **Node Power Class Information Signaling for System Power Management**
- **Cable Power Presence Monitoring**
- **Cable Ports Monitor Line Conditions for Active Connection to Remote Node**
- **Register Bits Give Software Control of Contender Bit, Power Class bits, Link Active Control Bit and P1394a Features**
- **Data Interface to Link-Layer Controller Through 2/4/8 Parallel Lines at 49.152 MHz**
- **Interface to Link Layer Controller Supports Low Cost TI Bus-Holder Isolation and Optional Annex J Electrical Isolation**
- **Interoperable With Link-Layer Controllers Using 3.3-V and 5-V Supplies**
- **Interoperable With Other Physical Layers (PHYs) Using 3.3-V and 5-V Supplies**
- **Low Cost 24.576-MHz Crystal Provides Transmit, Receive Data at 100/200/400 Mbits/s, and Link-Layer Controller Clock at 49.152 MHz**
- **Incoming Data Resynchronized to Local Clock**
- **Logic Performs System Initialization and Arbitration Functions**
- **Encode and Decode Functions Included for Data–Strobe Bit Level Encoding**
- **Separate Cable Bias (TPBIAS) for Each Port**
- **Single 3.3-V Supply Operation**
- **Low Cost High Performance 80-Pin TQFP (PFP) Thermally Enhanced Package**
- **Direct Drop-In Upgrade for TSB41LV03PFP**

NOTE: Implements technology covered by one or more patents of Apple Computer, Incorporated and SGS Thompson, Limited.

DESCRIPTION

The TSB41LV03A provides the digital and analog transceiver functions needed to implement a three-port node in a cable-based IEEE 1394 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. The TSB41LV03A is designed to interface with a line layer controller (LLC), such as the TSB12LV21, TSB12LV22, TSB12LV23, TSB12LV31, TSB12LV41, TSB12LV42, or TSB12LV01A.

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The TSB41LV03A requires only an external 24.576 MHz crystal as a reference. An external clock may be provided instead of a crystal. An internal oscillator drives an internal phase-locked loop (PLL), which generates the required 393.216 MHz reference signal. This reference signal is internally divided to provide the clock signals used to control transmission of the outbound encoded strobe and data information. A 49.152 MHz clock signal is supplied to the associated LLC for synchronization of the two chips and is used for resynchronization of the received data. The power-down (PD) function, when enabled by asserting the PD terminal high, stops operation of the PLL.

The TSB41LV03A supports an optional isolation barrier between itself and its LLC. When the $\overline{\text{ISO}}$ input terminal is tied high, the LLC interface outputs behave normally. When the $\overline{\text{ISO}}$ terminal is tied low, internal differentiating logic is enabled, and the outputs are driven such that they can be coupled through a capacitive or transformer galvanic isolation barrier as described in Annex J of IEEE Std 1394-1995 and in the P1394a Supplement section 5.9.4) (hereafter referred to as Annex J type isolation). To operate with TI bus holder isolation, the $\overline{\text{ISO}}$ terminal on the PHY must be high.

Data bits to be transmitted through the cable ports are received from the LLC on two, four, or eight parallel paths (depending on the requested transmission speed). They are latched internally in the TSB41LV03A in synchronization with the 49.152-MHz system clock. These bits are combined serially, encoded, and transmitted at 98.304, 196.608, or 392.216 Mbits/s (referred to as S100, S200, and S400 speed respectively) as the outbound data-strobe information stream. During transmission, the encoded data information is transmitted differentially on the TPB cable pair(s), and the encoded strobe information is transmitted differentially on the TPA cable pair(s).

During packet reception the TPA and TPB transmitters of the receiving cable port are disabled, and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair, and the encoded strobe information is received on the TPB cable pair. The received data-strobe information is decoded to recover the receive clock signal and the serial data bits. The serial data bits are split into two-, four-, or eight-bit parallel streams (depending upon the indicated receive speed), resynchronized to the local 49.152-MHz system clock and sent to the associated LLC. The received data is also transmitted (repeated) on the other active (connected) cable ports.

Both the TPA and TPB cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration. The outputs of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage. The value of this common-mode voltage is used during arbitration to set the speed of the next packet transmission. In addition, the TPB channel monitors the incoming cable common-mode voltage on the TPB pair for the presence of the remotely supplied twisted-pair bias voltage.

The TSB41LV03A provides a 1.86-V nominal bias voltage at the TPBIAS terminal for port termination. The PHY contains three independent TPBIAS circuits. This bias voltage, when seen through a cable by a remote receiver, indicates the presence of an active connection. This bias voltage source must be stabilized by an external filter capacitor of 1 μF.

The line drivers in the TSB41LV03A, operating in a high-impedance current mode, are designed to work with external 112-Ω line-termination resistor networks in order to match the 110-Ω cable impedance. One network is provided at each end of a twisted-pair cable. Each network is composed of a pair of series-connected 56-Ω resistors. The midpoint of the pair of resistors that is directly connected to the twisted-pair A terminals is connected to its corresponding TPBIAS voltage terminal. The midpoint of the pair of resistors that is directly connected to the twisted-pair B terminals is coupled to ground through a parallel R-C network with recommended values of 5 kΩ and 220 pF. The values of the external line-termination resistors are designed to meet the standard specifications when connected in parallel with the internal receiver circuits. An external resistor connected between the R0 and R1 terminals sets the driver output current, along with other internal operating currents. This current setting resistor has a value of 6.3 kΩ± 1%. This may be accomplished by placing a 6.34-kΩ± 1% resistor in parallel with a 1-MΩ resistor.

When the power supply of the TSB41LV03A is off while the twisted-pair cables are connected, the TSB41LV03A transmitter and receiver circuitry presents a high-impedance signal to the cable and does not load the TPBIAS voltage at the other end of the cable.

When the TSB41LV03A is used with one or more of the ports not brought out to a connector, the twisted-pair terminals of the unused ports must be terminated for reliable operation. For each unused port, the TPB+ and TPB– terminals can be tied together and then pulled to ground, or the TPB+ and TPB– terminals can be connected to the suggested termination network. The TPA+ and TPA– and TPBIAS terminals of an unused port can be left unconnected. The TPBias terminal can be connected to a 1-μF capacitor to ground or left floating.

The TESTM, SE, and SM terminals are used to set up various manufacturing test conditions. For normal operation, the TESTM terminal should be connected to V_{DD}, SE should be tied to ground through a 1-kΩ resistor, while SM should be connected directly to ground.

Four package terminals are used as inputs to set the default value for four configuration status bits in the self-ID packet, are hardwired high or low as a function of the equipment design. The PC0–PC2 terminals are used to indicate the default power-class status for the node (the need for power from the cable or the ability to supply power to the cable). The C/LKON terminal is used as an input to indicate that the node is a contender for either isochronous resource manager (IRM) or for bus manager (BM).

The TSB41LV03A supports suspend/resume as defined in the IEEE P1394a specification. The suspend mechanism allows pairs of directly-connected ports to be placed into a low-power conservation state suspended state) while maintaining a port-to-port connection between 1394 bus segments. While in the suspended state, a port is unable to transmit or receive data transaction packets. However, a port in the suspended state is capable of detecting connection status changes and detecting incoming TPBias. When all three ports of the TSB41LV03A are suspended, all circuits except the bandgap reference generator and bias detection circuits are powered down, resulting in significant power savings. For additional details of suspend/resume operation refer to the P1394a specification. The use of suspend/resume is recommended for new designs.

The port transmitter and receiver circuitry is disabled during power down (when the PD input terminal is asserted high), during reset (when the $\overline{\text{RESET}}$ input terminal is asserted low), when no active cable is connected to the port, or when controlled by the internal arbitration logic. The TPBias output is disabled during power-down, during reset, or when the port is disabled as commanded by the LLC.

The CNA (cable-not-active) terminal provides a high when there are no twisted-pair cable ports receiving incoming bias (i.e., they are either disconnected or suspended), and can be used along with LPS to determine when to power down the TSB41LV03A. The CNA output is not debounced. When the PD terminal is asserted high, the CNA detection circuitry is enabled (regardless of the previous state of the ports) and a pulldown is activated on the $\overline{\text{RESET}}$ terminal so as to force a reset of the TSB41LV03A internal logic.

The LPS (link power status) terminal works with the C/LKON terminal to manage the power usage in the node. The LPS signal from the LLC is used in conjunction with the LCtrl bit to indicate the active/power status of the LLC. The LPS signal is also used to reset, disable, and initialize the PHY-LLC interface (the state of the PHY-LCC interface is controlled solely by the LPS input, regardless of the state of the LCtrl bit).

The LPS input is considered inactive if it remains low for more than 2.6 μs and is considered active otherwise. When the TSB41LV03A detects that LPS is inactive, it places the PHY-LLC interface into a low–power reset state in which the CTL and D outputs are held in the logic zero state and the LREQ input is ignored; however, the SYSCLK output remains active. If the LPS input remains low for more than 26 μs, the PHY-LLC interface is put into a low-power disabled state in which the SYSCLK output is also held inactive. The PHY-LLC interface is also held in the disabled state during hardware reset. The TSB41LV03A continues the necessary repeater functions required for normal network operation regardless of the state of the PHY-LLC interface. When the interface is in the reset or disabled state and LPS is again observed active, the PHY initializes the interface and returns it to normal operation.

When the PHY-LLC interface in the low-power disabled state, the TSB41LV03A automatically enters a low-power mode if all ports are inactive (disconnected, disabled, or suspended). In this low-power mode, the TSB41LV03A disables its internal clock generators and also disables various voltage and current reference circuits depending on the state of the ports (some reference circuitry must remain active in order to detect new cable connections, disconnections, or incoming TPBias, for example). The lowest power consumption (the *ultralow-power sleep mode*) is attained when all ports are either disconnected, or disabled with the port's interrupt enable bit cleared. The TSB41LV03A exits the low-power mode when the LPS input is asserted high or when a port event occurs which requires that the TSB41LV03A become active in order to respond to the event or to notify the LLC of the event (e.g., incoming bias is detected on a suspended port, a disconnection is detected on a suspended port, a new connection is detected on a nondisabled port, etc.). The SYSCLK output becomes active (and the PHY-LLC interface is initialized and becomes operative) within 7.3 ms after LPS is asserted high when the TSB41LV03A is in the low-power mode.

The PHY uses the C/LKON terminal to notify the LLC to power up and become active. When activated, the C/LKON signal is a square wave of approximately 163 ns period. The PHY activates the C/LKON output when the LLC is inactive and a wake-up event occurs. The LLC is considered inactive when either the LPS input is inactive, as described above, or the LCtrl bit is cleared to 0. A wake-up event occurs when a link-on PHY packet addressed to this node is received, or conditionally when a PHY interrupt occurs. The PHY deasserts the C/LKON output when the LLC becomes active (both LPS active and the LCtrl bit set to 1). The PHY also deasserts the C/LKON output when a bus-reset occurs unless a PHY interrupt condition exists which would otherwise cause C/LKON to be active.

NOTE:

This product is for high-volume applications only. For a complete datasheet or more information contact support@ti.com.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSB41LV03APFP	LIFEBUY	HTQFP	PFP	80	96	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	TSB41LV03A	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

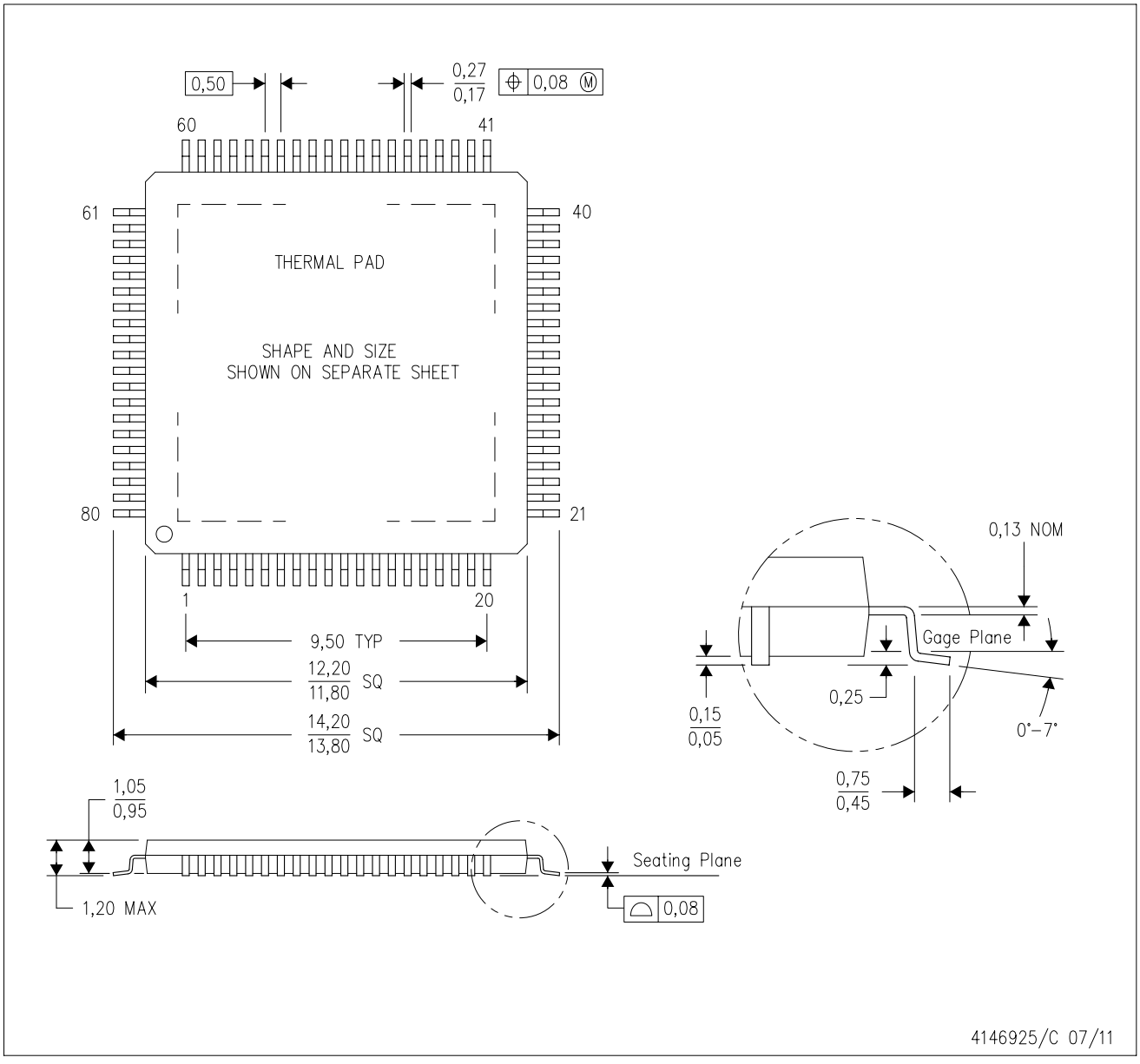
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

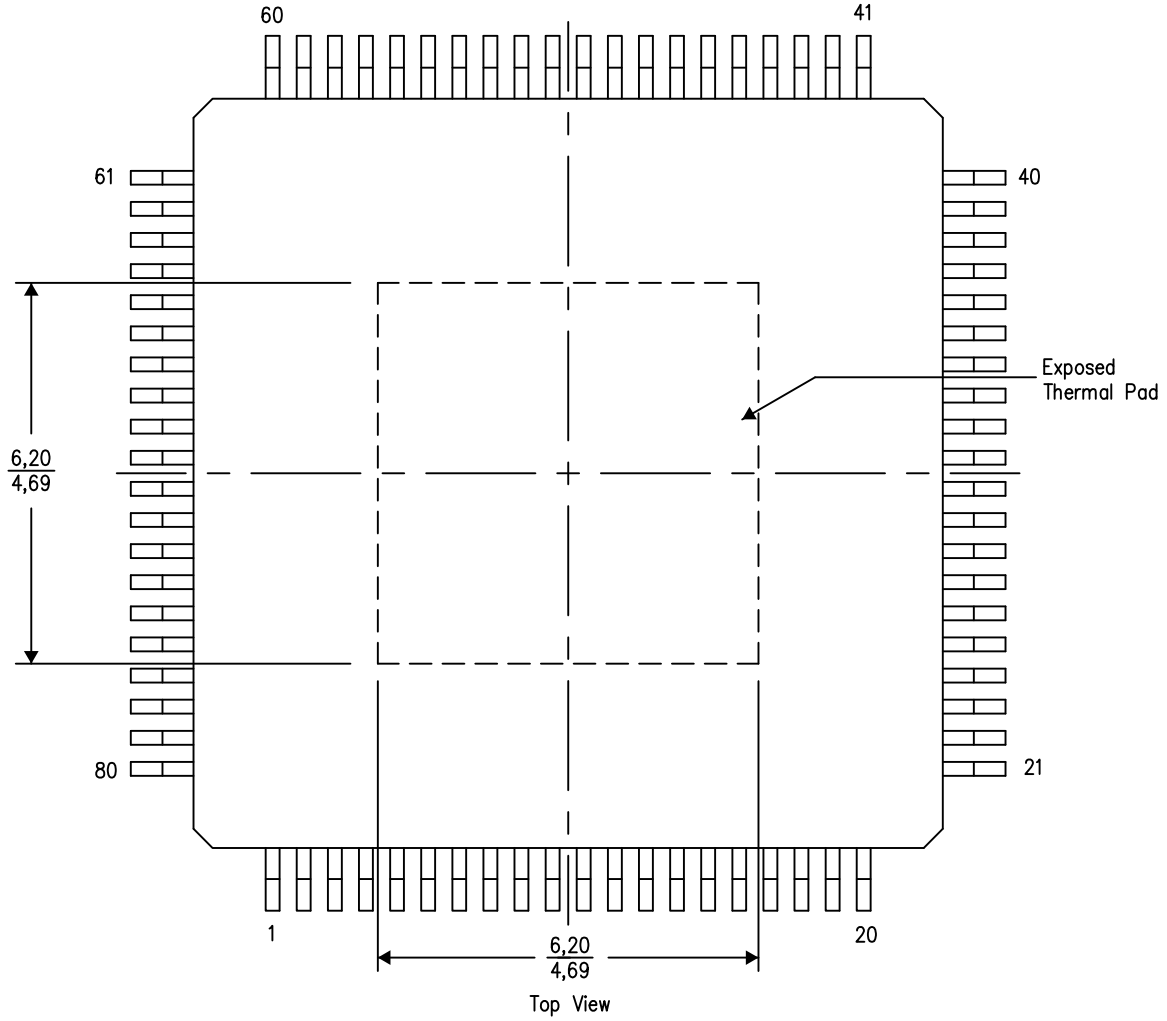
PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



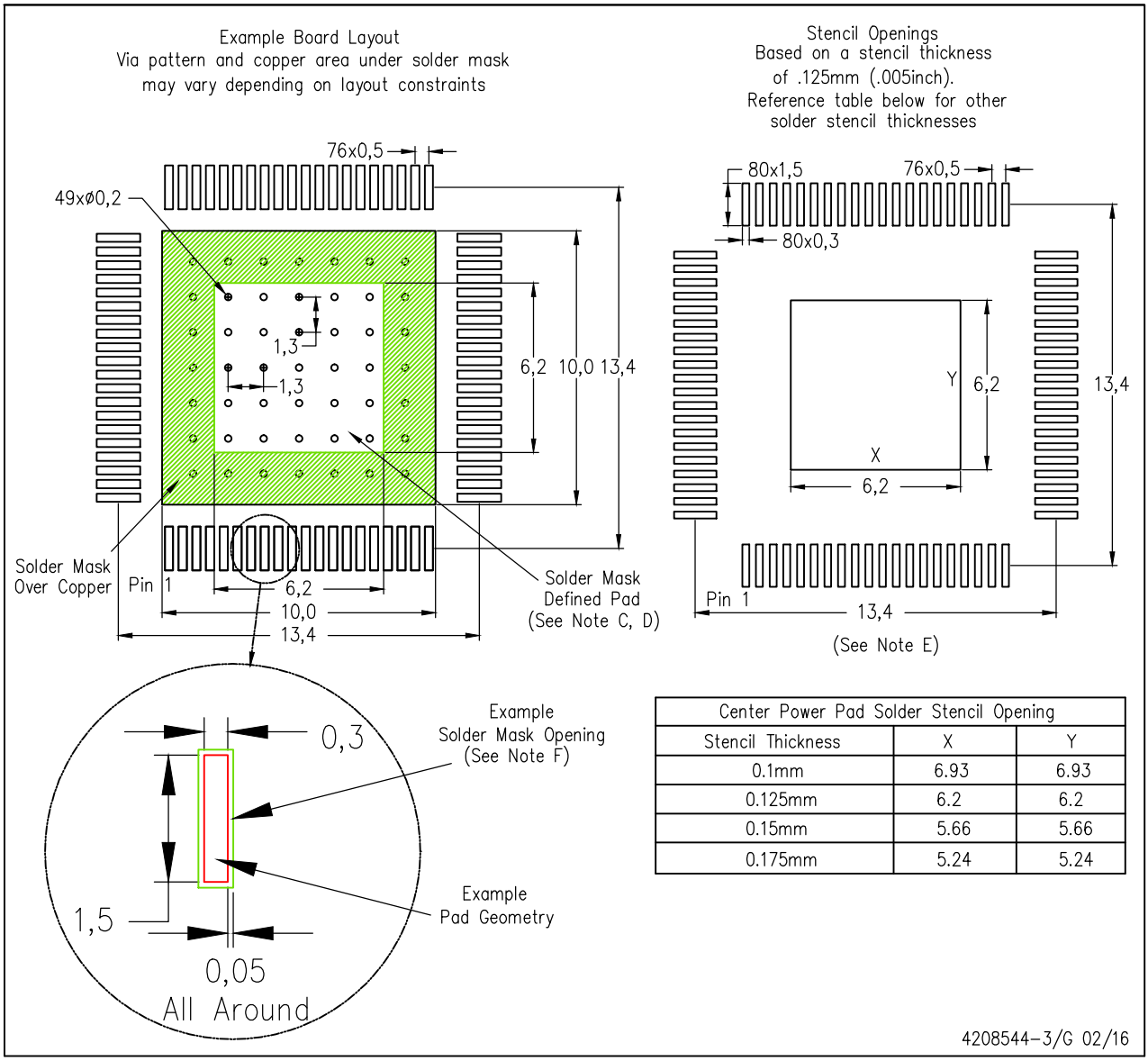
Exposed Thermal Pad Dimensions

4206327–3/P 05/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.93	6.93
0.125mm	6.2	6.2
0.15mm	5.66	5.66
0.175mm	5.24	5.24

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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