Analog Matrix TOUCH SCREEN CONTROLLER with I²C™ Serial Interface for 3 × 5 Array

Check for Samples: TSC2020

FEATURES

- **Supports up to 3.5-Inch Analog Matrix Sensor with 3 × 5 Multiple Touch Resolution and 12-Bit Global Resolution**
- **Supports Both Finger and Stylus**
- **Ratiometric Conversion**
- **Single 1.6V to 3.6V Supply**
- **Preprocessing to Reduce Bus Activity**
- **I²C Interface Supports Standard, Fast, and High-Speed Modes**
- **Internal Detection of Screen Touch**
- **Register-Based, Programmable:**
  - **Sampling Rates, System Timing, Zoning, Normal/Fast Scan Mode**
- **On-Chip Temperature Measurement**
- **Auto Power-Down Control**
- **Low Power:**
  - **70.72µW at 1.6V, at 8.2kSPS Eq Rate, ST**
  - **87.5µW at 1.8V, at 8.2kSPS Eq Rate, ST**
  - **675µW at 1.8V, at 250SSPS Worst-Case, MT (average 300µW at 1.8V, 50SSPS, 3T)**
- **Enhanced ESD Protection to Assist IEC Testing:**
  - **±12kV Air**
  - **±11kV Contact**
- **Packages: 5 × 5 QFN-32, 2.5 × 2.5 WCSP(1)**

(1) WCSP (YZK) package available Q2, 2011.

U.S. Patent Nos. 6,246,394; 7,812,830; other patents pending.

APPLICATIONS

- **Smart Phones, Feature Phones**
- **MIDs, Netbooks, and eBooks**
- **Digital Picture Frames**
- **Portable Instruments**
- **MP3 Players, GPSs, PNDs, and PMPs**

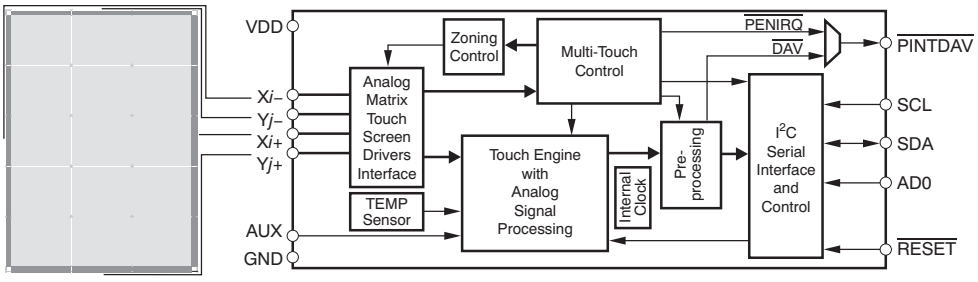
DESCRIPTION

The TSC2020 is a very low power, resistive touch screen controller designed to work with power-sensitive, handheld applications that are based on advanced low-voltage processors. This device works with a supply voltage as low as 1.6V that can be supplied by a single-cell battery. The TSC2020 contains a complete, ultra-low power, 12-bit, analog-to-digital converter (ADC) including sensor drivers and the control logic to measure touch pressure. Unlike other resistive touch screen controllers, the TSC2020 is capable of detecting at least three touches simultaneously and delivers a very low power standby touch detection scheme. This flexibility allows for many new applications that require multiple touches but must remain at low power.

The TSC2020 supports the I²C serial bus and data transmission protocol for all three defined modes: standard, fast, and high-speed. The TSC2020 offers programmable resolution, single-/multi-touch modes to accommodate different screen types, sizes, and application needs.

The TSC2020 is available in a 32-pin 5 × 5 QFN package, and is characterized for the –40°C to +85°C industrial temperature range.

Functional Block Diagram



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	TYPICAL INTEGRAL LINEARITY (LSB)	TYPICAL GAIN ERROR (LSB)	NO MISSING CODES RESOLUTION (BITS)	PACKAGE TYPE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TSC2020I	±0.5	+0.1	11	32-Pin, 0.75 × 5 x 5 Thin QFN	RTV	–40°C to +85°C	TSC2020I	TSC2020IRTVT	Small Tape and Reel, 250
								TSC2020IRTVR	Tape and Reel, 3000
				25-Pin 2.5 × 2.5 WCSP 5 × 5 Matrix	YZK(2)	–40°C to +85°C	TSC2020I	TSC2020IYZKT	Small Tape and Reel, 250
								TSC2020IYZKR	Tape and Reel, 3000

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or visit the device product folder at www.ti.com.
(2) WCSP (YZK) package available Q2, 2011.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		TSC2020	UNIT
Voltage range	Analog inputs X*i*+, X*i*–, Y*j*+, Y*j*–, AUX to GND	–0.4 to V_{DD} + 0.1	V
	V_{DD} to GND	–0.3 to 5	V
Digital pin voltages to GND		–0.3 to 5	V
Operating free-air temperature range, T_A		–40 to +85	°C
Storage temperature range, T_{STG}		–65 to +150	°C
Junction temperature, T_J Max		+150	°C
IEC contact discharge(2)	X*i*+, X*i*–, Y*j*+, Y*j*–	±11	kV
IEC air discharge(2)	X*i*+, X*i*–, Y*j*+, Y*j*–	±12	kV

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.
(2) Test method based on IEC standard 61000-4-2. Contact Texas Instruments for test details.

THERMAL INFORMATION

THERMAL METRIC(1)		TSC2020		UNITS
		RTV	YZK	
		32 PINS	25 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	32.1	99.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	15.4	5.5	
θ_{JB}	Junction-to-board thermal resistance	5.8	35	
ψ_{JT}	Junction-to-top characterization parameter	0.2	13.0	
ψ_{JB}	Junction-to-board characterization parameter	5.7	37.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.2	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TSC2020IRTVR	ACTIVE	WQFN	RTV	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TSC2020IRTVT	ACTIVE	WQFN	RTV	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

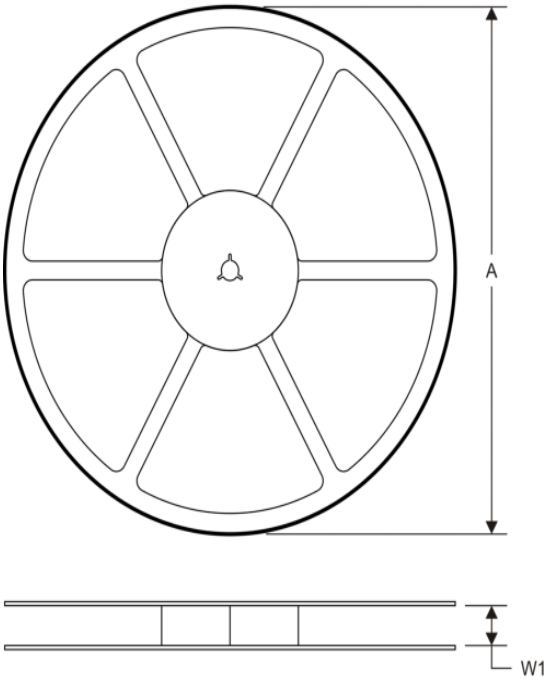
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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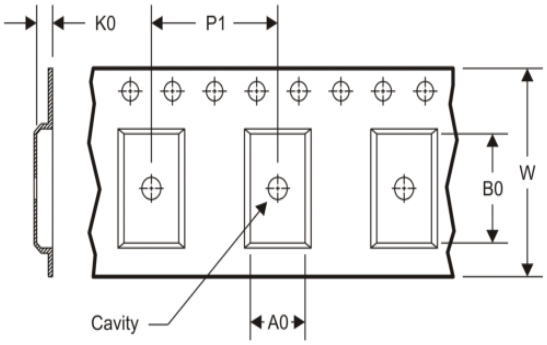
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



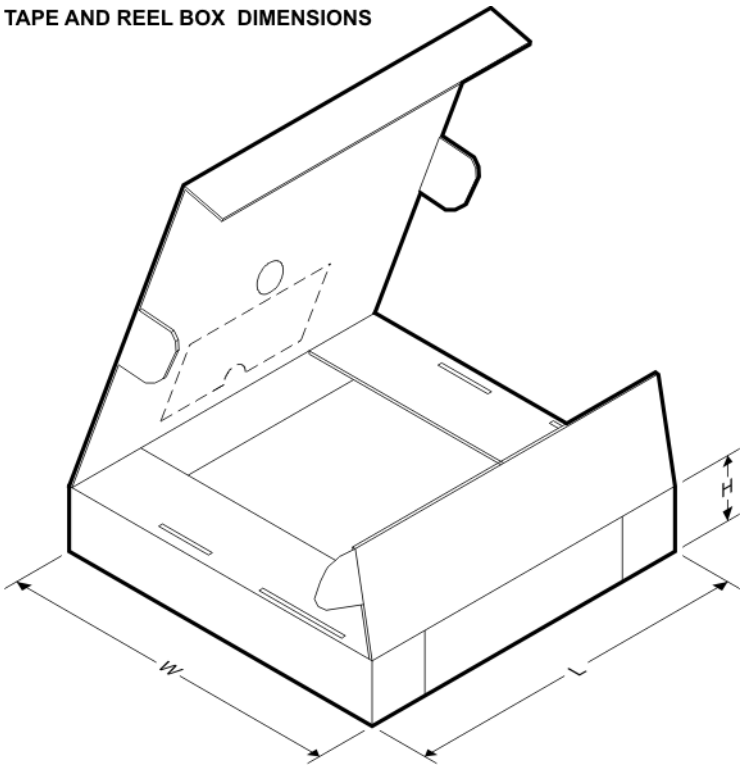
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSC2020IRTVR	WQFN	RTV	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TSC2020IRTVT	WQFN	RTV	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

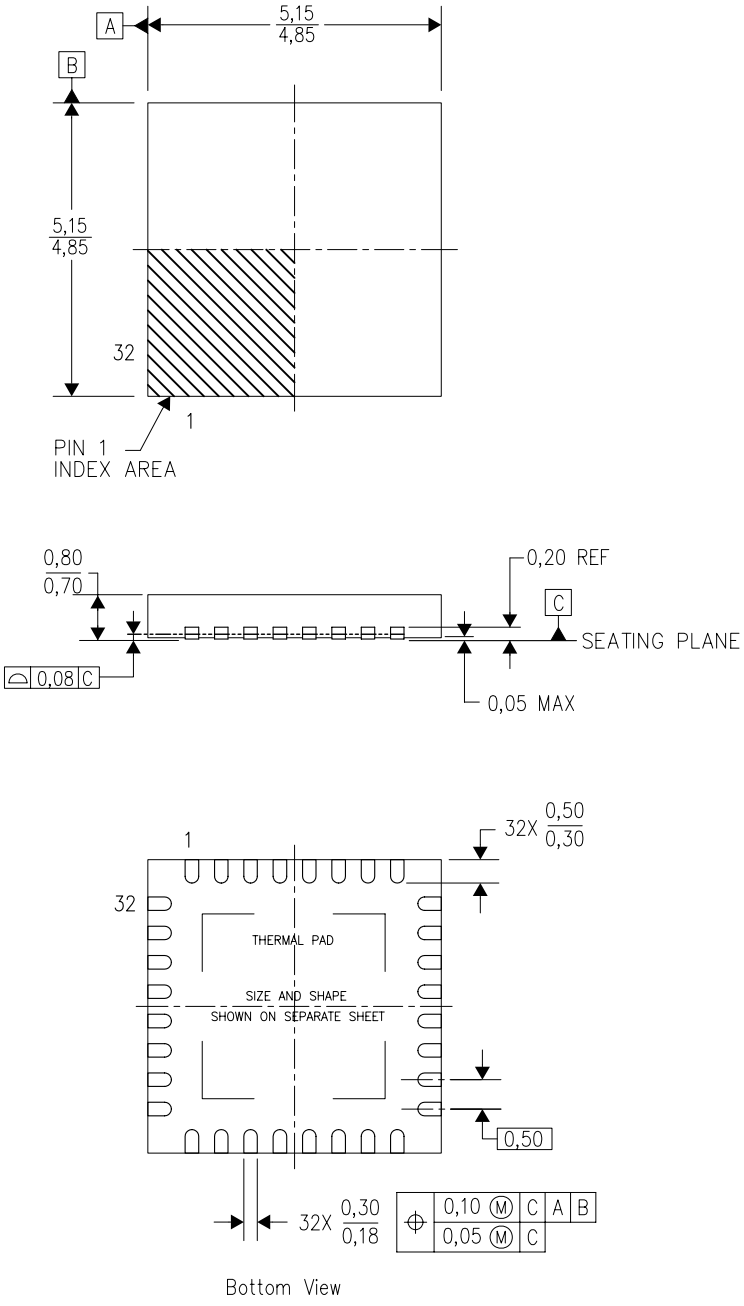
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSC2020IRTVR	WQFN	RTV	32	3000	367.0	367.0	35.0
TSC2020IRTVT	WQFN	RTV	32	250	210.0	185.0	35.0

RTV (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



4206245/C 10/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

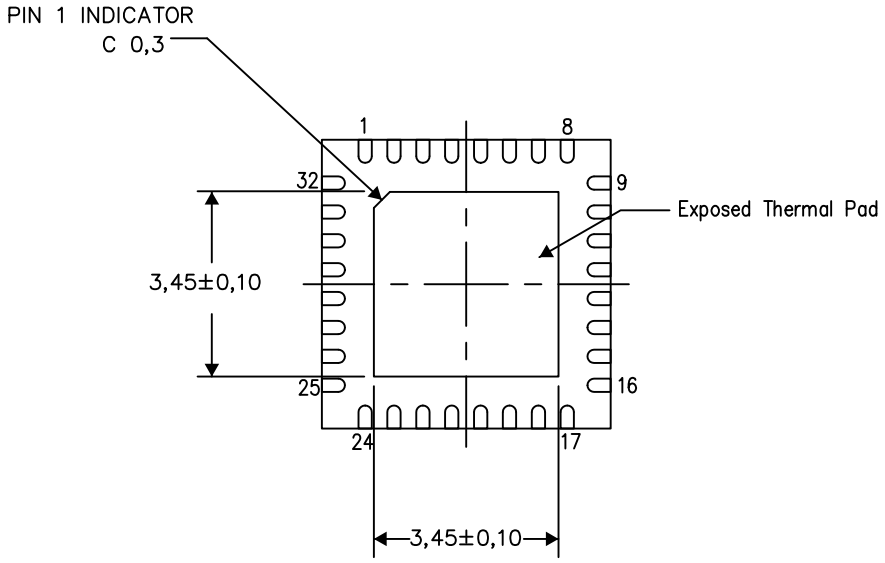
RTV (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



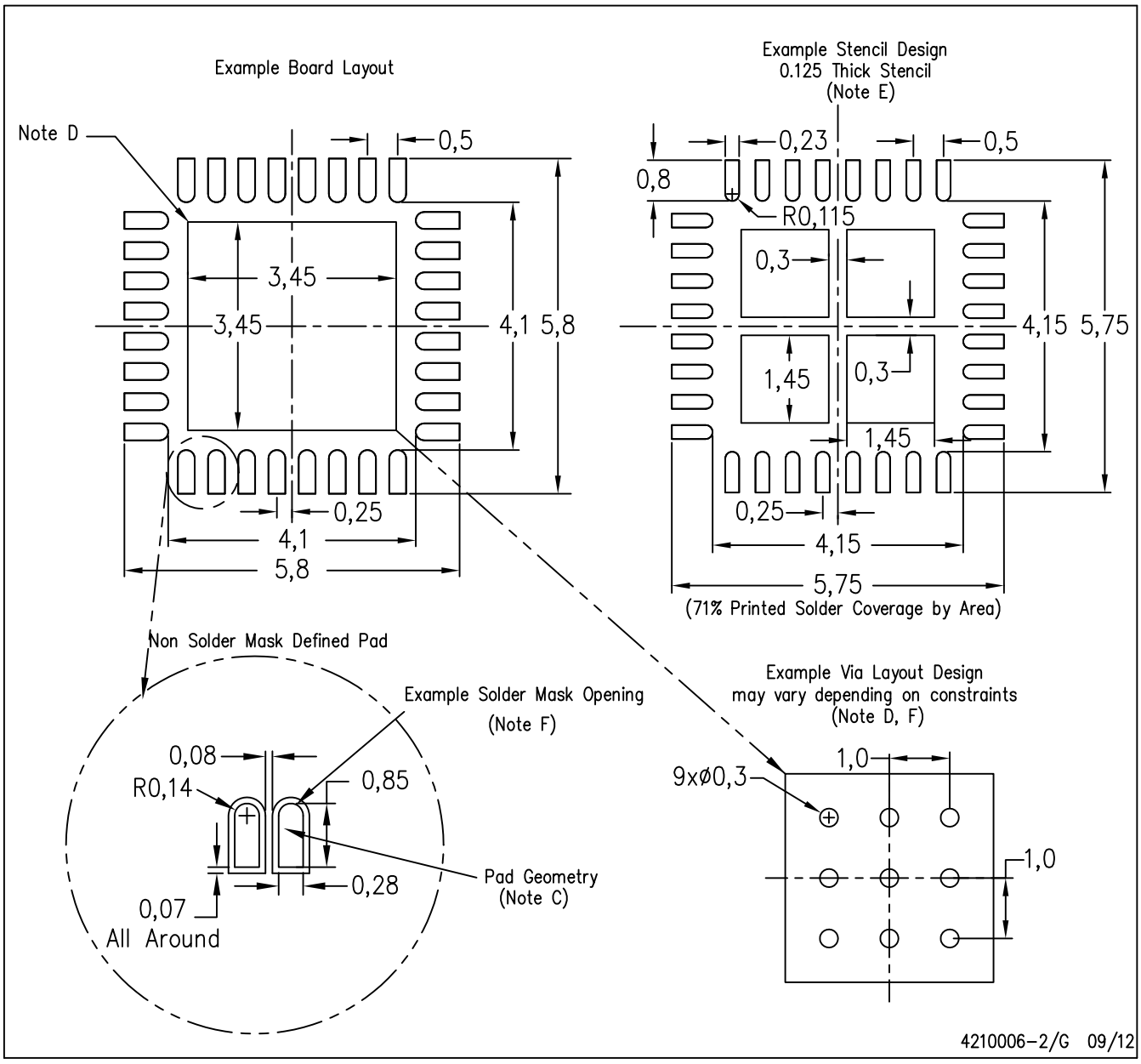
Bottom View

Exposed Thermal Pad Dimensions

4206250–2/K 09/12

NOTE: All linear dimensions are in millimeters

RTV (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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