TSM971/72/73/82/84

Ultra-Low-Power, Open-Drain Single/Dual-Supply Comparators

FEATURES

- Alternate source for:
  MAX971/MAX972/MAX973/MAX982/MAX984
- Ultra-Low Quiescent Current Over Temperature
  TSM971 Single+Reference: 4µA (max)
  TSM972: Dual Comparator Only: 4µA (max)
  TSM973/TSM982 Dual+Reference: 6µA (max)
  TSM984 Quad+Reference: 8.5µA (max)
- Single or Dual Power Supplies:
  Single: +2.5V to +11V
  Dual: ±1.25V to ±5.5V
- Input Voltage Range Includes Negative Supply
- 12µs Propagation Delay at 10mV Overdrive
- Open-drain Output Stages for Wired-OR Applications
- Internal 1.182V±1% Reference: TSM971/TSM973
- Internal 1.182V±2% Reference: TSM982/TSM984
- Adjustable Hysteresis: TSM971/TSM973/TSM982
- Separate Output GND Pin: TSM971/TSM984

APPLICATIONS

Threshold Detectors
Window Comparator
Level Translators
Oscillator Circuits
Battery-Powered Systems

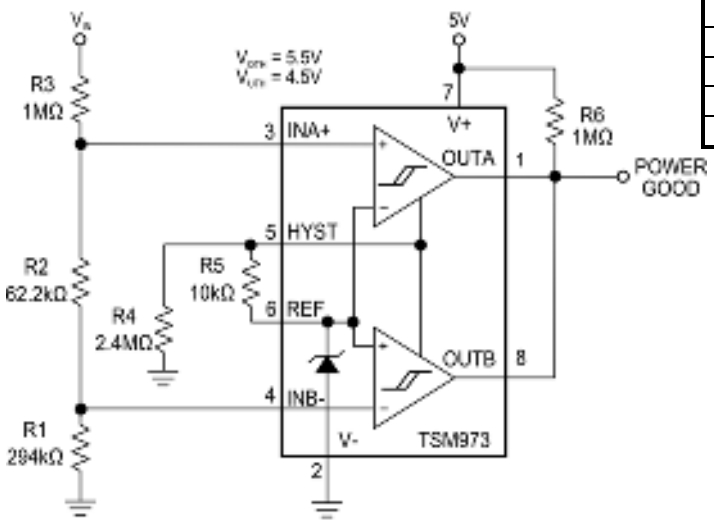
DESCRIPTION

The TSM971/972/973/982/984 family of single/dual/quad, low-voltage, micropower analog comparators is electrically and form-factor identical to the MAX971/972/973/982/984 family of analog comparators. Ideal for 3V or 5V single-supply applications, this comparator family can operate from single +2.5V to +11V supplies or from ±1.25V to ±5.5V dual supplies. The single TSM971 and the dual TSM972 draw less than 4µA (max) supply current over temperature. The TSM973/TSM982 duals and the quad TSM984 draw less than 3µA per comparator over temperature.

All comparators in this family exhibit an input voltage range from the negative supply rail to within 1.3V of the positive supply. Wired-OR applications are enabled as the comparators' output stages are open-drain. A 1.182V reference is internal to the TSM971/TSM973 (±1%) and the TSM982/TSM984 (±2%). Without complicated feedback configurations and only requiring two additional resistors, adding external hysteresis is available on the TSM971, TSM973, and the TSM982.

TYPICAL APPLICATION CIRCUIT

A 5V, Low-Parts-Count Window Detector



PART	INTERNAL REFERENCE	COMPARATORS PER PACKAGE	INTERNAL HYSTERESIS
TSM971	Yes, ±1%	1	Yes
TSM972	No	2	No
TSM973	Yes, ±1%	2	Yes
TSM982	Yes, ±2%	2	Yes
TSM984	Yes, ±2%	4	No

PART	TEMPERATURE RANGE	PACKAGE
TSM971C	0ºC to 70ºC	8-Pin MSOP/SOIC
TSM971E	-40ºC to 85ºC	
TSM972C	0ºC to 70ºC	8-Pin MSOP/SOIC
TSM972E	-40ºC to 85ºC	
TSM973C	0ºC to 70ºC	8-Pin MSOP/SOIC
TSM973E	-40ºC to 85ºC	
TSM982C	0ºC to 70ºC	8-Pin MSOP/SOIC
TSM982E	-40ºC to 85ºC	
TSM984C	0ºC to 70ºC	16-Pin SOIC
TSM984E	-40ºC to 85ºC	

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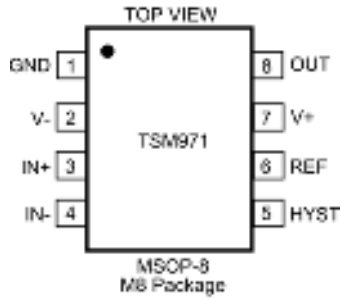
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to V-, V+ to GND, GND to V-).....-0.3V, +12V
Voltage Inputs
  (IN+, IN-).....(V+ + 0.3V) to (V- - 0.3V)
  HYST.....(REF + 5V) to (V- - 0.3V)
Output Voltage
  REF..... (V+ + 0.3V) to (V- - 0.3V)
  OUT (TSM971, TSM984).....(V+ + 0.3V) to (GND - 0.3V)
  OUT (TSM972/73, TSM982/84).... .....(V+ + 0.3V) to (V- - 0.3V)
Input Current (IN+, IN-, HYST).....20mA
Output Current
  REF.....20mA
  OUT.....50mA
Output Short-Circuit Duration (V+ ≤ 5.5V) .....Continuous

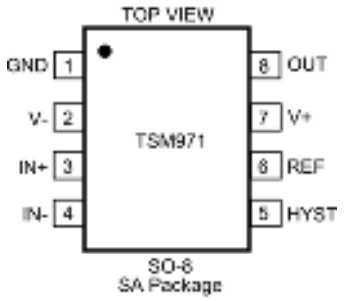
Continuous Power Dissipation (T_A = +70°C)
  8-Pin MSOP (derate 4.1mW/°C above +70°C) 330mW
  8-Pin SOIC (derate 5.88mW/°C above +70°C).....471mW
  16-Pin SOIC (8.7mW/°C above +70°C) 696mW
Operating Temperature Range
  TSM97xC.....0°C to +70°C
  TSM98xE.....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Electrical and thermal stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to any absolute maximum rating conditions for extended periods may affect device reliability and lifetime.

PACKAGE/ORDERING INFORMATION



MSOP-8
M8 Package

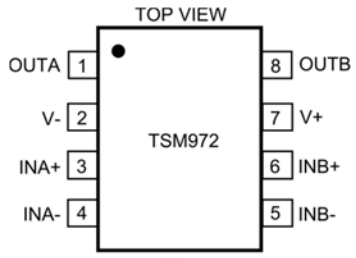


SO-8
SA Package

ORDER NUMBER	PART MARKING	CARRIER	QUANTITY
TSM971CUA+	TAAZ	Tube	50
TSM971CUA+T		Tape & Reel	2500

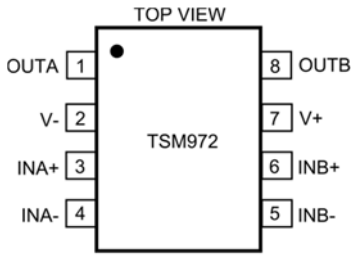
ORDER NUMBER	PART MARKING	CARRIER	QUANTITY
TSM971CSA+	TS971	Tube	97
TSM971CSA+T		Tape & Reel	2500
TSM971ESA+	TS971E	Tube	97
TSM971ESA+T		Tape & Reel	2500

PACKAGE/ORDERING INFORMATION



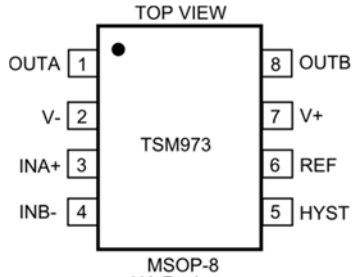
MSOP-8
M8 Package

ORDER NUMBER	PART MARKING	CARRIER	QUANTITY
TSM972CUA+	TABJ	Tube	50
TSM972CUA+T		Tape & Reel	2500



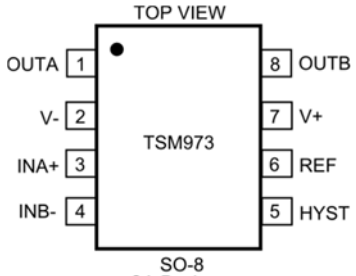
SO-8
SA Package

ORDER NUMBER	PART MARKING	CARRIER	QUANTITY
TSM972CSA+	TS972	Tube	97
TSM972CSA+T		Tape & Reel	2500
TSM972ESA+	TS972E	Tube	97
TSM972ESA+T		Tape & Reel	2500



MSOP-8
UA Package

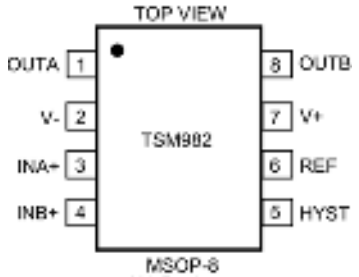
ORDER NUMBER	PART MARKING	CARRIER	QUANTITY
TSM973CUA+	TABE	Tube	50
TSM973CUA+T		Tape & Reel	2500



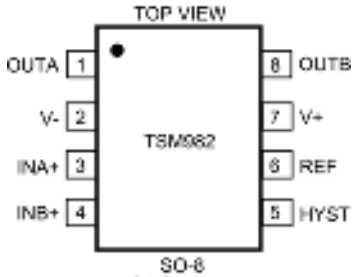
SO-8
SA Package

ORDER NUMBER	PART MARKING	CARRIER	QUANTITY
TSM973CSA+	TS973	Tube	97
TSM973CSA+T		Tape & Reel	2500
TSM973ESA+	TS973E	Tube	97
TSM973ESA+T		Tape & Reel	2500

PACKAGE/ORDERING INFORMATION



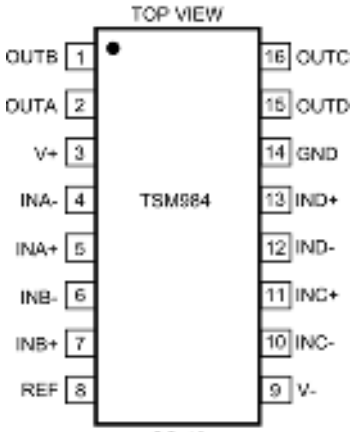
MSOP-8
UA Package



SO-8
SA Package

ORDER NUMBER	PART MARKING	CARRIER	QUANTITY
TSM982CUA+	TABK	Tube	50
TSM982CUA+T		Tape & Reel	2500

ORDER NUMBER	PART MARKING	CARRIER	QUANTITY
TSM982CSA+	TS982	Tube	97
TSM982CSA+T		Tape & Reel	2500
TSM982ESA+	TS982E	Tube	97
TSM982ESA+T		Tape & Reel	2500



SO-16
SE Package

ORDER NUMBER	PART MARKING	CARRIER	QUANTITY
TSM984CSE+	TS984	Tube	48
TSM984CSE+T		Tape & Reel	2500

ORDER NUMBER	PART MARKING	CARRIER	QUANTITY
TSM984ESE+	TS984E	Tube	48
TSM984ESE+T		Tape & Reel	2500

Lead-free Program: Silicon Labs supplies only lead-free packaging.

Consult Silicon Labs for products specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS – 5V OPERATION

V+ = 5V, V- = GND = 0V; T_A = -40ºC to +85ºC, unless otherwise noted. Typical values are at T_A = +25ºC. See Note 1.

PARAMETER	CONDITIONS			MIN	TYP	TSM	UNITS
POWER REQUIREMENTS							
Supply Voltage Range	See Note 2			2.5		11	V
Output Voltage Range				0		11	V
Supply Current	IN+ = IN- + 100mV	TSM971; HYST = REF	T_A = +25°C		2.5	3.2	µA
			T_A = -40°C to +85°C			4	
		TSM972	T_A = +25°C		2.5	3.2	
			T_A = -40°C to +85°C			4	
		TSM973 TSM982; HYST = REF	T_A = +25°C		3.1	4.5	
			T_A = -40°C to +85°C			6	
		TSM984	T_A = +25°C		5.5	6.5	
			T_A = -40°C to +85°C			8.5	
COMPARATOR							
Input Offset Voltage	V_{CM} = 2.5V					±10	mV
Input Leakage Current (IN-, IN+)	IN+ = IN- = 2.5V	C/E temp ranges			±0.01	±5	nA
Input Leakage Current (at HYST Pin)	TSM971, TSM973, TSM982				±0.02		nA
Input Common-Mode Voltage Range				V-		V+ – 1.3V	V
Common-Mode Rejection Ratio	V- to (V+ – 1.3V)				0.1	1.0	mV/V
Power-Supply Rejection Ratio	V+ = 2.5V to 11V				0.1	1.0	mV/V
Voltage Noise	100Hz to 100kHz				20		μV_{RMS}
Hysteresis Input Voltage Range	TSM971, TSM973, TSM982			REF- 0.05V		REF	V
Response Time (High-to-Low Transition)	T_A = +25°C; 100pF load; 1MΩ Pullup to V+	Overdrive = 10 mV			12		µs
		Overdrive = 100 mV			4		
Response Time (Low-to-High Transition)	T_A = +25°C; 100pF load; 1MΩ Pullup to V+. See Note 3				300		µs
Output Low Voltage	TSM9x2, TSM973	I_{OUT} = 1.8mA				V- + 0.4	V
	TSM971, TSM984	I_{OUT} = 1.8mA				GND + 0.4	
Output Leakage Current	V_{OUT} = 11V					100	nA
REFERENCE							
Reference Voltage	TSM971, TSM973		T_A = 0°C to +70°C, 1%	1.170	1.182	1.194	V
			T_A = -40°C to +85°C, 2%	1.158		1.206	V
	TSM982, TSM984		T_A = 0°C to +70°C, 2%	1.158	1.182	1.206	V
			T_A = -40°C to +85°C, 3%	1.147		1.217	V
Source Current			T_A = +25°C	15	25		µA
			T_A = -40°C to +85°C	6			
Sink Current			T_A = +25°C	8	15		µA
			T_A = -40°C to +85°C	4			
Voltage Noise	100Hz to 100kHz				100		μV_{RMS}

ELECTRICAL CHARACTERISTICS – 3V OPERATION

V+ = 3V, V- = GND = 0V; T_A = -40ºC to +85ºC, unless otherwise noted. Typical values are at T_A = +25ºC. See Note 1.

PARAMETER	CONDITIONS			MIN	TYP	TSM	UNITS
POWER REQUIREMENTS							
Supply Current	IN+ = IN- + 100mV	TSM971; HYST = REF	T_A = +25°C		2.4	3.0	µA
			T_A = -40°C to +85°C			3.8	
		TSM972	T_A = +25°C		2.4	3.0	
			T_A = -40°C to +85°C			3.8	
		TSM973 TSM982; HYST = REF	T_A = +25°C		3.4	4.3	
			T_A = -40°C to +85°C			5.8	
		TSM984	T_A = +25°C		5.2	6.2	
			T_A = -40°C to +85°C			8.0	
COMPARATOR							
Input Offset Voltage	V_{CM} = 1.5V					±10	mV
Input Leakage Current (IN-, IN+)	IN+ = IN- = 1.5V	C/E temp ranges			±0.01	±5	nA
Input Leakage Current (at HYST Pin)	TSM971, TSM973, TSM982				±0.02		nA
Input Common-Mode Voltage Range				V-		V+ – 1.3V	V
Common-Mode Rejection Ratio	V- to (V+ – 1.3V)				0.2	1.0	mV/V
Power-Supply Rejection Ratio	V+ = 2.5V to 11V				0.1	1.0	mV/V
Voltage Noise	100Hz to 100kHz				20		μV_{RMS}
Hysteresis Input Voltage Range	TSM971, TSM973, TSM982			REF- 0.05V		REF	V
Response Time (High-to-Low Transition)	T_A = +25°C; 100pF load; 1MΩ Pullup to V+	Overdrive = 10 mV			12		µs
		Overdrive = 100 mV			4		
Response Time (Low-to-High Transition)	T_A = +25°C; 100pF load; 1MΩ Pullup to V+. See Note 3				300		µs
Output Low Voltage	TSM9x2, TSM973	I_{OUT} = 0.8mA				V- + 0.4	V
	TSM971, TSM984	I_{OUT} = 0.8mA				GND + 0.4	
Output Leakage Current	V_{OUT} = 11V					100	nA
REFERENCE							
Reference Voltage	TSM971, TSM973		T_A = 0°C to +70°C, 1%	1.170	1.182	1.194	V
			T_A = -40°C to +85°C, 2%	1.158		1.206	V
	TSM982, TSM984		T_A = 0°C to +70°C, 2%	1.158	1.182	1.206	V
			T_A = -40°C to +85°C, 3%	1.147		1.217	V
Source Current			T_A = +25°C	15	25		µA
			T_A = -40°C to +85°C	6			
Sink Current			T_A = +25°C	8	15		µA
			T_A = -40°C to +85°C	4			
Voltage Noise	100Hz to 100kHz				100		μV_{RMS}

Note 1: All specifications are 100% tested at T_A = +25°C. Specification limits over temperature (T_A = T_{MIN} to T_{MAX}) are guaranteed by device characterization, not production tested.

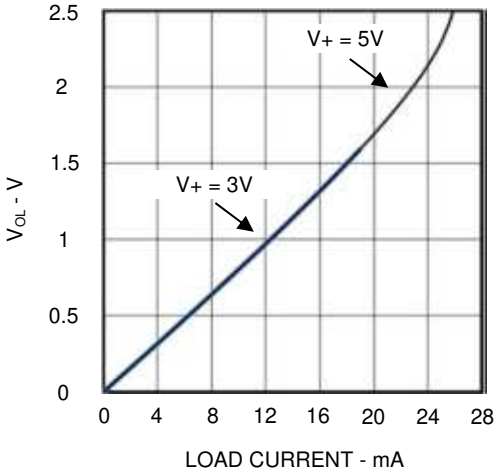
Note 2: The TSM934 comparator operates below 2.5V. Refer to the "Low-Voltage Operation: V+ = 1.5V (TSM984 Only)" section.

Note 3: Low-to-high response time is due to a 1MΩ pullup resistor and a 100pF capacitive load, based after three time constants. A smaller RC combination results in a faster response time.

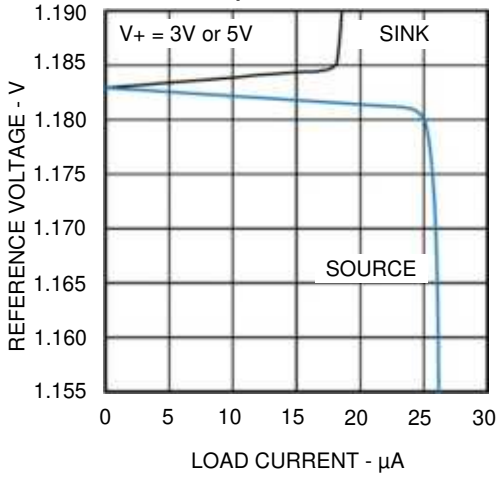
TYPICAL PERFORMANCE CHARACTERISTICS

V_+ = 5V; V_- = GND; T_A = +25°C, unless otherwise noted.

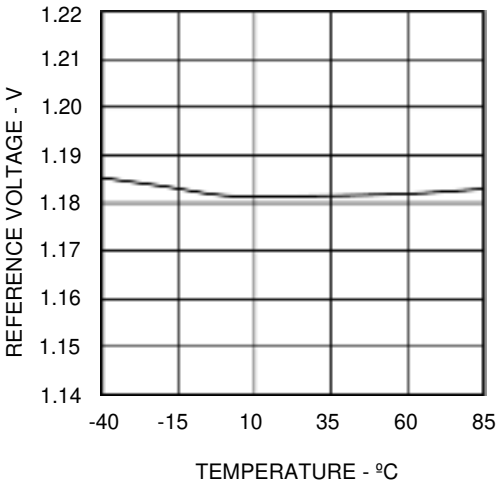
Output Voltage Low vs Load Current



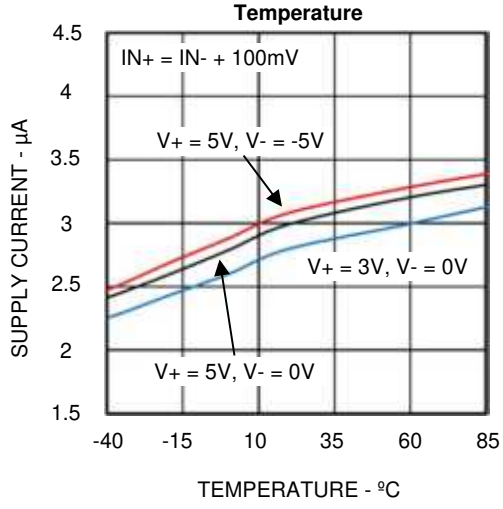
Reference Output Voltage vs Output Load Current



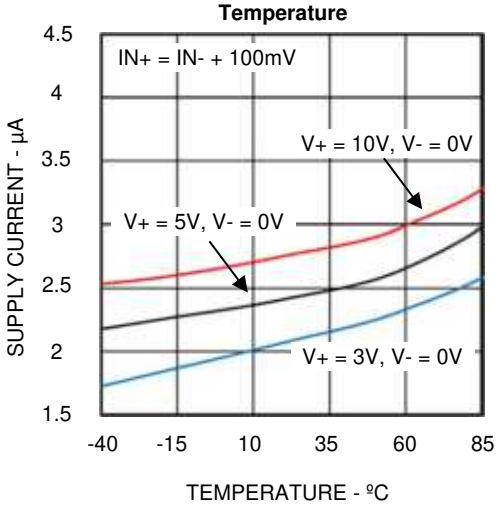
Reference Voltage vs Temperature



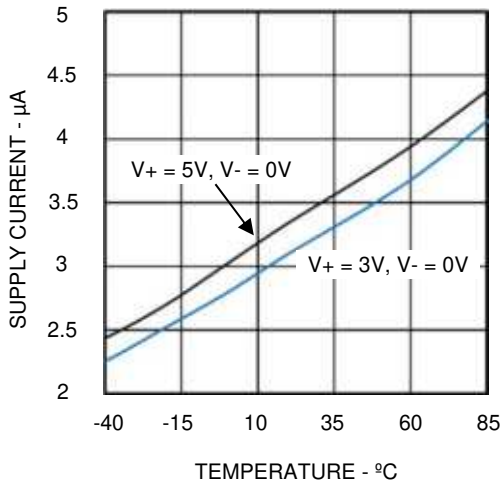
TSM971 Supply Current vs Temperature



TSM972 Supply Current vs Temperature



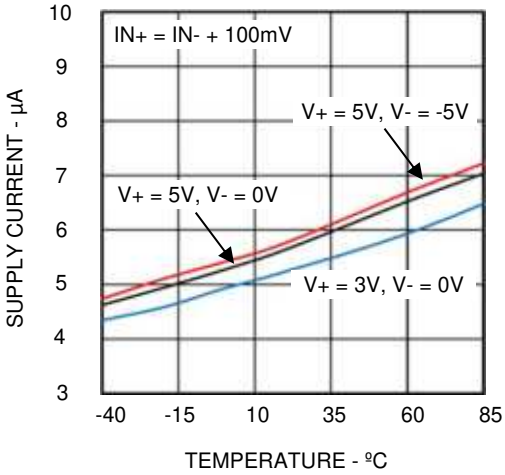
TSM973/982 Supply Current vs Temperature



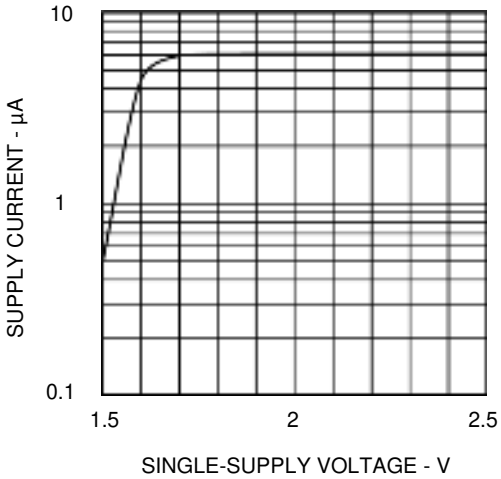
TYPICAL PERFORMANCE CHARACTERISTICS

V_+ = 5V; V_- = GND; T_A = +25°C, unless otherwise noted.

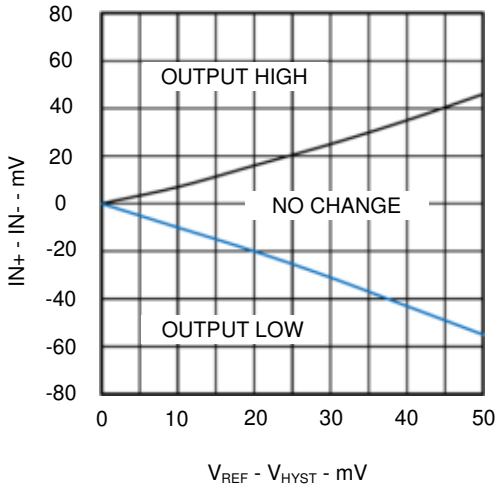
TSM984 Supply Current vs Temperature



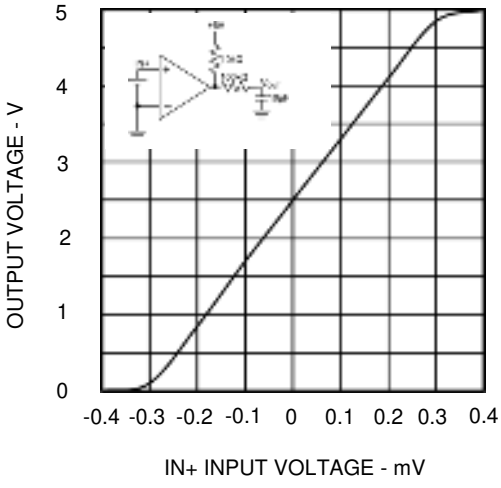
TSM984 Supply Current vs Low Supply Voltages



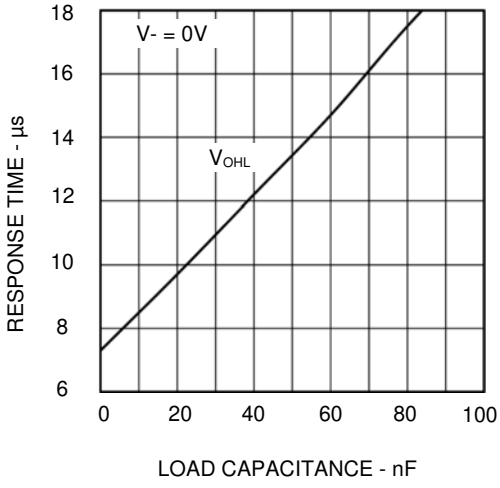
TSM971/973/982 Hysteresis Control



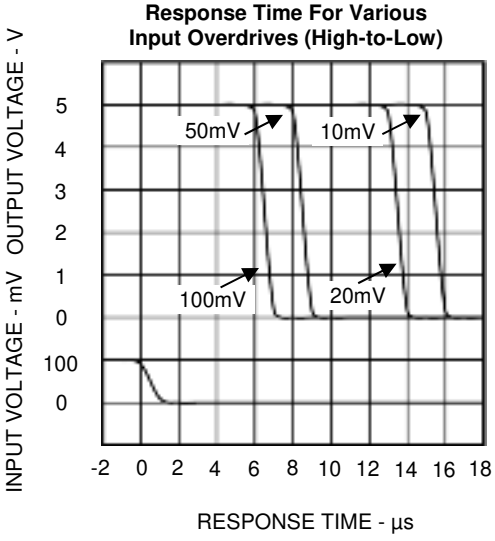
TSM971/972/984 Transfer Function



Response Time vs Load Capacitance



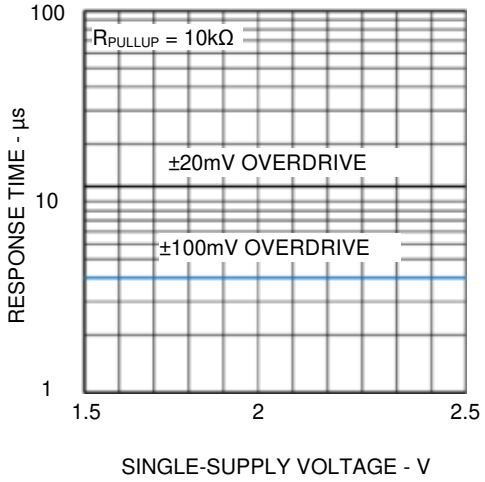
Response Time For Various Input Overdrives (High-to-Low)



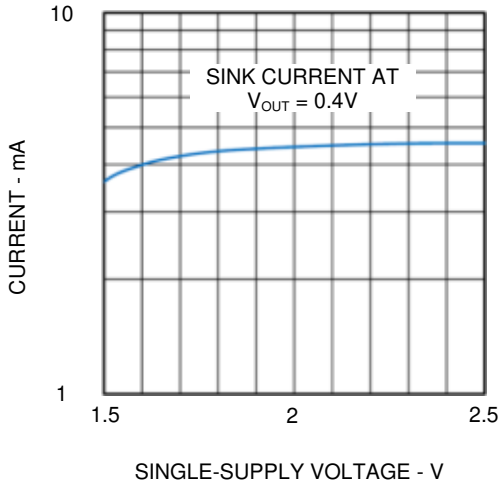
TYPICAL PERFORMANCE CHARACTERISTICS

V_+ = 5V; V_- = GND; T_A = +25°C, unless otherwise noted.

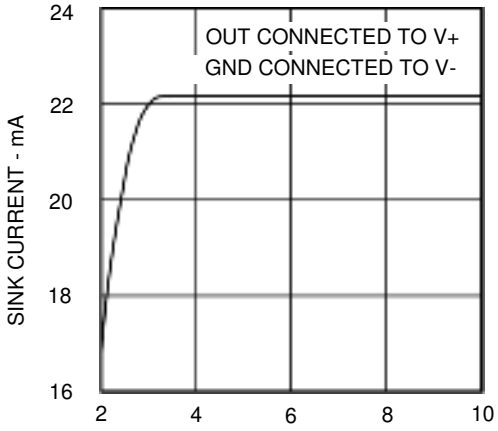
Response Time at Low Supply Voltages (Low-to-High)



TSM984 Sink Current at Low Supply Voltages



Short-Circuit Sink Current vs Supply Voltage

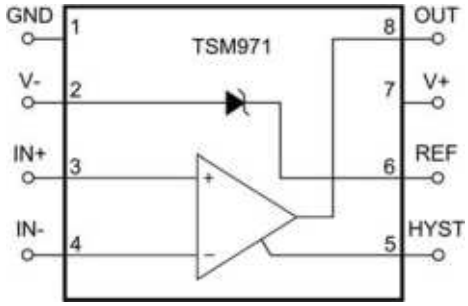


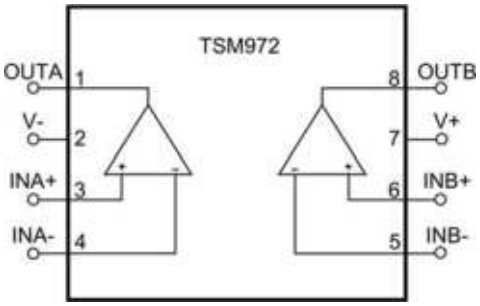
PIN FUNCTIONS

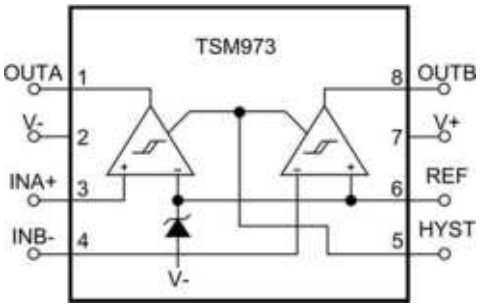
PIN				NAME	FUNCTION
TSM971	TSM972	TSM973	TSM982		
1	—	—	—	GND	Ground. Connect to V- for single-supply operation.
2	2	2	2	V-	Negative Supply. Connect to ground for single-supply operation (TSM971).
3	—	—	—	IN+	Comparator Noninverting Input
4	—	—	—	IN-	Comparator Inverting Input
5	—	5	5	HYST	Hysteresis Input. Connect to REF if not used. Input voltage range is from V_{REF} to (V_{REF} - 50mV).
6	—	6	6	REF	Reference Output. 1.182V with respect to V-.
7	7	7	7	V+	Positive Supply Voltage
8	—	—	—	OUT	Comparator Output. Sinks current to GND.
—	1	1	1	OUTA	Comparator A Output. Sinks current to V-.
—	3	3	3	INA+	Comparator A Noninverting Input
—	4	—	—	INA-	Comparator A Inverting Input
—	5	4	—	INB-	Comparator B Inverting Input
—	6	—	4	INB+	Comparator B Noninverting Input
—	8	8	8	OUTB	Comparator B Output. Sinks current to V-.

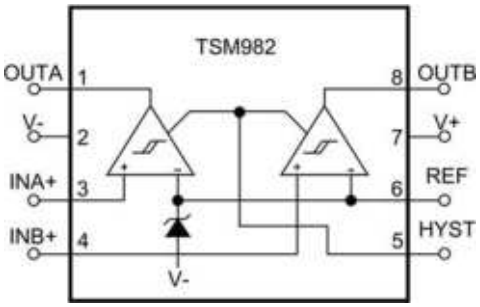
PIN	NAME	FUNCTION
TSM984		
1	OUTB	Comparator B Output. Sinks current to GND.
2	OUTA	Comparator A Output. Sinks current to GND.
3	V+	Positive Supply Voltage
4	INA-	Comparator A Inverting Input
5	INA+	Comparator A Noninverting Input
6	INB-	Comparator B Inverting Input
7	INB+	Comparator B Noninverting Input
8	REF	1.182V Reference Output with respect to V-.
9	V-	Negative Supply Voltage. Connect to ground for single-supply operation.
10	INC-	Comparator C Inverting Input
11	INC+	Comparator C Noninverting Input
12	IND-	Comparator D Inverting Input
13	IND+	Comparator D Noninverting Input
14	GND	Ground. Connect to V- for single-supply operation.
15	OUTD	Comparator D Output. Sinks current to GND.
16	OUTC	Comparator C Output. Sinks current to GND.

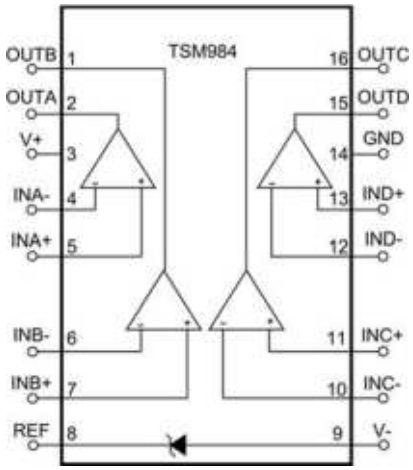
BLOCK DIAGRAMS











THEORY OF OPERATION

The TSM971/972/973/982/984 family of single/dual/quad, low-voltage, micropower analog comparators provide excellent flexibility and performance while sourcing continuously up to 40mA of current. The TSM971, TSM973, TSM982, and the TSM984 provide an on-board 1.182V reference voltage. To minimize current consumption while providing flexibility, the TSM971, TSM973, and the TSM982 have an on-board HYST pin in order to add additional hysteresis.

Power-Supply and Input Signal Ranges

The TSM971/972/973/982/984 can operate from a single supply voltage range of +2.5V to +11V, provide a wide common mode input voltage range of V- to V+-1.3V, and accept input signals ranging from V- to V+ - 1V. The inputs can accept an input as much as 300mV above the below the power supply rails without damage to the part. While the TSM971 and the TSM984 are able to operate from a single supply voltage range, a GND pin is available that allows for a dual supply operation with a range of ±1.25V to ±5.5V. If a single supply operation is desired, the GND pin needs to be tied to V-. In a dual supply mode, the TSM971 and the TSM984 are compatible with TTL/CMOS with a ±5V voltage and the TSM972, TSM973, and TSM982 are compatible with TTL with a single +5V supply.

Low-Voltage Operation: V+ = 1.5V (TSM984 Only)

Due to a decrease in propagation delay and a reduction in output drive, the TSM971/972/973/982 cannot be used with a supply voltage much lower than 2.5V. However, the TSM984 can operate down to a supply voltage of 2V; furthermore, as the supply voltage reduces, the TSM984 supply current drops and the performance is degraded. When the supply voltage drops to 2.2V, the reference voltage will no longer function; however, the comparators will function down to a 1.5V supply voltage. Furthermore, the input voltage range is extended to just below 1V the positive supply rail. For applications with a sub-2.5V power supply, it is recommended to evaluate the circuit over the entire power supply range and temperature.

Comparator Output

The TSM971 and the TSM984 have a GND pin that allows the output to swing from V+ to GND while the V- pin can be set to a voltage below GND as long as the voltage difference between V+ and V- is within 11V. The TSM971 and the TSM984 sink current to GND. By having open-drain outputs, the TSM971/972/973/982/984 can be used in wire-OREd and level-shifting applications. On the other hand, the TSM972, TSM973, and the TSM982 do not have a GND pin so the outputs sink current to V-. With a 100mV input overdrive, the propagation delay of the TSM971/972/973/982/984 is 4µs.

Voltage Reference

The TSM971/972/973 have an on-board 1.182V reference voltage with an accuracy of ±1% while the TSM982/984 have an on-board 1.182V reference voltage with an accuracy of ±2% across a temperature range of 0°C to +70°C. The REF pin is able to source and sink 25µA and 15µA of current, respectively. The REF pin is referenced to V- and it should not be bypassed.

Noise Considerations

Noise can play a role in the overall performance of the TSM971/972/973/982/984. Despite having a large gain, if the input voltage is near or equal to the input offset voltage, the output will randomly switch HIGH and LOW. As a result, the TSM971/972/973/982/984 produces a peak-to-peak noise of about 0.3mV while the reference voltage produces a peak-to-peak noise of about 1mV. Furthermore, it is important to design a layout that minimizes capacitive coupling from a given output to the reference pin as crosstalk can add noise and as a result, degrade performance.

APPLICATIONS INFORMATION

Hysteresis

As a result of circuit noise or unintended parasitic feedback, many analog comparators often break into oscillation within their linear region of operation especially when the applied differential input voltage approaches 0V (zero volt). Externally-introduced hysteresis is a well-established technique to stabilizing analog comparator behavior and requires external components. As shown in Figure 1, adding comparator hysteresis creates two trip points: V_{THR} (for the rising input voltage) and V_{THF} (for the falling input voltage). The hysteresis band (V_{HB}) is defined as the voltage difference between the two trip points. When a comparator's input voltages are equal,

hysteresis effectively forces one comparator input to move quickly past the other input, moving the input

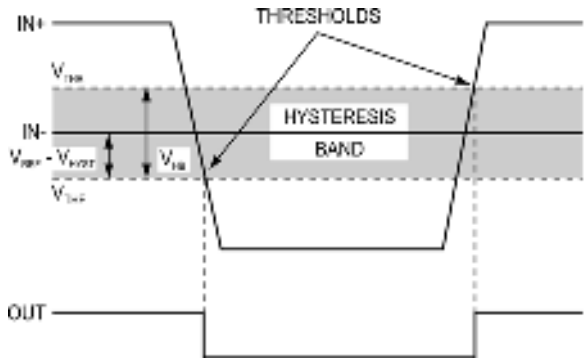


Figure 1. Threshold Hysteresis Band

out of the region where oscillation occurs. Figure 1 illustrates the case in which an IN- input is a fixed voltage and an IN+ is varied. If the input signals were reversed, the figure would be the same with an inverted output.

Hysteresis (TSM971/973 and TSM982)

Hysteresis can be generated with two external resistors using positive feedback as shown in Figure 2. Resistor R1 is connected between REF and HYST and R2 is connected between HYST and V-. This will increase the trip point for the rising input voltage, V_{THR}, and decrease the trip point for the falling input voltage, V_{THF}, by the same amount. If no hysteresis is required, connect HYST to REF. The hysteresis band, V_{HB}, is voltage across the REF and HYST pin multiplied by a factor of 2. The HYST pin can accept a voltage between REF and REF-50mV, where a voltage of REF-50mV generates the maximum voltage across R1 and thus, the maximum hysteresis and hysteresis band of 50mV and 100mV, respectively. To design the circuit for a desired hysteresis band, consider the equations below to acquire the values for resistors R1 and R2:

$$R1 = \frac{V_{HB}}{(2 \times I_{REF})}$$

$$R2 = \frac{1.182 - \frac{V_{HB}}{2}}{I_{REF}}$$

where I_{REF} is the primary source of current out of the reference pin and should be maintained within the maximum current the reference can source. This is

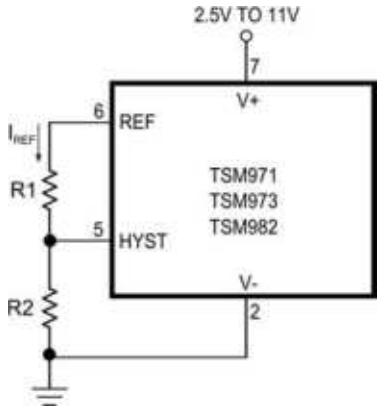


Figure 2. Programming the HYST Pin

typically in the range of 0.1µA and 4µA. It is also important to ensure that the current from reference is much larger than the HYST pin input current. Given R2 = 2.4MΩ, the current sourced by the reference is 0.5µA. This allows the hysteresis band and R1 to be approximated as follows:

$R1(k\Omega) = V_{HB}(mv)$

For the TSM973 and TSM982, the hysteresis is the same for both comparators.

Hysteresis (TSM972 and TSM984)

Relative to adding hysteresis with the HYST pin as was done for the TSM971, TSM973, and the TSM982, the circuit in Figure 3 uses positive feedback along with two external resistors to set the desired hysteresis. The circuit consumes more

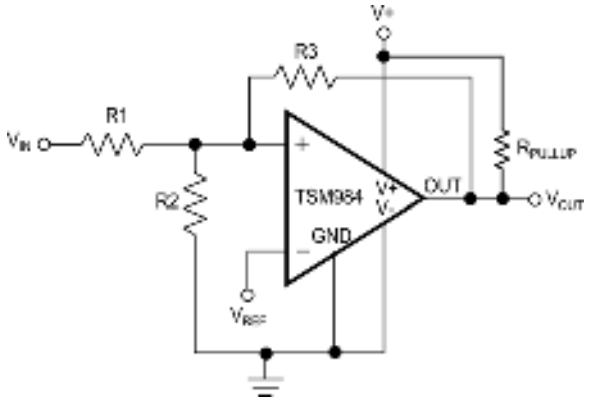


Figure 3. External Hysteresis

current and it slows down the hysteresis effect due to the high impedance on the feedback. Due to the pull-up resistor on the output and its inability to

source current, upper threshold variations will depend on the value of the pull-up resistor.

Board Layout and Bypassing

While power-supply bypass capacitors are not typically required, it is good engineering practice to use 0.1µF bypass capacitors close to the device's power supply pins when the power supply impedance is high, the power supply leads are long, or there is excessive noise on the power supply traces. To reduce stray capacitance, it is also good engineering practice to make signal trace lengths as short as possible. Also recommended are a ground plane and surface mount resistors and capacitors.

TYPICAL APPLICATION CIRCUITS

Window Detector

The schematic shown in Figure 4 is for a 4.5V undervoltage threshold detector and a 5.5V overvoltage threshold detector using the TSM973. Resistor components R1, R2, and R3 can be selected based on the threshold voltage desired while resistors R4 and R5 can be selected based on the hysteresis desired. Adding hysteresis to the circuit will minimize chattering on the output when the input voltage is close to the trip point. OUTA and OUTB generate the active-low undervoltage indication and active-low overvoltage indication, respectively. If both OUTA and OUTB signals are Wired-ORed, the resulting output is an active-high, power-good signal. To design the circuit, the following procedure needs to be performed:

1. As described in the section "Hysteresis (TSM971/973 and TSM982)", determine the desired hysteresis and select resistors R4 and R5 accordingly. This circuit has ±5mV of hysteresis at the input where the input voltage V_{IN} will appear larger due to the input resistor divider.
2. Selecting R1. As the leakage current at the INB- pin is less than 1nA, the current through R1 should be at least 100nA to minimize offset voltage errors caused by the input leakage current. Values within 100kΩ and 1MΩ are recommended. In this example, a 294kΩ, 1% standard value resistor is selected for R1.
3. Calculating R2 + R3. As the input voltage V_{IN} rises, the overvoltage threshold should be 5.5V. Choose R2 + R3 as follows:

$$R2 + R3 = R1 \times \left(\frac{V_{OTH}}{V_{REF}+V_{HYS}} - 1\right)$$

$$= 294k\Omega \times \left(\frac{5.5V}{1.182V + 5mV} - 1\right)$$

$$= 1.068M\Omega$$

4. Calculating R2. As the input voltage V_{IN} falls, the undervoltage threshold should be 4.5V. Choose R2 as follows:

$$R2 = (R1 + R2 + R3) \times \frac{(V_{REF}-V_{HYS})}{V_{UTH}} - 294k$$

$$= (294k\Omega + 1.068M\Omega) \times \frac{(1.182V-5mV)}{4.5} - 294k$$

$$= 62.2k\Omega$$

In this example, a 61.9kΩ, 1% standard value resistor is selected for R2.

5. Calculating R3.

$$R3 = (R2 + R3) - R2$$

$$= 1.068M\Omega - 61.9k\Omega$$

$$= 1.006M\Omega$$

In this example, a 1MΩ, 1% standard value resistor is selected for R3.

6. Using the equations below, verify all resistor values selected:

$$V_{OTH} = (V_{REF} + V_{HYS}) \times \frac{(R1 + R2 + R3)}{R1}$$

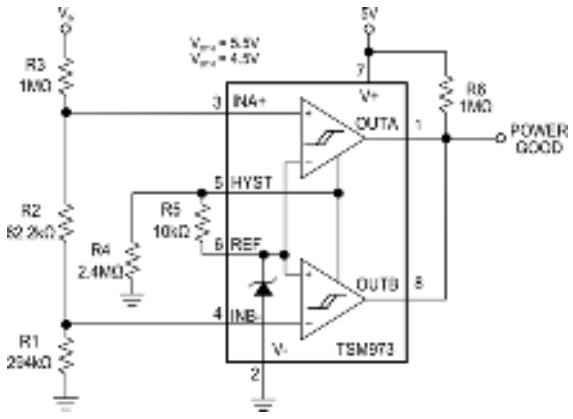


Figure 4. Window Detector

= 5.474V

$$V_{OTH} = (V_{REF} - V_{HYS}) \times \frac{(R1 + R2 + R3)}{(R1+R2)}$$

= 4.484V

Where the hysteresis voltage is given by:

$$V_{HYS} = V_{REF} \times \frac{R5}{R4}$$

Battery Switchover Circuit

Diodes are typically used in applications where power to a device switches from a line-powered DC to a backup battery. However, the voltage drop and power loss across the diodes is undesired. Figure 5 shows a different approach that replaces the diode with a P-channel MOSFET and uses the TSM973 to control the MOSFET. When the voltage from the line-powered DC drops below 4V, OUTA switches low, and then turns on Q1. When the battery drops below 3.6V, Comparator B generates a “low-battery” signal.

Level Shifter

Figure 6 provides a simple way to shift from bipolar ±5V inputs to TTL signals by using the TSM984. To protect the comparator inputs, 10kΩ resistors are placed in series and do not have an effect on the performance of the circuit.

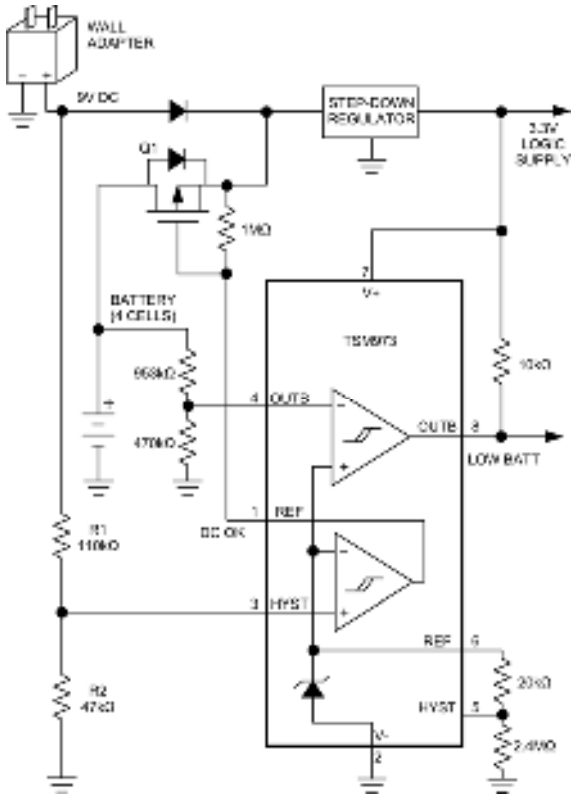


Figure 5. Battery Switchover Circuit

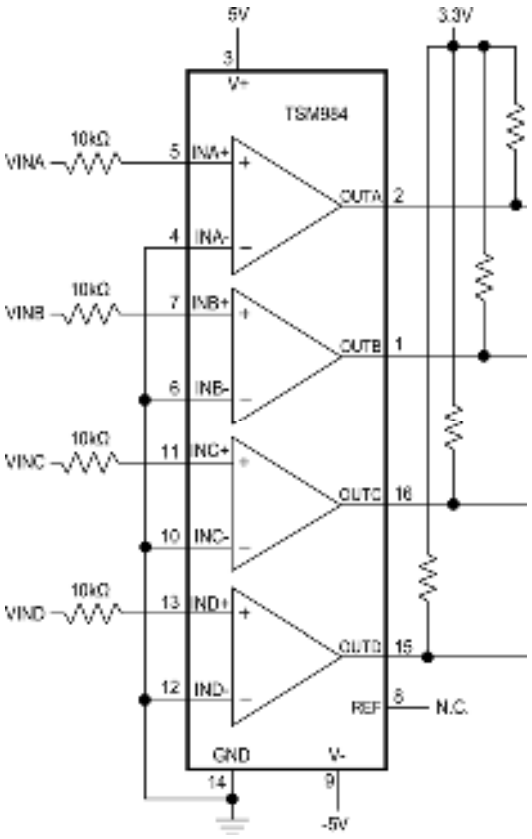
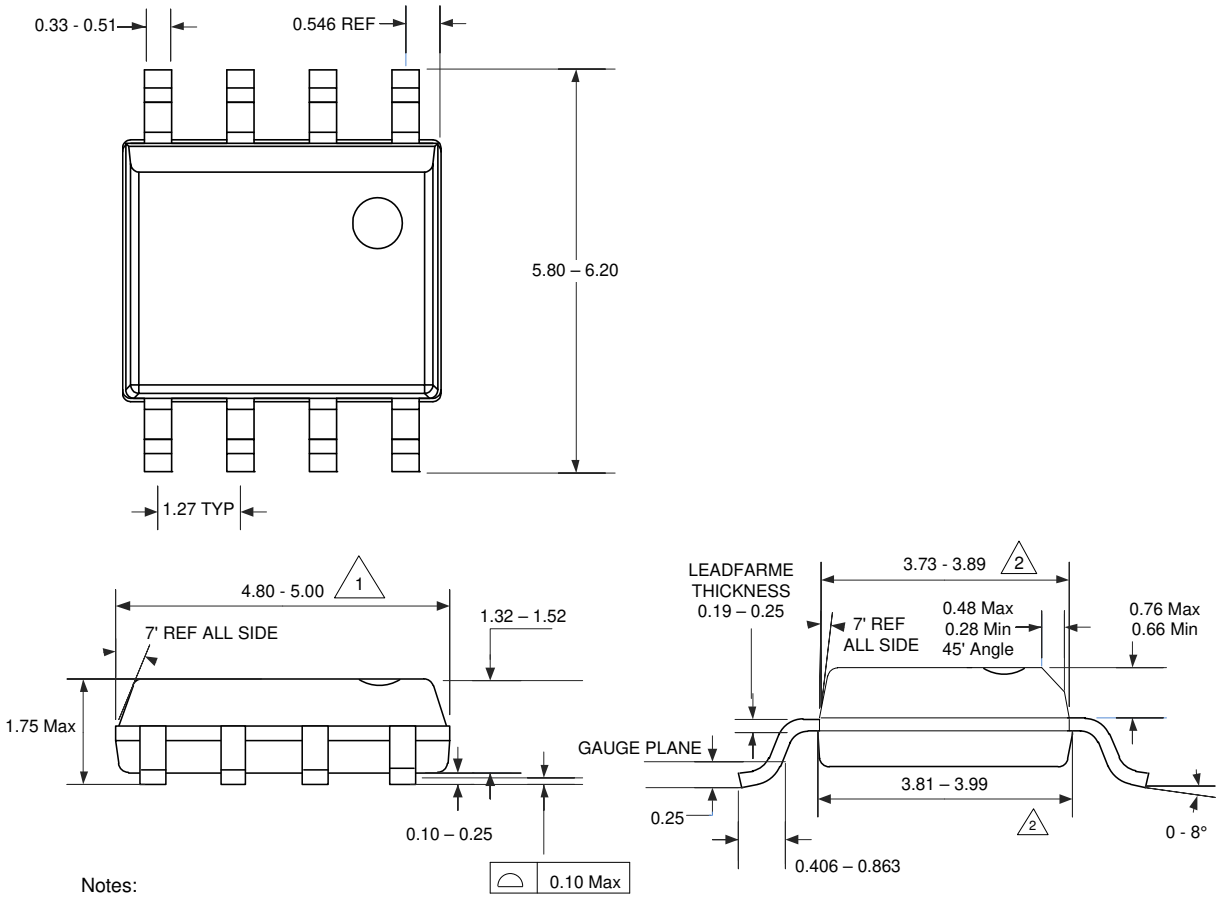


Figure 6. Level Shifter: ±5V Input to Single-Ended 3.3V Output

PACKAGE OUTLINE DRAWING

8-Pin SOIC Package Outline Drawing

(N.B., Drawings are not to scale)



Notes:

1. Does not include mold flash, protrusions or gate burns. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.

2. Does not include inter-lead flash or protrusions. Inter-lead flash or protrusions shall not exceed 0.25 mm per side.

3. Lead span/stand off height/coplanarity are considered as special characteristic (s).

4. Controlling dimensions are in mm.

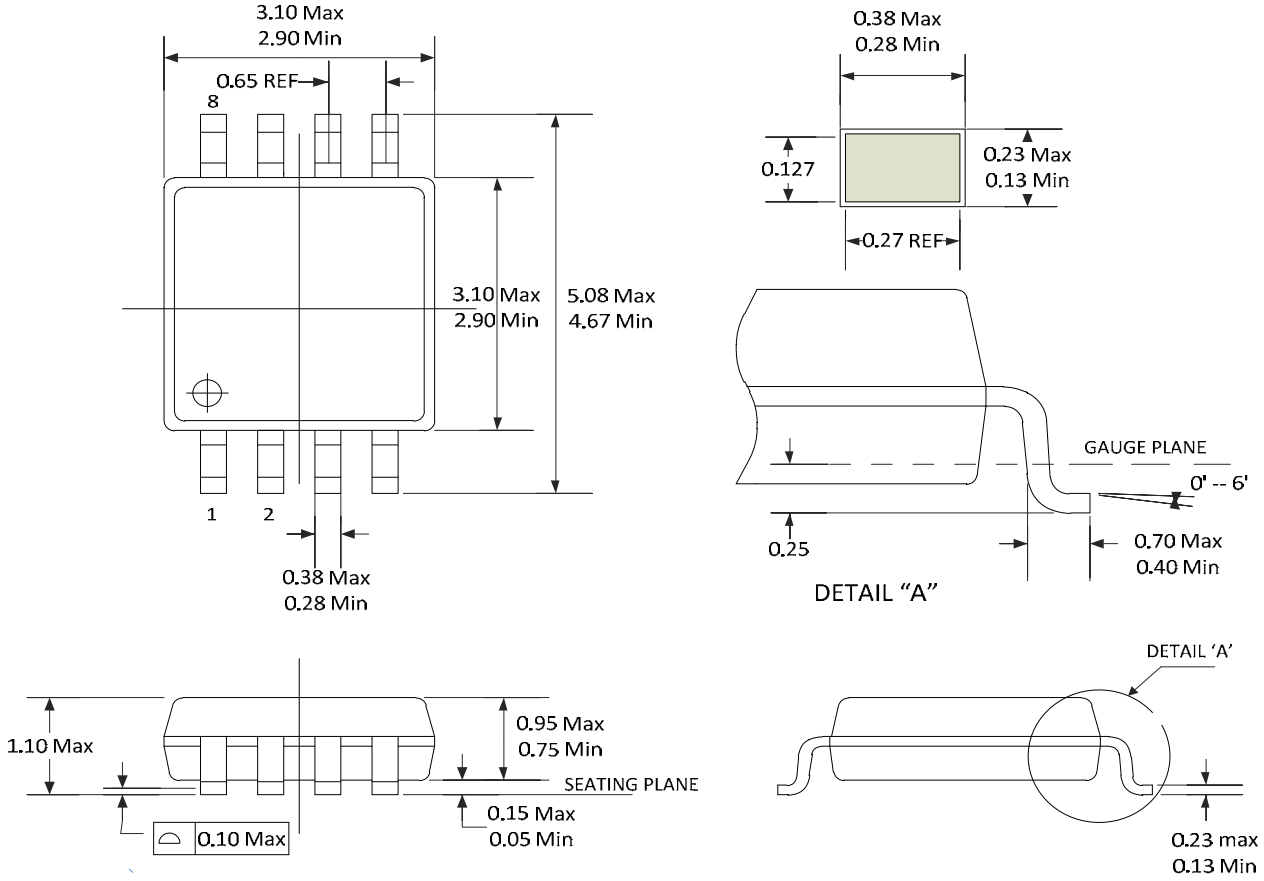
5. This part is compliant with JEDEC specification MS-012

6. Lead span/stand off height/coplanarity are considered as Special characteristic.

PACKAGE OUTLINE DRAWING

8-Pin MSOP Package Outline Drawing

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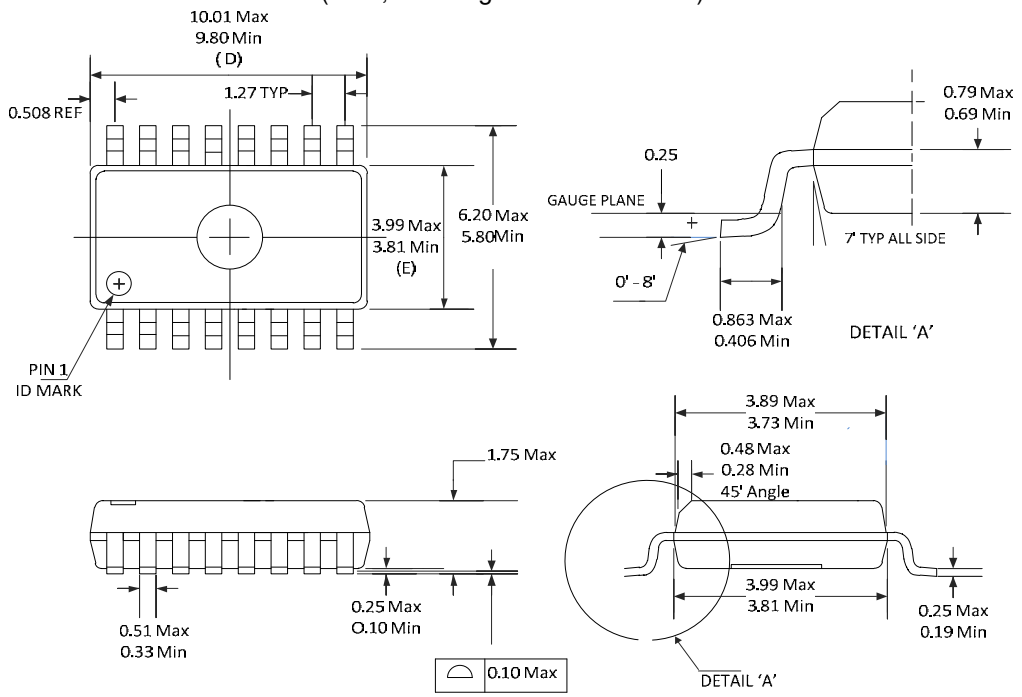
NOTE:

1. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
2. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTUSIONS.
3. CONTROLLING DIMENSION IN MILIMETERS.
4. THIS PART IS COMPLIANT WITH JEDEC MO-187 VARIATIONS AA
5. LEAD SPAN/STAND OFF HEIGHT/COPLANARITY ARE CONSIDERED AS SPECIAL CHARACTERISTIC.

PACKAGE OUTLINE DRAWING

16-Pin SOIC Package Outline Drawing

(N.B., Drawings are not to scale)



NOTE:

1. "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE.
2. "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS.
   INTER-LEAD FLASH AND PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25 mm PER SIDE.
3. CONTROLLING DIMENSIONS IN MILIMETERS AND ANGLES IN DEGREES.
4. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MS-012 AB
5. LEAD SPAN/STAND OFF HEIGHT/COPLANARITY ARE CONSIDERED AS SPECIAL CHARACTERISTIC.

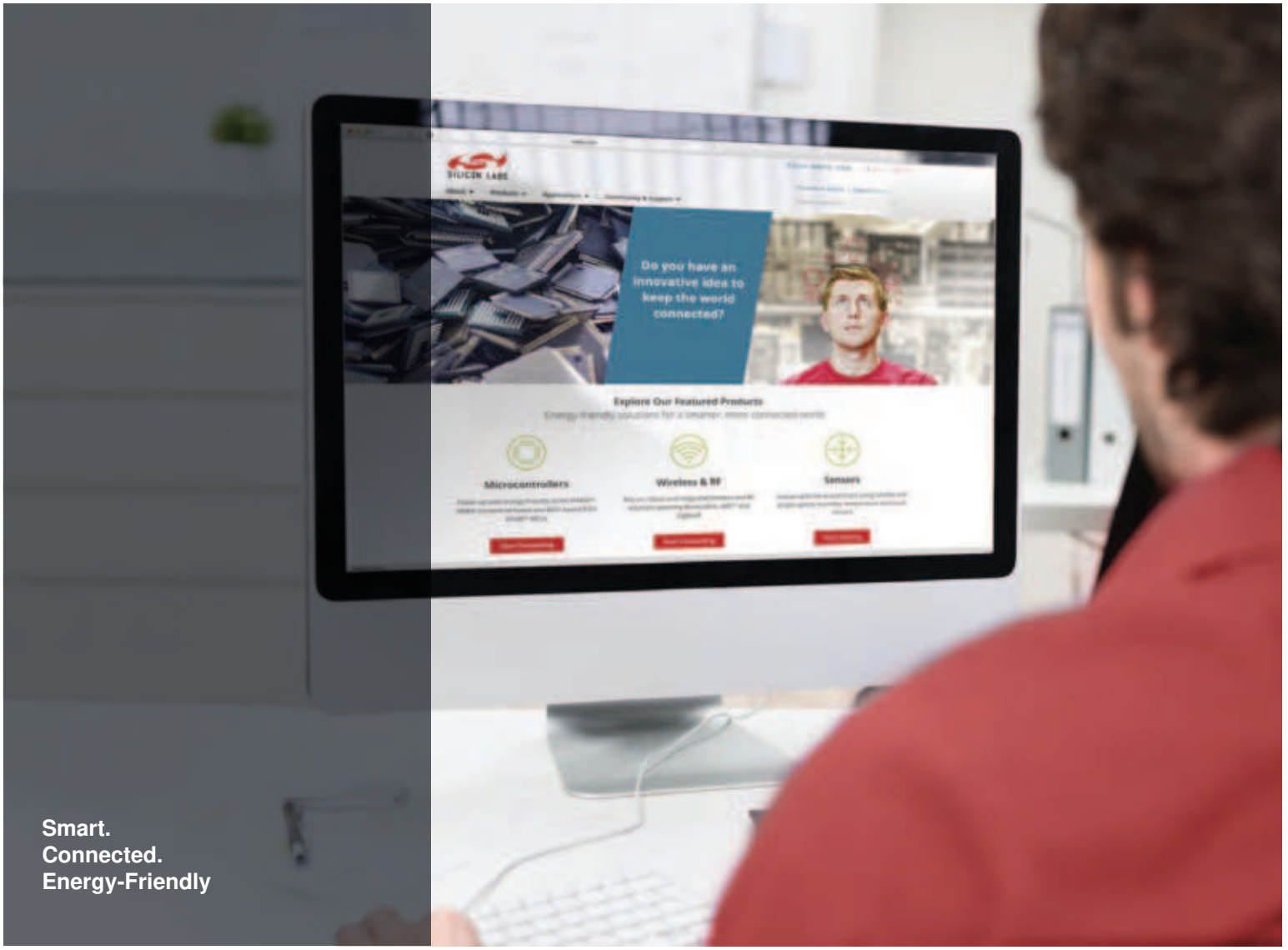
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