TVP9900
VSB/QAM Receiver

Data Manual

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TEXAS INSTRUMENTS

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1 Introduction

The TVP9900 is a cost-effective digital TV (DTV) front-end IC targeted for low-cost high-volume DTV receivers. The TVP9900 is a system-on-chip (SoC) device that integrates the main functions of a DTV front-end system, including a programmable gain amplifier (PGA), A/D converter, VSB demodulator, ATSC forward error correction (FEC), QAM demodulator, and ITU-T Annex B FEC. It provides rich peripheral support including AGC control, tuner control, CEA-909 antenna control, and host I^2C interface. The TVP9900 supports processing of ATSC VSB or ITU-T Annex B QAM IF inputs.

1.1 Features

- **ATSC 8-VSB Demodulation and FEC**
- **ITU-J.83B Compliant 64/256 QAM Demodulation and FEC**
- **Direct 44-MHz IF Sampling Eliminates Need for External Downconverter**
- **Integrated IF PGA**
- **Integrated High-Speed 10-bit A/D Converter**
- **Integrated Digital Filter Relaxes External Tuner Filters**
- **Sigma-Delta Digital-to-Analog Converter (DAC) for AGC Control**
- **Adjacent Channel Filter**
- **NTSC Co-Channel Rejection Filter**
- **All Digital Timing Recovery**
- **Pilot Tracking Loop With Lock Status Indicator Signal**
- **Decision-Directed Carrier Phase Tracking Loop**
- **Field and Segment Synchronization With Sync Status Indicator Signal**
- **Host Interrupt for Remote Monitoring of Signal Quality**
- **SNR Monitor**
- **BER Monitor**
- **Integrated De-Interleaver RAM**
- **Parallel/Serial MPEG Output Interface With Error Packet Indicator**
- **Direct Tuner Control Interface**
- **EIA/CEA-909 Antenna Control Interface**
- **Option for 4-MHz Clock Input Driven by MOP IC in Tuner, So No Quartz Crystal Required for Demodulator**
- **External DAC and VCXO for Clock Recovery Not Required**
- **Equalizer Covers Echo Profile Required by ATSC A.74 Guideline**
- **Superior Multipath Performance Demodulating for Brazil Ensembles A Through E**
- **Power-Down Mode**
- **80-Pin TQFP Package**

1.2 Ordering Information

T_A	PACKAGED DEVICES(1)	PACKAGE OPTION
	80-Pin TQFP PowerPAD™ Package	
0°C to 70°C	TVP9900PFP	Tray
	TVP9900PFPR	Tape and Reel

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

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2 Block Diagram

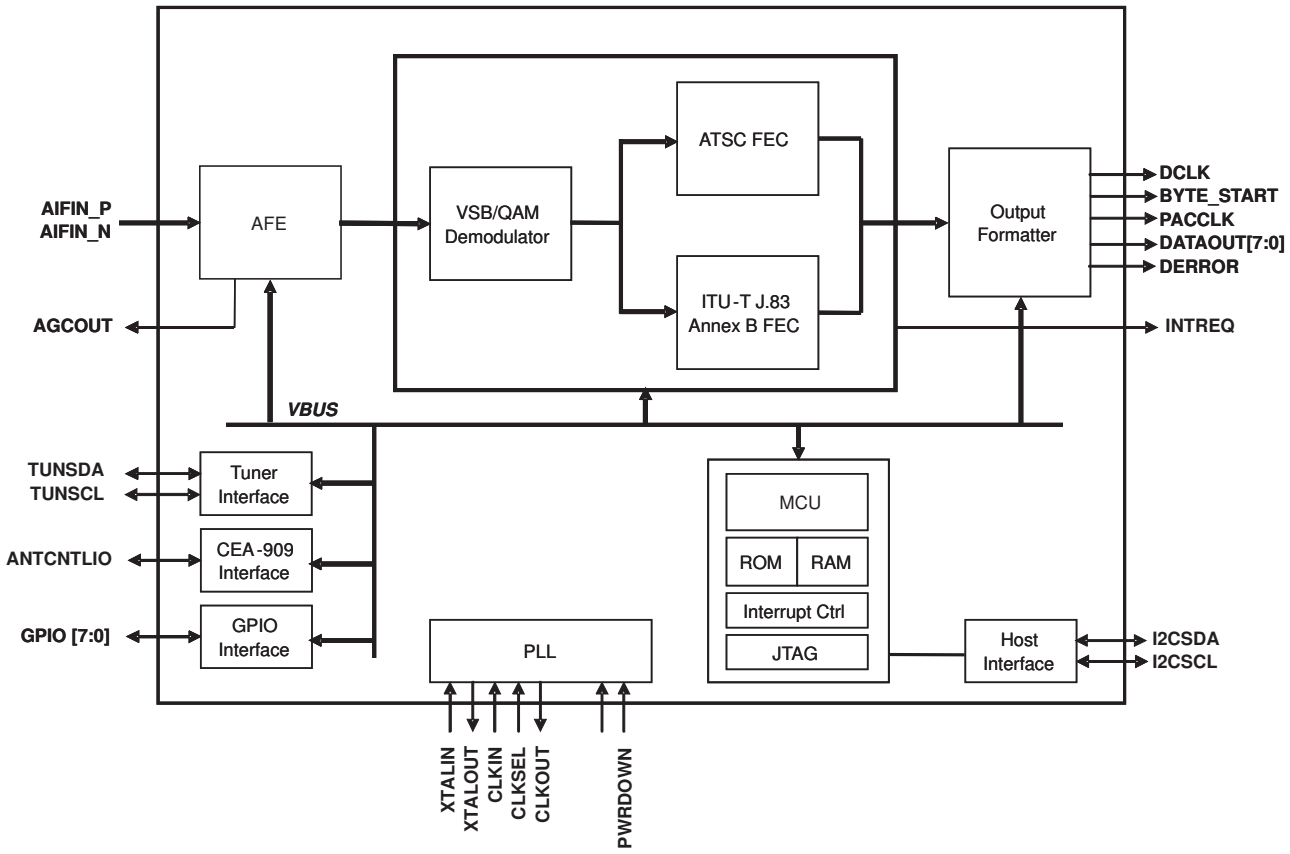
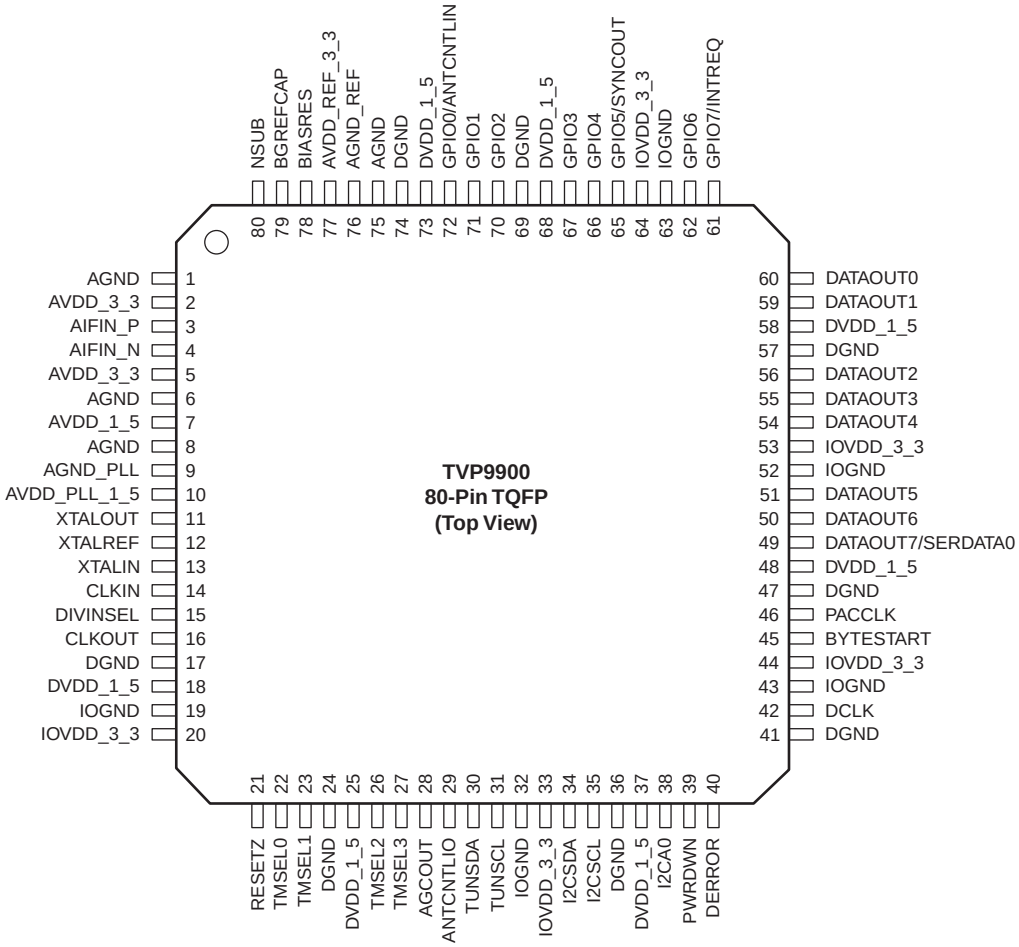


Figure 2-1. TVP9900 Block Diagram

3 Terminal Assignments

3.1 Pinout



3.2 Terminal Functions

Table 3-1. Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
IF Interface			
AIFIN_P	3	I	Analog positive differential IF input
AIFIN_N	4	I	Analog negative differential IF input
Transport Stream Interface			
DCLK	42	O	MPEG-2 data clock output
BYTE_START	45	O	MPEG-2 byte start signal. An active-high output signal that indicates the first byte of a transport stream data packet.
PACCLK	46	O	MPEG-2 interface packet framing signal. An active-high output signal that remains high for the entire length of the valid data packet.
DERROR	40	O	MPEG-2 interface data error. An active-high output signal that indicates an error in the data output packet. Indicates an error in the input data. This pin should be tied low if not in use.
DATAOUT7/SERDATA0	49	O	1. MPEG-2 parallel data output. Bit 7 is the first bit of the transport stream. 2. MPEG-2 serial data output
DATAOUT[6:0]	50, 51, 54, 55, 56, 59, 60	O	MPEG-2 parallel data output bits 6-0
Clock Signals			
XTALIN	13	I	Crystal input. Input to the on-chip oscillator from an external crystal. The required crystal frequency is 25 MHz. This input can also be driven by an external clock source instead of a crystal. When using an external clock source, a 4-MHz or 25-MHz clock must be used. NOTE: If an external clock source is used, the input can only be used with 1.5-V signal levels.
XTALOUT	11	O	Crystal output. Output from the on-chip oscillator to an external crystal.
XTALREF	12	I	External crystal reference. This pin is used for the external crystal capacitor ground reference.
CLKIN	14	I	Test clock input. For normal operation, this input should be tied low.
DIVINSEL	15	I	PLL VCO divider default input select. This input is used to select the default VCO divider value for the PLL. If a 25-MHz crystal or clock is used for XTALIN, DIVINSEL should be driven low. If a 4-MHz clock is used for XTALIN, DIVINSEL should be driven high.
CLKOUT	16	O	Test clock output. For normal operation, this output is not used.
Miscellaneous Signals			
AGCOUT	28	O	AGC control delta-sigma DAC output
ANTCNTLIO	29	I/O	Smart antenna control interface input/output
TUNSDA	30	I/O	Tuner I^2C serial data input/output. NOTE: The output functions as an open drain.
TUNSCL	31	I/O	Tuner I^2C serial clock. NOTE: The output functions as an open drain.
GPIO7/INTREQ	61	I/O	1. General-purpose I/O 2. Interrupt request output
GPIO6	62	I/O	1. General-purpose I/O 2. Reserved
GPIO5/SYNCOUT	65	I/O	1. General-purpose I/O 2. Sync output
GPIO[4:2]	66, 67, 70	I/O	General-purpose I/O
GPIO1	71	O	Dedicated to smart antenna support. Outputs direction of signal on pin 29 in smart antenna 1-pin mode. 0 = Signal input from antenna to TVP9900, pin 29 1 = Signal output from TVP9900 pin 29 to antenna
GPIO0/ANTCNTLIN	72	I/O	1. General-purpose I/O 2. Antenna Control Input

Table 3-1. Terminal Functions (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
RESETZ	21	I	System reset. An active-low asynchronous input that initializes the device to the default state.
PWRDOWN	39	I	Power down terminal. An active-high signal puts the device in a low power state.
TMSEL[3:0]	22, 23, 26, 27	I	Test mode select. Tie low for normal operation.
Host Interface			
I2CSDA	34	I/O	Host I^2C serial data input/output. NOTE: The pin functions as an open-drain output.
I2CSCL	35	I/O	Host I^2C serial clock. NOTE: The pin functions as an open-drain output.
I2CA0	38	I	Host I^2C device address select. Determines address for I^2C (sampled during reset). A pullup or pulldown 10-kΩ resistor is needed to program the terminal to the desired address. 0 = Address is 0xB8h 1 = Address is 0xBAh
Power Supplies			
DVDD_1_5	18, 25, 37, 48, 58, 68, 73	P	Digital power supply. Connect to 1.5-V digital supply.
DGND	17, 24, 36, 41, 47, 57, 69, 74	P	Digital power supply return. Connect to digital ground.
IOVDD_3_3	20, 33, 44, 53, 64	P	IO power supply. Connect to 3.3-V digital supply.
IOGND	19, 32, 43, 52, 63	P	IO power supply return. Connect to digital ground.
AVDD_3_3	2, 5	P	Analog power supply. Connect to 3.3-V analog supply.
AVDD_1_5	7	P	Analog power supply. Connect to 1.5-V analog supply.
AGND	1, 6, 8, 75	P	Analog power supply return. Connect to analog ground.
AVDD_PLL_1_5	10	P	PLL power supply. Connect to 1.5-V analog supply.
AGND_PLL	9	P	PLL power supply return. Connect to analog ground.
NSUB	80	P	Die substrate. Connect to PCB ground.
AVDD_REF_3_3	77	P	Analog reference power supply. Connect to 3.3-V analog supply.
AGND_REF	76	P	Analog reference ground. Connect to analog ground.
BGREFCAP	79	O	Band-gap reference capacitor connection
BIASRES	78	O	Analog bias register. Connect through a 24-kΩ resistor to PCB ground.

4 Functional Description

4.1 Analog Front End

The TVP9900 receiver has an analog input channel that accepts one differential or single-ended 44-MHz center frequency IF input, which are ac coupled. The receiver supports a maximum input differential voltage range of 1 Vpp with PGA setting at unity gain. The programmable gain amplifier (PGA) and the AGC circuit work together and ensure that the input signal is amplified sufficiently to ensure the proper input range for the ADC. The ADC has 10 bits of resolution. The clock input for the ADC comes from the phase-locked loop (PLL). An external downconverter is not required to use this IF direct sampling method. The analog front end and adjacent digital filter can potentially relax the requirement for external analog filters, and only one external SAW filter is required.

4.2 VSB/QAM Demodulator

The VSB/QAM demodulator is designed for 8-VSB demodulation compliant with ATSC, and 64/256 QAM demodulation compliant with ITU-T J83 Annex B. The VSB/QAM demodulator in the TVP9900 is composed of the following blocks:

- Automatic gain control (AGC)
- Adjacent channel filter
- NTSC rejection filter
- Timing recovery
- Pilot tracking
- Matched filter
- Decision feedback equalizer
- Carrier recovery

The all-digital demodulator architecture does not require an external downconverter, AGC control DAC, clock recovery VCXO, or carrier recovery VCXO. This architecture makes a low-cost system implementation possible.

4.3 Forward Error Correction (FEC)

FEC in the TVP9000 includes the following blocks:

- QAM FEC
  - Trellis decoder
  - Synchronizer
  - De-randomizer
  - De-interleaver
  - Reed Solomon decoder
  - MPEG deframer
- VSB FEC
  - Trellis decoder
  - Synchronizer
  - De-interleaver
  - Reed Solomon decoder
  - De-randomizer

The Trellis decoder is designed for help protect against short-burst interference. The VSB synchronizer performs segment and frame synchronization and outputs the synchronization signal with data. An internal RAM is shared by both VSB and QAM modes, and additional external RAM is not required.

4.4 Output Formatter

The TVP9900 transport stream interfaces directly to the back-end IC, which provides transport stream compliance with ISO/IEC 13818-1 in parallel or serial modes. The details of the transport stream interface are shown in Table 4-1. In serial mode, DATAOUT[7] is used as the serial data output, with the MSB output first. The maximum output rate is 42.1 Mbit/s in serial mode. The polarity of DCLK, BYTE_START, DERROR, and PACCLK is programmable.

Table 4-1. MPEG-2 Transport Stream Interface

TERMINAL	TYPE	DESCRIPTION
DCLK	O	Parallel/serial clock output
DATAOUT[7:0]	O	Parallel/serial data output DATAOUT7 is the first bit of the transport stream in parallel mode. DATAOUT7 is the serial data output in serial mode.
BYTE_START	O	Packet sync, indicates the start byte of a transport packet
PACCLK	O	Packet enable, indicates the valid packet data

Figure 4-1 and Figure 4-2 show the parallel and serial transport stream timing diagrams in data-only mode. In data-only mode, 188 bytes of data is transferred from the transport stream interface continuously. PACCLK is always kept high.

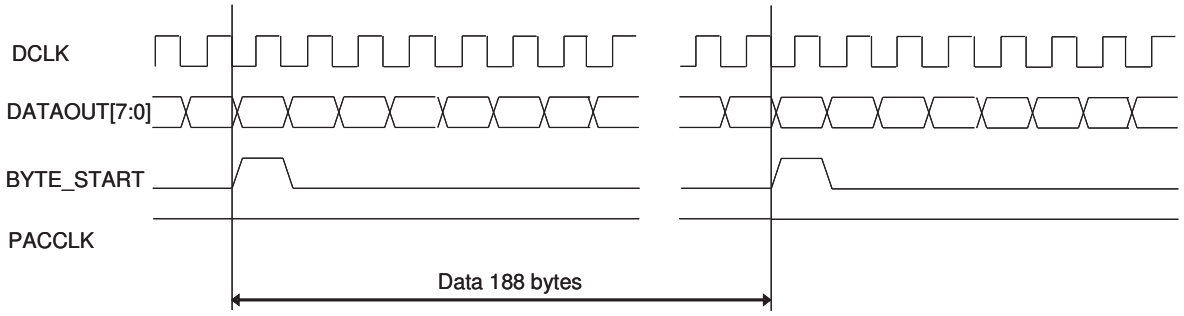


Figure 4-1. Parallel Transport Stream Timing Diagram (Data Only)

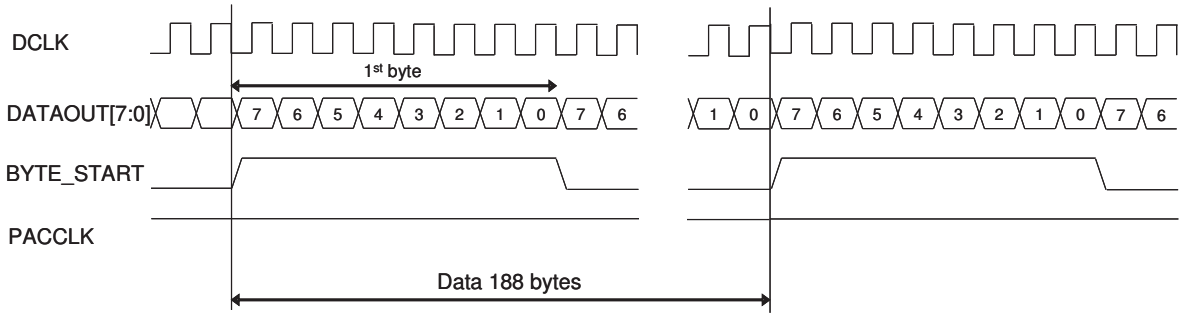


Figure 4-2. Serial Transport Stream Timing Diagram (Data Only)

Figure 4-3 and Figure 4-4 show the parallel and serial transport stream timing diagrams in data and redundancy mode. In data and redundancy mode, 188 bytes of data is transferred from the transport stream interface with redundant data bytes. PACCLK only becomes high when the data is valid. Redundancy data is 20 bytes in the ATSC standard and 16 bytes in ITU-T J.83 Annex B.

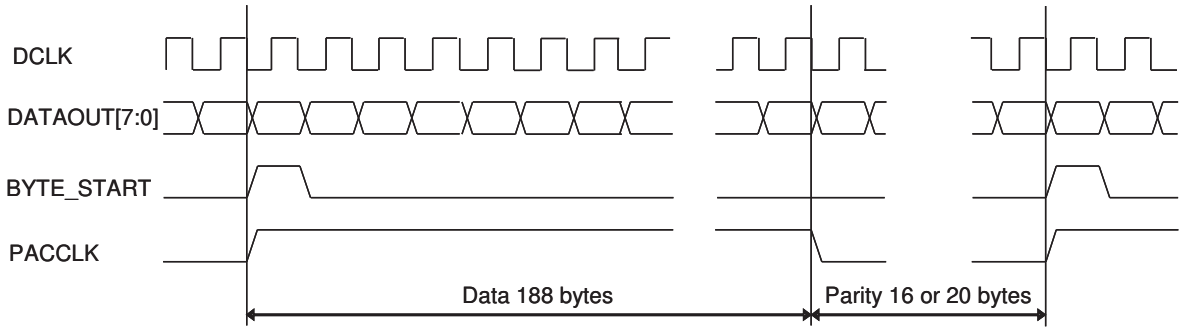


Figure 4-3. Parallel Transport Stream Timing Diagram (Data + Redundancy)

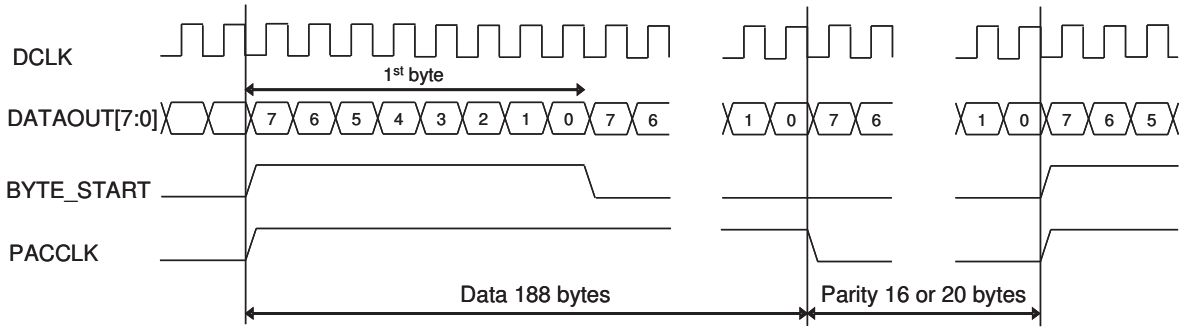


Figure 4-4. Serial Transport Stream Timing Diagram (Data + Redundancy)

Table 4-2 shows the transport stream clock frequency in each mode.

Table 4-2. MPEG-2 Transport Stream Output Clock Frequency

MODE	BIT RATE (Mbps)	DATA ONLY		DATA + REDUNDANCY	
		SERIAL CLOCK (MHz)	PARALLEL CLOCK (MHz)	SERIAL CLOCK (MHz)	PARALLEL CLOCK (MHz)
8VSB	19.39266	19.39266	2.42408	21.45571	2.68196
64QAM	26.97035	26.97035	3.37129	29.26570	3.65821
256QAM	38.81070	38.81070	4.85133	42.11374	5.26422

4.5 I^2C Host Interface

Communication with the TVP9900 receiver is via an I^2C host interface. The I^2C standard consists of two signals, the serial input/output data (I2CSDA) line and the input/output clock line (I2CSCL), which carry information between the devices connected to the bus. A 1-bit control signal (I2CA0) is used for slave address selection. Although an I^2C system can be multi-mastered, the TVP9900 can function as a slave device only. Since I2CSDA and I2CSCL are kept open-drain at logic high output level or when the bus is not driven, the user should connect I2CSDA and I2CSCL to IOVDD_3.3 via a pullup resistor on the board. At the trailing edge of reset, the status of the I2CA0 line is sampled to determine the device address used. Table 4-3 summarizes the terminal functions of the I^2C-mode host interface. Table 4-4 and Table 4-5 show the device address selection options.

Table 4-3. I²C Terminal Description

SIGNAL	TYPE	DESCRIPTION
I2CA0	I	Slave address selection
I2CSCL	I/O (open drain)	Input/output clock line
I2CSDA	I/O (open drain)	Input/output data line

Table 4-4. I²C Host Interface Device Write Addresses

I2CA0	WRITE ADDRESS
0	B8h
1	BAh

Data transfer rate on the bus is up to 400 kbits/s. The number of interfaces connected to the bus is dependent on the bus capacitance limit of 400 pF. The data on the SDA line must be stable during the high period of the SCL, except for start and stop conditions. The high or low state of the data line can only change with the clock signal on the SCL line being low. A high-to-low transition on the SDA line while the SCL is high indicates an I²C start condition. A low-to-high transition on the SDA line while the SCL is high indicates an I²C stop condition.

Every byte placed on the SDA must be eight bits long. The number of bytes that can be transferred is unrestricted. Each byte must be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the I²C master.

4.5.1 I²C Write Operation

Data transfers occur utilizing the following illustrated formats. An I²C master initiates a write operation to the TVP9900 receiver by generating a start condition (S), followed by the TVP9900 I²C address (as shown below), in MSB first bit order, followed by a 0 to indicate a write cycle. After receiving an acknowledge from the TVP9900 receiver, the master presents the subaddress of the register or the first of a block of registers it wants to write, followed by one or more bytes of data, MSB first. The TVP9900 receiver acknowledges each byte after completion of each transfer. The I²C master terminates the write operation by generating a stop condition (P).

Step 1	**0**
I²C Start (master)	S

Step 2	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C General address (master)	1	0	1	1	1	0	X	0

Step 3	**9**
I²C Acknowledge (slave)	A

Step 4	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C Write register address (master)	Addr	Addr	Addr	Addr	Addr	Addr	Addr	Addr

Step 5	**9**
I²C Acknowledge (slave)	A

Step 6	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C Write data (master)	Data	Data	Data	Data	Data	Data	Data	Data

Step 7(1)	**9**
I²C Acknowledge (slave)	A

Step 8	**0**
I²C Stop (master)	P

(1) Repeat steps 6 and 7 until all data have been written.

4.5.2 I²C Read Operation

The read operation consists of two phases. The first phase is the address phase. In this phase, an I²C master initiates a write operation to the TVP9900 receiver by generating a start condition (S) followed by the TVP9900 I²C address, in MSB first bit order, followed by a 0 to indicate a write cycle. After receiving acknowledges from the TVP9900 receiver, the master presents the subaddress of the register or the first of a block of registers it wants to read. After the cycle is acknowledged, the master terminates the cycle immediately by generating a stop condition (P).

Table 4-5. I²C Host Interface Device Read Address

I2CA0	READ ADDRESS
0	B8h
1	BAh

The second phase is the data phase. In this phase, an I²C master initiates a read operation to the TVP9900 receiver by generating a start condition, followed by the TVP9900 I²C address (as shown below for a read operation), in MSB-first bit order, followed by a 1 to indicate a read cycle. After an acknowledge from the TVP9900 receiver, the I²C master receives one or more bytes of data from the TVP9900 receiver. The I²C master acknowledges the transfer at the end of each byte. After the last data byte desired has been transferred from the TVP9900 receiver to the master, the master generates a not acknowledge, followed by a stop.

Read Phase 1

Step 1	**0**
I²C Start (master)	S

Step 2	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C General address (master)	1	0	1	1	1	0	X	0

Step 3	**9**
I²C Acknowledge (slave)	A

Step 4	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C Write register address (master)	Addr	Addr	Addr	Addr	Addr	Addr	Addr	Addr

Step 5	**9**
I²C Acknowledge (slave)	A

Step 6	**0**
I²C Stop (master)	P

Read Phase 2

Step 7	**0**
I²C Start (master)	S

Step 8	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C General address (master)	1	0	1	1	1	0	X	0

Step 9	**9**
I²C Acknowledge (slave)	A

Step 10	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C Read data (slave)	Data	Data	Data	Data	Data	Data	Data	Data

Step 11 (1)	**9**
I²C Not Acknowledge (master)	A

Step 12	**0**
I²C Stop (master)	P

(1) Repeat steps 10 and 11 for all bytes read. Master does not acknowledge the last read data received.

4.6 Tuner Control Interface

The TVP9900 has an I^{2}C-compatible two-wire serial interface that can be used by the host processor for tuner control. This dedicated tuner interface can be used by the host processor to transfer data to/from the tuner in order to isolate the tuner from the main system I^{2}C bus. As a result, noise coupling to the tuner from host processor I^{2}C bus transfers should be minimized.

The TVP9900 tuner control interface operates as an I^{2}C bus master and supports both 100-kbps and 400-kbps data transfer rates. The mode and transfer rate is set in the Tuner Control Interface – Control and Status Register (5Eh), bit 0. The device does not support a multi-master bus environment (bus arbitration is not supported).

To transfer data to/from the tuner, the host processor first writes the transaction to a set of registers in the TVP9900 via the host processor I^{2}C interface. Then the TVP9900 internal MCU transfers the data to/from the tuner via the tuner control interface.

TUNSCL and TUNSDA must be pulled up to the 3.3-V supply (IOVDD) and not to a 5-V supply.

Figure 4-5 shows the block diagram of the tuner control interface system.

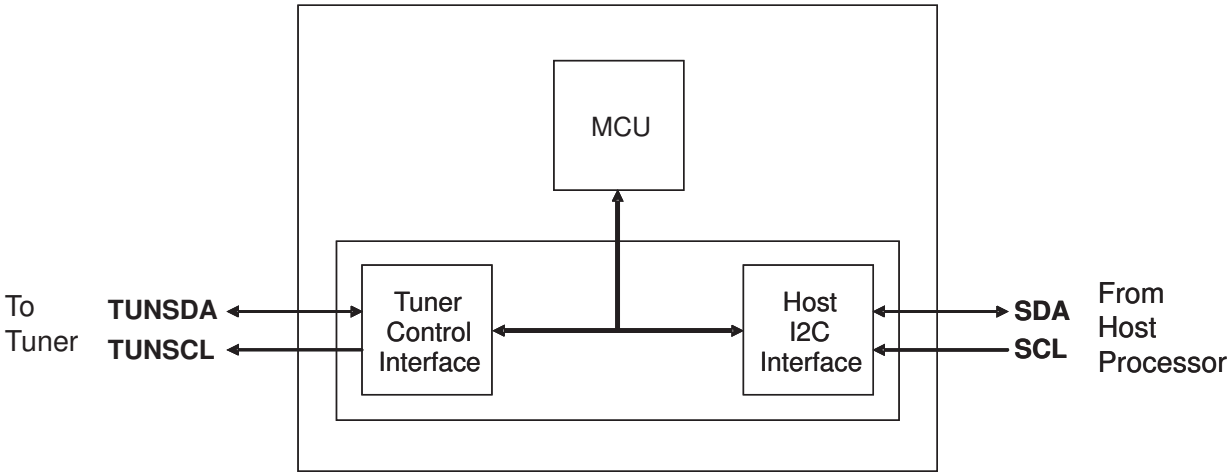


Figure 4-5. Tuner Control Interface System

Table 4-6 lists the I^{2}C registers and their functions used to control the tuner interface.

Table 4-6. Tuner Control Interface Registers

REGISTER	FUNCTION
55h	Tuner I^{2}C slave address and R/W control
56h to 5Dh	Data registers 1 through 8
5Eh	Byte Count, Transaction Start, and I^{2}C Mode
F9, FB, FD, FFh	Software Interrupt Raw Status, Status, Mask, and Clear – Transaction Error and Done Status

When the TVP9900 tuner I^{2}C interface is used, rather than controlling the tuner over the host processor I^{2}C bus interface, two status bits are provided in the TVP9900 to indicate a transaction error or the completion of a successful transaction. The TCIERROR bit in the TVP9900 Software Interrupt Status Register (FBh) gets set as a result of a transaction error. The TCIDONE bit in the same register gets set at the end of a normal transaction; it does not get set for an abnormal transaction. The TVP9900 can be configured so that setting the TCIERROR or TCODONE status bits can assert the INTREQ output of the TVP9900; this requires the mask bits to be configured correctly in the TVP9900 Software Interrupt Mask Register (FDh).

If the host INTREQ is not used, the TCIDONE and TCIERROR interrupts should be masked and the host should poll the TCIDONE status bit to determine when the transaction is complete, and the host should poll the TCIERROR status bit to determine when an error has occurred.

Tuner data transfers occur utilizing the following illustrated formats.

4.6.1 Tuner Write Operation

The following steps are required to initiate a write operation to the tuner. The host processor first writes the required transaction data to a set of registers in the TVP9900 via the host processor I^2C interface.

Step 1	
Register 55h	Set tuner I^2C slave address (bits 7:1) and read/write control (bit 0 = 0)
Step 2	
Registers 56h to 5Dh	Write data bytes to be sent to tuner; 56h is first byte sent
Step 3	
Register 5Eh	Set byte count (bits 7:5) and I^2C mode (bit 0) Set bit 2 to 1 to start transaction to tuner
Step 4	
Register FBh	Check state of bits 1:0 or INTREQ pin to verify successful transaction

After the transaction has been initiated, the TVP9900 internal MCU transfers the data to the tuner via the tuner control interface. Acting as the I^2C master, the TVP9900 initiates a write operation to the tuner (as shown below), by generating a start condition, followed by the tuner I^2C address, in MSB-first bit order, followed by a 0 to indicate a write cycle. After receiving an acknowledge from the tuner, the TVP9900 presents the subaddress of the register, if needed, followed by one or more bytes of data, MSB first. The tuner acknowledges each byte after completion of each transfer. The TVP9900 terminates the write operation by generating a stop condition.

TVP9900/Tuner Write Operation

SDA	Start	Device Address	W	Ack	Base Address	Ack	Data 1	Ack	...	Data N	Ack	Stop

4.6.2 Tuner Read Operation

The following steps are required to initiate a read operation from the tuner. The host processor first writes the required transaction data to a set of registers in the TVP9900 via the host processor I^2C interface, then reads the data bytes received from the tuner stored in TVP9900 registers.

Step 1	
Register 55h	Set tuner I^2C slave address (bits 7:1) and read/write control (bit 0 = 1)
Step 2	
Register 5Eh	Set byte count (bits 7:5) and I^2C mode (bit 0) Set bit 2 to 1 to start transaction to tuner
Step 3	
Register FBh	Check state of bits 1:0 or INTREQ pin to verify successful transaction
Step 4	
Registers 56h to 5Dh	Read data bytes from tuner; 56h is first byte received

After the transaction has been initiated, the TVP9900 internal MCU transfers the data from the tuner via the tuner control interface. The read operation consists of two phases, as shown in the following sections. The first phase is the address phase. In this phase, the TVP9900 I^2C master initiates a write operation to the tuner by generating a start condition, followed by the tuner I^2C address, in MSB-first bit order, followed by a 0 to indicate a write cycle. After receiving an acknowledge from the tuner, the TVP9900 presents the subaddress of the register, if needed. After the cycle is acknowledged, the master terminates the cycle immediately by generating a stop condition.

The second phase is the data phase. In this phase, the TVP9900 I^2C master initiates a read operation to the tuner by generating a start condition, followed by the tuner I^2C address, in MSB-first bit order, followed by a 1 to indicate a read cycle. After an acknowledge from the tuner, the TVP9900 receives one or more bytes of data from the tuner. The TVP9900 acknowledges the transfer at the end of each byte. After the last data byte desired has been transferred from the tuner to the TVP9900, the TVP9900 generates a not acknowledge, followed by a stop.

TVP9900/Tuner Set Start Address, Then Read Operation

SDA	Start	Device Address	W	Ack	Base Address	Ack	Stop			
SDA	Start	Device Address	R	Ack	Data 1	Ack	...	Data N	Ack	Stop

4.7 Antenna Control Interface

The TVP9900 has an antenna control interface compliant with EIA/CEA-909. The TVP9900 receives the antenna parameters from the host processor via I^2C, and sends a modulated PWM signal to the antenna. The antenna parameters include antenna direction, antenna polarization, preamplifier gain and channel number. This interface can be used to automatically optimize the signal by adjusting the antenna configuration for the best possible reception.

Figure 4-6 shows the block diagram of the antenna control interface system.

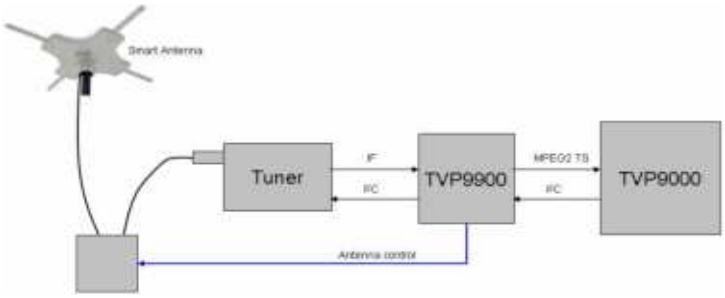


Figure 4-6. Antenna Control Interface System

Table 4-7 lists the I^2C registers and their functions used with the antenna control interface.

Table 4-7. Antenna Control Interface Registers

REGISTER	FUNCTION
4Fh	GPIO Alternate Function Select
5Fh	Antenna Control Interface – Control and Status
60h to 61h	Antenna Control Interface – Transmit Data
62h to 63h	Antenna Control Interface – Receive Data
F9, FB, FD, FFh	Software Interrupt Raw Status, Status, Mask, and Clear – Transaction Complete and Timeout Status

The TVP9900 supports two modes of antenna control: Mode A for basic control (transmit transaction only) and Mode B for advanced control (transmit and receive transactions) as defined in the CEA-909 standard. For Mode B operation, the TVP9900 supports both 1-pin and 2-pin operation. In 1-pin mode, the data input and output are muxed into one pin (pin 29), and in 2-pin mode the input and output use separate pins (pin 29 for output, pin 72 for input.) The desired pin mode is selected by setting register 5Fh, bit 0.

Table 4-8 lists the TVP9900 pins and their functions used with the antenna control interface.

Table 4-8. Antenna Control Interface Pins

PIN	NAME	FUNCTION
29	ANTCNTLIO	Antenna control interface input/output
71	GPIO1	Signal direction of pin 29 in 1-pin mode
72	GPIO0/ANTCNTLIN	Antenna control input for 2-pin mode

The GPIO1 pin provides dedicated smart antenna control support, and in 1-pin mode this pin outputs the direction of the signal on pin 29:

GPIO1 = 0 indicates signal input from antenna to TVP9900 pin 29

GPIO1 = 1 indicates signal output from TVP9900 pin 29 to antenna

Four status bit are provided in the TVP9900 to indicate the completion of a successful receive or transmit transaction, or if a transaction timeout has occurred.

- The ACIRXCT bit in the TVP9900 Software Interrupt Status Register (FBh) gets set when the receive transaction from a Mode B antenna is complete.
- The ACITXCT bit in the same register gets set when the transmit transaction to the antenna is complete.
- The ACIRXTO bit in the same register gets set when an interface timeout has occurred due to no reply form the antenna following a transmit transaction, or an incomplete receive transaction from the antenna.
- The RXERR bit in the Antenna Control Interface Control and Status Register (5Fh) is set if an incomplete receive transaction occurs.

The TVP9900 can be configured so that setting the ACIRXCT, ACITXCT, or ACIRXTO status bits can assert the INTREQ output of the TVP9900; this requires the mask bits to be configured correctly in the TVP9900 Software Interrupt Mask Register (FDh).

If the host INTREQ is not used, the ACIRXCT, ACITXCT, and ACIRXTO interrupts should be masked and the host should poll the ACIRXCT and ACITXCT status bits to determine when the transactions are complete, and the host should poll the ACIRXTO and RXERR status bits to determine when a receive timeout or error has occurred.

Antenna control data transfers occur utilizing the following illustrated formats.

4.7.1 Antenna Interrogation/Initialization

The following steps are required to interrogate and initialize a smart antenna. The host processor first writes the required transaction data to a set of registers in the TVP9900 via the host processor I^2C interface.

1. The system host processor transmits to the antenna a basic Mode A 14-bit serial data stream with an RF channel number of zero.
2. The system tri-states the line and waits 100 ms for a reply message from the antenna controller. If no response is received, a timeout occurs, and the antenna controller is assumed to be a Mode A system. The system uses only transmit operations for antenna control.
3. If the antenna responds with a 10-bit program identifier, the antenna controller is assumed to be a Mode B system, and the system uses transmit and receive operations for antenna control.

This initialization is optional. If the system has only Mode A enabled, with no Mode B support, this initialization step may be omitted.

4.7.2 Transmit Data to Antenna Operation

The following steps are required to transmit data to the antenna. The host processor writes the required transaction data to a set of registers in the TVP9900, via the host processor I^2C interface.

Step 1	
Register 5Fh	Set TXRXSEL (bit 2 = 1) to select a transmit data transaction, and set MODE (bit 4 = 1) to enable auto receive mode
Step 2	
Registers 60h to 61h	Load 14-bit data value to be transmitted to antenna
Step 3	
Register 5Fh	Set TXSTART (bit 3) to 1 to start transmit transaction to tuner
Step 4	
Register FBh	Check state of bit 4 or INTREQ pin to verify successful transaction

4.7.3 Receive Data from Antenna Operation

After an antenna transmit transaction is executed, a Mode B antenna should respond with a 10-bit data value within 100 ms. If the receive data is not received within 100 ms, a receive timeout occurs. The following steps are required to receive data from the antenna. The host processor first writes the required transaction data to a set of registers in the TVP9900, via the host processor I^2C interface, then reads the data bytes received from the antenna stored in TVP9900 registers.

Step 1	
Register 5Fh	Set TXRXSEL (bit 2 = 0) to select a receive data transaction, and set MODE (bit 4 = 1) to enable auto receive mode
Step 2	
Register FBh	Check state of bit 5 or INTREQ pin to verify successful transaction, or wait for timeout interrupt (bit 3) to occur
Step 3	
Registers 62h to 63h	Read 10-bit data value received from antenna
Step 4	
Register 5Fh	Read RXERR value (bit 5)

The RXERR bit is set to 1 to indicate an error occurred when receiving data from a Mode B antenna. If a non-zero data value was received from the antenna and no error occurred, the data is valid and the antenna is a Mode B antenna. If the data value is zero and no error occurred, a receive transaction did not occur and it is assumed that the antenna is a Mode A antenna.

4.8 General-Purpose Input/Output (GPIO)

The TVP9900 has eight GPIO pins, GPIO0–GPIO7. GPIO1 is a dedicated pin for Smart Antenna support. GPIO0, GPIO5, GPIO6, and GPIO7 are shared pins and can be programmed as the following dedicated functions. See register 4Fh description for details about selecting these alternate functions. All pins are configured as inputs at device power-up.

- GPIO0 – Antenna control input
- GPIO5 – Sync output
- GPIO6 – Reserved
- GPIO7 – Interrupt request output

4.9 Clock Circuits

An internal PLL generates all clocks required in the chip. A 25-MHz clock is required to derive the PLL. Most tuner devices have a 4-MHz crystal oscillator that can be output to the demodulator as a clock source. In the TVP9900, a 4-MHz clock input also can be used as the clock source. A 4-MHz clock is input to the TVP9900 receiver on terminal 13 (XTALIN), or a crystal of 25-MHz fundamental resonant frequency may be connected across terminals 13 (XTALIN) and 11 (XTALOUT). Figure 4-7 shows the reference clock configuration of 25-MHz crystal oscillation. NOTE: The oscillator input, XTALIN, is not 3.3-V tolerant and only works at 1.5-V signal levels.

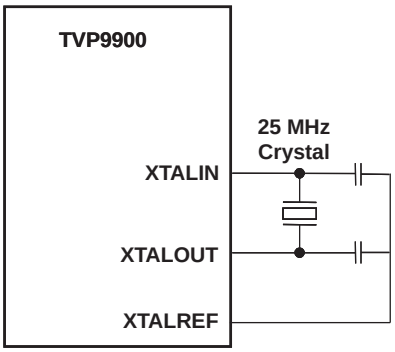


Figure 4-7. 25-MHz Crystal Oscillation

Figure 4-8 shows the reference clock configuration of 4-MHz clock input.

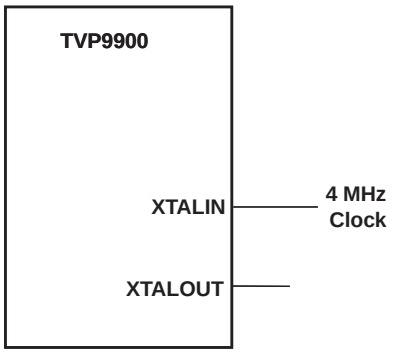


Figure 4-8. 4-MHz Clock Input

4.10 Power-Up Sequence

No specific power-supply sequence is required, as long as all power supplies are ramped to valid operating levels within 500 ms of one another. Output or bidirectional buffers power-up with the output buffers in tri-state mode.

4.11 Reset

The reset signal, RESETZ, is an active-low asynchronous reset that is used to initialize the device at power-up. The RESETZ signal may be low during power-up but must remain active low for a minimum of 1 ms after all power-supply voltages are stable at the recommended operating voltage. Internal circuits synchronize the power-on reset with internal clocks; therefore, the RESETZ signal must remain active low for a minimum of 1 µs after the crystal oscillator and clocks are stable.

Reset may be asserted any time after power up and stable crystal oscillation and must remain asserted for at least 1 µs. A minimum of 200 µs must be allowed after reset before commencing I^2C operations.

4.12 Power Down

There is no required power-down sequence for the TVP9900.

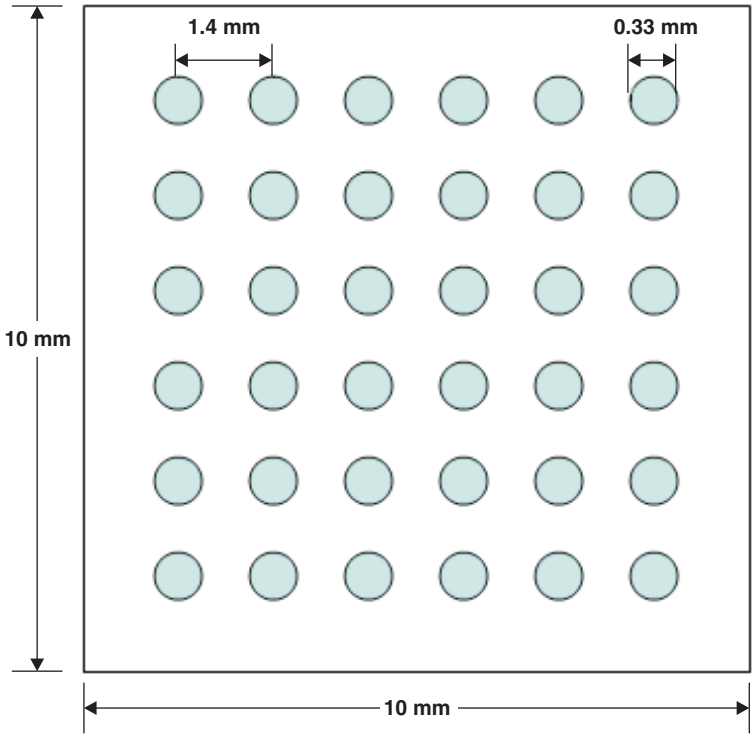
4.13 Power-Supply Voltage Requirements

The digital core uses a 1.5-V power supply. The digital I/O cells use a 3.3-V power supply. Note that the exception is for the oscillator input, XTALIN, which is not 3.3-V tolerant and only works at 1.5-V signal levels. The analog circuitry uses both a 1.5-V and a 3.3-V power supply.

5 High-K PCB Design Recommendations

In order to effectively transfer heat out of the package and to keep the die junction temperature below 105°C, the TVP9900 is packaged in the thermal PowerPAD™ package, which has an exposed metal pad on the bottom of the device. To effectively use this package, the following PCB design requirements must be followed.

- An array of thermal vias should be placed in the board at the placement location of the TVP9900, as shown in Figure 5-1.
- The ideal thermal land size is 10 mm × 10 mm, and the ideal thermal via pattern is a 6 × 6 array.
- The vias should be connected to the PCB ground plane.
- The exposed metal pad of the TVP9900 should be soldered to these vias.
- The copper trace thickness should be 0.071 mm (2 oz), if possible.



10-mm × 10-mm thermal land size
6 × 6 array of vias
1.4-mm via spacing
0.33-mm via diameter

Figure 5-1. Thermal Land Size and Via Array

Each of these recommendations is important to maximize the heat-sinking characteristics of the PCB. Refer to the Texas Instruments application report, *PowerPAD™ Thermally Enhanced Package* (literature number SLMA002), for more detailed information.

6 Host Processor I²C Register Summary

6.1 Overview

The TVP9900 IC is controlled by a host processor by using a set of control and status registers. Access to these registers by the host processor is via an I²C serial interface. A summary of the I²C host interface registers is given in Table 6-1.

Table 6-1. I²C Host Interface Registers

ADDRESS	REGISTER NAME	DEFAULT	R/W
00h	Receiver Control Register 1 / Soft Reset	20h	R/W
01h	Receiver Control Register 2	11h	R/W
02h	Reserved		
03h	VSB Control Register	02h	R/W
04h	AGC Control Register	07h	R/W
05h–1Ah	Reserved		
1Bh	VSB FEC Time Counter Control Register 1	BCh	R/W
1Ch	VSB FEC Time Counter Control Register 2	64h	R/W
1Dh	VSB FEC Time Counter Control Register 3	00h	R/W
1Eh	QAM FEC Time Counter Control Register 1	00h	R/W
1Fh	QAM FEC Time Counter Control Register 2	08h	R/W
20h	QAM FEC Time Counter Control Register 3	00h	R/W
21h	VSB FEC Segment Error Count Threshold 1	05h	R/W
22h	VSB FEC Segment Error Count Threshold 2	00h	R/W
23h–24h	Reserved		
25h	Update Status Control Register	N/A	R/W
26h	Receiver Status Register	N/A	R
27h	AGC Status Register 1 – AGC LF Accumulator Output (7:0)	N/A	R
28h	AGC Status Register 2 – AGC LF Accumulator Output (15:8)	N/A	R
29h	AGC Status Register 3 – AGC LF Accumulator Output (19:16)	N/A	R
2Ah	NTSC Rejection Filter Status Register	N/A	R
2Bh	Timing Recovery Status Register 1 – DTR LF Accumulator Output (7:0)	N/A	R
2Ch	Timing Recovery Status Register 2 – DTR LF Accumulator Output (15:8)	N/A	R
2Dh	Timing Recovery Status Register 3 – DTR LF Accumulator Output (23:16)	N/A	R
2Eh	Timing Recovery Status Register 4 – DTR LF Accumulator Output (31:24)	N/A	R
2Fh	Timing Recovery Status Register 5 – DTR LF Accumulator Output (39:32)	N/A	R
30h	Timing Recovery Status Register 6 – DTR LF Accumulator Output (43:40)	N/A	R
31h–33h	Reserved		
34h	Pilot Tracking Status Register 1 – DPT LF Accumulator Output (7:0)	N/A	R
35h	Pilot Tracking Status Register 2 – DPT LF Accumulator Output (15:8)	N/A	R
36h	Pilot Tracking Status Register 3 – DPT LF Accumulator Output (19:16)	N/A	R
37h–38h	Reserved		
39h	Carrier Recovery Status Register 1 – DCL Average Error (7:0)	N/A	R
3Ah	Carrier Recovery Status Register 2 – DCL Average Error (15:8)	N/A	R
3Bh	Carrier Recovery Status Register 3 – DCL Average Error (19:16)	N/A	R
3Ch	Carrier Recovery Status Register 4 – QAM DCL LF Accumulator Output (7:0)	N/A	R
3Dh	Carrier Recovery Status Register 5 – QAM DCL LF Accumulator Output (15:8)	N/A	R
3Eh	Carrier Recovery Status Register 6 – QAM DCL LF Accumulator Output (19:16)	N/A	R
3Fh–40h	Reserved		
41h	Forward Error Correction Status Register 1	N/A	R

Table 6-1. I²C Host Interface Registers (continued)

ADDRESS	REGISTER NAME	DEFAULT	R/W
42h	Reserved		
43h	Forward Error Correction Status Register 2 – FEC Segment Error Count (7:0)	N/A	R
44h	Forward Error Correction Status Register 3 – FEC Segment Error Count (11:8)	N/A	R
45h	Forward Error Correction Status Register 4	N/A	R
46h–4Eh	Reserved		
4Fh	GPIO Alternate Function Select Register	00h	R/W
50h	GPIO Output Data Register	00h	R/W
51h	GPIO Output Enable Register	FFh	R/W
52h	GPIO Input Data Register	00h	R
53h	MPEG Interface Output Enable Register 1	00h	R/W
54h	MPEG Interface Output Enable Register 2	00h	R/W
55h	Tuner Control Interface – I²C Slave Device Address	00h	R/W
56h	Tuner Control Interface – Data Register 1	00h	R/W
57h	Tuner Control Interface – Data Register 2	00h	R/W
58h	Tuner Control Interface – Data Register 3	00h	R/W
59h	Tuner Control Interface – Data Register 4	00h	R/W
5Ah	Tuner Control Interface – Data Register 5	00h	R/W
5Bh	Tuner Control Interface – Data Register 6	00h	R/W
5Ch	Tuner Control Interface – Data Register 7	00h	R/W
5Dh	Tuner Control Interface – Data Register 8	00h	R/W
5Eh	Tuner Control Interface – Control and Status Register	00h	R/W
5Fh	Antenna Control Interface – Control and Status Register	00h	R/W
60h	Antenna Control Interface – Transmit Data Register 1	00h	R/W
61h	Antenna Control Interface – Transmit Data Register 2	00h	R/W
62h	Antenna Control Interface – Receive Data Register 1	00h	R/W
63h	Antenna Control Interface – Receive Data Register 2	00h	R/W
64h–6Fh	Reserved		
70h	Firmware ID – ROM Version	02h	R
71h	Firmware ID – RAM Major Version	00h	R
72h	Firmware ID – RAM Minor Version	00h	R
73h–7Fh	Reserved		
80h	Device ID LSB	00h	R
81h	Device ID MSB	99h	R
82h–EDh	Reserved		
EEh	Miscellaneous Control Register	00h	R/W
EFh–F8h	Reserved		
F9h	Software Interrupt Raw Status Register	00h	R
FAh	Reserved		
FBh	Software Interrupt Status Register	00h	R
FCh	Reserved		
FDh	Software Interrupt Mask Register	00h	R/W
FEh	Reserved		
FFh	Software Interrupt Clear Register	00h	W

6.2 I²C Register Definitions

6.2.1 Receiver Control Register 1 / Soft Reset

Any write to this register causes a soft reset, which puts the receiver back into signal acquisition, and enables any changes made to registers 01h to 22h. Recommend performing soft reset after channel change.

Address	00h							
Default	20h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	RDNSEL	MPEGSEL	DCLKPS	BYSTPS	DERRPS	PCLKPS	DMDSEL	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Default	0	0	1	0	0	0	00	

BIT	MNEMONIC	NAME	DESCRIPTION
7	RDNSEL	MPEG interface redundancy select	The MPEG interface redundancy select is used by the host processor to select the data with redundancy output mode. 0 = No redundancy (data only mode) selected (default) 1 = Data with redundancy mode selected
6	MPEGSEL	MPEG interface serial output select	The MPEG interface serial output select is used by the host processor to select the serial versus parallel output mode for the MPEG interface. 0 = 8-bit parallel data output mode selected (default) 1 = Serial data output mode selected
5	DCLKPS	MPEG interface data clock output polarity select	The MPEG interface data clock output polarity select is used by the host processor to select the polarity of the DCLK output pin. 0 = All MPEG interface output signals transition with respect to the rising edge of DCLK 1 = All MPEG interface output signals transition with respect to the falling edge of DCLK (default)
4	BYSTPS	MPEG interface byte start output polarity select	The MPEG interface byte start output polarity select is used by the host processor to select the polarity of the BYTESTART output pin. 0 = BYTESTART is active high (default) 1 = BYTESTART is active low
3	DERRPS	MPEG interface data error output polarity select	The MPEG interface data error output polarity select is used by the host processor to select the polarity of the DERROR output pin. 0 = DERROR is active high (default) 1 = DERROR is active low
2	PCLKPS	MPEG interface packet clock output polarity select	The MPEG interface packet clock output polarity select is used by the host processor to select the polarity of the PACCLK output pin. 0 = PACCLK is active high (default) 1 = PACCLK is active low
1:0	DMDSEL	VSB or QAM demodulation mode select	The VSB or QAM mode select bits are used by the host processor to select the demodulation type to be used by the TVP9900 receiver device. 00 = 8 VSB mode selected (default) 01 = Reserved 10 = 64 QAM mode selected 11 = 256 QAM mode selected

6.2.2 Receiver Control Register 2

A soft reset is required to enable any changes made to this register. A soft reset is initiated by writing to register 00h.

Address	01h							
Default	11h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	Reserved	Reserved	IQSWAP	Reserved	DNFCTRL		DAFBYP	Reserved
Type	R	R	R	R/W	R/W		R/W	R/W
Default	0	0	0	1	00		0	1

BIT	MNEMONIC	NAME	DESCRIPTION
7:6	—	Reserved	Reserved for future use
5	IQSWAP	IQ swap	Timing recovery spectral shift 0 = Shift spectrum positive frequency (default) 1 = Shift spectrum negative frequency. For QAM mode, this bit swaps I and Q.
4	—	Reserved	Reserved for future use. Always set to 1.
3:2	DNFCTRL	NTSC detection circuit control	NTSC detection circuit control for VSB (always bypassed for QAM) 00 = Use detection circuit (default) 01 = Force bypass of NTSC filter 10 = Force insertion of NTSC filter 11 = Reserved
1	DAFBYP	Adjacent channel filter bypass	Adjacent channel filter bypass for VSB (always bypassed for QAM) 0 = Enable the adjacent channel filter (default) 1 = Bypass the adjacent channel filter
0	—	Reserved	Reserved for future use. Always set to 1.

6.2.3 VSB Control Register

A soft reset is required to enable any changes made to this register. A soft reset is initiated by writing to register 00h.

Address	03h							
Default	02h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	Reserved	Reserved	Reserved	RSTDIS	Reserved	Reserved	Reserved	Reserved
Type	R	R	R	R/W	R	R	R	R
Default	0	0	0	0	0	0	1	0

BIT	MNEMONIC	NAME	DESCRIPTION
7:5	—	Reserved	Reserved for future use
4	RSTDIS	Auto restart disable	Disable VSB automatic soft reset mode. 0 = Firmware automatically restarts acquisition when there are too many segment errors (default) 1 = Disable automatic restarts
3:0	—	Reserved	Reserved for future use. Always set to 2h.

6.2.4 AGC Control Register

A soft reset is required to enable any changes made to this register. A soft reset is initiated by writing to register 00h.

Address	04h							
Default	07h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	Reserved	Reserved	Reserved	Reserved	Reserved	DAGINV	Reserved	
Type	R	R	R	R	R	R/W	R	
Default	0	0	0	0	0	1	11	

BIT	MNEMONIC	NAME	DESCRIPTION
7:3	—	Reserved	Reserved for future use
2	DAGINV	AGC output signal invert select	The automatic gain control output signal (AGCOUT) invert select bit is used by the host processor to change the polarity of the output signal. 0 = AGCOUT is non-inverted 1 = AGCOUT is inverted (default)
1:0	—	Reserved	Reserved for future use. Always set to 3h.

6.2.5 VSB FEC Time Counter Register 1

A soft reset is required to enable any changes made to this register. A soft reset is initiated by writing to register 00h.

Address	1Bh							
Default	BCh							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	FCSFRSTIMECOUNT1							
Type	R/W							
Default	0xBC							

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	FCSFRSTIMECOUNT1	VSB update interval count, bits (7:0)	Update interval count value (RS blocks) for segment error count; bits (7:0) of 24-bit value. The remaining bits are stored in registers 1Ch and 1Dh.

6.2.6 VSB FEC Time Counter Register 2

A soft reset is required to enable any changes made to this register. A soft reset is initiated by writing to register 00h.

Address	1Ch							
Default	64h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	FCSFRSTIMECOUNT2							
Type	R/W							
Default	0x64							

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	FCSFRSTIMECOUNT2	VSB update interval count, bits (15:8)	Update interval count value (RS blocks) for segment error count; bits (15:8) of 24-bit value

6.2.7 VSB FEC Time Counter Register 3

A soft reset is required to enable any changes made to this register. A soft reset is initiated by writing to register 00h.

Address	1Dh							
Default	00h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	FCSFRSTIMECOUNT3							
Type	R/W							
Default	0x00							

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	FCSFRSTIMECOUNT3	VSB update interval count, bits (23:16)	Update interval count value (RS blocks) for segment error count; bits (23:16) of 24-bit value

6.2.8 QAM FEC Time Counter Register 1

A soft reset is required to enable any changes made to this register. A soft reset is initiated by writing to register 00h.

Address	1Eh							
Default	00h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	JCSJRSTIMECOUNT1							
Type	R/W							
Default	0x08							

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	JCSJRSTIMECOUNT1	QAM update interval count, bits (7:0)	Update interval count value (RS blocks) for segment error count; bits (7:0) of 24-bit value. The remaining bits are stored in registers 1Fh and 20h.

6.2.9 QAM FEC Time Counter Register 2

A soft reset is required to enable any changes made to this register. A soft reset is initiated by writing to register 00h.

Address	1Fh							
Default	08h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	JCSJRSTIMECOUNT2							
Type	R/W							
Default	0x08							

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	JCSJRSTIMECOUNT2	QAM update interval count, bits (15:8)	Update interval count value (RS blocks) for segment error count; bits (15:8) of 24-bit value

6.2.10 QAM FEC Time Counter Register 3

A soft reset is required to enable any changes made to this register. A soft reset is initiated by writing to register 00h.

Address	20h							
Default	00h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	JCSJRSTIMECOUNT3							
Type	R/W							
Default	0x00							

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	JCSJRSTIMECOUNT3	QAM update interval count, bits (23:16)	Update interval count value (RS blocks) for segment error count; bits (23:16) of 24-bit value

6.2.11 VSB FEC Segment Error Count Threshold Register 1

A soft reset is required to enable any changes made to this register. A soft reset is initiated by writing to register 00h.

Address	21h							
Default	05h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	UNCORRINT1							
Type	R/W							
Default	0x05							

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	UNCORRINT1	Segment error count threshold, bits (7:0)	Segment error count threshold; bits (7:0) of a 12-bit value. The remaining bits are stored in register 22h.

6.2.12 VSB FEC Segment Error Count Threshold Register 2

A soft reset is required to enable any changes made to this register. A soft reset is initiated by writing to register 00h.

Address	22h							
Default	00h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	Reserved	Reserved	Reserved	Reserved	UNCORRINT2			
Type	R	R	R	R	R/W			
Default	0	0	0	0	0h			

BIT	MNEMONIC	NAME	DESCRIPTION
7:4	Reserved	Reserved	Reserved for future use
3:0	UNCORRINT2	Segment error count threshold, bits (11:8)	Segment error count threshold; bits (11:8) of a 12-bit value

6.2.13 Update Status Control Register

Address	25h							
Default	00h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	UPDATE
Type	R	R	R	R	R	R	R	R/W
Default	0	0	0	0	0	0	0	0

BIT	MNEMONIC	NAME	DESCRIPTION
7:1	—	Reserved	Reserved for future use
0	UPDATE	Update status registers	Update all status registers (26h to 45h) Host writes a 1 to this bit to update all the status registers. Host should then read this bit until it reads 0; the status update is then complete, and it is safe to read any/all of the status registers.

6.2.14 Receiver Status Register

Address	26h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	Reserved	Reserved		Reserved	ERRCNT	Reserved	SLCERR	FLDSYNC
Type	R	R		R	R	R	R	R
Default	0	N/A		N/A	N/A	N/A	N/A	N/A

BIT	MNEMONIC	NAME	DESCRIPTION
7:4	—	Reserved	Reserved for future use
3	ERRCNT	Reed Solomon segment error count status	Immediate RS segment error count threshold status bit 0 = RS segment error count is below threshold 1 = RS segment error count is above threshold
2	—	Reserved	Reserved for future use
1	SLCERR	Slicer error status	Immediate slicer error threshold status bit 0 = Slicer error is below threshold 1 = Slicer error is above threshold
0	FLDSYNC	Field sync lock status	Immediate field sync lock status bit 0 = Field sync is lost 1 = Field sync is locked (not lost)

6.2.15 AGC Status Register 1

Address	27h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	DAGLFACC1STAT							
Type	R							
Default	N/A							

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	DAGLFACC1STAT	AGC accumulator output, bits (7:0)	Bits (7:0) of the 20-bit AGC loop filter accumulator output. The remaining bits are stored in registers 28h and 29h. These register values are updated by writing a 1 to register 25h, bit 0.

6.2.16 AGC Status Register 2

Address	28h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	DAGLFACC2STAT							
Type	R							
Default	N/A							

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	DAGLFACC2STAT	AGC accumulator output, bits (15:8)	Bits (15:8) of the 20-bit AGC loop filter accumulator output

6.2.17 AGC Status Register 3

Address	29h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	Reserved	Reserved	Reserved	Reserved	DAGLFACC3STAT			
Type	R	R	R	R	R			
Default	0	0	0	0	N/A			

BIT	MNEMONIC	NAME	DESCRIPTION
7:4	—	Reserved	Reserved for future use
3:0	DAGLFACC3STAT	AGC accumulator output, bits (19:16)	Bits (19:16) of the 20-bit AGC loop filter accumulator output

6.2.18 NTSC Rejection Filter Status Register

Address	2Ah							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	DNFDETECT
Type	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	N/A

BIT	MNEMONIC	NAME	DESCRIPTION
7:1	—	Reserved	Reserved for future use
0	DNFDETECT	NTSC detection circuit status	NTSC detection circuit status 0 = NTSC is NOT detected 1 = NTSC is detected

6.2.19 Timing Recovery Status Register 1

Address	2Bh							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	DTRLFACC1STAT							
Type	R							
Default	N/A							

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	DTRLFACC1STAT	Timing recovery accumulator output, bits (7:0)	Bits (7:0) of the 44-bit timing recovery loop filter accumulator output. The remaining bits are stored in registers 2Ch to 30h. These register values are updated by writing a 1 to register 25h, bit 0.

6.2.20 Timing Recovery Status Register 2

Address	2Ch							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	DTRLFACC2STAT							
Type	R							
Default	N/A							

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	DTRLFACC2STAT	Timing recovery accumulator output, bits (15:8)	Bits (15:8) of the 44-bit timing recovery loop filter accumulator output

6.2.21 Timing Recovery Status Register 3

Address	2Dh							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	DTRLFACC3STAT							
Type	R							
Default	N/A							

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	DTRLFACC3STAT	Timing recovery accumulator output, bits (23:16)	Bits (23:16) of the 44-bit timing recovery loop filter accumulator output

6.2.22 Timing Recovery Status Register 4

Address	2Eh							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	DTRLFACC4STAT							
Type	R							
Default	N/A							

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	DTRLFACC4STAT	Timing recovery accumulator output, bits (31:24)	Bits (31:24) of the 44-bit timing recovery loop filter accumulator output

6.2.23 Timing Recovery Status Register 5

Address	2Fh							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	DTRLFACC5STAT							
Type	R							
Default	N/A							

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	DTRLFACC5STAT	Timing recovery accumulator output, bits (39:32)	Bits (39:32) of the 44-bit timing recovery loop filter accumulator output

6.2.24 Timing Recovery Status Register 6

Address	30h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	Reserved	Reserved	Reserved	Reserved	DTRLFACC6STAT			
Type	R	R	R	R	R			
Default	0	0	0	0	N/A			

BIT	MNEMONIC	NAME	DESCRIPTION
7:4	—	Reserved	Reserved for future use
3:0	DTRLFACC6STAT	Timing recovery accumulator output, bits (43:40)	Bits (43:40) of the 44-bit timing recovery loop filter accumulator output

6.2.25 Pilot Tracking Status Register 1

Address	34h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	DPTLFACC1STAT							
Type	R							
Default	N/A							

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	DPTLFACC1STAT	Pilot tracking accumulator output, bits (7:0)	Bits (7:0) of the 20-bit pilot tracking loop filter accumulator output. The remaining bits are stored in registers 35h and 36h. These register values are updated by writing a 1 to register 25h, bit 0.

6.2.26 Pilot Tracking Status Register 2

Address	35h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	DPTLFACC2STAT							
Type	R							
Default	N/A							

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	DPTLFACC2STAT	Pilot tracking accumulator output, bits (15:8)	Bits (15:8) of the 20-bit pilot tracking loop filter accumulator output

6.2.27 Pilot Tracking Status Register 3

Address	36h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	Reserved	Reserved	Reserved	Reserved	DPTLFACC3STAT			
Type	R	R	R	R	R			
Default	0	0	0	0	N/A			

BIT	MNEMONIC	NAME	DESCRIPTION
7:4	—	Reserved	Reserved for future use
3:0	DPTLFACC3STAT	Pilot tracking accumulator output, bits (19:16)	Bits (19:16) of the 20-bit pilot tracking loop filter accumulator output

6.2.28 Carrier Recovery Status Register 1

Address	39h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	DCLAVGERR1STAT							
Type	R							
Default	N/A							

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	DCLAVGERR1STAT	DCL average error, bits (7:0)	Bits (7:0) of the 20-bit DCL average error (derotator SNR) value. The remaining bits are stored in registers 3Ah and 3Bh. These register values are updated by writing a 1 to register 25h, bit 0.

6.2.29 Carrier Recovery Status Register 2

Address	3Ah							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	DCLAVGERR2STAT							
Type	R							
Default	N/A							

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	DCLAVGERR2STAT	DCL average error, bits (15:8)	Bits (15:8) of the 20-bit DCL average error (derotator SNR) value

6.2.30 Carrier Recovery Status Register 3

Address	3Bh							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	Reserved	Reserved	Reserved	Reserved	DCLAVGERR3STAT			
Type	R	R	R	R	R			
Default	0	0	0	0	N/A			

BIT	MNEMONIC	NAME	DESCRIPTION
7:4	—	Reserved	Reserved for future use
3:0	DCLAVGERR3STAT	DCL average error, bits (19:16)	Bits (19:16) of the 20-bit DCL average error (derotator SNR) value

6.2.31 Carrier Recovery Status Register 4

Address	3Ch							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	DCLLFACC1STAT							
Type	R							
Default	N/A							

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	DCLLFACC1STAT	QAM DCL loop filter accumulator output, bits (7:0)	Bits (7:0) of the 20-bit DCL loop filter accumulator output for QAM. The remaining bits are stored in registers 3Dh and 3Eh. These register values are updated by writing a 1 to register 25h, bit 0.

6.2.32 Carrier Recovery Status Register 5

Address	3Dh							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	DCLLFACC2STAT							
Type	R							
Default	N/A							

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	DCLLFACC2STAT	QAM DCL loop filter accumulator output, bits (15:8)	Bits (15:8) of the 20-bit DCL loop filter accumulator output for QAM.

6.2.33 Carrier Recovery Status Register 6

Address	3Eh							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	Reserved	Reserved	Reserved	Reserved	DCLLFACC3STAT			
Type	R	R	R	R	R			
Default	0	0	0	0	N/A			

BIT	MNEMONIC	NAME	DESCRIPTION
7:4	—	Reserved	Reserved for future use
3:0	DCLLFACC3STAT	QAM DCL loop filter accumulator output, bits (19:16)	Bits (19:16) of the 20-bit DCL loop filter accumulator output for QAM.

6.2.34 FEC Status Register 1

6.2.34.1 VSB Mode

Address	41h							
Bit	7	6	5	4	3	2	1	0
Mnemonic	FECSADDR1							
Type	R							
Default	N/A							

BIT	MNEMONIC	NAME	DESCRIPTION
7:2	FECSADDR1	Reserved	Reserved for future use
1:0		FEC synchronizer status	FEC synchronizer status bits 00 = Searching for sync (data not valid) 01 = Locked sync (data valid) 10 = Reserved 11 = Sync lost (data not valid)

6.2.34.2 QAM Mode

Address	41h							
Bit	7	6	5	4	3	2	1	0
Mnemonic	FECSADDR1							
Type	R							
Default	N/A							

BIT	MNEMONIC	NAME	DESCRIPTION
7:6	FECSADDR1	Trellis sync status	Trellis sync status bits 00 = Sync locked, error under threshold 01 = Reserved 10 = Sync locked, error above threshold 11 = Hunting for sync
5:2		Current deinterleaver control work value	Current deinterleaver control work value
1:0		FEC synchronizer status	FEC synchronizer status bits 00 = Searching for sync (data not valid) 01 = Locked sync (data valid) 10 = Reserved 11 = Sync lost (data not valid)

6.2.35 FEC Status Register 2

Address	43h							
Bit	7	6	5	4	3	2	1	0
Mnemonic	FECSADDR2							
Type	R							
Default	N/A							

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	FECSADDR2	FEC segment error count, bits (7:0)	Bits (7:0) of the 12-bit FEC segment error count value. Bits (11:8) are stored in register 44h, bits (7:4). These register values are updated by writing a 1 to register 25h, bit 0.

6.2.36 FEC Status Register 3

Address	44h							
Bit	7	6	5	4	3	2	1	0
Mnemonic	FECSADDR3							
Type	R							
Default	N/A							

BIT	MNEMONIC	NAME	DESCRIPTION
7:4	FECSADDR3	FEC segment error count, bits (11:8)	Bits (11:8) of the 12-bit FEC segment error count value
3:0		Reserved	Reserved for future use

6.2.37 FEC Status Register 4

6.2.37.1 VSB Mode

Address	45h							
Bit	7	6	5	4	3	2	1	0
Mnemonic	FECSADDR4							
Type	R							
Default	N/A							

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	FECSADDR4	Reserved	Reserved for future use

6.2.37.2 QAM Mode

Address	45h							
Bit	7	6	5	4	3	2	1	0
Mnemonic	FECSADDR4							
Type	R							
Default	N/A							

BIT	MNEMONIC	NAME	DESCRIPTION
7:5	FECSADDR4	Reserved	Reserved for future use
4		Deframer synchronization	Deframer synchronization 0 = Sync not locked 1 = Sync locked
3:0		Frame error maximum	Maximum number of frame errors encountered

6.2.38 GPIO Alternate Function Select Register

Address	4Fh							
Default	00h							
Bit	7	6	5	4	3	2	1	0
Mnemonic	GPIO7FS	GPIO6FS	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Type	R/W	R/W	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

BIT	MNEMONIC	NAME	DESCRIPTION
7	GPIO7FS	GPIO bit 7 function select	The GPIO bit 7 function select bit is used by the host processor to select the alternate function of the GPIO7 device pin. 0 = Configures the GPIO7 pin as general-purpose I/O bit 7 (default). 1 = Configures the GPIO7 pin as the host processor INTREQ output.
6	GPIO6FS	GPIO bit 6 and GPIO bit 5 function select	The GPIO bit 6 and GPIO bit 5 function select bit is used by the host processor to select the alternate function for both the GPIO6 and GPIO5 device pins. 0 = Configures the GPIO6 pin as general-purpose I/O bit 6 and GPIO5 pin as general-purpose I/O bit 5 (default). 1 = Configures the GPIO5 pin as the SYNCOUT output. GPIO6 is reserved.
5:2	—	Reserved	Reserved for future use
1	—	Reserved	**NOTE:** The GPIO1 pin is dedicated to Smart Antenna support. This pin outputs the direction of the signal on pin 29 in Smart Antenna 1-pin mode (see register 5Fh, bit 0). If GPIO1 = 0, signal input from antenna to TVP9900 pin 29 If GPIO1 = 1, signal output from TVP9900 pin 29 to antenna
0	—	Reserved	**NOTE:** The GPIO0 pin has an alternate function, which is the Antenna Control Interface input (ANTCNTLIN) when 2-pin mode is selected for this interface. See the Antenna Control Interface Control and Status Register (5Fh), bit 0 (pin mode select), for information on how to select this alternate function.

6.2.39 GPIO Output Data Register

Address	50h							
Default	00h							
Bit	7	6	5	4	3	2	1	0
Mnemonic	GPDO7	GPDO6	GPDO5	GPDO4	GPDO3	GPDO2	Reserved	GPDO0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

BIT	MNEMONIC	NAME	DESCRIPTION
7	GPDO7	General-purpose data output bit 7	General-purpose data output bit 7 is used by the host processor to set the data value on the GPIO7 device pin.
6	GPDO6	General-purpose data output bit 6	General-purpose data output bit 6 is used by the host processor to set the data value on the GPIO6 device pin.
5	GPDO5	General-purpose data output bit 5	General-purpose data output bit 5 is used by the host processor to set the data value on the GPIO5 device pin.
4	GPDO4	General-purpose data output bit 4	General-purpose data output bit 4 is used by the host processor to set the data value on the GPIO4 device pin.
3	GPDO3	General-purpose data output bit 3	General-purpose data output bit 3 is used by the host processor to set the data value on the GPIO3 device pin.
2	GPDO2	General-purpose data output bit 2	General-purpose data output bit 2 is used by the host processor to set the data value on the GPIO2 device pin.
1	—	Reserved	Reserved for future use
0	GPDO0	General-purpose data output bit 0	General-purpose data output bit 0 is used by the host processor to set the data value on the GPIO0 device pin.

6.2.40 GPIO Output Enable Register

Address	51h							
Default	FFh							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	GPIO7OE	GPIO6OE	GPIO5OE	GPIO4OE	GPIO3OE	GPIO2OE	Reserved	GPIO0OE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1

BIT	MNEMONIC	NAME	DESCRIPTION
7	GPIO7OE	General-purpose I/O bit 7 output enable	General-purpose I/O bit 7 output enable is used by the host processor to configure the GPIO7 device pin as either an input or output. 0 = Configures GPIO7 as an output 1 = Configures GPIO7 as an input (default)
6	GPIO6OE	General-purpose I/O bit 6 output enable	General-purpose I/O bit 6 output enable is used by the host processor to configure the GPIO6 device pin as either an input or output. 0 = Configures GPIO6 as an output 1 = Configures GPIO6 as an input (default)
5	GPIO5OE	General-purpose I/O bit 5 output enable	General-purpose I/O bit 5 output enable is used by the host processor to configure the GPIO5 device pin as either an input or output. 0 = Configures GPIO5 as an output 1 = Configures GPIO5 as an input (default)
4	GPIO4OE	General-purpose I/O bit 4 output enable	General-purpose I/O bit 4 output enable is used by the host processor to configure the GPIO4 device pin as either an input or output. 0 = Configures GPIO4 as an output 1 = Configures GPIO4 as an input (default)
3	GPIO3OE	General-purpose I/O bit 3 output enable	General-purpose I/O bit 3 output enable is used by the host processor to configure the GPIO3 device pin as either an input or output. 0 = Configures GPIO3 as an output 1 = Configures GPIO3 as an input (default)
2	GPIO2OE	General-purpose I/O bit 2 output enable	General-purpose I/O bit 2 output enable is used by the host processor to configure the GPIO2 device pin as either an input or output. 0 = Configures GPIO2 as an output 1 = Configures GPIO2 as an input (default)
1	—	Reserved	Reserved for future use
0	GPIO0OE	General-purpose I/O bit 0 output enable	General-purpose I/O bit 0 output enable is used by the host processor to configure the GPIO0 device pin as either an input or output. 0 = Configures GPIO0 as an output 1 = Configures GPIO0 as an input (default)

6.2.41 GPIO Input Data Register

Address	52h							
Default	00h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	GPDI7	GPDI7	GPDI7	GPDI7	GPDI7	GPDI7	Reserved	GPDI7
Type	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

BIT	MNEMONIC	NAME	DESCRIPTION
7	GPDI7	General-purpose data input bit 7	General-purpose data input bit 7 is used by the host processor to read the data value on the GPIO7 device pin.
6	GPDI6	General-purpose data input bit 6	General-purpose data input bit 6 is used by the host processor to read the data value on the GPIO6 device pin.
5	GPDI5	General-purpose data input bit 5	General-purpose data input bit 5 is used by the host processor to read the data value on the GPIO5 device pin.
4	GPDI4	General-purpose data input bit 4	General-purpose data input bit 4 is used by the host processor to read the data value on the GPIO4 device pin.
3	GPDI3	General-purpose data input bit 3	General-purpose data input bit 3 is used by the host processor to read the data value on the GPIO3 device pin.
2	GPDI2	General-purpose data input bit 2	General-purpose data input bit 2 is used by the host processor to read the data value on the GPIO2 device pin.
1	—	Reserved	Reserved for future use
0	GPDI0	General-purpose data input bit 0	General-purpose data input bit 0 is used by the host processor to read the data value on the GPIO0 device pin.

6.2.42 MPEG Interface Output Enable Register 1

Address	53h							
Default	00h							
Bit	7	6	5	4	3	2	1	0
Mnemonic	DO7OE	DO6OE	DO5OE	DO4OE	DO3OE	DO2OE	DO1OE	DO0OE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

BIT	MNEMONIC	NAME	DESCRIPTION
7	DO7OE	MPEG data output bit 7 output enable	MPEG data output bit 7 output enable is used by the host processor to enable the output. After power-on reset, the output is disabled. 0 = Output is disabled (default) 1 = Output is enabled
6	DO6OE	MPEG data output bit 6 output enable	MPEG data output bit 6 output enable is used by the host processor to enable the output. After power-on reset, the output is disabled. 0 = Output is disabled (default) 1 = Output is enabled
5	DO5OE	MPEG data output bit 5 output enable	MPEG data output bit 5 output enable is used by the host processor to enable the output. After power-on reset, the output is disabled. 0 = Output is disabled (default) 1 = Output is enabled
4	DO4OE	MPEG data output bit 4 output enable	MPEG data output bit 4 output enable is used by the host processor to enable the output. After power-on reset, the output is disabled. 0 = Output is disabled (default) 1 = Output is enabled
3	DO3OE	MPEG data output bit 3 output enable	MPEG data output bit 3 output enable is used by the host processor to enable the output. After power-on reset, the output is disabled. 0 = Output is disabled (default) 1 = Output is enabled
2	DO2OE	MPEG data output bit 2 output enable	MPEG data output bit 2 output enable is used by the host processor to enable the output. After power-on reset, the output is disabled. 0 = Output is disabled (default) 1 = Output is enabled
1	DO1OE	MPEG data output bit 1 output enable	MPEG data output bit 1 output enable is used by the host processor to enable the output. After power-on reset, the output is disabled. 0 = Output is disabled (default) 1 = Output is enabled
0	DO0OE	MPEG data output bit 0 output enable	MPEG data output bit 0 output enable is used by the host processor to enable the output. After power-on reset, the output is disabled. 0 = Output is disabled (default) 1 = Output is enabled

6.2.43 MPEG Interface Output Enable Register 2

Address	54h							
Default	00h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SYNCSOE	DCLKOE
Type	R	R	R	R	R	R	R/W	R/W
Default	0	0	0	0	0	0	0	0

BIT	MNEMONIC	NAME	DESCRIPTION
7:2	—	Reserved	Reserved for future use
1	SYNCSOE	MPEG sync signals output enable	MPEG sync signals output enable is used by the host processor to enable the MPEG interface sync signals, which are packet clock (PACCLK), byte start (BYTESTART) and data error (DERROR). After power-on reset, the outputs are disabled. 0 = Outputs are disabled (default) 1 = Outputs are enabled
0	DCLKOE	MPEG data clock output enable	MPEG data clock output enable is used by the host processor to enable the clock output. After power-on reset, the output is disabled. 0 = Output is disabled (default) 1 = Output is enabled

6.2.44 Tuner Control Interface – I^2C Slave Device Address Register

The I^2C slave device address register contains the 7-bit I^2C slave device address and the read/write transaction control bit to be used for the tuner device.

Address	55h							
Default	00h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	A6	A5	A4	A3	A2	A1	A0	RW
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

BIT	MNEMONIC	NAME	DESCRIPTION
7:1	A(6:0)	Slave device address	The slave device address bits are set by the host processor with the 7-bit I^2C slave address of the Tuner device to be accessed.
0	RW	Read/write control	The read/write control bit value is set by the host processor to program the type of Tuner Control Interface I^2C transaction to be done. 1 = Read transaction 0 = Write transaction (default)

6.2.45 Tuner Control Interface – Data Register 1 Through 8

Address	56h to 5Dh							
Default	00h							
Bit	7	6	5	4	3	2	1	0
Mnemonic	D7	D6	D5	D4	D3	D2	D1	D0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	D(7:0)	Data (7:0)	Data register 1 through data register 8 contain the data bytes to be sent to the tuner for a write transaction or the data bytes received from the tuner for a read transaction. The data byte contained in data register 1 (56h) shall be the first byte sent to or read from the tuner.

6.2.46 Tuner Control Interface – Control and Status Register

Address	5Eh							
Default	00h							
Bit	7	6	5	4	3	2	1	0
Mnemonic	BCNT2	BCNT2	BCNT2	Reserved	Reserved	START	Reserved	MODE
Type	R/W	R/W	R/W	R	R	R/W	R	R/W
Default	0	0	0	0	0	0	0	0

BIT	MNEMONIC	NAME	DESCRIPTION
7:5	BCNT(2:0)	Byte count	The byte count is used by the host processor to set the number of data bytes to be transferred to/from the tuner device. The byte count should not include the tuner I^2C slave address byte. 000b = 1 byte, 001b = 2 bytes, ..., 110b = 7 bytes, 111b = 8 bytes
4:3	—	Reserved	Reserved for future use
2	START	Transaction start	The transaction start bit is set to 1 by the host processor to indicate to the MCU to start the transaction to the tuner. The MCU clears this bit at the end of the transaction.
1	—	Reserved	Reserved for future use
0	MODE	I^2C mode	The mode bit is used by the host processor to set the I^2C transfer mode and rate. 0 = Standard mode and 100-kbps transfer rate (default) 1 = Fast mode and 400-kbps transfer rate

6.2.47 Antenna Control Interface – Control and Status Register

Address	5Fh							
Default	00h							
Bit	7	6	5	4	3	2	1	0
Mnemonic	Reserved	Reserved	RXERR	MODE	TXSTART	TXRXSEL	TXDINV	PINSEL
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

BIT	MNEMONIC	NAME	DESCRIPTION
7:6	—	Reserved	Reserved for future use
5	RXERR	Receive data error	The receive data error bit is set to 1 by the MCU to indicate an error occurred when receiving data from a Mode B antenna. The MCU clears this bit at the beginning of the next transaction.
4	MODE	Auto receive mode	The auto receive mode bit is set to 1 by the host processor to enable the antenna control interface logic to automatically set-up the receive mode after a transmit data transaction.
3	TXSTART	Transmit start	This bit is set to 1 by the host processor to start the transmit data transaction to the antenna. The MCU clears this bit when the transaction is complete.
2	TXRXSEL	Transmit/receive select	This bit is used by the host processor to select the next type of transaction to be done by the antenna control interface. In manual mode, the host processor controls this bit. In auto receive mode, the host processor sets this bit to 1 for the transmit data transaction, and the MCU sets this bit to 0 after the completion of the transmit transaction to enable the receive transaction. 0 = Receive data transaction 1 = Transmit data transaction
1	TXDINV	Transmit data polarity	The transmit data polarity bit is set to 1 by the host processor to invert the transmit data output. 0 = Normal polarity in conformance with CEA909 1 = Invert the transmit data output
0	PINSEL	Pin mode select	The pin mode select bit is used by the host processor to select the antenna control interface pin configuration. Before the 2-pin mode is selected, the GPIO0 pin must be configured as an input in register 51h, bit 0. 0 = 2-pin mode (separate input and output pins are used, input = pin 72, output = pin 29) (default) 1 = 1-pin mode (one bidirectional pin is used, pin 29)

6.2.48 Antenna Control Interface – Transmit Data Register 1

Address	60h							
Default	00h							
Bit	7	6	5	4	3	2	1	0
Mnemonic	TXD7	TXD6	TXD5	TXD4	TXD3	TXD2	TXD1	TXD0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	TXD(7:0)	Transmit data (7:0)	The least significant 8 bits of the 14-bit data word to be transmitted to the antenna. Bits (13:8) are stored in register 61h, bits (5:0). The data word is set by the host processor.

6.2.49 Antenna Control Interface – Transmit Data Register 2

Address	61h							
Default	00h							
Bit	7	6	5	4	3	2	1	0
Mnemonic	Reserved	Reserved	TXD13	TXD12	TXD11	TXD10	TXD9	TXD8
Type	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

BIT	MNEMONIC	NAME	DESCRIPTION
7:6	—	Reserved	Reserved for future use
5:0	TXD(13:8)	Transmit data (13:8)	The most significant 6 bits of the 14-bit data word to be transmitted to the antenna. The data word is set by the host processor.

6.2.50 Antenna Control Interface – Receive Data Register 1

Address	62h							
Default	00h							
Bit	7	6	5	4	3	2	1	0
Mnemonic	RXD7	RXD6	RXD5	RXD4	RXD3	RXD2	RXD1	RXD0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	RXD(7:0)	Receive data (7:0)	The least significant 8 bits of the 10-bit program code received from a Mode B antenna. Bits (9:8) are stored in register 63h, bits (1:0).

6.2.51 Antenna Control Interface – Receive Data Register 2

Address	63h							
Default	00h							
Bit	7	6	5	4	3	2	1	0
Mnemonic	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RXD9	RXD8
Type	R	R	R	R	R	R	R/W	R/W
Default	0	0	0	0	0	0	0	0

BIT	MNEMONIC	NAME	DESCRIPTION
7:2	—	Reserved	Reserved for future use
1:0	RXD(9:8)	Receive data (9:8)	The most significant 2 bits of the 10-bit program code received from a Mode B antenna

6.2.52 Firmware ID – ROM Version Register

Address	70h							
Default	02h							
Bit	7	6	5	4	3	2	1	0
Mnemonic	ROMVER							
Type	R							
Default	0x02							

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	ROMVER	ROM version	Version identification for ROM code

6.2.53 Firmware ID – RAM Major Version Register

Address	71h							
Default	00h							
Bit	7	6	5	4	3	2	1	0
Mnemonic	RAM1VER							
Type	R							
Default	0x00							

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	RAM1VER	Major RAM version	Major version identification for RAM code

6.2.54 Firmware ID – RAM Minor Version Register

Address	72h							
Default	00h							
Bit	7	6	5	4	3	2	1	0
Mnemonic	RAM2VER							
Type	R							
Default	0x00							

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	RAM2VER	Minor RAM version	Minor version identification for RAM code

6.2.55 Device ID LSB Register

Address	80h							
Default	00h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	DEVID1							
Type	R							
Default	0x00							

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	DEVID1	Device ID LSB	LSB of the device ID

6.2.56 Device ID MSB Register

Address	81h							
Default	99h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	DEVID2							
Type	R							
Default	0x99							

BIT	MNEMONIC	NAME	DESCRIPTION
7:0	DEVID2	Device ID MSB	MSB of the device ID

6.2.57 Miscellaneous Control Register

Address	EEh							
Default	00h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	Reserved	Reserved	Reserved	Reserved	Reserved	INTRQPS	MCUMDE	MCURST
Type	R	R	R	R	R	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

BIT	MNEMONIC	NAME	DESCRIPTION
7:3	—	Reserved	Reserved for future use
2	INTRQPS	Interrupt request pin polarity select	The interrupt request pin polarity select bit is used by the host processor to select either an active low or active-high INTREQ output. Note that when active low is selected, the output goes tri-state when inactive (not driven high). Hence a pullup resistor needs to be used on the PCB. This is done so interrupt request sources from multiple ICs can be wired together. 0 = INTREQ output pin is active low (default) 1 = INTREQ output pin is active high
1	MCUMDE	MCU memory mode	The MCU memory mode is used by the host processor to select ROM or RAM as the code memory for the internal TVP9900 MCU. 0 = MCU executes from ROM (default) 1 = MCU executes from RAM
0	MCURST	MCU reset	The MCU reset bit is used by the host processor to do a soft reset of the internal TVP9900 MCU. 0 = MCU not in reset mode (default) 1 = MCU in reset mode

6.2.58 Software Interrupt Raw Status Register

The raw status bits in this register are cleared by the host processor by writing a 1 to the corresponding bit in the Software Interrupt Clear Register (FFh). The intended use of the raw status registers is for events to be monitored by the host processor via polling instead of interrupt driven.

Address	F9h							
Default	00h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	Reserved	Reserved	ACIRXCT	ACITXCT	ACIRXTO	Reserved	TCIERROR	TCIDONE
Type	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

BIT	MNEMONIC	NAME	DESCRIPTION
7:6	—	Reserved	Reserved for future use
5	ACIRXCT	Antenna Control Interface receive transaction complete	The Antenna Control Interface receive transaction complete raw status bit is set to 1 by the MCU when the receive transaction from a Mode B antenna is complete. This means an entire 10-bit data word was received. If an incomplete receive transaction (less than 10 bits) occurs, then this bit is not set; instead the ACIRXTO (bit 3) occurs. After the receive transaction is complete, the host processor should also check the receive data error status bit (RXERR) in the Antenna Control Interface Control and Status Register (5Fh) to ensure that an error was not detected while receiving the data.
4	ACITXCT	Antenna Control Interface transmit transaction complete	The Antenna Control Interface transmit transaction complete raw status bit is set to 1 by the MCU when the transmit transaction to the antenna is complete.
3	ACIRXTO	Antenna Control Interface receive timeout	The Antenna Control Interface receive timeout raw status bit is set to 1 by the MCU when the 100-ms timeout has occurred. If a 100-ms timeout occurs, then the antenna either did not reply to the transmit transaction (it is a mode A antenna) or an incomplete (less than 10-bits) receive transaction occurred. If an incomplete transaction occurred, then the receive error status bit (RXERR) in the Antenna Control Interface Control and Status Register (5Fh) is also set.
2	—	Reserved	Reserved for future use
1	TCIERROR	Tuner Control Interface transaction error	The Tuner Control Interface transaction error raw status bit is set to 1 by the MCU to indicate to the host processor that the tuner device did not respond to the I^2C transaction or that a NO ACK was received from the tuner when an ACK was expected.
0	TCIDONE	Tuner Control Interface transaction done	The Tuner Control Interface transaction done raw status bit is set to 1 by the MCU at the end of a normal transaction to indicate to the host processor that the tuner I^2C transaction completed successfully. If an error occurs during a transaction to the tuner, the MCU does not set this bit to 1.

6.2.59 Software Interrupt Status Register

The status bits in this register are the result of the logical AND of the corresponding raw status bits and mask bits. A status bit is also automatically cleared when the corresponding raw status bit is cleared. Unmasked status bits in this register assert the host processor interrupt request output pin, INTREQ, of the TVP9900 when the status bit is set to 1. All unmasked hardware and software status bits are ORed together to drive the INTREQ output pin.

Address	FBh							
Default	00h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	Reserved	Reserved	ACIRXCT	ACITXCT	ACIRXTO	Reserved	TCIERROR	TCIDONE
Type	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

BIT	MNEMONIC	NAME	DESCRIPTION
7:6	—	Reserved	Reserved for future use
5	ACIRXCT	Antenna Control Interface receive transaction complete	The Antenna Control Interface receive complete status bit is set to 1 (if unmasked) when the receive transaction from a Mode B antenna is complete and the bit is unmasked.
4	ACITXCT	Antenna Control Interface transmit transaction complete	The Antenna Control Interface transmit complete status bit is set to 1 (if unmasked) when the transmit transaction to the antenna is complete and the bit is unmasked.
3	ACIRXTO	Antenna Control Interface receive timeout	The Antenna Control Interface receive timeout status bit is set to 1 (if unmasked) when the 100-ms timeout has occurred and the bit is unmasked.
2	—	Reserved	Reserved for future use
1	TCIERROR	Tuner Control Interface transaction error	The Tuner Control Interface transaction error status bit is set to 1 (if unmasked) to indicate to the host processor that the tuner device did not respond to the I^2C transaction or that a NO ACK was received from the tuner when an ACK was expected.
0	TCIDONE	Tuner Control Interface transaction done	The Tuner Control Interface transaction done status bit is set to 1 (if unmasked) at the end of a normal transaction to indicate to the host processor that the tuner I^2C transaction completed successfully. If an error occurs during a transaction to the tuner, the MCU does not set this bit to 1.

6.2.60 Software Interrupt Mask Register

The interrupt mask registers are used by the host processor to mask unused interrupt sources. When an interrupt status bit is masked, the event results in the raw status bit being set but does not result in the status bit being set or the assertion of the interrupt request output pin, INTREQ.

Address	FDh							
Default	00h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	Reserved	Reserved	ACIRXCT	ACITXCT	ACIRXTO	Reserved	TCIERROR	TCIDONE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

BIT	MNEMONIC	NAME	DESCRIPTION
7:6	—	Reserved	Reserved for future use
5	ACIRXCT	Antenna Control Interface receive transaction complete interrupt mask	This bit is used by the host processor to enable the Antenna Control Interface receive transaction complete interrupt. 0 = Interrupt disabled (default) 1 = Interrupt enabled
4	ACITXCT	Antenna Control Interface transmit transaction complete interrupt mask	This bit is used by the host processor to enable the Antenna Control Interface transmit transaction complete interrupt. 0 = Interrupt disabled (default) 1 = Interrupt enabled
3	ACIRXTO	Antenna Control Interface receive timeout interrupt mask	This bit is used by the host processor to enable the Antenna Control Interface receive timeout interrupt. 0 = Interrupt disabled (default) 1 = Interrupt enabled
2	—	Reserved	Reserved for future use
1	TCIERROR	Tuner Control Interface transaction error interrupt mask	This bit is used by the host processor to enable the Tuner Control Interface transaction error interrupt. 0 = Interrupt disabled (default) 1 = Interrupt enabled
0	TCIDONE	Tuner Control Interface transaction done interrupt mask	This bit is used by the host processor to enable the Tuner Control Interface transaction done interrupt. 0 = Interrupt disabled (default) 1 = Interrupt enabled

6.2.61 Software Interrupt Clear Register

The interrupt clear registers are used by the host processor to clear the interrupt raw status and status bits. To clear an interrupt, a 1 must be written to the corresponding bit in this register. The interrupt clear bits are automatically reset to 0 by the TVP9900 hardware. When all unmasked interrupts are cleared, the INTREQ device output pin is inactive.

Address	FFh							
Default	00h							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mnemonic	Reserved	Reserved	ACIRXCT	ACITXCT	ACIRXTO	Reserved	TCIERROR	TCIDONE
Type	W	W	W	W	W	W	W	W
Default	0	0	0	0	0	0	0	0

BIT	MNEMONIC	NAME	DESCRIPTION
7:6	—	Reserved	Reserved for future use
5	ACIRXCT	Antenna Control Interface receive transaction complete interrupt clear	This bit should be set to 1 by the host processor to clear the Antenna Control Interface receive transaction complete raw status bit, which also clears the status bit and interrupt if unmasked.
4	ACITXCT	Antenna Control Interface transmit transaction complete interrupt clear	This bit should be set to 1 by the host processor to clear the Antenna Control Interface transmit transaction complete raw status bit, which also clears the status bit and interrupt if unmasked.
3	ACIRXTO	Antenna Control Interface receive timeout interrupt clear	This bit should be set to 1 by the host processor to clear the Antenna Control Interface receive timeout raw status bit, which also clears the status bit and interrupt if unmasked.
2	—	Reserved	Reserved for future use
1	TCIERROR	Tuner Control Interface transaction error interrupt clear	This bit should be set to 1 by the host processor to clear the Tuner Control Interface transaction error raw status bit, which also clears the status bit and interrupt if unmasked.
0	TCIDONE	Tuner Control Interface transaction done interrupt clear	This bit should be set to 1 by the host processor to clear the Tuner Control Interface transaction done raw status bit, which also clears the status bit and interrupt if unmasked.

7 Electrical Specifications

This section provides the absolute maximum ratings and the recommended operating conditions for the TVP9900 device.

All electrical and timing characteristics in this specification shall be valid over the recommended operating conditions, unless otherwise noted.

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

DVDD_1_5	Supply voltage range	1.5-V digital core supply	–0.5 V to 2.1 V
IOVDD_3_3	Supply voltage range	3.3-V I/O cell supply	–0.5 V to 4.2 V
AVDD_1_5	Supply voltage range	1.5-V analog core supply	–0.5 V to 2.1 V
AVDD_3_3	Supply voltage range	3.3-V analog core supply	–0.5 V to 4.2 V
AVDD_REF_3_3	Supply voltage range	3.3-V reference supply	–0.5 V to 4.2 V
AVDD_PLL_1_5	Supply voltage range	1.5-V PLL supply	–0.5 V to 2.1 V
V_I	Input voltage range	XTALIN, oscillator input	–0.5 V to AVDD_PLL_1_5 + 0.5 V
		Fail-safe LVCMOS	–0.5 V to IOVDD_3_3 + 0.5 V
		Differential IF inputs: AIFIN_P, AIFIN_N	–0.5 V to AVDD_3_3 + 0.5 V
V_O	Output voltage range	XTALOUT, oscillator output	–0.5 V to AVDD_PLL_1_5 + 0.5 V
		Fail-safe LVCMOS	–0.5 V to IOVDD_3_3 + 0.5 V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{CC}$	±20 mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$	±20 mA
T_A	Operating free-air temperature range		0°C to 70°C
T_{stg}	Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. **These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.** Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
DVDD_1_5	1.5-V digital core supply voltage		1.35	1.5	1.65	V
IOVDD_3_3	3.3-V I/O cell supply voltage		3	3.3	3.6	V
AVDD_1_5	1.5-V analog core supply voltage		1.35	1.5	1.65	V
AVDD_3_3	3.3-V analog core supply voltage		3	3.3	3.6	V
AVDD_PLL_1_5	1.5-V PLL supply voltage		1.35	1.5	1.65	V
AVDD_REF_3_3	3.3-V reference supply voltage		3	3.3	3.6	V
V_I	Input voltage	XTALIN	0		AVDD_PLL_1_5	V
		LVCMOS	0		IOVDD_3_3	
V_O	Output voltage	XTALOUT	0		AVDD_PLL_1_5	V
		LVCMOS	0		IOVDD_3_3	
V_{IH}	High-level input voltage	XTALIN	0.7(AVDD_PLL_1_5)		AVDD_PLL_1_5	V
		LVCMOS	0.7(IOVDD_3_3)		IOVDD3_3	
V_{IL}	Low-level input voltage	XTALIN	0		0.3(AVDD_PLL_1_5)	V
		LVCMOS	0		0.3(IOVDD_3_3)	
I_{OH}	High-level output current	LVCMOS			–8	mA
I_{OL}	Low-level output current	LVCMOS			8	mA
f_{clock}	Clock input frequency	XTALIN		25		MHz
		CLKIN		25		
t_t (1)	Input transition, rise and fall time, 10% to 90%		0		25	ns
T_A	Operating free-air temperature		0	25	70	°C
T_J	Operating junction temperature		0	25	105	°C

(1) Specified by design

7.3 DC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	LVCMOS	I_{OH} = –8 mA	0.8(IOVDD_3_3)			V
V_{OL}	Low-level output voltage	LVCMOS	I_{OL} = 8 mA			0.22(IOVDD_3_3)	V
I_{IL}	Low-level input current		$V_I = V_{IL}$ (min)			±1	µA
I_{IH}	High-level input current		$V_I = V_{IH}$ (max)			±1	µA
I_{OZ}	High-impedance output current		Specified by design			±20	µA
$I_{DVDD_1_5}$	1.5-V digital core supply current		(1)		630		mA
$I_{IOVDD_3_3}$	3.3-V I/O cell supply current		(1)		3		mA
$I_{AVDD_1_5}$	1.5-V analog core supply current		(1)		0.2		mA
$I_{AVDD_3_3}$	3.3-V analog core supply current		(1)		45		mA
$I_{AVDD_PLL_1_5}$	1.5-V analog PLL supply current		(1)		5		mA
$I_{AVDD_REF_3_3}$	3.3-V analog reference supply current		(1)		22		mA
P_D	Power dissipation		8-VSB mode with parallel MPEG output (1)		1.2		W
			Power-down mode		0.45		mW
C_i	Input capacitance				8		pF
C_o	Output capacitance				8		pF

(1) For typical values: nominal voltages, T_A = 25°C

7.4 Analog Input Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Differential input voltage	$C_{coupling}$ = 0.1 µF			1	Vp-p
R_I	Input resistance			2.4		kΩ
C_I	Differential input capacitance	Specified by design			10	pF
	Minimum input gain control			-6		dB
	Maximum input gain control			6		dB

7.5 Timing Characteristics

over recommended operating conditions (unless otherwise noted), specified by design

7.5.1 Crystal and Input Clock

The TVP9900 can be used with an external crystal with a frequency of 25 MHz or with an external clock source with a frequency of 4 MHz or 25 MHz. The on-chip oscillator in the TVP9900 is designed to work with an external crystal with a frequency range of 15 MHz to 35 MHz. Therefore, if a clock frequency of 4 MHz is required, an external clock source, not an external crystal, must be used. When an external clock source is used, the on-chip oscillator simply functions as an input buffer.

Table 7-1. Crystal and Input Clock Timing

PARAMETER		MIN	TYP	MAX	UNIT
f_{XTALIN}	Frequency, XTALIN (external crystal or clock source)		25		MHz
t_{cyc1}	Cycle time, XTALIN (external crystal or clock source)(1)		40		ns
f_{XTALIN}	Frequency, XTALIN (external clock source only)		4		MHz
t_{cyc1}	Cycle time, XTALIN (external clock source only)(1)		250		ns
	Frequency stability	–50		50	ppm

(1) Worst-case duty cycle is 45/55.



Figure 7-1. Crystal or Clock Timing Waveform

7.5.2 Device Reset

The power-on reset signal, RESETZ, is an active-low asynchronous reset that is used to initialize the device at power-up. The RESETZ signal may be low during power-up but must remain active low for a minimum of 1 ms after all power-supply voltages are stable at the recommended operating voltage. Internal circuits synchronize the power-on reset with internal clocks; therefore, the RESETZ signal must remain active low for a minimum of 1 µs after the crystal oscillator and clocks are stable.

Table 7-2. Device Reset Timing

PARAMETER		MIN	TYP	MAX	UNIT
$t_{w1(L)}$	Pulse duration, RESETZ low after all power supplies are stable at the recommended operating voltage and the crystal oscillator is stable	1			ms

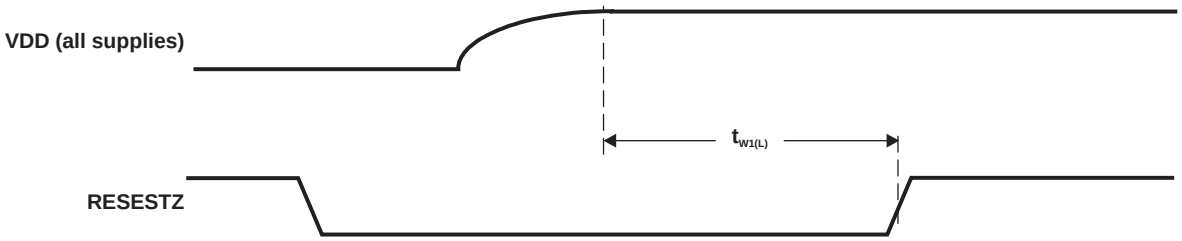


Figure 7-2. Device Reset Signal Timing Waveforms

7.5.3 MPEG Interface

7.5.3.1 Parallel Mode (Data Only)

The polarity of DCLK, BYTE_START, PACCLK and DERROR are programmable. The timing waveforms in Figure 7-3 are shown with BYTE_START, PACCLK, and DERROR as active-high signals and with the output signals transitioning with respect to the falling edge of DCLK. In this mode, PACCLK is always active. If an error occurs, the DERROR signal is active for the length of the entire packet. The packet length is 188 bytes.

Table 7-3. Parallel Mode (Data Only) Timing

C_L = 30 pF

PARAMETER			MIN	TYP	MAX	UNIT
f_{DCLK}	Frequency, DCLK	8 VSB mode		2.42408		MHz
		64 QAM mode		3.37129		
		256 QAM mode		4.85133		
d_{cyc}	Duty cycle, DCLK			50		%
t_{pd1}	Propagation delay time, DCLK falling (or rising) edge to DATAOUT [7:0] valid		–2		3	ns
t_{pd2}	Propagation delay time, DCLK falling (or rising) edge to BYTE_START high		–2		3	ns
t_{pd3}	Propagation delay time, DCLK falling (or rising) edge to BYTE_START low		–2		3	ns
t_{pd4}	Propagation delay time, DCLK falling (or rising) edge to DERROR high		–2		3	ns
t_{pd5}	Propagation delay time, DCLK falling (or rising) edge to DERROR low		–2		3	ns

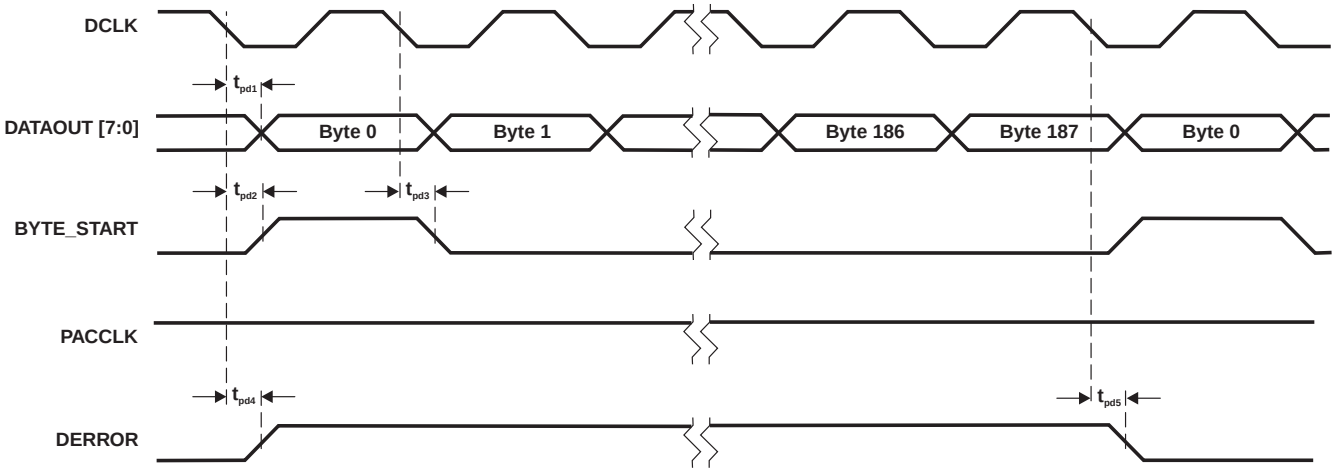


Figure 7-3. MPEG Interface – Parallel Mode (Data Only) Timing Waveforms

7.5.3.2 Serial Mode (Data Only)

The polarity of DCLK, BYTE_START, PACCLK and DERROR are programmable. The timing waveforms in Figure 7-4 are shown with BYTE_START, PACCLK, and DERROR as active-high signals and with the output signals transitioning in respect to the falling edge of DCLK. BYTE_START is active for the eight clock cycles corresponding to the eight bits of the first byte of data. In this mode, PACCLK is always active. If an error occurs, the DERROR signal is active for the length of the entire packet. The packet length is 188 bytes.

Table 7-4. Serial Mode (Data Only) Timing

C_L = 30 pF

PARAMETER			MIN	TYP	MAX	UNIT
f_{DCLK}	Frequency, DCLK	8 VSB mode		19.39266		MHz
		64 QAM mode		26.97035		
		256 QAM mode		38.81070		
d_{cyc}	Duty cycle, DCLK			50		%
t_{pd1}	Propagation delay time, DCLK falling (or rising) edge to SERDATAO valid		–2		3	ns
t_{pd2}	Propagation delay time, DCLK falling (or rising) edge to BYTE_START high		–2		3	ns
t_{pd3}	Propagation delay time, DCLK falling (or rising) edge to BYTE_START low		–2		3	ns
t_{pd4}	Propagation delay time, DCLK falling (or rising) edge to DERROR high		–2		3	ns
t_{pd5}	Propagation delay time, DCLK falling (or rising) edge to DERROR low		–2		3	ns

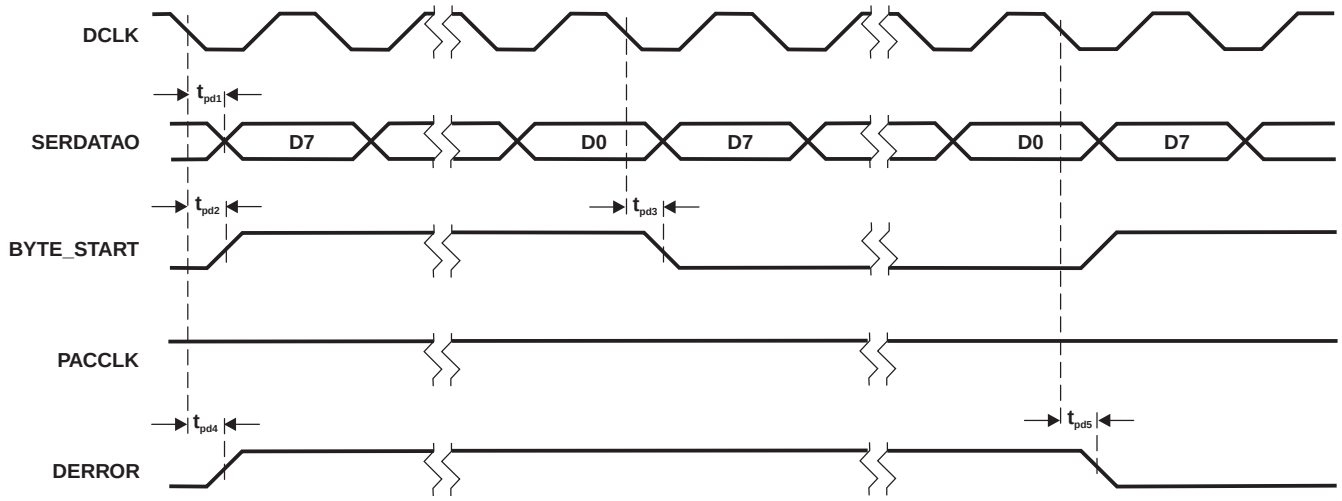


Figure 7-4. MPEG Interface – Serial Mode (Data Only) Timing Waveforms

7.5.3.3 Parallel Mode (Data With Redundancy)

The polarity of DCLK, BYTE_START, PACCLK and DERROR are programmable. The timing waveforms in Figure 7-5 are shown with BYTE_START, PACCLK and DERROR as active-high signals and with the output signals transitioning with respect to the falling edge of DCLK. PACCLK is only active during the time period that the 188 bytes of data are being transferred. If an error occurs, the DERROR signal is active for the length of the entire packet.

Table 7-5. Parallel Mode (Data With Redundancy) Timing

C_L = 30 pF

PARAMETER			MIN	TYP	MAX	UNIT
f_{DCLK}	Frequency, DCLK	8 VSB mode		2.68196		MHz
		64 QAM mode		3.65821		
		256 QAM mode		5.26422		
d_{cyc}	Duty cycle, DCLK			50		%
t_{pd1}	Propagation delay time, DCLK falling (or rising) edge to DATAOUT [7:0] valid		–2		3	ns
t_{pd2}	Propagation delay time, DCLK falling (or rising) edge to BYTE_START high		–2		3	ns
t_{pd3}	Propagation delay time, DCLK falling or rising edge to BYTE_START low		–2		3	ns
t_{pd4}	Propagation delay time, DCLK falling (or rising) edge to PACCLK high		–2		3	ns
t_{pd5}	Propagation delay time, DCLK falling (or rising) edge to PACCLK low		–2		3	ns
t_{pd6}	Propagation delay time, DCLK falling (or rising) edge to DERROR high		–2		3	ns
t_{pd7}	Propagation delay time, DCLK falling (or rising) edge to DERROR low		–2		3	ns

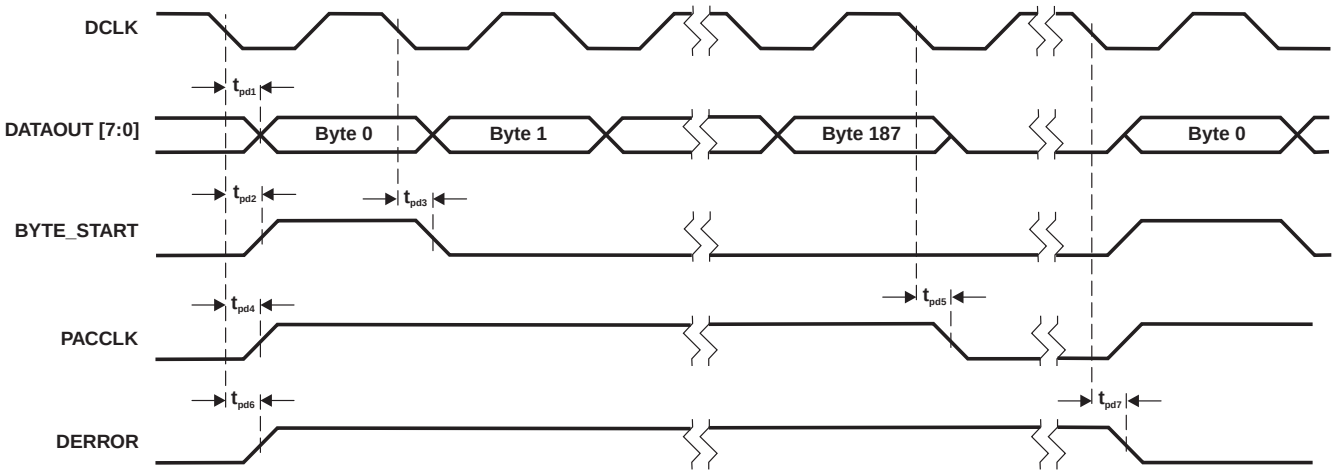


Figure 7-5. MPEG Interface – Parallel Mode (Data With Redundancy) Timing Waveforms

7.5.3.4 Serial Mode (Data With Redundancy)

The polarity of DCLK, BYTE_START, PACCLK and DERROR are programmable. The timing waveforms in Figure 7-6 are shown with BYTE_START, PACCLK, and DERROR as active-high signals and with the output signals transitioning in respect to the falling edge of DCLK. BYTE_START is active for the eight clock cycles corresponding to the eight bits of the first byte of data. PACCLK is only active during the time period that the 188 bytes of data are being transferred. If an error occurs, the DERROR signal is active for the length of the entire packet.

Table 7-6. Serial Mode (Data With Redundancy) Timing

C_L = 30 pF

PARAMETER			MIN	TYP	MAX	UNIT
f_{DCLK}	Frequency, DCLK	8 VSB mode		2.42408		MHz
		64 QAM mode		3.37129		
		256 QAM mode		4.85133		
d_{cyc}	Duty cycle, DCLK			50		%
t_{pd1}	Propagation delay time, DCLK falling (or rising) edge to DATAOUT [7:0] valid				3	ns
t_{pd2}	Propagation delay time, DCLK falling (or rising) edge to BYTE_START high				3	ns
t_{pd3}	Propagation delay time, DCLK falling (or rising) edge to BYTE_START low				3	ns
t_{pd4}	Propagation delay time, DCLK falling (or rising) edge to DERROR high				3	ns
t_{pd5}	Propagation delay time, DCLK falling (or rising) edge to DERROR low				3	ns

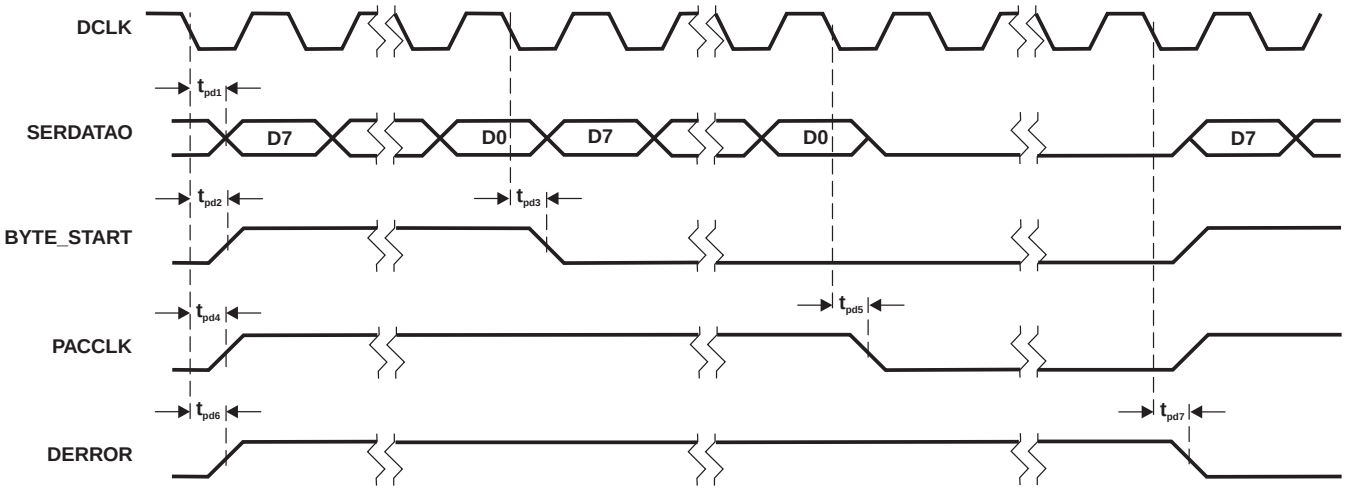


Figure 7-6. MPEG Interface – Serial Mode (Data With Redundancy) Timing Waveforms

7.5.4 Host and Tuner I²C Interface

Host processor communication with the TVP9900 device is done via an I²C slave interface. The TVP9900 also has an I²C master interface that is used by the TVP9900 to communicate with the system tuner. Both of these I²C interfaces are designed to work for both standard and fast modes of operation. The timing parameters and the timing waveforms below pertain to both I²C interfaces.

Table 7-7. Host and Tuner I ²C Interface Timing

PARAMETER		STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
f_{SCL}	Frequency, SCL	0	100	0	400	kHz
$t_{W(H)}$	Pulse duration, SCL high	4		0.6		µs
$t_{W(L)}$	Pulse duration, SCL low	4.7		1.3		µs
t_r	Rise time, SCL and SDA		1000		300	ns
t_f	Fall time, SCL and SDA		300		300	ns
t_{su1}	Setup time, SDA to SCL	250		100		ns
t_{h1}	Hold time, SCL to SDA(1)	0		0		ns
t_{buf}	Bus free time between stop and start condition	4.7		1.3		µs
t_{su2}	Setup time, SCL to start condition	4.7		0.6		µs
t_{h2}	Hold time, start condition to SCL	4		0.6		µs
t_{su3}	Setup time, SCL to stop condition	4		0.6		µs
C_L	Load capacitance for each bus line		400		400	pF

(1) The TVP9900 internally provides a minimum hold time of 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

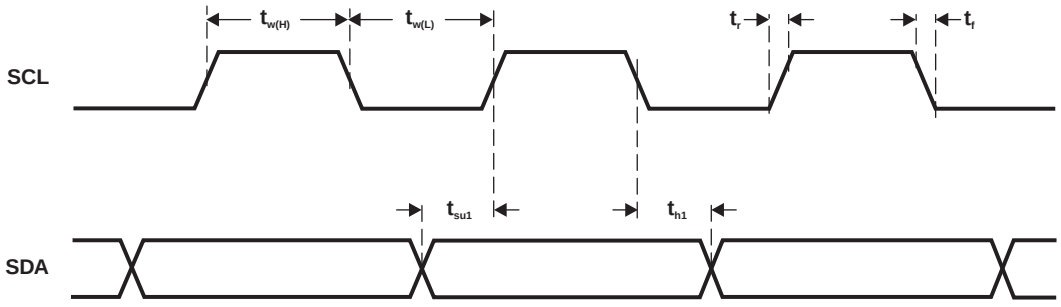


Figure 7-7. I²C SCL and SDA Timing Waveforms

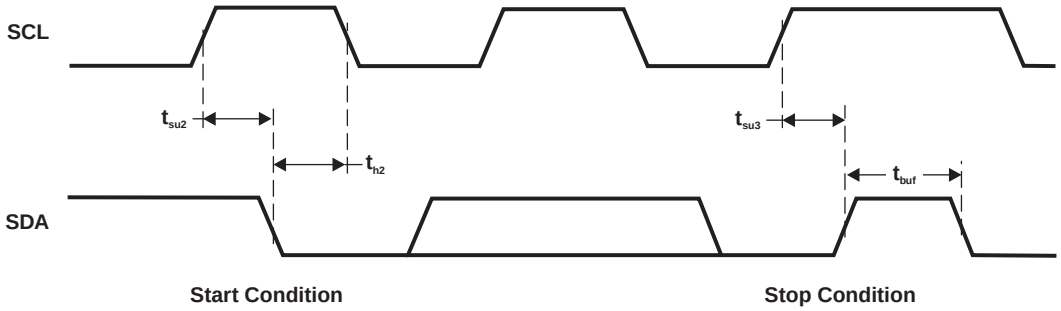
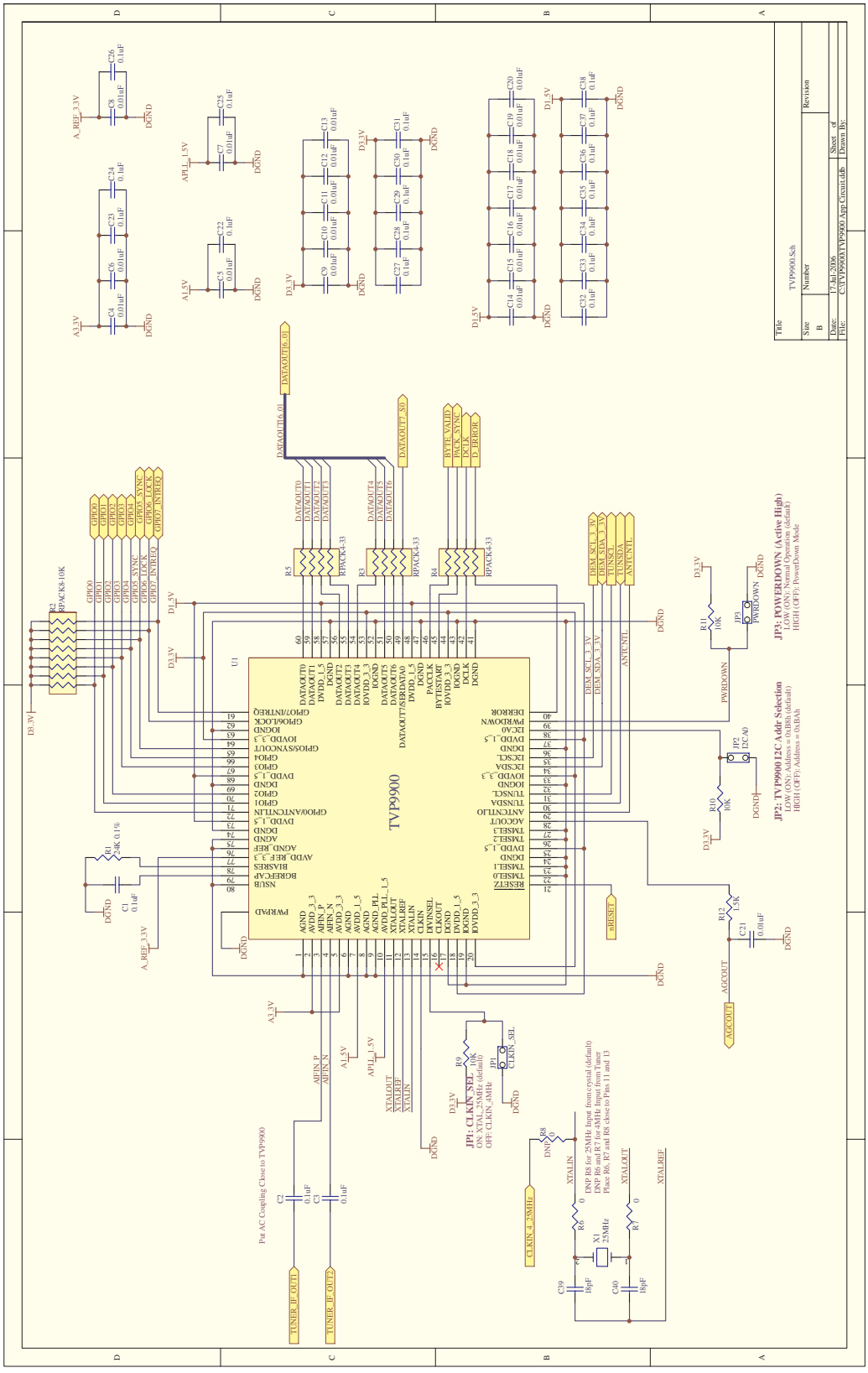


Figure 7-8. I²C Start and Stop Conditions Timing Waveforms

8 Application Circuit



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TVP9900PFP	NRND	HTQFP	PFP	80		TBD	Call TI	Call TI	0 to 70	TVP9900	
TVP9900PFPR	NRND	HTQFP	PFP	80		TBD	Call TI	Call TI	0 to 70	TVP9900	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

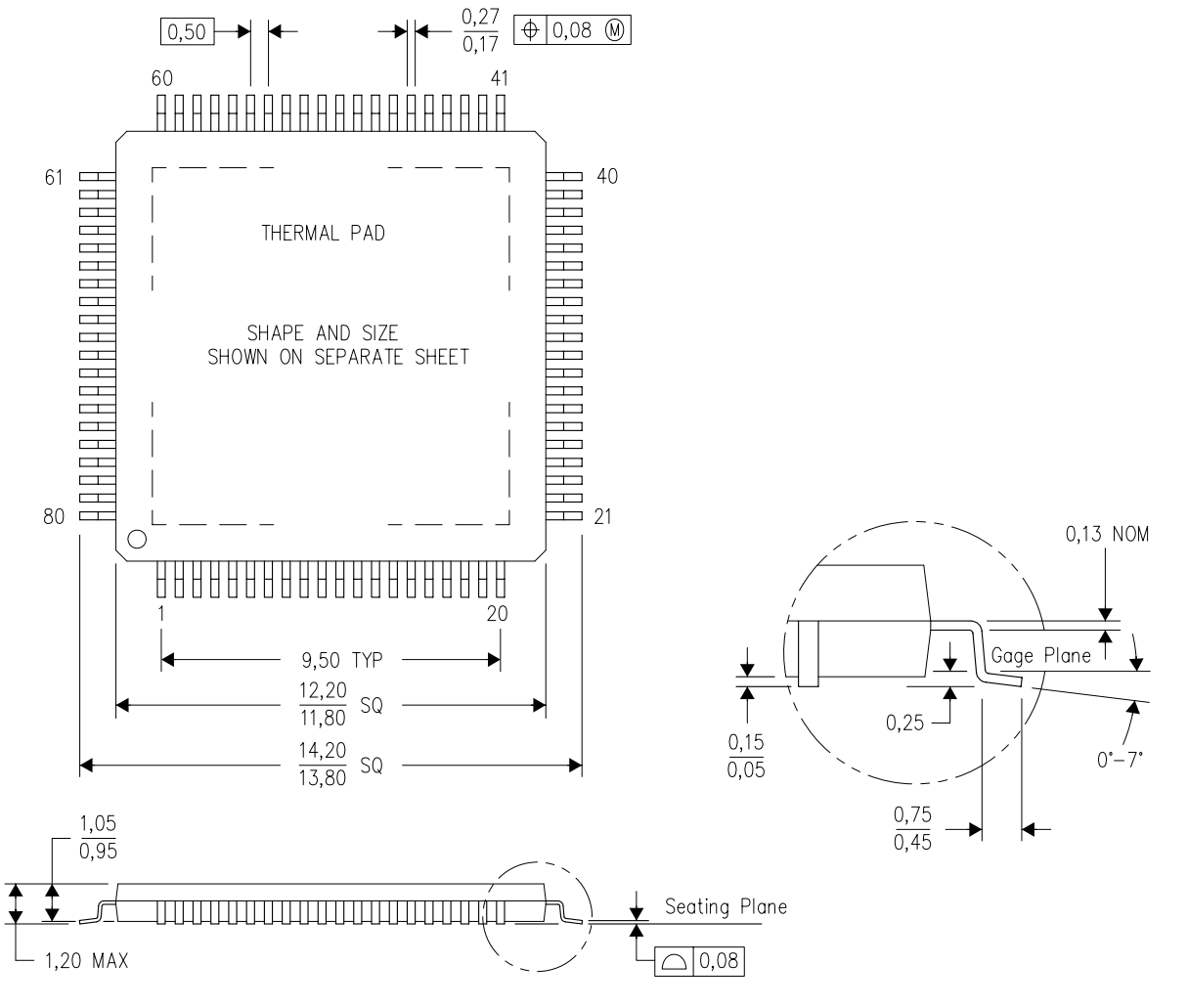
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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