Features

- 8.5 V Supply Voltage
- Voltage Regulator for Stable Operating Conditions
- Microprocessor-controlled Via a Simple Two-wire Bus
- Two Addresses Selectable
- Gain-controlled RF Amplifier with Two Inputs, Selectable Via a Simple Two-wire Bus Control
- Balanced RF Amplifier Inputs
- Gain-controlled RF Mixer
- Four-pin Voltage-controlled Oscillator
- SAW Filter Driver with Differential Low-impedance Output
- AGC Voltage Generation for RF Section, Available at Charge-pump Output (Can Also Be Used to Control a PIN Diode Attenuator)
- Gain-controlled IF Amplifier
- Balanced IF Amplifier Inputs
- Selectable Gain-controlled IF Mixer
- Single-ended IF Output
- AGC Voltage Generation for IF Section, Available at Charge-pump Output
- Separate Differential Input for the IF AGC Block
- All AGC Time Constants Adjustable
- AGC Thresholds Programmable Via a Simple Two-wire Bus
- Three AGC Charge Pump Currents Selectable (Zero, Low, High)
- Reference Oscillator
- Programmable 9-bit Reference Divider
- Programmable 15-bit Counter 1:2048 to 1:32767 Effectively
- Tristate Phase Detector with Programmable Charge Pump
- Superior Phase-noise Performance
- Deactivation of Tuning Output Programmable
- Three Switching Outputs (Open Collector)
- Three D/A Converters (Resolution: 8 Bits)
- Lock Status Indication (Open Collector)

Electrostatic sensitive device.
Observe precautions for handling.

DAB One-chip Front End

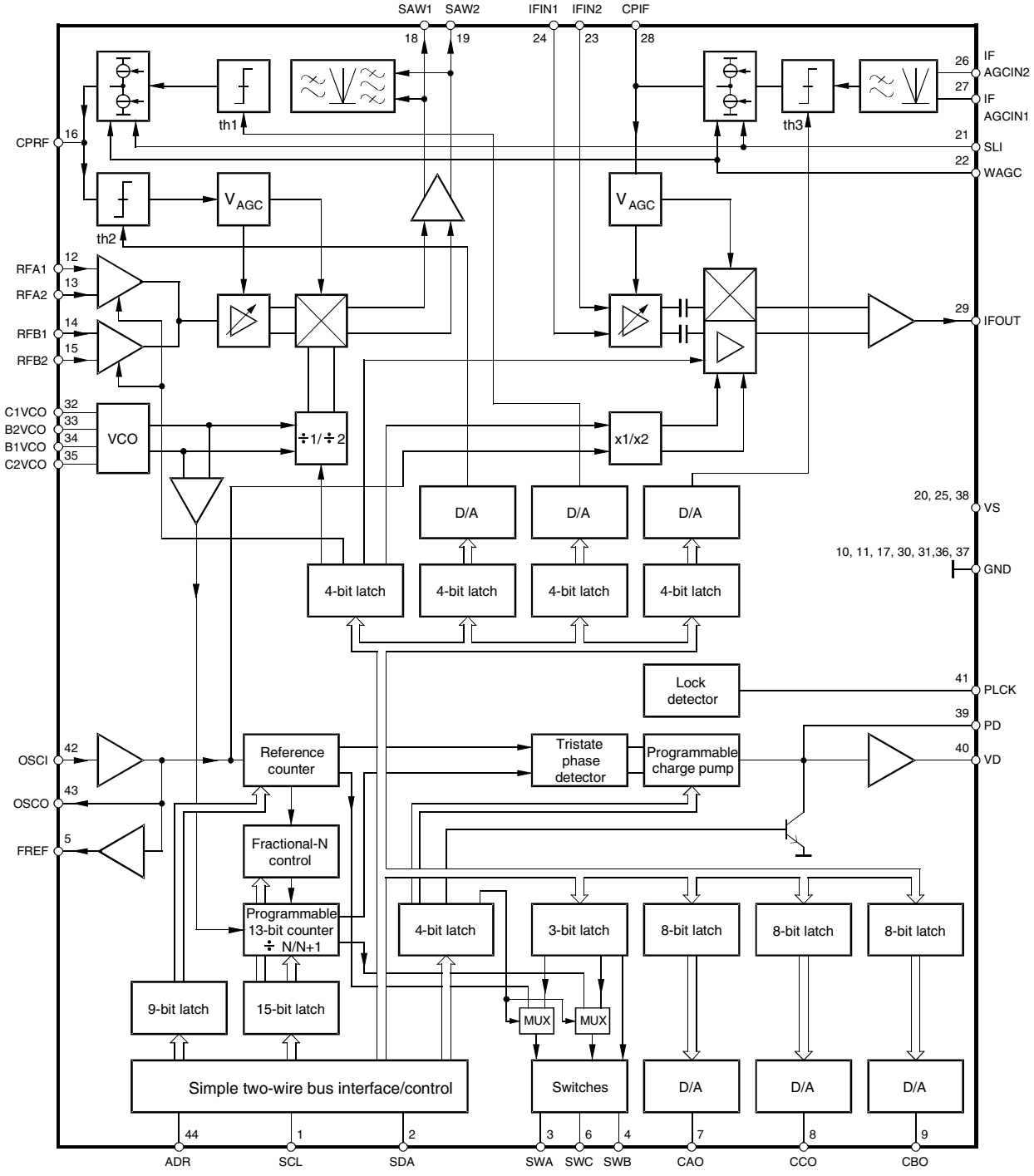
U2731B

Description

The U2731B is a monolithically integrated Digital Audio Broadcasting one-chip front end circuit manufactured using Atmel's advanced UHF5S technology. Its functionality covers a gain-controlled RF amplifier with two selectable RF inputs, a gain-controlled RF mixer, a VCO which provides the LO signal for the RF mixers, either directly or after passing a frequency divider, a SAW filter driver, an AGC block for the RF section, a gain-controlled IF amplifier, an IF mixer which can also be bypassed, an AGC block for the IF section and a fractional-N frequency synthesizer. The frequency synthesizer controls the VCO to synthesize frequencies in the range of 70 MHz to 500 MHz in a 16-kHz raster; within certain limits the reference divider factor is fully programmable. The lock status of the phase detector is indicated at a special output pin; three switching outputs can be addressed. A reference signal which is generated by an on-chip reference oscillator is available at an output pin. This reference signal is also used to generate the LO signal for the IF mixer, either by doubling the frequency or by using the reference frequency itself. Three D/A converters at a resolution of 8 bits provide a digitally controllable output voltage. The thresholds inside the AGC blocks can be digitally controlled by means of on-chip 4-bit D/A converters. All functions of this IC are controlled via a simple two-wire bus.

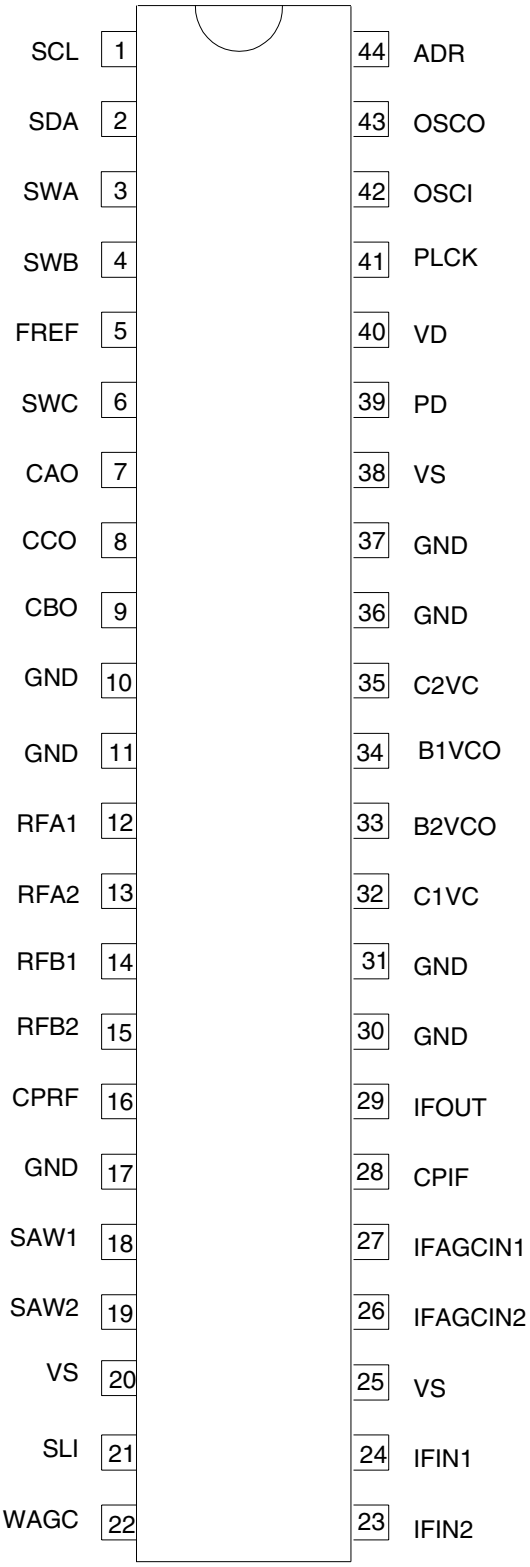
Rev. 4671C–DAB–06/04

Figure 1. Block Diagram



Pin Configuration

Figure 2. Pinning



Pin Description

Pin	Symbol	Function
1	SCL	Clock (simple two-wire bus)
2	SDA	Data (simple two-wire bus)
3	SWA	Switching output (open collector)
4	SWB	Switching output (open collector)
5	FREF	Reference frequency output (for U2731B)
6	SWC	Switching output (open collector)
7	CAO	Output of D/A converter A
8	CCO	Output of D/A converter B
9	CBO	Output of D/A converter C
10	GND	Ground
11	GND	Ground
12	RFA1	Input 1 of RF amplifier A (differential)
13	RFA2	Input 2 of RF amplifier A (differential)
14	RFB1	Input 1 of RF amplifier B (differential)
15	RFB2	Input 2 of RF amplifier B (differential)
16	CPRF	Charge-pump output (RF AGC block)
17	GND	Ground
18	SAW1	SAW driver output 1 (differential)
19	SAW2	SAW driver output 2 (differential)
20	VS	Supply voltage RF part
21	SLI	AGC mode selection (charge-pump current high)
22	WAGC	AGC mode selection (charge-pump current off)
23	IFIN2	Input 2 of IF amplifier (differential)
24	IFIN1	Input 1 of IF amplifier (differential)
25	VS	Supply voltage IF part
26	IFAGCIN2	Input 2 of IF AGC block (differential)
27	IFAGCIN1	Input 1 of IF AGC block (differential)
28	CPIF	Charge-pump output (IF AGC block)
29	IFOUT	IF output (single ended)
30	GND	Ground
31	GND	Ground
32	C1VC	Collector 1 of VCO
33	B2VCO	Base 2 of VCO
34	B1VCO	Base 1 of VCO
35	C2VC	Collector 2 of VCO
36	GND	Ground
37	GND	Ground
38	VS	Supply voltage PLL
39	PD	Tri-state charge pump output
40	VD	Active filter output

Pin Description (Continued)

Pin	Symbol	Function
41	PLCK	Lock-indicating output (open collector)
42	OSCI	Input of reference oscillator/buffer
43	OSCO	Output of reference oscillator/buffer
44	ADR	Address selection (simple two-wire bus)

Functional Description

The U2731B represents a monolithically integrated front end IC designed for applications in DAB receivers. It covers RF and IF signal processing, the PLL section and also supporting functions such as D/A converters or switching outputs.

Two RF input ports offer the possibility of handling various input signals such as a down-converted L-band signal or band II and band III RF signals. The high dynamic range of the RF inputs and the use of a gain-controlled amplifier and a gain-controlled mixer in the RF section offer the possibility of handling even strong RF input signals. The LO signal of the first mixer stage is derived from an on-chip VCO. The VCO frequency is either divided by two or directly fed to the mixer. In this way band II and band III can be covered easily.

In the IF section, it can be selected if the first IF signal is down-converted to a second, lower IF or if it is simply amplified to appear at the IF output. If the down-conversion option is chosen, it can be selected if the LO signal of the IF mixer is directly derived from the reference signal of the PLL, or if it is generated by doubling its frequency. The amplifiers in the IF section are gain-controlled in similar fashion to the RF section.

The RF and the IF part also contain AGC functional blocks which generate the AGC control voltages. The AGC thresholds can be defined by means of three on-chip 4-bit D/A converters.

The frequency of the VCO is locked to a reference frequency by an on-chip fractional-N PLL circuit which guarantees a superior phase-noise performance. The reference frequency is generated by an on-chip crystal oscillator which can also be overdriven by an external signal. Starting from a minimum value, the reference scaling factor is freely programmable.

Three switching outputs can be used for various switching tasks on the front end board. Three 8-bit D/A converters providing an output voltage between 0 and 8.5 V are used to improve the tuning voltages of the tuned preselectors which are derived from the tuning voltage of the VCO.

RF Part

RF Gain-controlled Amplifier

In order to support two different channels, two identical input buffers with balanced inputs (RFA1, RFA2; RFB1, RFB2) are integrated. By setting the two-wire bus bits M0 and M1 (see section “Simple Two-wire Bus Functions” on page 11), the active buffer can be selected. The buffers are followed by a gain-controlled amplifier whose output signal is fed to a gain-controlled mixer. The RF amplifiers are capable of handling input signals up to a typical power of -6 dBm without causing third-order intermodulation components stronger than -40 dBc.

RF Gain-controlled Mixer, VCO and LO Divider

The purpose of the RF mixer is to down-convert the incoming signal (band II, band III) to an IF frequency which is typically 38.912 MHz. This IF signal is fed to an AGC voltage-generation block (which is described in the following section) and an output buffer stage. This driver stage has a low output impedance and is capable of driving a SAW filter directly via its differential output pins SAW1, SAW2. The mixer's LO signal is generated by a balanced voltage-controlled oscillator whose frequency is stabilized by a fractional-N phase-locked loop. An example circuit of the VCO is shown in Figure 12 on page 23. The oscillator's tank is applied to the pins B1VC, C1VC, B2VC, C2VC as shown in the application circuit in Figure 8 on page 20. Before the VCO's signal is fed to the RF mixer, it has to pass an LO divider block where the VCO frequency is either divided by 1 or 2. The setting of this divider is defined by means of the two-wire bus bits M0 and M1 as indicated in the section “Simple Two-wire Bus Functions” on page 11. This feature offers the possibility of covering both band II and band III by tuning the VCO frequency in the range between 200 MHz to 300 MHz.

RF AGC Voltage-generation Block

In this functional block, the output signal of the RF mixer is amplified, weakly bandpass filtered (transition range: X8 MHz to X80 MHz), rectified and finally lowpass filtered. The voltage derived in this *power-measurement process* is compared to a voltage threshold (th1) which can be digitally controlled by an on-chip 4-bit D/A converter. The setting of this converter is defined by means of the two-wire bus bits TAi (i = 1, 2, 3, 4). Depending on the result of this comparison, a charge pump feeds a positive or negative current to pin CPRF in order to charge or discharge an external capacitor. The voltage of this external capacitor can be used to control the gain of an external preamplifier or attenuator stage. Furthermore, it is also used to generate the internal control voltages of an RF amplifier and mixer. For this purpose, the voltage at pin CPRF is compared to a voltage threshold (th2) which is also controlled by an on-chip 4-bit D/A converter whose setting is fixed by the two-wire bus bits TBi (i =1, 2, 3, 4).

By means of the input pins WAGC and SLI the current of the RF AGC charge pump can be selected according to the following table:

Table 1. Current of Charge Pump

WAGC	SLI	Charge-pump Current/µA
HIGH	X	off
LOW	LOW	50 µA (slow mode)
LOW	HIGH	190 µA (fast mode)

The function can be seen in Figure 11 on page 22.

IF Part

IF Gain-controlled Amplifier

The signal applied to the balanced input pins IFIN1, IFIN2 is amplified by a gain-controlled IF amplifier. The gain-control signal is generated by an IF AGC voltage-generation block which is described in the next section. To avoid offset problems, the output of the gain-controlled amplifier is fed to an amplifier/mixer combination by AC coupling.

IF Gain-controlled Amplifier/Mixer Combination

Depending on the setting of the two-wire bus bits M2, M3, the output signal of the gain-controlled IF amplifier is either mixed down to a lower, second IF or, after passing an output buffer stage, amplified before it appears at the single-ended output pin IFOUT. If the down-conversion option is chosen this circuit still offers two possibilities concerning the synthesis of the IF mixers LO signal. This LO signal is derived from the PLL's on-chip reference oscillator. By means of the two-wire bus bits M2, M3, it can be decided whether the reference frequency is doubled before it is given to the mixer's LO port, or if it is used directly. The gain-control voltage of the amplifier/mixer combination is similar to the gain-controlled IF amplifier generated by an internal gain-control circuit.

IF AGC Voltage-generation Block

The purpose of this gain-control circuit in the IF part is to measure the power of the incoming signal at the balanced input pins IFAGCIN1, IFAGCIN2, to compare it with a certain power level and to generate a control voltage for the IF gain-controlled amplifiers and mixer. This architecture offers the possibility of ensuring an optimal use of the dynamic range of the A/D converter which transforms the output signal at pin IFOUT from the analog to the digital domain despite possible insertion losses of (anti-aliasing) filters which are arranged in front of the converter. Such a constellation is indicated in the application circuit in Figure 8 on page 20.

The incoming signal at the balanced input pins IFAGC1, IFAGC2 passes a *power-measurement process* similar to that described in the section “RF AGC Voltage-generation Block” on page 6. For flexibility reasons, no bandpass filtering is implemented. The voltage derived in this process is compared to a voltage threshold (th3) which is defined by an on-chip 4-bit D/A converter. The setting of this converter is defined by the two-wire bus bits TCi (i = 1, 2, 3, 4). Depending on the result of this comparison, a charge pump feeds a positive or negative current to pin CPIF in order to charge or discharge an external capacitor. By means of the pins WAGC and SLI the current of this charge pump can be selected according to the following table:

Table 2. Current of Charge Pump

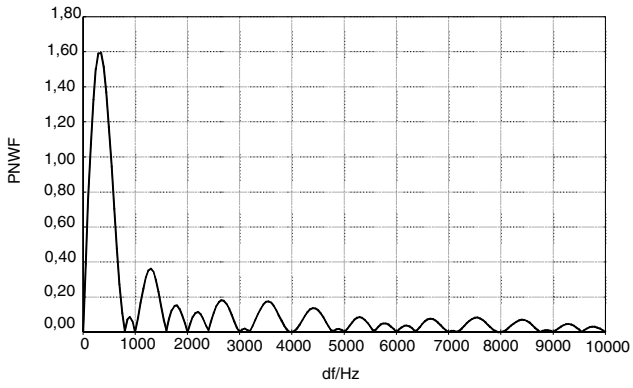
WAGC	SLI	Charge-pump Current/µA
HIGH	X	off
LOW	LOW	50 µA (slow mode)
LOW	HIGH	190 µA (fast mode)

The function can be seen in Figure 12 on page 23.

PLL Part

The purpose of the PLL part is to perform a phase lock of the voltage-controlled RF oscillator to an on-chip crystal reference oscillator. This is achieved by means of a special phase-noise-shaping technique based on the fractional-N principle which is already used in Atmel's U2733B frequency synthesizer series. It concentrates the phase detector's phase-noise contribution to the spectrum of the controlled VCO at frequency positions where it does not impair the quality of the received DAB signal. A special property of the transmission technique which is used in DAB is that the phase-noise-weighting function which measures the influence of the LO's phase noise to the phase information of the coded signal in a DAB receiver has zeros, i.e., if phase noise is concentrated in the position of such zeros as discrete lines, the DAB signal is not impaired as long as these lines do not exceed a set limit. For DAB mode I, this phase-noise-weighting function is shown in Figure 3.

Figure 3. Phase-noise-weighting Function



It is important to realize that this function shows zeros in all distances from the center line which are multiples of the carrier spacing. The technique of concentrating the phase noise in the positions of such zeros is patent protected.

Reference Oscillator

An on-chip crystal oscillator generates the reference signal which is fed to the reference divider. As already described in the section “IF Gain-controlled Amplifier/Mixer Combination” on page 7, the LO signal for the mixer in the IF section is derived. By applying a crystal to the pins OSCI, OSCO, see Figure 8 on page 20, this oscillator generates a highly stable reference signal. If an external reference signal is available, the oscillator can be used as an input buffer. In such an application, see Figure 9 on page 21, the reference signal has to be applied to the pin OSCI and the pin OSCO must be left open.

Reference Divider

Starting from a minimum value, the scaling factor SFref of the 9-bit reference divider is freely programmable by means of the two-wire bus bits ri (i = 0, ..., 8) according to

$$SF_{ref} = \sum r_i \times 2^i$$

If, for example, a frequency raster of 16 kHz is requested, the scaling factor of the reference divider has to be specified in such a way that the division process results in an output frequency which is four times higher than the desired frequency raster, i.e., the comparison frequency of the phase detector equals four times the frequency raster. By changing the division ratio of the main divider from N to N+1 in an appropriate way (fractional-N technique), this frequency raster is interpolated to deliver a frequency spacing of 16 kHz. So effectively a reference scaling divide factor

$SF_{ref,eff} = 4 \times \sum r_i \times 2^i$ is achieved.

By setting, the two-wire bus bit T, a test signal representing the divided input signal can be monitored at the switching output SWA.

Main Divider

The main divider consists of a fully programmable 13-bit divider which defines a division ratio N. The applied division ratio is either N or N+1 according to the control of a special control unit. On average, the scaling factors SF = N + k/4 can be selected where k = 0, 1, 2 or 3.

In this way, VCO frequencies $f_{VCO} = 4 \times (N+k/4) \times f_{ref}/(4 \times SF_{ref})$ can be synthesized starting from a reference frequency fref. If we define $SF_{eff} = 4 \times N + k$ and $SF_{ref,eff} = 4 \times SF_{ref}$ (previous section), then $f_{VCO} = SF_{eff} \times f_{ref}/SF_{ref,eff}$, where SF_{eff} is defined by 15 bits.

In the following, this circuit is described in terms of SF_{eff} and $SF_{ref,eff}$. SF_{eff} has to be programmed via the two-wire bus interface. An effective scaling factor from 2048 to 32767 can be selected by means of the two-wire bus bits ni (i = 0, ..., 14) according to

$SF_{eff} = \sum n_i \times 2^i$

By setting the two-wire bus bit T, a test signal representing the divided input signal can be monitored at the switching output SWC.

When the supply voltage is switched on, both the reference divider and the programmable divider are kept in RESET state until a complete scaling factor is written onto the chip. Changes in the setting of the programmable divider become active when the corresponding two-wire bus transmission is completed. An internal synchronization procedure ensures that such changes do not become active while the charge pump is sourcing or sinking current at its output pin. This behavior allows a smooth tuning of the output frequency without restricting the controlled VCO's frequency spectrum.

Phase Comparator and Charge Pump

The tri-state phase detector causes the charge pump to source or to sink current at the output Pin PD depending on the phase relation of its input signals which are provided by the reference and the main divider respectively. Four different values of this current can be selected by means of the two-wire bus bits I50 and I100. By use of this option, changes of the loop characteristics due to the variation of the VCO gain as a function of the tuning voltage can be reduced. The charge-pump current can be switched off using the two-wire bus bit TRI. A change in the setting of the charge pump current becomes active when the corresponding two-wire bus transmission is completed. As described for the setting of the scaling factor of the programmable divider, an internal synchronization procedure ensures that such changes do not become active while the charge pump is sourcing or sinking current at its output pin. This behavior allows a change in the charge pump current without restricting the controlled VCO's frequency spectrum.

A high-gain amplifier (output pin: VD), which is implemented in order to construct a loop filter, as shown in the application circuit, can be switched off by means of the two-wire bus bit OS.

An internal lock detector checks if the phase difference of the input signals of the phase detector is smaller than approximately 250 ns in seven subsequent comparisons. If phase lock is detected, the open collector output pin PLCK is set to H (logical value). It should be noted that the output current of this pin must be limited by external circuitry as it is not limited internally. If the two-wire bus bit TRI is set to H, the lock detector function is deactivated and the logical value of the PLCK output is undefined.

Switching Outputs

Three switching outputs controlled by the two-wire bus bits SWA, SWB, SWC can be used for any switching task on the front-end board. The currents of these outputs are not limited internally. They have to be limited by an external circuit.

D/A Converters

Three D/A converters, A, B and C, offer the possibility of generating three output voltages at a resolution of 8 bits. These voltages appear at the output pins CAO, CBO and CCO. The converters are controlled via the two-wire bus interface by means of the control bits CA0, ..., CA7, CB0, ..., CB7 and CC0, ..., CC7 respectively as described in the section “Two-wire Bus Instruction Codes”. The output voltages are defined as

$$V_{CAO} = \frac{V_M}{128} \times \sum_{j=0}^{7} CAj \times 2^j$$

$$V_{CBO} = \frac{V_M}{128} \times \sum_{j=0}^{7} CBj \times 2^j$$

$$V_{CCO} = \frac{V_M}{128} \times \sum_{j=0}^{7} CCj \times 2^j$$

where VM = 4.25 V nominally. Due to the rail-to-rail outputs of these converters, almost the full voltage range from 0 to 8.5 V can be used. A common application of these converters is the digital synthesis of control signals for the tuning of preselectors. The output pins CAU, CBO and CCO must be blocked externally with capacitors (100 nF) as shown in the application circuit (see Figure 8 on page 20).

Simple Two-wire Bus Interface

Via its two-wire bus interface, various functions can be controlled by a microprocessor. These functions are outlined in the following table “Simple Two-wire Bus Instruction Codes” on page 11 and in the section “Simple Two-wire Bus Functions” on page 11. The programming information is stored in a set of internal registers. By means of the Pin ADR, two different two-wire bus addresses can be selected as described in the section “Electrical Characteristics”. In Figure 6 on page 19, the two-wire bus timing parameters are explained, Figure 7 on page 20 shows a typical two-wire bus pulse diagram.

Table 3. Simple Two-wire Bus Instruction Codes

Description	MSB							LSB
Address	1	1	0	0	0	AS1	0	0
A byte 1	0	0	X	X	X	n_{14}	n_{13}	n_{12}
A byte 2	X	X	n_{11}	n_{10}	n_9	n_8	n_7	n_6
A byte 3	X	X	n_5	n_4	n_3	n_2	n_1	n_0
B byte 1	0	1	X	r_8	TA3	TA2	TA1	TA0
B byte 2	r_7	r_6	r_5	r_4	TB3	TB2	TB1	TB0
B byte 3	r_3	r_2	r_1	r_0	TC3	TC2	TC1	TC0
C byte 1	1	0	X	X	X	X	X	X
C byte 2	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
C byte 3	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
D byte 1	1	1	0	OS	T	TRI	I100	I50
D byte 2	SWA	SWB	SWC	X	M3	M2	M1	M0
D byte 3	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0

Simple Two-wire Bus Functions

AS1 — Defines the two-wire bus address

n_i — Deffective scaling factor (SFeff) of the main divider $SF_{eff} = \sum n_i \times 2^i$

r_i — Scaling factor ($SF_{ref,eff}$) of the reference divider $SF_{ref,eff} = 4 \times r_i\, 2^i$

TAi — Define the setting of a 4-bit D/A converter controlling the threshold, th1, of the RF AGC to adjust the controlled output power

TBi — Define the setting of a 4-bit D/A converter controlling the threshold, th2, which determines the activation voltage for the internal RF AGC

TCi — Define the setting of a 4-bit D/A converter controlling the threshold, th3, of the IF AGC to adjust the output power

CAi, CBi, CCi — Define the setting of the three D/A converters A, B and C (i = 0, ..., 7)

OS — OS = HIGH switches off the tuning output

T — For T = HIGH, reference signals describing the output frequencies of the reference divider and programmable divider are monitored at SWA (reference divider) and SWC (programmable divider).

TRI — TRI = HIGH switches off the charge pump

I50 and I100 define the charge pump current:

Table 4. Current of Charge Pump

I50	I100	Charge-pump Current (nominal)/µA
LOW	LOW	50
HIGH	LOW	100
LOW	HIGH	150
HIGH	HIGH	200

Mi defines the operation mode:

Table 5. Mode Selection

M3	M2	M1	M0	Mode
LOW	LOW	X	X	$f_{LO,IFMIX} = f_{ref}$
LOW	HIGH	X	X	$f_{LO,IFMIX} = 2 \times f_{ref}$
HIGH	HIGH	X	X	IF mixer switched off
X	X	LOW	LOW	RF mixer A active, $f_{LO,RFMIX} = f_{VCO}$
X	X	HIGH	LOW	RF mixer B active, $f_{LO,RFMIX} = f_{VCO}$
X	X	HIGH	HIGH	RF mixer B active, $f_{LO,RFMIX} = f_{VCO}/2$

Note: SWα = HIGH switches on the output current (α = A, B, C)

Simple Two-wire Bus Data Transfer

Format:

START - ADR - ACK - <instruction set> - STOP

The <instruction set> consists of a sequence of A bytes, B bytes, C bytes and D bytes each followed by ACK. Always a triplet of these bytes (A, B, C or D) has to be completed before a new triplet is started. If no new triplet is started the transmission can be finished before the current triplet is finished.

Examples:

START - ADR - ACK - DB1 - ACK - DB2 - ACK - DB3 - ACK - CB1 - ACK - CB2 - ACK - CB3 - ACK - AB1 - ACK - AB2 - ACK - AB3 - ACK - BB1 - ACK - BB2 - ACK - BB3 - ACK - STOP

START - ADR - ACK - CB1 - ACK - CB2 - ACK - STOP

However:

START - ADR - ACK - DB1 - ACK - CB1 -ACK - STOP is not allowed.

Description:

START	Start condition
STOP	Stop condition
ACK	Acknowledge
ADR	Address byte
αBi	α byte i (α = A, B, C, D; i = 1, 2, 3)

Simple Two-wire Bus Timing

The values of the periods shown are specified in the table “Electrical Characteristics” on page 15. More detailed information can be taken from the “Application Note 1.0 (Two-wire Bus Description)”. Please note, that due to the two-wire bus specification, the MSB of a byte is transmitted first, the LSB last.

Figure 4. Two-wire Bus Timing

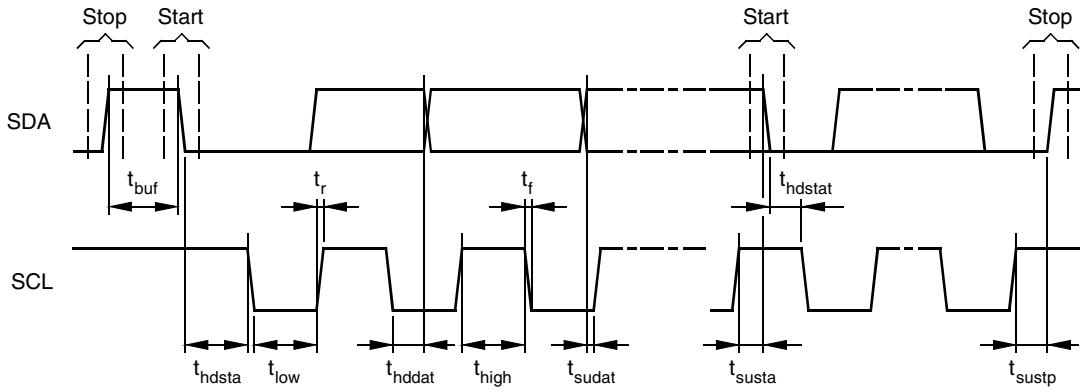
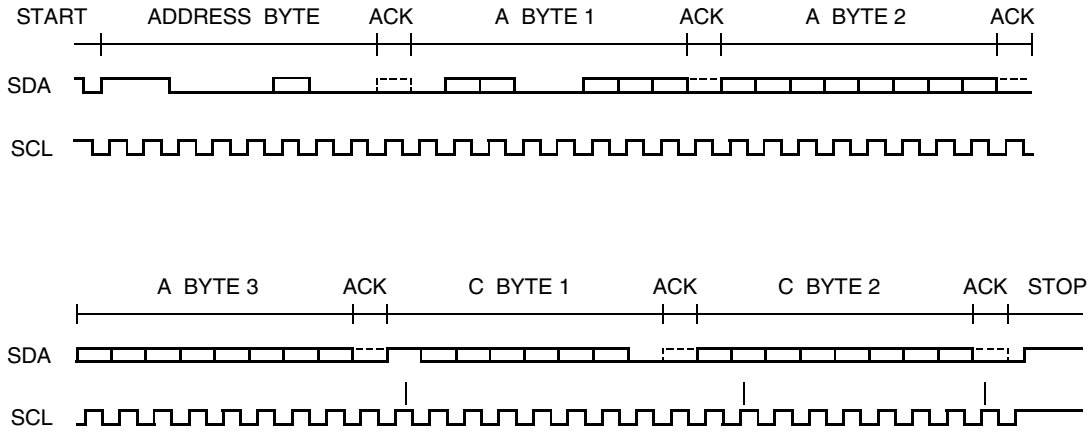


Figure 5. Typical Pulse Diagram



Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit
Supply voltage	V_S	-0.3	+9.5	V
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	-40	+150	°C
Differential input RF amplifier, pins 12 and 13	$V_{RFA1,2}$		500	mV_{rms}
Pins 14 and 15	$V_{RFB1,2}$		500	mV_{rms}
Externally applied voltage at RF charge pump output, pin 16	V_{CPRF}	0.5	6.75	V
Pin 28	V_{CPIF}	0.5	6.25	V
WAGC input voltage, pin 22	V_{WAGC}	-0.3	5.5	V
SLI input voltage, pin 21	V_{SLI}	-0.3	5.5	V
Differential base input VCO, pins 33 and 34	V_{BiVC}		500	mV_{rms}
Differential input IF amplifier, pins 23 and 24	V_{IFIN}		500	mV_{rms}
Differential input IF AGC block, pins 26 and 27	$V_{IFAGCIN}$		500	mV_{rms}
Reference input voltage (AC), pin 42	V_{OSCI}		1	V_{pp}
Two-wire bus input/output voltage, pins 1 and 2	SCL, SDA	-0.3	5.5	V
SDA output current, pin 2	SDA		5	mA
Address select voltage, pin 44	ADR	-0.3	5.5	V
Switch output voltage; pins 3, 4 and 6	SWα	-0.3	9.5	V
Switch output current	SWα		4	mA
PLCK output voltage, pin 41	PLCK	-0.3	5.5	V
PLCK output current, pin 41	PLCK		0.5	mA

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient (soldered on application board)	R_{thJA}	40	K/W

Operating Range

Parameters	Symbol	Value	Unit
Supply voltage	V_S	8.0 to 9.35	V
Ambient temperature range	T_{amb}	-40 to +85	°C

Electrical Characteristics

Test conditions (unless otherwise specified): V_S = 8.5 V, T_{amb} = 25°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**Overall Characteristics**		**20, 25, 38**						
1.1	Supply voltage			V_S	8.0	8.5	9.35	V	
1.2	Minimum supply current	V(CPRF) = V(CPIF) < 0.8 V M3 = M2 = HIGH M1 = M0 = LOW TAi = TCi = 0000; TBi = 1000 SWA = SWB = SWC = LOW TRI = LOW; PLCK = LOW I100 = I50 = LOW; V(ADR) = open SLI = LOW; WAGC = HIGH		$I_{S,min}$		74		mA	B
1.3	Maximum supply current	3.4 V < V(CPRF) = V(CPIF) < 3.6 V; M3 = M2 = HIGH M1 = M0 = LOW TAi = TCi = 0000; TBi = 1000 SWA = LOW; SWB = LOW SWC = LOW; TRI = LOW PLCK = LOW; I100 = I50 = LOW V(ADR) = open; SLI = LOW WAGC = HIGH		$I_{S,max}$		79		mA	B
2	**RF Part**								
2.1	Voltage gain	RFA1, RFA2; RFB1, RFB2) → SAW1, SAW2 (see Figure 9 on page 21)	12 (14) →18, 19	$G_{V,RF}$	20	24	26	dB	A
2.2	AGC range RF				23	27	29	dB	A
2.3	Noise figure (double side band)	RFA1, (RFB1) →SAW1, SAW2; RFA2, RFB2 blocked	12 (14) →19	$NF_{DSB,RF}$		12		dB	D
2.4	Maximum input power level	Differential, 3rd order intermodulation distance ≥ 40 dBc, Pout = -19 dBm, TAi = 0000, RL (SAW1, SAW2) = 200 Ω	12, 13 (14, 15)	$P_{in,max,MIX}$	-10			dBm	A
2.5	Input frequency range		12, 13 (14, 15)	$f_{in,RF}$	70		260	MHz	B
2.6	Input impedance	Single ended	12 (14)	$Z_{in,RF}$		1.3		kΩ	D
2.7	Output frequency range for AGC-voltage generation		18, 19	$f_{out,SAW}$		38,912 ±5		MHz	D
2.8	Maximum output power level	Output power, differential; RL (SAW1, SAW2) > 200 Ω, TAi = 0000	18, 19			-7		dBm	D
2.9	AGC threshold (th1) TAi = '1000' TAi = '1111' TAi = '0000'	Output power, differential controlled by two-wire bus bits TAi; RL (SAW1, SAW2) = 200 Ω	18, 19	$p_{TH,RF}$	50	90 160 10	120	mV_{rms}	A B B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. The phase detector's phase-noise contribution to the VCO's frequency spectrum is determined by the operating frequency of the phase detector divided by 4 according to the fractional-N technique (regularly: 16 kHz).

Electrical Characteristics (Continued)

Test conditions (unless otherwise specified): V_S = 8.5 V, T_{amb} = 25°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
2.10	AGC threshold (th2) (internal AGC) upper limit (TBi = 1111) lower limit (TBi = 0000)	Controlled by two-wire bus bits TBi; $P_{IN,MAX}$ = -25 dBm	16	$V_{int\ AGC,RF}$	 1.0	 5.1 1.5	 1.8	 V V	 B A
2.11	Output impedance	Single ended; f(SAW1) = 39 MHz	18 (19)	$Z_{out,SAW}$		30		Ω	
3	**VCO**								
3.1	Phase noise	Δf = 10 kHz		L(f)		-88		dBc/Hz	D
3.2	Phase noise			f_{LO}	100		400	MHz	D
4	**IF Part**								
4.1	Voltage gain	IFIN2 blocked (see Figure 9 on page 21) $f_{LO,IFMIX} = f_{ref}$ or $F_{LO,IFMIX} = 2 \times f_{ref}$	24 →29	$G_{V,tot}$	42	44	48	dB	A
4.2	Voltage gain	IFIN2 blocked (see Figure 9 on page 21) IF mixer switched off	24 →29	$G_{V,tot}$	45	47	51	dB	A
4.3	AGC range IF				42	44	48	dB	A
4.4	Noise figure (double side band)	IFIN2 blocked	24 →29	NF_{DSB}		11		dB	D
4.5	Maximum input power level	IFIN2 blocked, 3rd order intermodulation distance ≥ 40 dBc; RL(IFOUT) = 1 k; TCi = 0000; R_{10} = 4.7 k, R_{11} = 1.8 k	24	$P_{in,max}$	-20			dBm	C
4.6	Input frequency range		23, 24	$f_{in,IFIN}$	10		60	MHz	D
4.7	Input impedance	IFIN2 blocked, $f_{IF,IFIN}$ = 38.912 MHz	23, 24	$Z_{in,IFIN}$		600 - j1000		Ω	D
4.8	Output frequency range	Single ended	29	$f_{out,IFO}$	1		45	MHz	D
4.9	Output impedance	Single ended $f_{out,IFO}$ (3 MHz) $f_{out,IFO}$ (20 MHz) $f_{out,IFO}$ (38.9 MHz)	29	$Z_{out,IFOUT}$		 20 + j50 65 + j35 58 - j25		 Ω Ω Ω	D
5	**RF AGC Unit**								
5.1	Positive charge pump current, fast mode	V_{WAGC} = LOW V_{SLI} = HIGH	16	$ICPRF_{POS,FM}$	145	180	220	µA	A
5.2	Negative charge pump current, fast mode	V_{WAGC} = LOW V_{SLI} = HIGH	16	$ICPRF_{NEG,FM}$	-220	-180	-145	µA	A
5.3	Positive charge pump current, slow mode	V_{WAGC} = LOW V_{SLI} = LOW	16	$ICPRF_{POS,SM}$	30	40	52	µA	A
5.4	Negative charge pump current, fast mode	V_{WAGC} = LOW V_{SLI} = LOW	16	$ICPRF_{NEG,FM}$	-52	-40	-30	µA	A
5.5	Minimum gain control voltage			$VAGC_{min}$		0.75		V	C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. The phase detector's phase-noise contribution to the VCO's frequency spectrum is determined by the operating frequency of the phase detector divided by 4 according to the fractional-N technique (regularly: 16 kHz).

Electrical Characteristics (Continued)

Test conditions (unless otherwise specified): V_S = 8.5 V, T_{amb} = 25°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
5.6	Maximum gain control voltage			$VAGC_{max}$		6.6		V	C
6	**IF AGC Unit**								
6.1	Positive charge pump current, fast mode	V_{WAGC} = LOW V_{SLI} = HIGH	28	$ICPIF_{POS,FM}$	145	180	220	µA	A
6.2	Negative charge pump current, fast mode	V_{WAGC} = LOW V_{SLI} = HIGH	28	$ICPIF_{NEG, FM}$	-220	-180	-145	µA	A
6.3	Positive charge pump current, slow mode	V_{WAGC} = LOW V_{SLI} = LOW	28	$ICPIF_{POS, SM}$	30	40	52	µA	A
6.4	Negative charge pump current, slow mode	V_{WAGC} = LOW V_{SLI} = LOW	28	$ICPIF_{NEG, SM}$	-52	-40	-30	µA	A
6.5	Window AGC mode charge pump current	V_{WAGC} = HIGH	28	$ICPIF_{WAGC}$	-4	0	+4	µA	A
6.6	Minimum gain control voltage		28	$VAGCIF_{min}$		0.75		V	C
6.7	Maximum gain control voltage		28	$VAGCIF_{max}$		5.9		V	C
6.8	Control voltage for activated WAGC	WAGC = HIGH	22	$VWAGC_{High}$	2.0			V	A
6.9	Control voltage for deactivated WAGC	WAGC = LOW	22	$VWAGC_{Low}$			0.7	V	A
6.10	Control voltage for activated SLI	SLI = HIGH	21	$VSLI_{High}$	2.0			V	A
6.11	Control voltage for deactivated SLI	SLI = LOW	21	$VSLI_{Low}$			0.7		A
7	**PLL Part**								
7.1	Effective scaling factor of programmable divider			SF_{eff}	2048		32766		D
7.2	Effective scaling factor of reference divider			$SF_{ref,eff}$	144		2047		D
7.3	Tuning step					16		kHz	D
8	**REF Input**		**42**						
8.1	Input frequency range	Internal oscillator overdriven		f_{ref}	5		30	MHz	B
8.2	Input sensitivity	Internal oscillator overdriven		$v_{ref,min}$			50	mV_{rms}	A
8.3	Maximum input signal	Internal oscillator overdriven		$v_{ref,max}$	300			mV_{rms}	D
8.4	Input impedance	Single ended		Z_{ref}		2 || 2.5		kΩ/pF	D
9	**REF Output**		**5**						
9.1	Output voltage	1.5 kΩ || 2.5 pF load		$v_{out,ref}$	65	100		mV_{rms}	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. The phase detector's phase-noise contribution to the VCO's frequency spectrum is determined by the operating frequency of the phase detector divided by 4 according to the fractional-N technique (regularly: 16 kHz).

Electrical Characteristics (Continued)

Test conditions (unless otherwise specified): V_S = 8.5 V, T_{amb} = 25°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
10	**Phase Detector**		**39**						
10.1	Charge-pump current	I100 = HIGH, I50 = HIGH		$\|I_{PD4}\|$	160	200	240	µA	A
10.2		I100 = HIGH, I50 = LOW		$\|I_{PD3}\|$	120	150	180	µA	A
10.3		I100 = LOW, I50 = HIGH		$\|I_{PD2}\|$	80	100	120	µA	A
10.4		I100 = LOW, I50 = LOW		$\|I_{PD1}\|$	35	50	65	µA	A
10.5	High impedance mode	TRI = HIGH		$I_{PD,tri}$	-100		100	nA	A
10.6	Effective phase noise[1]	I_{PD} = 203 mA		L_{PD}		-159		dBc/ Hz	C
11	**Lock Indication**		**41**						
11.1	Leakage current	V_{PLCK} = 5.5 V		$I_{PLCK,L}$			10	µA	A
11.2	Saturation voltage	I_{PLCK} = 0.25 mA		$V_{PLCK,sat}$			0.5	V	A
12	**Switches**		**3, 4, 6**						
12.1	Leakage current			$I_{SW,L}$			10	µA	A
12.2	Saturation voltage	I_{SW} = 0.25 mA		$V_{SW,sat}$			0.5	V	A
13	**Address Selection**		**44**						
13.1	AS1 = 0				0		0.1 V_S		C
13.2	AS1 = 1				0.4 V_S		0.6 V_S		C
14	**D/A Converters**		**7, 8, 9**						
14.1	Output voltage	Cα7 = HIGH Cα0 to Cα6 = LOW α = A, B, C		V_M	4.05	4.25	4.45	V	A
14.2	Variation of V_M	V_S = 8.00 to 9.35 V		$\Delta V_{M,VS}$	-50		50	mV	A
14.3	Variation of V_M	T_{amb} = -40 to +85° C		$\Delta V_{M,temp}$		±20		mV	C
14.4	Accuracy	VCαn-n V_M/128 n = 24 ... 232, α = A, B, C		$\Delta V_{C\alpha n}$	-70		70	mV	A
14.5	Maximum output current			I_{CAOmax} I_{CBOmax} I_{CCOmax}		20		µA	C
15	**Simple Two-wire Bus**		**1, 2**						
15.1	Input voltage SCL/SDA	HIGH			3		5.5	V	D
15.2	Input voltage SCL/SDA	LOW					1.5	V	D
15.3	Output voltage SDA (open collector)	I_{SDA} = 2 mA, SDA = LOW					0.4	V	D
15.4	SCL clock frequency				0.1		100	kHz	D
15.5	Rise time (SCL, SDA)			t_r			1	µs	D
15.6	Fall time (SCL; SDA)			t_f			300	µs	D
15.7	Time before new transmission can start			t_{buf}	4.7			µs	D

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. The phase detector's phase-noise contribution to the VCO's frequency spectrum is determined by the operating frequency of the phase detector divided by 4 according to the fractional-N technique (regularly: 16 kHz).

Electrical Characteristics (Continued)

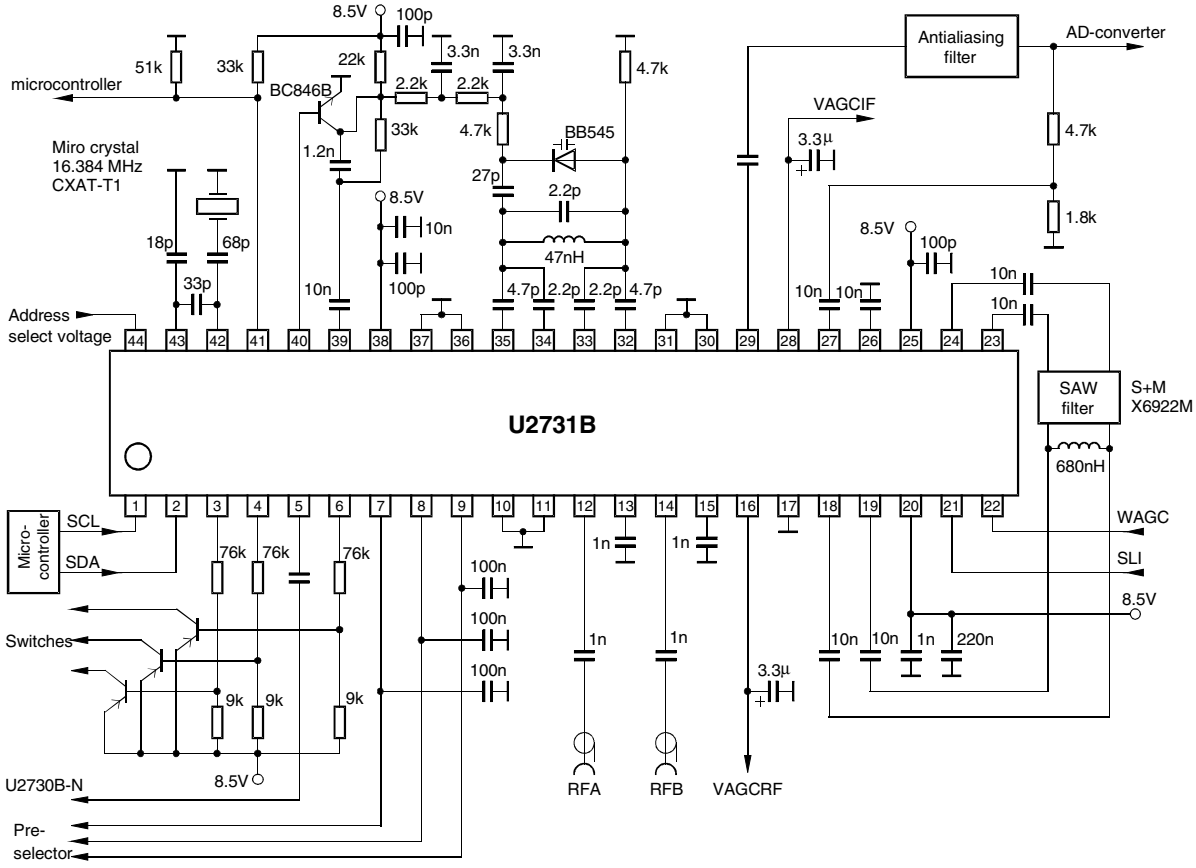
Test conditions (unless otherwise specified): V_S = 8.5 V, T_{amb} = 25°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
15.8	SCL HIGH period			t_{high}	4			µs	D
15.9	SCL LOW period			t_{low}	4.7			µs	D
15.10	Hold time START			t_{hdsta}	4			µs	D
15.11	Setup time START			t_{susta}	4.7			µs	D
15.12	Setup time STOP			t_{sustp}	4.7			µs	D
15.13	Hold time DATA			t_{hddat}	0			µs	D
15.14	Setup time DATA			t_{sudat}	250			ns	D

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. The phase detector's phase-noise contribution to the VCO's frequency spectrum is determined by the operating frequency of the phase detector divided by 4 according to the fractional-N technique (regularly: 16 kHz).

Figure 6. Application Circuit



Application Circuits of the Reference Oscillator

Figure 7. Oscillator Operation

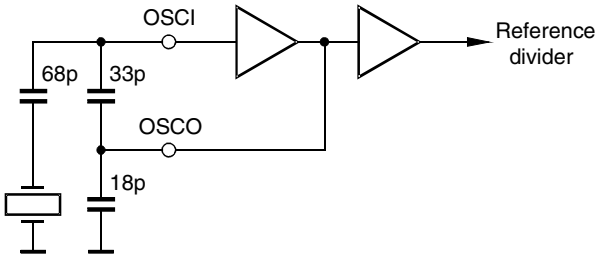


Figure 8. Oscillator Overdriven

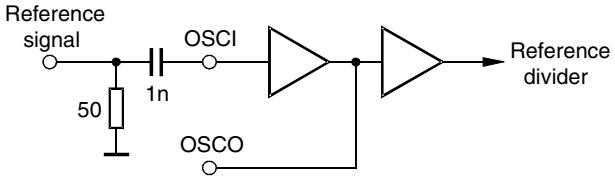


Figure 9. Measurement Circuit for Electrical Characteristics

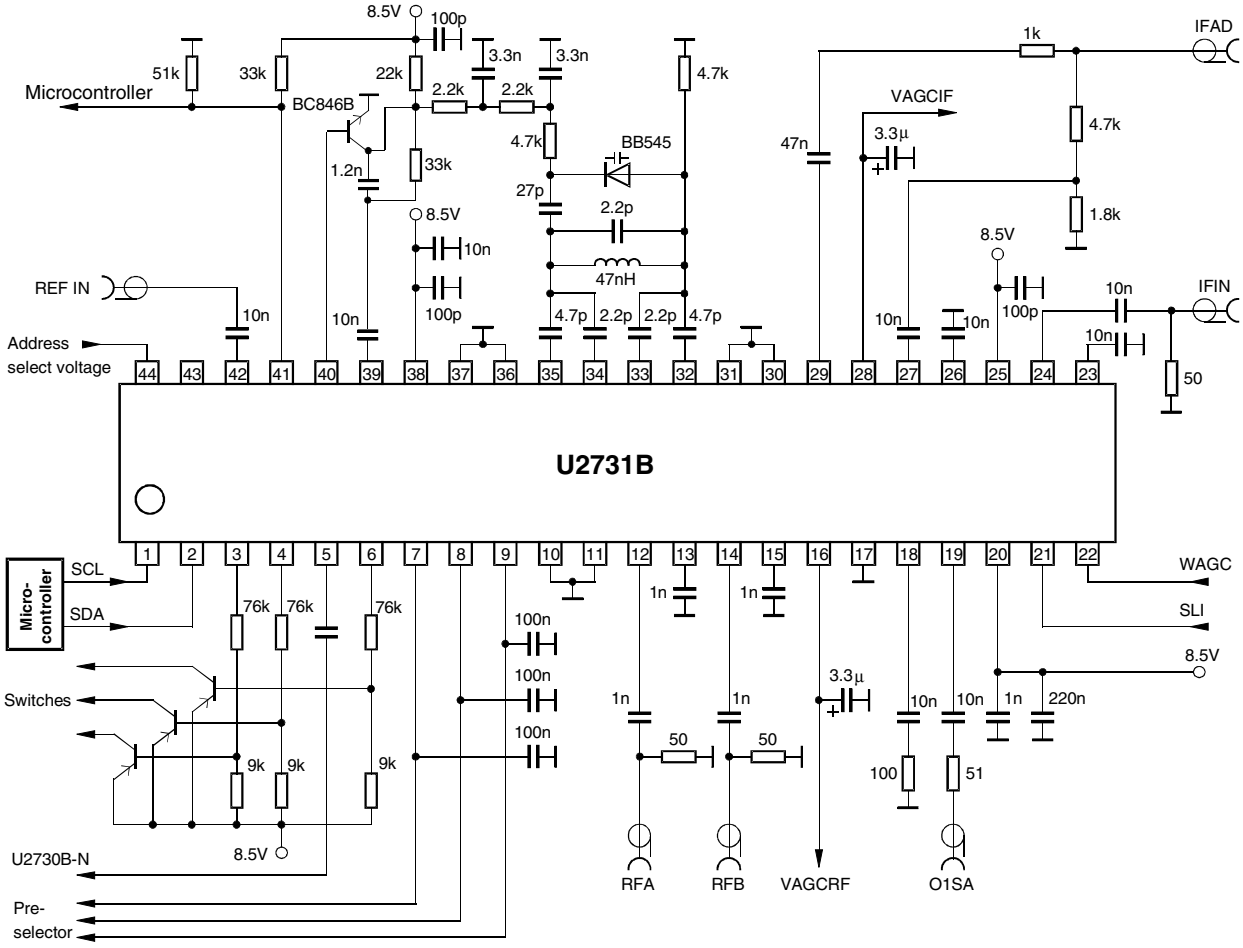


Figure 10. RFAGC Voltage-generation Block Circuit

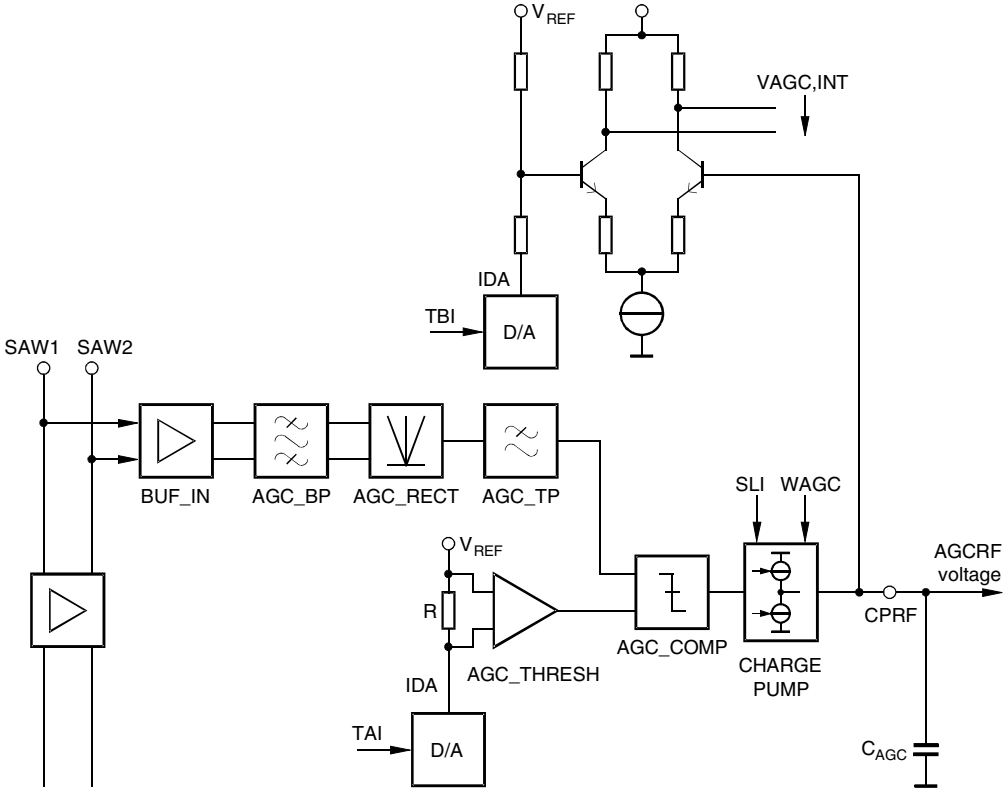


Figure 11. IFAGC Voltage-generation Block Circuit

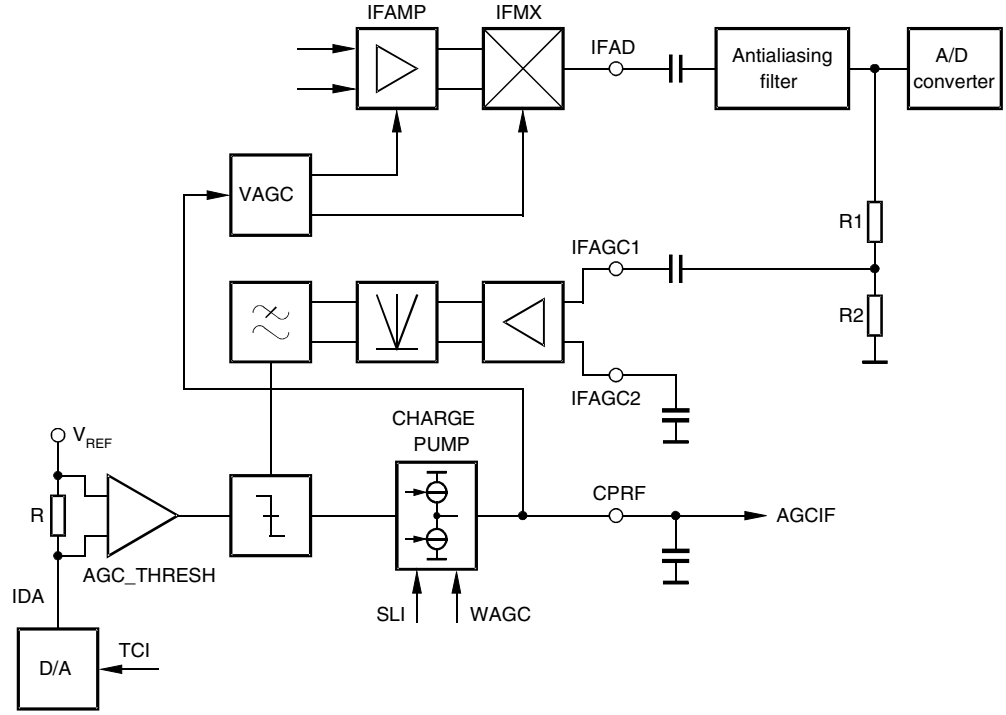
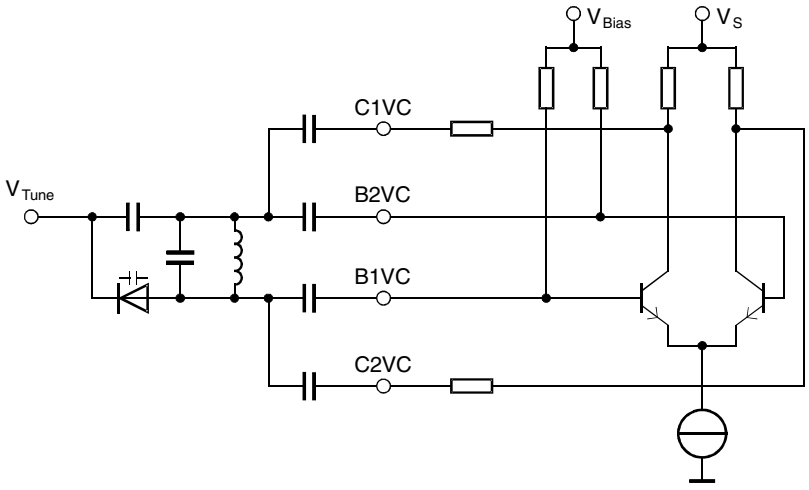


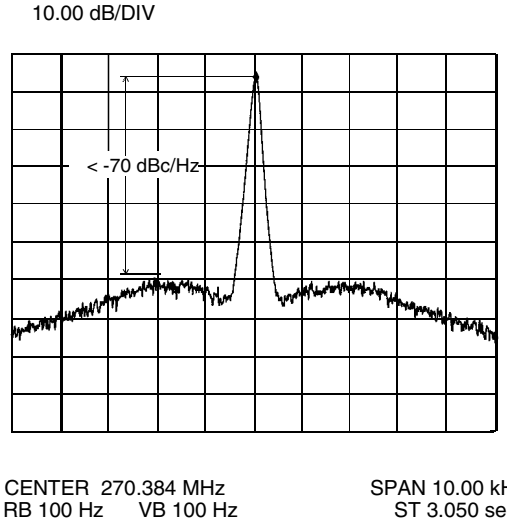
Figure 12. VCO Circuit

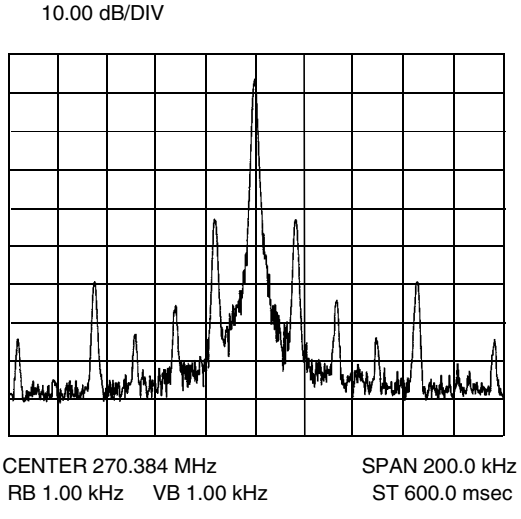


Phase-noise Performance

(Example: SF_{eff} = 16899, $SF_{ref,eff}$ = 1120, f_{ref} = 17.92 MHz, I_{PD} = 200 mA, spectrum analysis: HP7000)

Figure 13. Phase-noise Over Frequency





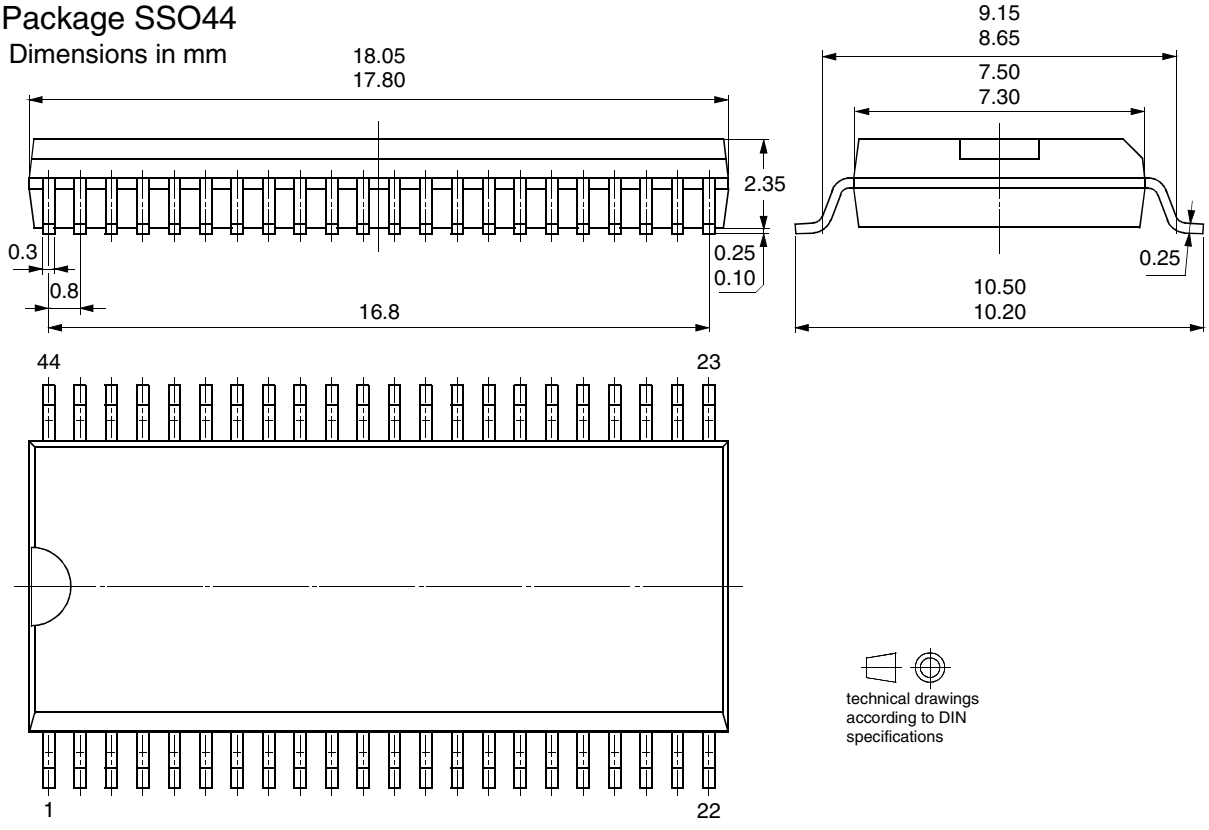
Ordering Information

Extended Type Number	Package	Remarks
U2731B–NFN	SSO44	Tube
U2731B–NFNG1	SSO44	Taped and reeled

Package Information

Package SSO44

Dimensions in mm



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