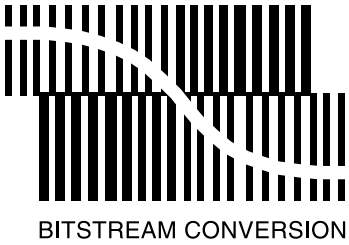
DATA SHEET



UDA1334TS
Low power audio DAC

Product specification
Supersedes data of 1999 Nov 11
File under Integrated Circuits, IC01

2000 Oct 25

Philips
Semiconductors

PHILIPS

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1 FEATURES

1.1 General

- 1.8 to 3.6 V power supply voltage
- Integrated digital filter plus DAC
- Supports sample frequencies from 8 to 100 kHz
- Automatic system clock versus sample rate detection
- Low power consumption
- No analog post filtering required for DAC
- Slave mode only applications
- Easy application
- SSOP16 package.

1.2 Multiple format data interface

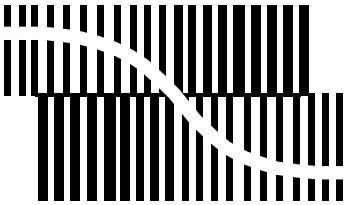
- I^2S-bus and LSB-justified format compatible
- $1f_s$ input data rate.

1.3 DAC digital sound processing

- Digital de-emphasis for 44.1 kHz sampling rate
- Mute function.

1.4 Advanced audio configuration

- High linearity, wide dynamic range and low distortion
- Standby or Sleep mode in which the DAC is powered down.



2 APPLICATIONS

This audio DAC is excellently suitable for digital audio portable application, such as portable MD, MP3 and DVD players.

3 GENERAL DESCRIPTION

The UDA1334TS supports the I^2S-bus data format with word lengths of up to 24 bits and the LSB-justified serial data format with word lengths of 16, 20 and 24 bits.

The UDA1334TS has basic features such as de-emphasis (at 44.1 kHz sampling rate) and mute.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1334TS	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1

5 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	DAC analog supply voltage		1.8	2.0	3.6	V
V_{DDD}	digital supply voltage		1.8	2.0	3.6	V
I_{DDA}	DAC analog supply current	normal operation	–	2.1	–	mA
		Sleep mode	–	150	–	µA
I_{DDD}	digital supply current	normal operation	–	1.2	–	mA
		Sleep mode	–	50	–	µA
T_{amb}	ambient temperature		–40	–	+85	°C
Digital-to-analog convertor (V_{DDA} = V_{DDD} = 2.0 V)						
$V_{o(rms)}$	output voltage (RMS value)	at 0 dB (FS) digital input; note 1	–	500	–	mV
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	f_s = 44.1 kHz; at 0 dB	–	–80	–	dB
		f_s = 44.1 kHz; at –60 dB; A-weighted	–	–37	–	dB
		f_s = 96 kHz; at 0 dB	–	–75	–	dB
		f_s = 96 kHz; at –60 dB; A-weighted	–	–35	–	dB
S/N	signal-to-noise ratio	f_s = 44.1 kHz; code = 0; A-weighted	–	97	–	dB
		f_s = 96 kHz; code = 0; A-weighted	–	95	–	dB
		MUTE = HIGH; A-weighted	–	110	–	dB
α_{cs}	channel separation		–	100	–	dB
Digital-to-analog convertor (V_{DDA} = V_{DDD} = 3.0 V)						
$V_{o(rms)}$	output voltage (RMS value)	at 0 dB (FS) digital input; note 1	–	750	–	mV
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	f_s = 44.1 kHz; at 0 dB	–	–90	–	dB
		f_s = 44.1 kHz; at –60 dB; A-weighted	–	–40	–	dB
		f_s = 96 kHz; at 0 dB	–	–85	–	dB
		f_s = 96 kHz; at –60 dB; A-weighted	–	–37	–	dB
S/N	signal-to-noise ratio	f_s = 44.1 kHz; code = 0; A-weighted	–	100	–	dB
		f_s = 96 kHz; code = 0; A-weighted	–	98	–	dB
		MUTE = HIGH; A-weighted	–	110	–	dB
α_{cs}	channel separation		–	100	–	dB
Power dissipation (at f_s = 44.1 kHz)						
P	power dissipation	at 2.0 V supply voltage	–	7.0	–	mW
		at 3.0 V supply voltage	–	17	–	mW
		Sleep mode; at 2.0V supply voltage				
		clock running	–	0.75	–	mW
		no clock running	–	0.3	–	mW

Note

1. The DAC output voltage scales proportional to the power supply voltage.

6 BLOCK DIAGRAM

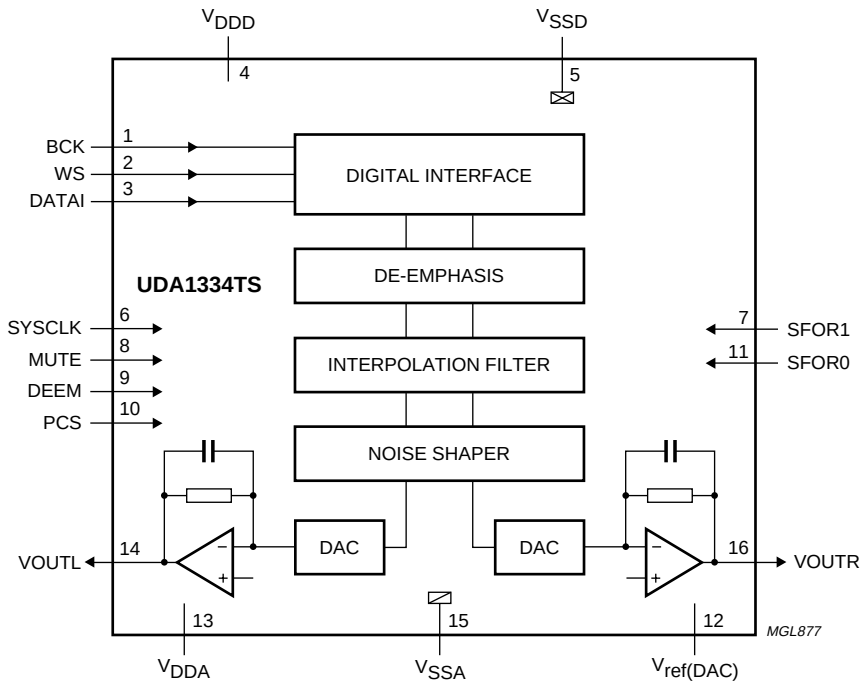


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	PAD TYPE	DESCRIPTION
BCK	1	5 V tolerant digital input pad; note 1	bit clock input
WS	2	5 V tolerant digital input pad; note 1	word select input
DATAI	3	5 V tolerant digital input pad; note 1	serial data input
V_{DDD}	4	digital supply pad	digital supply voltage
V_{SSD}	5	digital ground pad	digital ground
SYSCLK	6	5 V tolerant digital input pad; note 1	system clock input
SFOR1	7	5 V tolerant digital input pad; note 1	serial format select 1
MUTE	8	5 V tolerant digital input pad; note 1	mute control
DEEM	9	5 V tolerant digital input pad; note 1	de-emphasis control
PCS	10	3-level input pad; note 2	power control and sampling frequency select
SFOR0	11	digital input pad; note 2	serial format select 0
$V_{ref(DAC)}$	12	analog pad	DAC reference voltage
V_{DDA}	13	analog supply pad	DAC analog supply voltage
VOUTL	14	analog output pad	DAC output left
V_{SSA}	15	analog ground pad	DAC analog ground
VOUTR	16	analog output pad	DAC output right

Notes

1. 5 V tolerant is only supported if the power supply voltage is between 2.7 and 3.6 V. For lower power supply voltages this is maximum 3.3 V tolerant.
2. Because of test issues these pads are not 5 V tolerant and they should be at power supply voltage level or at a maximum of 0.5 V above that level.

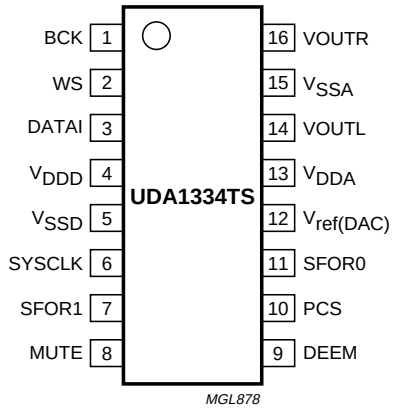


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

8.1 System clock

The UDA1334TS operates in slave mode only; this means that in all applications the system must provide the system clock and the digital audio interface signals (BCK and WS).

The system clock must be locked in frequency to the digital interface signals.

The UDA1334TS automatically detects the ratio between the SYSCLK and WS frequencies.

The BCK clock can be up to $64f_s$, or in other words the BCK frequency is 64 times the Word Select (WS) frequency or less: $f_{BCK} \leq 64 \times f_{WS}$.

Remarks

1. The WS edge MUST fall on the negative edge of the BCK at all times for proper operation of the digital I/O data interface.
2. For LSB-justified formats it is important to have a WS signal with a duty factor of 50%.

The modes which are supported are given in Table 1.

Table 1 Supported sampling ranges

CLOCK MODE	SAMPLING RANGE
$768f_s$	8 to 55 kHz
$512f_s$	8 to 100 kHz
$384f_s$	8 to 100 kHz
$256f_s$	8 to 100 kHz
$192f_s$	8 to 100 kHz[1][2]
$128f_s$	8 to 100 kHz[2]

Notes

1. This mode can only be supported for power supply voltages down to 2.4 V. For lower voltages, in $192f_s$ mode the sampling frequency should be limited to 55 kHz.
2. Not supported in low-sampling frequency mode.

An example is given in Table 2 for a 12.228 MHz system clock input.

Table 2 Example using a 12.228 MHz system clock

SAMPLING FREQUENCY	CLOCK MODE
96 kHz	$128f_s$
64 kHz[1]	$192f_s$
48 kHz	$256f_s$
32 kHz	$384f_s$
24 kHz	$512f_s$
16 kHz	$768f_s$

Note

1. This mode can only be supported for power supply voltages down to 2.4 V. For lower voltages, in $192f_s$ mode the sampling frequency should be limited to 55 kHz.

8.2 Interpolation filter

The interpolation digital filter interpolates from $1f_s$ to $64f_s$ by cascading FIR filters (see Table 3).

Table 3 Interpolation filter characteristics

ITEM	CONDITION	VALUE (dB)
Pass-band ripple	0 to $0.45f_s$	±0.02
Stop band	$>0.55f_s$	–50
Dynamic range	0 to $0.45f_s$	>114

8.3 Noise shaper

The 5th-order noise shaper operates at $64f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using an Filter Stream DAC (FSDAC).

8.4 Filter stream DAC

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. No post-filter is needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

The output voltage of the FSDAC scales proportional with the power supply voltage.

8.5 Power-on reset

The UDA1334TS has an internal Power-on reset circuit (see Fig.3) which resets the test control block.

The reset time (see Fig.4) is determined by an external capacitor which is connected between pin $V_{ref(DAC)}$ and ground. The reset time should be at least 1 µs for $V_{ref(DAC)} < 1.25$ V. When V_{DDA} is switched off, the device will be reset again for $V_{ref(DAC)} < 0.75$ V.

During the reset time the system clock should be running.

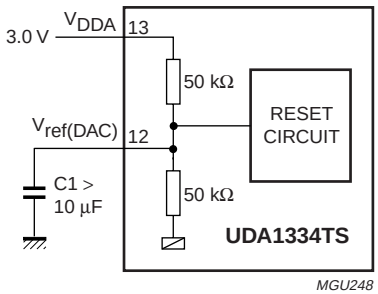


Fig.3 Power-on reset circuit.

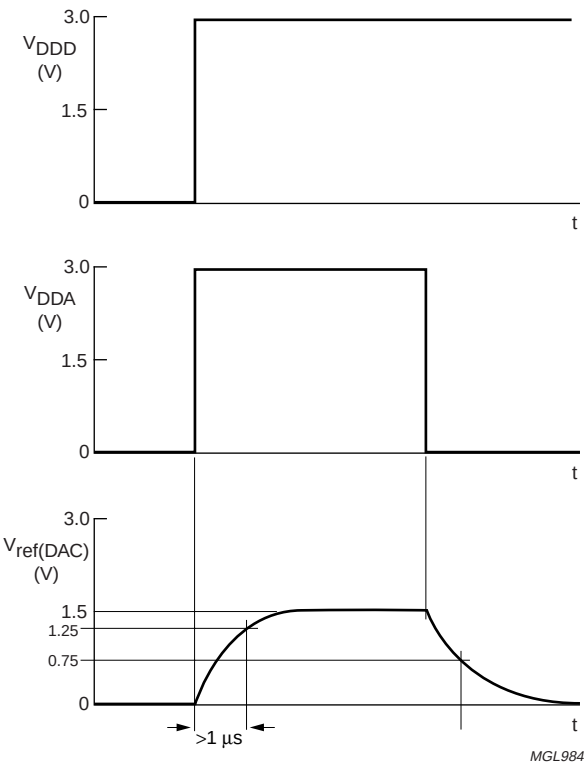


Fig.4 Power-on reset timing.

8.6 Feature settings

The features of the UDA1334TS can be set by control pins SFOR1, SFOR0, MUTE, DEEM and PCS.

8.6.1 Digital interface format select

The digital audio interface formats (see Fig.5) can be selected via the pins SFOR1 and SFOR0 as shown in Table 4.

The BCK frequency for the digital audio interface can be maximum 64 times the WS frequency: $f_{BCK} \leq 64f_{WS}$.

Table 4 Data format selection

SFOR1	SFOR0	INPUT FORMAT
LOW	LOW	I^2S-bus input
LOW	HIGH	LSB-justified 16 bits input
HIGH	LOW	LSB-justified 20 bits input
HIGH	HIGH	LSB-justified 24 bits input

8.6.2 Mute control

The output signal can be soft muted by setting pin MUTE to HIGH level as shown in Table 5.

Table 5 Mute control

MUTE	FUNCTION
LOW	mute off
HIGH	mute on

When the output signal is fully muted (pin MUTE at HIGH level), a silence switch inside the FSDAC is activated. In this way a very high signal-to-noise ratio can be achieved in case the output is muted.

8.6.3 De-emphasis control

De-emphasis can be switched on for f_s = 44.1 kHz by setting pin DEEM at HIGH level. The function description of pin DEEM is given in Table 6.

Table 6 De-emphasis control

DEEM	FUNCTION
LOW	de-emphasis off
HIGH	de-emphasis on

8.6.4 Power control and sampling frequency select

Pin PCS is a 3-level pin and is used to set the mode of the UDA1334TS. The definition is given in Table 7.

Table 7 PCS function definition

PCS	FUNCTION
LOW	normal operating mode
MID	low sampling frequency mode
HIGH	Power-down or Sleep mode

The low sampling frequency mode is required to have a higher oversampling rate in the noise shaper in order to improve the signal-to-noise ratio. In this mode the oversampling ratio of the noise shaper will be $128f_s$ instead of $64f_s$.

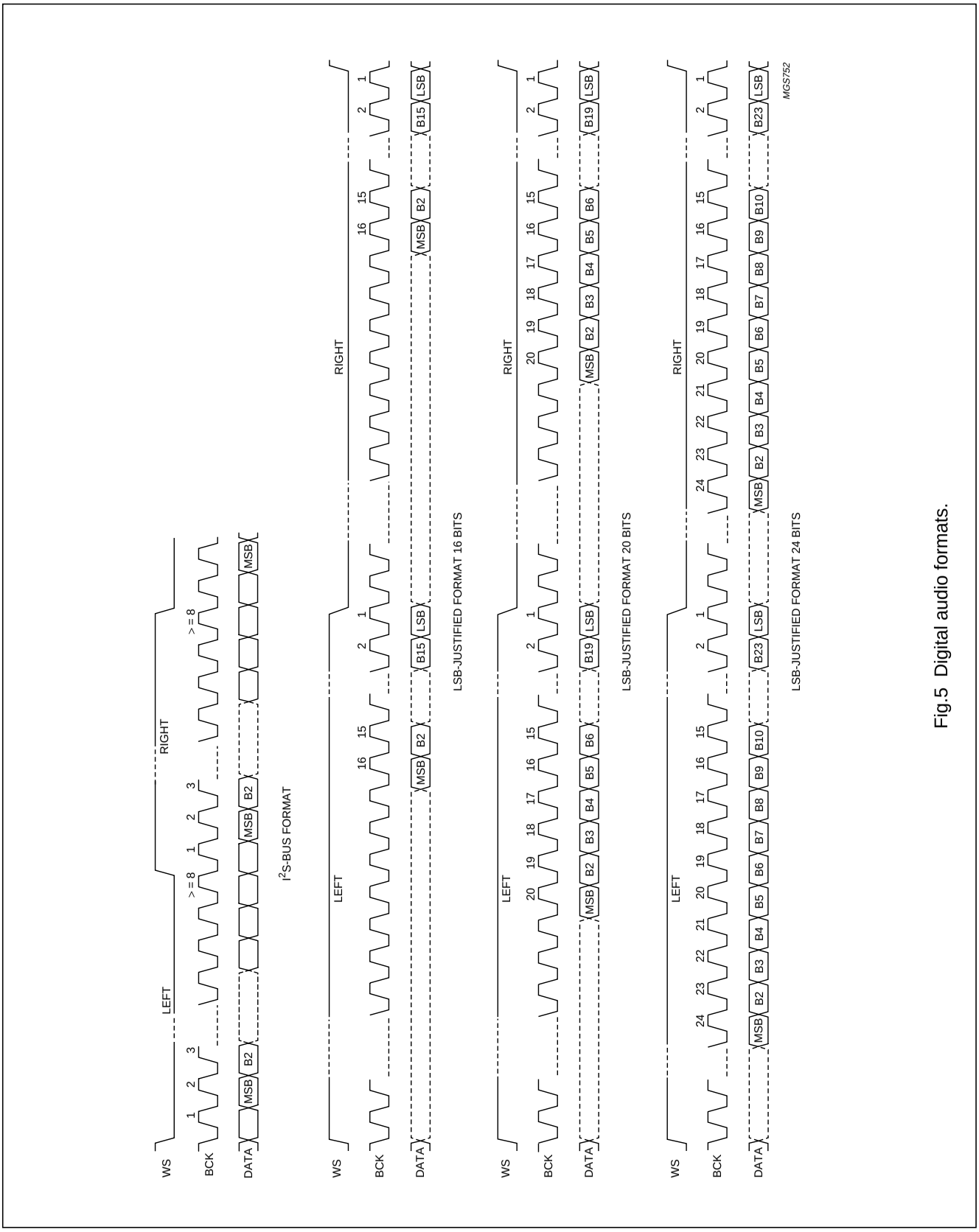


Fig.5 Digital audio formats.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	note 1	–	4.0	V
$T_{xtal(max)}$	maximum crystal temperature		–	150	°C
T_{stg}	storage temperature		–65	+125	°C
T_{amb}	ambient temperature		–40	+85	°C
V_{es}	electrostatic handling voltage	human body model	–2000	+2000	V
		machine model	–200	+200	V

Note

1. All supply connections must be made to the same power supply.

10 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices.

11 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	145	K/W

12 QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611-E"*.

13 DC CHARACTERISTICS

$V_{DDD} = V_{DDA} = 2.0$ V; $T_{amb} = 25$ °C; $R_L = 5$ kΩ. All voltages with respect to ground (pins V_{SSA} and V_{SSD}); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	DAC analog supply voltage	note 1	1.8	2.0	3.6	V
V_{DDD}	digital supply voltage	note 1	1.8	2.0	3.6	V
I_{DDA}	DAC analog supply current	normal operating mode; at 2.0 V supply voltage	–	2.1	–	mA
		normal operating mode; at 3.0 V supply voltage	–	3.3	–	mA
		Sleep mode	–	150	–	μA
I_{DDD}	digital supply current	normal operating mode; at 2.0 V supply voltage	–	1.2	–	mA
		normal operating mode; at 3.0 V supply voltage	–	2.1	–	mA
		Sleep mode	–	50	–	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital input pins; note 2						
V_{IH}	HIGH-level input voltage	at 2.0 V supply voltage	1.3	–	3.3	V
		at 3.0 V supply voltage	2.0	–	5.0	V
V_{IL}	LOW-level input voltage	at 2.0 V supply voltage	–0.5	–	+0.5	V
		at 3.0 V supply voltage	–0.5	–	+0.8	V
$\|I_{LI}\|$	input leakage current		–	–	1	μA
C_i	input capacitance		–	–	10	pF
3-level input: pin PCS						
V_{IH}	HIGH-level input voltage		$0.9V_{DDD}$	–	V_{DDD}	V
V_{IM}	MID-level input voltage		$0.4V_{DDD}$	–	$0.6V_{DDD}$	V
V_{IL}	LOW-level input voltage		0	–	0.5	V
DAC						
$V_{ref(DAC)}$	reference voltage	with respect to V_{SSA}	$0.45V_{DD}$	$0.5V_{DD}$	$0.55V_{DD}$	V
$R_{O(ref)}$	$V_{ref(DAC)}$ reference output resistance		–	12.5	–	kΩ
$I_{o(max)}$	maximum output current	(THD + N)/S < 0.1%; R_L = 800 Ω	–	0.88	–	mA
R_L	load resistance		3	–	–	kΩ
C_L	load capacitance	note 3	–	–	50	pF

Notes

1. All supply connections must be made to the same external power supply unit.
2. At 3 V supply voltage, the input pads are TTL compatible. However, at 2.0 V supply voltage no TTL levels can be accepted, but levels from 3.3 V domain can be applied to the pins.
3. When the DAC drives a capacitive load above 50 pF, a series resistance of 100 Ω must be used to prevent oscillations in the output operational amplifier.

14 AC CHARACTERISTICS

14.1 2.0 V supply voltage

$V_{DDD} = V_{DDA}$ = 2.0 V; f_i = 1 kHz; T_{amb} = 25 °C; R_L = 5 kΩ. All voltages with respect to ground (pins V_{SSA} and V_{SSD}); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DAC						
$V_{o(rms)}$	output voltage (RMS value)	at 0 dB (FS) digital input	–	0.5	–	V
ΔV_o	unbalance between channels		–	0.1	–	dB
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	f_s = 44.1 kHz; at 0 dB	–	–80	–	dB
		f_s = 44.1 kHz; at –60 dB; A-weighted	–	–37	–	dB
		f_s = 96 kHz; at 0 dB	–	–75	–	dB
		f_s = 96 kHz; at –60 dB; A-weighted	–	–35	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N	signal-to-noise ratio	f_s = 44.1 kHz; code = 0; A-weighted	–	97	–	dB
		f_s = 96 kHz; code = 0; A-weighted	–	95	–	dB
		MUTE = HIGH; A-weighted	–	110	–	dB
α_{cs}	channel separation		–	100	–	dB
PSRR	power supply rejection ratio	f_{ripple} = 1 kHz; V_{ripple} = 30 mV (p-p)	–	60	–	dB

14.2 3.0 V supply voltage

$V_{DDD} = V_{DDA}$ = 3.0 V; f_i = 1 kHz; T_{amb} = 25 °C; R_L = 5 kΩ. All voltages with respect to ground (pins V_{SSA} and V_{SSD}); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DAC						
$V_{o(rms)}$	output voltage (RMS value)	at 0 dB (FS) digital input	–	0.75	–	V
ΔV_o	unbalance between channels		–	0.1	–	dB
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	f_s = 44.1 kHz; at 0 dB	–	–90	–	dB
		f_s = 44.1 kHz; at –60 dB; A-weighted	–	–40	–	dB
		f_s = 96 kHz; at 0 dB	–	–85	–	dB
		f_s = 96 kHz; at –60 dB; A-weighted	–	–37	–	dB
S/N	signal-to-noise ratio	f_s = 44.1 kHz; code = 0; A-weighted	–	100	–	dB
		f_s = 96 kHz; code = 0; A-weighted	–	98	–	dB
		MUTE = HIGH; A-weighted	–	110	–	dB
α_{cs}	channel separation		–	100	–	dB
PSRR	power supply rejection ratio	f_{ripple} = 1 kHz; V_{ripple} = 30 mV (p-p)	–	60	–	dB

14.3 Timing

$V_{DDD} = V_{DDA}$ = 1.8 to 3.6 V; T_{amb} = –20 to +85 °C; R_L = 5 kΩ. The typical timing is specified at f_s = 44.1 kHz (sampling frequency). All voltages with respect to ground (pins V_{SSA} and V_{SSD}); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
System clock timing (see Fig.6)						
T_{sys}	system clock cycle time	$f_{sys} = 256f_s$	35	88	780	ns
		$f_{sys} = 384f_s$	23	59	520	ns
		$f_{sys} = 512f_s$	17	44	390	ns
t_{CWH}	system clock HIGH time	f_{sys} < 19.2 MHz	$0.3T_{sys}$	–	$0.7T_{sys}$	ns
		$f_{sys} \geq$ 19.2 MHz	$0.4T_{sys}$	–	$0.6T_{sys}$	ns
t_{CWL}	system clock LOW time	f_{sys} < 19.2 MHz	$0.3T_{sys}$	–	$0.7T_{sys}$	ns
		$f_{sys} \geq$ 19.2 MHz	$0.4T_{sys}$	–	$0.6T_{sys}$	ns
Serial interface timing (see Fig.7)						
f_{BCK}	bit clock frequency		–	–	$64f_s$	Hz
t_{BCKH}	bit clock HIGH time		50	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{BCKL}	bit clock LOW time		50	–	–	ns
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
$t_{su(DATAI)}$	set-up time data input		20	–	–	ns
$t_{h(DATAI)}$	hold time data input		0	–	–	ns
$t_{su(WS)}$	set-up time word select		20	–	–	ns
$t_{h(WS)}$	hold time word select		10	–	–	ns

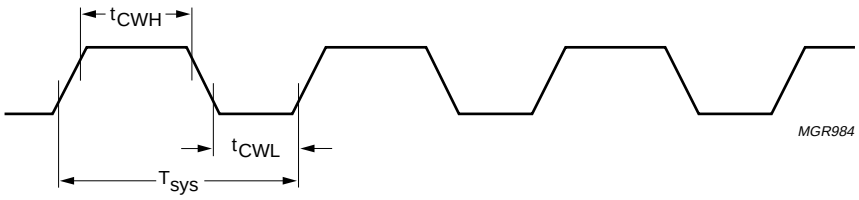


Fig.6 System clock timing.

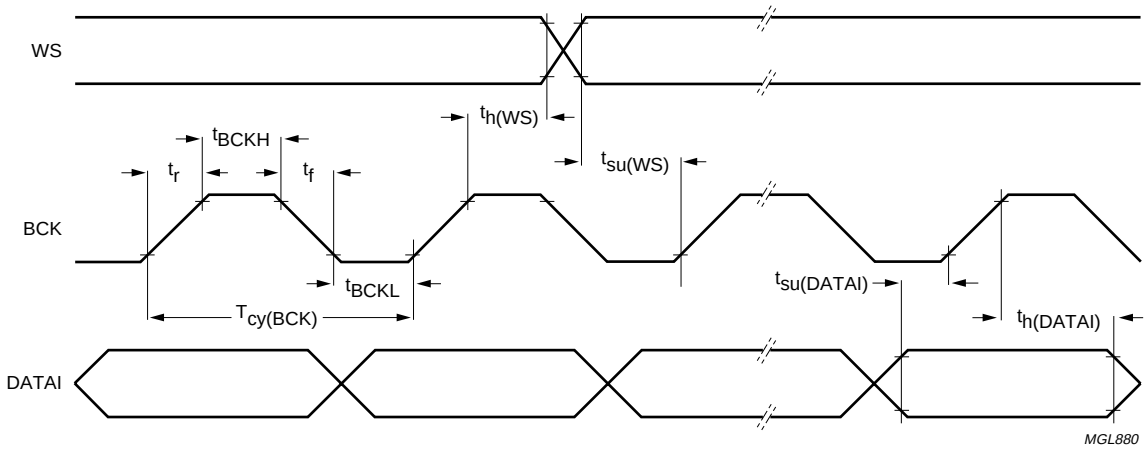


Fig.7 Serial interface timing.

15 APPLICATION INFORMATION

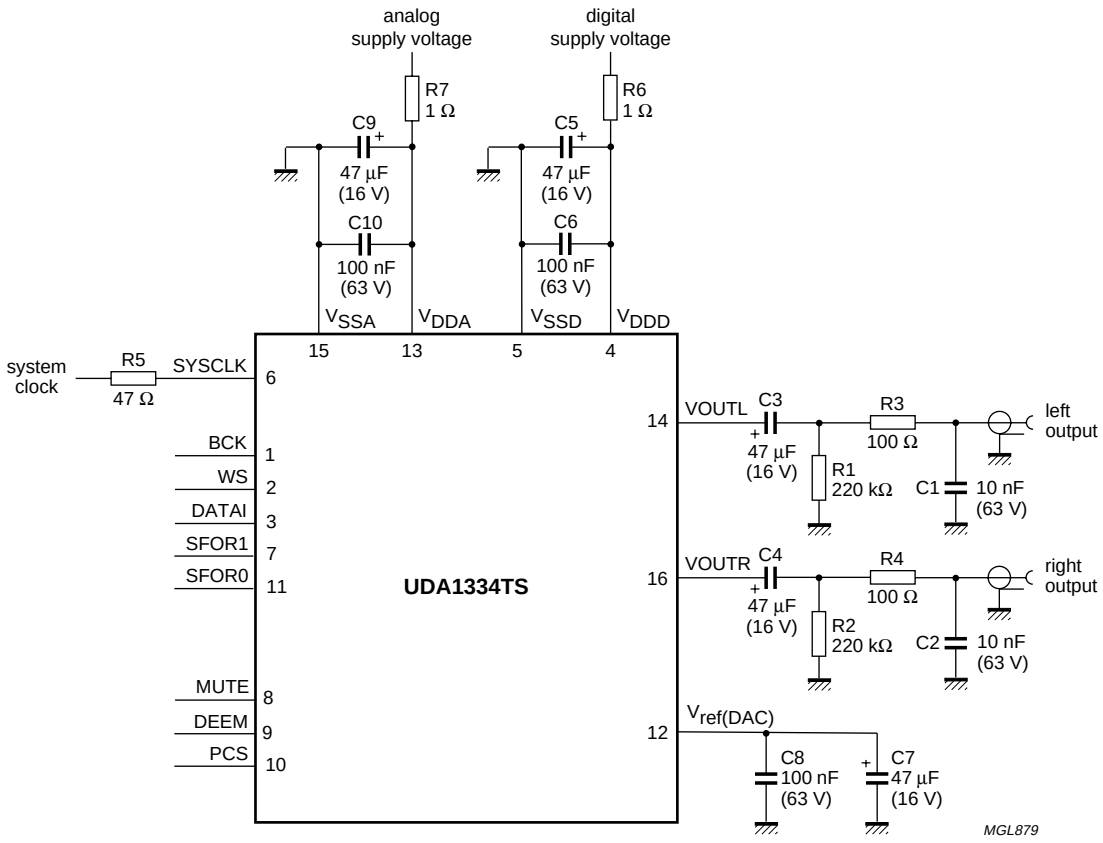
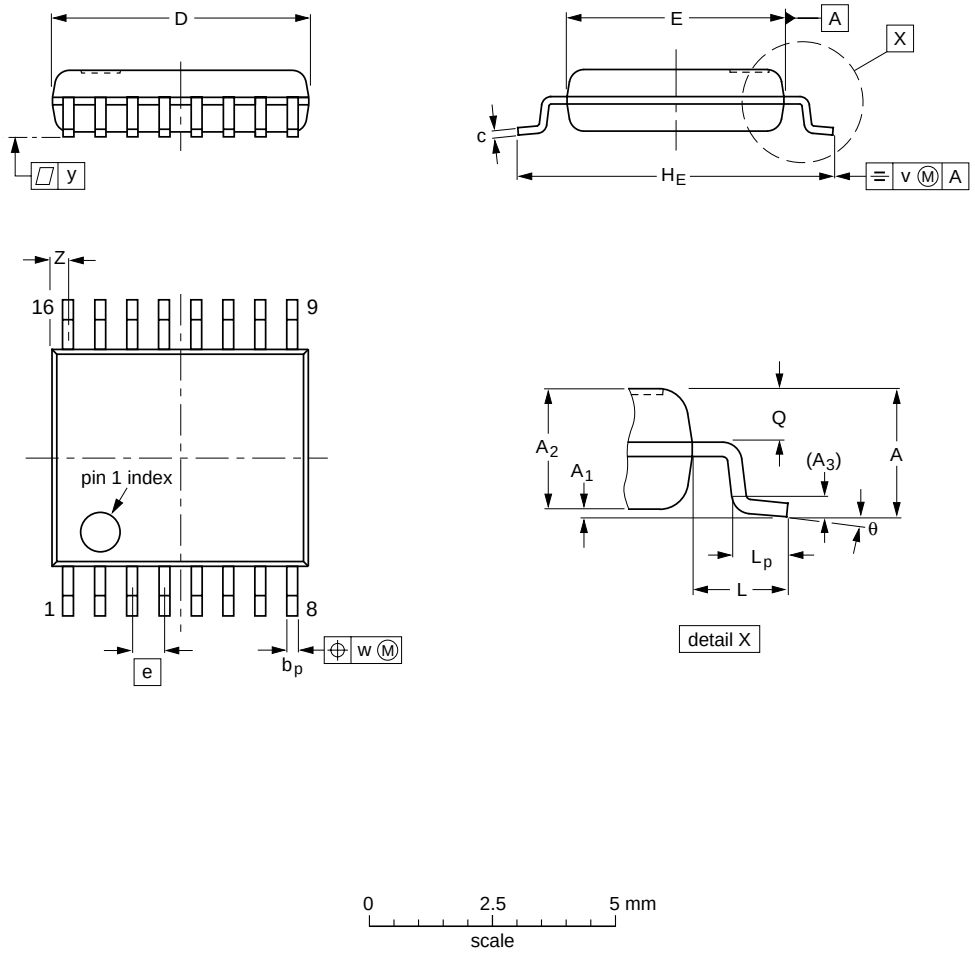


Fig.8 Typical application diagram.

16 PACKAGE OUTLINE

SSOP16: plastic shrink small outline package; 16 leads; body width 4.4 mm **SOT369-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0.00	1.4 1.2	0.25	0.32 0.20	0.25 0.13	5.30 5.10	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT369-1		MO-152				~~95-02-04~~ 99-12-27

17 SOLDERING

17.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

17.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

17.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

17.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

17.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

18 DATA SHEET STATUS

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Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

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