UJA1163

Mini high-speed CAN system basis chip with Standby mode

Rev. 2 — 17 April 2014 Product data sheet

1. General description

The UJA1163 is a mini high-speed CAN System Basis Chip (SBC) containing an ISO 11898-2/5 compliant HS-CAN transceiver and an integrated 5 V/100 mA supply for a microcontroller. The UJA1163 can be operated in a very low-current Standby mode with bus wake-up capability and supports ISO 11898-6 compliant autonomous CAN biasing.

The UJA1163 implements the standard CAN physical layer as defined in the current ISO11898 standard (-2 and -5). Pending the release of the updated version of ISO11898 including CAN FD, additional timing parameters defining loop delay symmetry are included. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 2 Mbit/s.

2. Features and benefits

2.1 General

- ISO 11898-2 and ISO 11898-5 compliant high-speed CAN transceiver
- Loop delay symmetry timing enables reliable communication at data rates up to 2 Mbit/s in the CAN FD fast phase
- Autonomous bus biasing according to ISO 11898-6
- Fully integrated 5 V/100 mA low-drop voltage regulator for 5 V microcontroller supply (V1)
- Bus connections are truly floating when power to pin BAT is off

2.2 Designed for automotive applications

- ±8 kV ElectroStatic Discharge (ESD) protection, according to the Human Body Model (HBM) on the CAN bus pins
- ±6 kV ESD protection, according to IEC 61000-4-2 on the CAN bus pins and on pin BAT
- CAN bus pins short-circuit proof to ±58 V
- Battery and CAN bus pins protected against automotive transients according to ISO 7637-3
- Very low quiescent current in Standby mode with full wake-up capability
- Leadless HVSON14 package (3.0 mm × 4.5 mm) with improved Automated Optical Inspection (AOI) capability and low thermal resistance
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)

2.3 Low-drop voltage regulator for 5 V microcontroller supply (V1)

- 5 V nominal output; ±2 % accuracy
- 100 mA output current capability
- Current limiting above 150 mA
- On-resistance of 5 Ω (max)
- Support for microcontroller RAM retention down to a battery voltage of 2 V
- Undervoltage reset at 90 % of nominal value
- Excellent transient response with a 4.7 μF ceramic output capacitor
- Short-circuit to GND/overload protection on pin V1

2.4 Power Management

- Standby mode featuring very low supply current; voltage V1 remains active to maintain the supply to the microcontroller
- Remote wake-up capability via standard CAN wake-up pattern

2.5 System control and diagnostic features

- Mode control via pin STBN
- Overtemperature shutdown
- Bidirectional reset pin

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
UJA1163TK	HVSON14	plastic thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 ´ 4.5 ´ 0.85 mm	SOT1086-2

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

4. Block diagram

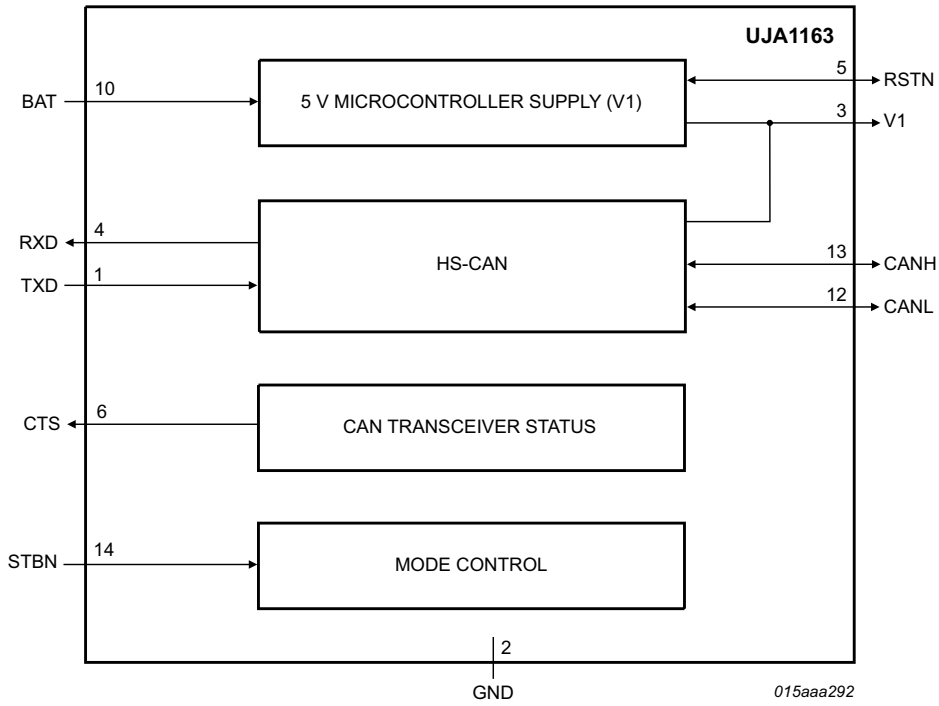


Fig 1. Block diagram of UJA1163

5. Pinning information

5.1 Pinning

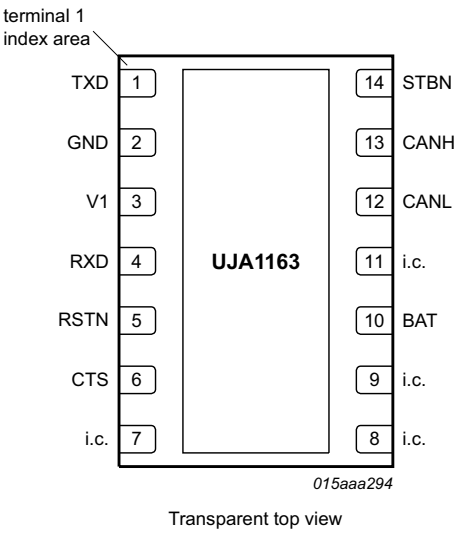


Fig 2. Pin configuration diagram

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
TXD	1	transmit data input
GND	2[1]	ground
V1	3	5 V microcontroller supply voltage
RXD	4	receive data output; reads out data from the bus lines
RSTN	5	reset input/output
CTS	6	CAN transceiver status output
i.c.	7	internally connected; should be left floating or connected to GND
i.c.	8	internally connected; should be left floating or connected to GND
i.c.	9	internally connected; should be left floating or connected to GND
BAT	10	battery supply voltage
i.c.	11	internally connected; should be left floating or connected to GND
CANL	12	LOW-level CAN bus line
CANH	13	HIGH-level CAN bus line
STBN	14	standby control input (active LOW)

[1] The exposed die pad at the bottom of the package allows for better heat dissipation and grounding from the SBC via the printed circuit board. For enhanced thermal and electrical performance, it is recommended to solder the exposed die pad to GND.

6. Functional description

6.1 System controller

The system controller controls the internal functions of the UJA1163.

6.1.1 Operating modes

The system controller contains a state machine that supports five operating modes: Normal, Standby, Reset, Overtemp and Off. The state transitions are illustrated in Figure 3.

6.1.1.1 Normal mode

Normal mode is the active operating mode. In this mode, all the hardware on the device is available and can be activated (see Table 3). Voltage regulator V1 is enabled to supply the microcontroller.

The CAN interface can be configured to be active and thus to support normal CAN communication.

Normal mode can be selected from Standby mode by setting pin STBN HIGH. Pending wake-up events (power-on, CAN bus wake-up) are cleared when the UJA1163 enters Normal mode.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

6.1.1.2 Standby mode

Standby mode is the UJA1163's power saving mode, offering reduced current consumption. The transceiver is unable to transmit or receive data in Standby mode. V1 remains active in Standby mode.

The receiver monitors bus activity for a wake-up request. The bus pins are biased to GND (via $R_{i(cm)}$) when the bus is inactive for $t > t_{to(silence)}$ and at approximately 2.5 V when there is activity on the bus (autonomous biasing).

Pin RXD is forced LOW when a wake-up event is detected on the CAN bus.

The UJA1163 switches to Standby mode via Reset mode:

- from Off mode if the battery voltage rises above the power-on detection threshold ($V_{th(det)pon}$)
- from Overtemp mode if the chip temperature falls below the overtemperature protection release threshold, $T_{th(rel)otp}$

Standby mode can also be selected from Normal by setting pin STBN LOW.

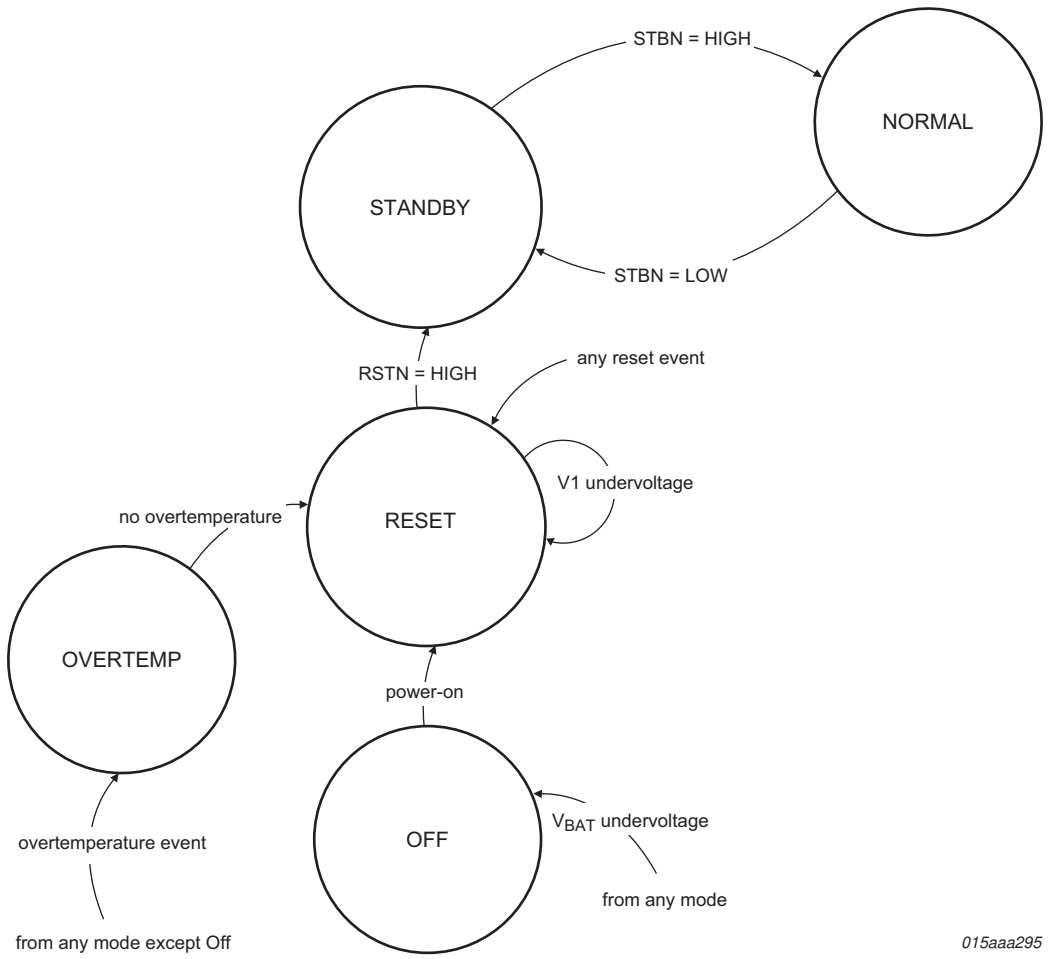


Fig 3. UJA1163 system controller state diagram

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

6.1.1.3 Reset mode

Reset mode is the reset execution state of the SBC. This mode ensures that pin RSTN is pulled down for a defined time to allow the microcontroller to start up in a controlled manner.

The transceiver is unable to transmit or receive data in Reset mode. V1 and overtemperature detection are active.

The UJA1163 switches to Reset mode from any mode in response to a reset event.

The UJA1163 exits Reset mode:

- and switches to Standby mode if pin RSTN is released HIGH
- if the SBC is forced into Off or Overtemp mode

If a V1 undervoltage event forced the transition to Reset mode, the UJA1163 will remain in Reset mode until the voltage on pin V1 has recovered.

6.1.1.4 Off mode

The UJA1163 switches to Off mode when the battery is first connected or from any mode when $V_{BAT} < V_{th(det)poff}$. Only power-on detection is enabled; all other modules are inactive. The UJA1163 starts to boot up when the battery voltage rises above the power-on detection threshold $V_{th(det)pon}$ (triggering an initialization process) and switches to Reset mode after $t_{startup}$. Pin RXD is driven LOW when the UJA1163 switches from Off mode to Standby mode, to indicate a power-on event has occurred.

In Off mode, the CAN pins disengage from the bus (zero load; high-ohmic).

6.1.1.5 Overtemp mode

Overtemp mode is provided to prevent the UJA1163 being damaged by excessive temperatures. The UJA1163 switches immediately to Overtemp mode from any mode (other than Off mode) when the global chip temperature rises above the overtemperature protection activation threshold, $T_{th(act)otp}$.

In Overtemp mode, the CAN transmitter and receiver are disabled and the CAN pins are in a high-ohmic state. No wake-up event will be detected, but a pending wake-up will still be signalled by a LOW level on pin RXD, which will persist after the overtemperature event has been cleared. V1 is off and pin RSTN is driven LOW after $t_{d(uvd)V1}$.

The UJA1163 exits Overtemp mode:

- and switches to Reset mode if the chip temperature falls below the overtemperature protection release threshold, $T_{th(rel)otp}$
- if the device is forced to switch to Off mode ($V_{BAT} < V_{th(det)poff}$)

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

6.1.1.6 Hardware characterization for the UJA1163 operating modes

Table 3. Hardware characterization by functional block

Block	Operating mode				
	Off	Standby	Normal	Reset	Overtemp
V1	off[1]	on	on	on	off
RSTN	LOW	HIGH	HIGH	LOW	LOW
CAN	off	Offline	Active	Offline	off
RXD	V_1 level	V1 level/LOW if wake-up detected	CAN bit stream	V1 level/LOW if wake-up detected	V1 level/LOW if wake-up detected

[1] When the SBC switches from Reset, Standby or Normal mode to Off mode, V1 behaves as a current source during power down while V_{BAT} is between 3 V and 2V.

6.1.2 Mode control via pin STBN

The UJA1163 can be switched between Normal and Standby modes via the STBN control input (see Figure 3). When STBN goes LOW, the UJA1163 switches to Standby mode. When STBN goes HIGH, the UJA1163 switches to Normal mode.

6.2 System reset

When a system reset occurs, the SBC switches to Reset mode and initiates a process that generates a low-level pulse on pin RSTN.

6.2.1 Characteristics of pin RSTN

Pin RSTN is a bidirectional open drain low side driver with integrated pull-up resistance, as shown in Figure 4. With this configuration, the SBC can detect the pin being pulled down externally, e.g. by the microcontroller. The input reset pulse width must be at least $t_{w(rst)}$.

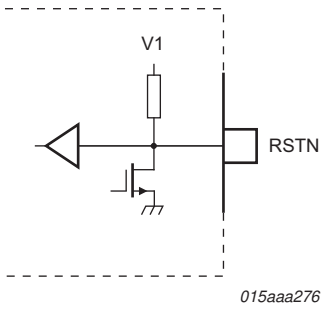


Fig 4. RSTN internal pin configuration

6.2.2 Output reset pulse width

The SBC distinguishes between a cold start and a warm start. A cold start is performed on start-up if the reset event was combined with a V1 undervoltage event (power-on reset, overtemperature reset, V1 undervoltage before entering or while in Reset mode). The cold start output reset pulse width ($t_{w(rst)}$) is between 20 ms and 25 ms.

If the reset event was triggered externally (by pulling RSTN LOW), the output reset pulse is between 1 ms and 1.5 ms. This is called warm start of the microcontroller.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

6.2.3 Reset sources

The following events will cause the UJA1163 to switch to Reset mode:

- V_{V1} drops below the 90 % undervoltage threshold
- pin RSTN is pulled down externally
- the SBC leaves Off mode
- the SBC leaves Overtemp mode

6.3 Global temperature protection

The temperature of the UJA1163 is monitored continuously, except in Off mode. The SBC switches to Overtemp mode if the temperature exceeds the overtemperature protection activation threshold, $T_{th(act)otp}$. In addition, pin RSTN is driven LOW and V1 and the CAN transceiver are switched off. When the temperature drops below the overtemperature protection release threshold, $T_{th(rel)otp}$, the SBC switches to Standby mode via Reset mode.

6.4 Power supplies

6.4.1 Battery supply voltage (V_{BAT})

The internal circuitry is supplied from the battery via pin BAT. The device needs to be protected against negative supply voltages, e.g. by using an external series diode. If V_{BAT} falls below the power-off detection threshold, $V_{th(det)poff}$, the SBC switches to Off mode. However, the microcontroller supply voltage (V1) remains active until V_{BAT} falls below 2 V.

The SBC switches from Off mode to Reset mode $t_{startup}$ after the battery voltage rises above the power-on detection threshold, $V_{th(det)pon}$. A power-on event is indicated by a LOW level on pin RXD. RXD remains LOW from the moment UJA1163 exits Off mode until it switches to Normal mode.

6.4.2 Low-drop voltage supply for 5 V microcontroller (V1)

V1 is intended to supply the microcontroller and the internal CAN transceiver and delivers up to 150 mA at 5 V. The output voltage on V1 is monitored. A system reset is generated if the voltage on V1 drops below the 90 % undervoltage threshold (90 % of the nominal V1 output voltage).

The internal CAN transceiver consumes 50 mA (max) when the bus is continuously dominant, leaving 100 mA available for the external load on pin V1. In practice, the typical current consumption of the CAN transceiver is lower (≈25 mA), depending on the application, leaving more current available for the load.

6.5 High-speed CAN transceiver

The integrated high-speed CAN transceiver is designed for active communication at bit rates up to 1 Mbit/s, providing differential transmit and receive capability to a CAN protocol controller. The transceiver is ISO 11898-2 and ISO 11898-5 compliant. The CAN transmitter is supplied from V1. The UJA1163 includes additional timing parameters on loop delay symmetry to ensure reliable communication in fast phase at data rates up to 2 Mbit/s, as used in CAN FD networks.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

The CAN transceiver supports autonomous CAN biasing as defined in ISO 11898-6, which helps to minimize RF emissions. CANH and CANL are always biased to 2.5 V when the UJA1163 is in Normal mode. Autonomous biasing is active when the UJA1163 is in Standby mode and the CAN transceiver is in CAN Offline mode - to 2.5 V if there is activity on the bus (CAN Offline Bias mode) and to GND if there is no activity on the bus for t > $t_{to(silence)}$ (CAN Offline mode).

This is useful when the node is disabled due to a malfunction in the microcontroller. The SBC ensures that the CAN bus is correctly biased to avoid disturbing ongoing communication between other nodes. The autonomous CAN bias voltage is derived directly from V_{BAT}.

6.5.1 CAN operating modes

The integrated CAN transceiver supports three operating modes: Active, Offline and Offline Bias (see Figure 6). The CAN transceiver operating mode depends on the UJA1163 operating mode and the output voltage on V1.

6.5.1.1 CAN Active mode

In CAN Active mode, the transceiver can transmit and receive data via CANH and CANL. The differential receiver converts the analog data on the bus lines into digital data, which is output on pin RXD. The transmitter converts digital data generated by the CAN controller (input on pin TXD) into analog signals suitable for transmission over the CANH and CANL bus lines.

The CAN transceiver is in Active mode when:

- the UJA1163 is in Normal mode (STBN = 1) AND
- the voltage on pin V1 is above the 90 % threshold

If pin TXD is LOW when the transceiver switches to CAN Active mode (UJA1163 in Normal mode), the transmitter and receiver will remain disabled until TXD goes HIGH. This prevents network traffic being blocked for $t_{to(dom)TXD}$ (i.e. while the TXD dominant time-out timer is running; see Section 6.7.1) every time the transceiver enters Active mode, if the TXD pin is clamped permanently LOW.

In CAN Active mode, the CAN bias voltage is derived from V1.

6.5.1.2 CAN Offline and Offline Bias modes

In CAN Offline mode, the transceiver monitors the CAN bus for a wake-up event. CANH and CANL are biased to GND.

CAN Offline Bias mode is the same as CAN Offline mode, with the exception that the CAN bus is biased to 2.5 V. This mode is activated automatically when activity is detected on the CAN bus while the transceiver is in CAN Offline mode. The transceiver will return to CAN Offline mode if the CAN bus is silent (no CAN bus edges) for longer than $t_{to(silence)}$.

The CAN transceiver switches to CAN Offline mode from CAN Active mode if:

- the SBC switches to Reset or Standby mode

provided the CAN-bus has been inactive for at least $t_{to(silence)}$. If the CAN-bus has been inactive for less than $t_{to(silence)}$, the CAN transceiver switches first to CAN Offline Bias mode and then to CAN Offline mode once the bus has been silent for $t_{to(silence)}$.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

The CAN transceiver switches to CAN Offline Bias mode from CAN Active mode if the voltage on V1 drops below the 90 % undervoltage threshold.

The CAN transceiver switches to CAN Offline mode:

- from CAN Offline Bias mode if no activity is detected on the bus (no CAN edges) for $t > t_{to(silence)}$ OR
- when the SBC switches from Off or Overtemp mode to Reset mode

The CAN transceiver switches from CAN Offline mode to CAN Offline Bias mode if:

- a standard wake-up pattern (according to ISO11898-5) is detected on the CAN bus OR
- the SBC is in Normal mode with $V_{V1} < 90$ %

6.5.1.3 CAN Off mode

The CAN transceiver is switched off completely with the bus lines floating when:

- the SBC switches to Off or Overtemp mode OR
- V_{BAT} falls below the CAN receiver undervoltage detection threshold, $V_{uvd(CAN)}$

It will be switched on again on entering CAN Offline mode when V_{BAT} rises above the undervoltage recovery threshold ($V_{uvr(CAN)}$) and the SBC is no longer in Off/Overtemp mode. CAN Off mode prevents reverse currents flowing from the bus when the battery supply to the SBC is lost.

6.5.2 CAN standard wake-up

The UJA1163 monitors the bus for a wake-up pattern when the CAN transceiver is in Offline mode.

A filter at the receiver input prevents unwanted wake-up events occurring due to automotive transients or EMI. A dominant-recessive-dominant wake-up pattern must be transmitted on the CAN bus within the wake-up timeout time ($t_{to(wake)}$) to pass the wake-up filter and trigger a wake-up event (see Figure 5; note that additional pulses may occur between the recessive/dominant phases). The recessive and dominant phases must last at least $t_{wake(busrec)}$ and $t_{wake(busdom)}$, respectively.

Pin RXD is driven LOW when a valid CAN wake-up pattern is detected on the bus.

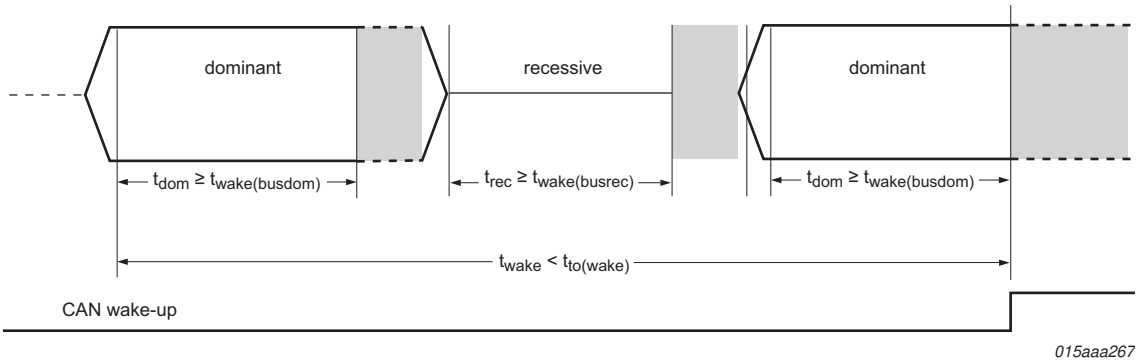
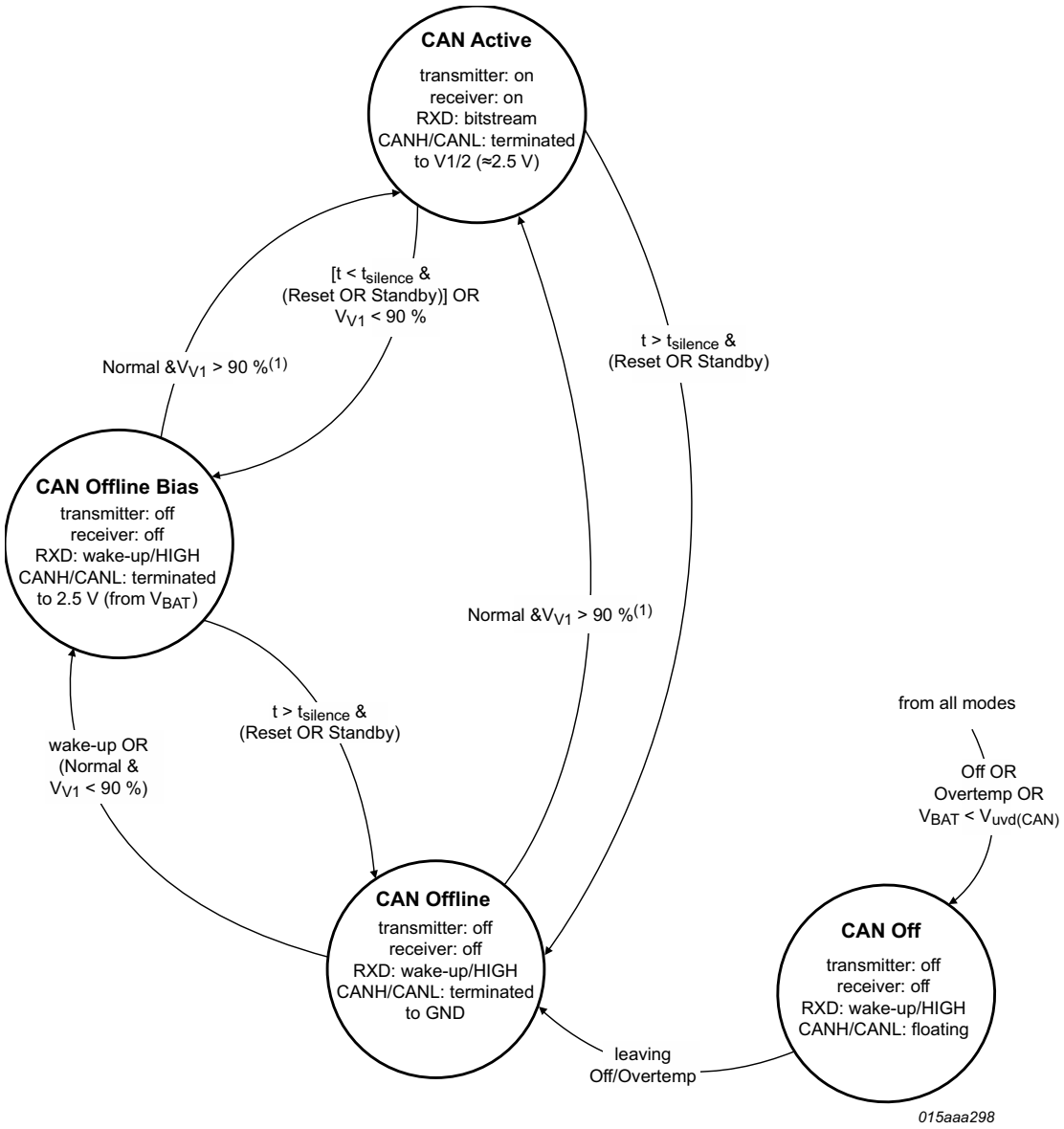


Fig 5. CAN wake-up timing

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.



(1) To prevent the bus lines being driven to a permanent dominant state, the transceiver will not switch to CAN Active mode if pin TXD is held LOW (e.g. by a short-circuit to GND)

Fig 6. CAN transceiver state machine

6.6 CAN transceiver status pin (CTS)

Pin CTS is driven HIGH to indicate to microcontroller that the transceiver is fully enabled and data can be transmitted and received via the TXD/RXD pins.

Pin CTS is actively driven LOW:

- while the transceiver is starting up (e.g. during a transition from Standby to Normal) or
- if pin TXD is clamped LOW for $t > t_{to(dom)TXD}$ or
- if an undervoltage is detected on V1

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

6.7 CAN fail-safe features

6.7.1 TXD dominant timeout

A TXD dominant time-out timer is started when pin TXD is forced LOW while the transceiver is in CAN Active Mode. If the LOW state on pin TXD persists for longer than the TXD dominant time-out time ($t_{to(dom)TXD}$), the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD goes HIGH. The TXD dominant time-out time also defines the minimum possible bit rate of 15 kbit/s.

6.7.2 Pull-up on TXD pin

Pin TXD has an internal pull-up towards V1 to ensure a safe defined recessive driver state in case the pin is left floating.

6.7.3 Pull-down on STBN pin

Pin STBN has an internal pull-down (to GND) to ensure the UJA1163 switches to Standby mode if STBN is left floating.

6.7.4 Loss of power at pin BAT

A loss of power at pin BAT has no influence on the bus lines or on the microcontroller. No reverse currents will flow from the bus.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_x	voltage on pin x	DC value			
		pin V1 [1]	−0.2	+6	V
		pins TXD, RXD, STBN, RSTN	−0.2	V_{V1} + 0.2	V
		pin BAT	−0.2	+40	V
		pins CANH and CANL with respect to any other pin	−58	+58	V
$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL		−40	+40	V
V_{trt}	transient voltage	on pins [2] BAT: via reverse polarity diode and capacitor to ground CANL, CANH: coupling via 1 nF capacitors	−150	+100	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 [3]			
		on pins CANH and CANL; pin BAT with capacitor	−6	+6	kV
		HBM [4]			
		on pins CANH, CANL [5]	−8	+8	kV
		on pins BAT	−4	+4	kV
		on any other pin	−2	+2	kV
		MM [6]			
		on any pin	−100	+100	V
		CDM [7]			
		on corner pins	−750	+750	V
		on any other pin	−500	+500	V
T_{vj}	virtual junction temperature	[8]	−40	+150	°C
T_{stg}	storage temperature		−55	+150	°C

[1] When the device is not powered up, I_{V1} (max) = 25 mA.

[2] Verified by an external test house to ensure pins can withstand ISO 7637 part 2 automotive transient test pulses 1, 2a, 3a and 3b.

[3] ESD performance according to IEC 61000-4-2 (150 pF, 330 Ω) has been verified by an external test house; the result was equal to or better than ±6 kV.

[4] Human Body Model (HBM): according to AEC-Q100-002 (100 pF, 1.5 kΩ).

[5] V1 and BAT connected to GND, emulating the application circuit.

[6] Machine Model (MM): according to AEC-Q100-003 (200 pF, 0.75 μH, 10 Ω).

[7] Charged Device Model (CDM): according to AEC-Q100-011 (field Induced charge; 4 pF).

[8] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(j-a)}$, where $R_{th(j-a)}$ is a fixed value used in the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(vj-a)}$	thermal resistance from virtual junction to ambient	[1]	60	K/W

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 μm) and thermal via array under the exposed pad connected to the first inner copper layer (thickness: 70 μm).

9. Static characteristics

Table 6. Static characteristics

T_{vj} = −40 °C to +150 °C; V_{BAT} = 3 V to 28 V; $R_{(CANH-CANL)}$ = 60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin BAT						
$V_{th(det)pon}$	power-on detection threshold voltage	V_{BAT} rising	4.2	-	4.55	V
$V_{th(det)poff}$	power-off detection threshold voltage	V_{BAT} falling	2.8	-	3	V
$V_{uvr(CAN)}$	CAN undervoltage recovery voltage	V_{BAT} rising	4.5	-	5	V
$V_{uvd(CAN)}$	CAN undervoltage detection voltage	V_{BAT} falling	4.2	-	4.55	V
I_{BAT}	battery supply current	Standby mode; I_{V1} = 0 μA; −40 °C < T_{vj} < 85 °C; V_{BAT} = 7 V to 18 V	-	60	85	μA
		Normal mode; CAN Active mode; CAN recessive; V_{TXD} = V_{V1}	-	4	7.5	mA
		Normal mode; CAN Active mode; CAN dominant; V_{TXD} = 0 V	-	46	67	mA
Voltage source: pin V1						
V_O	output voltage	V_{BAT} = 5.5 V to 18 V; I_{V1} = −120 mA to 0 mA; V_{TXD} = V_{V1}	4.9	5	5.1	V
		V_{BAT} = 5.65 V to 18 V; I_{V1} = −150 mA to 0 mA; V_{TXD} = V_{V1}	4.9	5	5.1	V
		V_{BAT} = 5.65 V to 18 V; I_{V1} = −100 mA to 0 mA; V_{TXD} = 0 V; V_{CANH} = 0 V	4.9	5	5.1	V
$\Delta V_{ret(RAM)}$	RAM retention voltage difference	V_{BAT} = 2 V to 3 V; I_{V1} = −2 mA	-	-	100	mV
		V_{BAT} = 2 V to 3 V; I_{V1} = −200 μA			10	mV
$R_{(BAT-V1)}$	resistance between pin BAT and pin V1	V_{BAT} = 4 V to 6 V; I_{V1} = −120 mA; T_{vj} < 150 °C	-	-	5	Ω
		V_{BAT} = 3 V to 4 V; I_{V1} = −40 mA	-	2.625	-	Ω

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

Table 6. Static characteristics *...continued*

T_{vj} = −40 °C to +150 °C; V_{BAT} = 3 V to 28 V; $R_{(CANH-CANL)}$ = 60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{uvd}	undervoltage detection voltage	$V_{uvd(nom)}$ = 90 %	4.5	-	4.75	V
V_{uvr}	undervoltage recovery voltage		4.5	-	4.75	V
$I_{O(sc)}$	short-circuit output current		−300	-	−150	mA
Standby mode control input; pin STBN						
$V_{th(sw)}$	switching threshold voltage		$0.25V_{V1}$	-	$0.75V_{V1}$	V
R_{pd}	pull-down resistance		40	60	80	kΩ
CAN transmit data input; pin TXD						
$V_{th(sw)}$	switching threshold voltage		$0.25V_{V1}$	-	$0.75V_{V1}$	V
R_{pu}	pull-up resistance		40	60	80	kΩ
CAN transmitter status; pin CTS						
I_{OH}	HIGH-level output current	$V_{CTS} = V_{V1} - 0.4$ V; transmitter on	-	-	−4	mA
I_{OL}	LOW-level output current	V_{CTS} = 0.4 V; transmitter off	4	-	-	mA
CAN receive data output; pin RXD						
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	$V_{V1} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	0.4	V
R_{pu}	pull-up resistance	CAN Offline mode	40	60	80	kΩ
High-speed CAN bus lines; pins CANH and CANL						
$V_{O(dom)}$	dominant output voltage	CAN Active mode; V_{V1} = 4.5 V to 5.5 V; V_{TXD} = 0 V;				
		pin CANH	2.75	3.5	4.5	V
		pin CANL	0.5	1.5	2.25	V
V_{TXsym}	transmitter voltage symmetry	$V_{TXsym} = V_{CANH} + V_{CANL}$; f_{TXD} = 250 kHz; C_{SPLIT} = 4.7 nF [1] [2]	$0.9V_{V1}$	-	$1.1V_{V1}$	V
$V_{dom(TX)sym}$	transmitter dominant voltage symmetry	$V_{dom(TX)sym} = V_{V1} - V_{CANH} - V_{CANL}$; V_{V1} = 5 V	−400	-	+400	mV
$V_{O(dif)bus}$	bus differential output voltage	CAN Active mode (dominant); V_{TXD} = 0 V; V_{V1} = 4.75 V to 5.5 V; $R_{(CANH-CANL)}$ = 45 Ω to 65 Ω	1.5	-	3.0	V
		CAN Active mode (recessive); CAN Offline mode; $V_{TXD} = V_{V1}$; T_{vj} < 150 °C; $R_{(CANH-CANL)}$ = no load	−50	-	+50	mV
$V_{O(rec)}$	recessive output voltage	CAN Active mode; $V_{TXD} = V_{V1}$ $R_{(CANH-CANL)}$ = no load	2	$0.5V_{V1}$	3	V
		CAN Offline mode; $R_{(CANH-CANL)}$ = no load	−0.1	-	+0.1	V
		CAN Offline Bias mode; $R_{(CANH-CANL)}$ = no load; V_{V1} = 0 V	2	2.5	3	V

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

Table 6. Static characteristics *...continued*

T_{vj} = −40 °C to +150 °C; V_{BAT} = 3 V to 28 V; $R_{(CANH-CANL)}$ = 60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{O(dom)}$	dominant output current	CAN Active mode; V_{TXD} = 0 V; V_{V1} = 5 V				
		pin CANH; V_{CANH} = 0 V	−50	-	-	mA
		pin CANL; V_{CANL} = 5 V	-	-	52	mA
$I_{O(rec)}$	recessive output current	V_{CANL} = V_{CANH} = −27 V to +32 V; V_{TXD} = V_{V1}	−3	-	+3	mA
$V_{th(RX)dif}$	differential receiver threshold voltage	CAN Active mode; V_{CANL} = V_{CANH} = −12 V to +12 V	0.5	0.7	0.9	V
		CAN Offline mode; V_{CANL} = V_{CANH} = −12 V to +12 V	0.4	0.7	1.15	V
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	CAN Active mode; V_{CANL} = V_{CANH} = −12 V to +12 V	50	200	400	mV
$R_{i(cm)}$	common-mode input resistance		9	15	28	kΩ
ΔR_i	input resistance deviation		−1	-	+1	%
$R_{i(dif)}$	differential input resistance	V_{CANL} = V_{CANH} = −12 V to +12 V	19	30	52	kΩ
$C_{i(cm)}$	common-mode input capacitance	[1]	-	-	20	pF
$C_{i(dif)}$	differential input capacitance	[1]	-	-	10	pF
I_{LI}	input leakage current	V_{BAT} = V_{V1} = 0 V or V_{BAT} = V_{V1} = shorted to ground via 47 kΩ; V_{CANH} = V_{CANL} = 5 V	−5	-	+5	µA
Temperature protection						
$T_{th(act)otp}$	overtemperature protection activation threshold temperature		167	177	187	°C
$T_{th(rel)otp}$	overtemperature protection release threshold temperature		127	137	147	°C
Reset output; pin RSTN						
V_{OL}	LOW-level output voltage	V_{V1} = 1.0 V to 5.5 V; pull-up resistor to V_{V1} ≥ 900 Ω	0	-	$0.2V_{V1}$	V
R_{pu}	pull-up resistance		40	60	80	kΩ
$V_{th(sw)}$	switching threshold voltage		$0.25V_{V1}$	-	$0.75V_{V1}$	V

[1] Not tested in production; guaranteed by design.

[2] The test circuit used to measure the bus output voltage symmetry (which includes C_{SPLIT}) is shown in Figure 11.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

10. Dynamic characteristics

Table 7. Dynamic characteristics

T_{vj} = −40 °C to +150 °C; V_{BAT} = 3 V to 28 V; $R_{(CANH-CANL)}$ = 60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage source; pin V1						
$t_{startup}$	start-up time	from V_{BAT} exceeding the power-on detection threshold until V_{V1} exceeds the 90 % undervoltage threshold; C_{V1} = 4.7 µF	-	2.8	4.7	ms
$t_{d(uvd)}$	undervoltage detection delay time		6	-	54	µs
$t_{d(uvd-RSTNL)}$	delay time from undervoltage detection to RSTN LOW	undervoltage on V1	-	-	63	µs
CAN transceiver timing; pins CANH, CANL, TXD and RXD						
$t_{d(TXD-RXD)}$	delay time from TXD to RXD	R_L = 60 Ω; C_L = 100 pF; 50 % V_{TXD} to 50 % V_{RXD}; C_{RXD} = 15 pF; f_{TXD} = 250 kHz	-	-	255	ns
		R_L = 120 Ω; C_L = 200 pF; [1] 50 % V_{TXD} to 50 % V_{RXD}; C_{RXD} = 15 pF; f_{TXD} = 250 kHz	-	-	350	ns
$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant		-	80	-	ns
$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive		-	80	-	ns
$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD	C_{RXD} = 15 pF	-	105	-	ns
$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD	C_{RXD} = 15 pF	-	120	-	ns
$t_{bit(RXD)}$	bit time on pin RXD	$t_{bit(TXD)}$ = 500 ns [2]	400	-	550	ns
$t_{wake(busdom)}$	bus dominant wake-up time	first pulse (after first recessive) for wake-up on pins CANH and CANL; CAN Offline mode	0.5	-	3.0	µs
		second pulse for wake-up on pins CANH and CANL	0.5	-	3.0	µs
$t_{wake(busrec)}$	bus recessive wake-up time	first pulse for wake-up on pins CANH and CANL; CAN Offline mode	0.5	-	3.0	µs
		second pulse (after first dominant) for wake-up on pins CANH and CANL	0.5	-	3.0	µs
$t_{to(wake)}$	wake-up time-out time	between first and second dominant pulses; CAN Offline mode	570	-	850	µs
$t_{to(dom)TXD}$	TXD dominant time-out time	CAN Active mode; V_{TXD} = 0 V	2.7	-	3.3	ms

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

Table 7. Dynamic characteristics *…continued*

T_{vj} = −40 °C to +150 °C; V_{BAT} = 3 V to 28 V; $R_{(CANH-CANL)}$ = 60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{to(silence)}$	bus silence time-out time	recessive time measurement started in all CAN modes; R_L = 120 Ω	0.95	-	1.17	s
$t_{d(busact-bias)}$	delay time from bus active to bias		-	-	200	µs
$t_{startup(CAN)}$	CAN start-up time	when switching to Active mode (CTS = HIGH)	-	-	220	µs
Pin RSTN: reset pulse width						
$t_{w(rst)}$	reset pulse width	output pulse width				
		cold start	20	-	25	ms
		warm start	1	-	1.5	ms
		input pulse width	18	-	-	µs

[1] Guaranteed by design.

[2] See Figure 8.

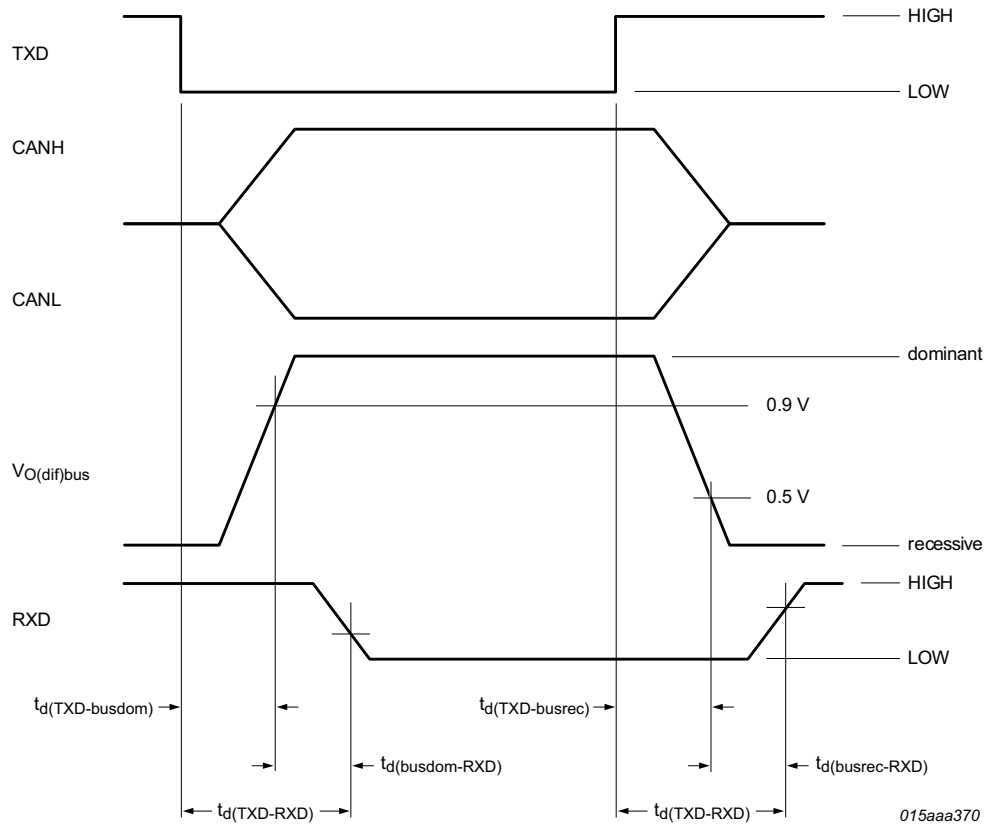


Fig 7. CAN transceiver timing diagram

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

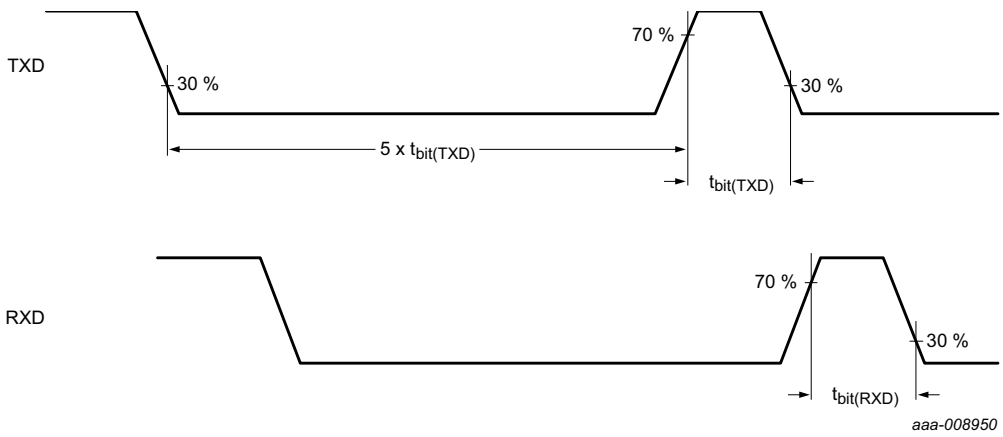


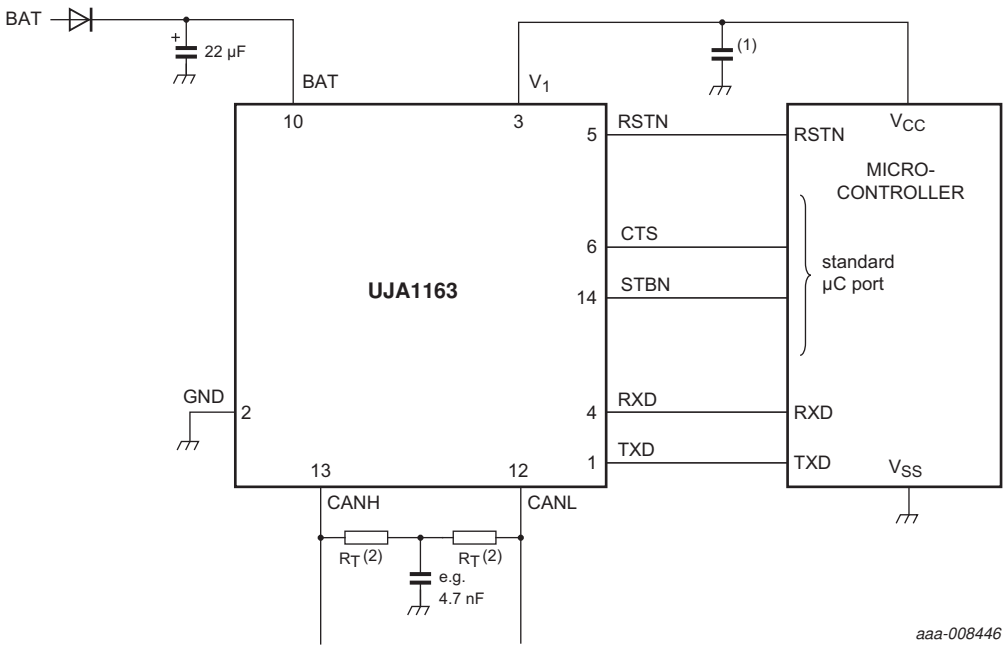
Fig 8. Loop delay symmetry timing diagram

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

11. Application information

11.1 Application diagram



(1) Actual capacitance value must be a least 1.76 µF with 5 V DC offset (recommended capacitor value is 4.7 µF)

(2) For bus line end nodes, R_T = 60 Ω in order to support the 'split termination concept'. For sub-nodes, an optional 'weak' termination of e.g. R_T = 1.3 kΩ can be used, if required by the OEM.

Fig 9. Typical application using the UJA1163

11.2 Application hints

Further information on the application of the UJA1163 can be found in the NXP application hints document *AH1306 Application Hints - Mini high speed CAN system basis chips UJA1163 / UJA1164 / UJA1167 / UJA1168.*

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

12. Test information

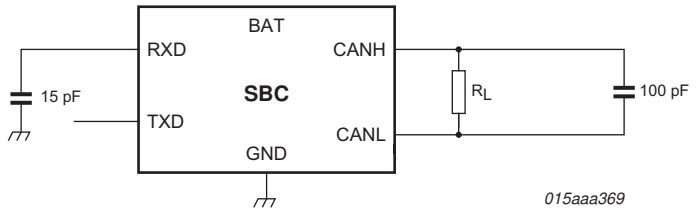


Fig 10. Timing test circuit for CAN transceiver

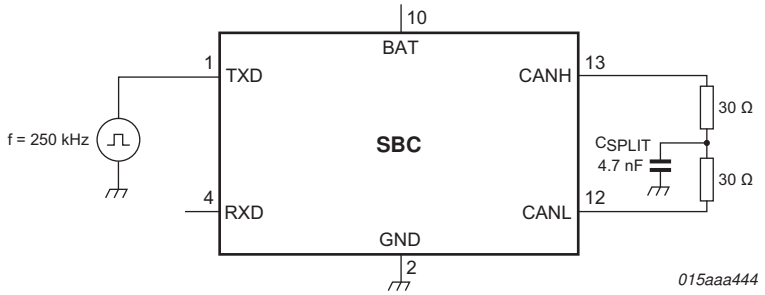


Fig 11. Test circuit for measuring transceiver driver symmetry

12.1 Quality information

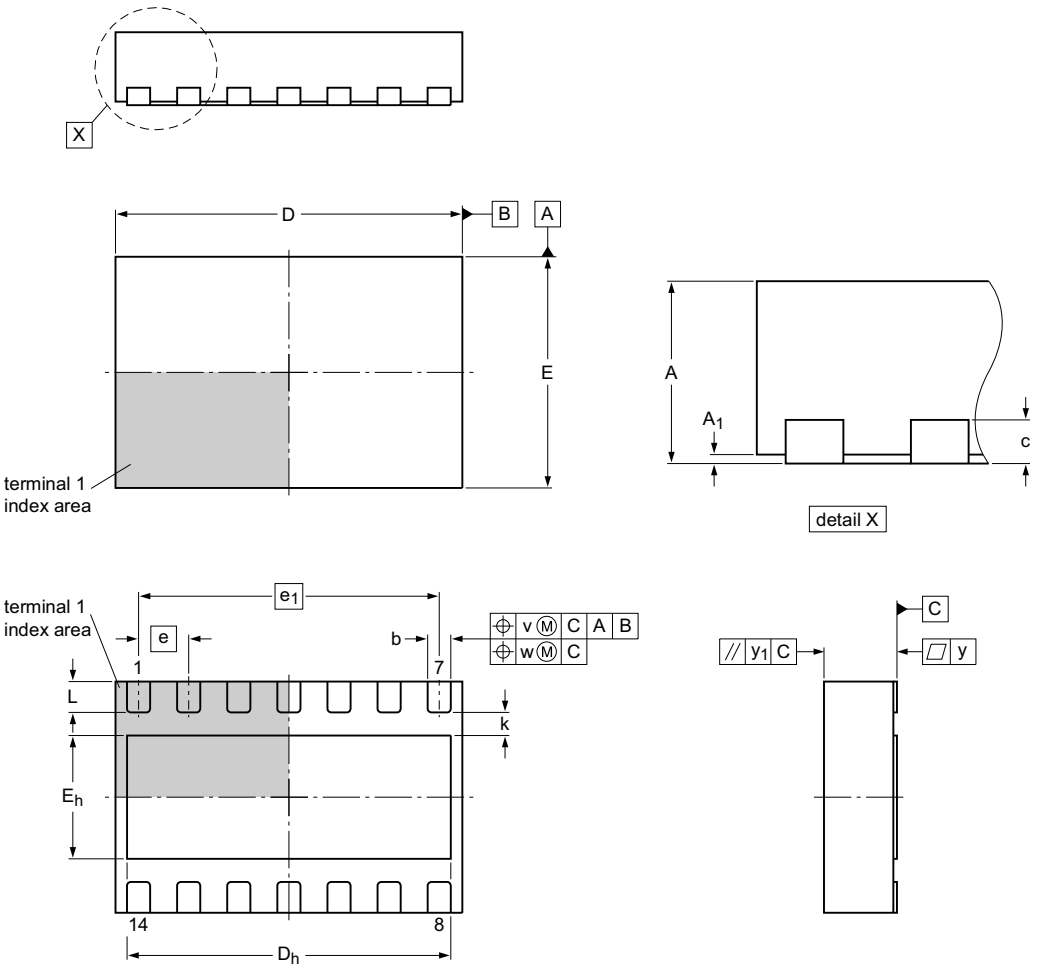
This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 Rev-G - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

13. Package outline

HVSON14: plastic, thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 x 4.5 x 0.85 mm **SOT1086-2**



Dimensions

Unit		A	A_1	b	c	D	D_h	E	E_h	e	e_1	k	L	v	w	y	y_1
	max	1.00	0.05	0.35		4.6	4.25	3.1	1.65			0.35	0.45				
mm	nom	0.85	0.03	0.32	0.2	4.5	4.20	3.0	1.60	0.65	3.9	0.30	0.40	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.29		4.4	4.15	2.9	1.55			0.25	0.35				

sot1086-2

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1086-2	- - -	MO-229	- - -		~~10-07-14~~ 10-07-15

Fig 12. Package outline SOT1086-2 (HVSON14)

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

14. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 13) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 8 and 9

Table 8. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 9. Lead-free process (from J-STD-020D)

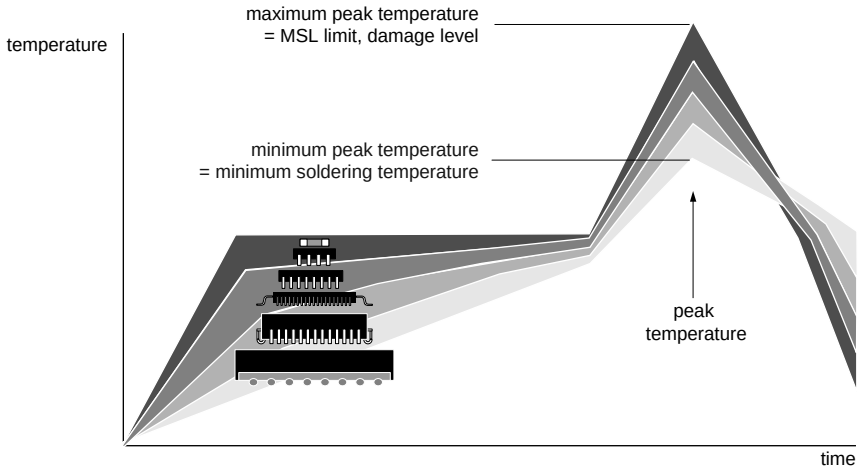
Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 13.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.



MSL: Moisture Sensitivity Level

Fig 13. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16. Soldering of HVSON packages

Section 15 contains a brief introduction to the techniques most commonly used to solder Surface Mounted Devices (SMD). A more detailed discussion on soldering HVSON leadless package ICs can found in the following application notes:

- *AN10365 'Surface mount reflow soldering description"*
- *AN10366 "HVQFN application information"*

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

17. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
UJA1163 v.2	20140417	Product data sheet	-	UJA1163 v.1
Modifications:	• Section 1: text revised (2nd paragraph added) • Section 2.1: feature added (loop delay symmetry) • Figure 1: amended • Table 2: CTS pin description changed; table note amended • Section 6.1.1.5: text revised (2nd paragraph) • Table 3: row CAN revised • Section 6.2.1: text revised • Section 6.2.2: text revised • Section 6.5: text revised • Section 6.6: text revised • Table 7: conditions revised for symbol $t_{startup}$; parameter values changed: $t_{d(uvd)}$ and $t_{d(uvd\text{-}RSTNL)}$ for pin V1; parameter $t_{bit(RXD)}$ added; additional measurement for parameter $t_{d(TXD\text{-}RXD)}$; parameter $t_{fltr(rst)}$ renamed to $t_{w(rst)}$ and value changed • Figure 8: added • Section 11.2: added • Section 12.1: text updated			
UJA1163 v.1	20131001	Product data sheet	-	-

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

18.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

18.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

18.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

19. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

20. Contents

1 General description 1
2 Features and benefits 1
2.1 General 1
2.2 Designed for automotive applications 1
2.3 Low-drop voltage regulator for 5 V microcontroller supply (V1) 2
2.4 Power Management 2
2.5 System control and diagnostic features 2
3 Ordering information 2
4 Block diagram 3
5 Pinning information 3
5.1 Pinning 3
5.2 Pin description 4
6 Functional description 4
6.1 System controller 4
6.1.1 Operating modes 4
6.1.1.1 Normal mode 4
6.1.1.2 Standby mode 5
6.1.1.3 Reset mode 6
6.1.1.4 Off mode 6
6.1.1.5 Overtemp mode 6
6.1.1.6 Hardware characterization for the UJA1163 operating modes 7
6.1.2 Mode control via pin STBN 7
6.2 System reset 7
6.2.1 Characteristics of pin RSTN 7
6.2.2 Output reset pulse width 7
6.2.3 Reset sources 8
6.3 Global temperature protection 8
6.4 Power supplies 8
6.4.1 Battery supply voltage (V_{BAT}) 8
6.4.2 Low-drop voltage supply for 5 V microcontroller (V1) 8
6.5 High-speed CAN transceiver 8
6.5.1 CAN operating modes 9
6.5.1.1 CAN Active mode 9
6.5.1.2 CAN Offline and Offline Bias modes 9
6.5.1.3 CAN Off mode 10
6.5.2 CAN standard wake-up 10
6.6 CAN transceiver status pin (CTS) 11
6.7 CAN fail-safe features 12
6.7.1 TXD dominant timeout 12
6.7.2 Pull-up on TXD pin 12
6.7.3 Pull-down on STBN pin 12
6.7.4 Loss of power at pin BAT 12
7 Limiting values 13
8 Thermal characteristics 14
9 Static characteristics 14
10 Dynamic characteristics 17
11 Application information 20
11.1 Application diagram 20
11.2 Application hints 20
12 Test information 21
12.1 Quality information 21
13 Package outline 22
14 Handling information 23
15 Soldering of SMD packages 23
15.1 Introduction to soldering 23
15.2 Wave and reflow soldering 23
15.3 Wave soldering 23
15.4 Reflow soldering 24
16 Soldering of HVSON packages 25
17 Revision history 26
18 Legal information 27
18.1 Data sheet status 27
18.2 Definitions 27
18.3 Disclaimers 27
18.4 Trademarks 28
19 Contact information 28
20 Contents 29

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2014. All rights reserved.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 17 April 2014
Document identifier: UJA1163