USB5742

2-Port SS/HS USB Controller Hub

Highlights

- USB Hub Feature Controller IC with 2 USB 3.2 Gen 1 / USB 2.0 downstream ports
- USB-IF Battery Charger revision 1.2 support on up & downstream ports (DCP, CDP, SDP)
- USB Link Power Management (LPM) support
- Enhanced OEM configuration options available through either OTP or SPI ROM
- USB-IF certified (TID 330000076), supporting latest Engineering Change Notices for compliance with USB-IF logo testing for new USB Type-C® industry initiative
  - Header Packet Timer (TD7.9, TD7.11, TD7.26)
  - Power Management Timer (TD7.18, TD7.20, TD7.23)
  - Unacknowledged Connect and Remote Wake Test Failure (TD10.25)
- Available in 56-pin (7 x 7 mm) VQFN lead-free, RoHS compliant package
- Commercial and industrial grade temperature support
- Configuration Straps: Predefined configuration of system level functions

Target Applications

- Standalone USB Hubs
- Laptop Docks
- PC Motherboards
- PC Monitor Docks
- Multi-function USB 3.2 Gen 1 Peripherals

Key Benefits

- USB 3.2 Gen 1 compliant 5 Gbps, 480 Mbps, 12 Mbps and 1.5 Mbps operation
  - 5 V tolerant USB 2.0 pins
  - 1.32 V tolerant USB 3.2 Gen 1 pins
  - Integrated termination & pull-up/pull-down resistors
- Supports per port battery charging of most popular battery powered devices
  - USB-IF Battery Charging rev. 1.2 support (DCP, CDP, SDP)
  - Apple® portable product charger emulation
  - Chinese YD/T 1591-2006 charger emulation
  - Chinese YD/T 1591-2009 charger emulation
  - European Union universal mobile charger support
  - Support for Microchip USC100x family of battery charging controllers
  - Supports additional portable devices
- Smart port controller operation
  - Firmware handling of companion port controllers
- On-chip microcontroller
  - Manages I/Os, VBUS, and other signals
- 8 KB RAM, 64 KB ROM
- 8 KB One Time Programmable (OTP) ROM
  - Includes on-chip charge pump
- Configuration programming via OTP ROM, SPI ROM, or SMBus
- **PortSwap**
  - Configurable differential intro-pair signal swapping
- **PHYBoost™**
  - Programmable USB transceiver drive strength for recovering signal integrity
- **VariSense™**
  - Programmable USB receiver sensitivity
- Compatible with Microsoft Windows 8, 7, XP, Apple OS X 10.4+, and Linux hub drivers
- Optimized for low-power operation and low thermal dissipation
- Package
  - 56-pin VQFN (7 x 7 mm)
- Environmental
  - 3 kV HBM JESD22-A114F ESD protection
  - Commercial temperature range (0°C to +70°C)
  - Industrial temperature range (-40°C to +85°C)

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1.0 PREFACE

1.1 General Terms

TABLE 1-1: GENERAL TERMS

Term	Description
ADC	Analog-to-Digital Converter
Byte	8 bits
CDC	Communication Device Class
CSR	Control and Status Registers
DWORD	32 bits
EOP	End of Packet
EP	Endpoint
FIFO	First In First Out buffer
FS	Full-Speed
FSM	Finite State Machine
GPIO	General Purpose I/O
HS	Hi-Speed
HSOS	High Speed Over Sampling
Hub Feature Controller	The Hub Feature Controller, sometimes called a Hub Controller for short is the internal processor used to enable the unique features of the USB Controller Hub. This is not to be confused with the USB Hub Controller that is used to communicate the hub status back to the Host during a USB session.
I^2C	Inter-Integrated Circuit
LS	Low-Speed
lsb	Least Significant Bit
LSB	Least Significant Byte
msb	Most Significant Bit
MSB	Most Significant Byte
N/A	Not Applicable
NC	No Connect
OTP	One Time Programmable
PCB	Printed Circuit Board
PCS	Physical Coding Sublayer
PHY	Physical Layer
PLL	Phase Lock Loop
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
SDK	Software Development Kit
SMBus	System Management Bus
UUID	Universally Unique IDentifier
WORD	16 bits

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1.2 Reference Documents

1. *UNICODE UTF-16LE For String Descriptors* USB Engineering Change Notice, December 29th, 2004, http://www.usb.org
2. *Universal Serial Bus Revision 3.2 Specification*, http://www.usb.org/developers/docs/
3. *Battery Charging Specification*, Revision 1.2, Dec. 07, 2010, http://www.usb.org
4. *I^2C-Bus Specification*, Version 1.1, http://www.nxp.com
5. *System Management Bus Specification*, Version 1.0, http://smbus.org/specs

2.0 INTRODUCTION

2.1 General Description

The Microchip USB5742 hub is low-power, OEM configurable, USB 3.2 Gen 1 hub feature controller with 2 downstream ports and advanced features for embedded USB applications. The USB5742 is fully compliant with the *Universal Serial Bus Revision 3.2 Specification* and *USB 2.0 Link Power Management Addendum*. The USB5742 supports 5 Gbps SuperSpeed (SS), 480 Mbps Hi-Speed (HS), 12 Mbps Full-Speed (FS), and 1.5 Mbps Low-Speed (LS) USB downstream devices on all enabled downstream ports.

The USB5742 supports the legacy USB speeds (HS/FS/LS) through a dedicated USB 2.0 hub feature controller that is the culmination of five generations of Microchip hub feature controller design and experience with proven reliability, interoperability, and device compatibility. The SuperSpeed hub feature controller operates in parallel with the USB 2.0 controller, decoupling the 5 Gbps SS data transfers from bottlenecks due to the slower USB 2.0 traffic.

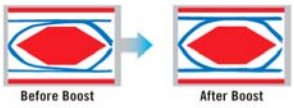
The USB5742 supports downstream battery charging. The USB5742 integrated battery charger detection circuitry supports the USB-IF Battery Charging (BC1.2) detection method and most Apple devices. The USB5742 provides the battery charging handshake and supports the following USB-IF BC1.2 charging profiles:

- DCP: Dedicated Charging Port (Power brick with no data)
- CDP: Charging Downstream Port (1.5A with data)
- SDP: Standard Downstream Port (0.5A with data)
- Custom profiles loaded via SMBus or OTP

Additionally, the USB5742 includes many powerful and unique features such as:

PortSwap, which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors to avoid uneven trace length or crossing of the USB differential signals on the PCB.

PHYBoost, which provides programmable levels of Hi-Speed USB signal drive strength in the downstream port transceivers. PHYBoost attempts to restore USB signal integrity in a compromised system environment. The graphic on the right shows an example of Hi-Speed USB eye diagrams before and after PHYBoost signal integrity restoration. in a compromised system environment



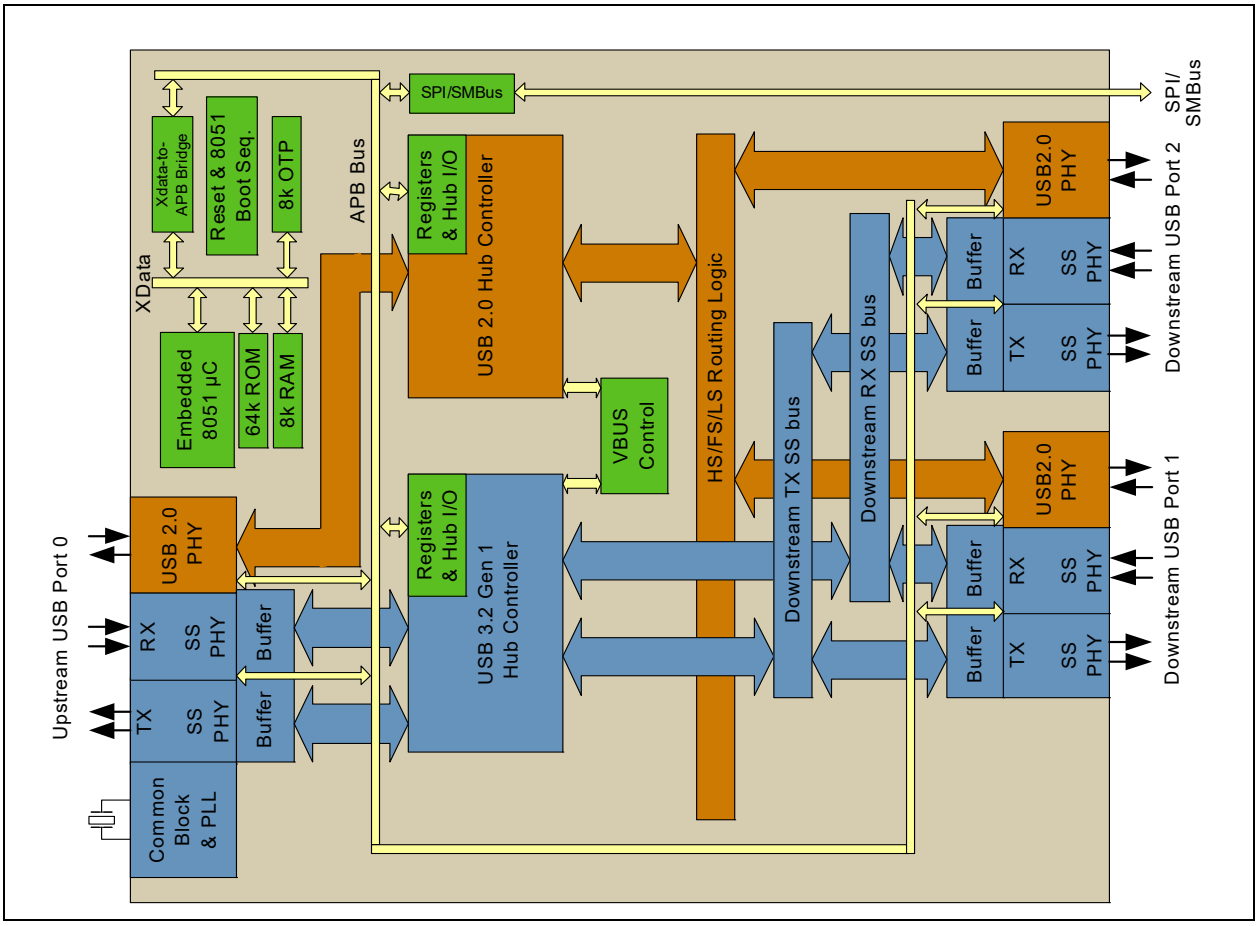
VariSense, which controls the USB receiver sensitivity enabling programmable levels of USB signal receive sensitivity. This capability allows operation in a sub-optimal system environment, such as when a captive USB cable is used.

The USB5742 can be configured for operation through internal default settings. Custom OEM configurations are supported through external SPI ROM or OTP ROM. All port control signal pins are under firmware control in order to allow for maximum operational flexibility, and are available as GPIOs for customer specific use.

The USB5742 is available in commercial (0°C to +70°C) and industrial (-40°C to +85°C) temperature range. An internal block diagram of the USB5742 is shown in Figure 2-1.

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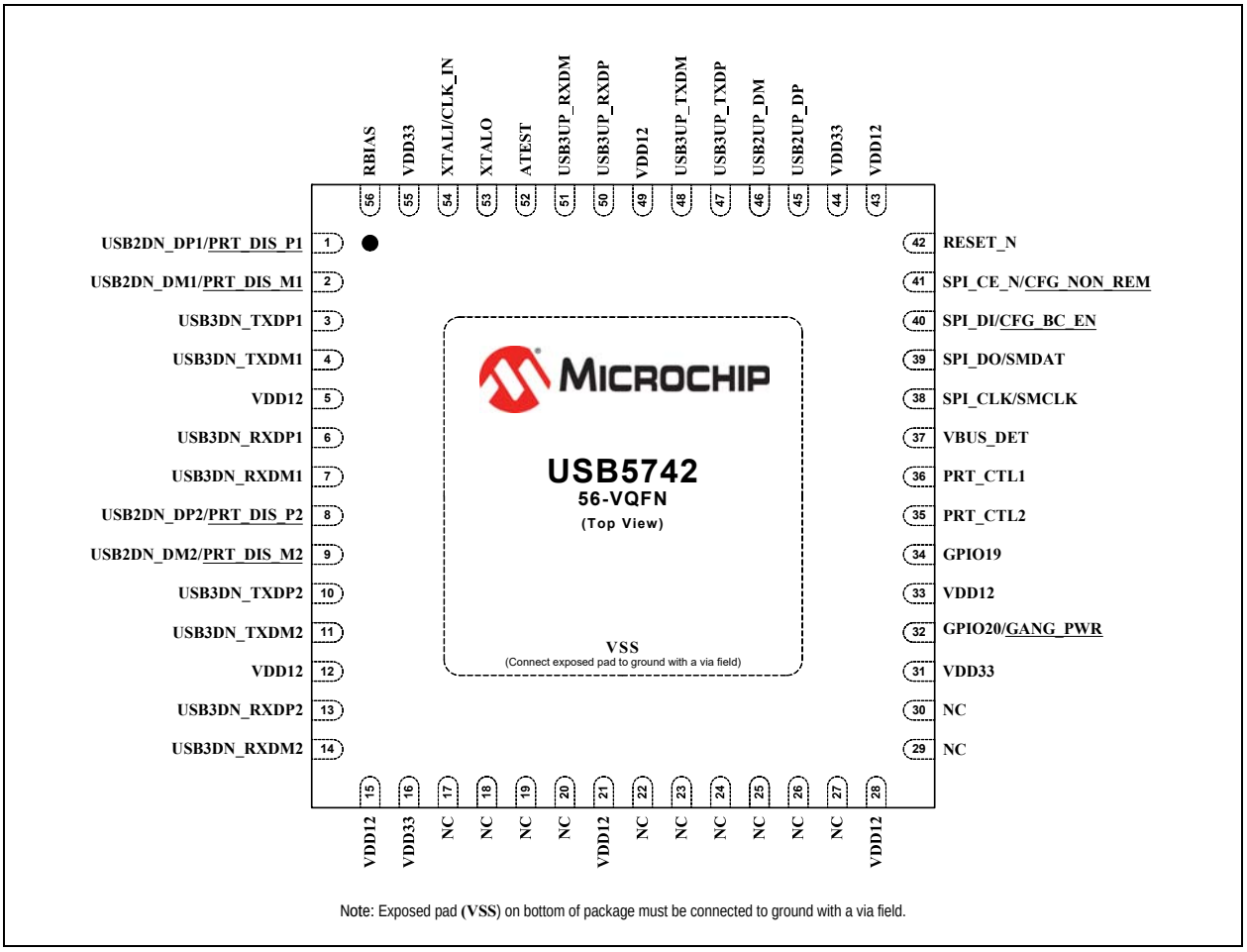
FIGURE 2-1: INTERNAL BLOCK DIAGRAM



3.0 PIN DESCRIPTION AND CONFIGURATION

3.1 Pin Assignments

FIGURE 3-1: 56-VQFN PIN ASSIGNMENTS



Note: Exposed pad (VSS) on bottom of package must be connected to ground with a via field.

Note 1: Configuration straps are identified by an underlined symbol name. Signals that function as configurations traps must be augmented with an external resistor when connected to a load. Refer to Section 3.4, "Configuration Straps and Programmable Functions" for additional information.

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Table 3-1 details the package pin assignments in table format.

TABLE 3-1: 56-VQFN PIN ASSIGNMENTS

Pin Num.	Pin Name	Reset State	Pin Num.	Pin Name	Reset State
1	USB2DN_DP1/PRT_DIS_P1	Z	29	NC	Z
2	USB2DN_DM1/PRT_DIS_M1	PD-15k	30	NC	A/P
3	USB3DN_TXDP1	PD-15k	31	VDD33	Z
4	USB3DN_TXDM1	Z	32	GPIO20/GANG_PWR	Z
5	VDD12	Z	33	VDD12	A/P
6	USB3DN_RXDP1	A/P	34	GPIO19	PD-50k
7	USB3DN_RXDM1	Z	35	PRT_CTL2	A/P
8	USB2DN_DP2/PRT_DIS_P2	Z	36	PRT_CTL1	PD-50k
9	USB2DN_DM2/PRT_DIS_M2	PD-15k	37	VBUS_DET	PD-50k
10	USB3DN_TXDP2	PD-15k	38	SPI_CLK/SMCLK	PD-50k
11	USB3DN_TXDM2	Z	39	SPI_DO/SMDAT	Z
12	VDD12	Z	40	SPI_DI/CFG_BC_EN	Z
13	USB3DN_RXDP2	A/P	41	SPI_CE_N/CFG_NON_REM	Z
14	USB3DN_RXDM2	Z	42	RESET_N	Z
15	VDD12	Z	43	VDD12	PD-50k
16	VDD33	Z	44	VDD33	Z
17	NC	A/P	45	USB2UP_DP	PU-50k
18	NC	A/P	46	USB2UP_DM	Z
19	NC	PD-15k	47	USB3UP_TXDP	Z
20	NC	PD-15k	48	USB3UP_TXDM	R
21	VDD12	Z	49	VDD12	Z
22	NC	Z	50	USB3UP_RXDP	Z
23	NC	A/P	51	USB3UP_RXDM	A/P
24	NC	Z	52	ATEST	A/P
25	NC	Z	53	XTALO	PD-1M
26	NC	PD-15k	54	XTALI/CLK_IN	PD-1M
27	NC	PD-15k	55	VDD33	Z
28	VDD12	Z	56	RBIAS	Z

The pin reset state definitions are detailed in Table 3-2.

TABLE 3-2: PIN RESET STATE LEGEND

Symbol	Description
A/P	Analog/Power Input
R	Reset Control Input
Z	Hardware disables output driver (high impedance)
PU-50k	Hardware enables internal 50kΩ pull-up
PD-50k	Hardware enables internal 50kΩ pull-down
PD-15k	Hardware enables internal 15kΩ pull-down
PD-1M	Hardware enables internal 1M pull-down

3.2 Pin Descriptions

This section contains descriptions of the various USB5742 pins. This pin descriptions have been broken into functional groups as follows:

- USB 3.2 Gen 1 Pin Descriptions
- USB 2.0 Pin Descriptions
- USB Port Control Pin Descriptions
- SPI/SMBus Pin Descriptions
- Miscellaneous Pin Descriptions
- Power and Ground Pin Descriptions

The "_N" symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. For example, **RESET_N** indicates that the reset signal is active low. When "_N" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of "active low" and "Active high" signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

Note: The buffer type for each signal is indicated in the "Buffer Type" column of the pin description tables. A description of the buffer types is provided in Section 3.3, "Buffer Types," on page 15.
For additional information on configuration straps and configurable pins, refer to Section 3.4, "Configuration Straps and Programmable Functions".

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TABLE 3-3: USB 3.2 GEN 1 PIN DESCRIPTIONS

Num Pins	Symbol	Buffer Type	Description
1	**USB3UP_TXDP**	IO-U	USB 3.2 Gen 1 upstream SuperSpeed transmit data plus.
1	**USB3UP_TXDM**	IO-U	USB 3.2 Gen 1 upstream SuperSpeed transmit data minus.
1	**USB3UP_RXDP**	IO-U	USB 3.2 Gen 1 upstream SuperSpeed receive data plus.
1	**USB3UP_RXDM**	IO-U	USB 3.2 Gen 1 upstream SuperSpeed receive data minus.
2	**USBDN_TXDP[2:1]**	IO-U	USB 3.2 Gen 1 downstream ports 2-1 SuperSpeed transmit data plus. **Note:** If unused, leave floating.
2	**USBDN_TXDM[2:1]**	IO-U	USB 3.2 Gen 1 downstream ports 2-1 SuperSpeed transmit data minus. **Note:** If unused, leave floating.
2	**USBDN_RXDP[2:1]**	IO-U	USB 3.2 Gen 1 downstream ports 2-1 SuperSpeed receive data plus. **Note:** If unused, leave floating.
2	**USBDN_RXDM[2:1]**	IO-U	USB 3.2 Gen 1 downstream ports 2-1 SuperSpeed receive data minus. **Note:** If unused, leave floating.

TABLE 3-4: USB 2.0 PIN DESCRIPTIONS

Num Pins	Symbol	Buffer Type	Description
1	**USB2UP_DP**	IO-U	USB 2.0 upstream data plus (D+).
1	**USB2UP_DM**	IO-U	USB 2.0 upstream data minus (D-).
2	**USB2DN_DP[2:1]**	IO-U	USB 2.0 downstream ports 2-1 data plus (D+).
	PRT_DIS_P[2:1]	I	Port 2-1 D+ Disable Configuration Strap. These configuration straps are used in conjunction with the corresponding **PRT_DIS_M[2:1]** straps to disable the related port (2-1). Refer to Section 3.4.2, "Port Disable Configuration (PRT_DIS_P[2:1] / PRT_DIS_M[2:1])" for more information. See Note 2.
2	**USB2DN_DM[2:1]**	IO-U	USB 2.0 downstream ports 2-1 data minus (D-).
	PRT_DIS_M[2:1]	I	Port 2-1 D- Disable Configuration Strap. These configuration straps are used in conjunction with the corresponding **PRT_DIS_P[2:1]** straps to disable the related port (2-1). Refer to Section 3.4.2, "Port Disable Configuration (PRT_DIS_P[2:1] / PRT_DIS_M[2:1])" for more information. See Note 2.

TABLE 3-4: USB 2.0 PIN DESCRIPTIONS (CONTINUED)

Num Pins	Symbol	Buffer Type	Description
1	**VBUS_DET**	IS	This signal detects the state of the upstream bus power. When designing a detachable hub, this pin must be connected to the VBUS power pin of the upstream USB port through a resistor divider (50 kΩ by 100 kΩ) to provide 3.3 V. For self-powered applications with a permanently attached host, this pin must be connected to either 3.3 V or 5.0 V through a resistor divider to provide 3.3 V. In embedded applications, **VBUS_DET** may be controlled (toggled) when the host desires to renegotiate a connection without requiring a full reset of the device.
	GPIO16	I/O6	General purpose input/output 16.

Note 2: Configuration strap values are latched on Power-On Reset (POR) and the rising edge of **RESET_N** (external chip reset). Configuration straps are identified by an underlined symbol name. Signals that function as configurations traps must be augmented with an external resistor when connected to a load. Refer to Section 3.4, "Configuration Straps and Programmable Functions" for additional information.

TABLE 3-5: USB PORT CONTROL PIN DESCRIPTIONS

Num Pins	Symbol	Buffer Type	Description
1	**PRT_CTL1**	I (PU)	Port 1 Power Enable / Overcurrent Sense. **Note:** If unused, leave floating. As an output, this signal is an active high control signal used to enable power to the downstream port 1. As an input, this signal indicates an overcurrent condition from an external current monitor on USB port 1.
1	**PRT_CTL2**	I (PU)	Port 2 Power Enable / Overcurrent Sense. **Note:** If unused, leave floating. As an output, this signal is an active high control signal used to enable power to the downstream port 2. As an input, this signal indicates an overcurrent condition from an external current monitor on USB port 2.

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TABLE 3-6: SPI/SMBUS PIN DESCRIPTIONS

Num Pins	Symbol	Buffer Type	Description
1	SPI_CE_N	O12	Active low SPI chip enable output.
	GPIO7	I/O12	General purpose input/output 7.
	CFG_NON_REM	I	Non-Removable Port Configuration Strap. This configuration strap is used to configure the number of non-removable ports. Refer to Section 3.4.3, "Non-Removable Port Configuration (CFG_NON_REM)" for more information. See Note 3.
1	SPI_CLK	O6	SPI clock output to the serial ROM, when configured for SPI operation.
	SMCLK	OD12	SMBus clock pin, when configured for SMBus slave operation.
	GPIO4	I/O6	General purpose input/output 4.
1	SPI_DO	O6	SPI data output, when configured for SPI operation.
	SMDAT	I/O12	SMBus data pin, when configured for SMBus slave operation.
	GPIO5	I/O6	General purpose input/output 5.
1	SPI_DI	IS	SPI data input, when configured for SPI operation.
	GPIO9	I/O12	General purpose input/output 9.
	CFG_BC_EN	I	Battery Charging Configuration Strap. This configuration strap is used to enable battery charging. Refer to Section 3.4.4, "Battery Charging Configuration (CFG_BC_EN)" for more information. See Note 3.

Note 3: Configuration strap values are latched on Power-On Reset (POR) and the rising edge of RESET_N (external chip reset). Configuration straps are identified by an underlined symbol name. Signals that function as configurations traps must be augmented with an external resistor when connected to a load. Refer to Section 3.4, "Configuration Straps and Programmable Functions" for additional information.

TABLE 3-7: MISCELLANEOUS PIN DESCRIPTIONS

Num Pins	Symbol	Buffer Type	Description
1	RESET_N	IS	The RESET_N pin puts the device into Reset Mode.
1	XTALI	ICLK	External 25 MHz crystal input
	CLK_IN	ICLK	External reference clock input. The device may alternatively be driven by a single-ended clock oscillator. When this method is used, XTALO should be left unconnected.
1	XTALO	OCLK	External 25 MHz crystal output
1	RBIAS	AI	A 12.0 kΩ (+/- 1%) resistor is attached from ground to this pin to set the transceiver's internal bias settings.
1	ATEST	AI	Analog test pin. This signal is used for test purposes and must always be connected to ground.
1	GPIO19	I/O6	General purpose input/output 19.
1	GPIO20	I/O6	General purpose input/output 20.
	GANG_PWR	I (PU)	When pulled high enables gang mode. Gang power pin when used in gang mode.
12	NC	-	No Connect. These pins must be left unconnected for proper operation.

TABLE 3-8: POWER AND GROUND PIN DESCRIPTIONS

Num Pins	Symbol	Buffer Type	Description
4	VDD33	P	+3.3 V power and internal regulator input Refer to Section 4.1, "Power Connections" for power connection information.
8	VDD12	P	+1.2 V core power Refer to Section 4.1, "Power Connections" for power connection information.
Pad	VSS	P	Common ground. This exposed pad must be connected to the ground plane with a via array.

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3.3 Buffer Types

TABLE 3-9: BUFFER TYPES

Buffer Type	Description
I	Input
IS	Schmitt-triggered input
O6	Output with 6 mA sink and 6 mA source
O12	Output with 12 mA sink and 12 mA source
OD12	Open-drain output with 12 mA sink
PU	50 µA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	50 µA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
IO-U	Analog input/output as defined in USB specification
AI	Analog input
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
P	Power pin

Note: Refer to Section 10.5, "DC Specifications" for individual buffer DC electrical characteristics.

3.4 Configuration Straps and Programmable Functions

Configuration straps are multi-function pins that are used during Power-On Reset (POR) or external chip reset (**RESET_N**) to determine the default configuration of a particular feature. The state of the signal is latched following de-assertion of the reset. Configuration straps are identified by an underlined symbol name. This section details the various device configuration straps and associated programmable pin functions.

Note:	The system designer must guarantee that configuration straps meet the timing requirements specified in Section 10.6.2, "Power-On and Configuration Strap Timing," on page 35 and Section 10.6.3, "Reset and Configuration Strap Timing," on page 36. If configuration straps are not at the correct voltage level prior to being latched, the device may capture incorrect strap values.

3.4.1 SPI/SMBUS CONFIGURATION

The SPI/SMBus pins can be configured into one of two functional modes:

- SPI Mode
- SMBus Slave Mode

If 10 kΩ pull-up resistors are detected on **SPI_DO** and **SPI_CLK**, the SPI/SMBus pins are configured into SMBus Slave Mode. If no pull-ups or pull-downs are detected on **SPI_DO** and **SPI_CLK**, the SPI/SMBus pins are first configured into SPI Mode. The strap settings for these supported modes are detailed in Table 3-10. The individual pin function assignments for each mode are detailed in Table 3-11. For additional device connection information, refer to Section 4.0, "Device Connections".

TABLE 3-10: SPI/SMBUS MODE CONFIGURATION SETTINGS

Pin	SPI Mode (Note 4)	SMBus Slave Mode
39 (**SPI_DO**)	No pull-up/down	10 kΩ pull-up
38 (**SPI_CLK**)	No pull-up/down	10 kΩ pull-up

Note 4: In order to use the SPI interface, an SPI ROM containing a valid signature of 2DFU (device firmware upgrade) beginning at address 0xFFFA must be present. Refer to Section 7.1, "SPI Master Interface" for additional information.

TABLE 3-11: SPI/SMBUS MODE PIN ASSIGNMENTS

Pin	SPI Mode	SMBus Slave Mode
41	**SPI_CE_N**	**CFG_NON_REM**
40	**SPI_DI**	**CFG_BC_EN**
39	**SPI_DO**	**SMDAT**
38	**SPI_CLK**	**SMCLK**

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3.4.2 PORT DISABLE CONFIGURATION (PRT_DIS_P[2:1] / PRT_DIS_M[2:1])

The **PRT_DIS_P[2:1]** and **PRT_DIS_M[2:1]** configuration straps are used in conjunction to disable the related port (2-1).

For **PRT_DIS_P*x*** (where *x* is the corresponding port 2-1):

0 = Port *x* D+ Enabled

1 = Port *x* D+ Disabled

For **PRT_DIS_M*x*** (where *x* is the corresponding port 2-1):

0 = Port *x* D- Enabled

1 = Port *x* D- Disabled

Note:	Both **PRT_DIS_P*x*** and **PRT_DIS_M*x*** (where *x* is the corresponding port) must be tied to 3.3 V to disable the associated downstream port. Disabling the USB 2.0 port will also disable the corresponding USB 3.2 Gen 1 port.

3.4.3 NON-REMOVABLE PORT CONFIGURATION (CFG_NON_REM)

The **CFG_NON_REM** configuration strap is used to configure the non-removable port settings of the device to one of three settings. These modes are selected by the configuration of an external resistor on the **CFG_NON_REM** pin. The resistor options are a 200 kΩ pull-down, 200 kΩ pull-up, and 10 kΩ pull-down, as shown in Table 3-12.

TABLE 3-12: CFG_NON_REM RESISTOR ENCODING

CFG_NON_REM Resistor Value	**Setting**
200 kΩ Pull-Down	All ports removable
200 kΩ Pull-Up	Port 1 non-removable
10 kΩ Pull-Down	Port 1, 2 non-removable

3.4.4 BATTERY CHARGING CONFIGURATION (CFG_BC_EN)

The **CFG_BC_EN** configuration strap is used to configure the battery charging port settings of the device to one of three settings. These modes are selected by the configuration of an external resistor on the **CFG_BC_EN** pin. The resistor options are a 200 kΩ pull-down, 200 kΩ pull-up, and 10 kΩ pull-down, as shown in Table 3-13.

TABLE 3-13: CFG_BC_EN RESISTOR ENCODING

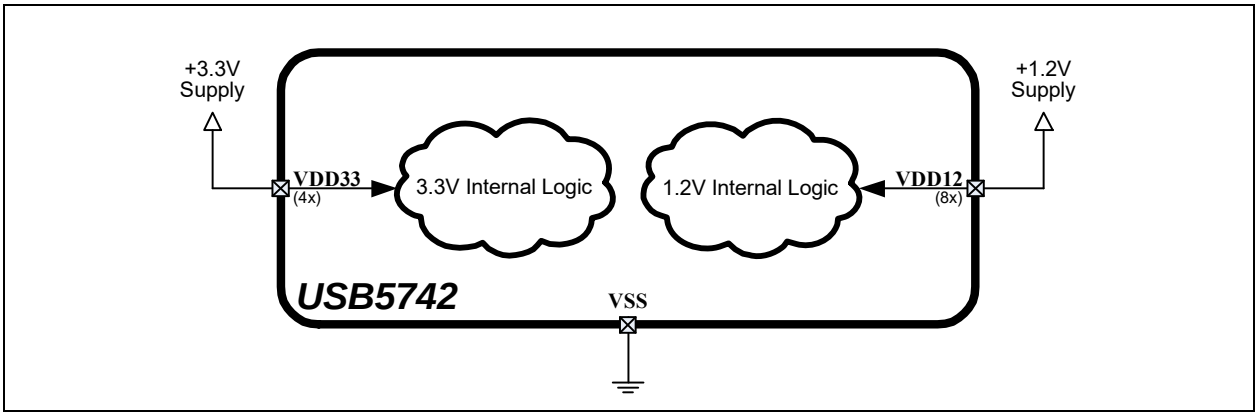
CFG_BC_EN Resistor Value	**Setting**
200 kΩ Pull-Down	No battery charging
200 kΩ Pull-Up	Port 1 battery charging
10 kΩ Pull-Down	Port 1, 2 battery charging

4.0 DEVICE CONNECTIONS

4.1 Power Connections

Figure 4-1 illustrates the device power connections.

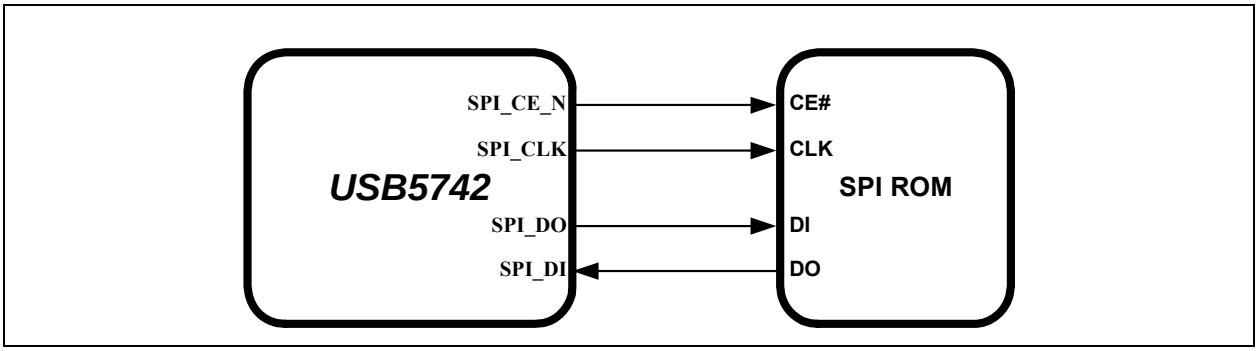
FIGURE 4-1: POWER CONNECTIONS



4.2 SPI ROM Connections

Figure 4-2 illustrates the device SPI ROM connections. Refer to Section 7.1, "SPI Master Interface," on page 24 for additional information on this device interface.

FIGURE 4-2: SPI ROM CONNECTIONS

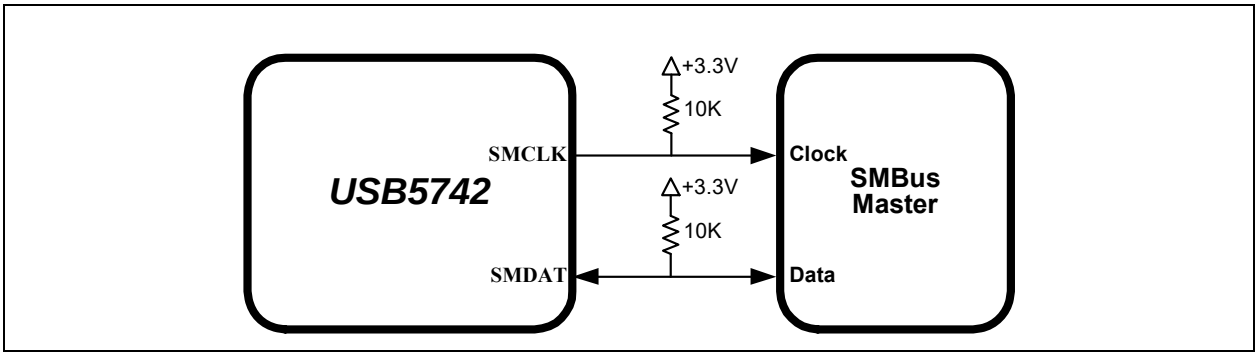


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4.3 SMBus Slave Connections

Figure 4-3 illustrates the device SMBus slave connections. Refer to Section 7.2, "SMBus Slave Interface," on page 24 for additional information on this device interface.

FIGURE 4-3: SMBUS SLAVE CONNECTIONS



5.0 MODES OF OPERATION

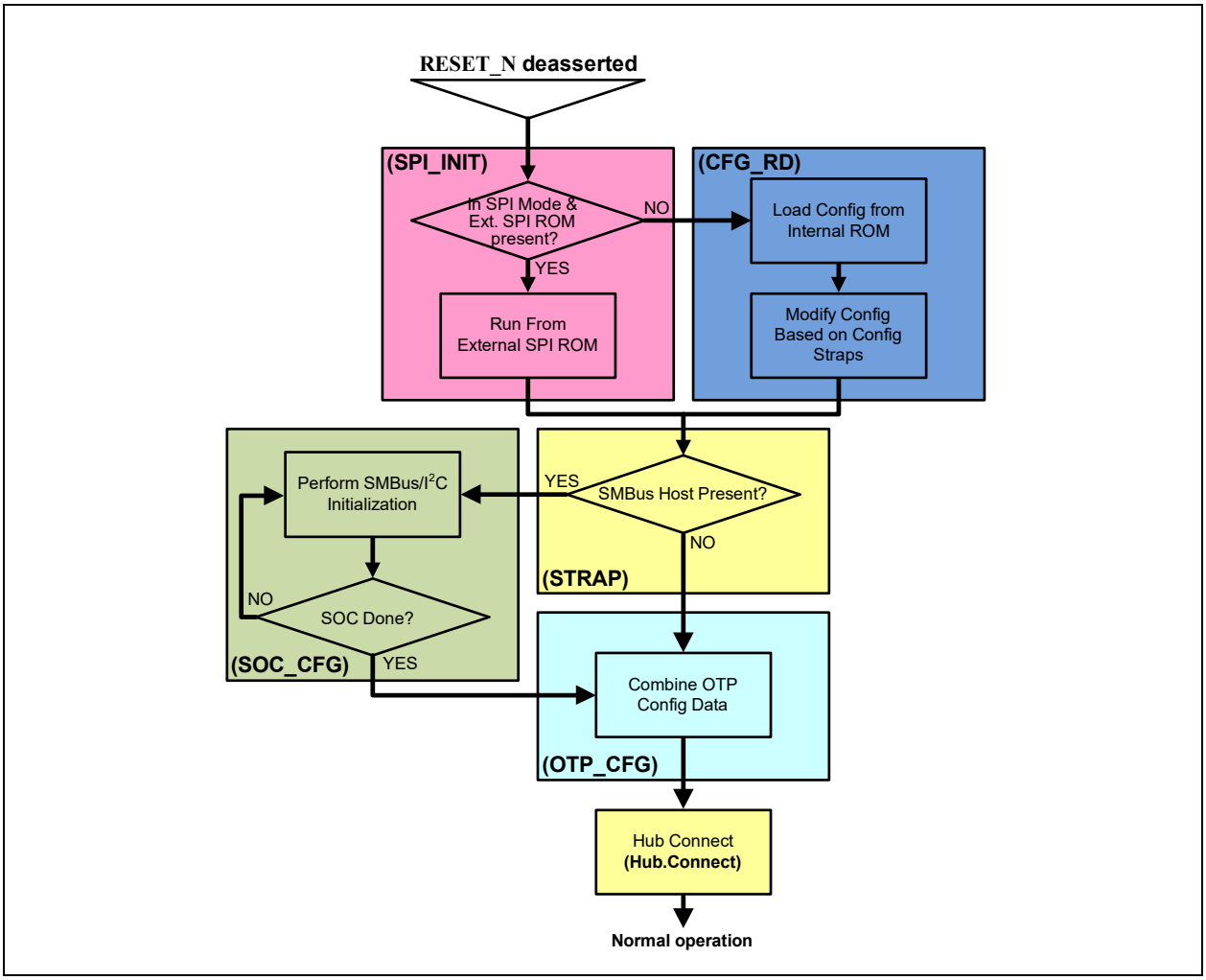
The device provides two main modes of operation: Standby Mode and Hub Mode. These modes are controlled via the RESET_N pin, as shown in Table 5-1.

TABLE 5-1: MODES OF OPERATION

RESET_N Input	Summary
0	**Standby Mode**: This is the lowest power mode of the device. No functions are active other than monitoring the RESET_N input. All port interfaces are high impedance and the PLL is halted. Refer to Section 8.2.2, "External Chip Reset (RESET_N)" for additional information on RESET_N.
1	**Hub (Normal) Mode**: The device operates as a configurable USB hub with battery charger detection. This mode has various sub-modes of operation, as detailed in Figure 5-1. Power consumption is based on the number of active ports, their speed, and amount of data received.

The flowchart in Figure 5-1 details the modes of operation and details how the device traverses through the Hub Mode stages (shown in bold). The remaining sub-sections provide more detail on each stage of operation.

FIGURE 5-1: HUB MODE FLOWCHART



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5.1 Boot Sequence

5.1.1 STANDBY MODE

If the **RESET_N** pin is asserted, the hub will be in Standby Mode. This mode provides a very low power state for maximum power efficiency when no signaling is required. This is the lowest power state. In Standby Mode all downstream ports are disabled, the USB data pins are held in a high-impedance state, all transactions immediately terminate (no states saved), all internal registers return to their default state, the PLL is halted, and core logic is powered down in order to minimize power consumption. Because core logic is powered off, no configuration settings are retained in this mode and must be re-initialized after **RESET_N** is negated high.

5.1.2 SPI INITIALIZATION STAGE (SPI_INIT)

The first stage, the initialization stage, occurs on the deassertion of **RESET_N**. In this stage, the internal logic is reset, the PLL locks if a valid clock is supplied, and the configuration registers are initialized to their default state. The internal firmware then checks for an external SPI ROM. The firmware looks for an external SPI flash device that contains a valid signature of “2DFU” (device firmware upgrade) beginning at address 0xFFFA. If a valid signature is found, then the external ROM is enabled and the code execution begins at address 0x0000 in the external SPI device. If a valid signature is not found, then execution continues from internal ROM (CFG_RD stage).

When using an external SPI ROM, a 1 Mbit, 60 MHz or faster ROM must be used. Both 1- and 2-bit SPI operation are supported. For optimum throughput, a 2-bit SPI ROM is recommended. Both mode 0 and mode 3 SPI ROMs are also supported.

If the system is not strapped for SPI Mode, code execution will continue from internal ROM (CFG_RD stage).

5.1.3 CONFIGURATION READ STAGE (CFG_RD)

In this stage, the internal firmware loads the default values from the internal ROM and then uses the configuration strapping options to override the default values. Refer to Section 3.4, "Configuration Straps and Programmable Functions" for information on usage of the various device configuration straps.

5.1.4 STRAP READ STAGE (STRAP)

In this stage, the firmware registers the configuration strap settings on the **SPI_DO** and **SPI_CLK** pins. Refer to Section 3.4.1, "SPI/SMBus Configuration" for information on configuring these straps. If configured for SMBus Slave Mode, the next state will be SOC_CFG. Otherwise, the next state is OTP_CFG.

5.1.5 SOC CONFIGURATION STAGE (SOC_CFG)

In this stage, the SOC can modify any of the default configuration settings specified in the integrated ROM, such as USB device descriptors and port electrical settings.

There is no time limit on this mode. In this stage the firmware will wait indefinitely for the SMBus/I^2C configuration. When the SOC has completed configuring the device, it must write to register 0xFF to end the configuration.

5.1.6 OTP CONFIGURATION STAGE (OTP_CFG)

Once the SOC has indicated that it is done with configuration, all configuration data is combined in this stage. The default data, the SOC configuration data, and the OTP data are all combined in the firmware and the device is programmed.

After the device is fully configured, it will go idle and then into suspend if there is no VBUS or Hub.Connect present. Once VBUS is present, and battery charging is enabled, the device will transition to the Battery Charger Detection Stage. If VBUS is present, and battery charging is not enabled, the device will transition to the Connect stage.

5.1.7 HUB CONNECT STAGE (HUB.CONNECT)

Once the CHGDET stage is completed, the device enters the Hub Connect stage. USB connect can be initiated by asserting the VBUS pin function high. The device will remain in the Hub Connect stage indefinitely until the VBUS pin function is deasserted.

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5.1.8 NORMAL MODE

Lastly, the hub enters Normal Mode of operation. In this stage full USB operation is supported under control of the USB Host on the upstream port. The device will remain in the normal mode until the operating mode is changed by the system.

If **RESET_N** is asserted low, then Standby Mode is entered. The device may then be placed into any of the designated hub stages. Asserting a soft disconnect on the upstream port will cause the hub to return to the Hub.Connect stage until the soft disconnect is negated.

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6.0 DEVICE CONFIGURATION

The device supports a large number of features (some mutually exclusive), and must be configured in order to correctly function when attached to a USB host controller. The hub can be configured either internally or externally depending on the implemented interface.

Microchip provides a comprehensive software programming tool, Pro-Touch, for configuring the USB5742 functions, registers and OTP memory. All configuration is to be performed via the Pro-Touch programming tool. For additional information on the Pro-Touch programming tool, refer to the Software Libraries within the Microchip USB5742 product page at www.microchip.com/USB5742.

Note: Device configuration straps and programmable pins are detailed in Section 3.4, "Configuration Straps and Programmable Functions," on page 16.
Refer to Section 7.0, "Device Interfaces" for detailed information on each device interface.

6.1 Customer Accessible Functions

The following USB or SMBus accessible functions are available to the customer via the Pro-Touch Programming Tool.

Note: For additional programming details, refer to the Pro-Touch programming tool.

6.1.1 USB ACCESSIBLE FUNCTIONS

6.1.1.1 OTP Access over USB

The OTP ROM in the device is accessible via the USB bus. All OTP parameters can be modified to the USB Host. The OTP operates in Single Ended mode. For more information, refer to the Microchip USB5742 product page and SDK at www.microchip.com/USB5742

6.1.1.2 Battery Charging Access over USB

The Battery charging behavior of the device can be dynamically changed by the USB Host when something other than the preprogrammed or OTP programmed behavior is desired. For more information, refer to the Microchip USB5742 product page and SDK at www.microchip.com/USB5742

6.1.2 SMBUS ACCESSIBLE FUNCTIONS

OTP access and configuration of specific device functions are possible via the USB5742 SMBus. All OTP parameters can be modified via the SMBus Host. The OTP can be programmed to operate in Single-Ended, Differential, Redundant, or Differential Redundant mode, depending on the level of reliability required. For more information, refer to AN1903 - “Configuration Options for the USB5734 and USB5744” application note at www.microchip.com/AN1903.

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7.0 DEVICE INTERFACES

The USB5742 provides multiple interfaces for configuration and external memory access. This section details the various device interfaces and their usage:

- SPI Master Interface
- SMBus Slave Interface

Note:	For details on how to enable each interface, refer to Section 3.4.1, "SPI/SMBus Configuration". For information on device connections, refer to Section 4.0, "Device Connections". For information on device configuration, refer to Section 6.0, "Device Configuration". Microchip provides a comprehensive software programming tool, Pro-Touch, for configuring the USB5742 functions, registers and OTP memory. All configuration is to be performed via the Pro-Touch programming tool. For additional information on the Pro-Touch programming tool, refer to Software Libraries within Microchip USB5742 product page at www.microchip.com/USB5742.

7.1 SPI Master Interface

The device is capable of code execution from an external SPI ROM. When configured for SPI Mode, on power up the firmware looks for an external SPI flash device that contains a valid signature of 2DFU (device firmware upgrade) beginning at address 0xFFFA. If a valid signature is found, then the external ROM is enabled and the code execution begins at address 0x0000 in the external SPI device. If a valid signature is not found, then execution continues from internal ROM.

Note:	For SPI timing information, refer to Section 10.6.7, "SPI Timing".

7.2 SMBus Slave Interface

The device includes an integrated SMBus slave interface, which can be used to access internal device run time registers or program the internal OTP memory. SMBus slave detection is accomplished by detection of pull-up resistors on both the **SMDAT** and **SMCLK** signals. Refer to Section 3.4.1, "SPI/SMBus Configuration" for additional information.

Note:	All device configuration must be performed via the Pro-Touch Programming Tool. For additional information on the Pro-Touch programming tool, refer to Software Libraries within Microchip USB5742 product page at www.microchip.com/USB5742.

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8.0 FUNCTIONAL DESCRIPTIONS

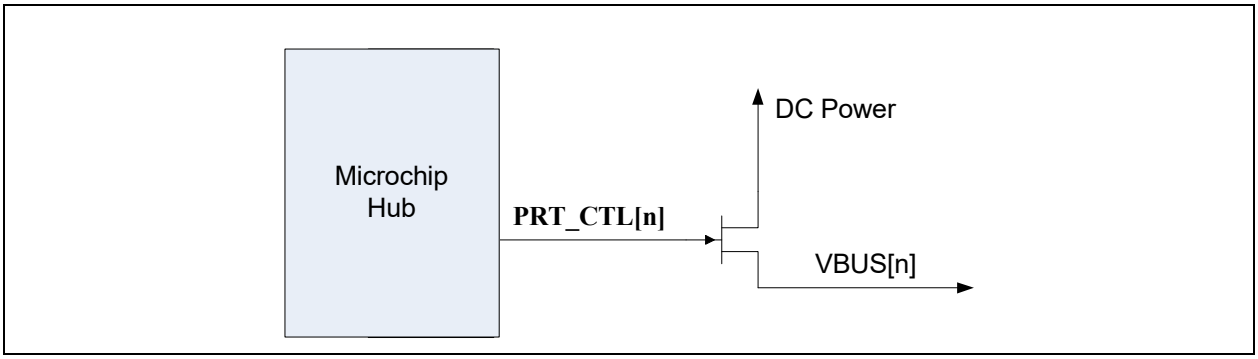
This section details various USB5742 functions, including:

- Downstream Battery Charging
- Resets
- Link Power Management (LPM)
- Port Control Interface

8.1 Downstream Battery Charging

The device can be configured by an OEM to have any of the downstream ports support battery charging. The hub's role in battery charging is to provide acknowledgment to a device's query as to whether the hub system supports USB battery charging. The hub silicon does not provide any current or power FETs or any additional circuitry to actually charge the device. Those components must be provided externally by the OEM.

FIGURE 8-1: BATTERY CHARGING EXTERNAL POWER SUPPLY



If the OEM provides an external supply capable of supplying current per the battery charging specification, the hub can be configured to indicate the presence of such a supply from the device. This indication, via the **PRT_CTL[2:1]** pins, is on a per port basis. For example, the OEM can configure two ports to support battery charging through high current power FETs and leave the other two ports as standard USB ports.

For additional information, refer to the Microchip USB5742 Battery Charging application note on the Microchip.com USB5742 product page at www.microchip.com/USB5742.

8.2 Resets

The device includes the following chip-level reset sources:

- Power-On Reset (POR)
- External Chip Reset (RESET_N)
- USB Bus Reset

8.2.1 POWER-ON RESET (POR)

A power-on reset occurs whenever power is initially supplied to the device, or if power is removed and reapplied to the device. A timer within the device will assert the internal reset per the specifications listed in Section 10.6.2, "Power-On and Configuration Strap Timing," on page 35.

8.2.2 EXTERNAL CHIP RESET (RESET_N)

A valid hardware reset is defined as assertion of RESET_N, after all power supplies are within operating range, per the specifications in Section 10.6.3, "Reset and Configuration Strap Timing," on page 36. While reset is asserted, the device (and its associated external circuitry) enters Standby Mode and consumes minimal current.

Assertion of RESET_N causes the following:

1. The PHY is disabled and the differential pairs will be in a high-impedance state.
2. All transactions immediately terminate; no states are saved.
3. All internal registers return to the default state.
4. The external crystal oscillator is halted.
5. The PLL is halted.

Note: All power supplies must have reached the operating levels mandated in Section 10.2, "Operating Conditions**," on page 31, prior to (or coincident with) the assertion of RESET_N.

8.2.3 USB BUS RESET

In response to the upstream port signaling a reset to the device, the device performs the following:

Note: The device does not propagate the upstream USB reset to downstream devices.

1. Sets default address to 0.
2. Sets configuration to Unconfigured.
3. Moves device from suspended to active (if suspended).
4. Complies with the USB Specification for behavior after completion of a reset sequence.

The host then configures the device in accordance with the USB Specification.

8.3 Link Power Management (LPM)

The device supports the L0 (On), L1 (Sleep), and L2 (Suspend) link power management states. These supported LPM states offer low transitional latencies in the tens of microseconds versus the much longer latencies of the traditional USB suspend/resume in the tens of milliseconds. The supported LPM states are detailed in Table 8-1.

TABLE 8-1: LPM STATE DEFINITIONS

State	Description	Entry/Exit Time to L0
L2	Suspend	Entry: ~3 ms Exit: ~2 ms (from start of RESUME)
L1	Sleep	Entry: <10 us Exit: <50 us
L0	Fully Enabled (On)	-

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8.4 Port Control Interface

Port power and over-current sense share the same pin (**PRT_CTLx**) for each port. These functions can be controlled directly from the USB hub, or via the processor.

The device can be configured into the following port control modes:

- Ganged Mode
- Combined Mode

Port connection in various modes are detailed in the following subsections.

8.4.1 PORT CONNECTION IN GANGED MODE

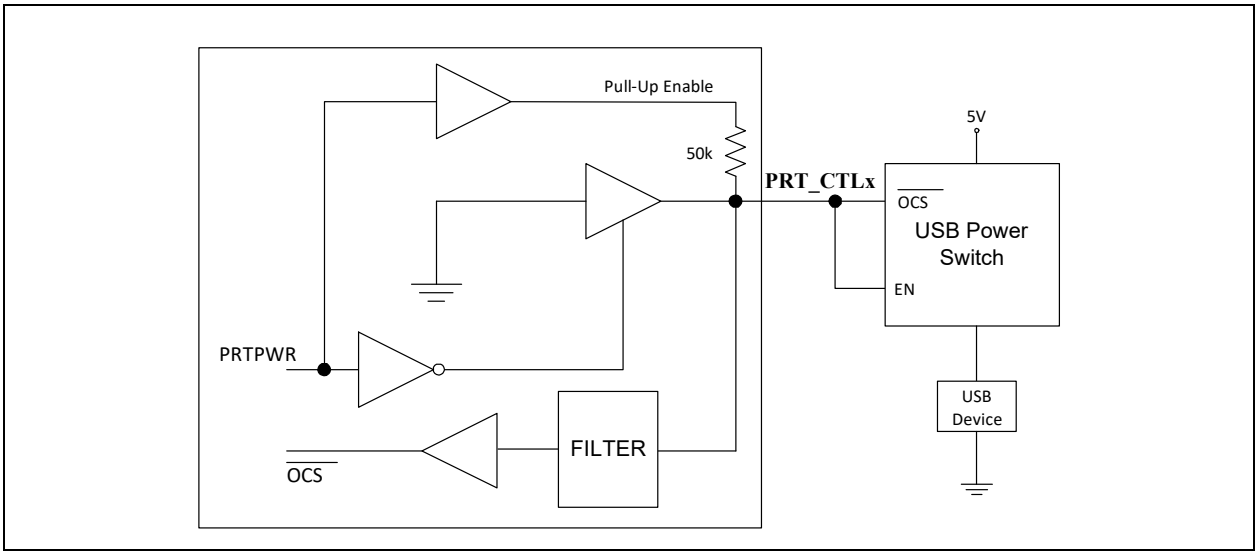
In this mode, one pin (**GANG_PWR**) is used to control port power and over-current sensing.

8.4.2 PORT CONNECTION IN COMBINED MODE

8.4.2.1 Port Power Control using USB Power Switch

When operating in combined mode, the device will have one port power control and over-current sense pin for each downstream port. When disabling port power, the driver will actively drive a '0'. To avoid unnecessary power dissipation, the pull-up resistor will be disabled at that time. When port power is enabled, it will disable the output driver and enable the pull-up resistor, making it an open drain output. If there is an over-current situation, the USB Power Switch will assert the open drain OCS signal. The Schmidt trigger input will recognize that as a low. The open drain output does not interfere. The over-current sense filter handles the transient conditions such as low voltage while the device is powering up.

FIGURE 8-2: PORT POWER CONTROL WITH USB POWER SWITCH



When the port is enabled, the **PRT_CTLx** pin input is constantly sampled. Overcurrent events can be detected in one of two ways:

- Single, continuous low pulse (consecutive low samples over t_{ocs_single}), as shown in Figure 8-3.
- Two short low pulses within a rolling window (two groupings of 1 or more low samples over t_{ocs_double}), as shown in Figure 8-4.

FIGURE 8-3: SINGLE LOW PULSE OVERCURRENT DETECTION

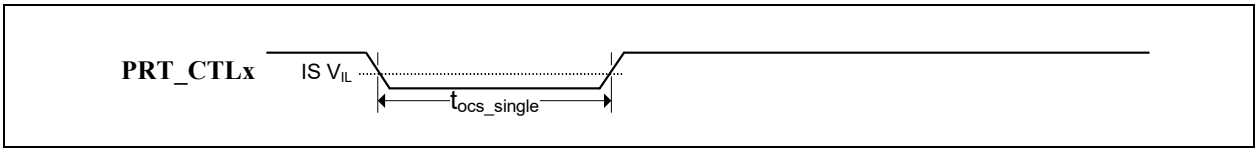


FIGURE 8-4: DOUBLE LOW PULSE OVERCURRENT DETECTION

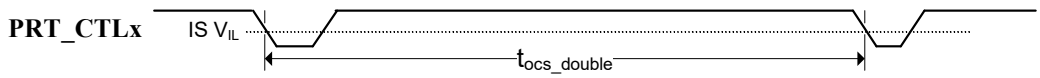


TABLE 8-2: OVERCURRENT PULSE TIMING

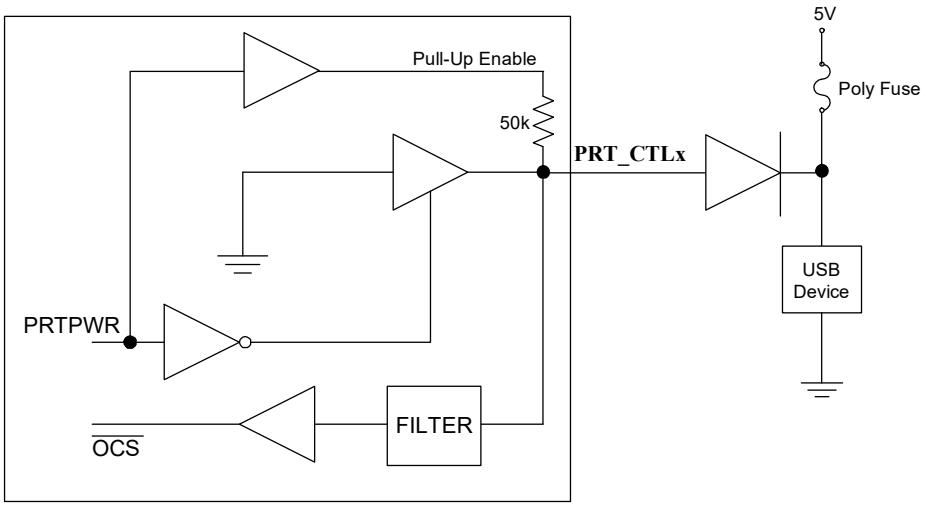
Symbol	Description	Min	Max	Units
t_{ocs_single}	single low pulse assertion time	5	-	ms
t_{ocs_double}	double low pulse window	-	20	ms

8.4.2.2 Port Power Control using Poly Fuse

When using the device with a poly fuse, there is no need for an output power control. To maintain consistency, the same circuit will be used. A single port power control and over-current sense for each downstream port is still used from the Hub's perspective. When disabling port power, the driver will actively drive a '0'. This will have no effect as the external diode will isolate pin from the load. When port power is enabled, it will disable the output driver and enable the pull-up resistor. This means that the pull-up resistor is providing 3.3 volts to the anode of the diode. If there is an over-current situation, the poly fuse will open. This will cause the cathode of the diode to go to 0 volts. The anode of the diode will be at 0.7 volts, and the Schmidt trigger input will register this as a low resulting in an over-current detection. The open drain output does not interfere.

Note: The USB 2.0 and USB 3.2 Gen 1 bPwrOn2PwrGood descriptors must be set to 0 when using poly-fuse mode. Refer to Microchip application note AN1903 “Configuration Options for the USB5734 and USB5744” for details on how to change these values.

FIGURE 8-5: PORT POWER CONTROL USING A POLY FUSE

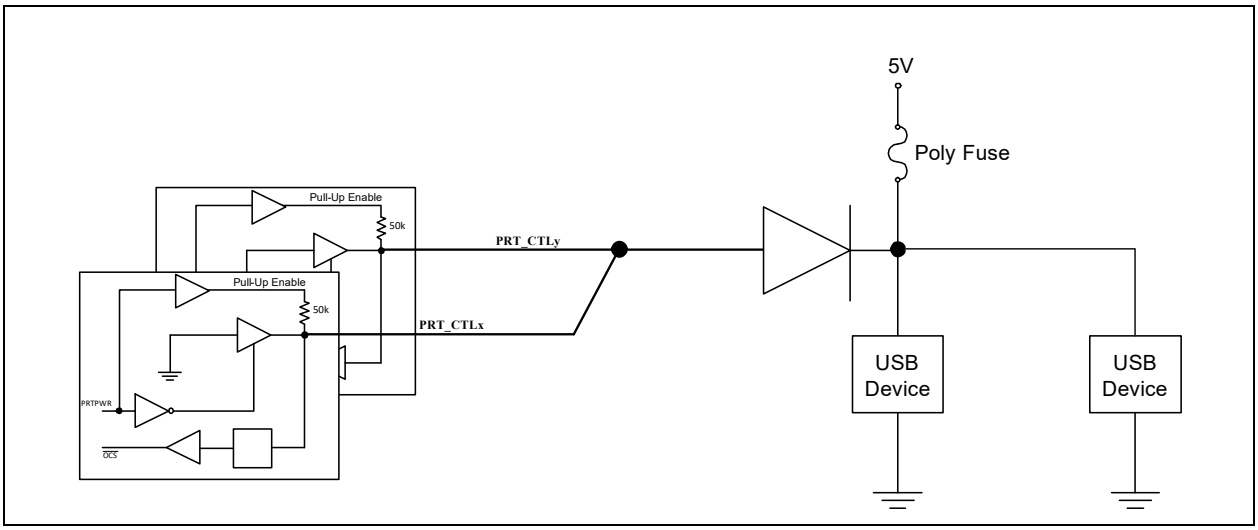


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8.4.2.3 Port Power Control with Single Poly Fuse and Multiple Loads

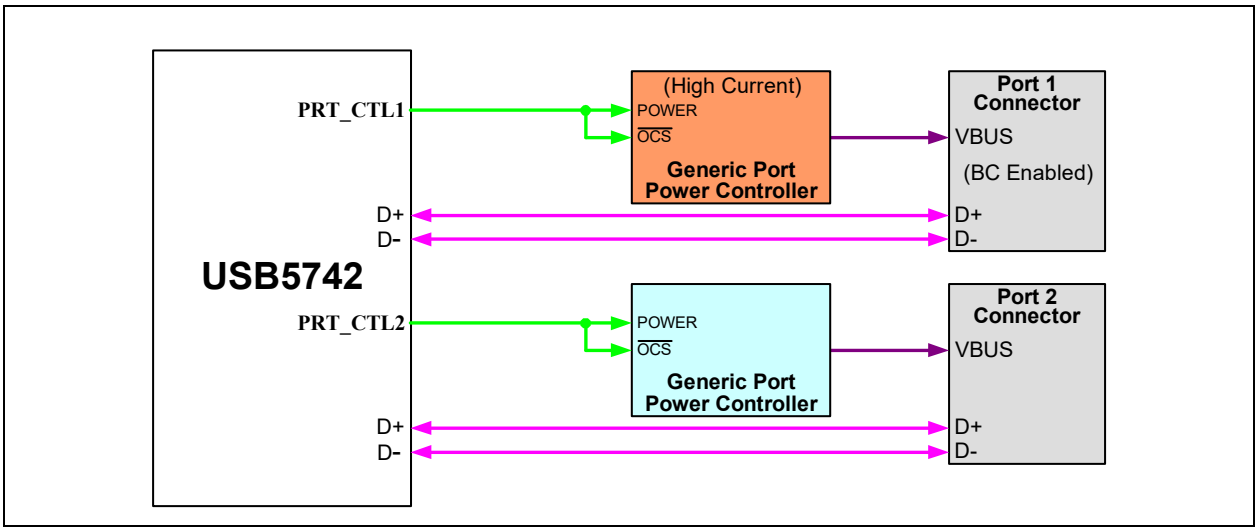
Many customers use a single poly fuse to power all their devices. For the ganged situation, all power control pins must be tied together.

FIGURE 8-6: PORT POWER CONTROL WITH GANGED CONTROL WITH POLY FUSE



8.4.3 PORT CONTROLLER CONNECTION EXAMPLE

FIGURE 8-7: USB5742 WITH 2 GENERIC PORT POWER CONTROLLERS (1 BC ENABLED)



Note: The **CFG_BC_EN** configuration strap must be properly configured to enable battery charging on the appropriate ports. For example, in the application shown in Figure 8-7, **CFG_BC_EN** must be connected to an external 200 kΩ pull-up resistor to enable battery charging on Port 1 only. For more information on the **CFG_BC_EN** configuration strap, refer to Section 3.4.4, "Battery Charging Configuration (CFG_BC_EN)".

9.0 COMPLIANCE UPDATE

In order to be USB-IF certified (TID 330000076), the USB5742 supports the USB 3.2 Engineering Change Notices (ECNs) included in the *Universal Serial Bus Revision 3.2 Specification*. This allows the latest revision of the USB5742 to be certified in compliance with USB-IF logo testing for the new USB Type-C® industry initiative. The following compliance updates are supported:

- Pending Header Packet (HP) Timer (TD7.9, TD7.11, TD7.26)
- Power Management (PM) Timer (TD7.18, TD7.20, TD7.23)
- Unacknowledged Connect and Remote Wake Test Failure (TD10.25)

These USB 3.2 ECNs can be found as part of the *Universal Serial Bus Revision 3.2 Specification* zip file, which can be downloaded from the USB developers website (http://www.usb.org/developers/docs/).

9.1 Pending Header Packet (HP) Timer (TD7.9, TD7.11, TD7.26)

A turn around time is defined between the communication of a Host and Device (Link Partners) for an acknowledgment of a USB connection. The time is budgeted between a number of steps (Transmit/Receive data path of the initiator, the delay in the cable, and the response time of the responder). If the time is exceeded, no USB communication is initiated.

The ECN calls to relax the timing from 3us to 10us at the link and PHY layers to allow for an extended propagation delay to account for the usage of active cables and retimers in new SuperSpeed Plus designs.

Impact to Legacy Systems:

- A new host with a retimer connected to an active cable AND a legacy device
- A legacy host connected to an active cable and a new device with or without a retimer

9.2 Power Management (PM) Timer (TD7.18, TD7.20, TD7.23)

There are three timers for link power management: PM_LC_TIMER, PM_ENTRY_TIMER, and Ux_EXIT_TIMER. The PM_LC_TIMER is used for a port initiating an entry request to a low power link state. The PM_ENTRY_TIMER is used for a port accepting the entry request to a low power link state. Ux_EXIT_TIMER is used for a port to initiate the exit from U1 or U2 to a low power state.

The ECN calls to increase the maximum timeout values to accommodate for the new connectivity models with retimers and active cables beyond the standard USB-IF transmission lengths.

Impact to Legacy Systems:

- No impact to USB 3.0 or early USB 3.2 ecosystems

9.3 Unacknowledged Connect and Remote Wake Test Failure (TD10.25)

If a USB3 port with a connected device is placed into Suspend and RemoteWake is set but the RemoteWake mask (C_PORT_CONNECTION bit) has not been cleared, the USB3 hub will automatically issue a wake up signal to the host.

In legacy systems, if a USB3 port with a connected device was placed into Suspend and RemoteWake is set without the mask bit being cleared, the USB3 hub would NOT issue a wake up signal to the host.

Impact to Legacy Systems:

- No impact – with the new implementation, a remote wake is automatically initiated if the mask bit is not set. In older systems the remote wake may or may not have been executed.

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10.0 OPERATIONAL CHARACTERISTICS

10.1 Absolute Maximum Ratings*

+1.2 V Supply Voltage (**VDD12**) (Note 1) . . . . . -0.5 V to +1.32 V

+3.3 V Supply Voltage (**VDD33**) (Note 1) . . . . . -0.5 V to +4.6 V

Positive voltage on input signal pins, with respect to ground (Note 2) . . . . . +4.6 V

Negative voltage on input signal pins, with respect to ground . . . . . -0.5 V

Positive voltage on **XTALI/CLK_IN**, with respect to ground . . . . . +3.63 V

Positive voltage on USB DP/DM signal pins, with respect to ground . . . . . +6.0 V

Positive voltage on USB 3.2 Gen 1 **USB3UP_*xxxx*** and **USB3DN_*xxxx*** signal pins, with respect to ground . . . . . 1.32 V

Storage Temperature . . . . . -55°C to +150°C

Junction Temperature . . . . . +125°C

Lead Temperature Range . . . . . Refer to JEDEC Spec. J-STD-020

HBM ESD Performance . . . . . 3 kV

Note 1: When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested to use a clamp circuit.

Note 2: This rating does not apply to the following pins: All USB DM/DP pins, **XTAL1/CLK_IN**, and **XTALO**

*Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in Section 10.2, "Operating Conditions**", Section 10.5, "DC Specifications", or any other applicable section of this specification is not implied.

10.2 Operating Conditions**

+1.2 V Supply Voltage (**VDD12**) . . . . . +1.08 V to +1.32 V

+3.3 V Supply Voltage (**VDD33**) . . . . . +3.0 V to +3.6 V

Input Signal Pins Voltage (Note 2) . . . . . -0.3 V to +3.6 V

XTALI/CLK_IN Voltage . . . . . -0.3 V to +3.6 V

USB 2.0 DP/DM Signal Pins Voltage . . . . . -0.3 V to +5.5 V

USB 3.2 Gen 1 **USB3UP_*xxxx*** and **USB3DN_*xxxx*** Signal Pins Voltage . . . . . -0.3 V to +1.32 V

Ambient Operating Temperature in Still Air (T_A) . . . . . Note 3

+1.2 V Supply Voltage Rise Time (T_{RT} in Figure 10-1) 5ms

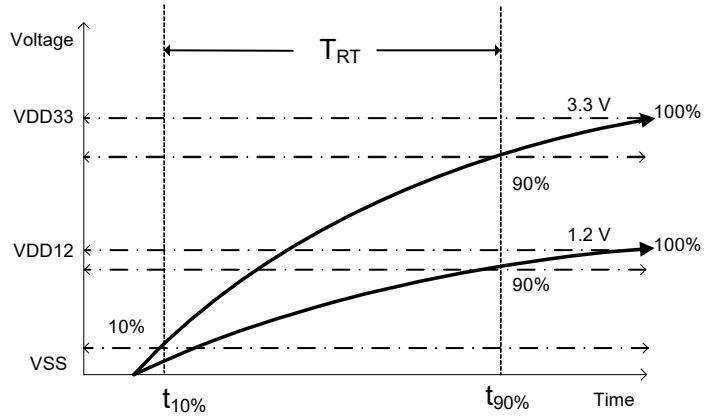
+3.3 V Supply Voltage Rise Time (T_{RT} in Figure 10-1) 5ms

Note 3: 0°C to +70°C for commercial version, -40°C to +85°C for industrial version.

**Proper operation of the device is guaranteed only within the ranges specified in this section.

Note:	Do not drive input signals without power supplied to the device.

FIGURE 10-1: SUPPLY RISE TIME MODEL



Note: The rise time for the 1.2V and 3.3V supplies can be extended to 100 ms max if RESET_N is actively driven low, typically by another IC, until 1 us after all supplies are within operating range.

10.3 Package Thermal Specifications

TABLE 10-1: PACKAGE THERMAL PARAMETERS

Symbol	°C/W	Velocity (Meters/s)
Θ_{JA}	30	0
	26	1
Ψ_{JT}	0.2	0
	0.3	1
Θ_{JC}	2.6	0
	2.6	1

Note: Thermal parameters are measured or estimated for devices in a multi-layer 2S2P PCB per JESDN51.

TABLE 10-2: MAXIMUM POWER DISSIPATION

Parameter	Value	Units
PD(max)	1400	mW

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10.4 Power Consumption

This section details the power consumption of the device as measured during various modes of operation. Power dissipation is determined by temperature, supply voltage, and external source/sink requirements.

TABLE 10-3: DEVICE POWER CONSUMPTION

	Typical (mA)		Typical Power
	VDD33	VDD12	(mW)
Reset	0.8	1.8	4.8
No VBUS	2.0	4.0	11.4
Global Suspend	2.0	4.1	11.5
2 HS Ports	35	26	146
2 SS Ports	40	441	661
2 SS/HS Ports	64	445	745

10.5 DC Specifications

TABLE 10-4: I/O DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typical	Max	Units	Notes
I Type Input Buffer						
Low Input Level	V_{IL}			0.9	V	
High Input Level	V_{IH}	2.1			V	
IS Type Input Buffer						
Low Input Level	V_{IL}			0.9	V	
High Input Level	V_{IH}	1.9			V	
Schmitt Trigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	9	20	40	mV	
O6 Type Output Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 6 mA
High Output Level	V_{OH}	**VDD33**-0.4			V	I_{OH} = -6 mA
O12 Type Output Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA
High Output Level	V_{OH}	**VDD33**-0.4			V	I_{OH} = -12 mA
OD12 Type Output Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA
ICLK Type Input Buffer (XTALI Input)						Note 4
Low Input Level	V_{IL}			0.50	V	
High Input Level	V_{IH}	0.85		**VDD33**	V	
IO-U Type Buffer (See Note 5)						Note 5

Note 4: **XTALI** can optionally be driven from a 25 MHz singled-ended clock oscillator.

Note 5: Refer to the USB 3.2 Gen 1 Specification for USB DC electrical characteristics.

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10.6 AC Specifications

This section details the various AC timing specifications of the device.

10.6.1 POWER SUPPLY AND RESET_N SEQUENCE TIMING

Figure 10-2 illustrates the recommended power supply sequencing and timing for the device. **VDD33** should rise after or at the same rate as **VDD12**. Similarly, **RESET_N** and/or **VBUS_DET** should rise after or at the same rate as **VDD33**. **VBUS_DET** and **RESET_N** do not have any other timing dependencies.

FIGURE 10-2: POWER SUPPLY AND RESET_N SEQUENCE TIMING

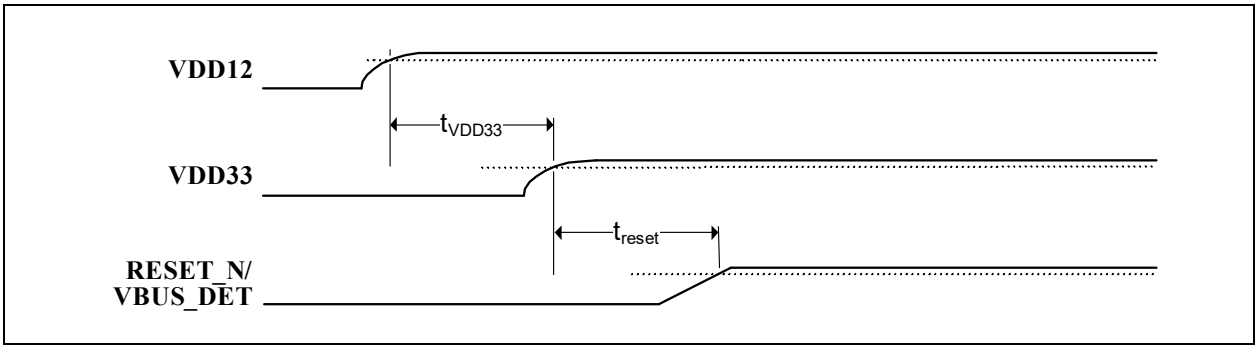


TABLE 10-5: POWER SUPPLY AND RESET_N SEQUENCE TIMING

Symbol	Description	Min	Typ	Max	Units
t_{VDD33}	**VDD12** to **VDD33** rise time	0			ms
t_{reset}	**VDD33** to **RESET_N/VBUS_DET** rise time	0			ms

10.6.2 POWER-ON AND CONFIGURATION STRAP TIMING

Figure 10-3 illustrates the configuration strap valid timing requirements in relation to power-on, for applications where **RESET_N** is not used at power-on. In order for valid configuration strap values to be read at power-on, the following timing requirements must be met. The operational levels (V_{opp}) for the external power supplies are detailed in Section 10.2, "Operating Conditions**," on page 31.

FIGURE 10-3: POWER-ON CONFIGURATION STRAP VALID TIMING

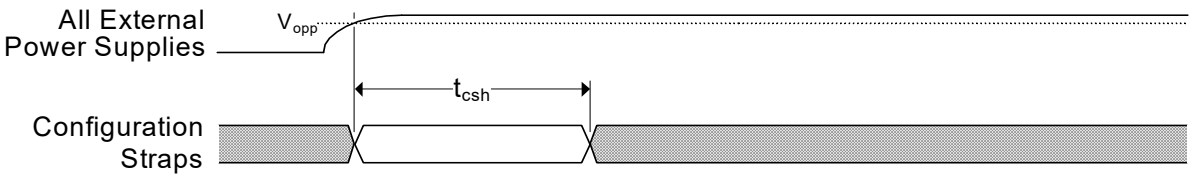


TABLE 10-6: POWER-ON CONFIGURATION STRAP LATCHING TIMING

Symbol	Description	Min	Typ	Max	Units
t_{csh}	Configuration strap hold after external power supplies at operational levels	1			ms

Device configuration straps are also latched as a result of **RESET_N** assertion. Refer to Section 10.6.3, "Reset and Configuration Strap Timing" for additional details.

10.6.3 RESET AND CONFIGURATION STRAP TIMING

Figure 10-4 illustrates the **RESET_N** pin timing requirements and its relation to the configuration strap pins. Assertion of **RESET_N** is not a requirement. However, if used, it must be asserted for the minimum period specified. Refer to Section 8.2, "Resets" for additional information on resets. Refer to Section 3.4, "Configuration Straps and Programmable Functions" for additional information on configuration straps.

FIGURE 10-4: RESET_N CONFIGURATION STRAP TIMING

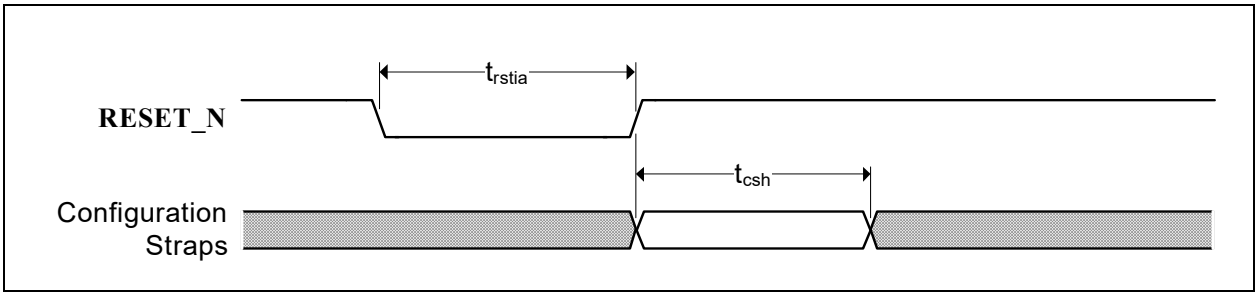


TABLE 10-7: RESET_N CONFIGURATION STRAP TIMING

Symbol	Description	Min	Typ	Max	Units
t_{rstia}	**RESET_N** input assertion time	5			µs
t_{csh}	Configuration strap pins hold after **RESET_N** deassertion	1			ms

Note: The clock input must be stable prior to **RESET_N** deassertion.

Configuration strap latching and output drive timings shown assume that the Power-On reset has finished first otherwise the timings in Section 10.6.2, "Power-On and Configuration Strap Timing" apply.

10.6.4 USB TIMING

All device USB signals conform to the voltage, power, and timing characteristics/specifications as set forth in the *Universal Serial Bus Specification*. Please refer to the *Universal Serial Bus Revision 3.2 Specification*, available at http://www.usb.org/developers/docs.

10.6.5 I^2C TIMING

All device I^2C signals conform to the 400KHz Fast Mode (Fm) voltage, power, and timing characteristics/specifications as set forth in the *I^2C-Bus Specification*. Please refer to the *I^2C-Bus Specification*, available at http://www.nxp.com/documents/user_manual/UM10204.pdf.

10.6.6 SMBUS TIMING

All device SMBus signals conform to the voltage, power, and timing characteristics/specifications as set forth in the *System Management Bus Specification.* Please refer to the *System Management Bus Specification*, Version 1.0, available at http://smbus.org/specs.

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10.6.7 SPI TIMING

This section specifies the SPI timing requirements for the device.

FIGURE 10-5: SPI TIMING

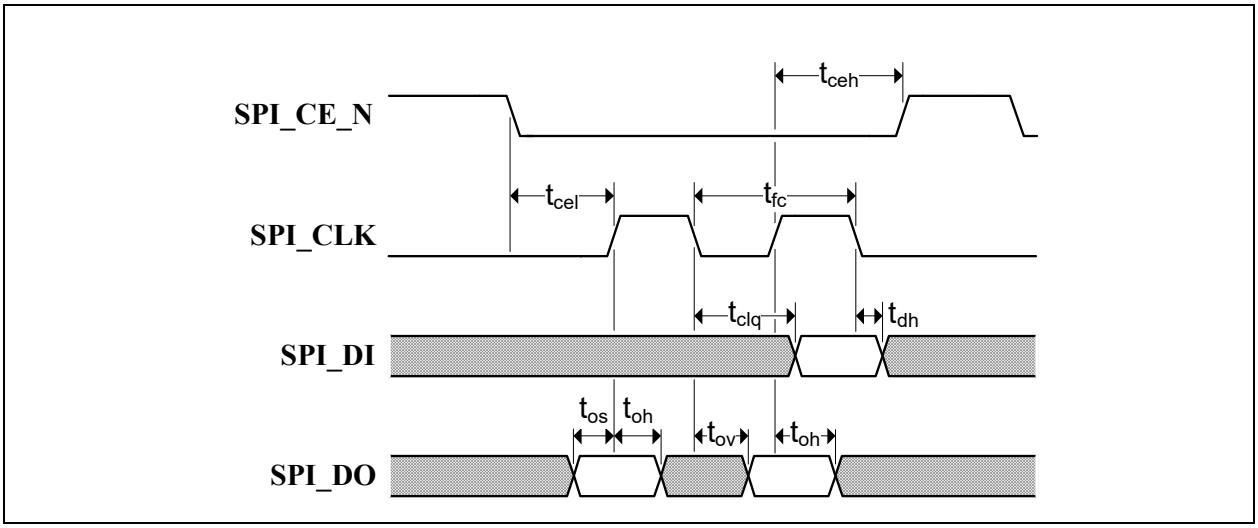


TABLE 10-8: SPI TIMING (30 MHZ OPERATION)

Symbol	Description	Min	Typ	Max	Units
t_{fc}	Clock frequency			30	MHz
t_{ceh}	Chip enable (**SPI_CE_EN**) high time	100			ns
t_{clq}	Clock to input data			13	ns
t_{dh}	Input data hold time	0			ns
t_{os}	Output setup time	5			ns
t_{oh}	Output hold time	5			ns
t_{ov}	Clock to output valid	4			ns
t_{cel}	Chip enable (**SPI_CE_EN**) low to first clock	12			ns
t_{ceh}	Last clock to chip enable (**SPI_CE_EN**) high	12			ns

TABLE 10-9: SPI TIMING (60 MHZ OPERATION)

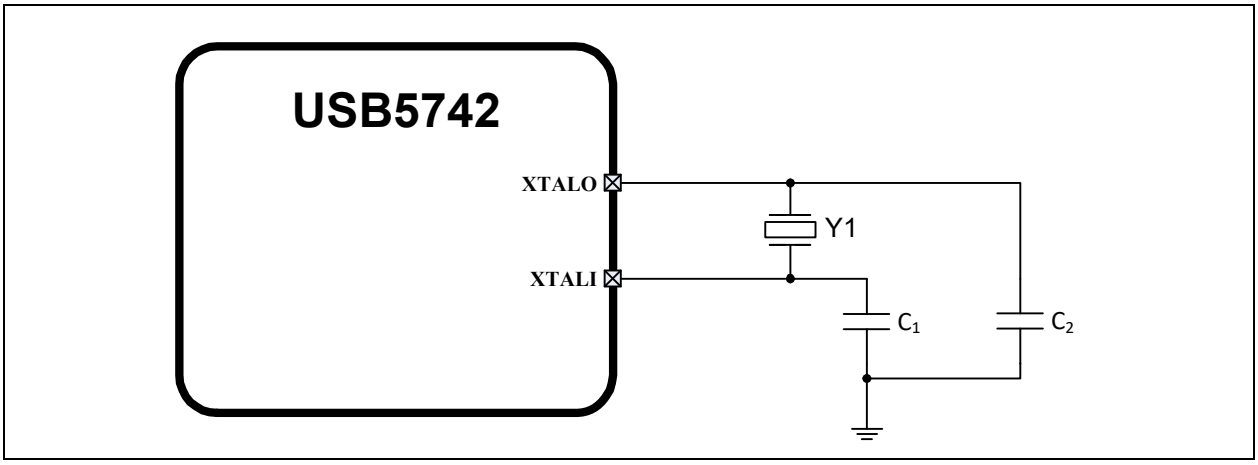
Symbol	Description	Min	Typ	Max	Units
t_{fc}	Clock frequency			60	MHz
t_{ceh}	Chip enable (**SPI_CE_EN**) high time	50			ns
t_{clq}	Clock to input data			9	ns
t_{dh}	Input data hold time	0			ns
t_{os}	Output setup time	5			ns
t_{oh}	Output hold time	5			ns
t_{ov}	Clock to output valid	4			ns
t_{cel}	Chip enable (**SPI_CE_EN**) low to first clock	12			ns
t_{ceh}	Last clock to chip enable (**SPI_CE_EN**) high	12			ns

10.7 Clock Specifications

The device can accept either a 25MHz crystal or a 25MHz single-ended clock oscillator (±50ppm) input. If the single-ended clock oscillator method is implemented, **XTALO** should be left unconnected and **XTALI/CLK_IN** should be driven with a nominal 0-3.3V clock signal. The input clock duty cycle is 40% minimum, 50% typical and 60% maximum.

It is recommended that a crystal utilizing matching parallel load capacitors be used for the crystal input/output signals (**XTALI/XTALO**). The following circuit design (Figure 10-6) and specifications (Table 10-10) are required to ensure proper operation.

FIGURE 10-6: 25MHZ CRYSTAL CIRCUIT



10.7.1 CRYSTAL SPECIFICATIONS

It is recommended that a crystal utilizing matching parallel load capacitors be used for the crystal input/output signals (**XTALI/XTALO**). Refer to Table 10-10 for the recommended crystal specifications.

TABLE 10-10: CRYSTAL SPECIFICATIONS

Parameter	Symbol	Min	Nom	Max	Units	Notes
Crystal Cut			AT, typ			
Crystal Oscillation Mode			Fundamental Mode			
Crystal Calibration Mode			Parallel Resonant Mode			
Frequency	F_{fund}	-	25.000	-	MHz	
Frequency Tolerance @ 25°C	F_{tol}	-	-	±50	PPM	Note 6
Frequency Stability Over Temp	F_{temp}	-	-	±50	PPM	Note 6
Frequency Deviation Over Time	F_{age}	-	±3 to 5	-	PPM	
Total Allowable PPM Budget		-	-	±100	PPM	Note 7
Shunt Capacitance	C_O	-	7 typ	-	pF	
Load Capacitance	C_L	-	20 typ	-	pF	
Drive Level	P_W	100	-	-	uW	
Equivalent Series Resistance	R_1	-	-	50	Ω	
Operating Temperature Range		Note 7	-	Note 8	°C	
XTALI/CLK_IN Pin Capacitance		-	3 typ	-	pF	Note 9
XTALO Pin Capacitance		-	3 typ	-	pF	Note 9

Note 6: Frequency Deviation Over Time is also referred to as Aging.

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Note 7: 0 °C for commercial version, -40 °C for industrial version.

Note 8: +70 °C for commercial version, +85 °C for industrial version.

Note 9: This number includes the pad, the bond wire and the lead frame. PCB capacitance is not included in this value. The **XTALI/CLK_IN** pin, **XTALO** pin and PCB capacitance values are required to accurately calculate the value of the two external load capacitors. These two external load capacitors determine the accuracy of the 25.000 MHz frequency.

10.7.2 EXTERNAL REFERENCE CLOCK (CLK_IN)

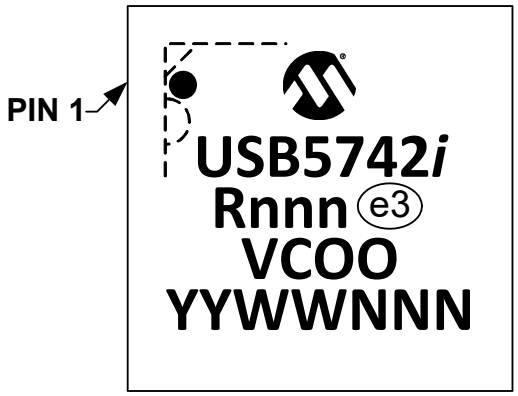
When using an external reference clock, the following input clock specifications are suggested:

- 25 MHz
- 50% duty cycle ±10%, ±100 ppm
- Jitter < 100 ps RMS

11.0 PACKAGE INFORMATION

11.1 Package Marking Information

56-VQFN (7x7 mm)



Legend:	*i*	Temperature range designator (Blank = commercial, *i* = industrial)
	R	Product revision
	nnn	Internal code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	V	Plant of assembly
	COO	Country of origin
	YY	Year code (last two digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

***** Standard device marking consists of Microchip part number, year code, week code and traceability code. For device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

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11.2 Package Drawings

Note: For the most current package drawings, see the Microchip Packaging Specification at: http://www.microchip.com/packaging.

FIGURE 11-1: 56-VQFN PACKAGE (DRAWING)

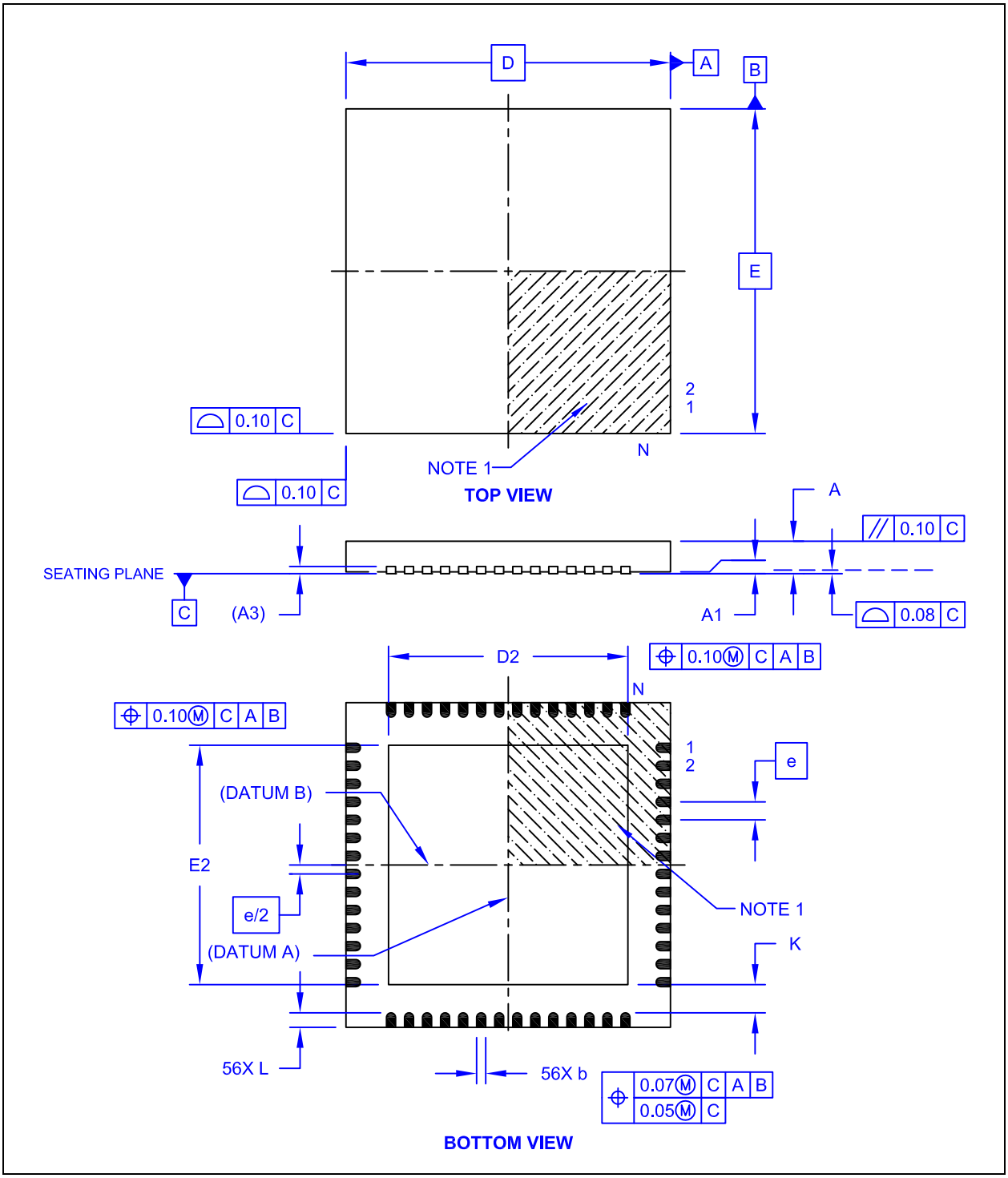
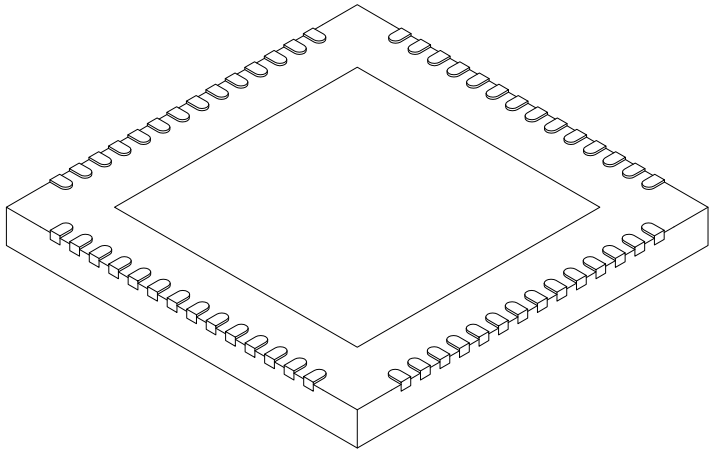


FIGURE 11-2: 56-VQFN PACKAGE (DIMENSIONS)



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		56	
Pitch	e		0.40 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		7.00 BSC	
Exposed Pad Width	E2	4.50	4.60	4.70
Overall Length	D		7.00 BSC	
Exposed Pad Length	D2	4.50	4.60	4.70
Contact Width	b	0.15	0.20	0.25
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.70	0.80	-

Notes:

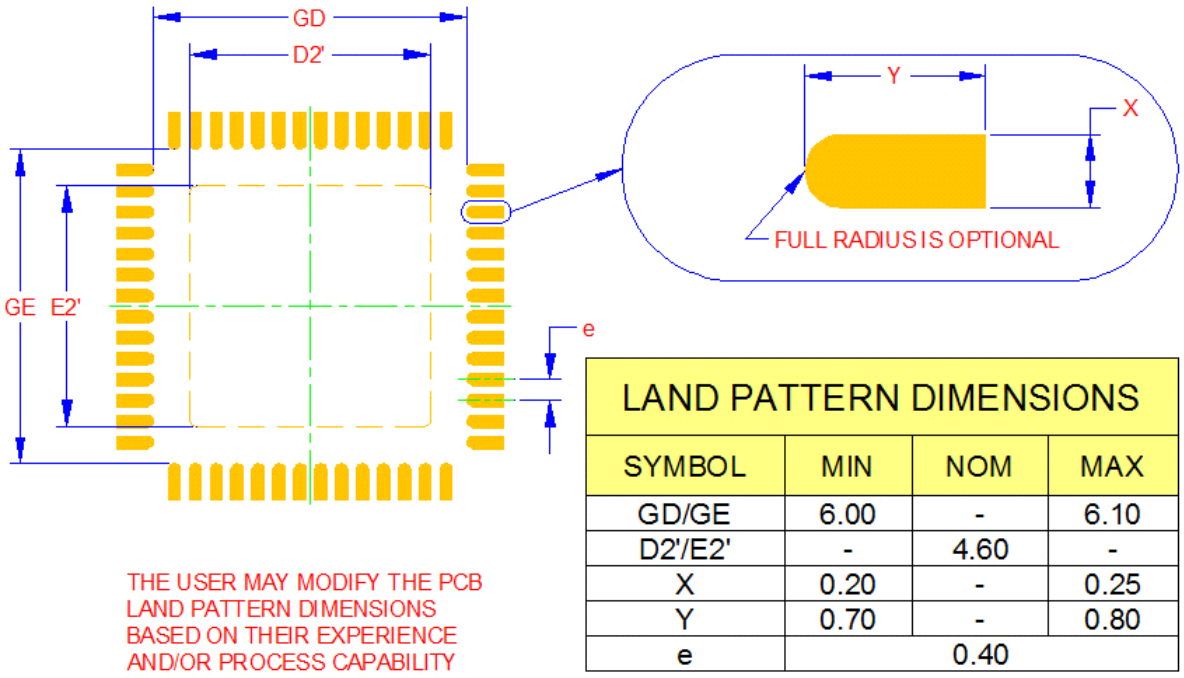
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

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FIGURE 11-3: 56-VQFN LAND PATTERN



LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	6.00	-	6.10
D2'/E2'	-	4.60	-
X	0.20	-	0.25
Y	0.70	-	0.80
e		0.40	

PCB LAND PATTERN

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00002016F (07-21-20)	“USB 3.1” changed to “USB 3.2” throughout document.	
	Table 3-2, "Pin Reset State Legend"	Table added.
	Pin Descriptions on page 10	“Reset State” column added to Pin Assignment table. Notes added to tables explaining what to do with certain pins when unused.
	Section 10.2, "Operating Conditions**"	Supply Voltage Rise Time increased to 5ms.
	Section FIGURE 10-1:, "Supply Rise Time Model"	Note added following diagram.
DS00002016E (11-11-19)	Product Identification System on page 46	Added additional “SEU” ordering code option.
DS00002016D (07-20-18)	FIGURE 10-2: on page 35 and Table 10-5, "Power Supply and RESET_N Sequence Timing"	Rise time modified: “VDD33 to VDD12” changed to “VDD12” to VDD33”.
	Section 9.0, "Compliance Update"	TID number added to first paragraph.
DS00002016C (06-12-18)	Cover	Added new Highlight bullet/sub-bullets regarding USB-IF ECN support: “USB-IF certified (TID 330000076), supporting latest Engineering Change Notices for compliance with USB-IF logo testing for new USB Type-C™ industry initiative”.
	Section 1.2, "Reference Documents"	Updated USB specification reference.
	Section 9.0, "Compliance Update"	Added new Compliance Update section.
	FIGURE 10-2: on page 35 and Table 10-5, "Power Supply and RESET_N Sequence Timing"	Rise time modified: “VDD12 to VDD33” changed to “VDD33” to VDD12”.
DS00002016B (06-06-16)	Section 11.0, Package Information	Added top marking information and land pattern drawing.
	Product Identification System on page 46	Added package with hub feature controller disabled
	Cover, Product Identification System	Added industrial temperature option.
	All	Updated “SQFN” references to “VQFN”. Name change only.
	Section 8.4.2.1, Port Power Control using USB Power Switch	Added additional information on overcurrent detection methods.
	Section 10.6.1, Power Supply and RESET_N Sequence Timing	Added Power Supply and RESET_N Sequence Timing section.
	Section 10.6.5, I2C Timing	“100kHz Standard Mode (Sm)” updated to “400kHz Fast Mode (Fm)”, since the device supports up to 400kHz I^2C operation.
DS00002016A (09-10-15)	All	Initial Release

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PART NO.	[X]	[-X]	/	XX	XXX
Device	Tape & Reel Option	Temperature Range		Package	Special (Optional)

Device:	USB5742	
Tape and Reel Option:	Blank T	= Standard packaging (tray) = Tape and Reel (Note 1)
Temperature Range:	Blank = 0°C to +70°C (Commercial) I = -40°C to +85°C (Industrial)	
Package:	2G = 56-pin VQFN	
Special (optional):	Blank X01 SEU	= Standard Configuration = Hub Feature Controller disabled = Single Event Upset (Low Alpha Emissions Package)

Examples:

a) USB5742/2G
Tray, Commercial temp., 56-pin VQFN

b) USB5742-I/2G
Tray, Industrial temp., 56-pin VQFN

c) USB5742T-I/2G
Tape & reel, Industrial temp., 56-pin VQFN

d) USB5742T/2G
Tape & reel, Commercial temp., 56-pin VQFN

e) USB5742/2GX01
Tray, Commercial temp., 56-pin VQFN
Hub Feature Controller disabled

f) USB5742T-I/2GSEU
Tape & reel, Industrial temp., 56-pin VQFN
Single Event Upset
(Low Alpha Emissions Package)

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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