VIPER28

Peak power high-voltage converter - VIPer Plus

Datasheet - production data

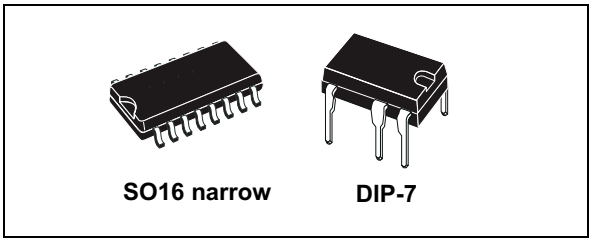
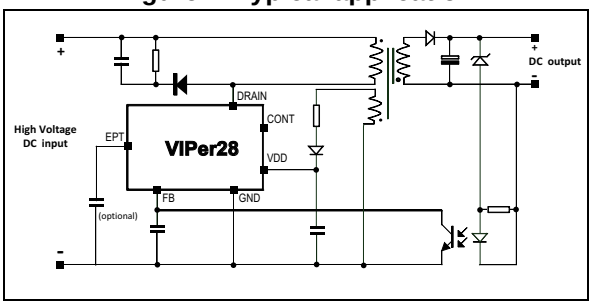


Figure 1. Typical application



Features

- 800 V avalanche-rugged power MOSFET allowing achieving ultra wide-range input V_{ac}
- Embedded HV startup and sense FET
- PWM current-mode controller
- OCP with selectable threshold (I_{Dlim}) and 2nd OCP with higher value (I_{DMAX}) to protect the IC from transformer saturation or short-circuit of the secondary diode
- 30 mW no-load consumption at 230 V_{ac}
- Two operating frequencies:
  - 60 kHz (L type) or 115 kHz (H type)
- Jittered frequency reduces the EMI
- Extra power timer (EPT) blanks the overload current for few seconds
- Output overvoltage protection with tight tolerance and digital noise filter
- Soft-start reduces the stress during startup and increases IC lifetime
- Automatic restart after a fault condition
- Thermal shutdown increases system reliability and IC lifetime

Applications

- Auxiliary power supply for consumer and home equipment
- Power supply for energy meters and data concentrators
- AC-DC adapters

Description

The device is a high-voltage converter that smartly integrates an 800 V rugged power MOSFET with PWM current-mode control.This IC is capable of meeting more stringent energy-saving standards as it has very low consumption and operates in burst mode under light load. The device features an adjustable extra power timer (EPT) that enables the IC to sustain overload conditions for a few seconds. The integrated HV startup, sense FET and oscillator with jitter allow the advantage of using minimal components in the application. The device features high-level protections like dual-level OCP, output overvoltage, short-circuit, and thermal shutdown with hysteresis. After the removal of a fault condition, the IC is automatically restarted.

Table 1. Device summary

Order codes	Package	Packaging
VIPER28LN / VIPER28HN	DIP-7	Tube
VIPER28HD / VIPER28LD	SO16 narrow	
VIPER28HDTR / VIPER28LDTR		Tape and reel

This is information on a product in full production. www.st.com

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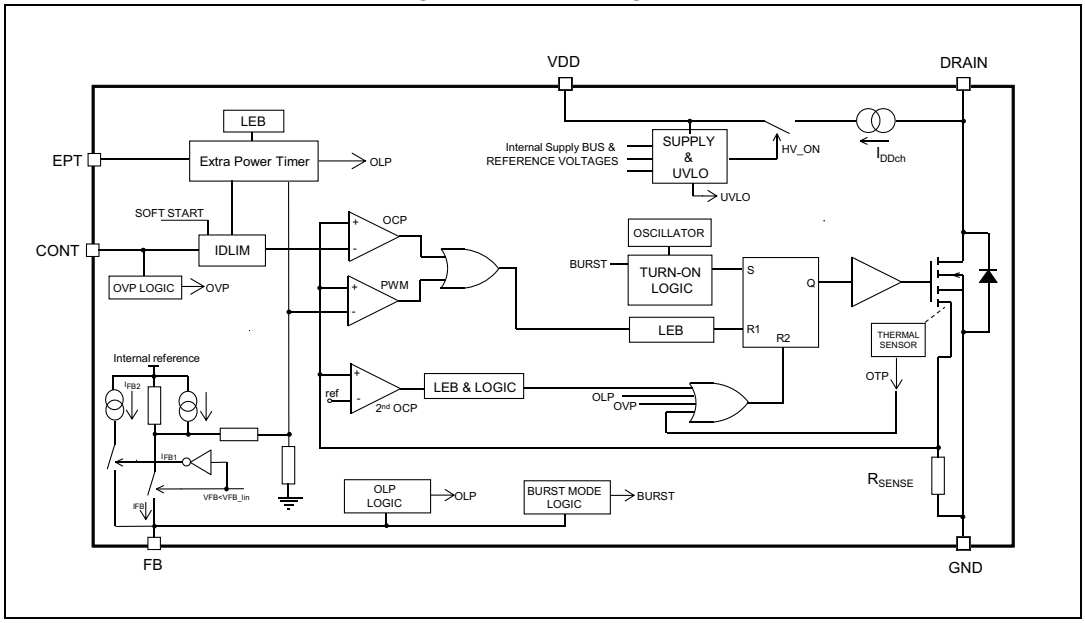
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1 Block diagram

Figure 2. Block diagram



2 Typical power

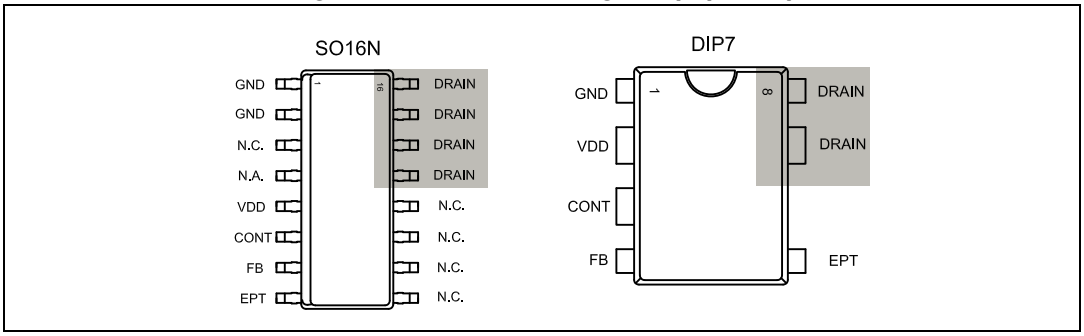
Table 2. Typical power

Nominal power	230 V_{AC}		85-265 V_{AC}	
	Adapter(1)	Open frame(2)	Adapter(1)	Open frame(2)
VIPER28xD/xN	13 W	16 W	10 W	12 W
	22 W (peak)(3)	26 W (peak)(3)	17 W (peak)(3)	20 W (peak)(3)

1. Typical continuous power in non-ventilated enclosed adapter measured at 50 °C ambient.
2. Maximum practical continuous power in an open frame design at 50 °C ambient, with adequate heat sinking.
3. Maximum practical peak power at 50 °C ambient, with adequate heat sinking for 2 sec (max).

3 Pin settings

Figure 3. Connection diagram (top view)



Note: The copper area for heat dissipation has to be designed under the DRAIN pins.

Table 3. Pin description

SO16N	Name	Function
1, 2	GND	This pin represents the device ground and the source of the power section.
3	N.C.	Not connected.
4	N.A.	Not available for user. This pin is mechanically connected to the controller die pad of the frame. In order to improve the noise immunity, is highly recommended connect it to GND (pin 1-2).
5	VDD	Supply voltage of the control section. This pin also provides the charging current of the external capacitor during startup.
6	CONT	Control pin. The following functions can be selected: 1. current limit setpoint adjustment. The default value (set internally) of the cycle-by-cycle current limit can be reduced by connecting an external resistor to ground. 2. output voltage monitoring. A voltage exceeding the V_{OVP} threshold (see *Table 9: Controller section on page 9*) shuts the IC down, reducing device consumption. This function is strobed and digitally filtered for high noise immunity.
7	FB	Control input for duty cycle control. The internal current generator provides bias current for loop regulation. A voltage below the threshold V_{FBbm} activates burst-mode operation. A level close to the threshold V_{FBlin} means that we are approaching the cycle-by-cycle overcurrent setpoint.
8	EPT	This pin allows the connection of an external capacitor for extra power management. If the function is not used, the pin has to be connected to GND.
9...12	N.C.	Not connected.
13...16	DRAIN	High-voltage drain pin. The built-in high-voltage switched startup bias current is drawn from this pin too. These pins are connected to the metal frame to facilitate heat dissipation.

4 Electrical ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min	Max	
V_{DRAIN}	Drain-to-source (ground) voltage		800	V
I_{DRAIN}	Pulse drain current (limited by T_J = 150 °C)		3	A
V_{CONT}	Control input pin voltage	-0.3	6	V
V_{FB}	Feedback voltage	-0.3	5.5	V
V_{EPT}	EPT input pin voltage	-0.3	5	V
V_{DD}	Supply voltage (I_{DD} = 25 mA)	-0.3	Self limited	V
I_{DD}	Input current		25	mA
P_{TOT}	Power dissipation at T_A < 40 °C (DIP-7)		1	W
	Power dissipation at T_A < 60 °C (SO16N)		1.5	
T_J	Operating junction temperature range	-40	150	°C
T_{STG}	Storage temperature	-55	150	°C
$HBM_{(ESD)}$	Human body model		2	kV
$ESD_{(CDM)}$	Charge device mode		1.5	

Table 5. Thermal ratings

Symbol	Parameter	Max value		Unit
		SO16N	DIP7	
R_{thJP}	Thermal resistance junction pin (dissipated power = 1 W)	35	35	°C/W
R_{thJA}	Thermal resistance junction ambient (dissipated power = 1 W)	105	110	°C/W
R_{thJA}	Thermal resistance junction ambient (1) (dissipated power = 1 W)	80	90	°C/W

1. When mounted on a standard single side FR4 board with 100 mm^2 (0.155 sq inch) of Cu (35 µm thick)

Table 6. Avalanche ratings

Symbol	Parameter	Test condition	Value	Unit
I_{AS}	Avalanche current	Repetitive or non repetitive (pulse width limited by T_{Jmax})	1	A
E_{AS}	Single pulse avalanche energy(1)	$I_D = I_{AS}$, V_{DS}=100 V starting T_J = 25°C	3	mJ

1. This parameter is derived from characterization data.

4.1 Electrical characteristics

T_J = -25 to 125 °C, V_{DD}= 14 V; unless otherwise specified (adjust V_{DD} above V_{DDon} startup threshold before setting to 14 V).

Table 7. Power section

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{BVDSS}	Breakdown voltage	I_{DRAIN} = 1 mA, V_{FB} = GND, T_J = 25 °C	800			V
I_{OFF}	OFF-state drain current	V_{DRAIN} = max rating,V_{FB} = GND, T_J = 25°C			60	µA
$R_{DS(on)}$	Drain-source on-state resistance	I_{DRAIN} = 0.4 A, V_{FB} = 3 V, V_{EPT} = GND, T_J = 25 °C			7	Ω
		I_{DRAIN} = 0.4 A, V_{FB} = 3 V, V_{EPT} = GND, T_J = 125 °C			14	Ω
C_{OSS}	Effective (energy related) output capacitance	V_{DRAIN} = 0 to 640 V, T_J = 25°C		40		pF

Table 8. Supply section

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Voltage						
V_{DRAIN_START}	Drain-source start voltage		60	80	100	V
I_{DDch1}	Startup charging current	V_{DRAIN} = 120 V, V_{EPT} = GND, V_{FB} = GND, V_{DD} = 4 V	-2	-3	-4	mA
I_{DDch2}	Restart charging current (after fault)	V_{DRAIN} = 120 V, V_{EPT} = GND, V_{FB} = GND, V_{DD} = 5 V	-0.4	-0.6	-0.8	mA
V_{DD}	Operating voltage range	After turn-on	8.5		23.5	V
$V_{DDclamp}$	V_{DD} clamp voltage	I_{DD} = 20 mA	23.5			V
V_{DDon}	V_{DD} startup threshold	V_{DRAIN} = 120 V, V_{EPT} = GND, V_{FB} = GND	13	14	15	V
V_{DDoff}	V_{DD} undervoltage shutdown threshold		7.5	8	8.5	V
$V_{DD(RESTART)}$	V_{DD} restart voltage threshold	V_{DRAIN} = 120 V, V_{EPT} = GND, V_{FB} = GND	4	4.5	5	V
Current						
I_{DD0}	Operating supply current, not switching	V_{FB} = GND, F_{OSC} = 0 kHz V_{EPT} = GND, V_{DD} = 10 V			0.9	mA
I_{DD1}	Operating supply current, switching	V_{DRAIN} = 120 V, F_{OSC} = 60 kHz			2.5	mA
		V_{DRAIN} = 120 V,F_{OSC} = 115 kHz			3.5	mA
I_{DD_FAULT}	Operating supply current, with protection tripping	V_{DD} = 10 V			400	uA
I_{DD_OFF}	Operating supply current with $V_{DD} < V_{DD_OFF}$	V_{DD} = 7 V			270	uA

Table 9. Controller section

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Feed-back pin						
V_{FBolp}	Overload shutdown threshold		4.5	4.8	5.2	V
V_{FBlin}	Overload detection threshold		3.2	3.5	3.7	V
V_{FBbm}	Burst mode threshold	Voltage falling	0.54	0.6	0.66	V
$V_{FBbmhys}$	Burst mode hysteresis	Voltage rising		100		mV
I_{FB1}	Feedback sourced current	V_{FB} = 0.3 V	-150	-200	-280	uA
I_{FB2}	Feedback current-OLP delay	$V_{FBlin} < V_{FB} < V_{FBolp}$		-3		uA
$R_{FB(DYN)}$	Dynamic resistance	V_{FB} < 3.3 V	14		20	kΩ
H_{FB}	$\Delta V_{FB} / \Delta I_D$	(1) T_J = 25 °C	2		6	V/A
CONT pin						
V_{CONT_l}	Low-level clamp voltage	I_{CONT} = -100 µA	0.4	0.5	0.6	V
V_{CONT_h}	High-level clamp voltage	I_{CONT} = 1 mA	5	5.5	6	V
Current limitation						
I_{Dlim}	Max drain current limitation	V_{FB} = 4 V, I_{CONT} = -10 µA T_J = 25 °C	0.75	0.80	0.85	A
t_{SS}	Soft-start time		7.6	8.5	9.4	ms
T_{ON_MIN}	Minimum turn-on time		220	370	480	ns
td	Propagation delay			100		ns
t_{LEB}	Leading edge blanking	(1)		300		ns
I_{D_BM}	Peak drain current during burst mode	V_{FB} = 0.6 V		160		mA
Oscillator section						
F_{OSC}	V_{FB} = 1 V	VIPER28L	54	60	66	kHz
		VIPER28H	103	115	127	kHz
FD	Modulation depth	VIPER28L		±4		kHz
		VIPER28H		±8		kHz
FM	Modulation frequency		200	250	300	Hz
D_{MAX}	Maximum duty cycle		70		80	%
Overcurrent protection (2nd OCP)						
I_{DMAX}	Second overcurrent threshold	(1)		1.2		A
Overvoltage protection						
V_{OVP}	Overvoltage protection threshold		2.7	3	3.3	V

Table 9. Controller section (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
t_{STROBE}	Overvoltage protection strobe time			2.2		µs
Extra power management						
I_{DLIM_EPT}	Drain current limit with EPT function	(1)		85% I_{Dlim}		A
$V_{EPT(STOP)}$	EPT shutdown threshold	I_{CONT} < -10 µA	3.6	4	4.4	V
$V_{EPT(RESTART)}$	EPT restart threshold		0.4	0.6	0.8	V
I_{EPT}	Sink/source current		4	5	6	µA
Thermal shutdown						
T_{SD}	Thermal shutdown temperature	(1)	150	160		°C
T_{HYST}	Thermal shutdown hysteresis	(1)		30		°C

1. Specification guaranteed by characterization.

Figure 4. Minimum turn-on time test circuit

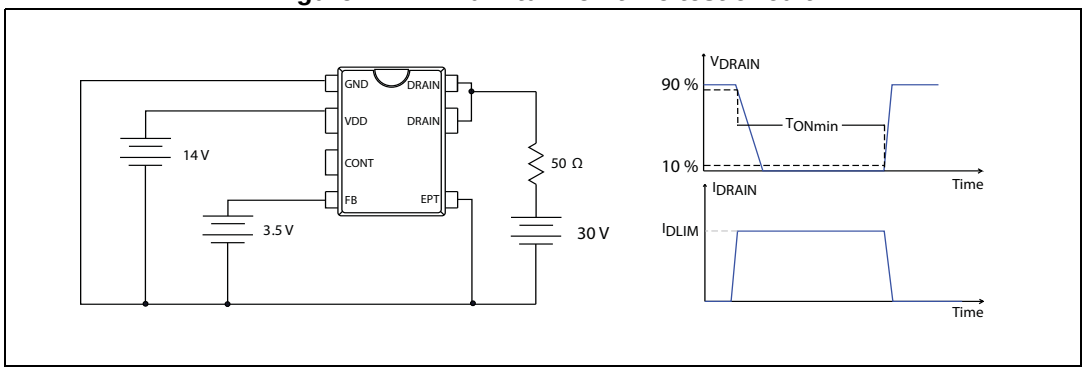
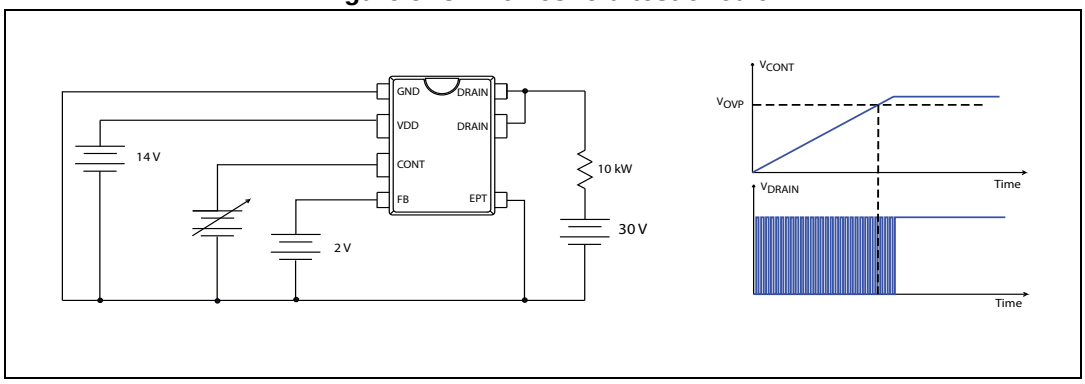


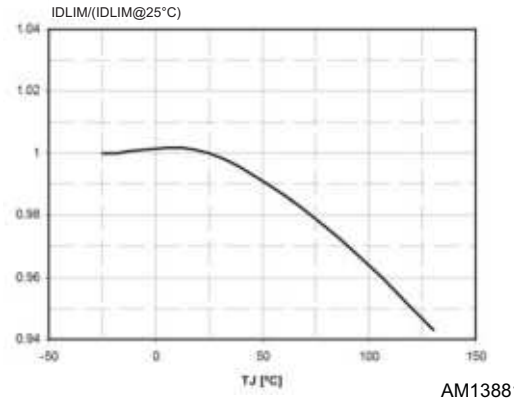
Figure 5. OVP threshold test circuit



Note: Adjust V_{DD} above V_{DDon} startup threshold before setting to 14 V.

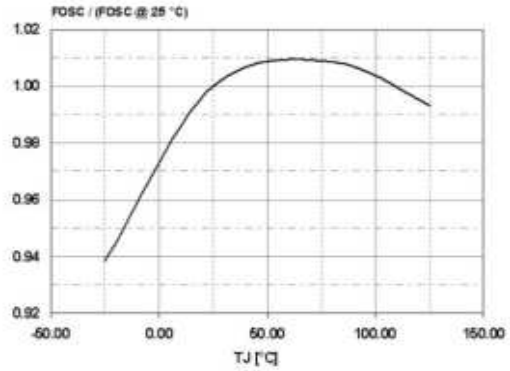
5 Typical electrical characteristics

Figure 6. I_{Dlim} vs. T_J



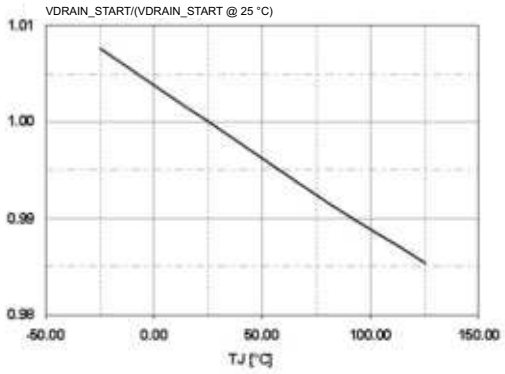
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Figure 7. F_{OSC} vs. T_J



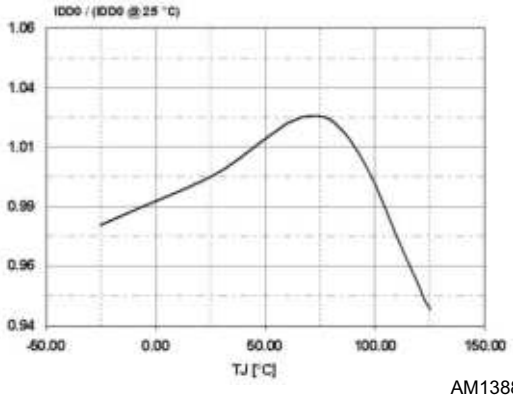
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Figure 8. V_{DRAIN_START} vs. T_J



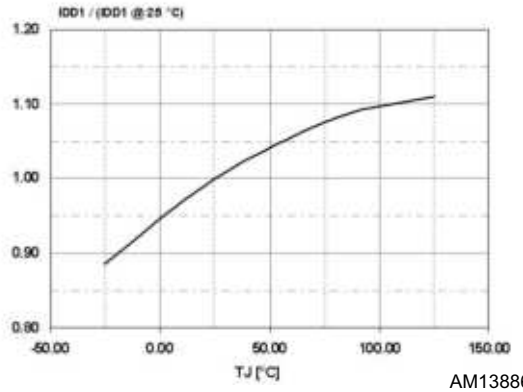
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Figure 9. I_{DD0} vs. T_J



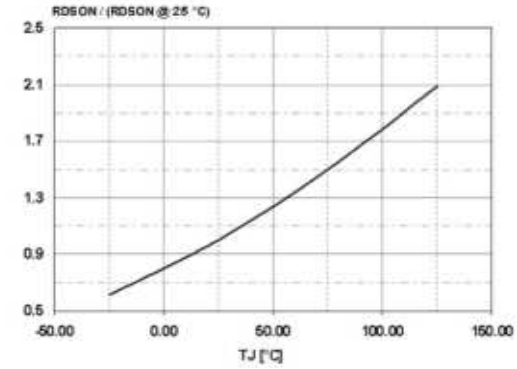
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Figure 10. I_{DD1} vs. T_J



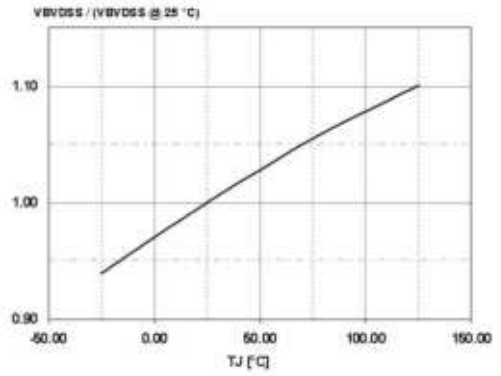
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Figure 11. Main FET R_{DSON} vs. T_J



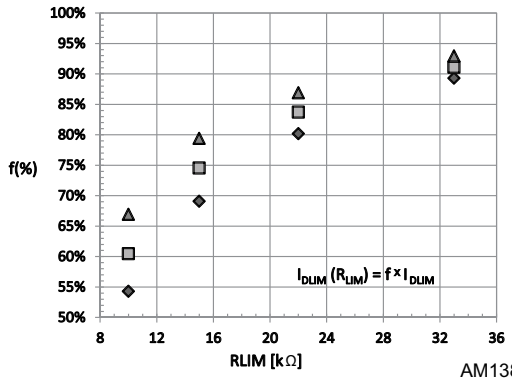
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Figure 12. Main FET V_{BVDSS} vs. T_J



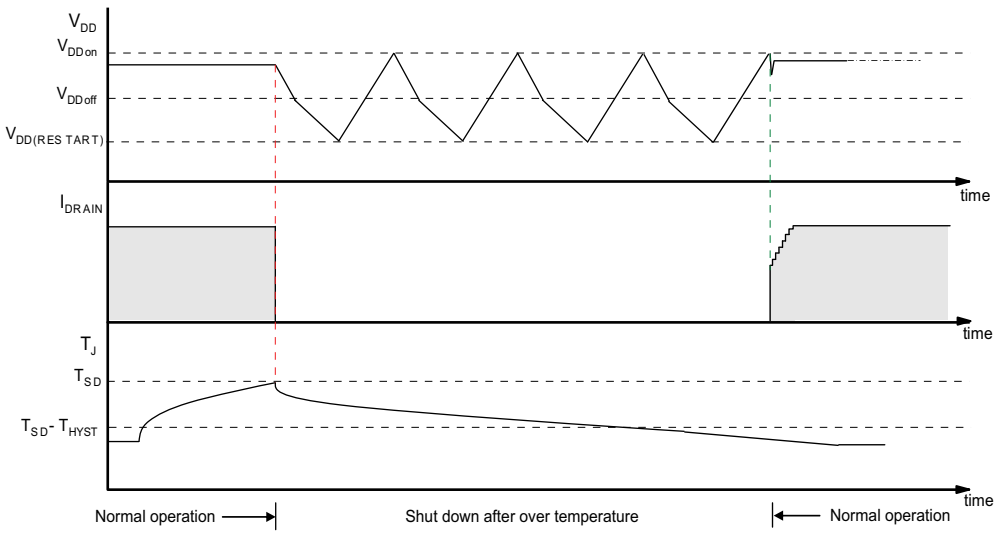
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Figure 13. I_{Dlim} vs. R_{LIM}



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Figure 14. Thermal shutdown



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6 Typical circuit

Figure 15. Basic flyback application

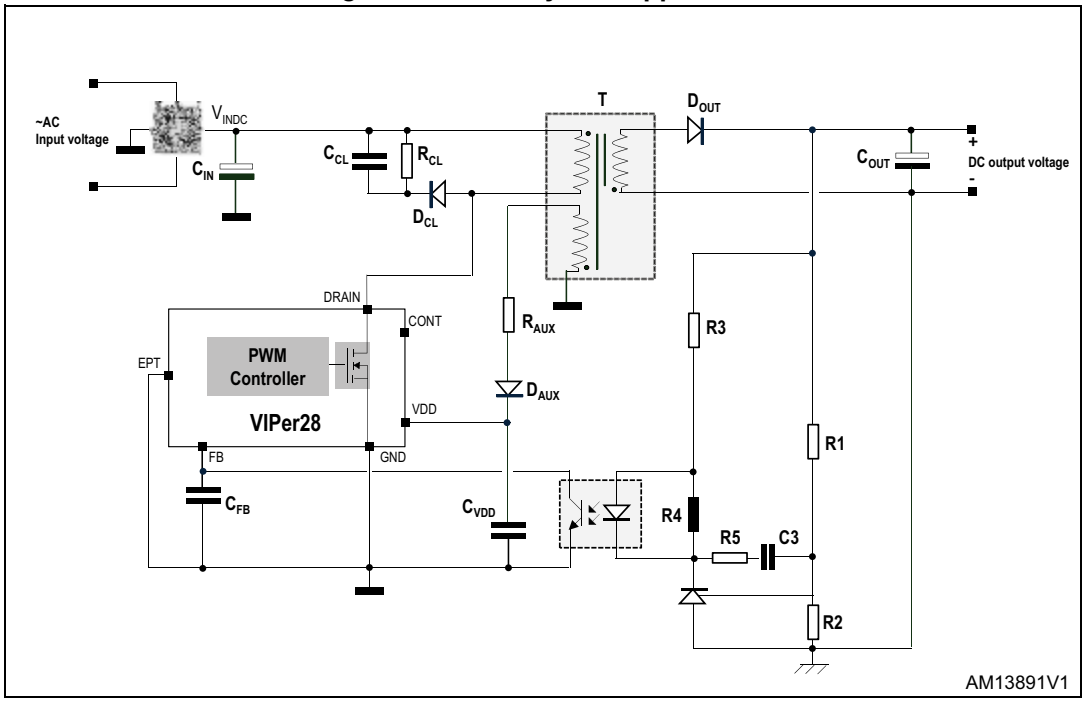
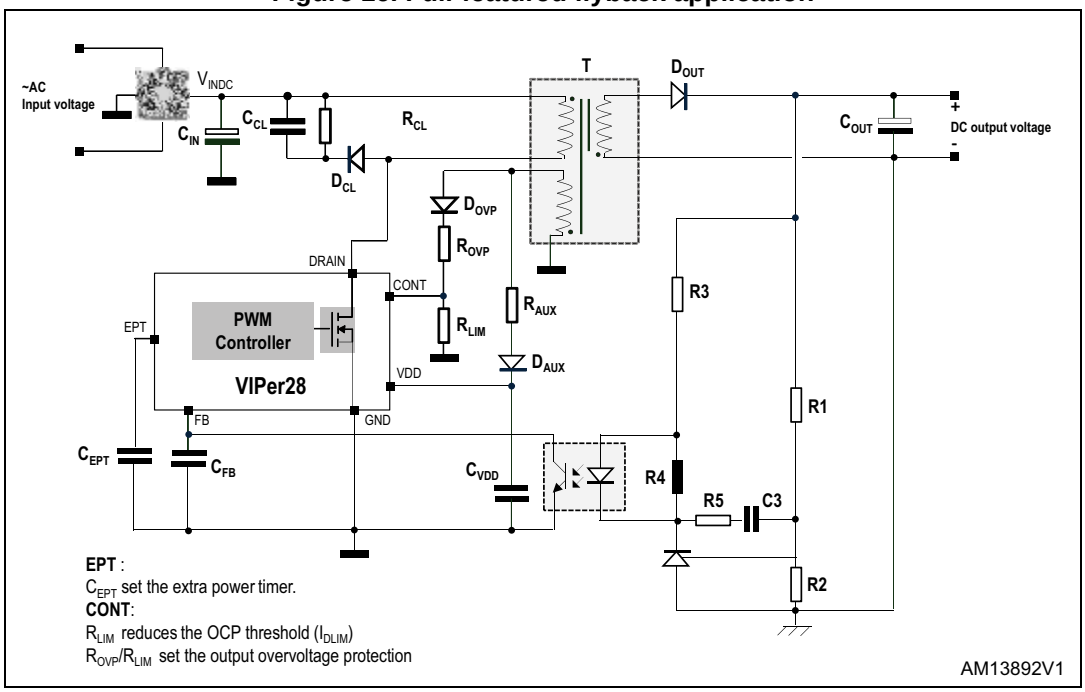


Figure 16. Full-featured flyback application



7 Operation

The device is a high-performance low-voltage PWM controller chip with an 800 V, avalanche rugged power section.

The controller includes the oscillator with jitter, startup circuit with soft-start, PWM logic, current limiting circuit with adjustable setpoint, second overcurrent circuit, burst mode management, Extra Power Timer circuit, UVLO circuit, auto-restart circuit and thermal protection circuit.

The current limit setpoint is set by the CONT pin. Burst mode operation guarantees high performance in standby mode and contributes to meeting energy-saving standards.

All the fault protections are built in auto-restart mode with very low repetition rate to prevent the IC from overheating.

7.1 Power section and gate driver

The power section is implemented with an avalanche-rugged N-channel MOSFET, which guarantees safe operation within the specified energy rating as well as high dv/dt capability. The power section has a B_{VDSS} of 800 V min. and a maximum $R_{DS(on)}$ of 7 Ω at 25 °C.

The integrated SenseFET structure allows a virtually loss-less current sensing.

The gate driver is designed to supply a controlled gate current during both turn-on and turn-off in order to minimize common-mode EMI. Under UVLO conditions an internal pull-down circuit holds the gate low in order to ensure that the power section cannot be turned on accidentally.

7.2 High-voltage startup generator

The HV current generator is supplied through the DRAIN pin and it is enabled only if the input bulk capacitor voltage is higher than the V_{DRAIN_START} threshold, 80 V DC typically. When the HV current generator is ON, the I_{DDch1} current (3 mA typical value) is delivered to the capacitor on the V_{DD} pin. During auto-restart mode after a fault event, the current is reduced to I_{DDch2} (0.6 mA, typ) in order to have a slow duty cycle during the restart phase.

7.3 Power-up and soft startup

When the input voltage rises to the device start threshold, V_{DRAIN_START}, the VDD voltage begins to grow due to the I_{DDch1} current (see *Table 8: Supply section*) coming from the internal high-voltage startup circuit. If the VDD voltage reaches the V_{DDon} threshold, the power MOSFET starts switching and the HV current generator is turned OFF.

The IC is powered by the energy stored in the capacitor on the VDD pin, C_{VDD}, until the self-supply circuit (typically an auxiliary winding of the transformer and a steering diode) develops a voltage high enough to sustain the operation.

The C_{VDD} capacitor must be correctly sized to avoid fast discharge and keep the required voltage higher than the V_{DDoff} threshold. In fact, an insufficient capacitance value could terminate the switching operation before the controller receives any energy from the auxiliary winding.

The following formula can be used for the C_{VDD} capacitor calculation:

Equation 1

$$C_{VDD} = \frac{I_{DDch1} \times t_{SSaux}}{V_{DDon} - V_{DDoff}}$$

The parameter t_{SSaux} is the time needed for the steady state of the auxiliary voltage. This time represents an estimate of the user's application according to the output stage configurations (transformer, output capacitances, etc.).

During the converter startup time, the drain current limitation is progressively increased to the maximum value. In this way the stress on the secondary diode is considerably reduced. It also helps to prevent transformer saturation. The soft-start time lasts 8.5 ms and the feature is implemented for every attempt of the startup converter or after a fault.

Figure 17. I_{DD} current during startup and burst mode

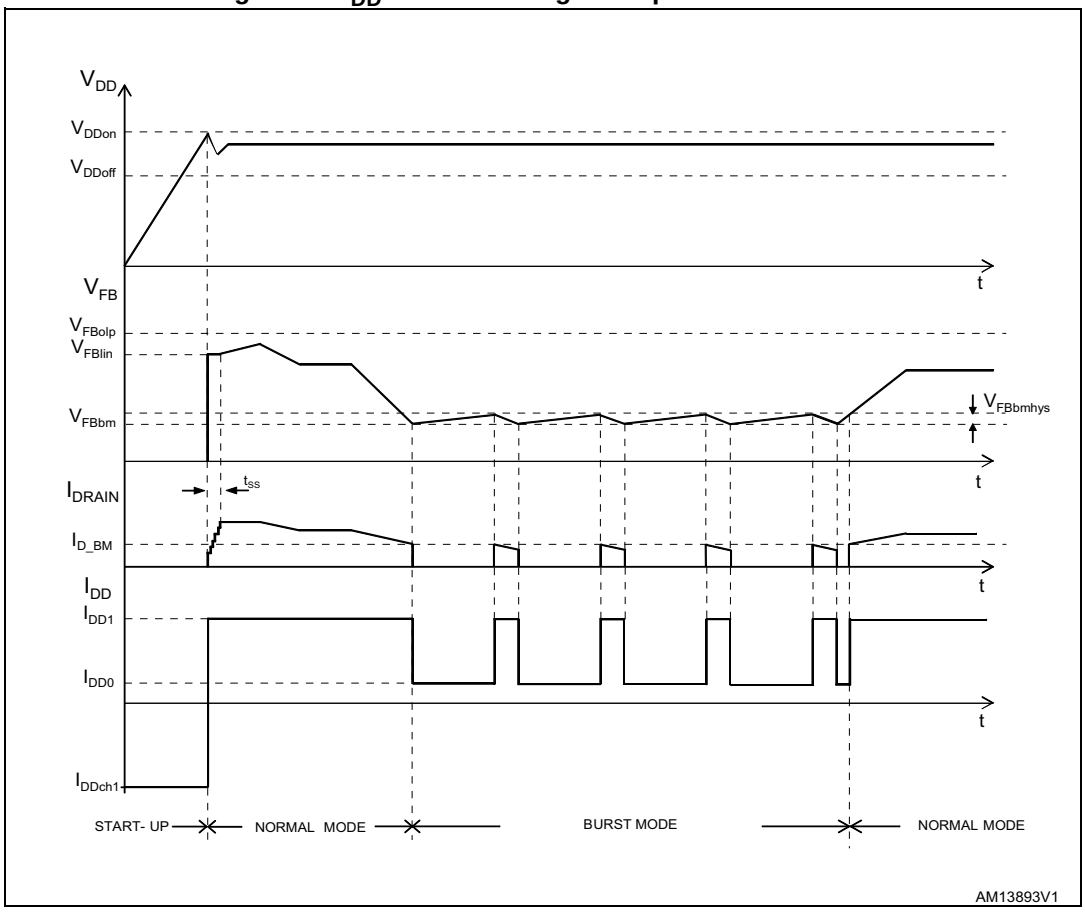


Figure 18. Timing diagram: normal power-up and power-down sequences

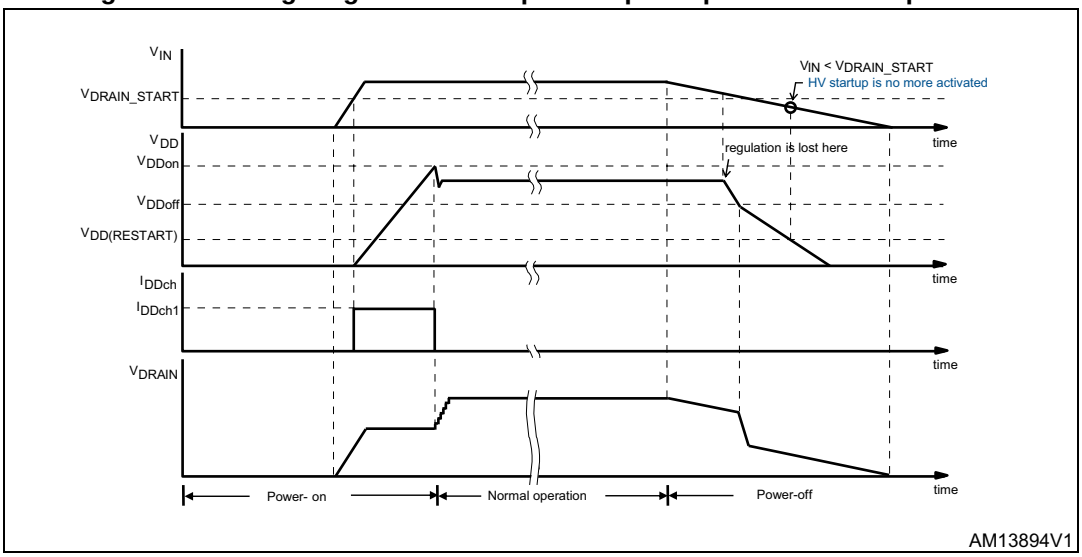
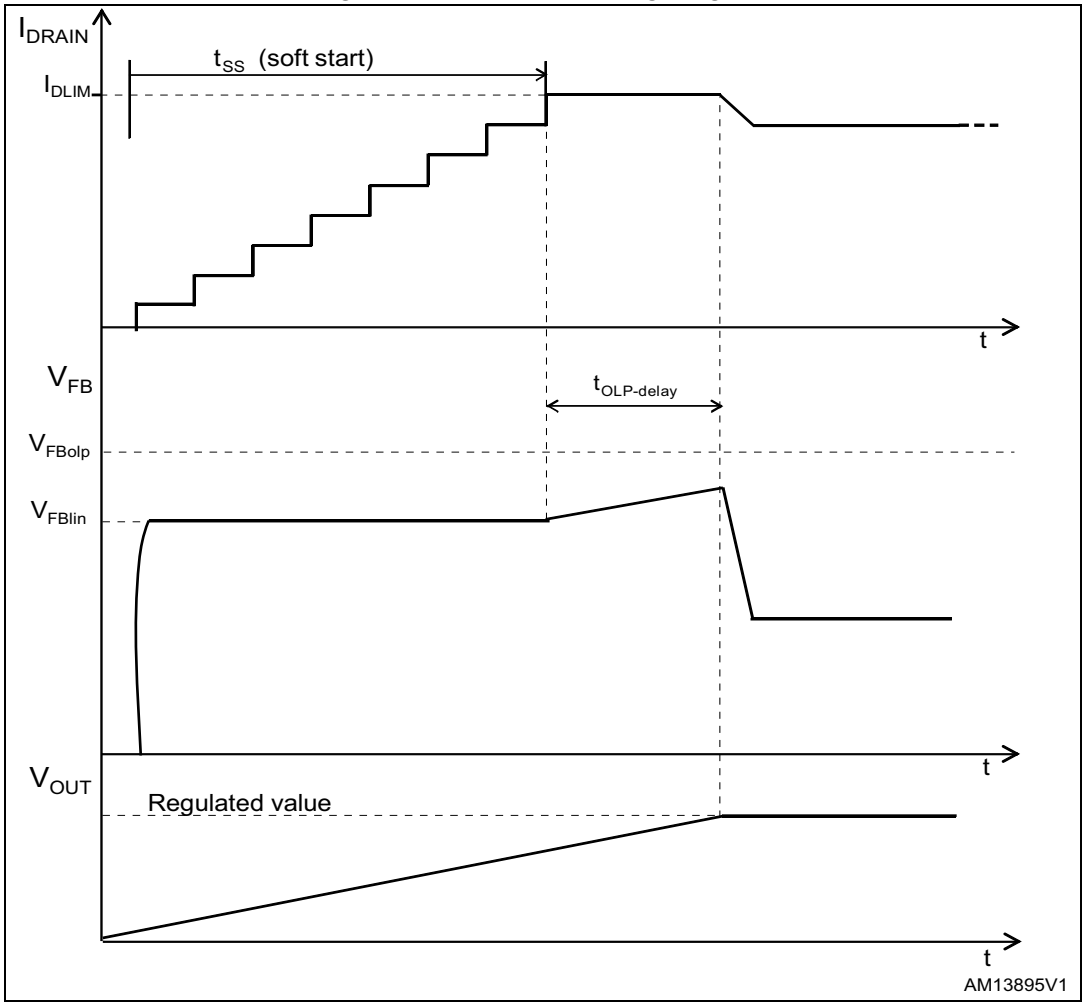


Figure 19. Soft-start: timing diagram



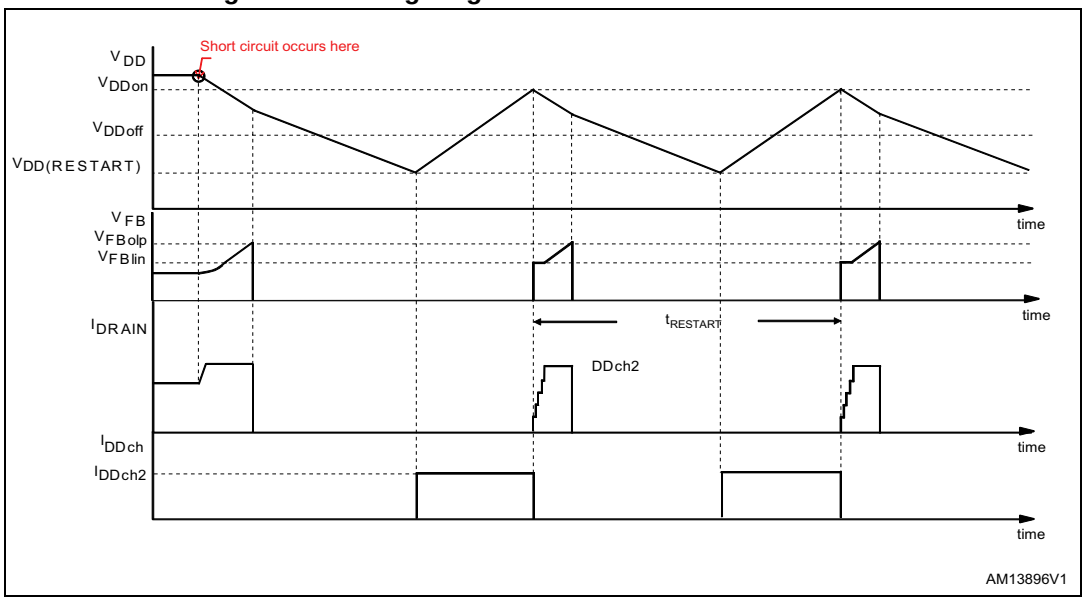
7.4 Power-down

At converter power-down, the system loses its ability to regulate as soon as the decreasing input voltage is low enough for the peak current limitation to be reached. The VDD voltage drops and when it falls below the V_{DDoff} threshold (see *Table 8: Supply section*) the power MOSFET is switched OFF, the energy transfers to the IC is interrupted and, consequently, the VDD voltage decreases (*Table 19: Soft-start: timing diagram*), the startup sequence is inhibited and the power-down is completed. This feature is useful as it prevents the converter from attempting a restart and ensures monotonic output voltage decay during system power-down.

7.5 Auto-restart

Every time a protection is tripped, the IC is automatically restarted after a duration that depends on the discharge and recharge of the C_{VDD} capacitor. As shown in *Figure 20*, after a fault the IC is stopped and, consequently, the V_{DD} voltage decreases because of the IC's consumption. As soon as the V_{DD} voltage falls below the threshold $V_{DD(RESTART)}$ and if the DC input voltage is higher than V_{DRAIN_START} threshold, the internal HV current source is turned ON and it starts to charge the C_{VDD} capacitor with the current I_{DDch2} (0.6 mA, typ). As soon as the V_{DD} voltage reaches the threshold $V_{DD(ON)}$, the IC restarts.

Figure 20. Timing diagram: behavior after short-circuit



7.6 Oscillator

The switching frequency is internally fixed to 60 kHz or 115 kHz. In both cases the switching frequency is modulated by approximately ±4 kHz (60 kHz version) or ±8 kHz (115 kHz version) at 250 Hz (typical) rate, so that the resulting spread-spectrum action distributes the energy of each harmonic of the switching frequency over a number of side-band harmonics having the same energy on the whole, but smaller amplitudes.

7.7 Current mode conversion with adjustable current limit setpoint

The device is a current mode converter. The drain current is sensed and converted to voltage that is applied to the non-inverting pin of the PWM comparator. This voltage is compared with the one on the feedback pin through a voltage divider on a cycle-by-cycle basis.

The device has a default current limit value, I_{Dlim}, that can be adjusted according to the electrical specification, by the R_{LIM} resistor connected to the CONT pin.

The CONT pin has a minimum current sunk needed to activate the I_{Dlim} adjustment. Without R_{LIM} or with high R_{LIM} (i.e. 100 kΩ) the current limit is set to the default value (see I_{Dlim}, *Table 9: Controller section*).

7.8 Overvoltage protection (OVP)

The device has integrated logic for the monitoring of the output voltage using as an input signal the voltage V_{CONT} during the OFF time of the power MOSFET. This is the time when the voltage from the auxiliary winding tracks the output voltage, through the turn ratio.

The CONT pin has to be connected to the auxiliary winding through the diode D_{OVP} and the resistors R_{OVP} and R_{LIM} as shown in *Figure 22: CONT pin configuration*. When, during the OFF time, the voltage V_{CONT} exceeds four consecutive times the reference voltage V_{OVP} (see *Table 9: Controller section*), the overvoltage protection will stop the power MOSFET and the converter enters auto-restart mode.

In order to bypass the noise immediately after the turn-off of the power MOSFET, the voltage V_{CONT} is sampled inside a short window after the time T_{STROBE}, see *Table 9: Controller section* and the *Figure 21: OVP timing diagram*. The sampled signal, if higher than V_{OVP}, triggers the internal OVP digital signal and increments the internal counter. The same counter is reset every time the signal OVP is not triggered in one oscillator cycle.

Referring to *Figure 22: CONT pin configuration*, the resistor divider ratio k_{OVP} will be given by:

Equation 2

$$k_{OVP} = \frac{V_{OVP}}{\frac{N_{AUX}}{N_{SEC}} \cdot (V_{OUTOVP} + V_{DSEC}) - V_{DAUX}}$$

Equation 3

$$k_{OVP} = \frac{R_{LIM}}{R_{LIM} + R_{OVP}}$$

Where:

- V_{OVP} is the OVP threshold (see *Table 9: Controller section*)
- $V_{OUT\ OVP}$ is the converter output voltage value to activate the OVP set by the designer
- N_{AUX} is the number of the auxiliary winding turns
- N_{SEC} is the number of the secondary winding turns
- V_{DSEC} is the secondary diode forward voltage
- V_{DAUX} is the auxiliary diode forward voltage
- R_{OVP} together with R_{LIM} constitute the output voltage divider

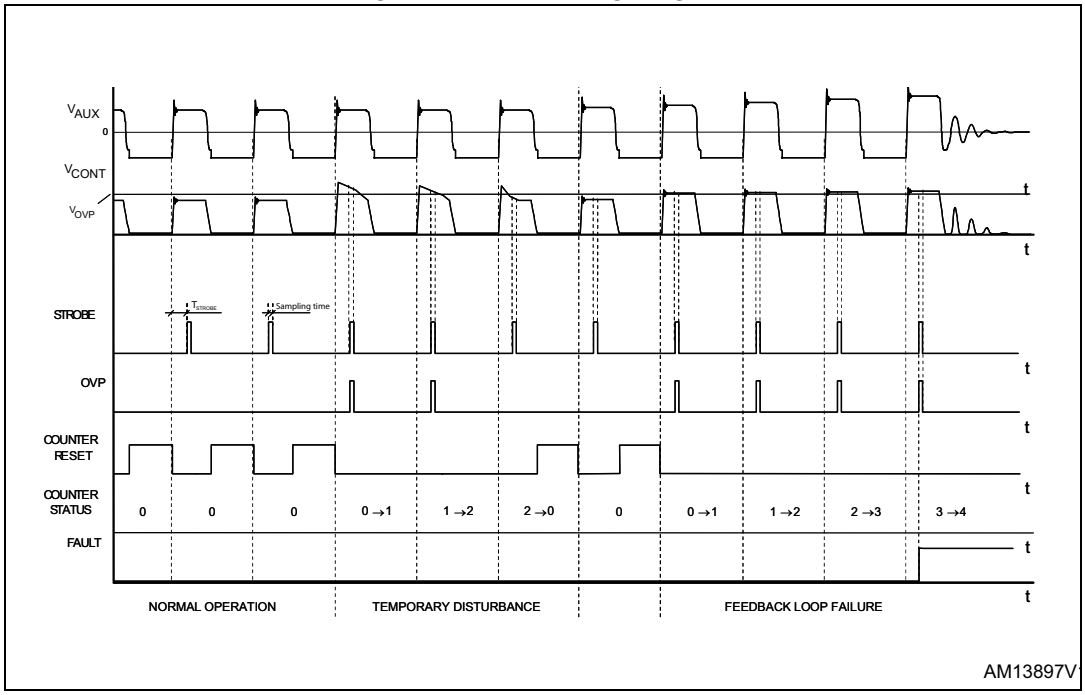
Then, fixing R_{LIM} according to the desired I_{Dlim}, the R_{OVP} can be calculated by:

Equation 4

$$R_{OVP} = R_{LIM} \times \frac{1 - k_{OVP}}{k_{OVP}}$$

The resistor values will be such that the current sourced and sunk by the CONT pin are within the rated capability of the internal clamp.

Figure 21. OVP timing diagram



7.9 About CONT pin

Referring to *Figure 22*, the CONT pin is used to configure the:

1. reduction of the OCP setpoint (I_{Dlim})
2. output overvoltage protection (OVP)

Table 10 lists the external components needed to activate one or more of the CONT pin functions.

Figure 22. CONT pin configuration

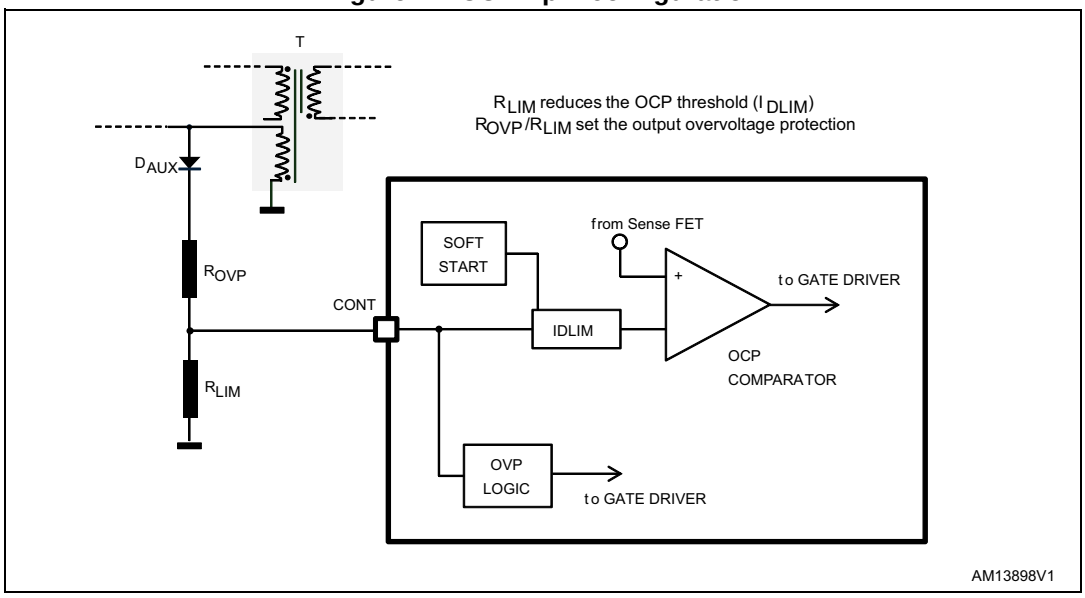


Table 10. CONT pin configurations

Function / component	R_{LIM}	R_{OVP}	D_{AUX}
I_{Dlim} reduction	See *Figure 13*	No	No
OVP	≥ *80 kΩ*	See *Equation 4*	Yes
I_{Dlim} reduction and OVP(1)	See *Figure 13*	See *Equation 4*	Yes

1. Select R_{LIM} then R_{OVP}.

7.10 Feedback and overload protection (OLP)

The device is a current-mode converter. The feedback pin controls PWM operation as well as burst mode and activates the overload protection. *Figure 23: FB pin configuration (option 1)* and *Figure 24: FB pin configuration (option 2)* show the internal current-mode structure.

With the feedback pin voltage between V_{FBbm} and V_{FBlin}, (see *Table 9: Controller section*) the drain current is sensed and converted to voltage that is applied to the non-inverting pin of the PWM comparator.

This voltage is compared to the voltage on the feedback pin through a voltage divider on a cycle-by-cycle basis. When these two voltages are equal, the PWM logic orders the switch-off of the power MOSFET. The drain current is always limited to the value of I_{Dlim}.

When the feedback pin voltage reaches the threshold V_{FBlin}, an internal current generator starts to charge the feedback capacitor (C_{FB}) and when the feedback voltage reaches the V_{FBolp} threshold, the converter is turned off and the automatic restart is activated.

During startup, when the output voltage is still low, if the feedback network is not properly dimensioned, the feedback voltage could rise up to the overload threshold (V_{FBolp}) generating the switching off of the IC itself. Taking into account that the feedback network also fixes the loop stability, two options can be considered for this network.

The time from the overload detection ($V_{FB} = V_{FBlin}$) to the device shutdown ($V_{FB} = V_{FBolp}$) must be set by C_{FB} (or C_{FB1}) using the formula:

Equation 5

$$T_{OLP-delay} = C_{FB} \times \frac{V_{FBolp} - V_{FBlin}}{I_{FB2}}$$

In the option 1 shown in *Figure 23: FB pin configuration (option 1)*, the capacitor C_{FB} has a dual function: guaranteeing the loop compensation and fixing the overload delay time as calculated in *Equation 5*.

Owing to the above considerations, the OLP delay time must be long enough to bypass the initial output voltage transient and check the overload condition only when the output voltage is in steady state. The output transient time depends on the value of the output capacitor and on the load.

When the value of the C_{FB} capacitor calculated for the loop stability is too low and cannot ensure enough OLP delay, an alternative compensation network can be used and it is shown in *Figure 24: FB pin configuration (option 2)*.

Using this alternative compensation network, two poles (f_{PFB}, f_{PFB1}) and one zero (f_{ZFB}) are introduced by the capacitors C_{FB} and C_{FB1} and the resistor R_{FB1}.

The capacitor C_{FB} introduces a pole (f_{PFB}) at higher frequency than f_{ZB} and f_{PFB1}. This pole is usually used to compensate the high-frequency zero due to the ESR (equivalent series resistor) of the output capacitance of the flyback converter.

The mathematical expressions of these poles and zero frequency are:

$$f_{ZFB} = \frac{1}{2 \cdot \pi \cdot C_{FB1} \cdot R_{FB1}}$$

Equation 6

$$f_{PFB} = \frac{R_{FB(DYN)} + R_{FB1}}{2 \cdot \pi \cdot C_{FB} \cdot (R_{FB(DYN)} \cdot R_{FB1})}$$

Equation 7

$$f_{PFB\ 1} = \frac{1}{2 \cdot \pi \cdot C_{FB\ 1} \cdot \left(R_{FB\ 1} + R_{FB\ (DYN\ )}\right)}$$

The $R_{FB(DYN)}$ is the dynamic resistance seen by the FB pin.

The C_{FB1} capacitor fixes the OLP delay and usually C_{FB1} results in a much higher value than C_{FB}. *Equation 5* can be still used to calculate the OLP delay, but C_{FB1} has to be considered instead of C_{FB}. Using the compensation network shown in option 2, in all cases the loop stability can be set as well as a sufficient OLP delay.

Figure 23. FB pin configuration (option 1)

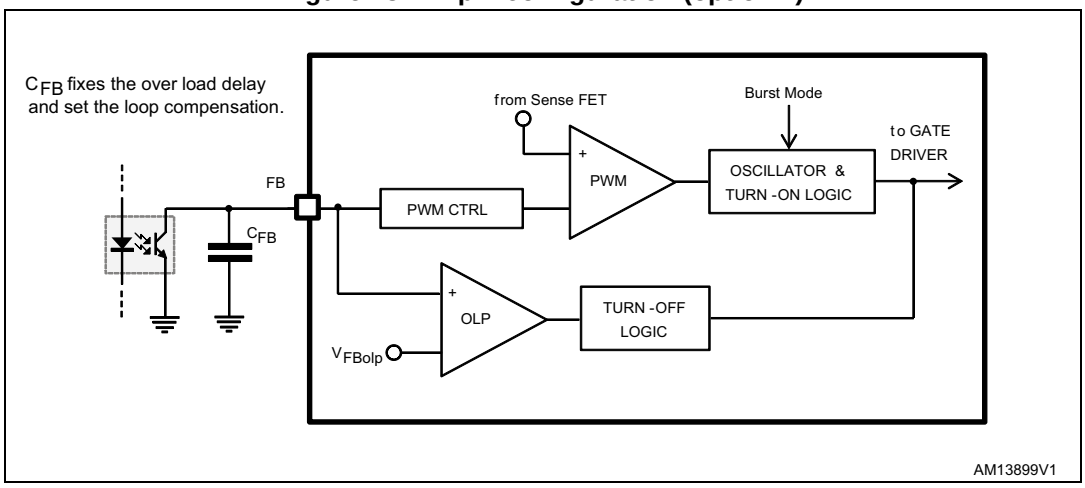
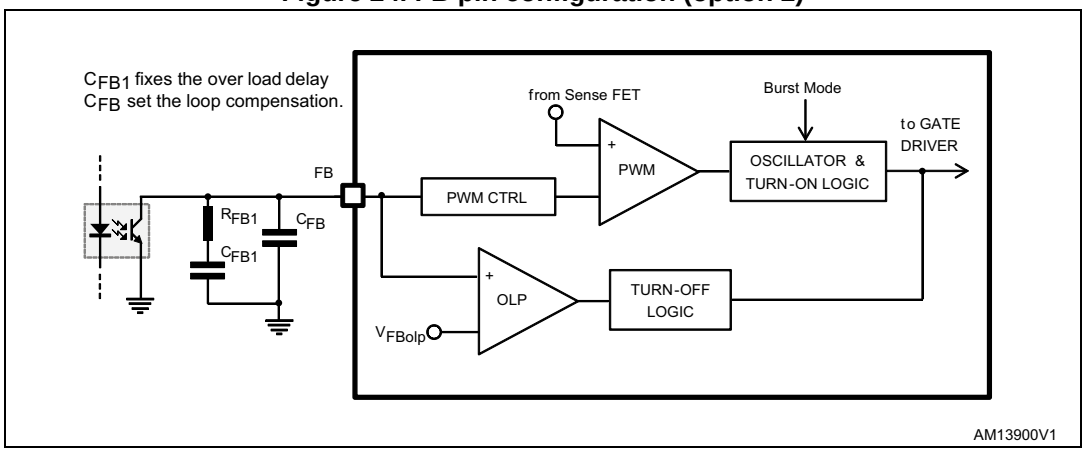


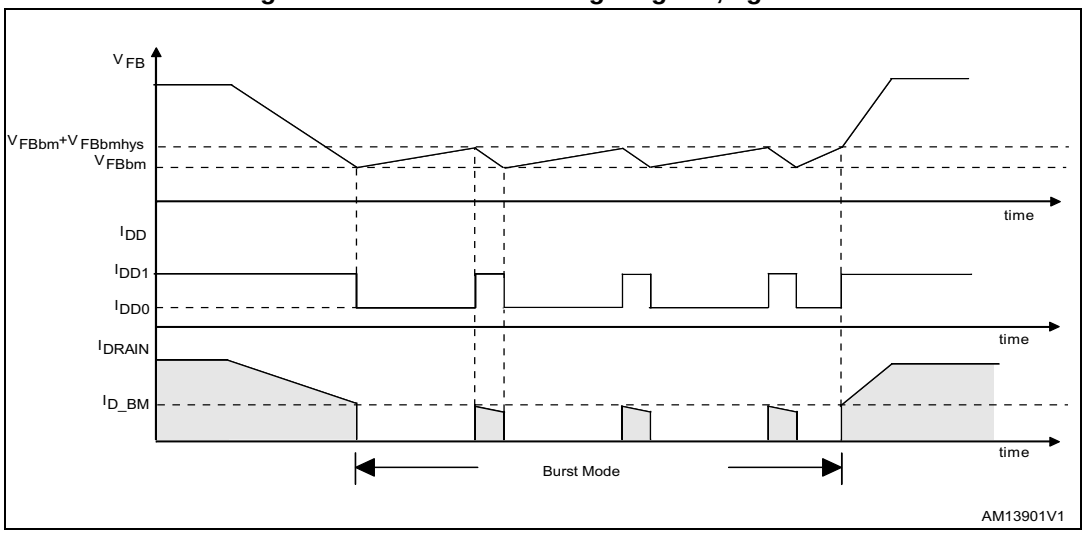
Figure 24. FB pin configuration (option 2)



7.11 Burst-mode operation at no load or very light load

When the load decreases, the feedback loop reacts by lowering the feedback pin voltage. If it falls below the burst mode threshold, V_{FBbm}, the power MOSFET is no longer allowed to be switched on. After the MOSFET stops, the feedback pin voltage increases and when it exceeds the level, $V_{FBbm} + V_{FBbmhys}$, the power MOSFET starts switching again. The burst mode thresholds are provided in *Table 9: Controller section* and *Figure 25: Burst mode timing diagram, light load* shows this behavior. The system alternates between a period of time where the power MOSFET is switching to a period of time where the power MOSFET is not switching. This mode of operation is the burst mode. The advantage of burst mode operation is an average switching frequency much lower than the normal operation frequency, up to several hundred hertz, minimizing all frequency-related losses. In order to prevent audible noise, during burst mode the drain current peak is clamped to the level, I_{D_BM}, given in *Table 9: Controller section*.

Figure 25. Burst mode timing diagram, light load



7.12 Extra power timer (EPT)

The extra power timer feature allows the setting of a blanking time inside which an overload current can be admitted.

The timer is set through a capacitor (C_{EPT}) connected to the EPT pin. Its duration is in the range of a few seconds and is limited by thermal constraints.

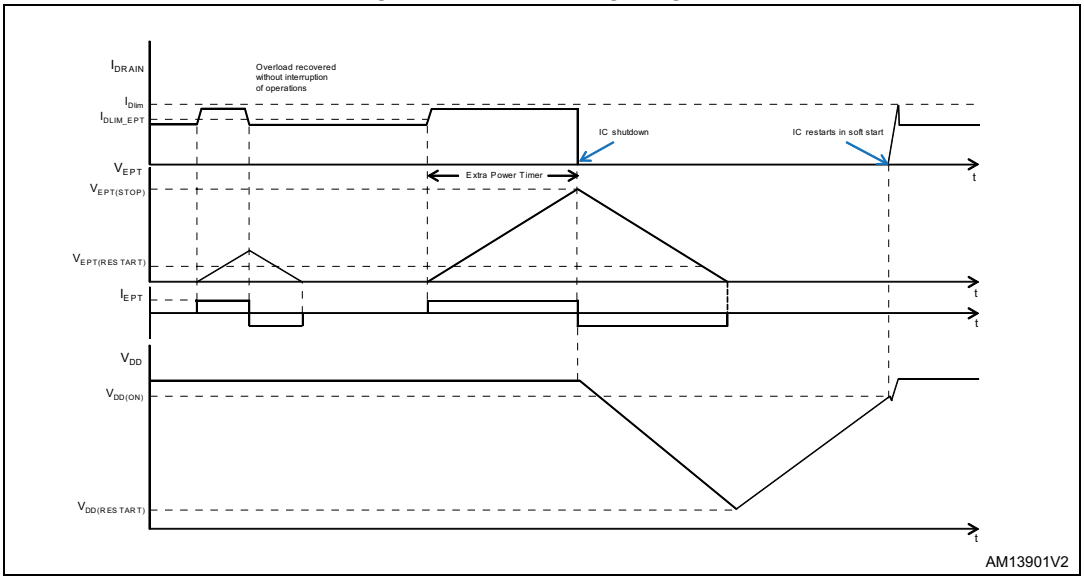
The extra power timer (EPT) is started as soon as the drain current reaches the threshold I_{DLIM_EPT} (typ. 85% of I_{Dlim}) and its duration is defined by the time needed to charge the capacitor C_{EPT} up to the value $V_{EPT(STOP)}$ (4V, typ). The charging current is I_{EPT} (5 uA, typ).

If the EPT starts, the IC sustains the overload and continues to operate normally if the drain current falls below the threshold I_{DLIM_EPT} (85% of I_{Dlim}) before the EPT voltage reaches the value $V_{EPT(STOP)}$. The capacitor C_{EPT} is discharged through the current I_{EPT} (5 uA, typ) and the next EPT is inhibited until the EPT voltage is higher than $V_{EPT(RESTART)}$ (0.6 V, typ).

If the EPT starts and the EPT voltage reaches the value $V_{EPT(STOP)}$, the IC stops and it is automatically restarted. The C_{VDD} capacitor is then discharged down to the value $V_{DD(RESTART)}$ (4.5 V, typ) and is recharged, through the HV current source, up to the value V_{DDon} (14 V, typ). Also in this case the capacitor C_{EPT} is discharged through the I_{EPT} current. See *Figure 26* and *Table 8: Supply section*.

The EPT pin has to be connected to GND if the function is not used.

Figure 26. EPT timing diagram



7.13 2nd level overcurrent protection and hiccup mode

The device is protected against short-circuit of the secondary rectifier, short-circuit on the secondary winding or a hard-saturation of the flyback transformer. This type of anomalous condition is invoked when the drain current exceeds the threshold I_{DMAX}, see *Table 9: Controller section*.

To distinguish a real malfunction from a disturbance (e.g. induced during ESD tests) a “warning state” is entered after the first signal is tripped. If, in the subsequent switching cycles, the signal is not tripped, a temporary disturbance is assumed and the protection logic will be reset in its idle state; otherwise if the I_{DMAX} threshold is exceeded for two consecutive switching cycles, a real malfunction is assumed and the power MOSFET is turned OFF.

The shutdown condition is latched as long as the device is supplied. While it is disabled, no energy is transferred from the auxiliary winding, hence the voltage on the C_{VDD} capacitor decays until the V_{DD} undervoltage threshold (V_{DDoff}), which clears the latch.

The startup HV current generator is still off, until the V_{DD} voltage falls below its restart voltage, $V_{DD(RESTART)}$. After this condition the C_{VDD} capacitor is charged again by the I_{DDch2} current, and the converter switching restarts if V_{DDon} occurs. If the fault condition is not removed, the device enters auto-restart mode. This behavior results in a low-frequency intermittent operation (hiccup-mode operation), with very low stress on the power circuit.

8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

8.1 DIP-7 package information

Figure 27. DIP-7 package outline

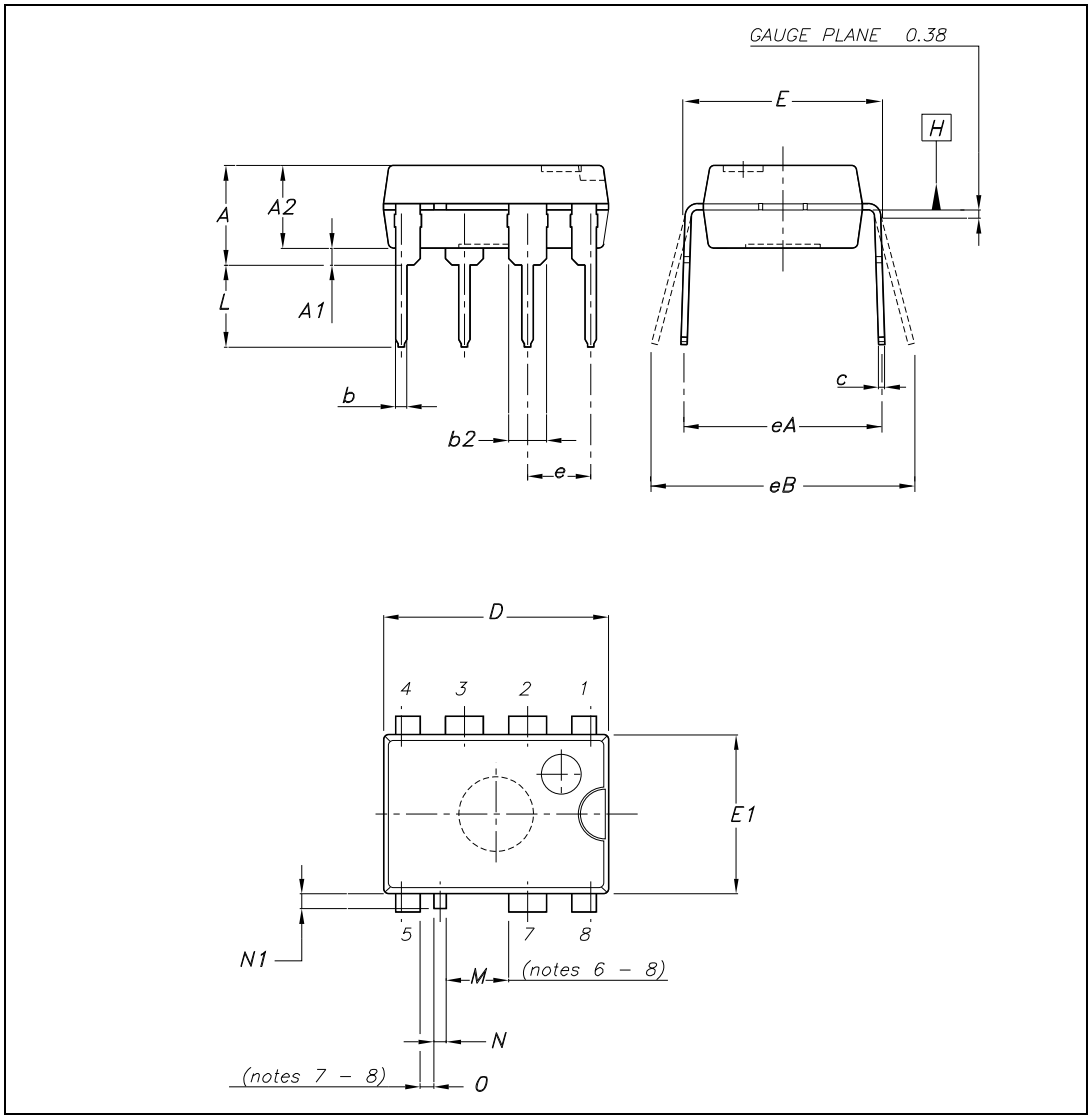


Table 11. DIP-7 mechanical data

Dim.	mm		
	Typ	Min	Max
A			5,33
A1		0,38	
A2	3,30	2,92	4,95
b	0,46	0,36	0,56
b2	1,52	1,14	1,78
c	0,25	0,20	0,36
D	9,27	9,02	10,16
E	7,87	7,62	8,26
E1	6,35	6,10	7,11
e	2,54		
eA	7,62		
eB			10,92
L	3,30	2,92	3,81
M (6)(8)	2,508		
N	0,50	0,40	0,60
N1			0,60
O (7)(8)	0,548		

8.2 SO16 narrow package information

Figure 28. SO16 narrow package outline

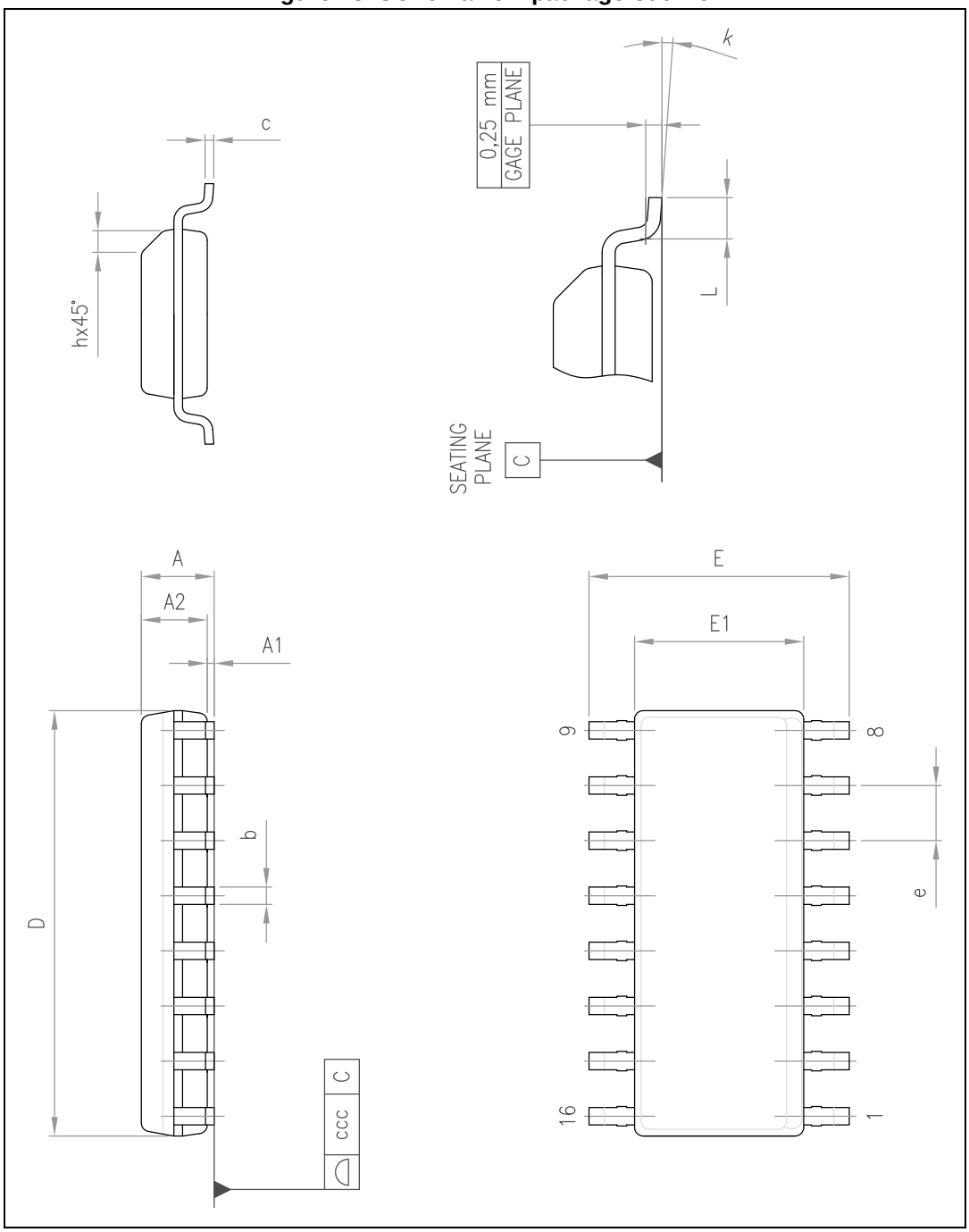


Table 12. SO16 narrow mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.1		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	9.8	9.9	10
E	5.8	6	6.2
E1	3.8	3.9	4
e		1.27	
h	0.25		0.5
L	0.4		1.27
k	0		8
ccc			0.1

9 Revision history

Table 13. Document revision history

Date	Revision	Changes
30-Sep-2008	1	Initial release
22-Jan-2009	2	Updated *Figure 3 on page 4*
21-Oct-2009	3	Added SO16N and SDIP10 packages
31-Aug-2010	4	Updated *Figure 3*, *Figure 4*, *Figure 5 on page 10* and *Table 3 on page 6*
08-Jan-2013	5	Minor text changes to improve readability in *Chapter 7.3*, *Chapter 7.4*, *Chapter 7.5*, *Chapter 7.7*, *Chapter 7.8*, *Chapter 7.9*, *Chapter 7.10*, *Chapter 7.11*, *Chapter 7.13*, in *Table 8 on page 8*, *Table 9 on page 9* and in *Figure 21 on page 19*
16-Dec-2014	6	Updated title in cover page. Removed SDIP10 package. Content reworked to improve readability.

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