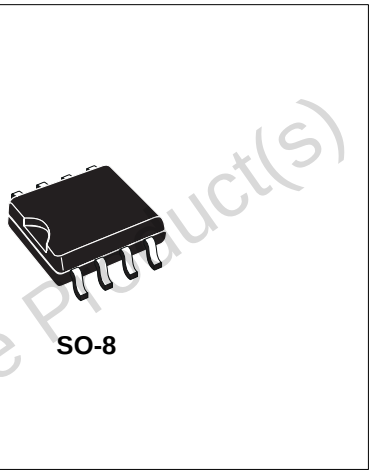
VK05CFL

ELECTRONIC DRIVER FOR CFL APPLICATION

TYPE	B_V	I_{Crms}	I_{Peak}
VK05CFL	520 V	0.25A	1.5A

- EMITTER SWITCH POWER OUTPUT STAGE
- INTEGRATED ANTIPARALLEL COLLECTOR SOURCE DIODE
- INTEGRATED DIAC FUNCTION
- NOMINAL WORKING FREQUENCY SETTABLE BY EXTERNAL CAPACITOR
- IGNITION FREQUENCY SET BY LOAD

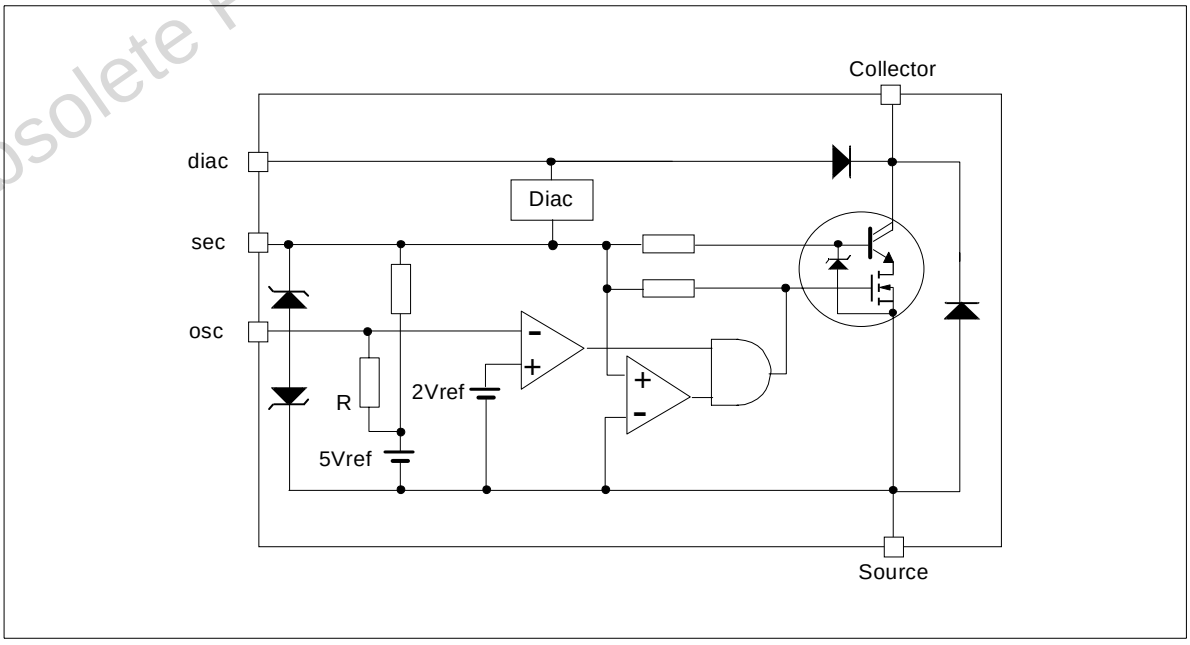


Obsolete Product(s) - Obsolete Product(s)

DESCRIPTION

The VK05CFL is a monolithic device housed in a standard SO-8 package, made by using STMicroelectronics proprietary VIPower M3 Technology. This device is intended both for the low side and the high side driver in half bridge CFL applications. This means that it is possible to realize a complete H-bridge by using two VK05CFL devices: one connected in HSD configuration and the other connected in LSD configuration. In the VK05CFL used in HSD configuration, the diac pin must be connected to source pin. Both diac functionality and discharge circuit for external diac capacitor are integrated. By an external capacitor it is possible to choose the nominal working frequency without influence on the ignition one.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

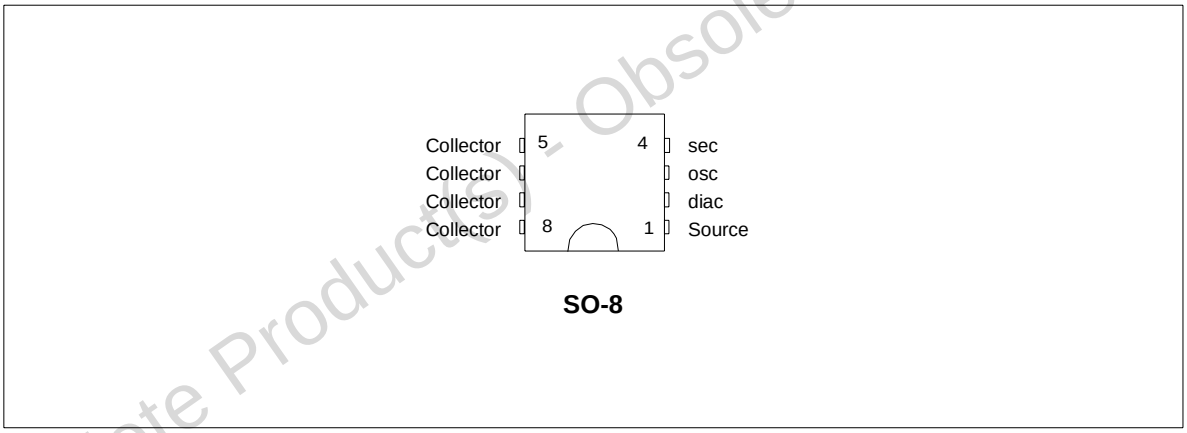
Symbol	Parameter	Min	Typ	Max	Unit
V_{CS}	Collector-Source Voltage			520	V
I_{sec}	Input Current (secondary)	-100		140	mA
V_{sec}	Input Voltage (secondary)	Internally limited			V
I_{CM}	Collector Peak Current	-1.8		1.8	A
I_{OSC}	Osc Pin Current			100	mA
V_{OSC}	Osc Pin Voltage	Internally limited			V
T_j	Max Operating Junction Temperature	-40		150	°C
T_{stg}	Storage Temperature Range	-55		150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{thj\text{-}lead}$	Thermal Resistance Junction - lead	Max	15	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction - ambient	Max	52 (*)	°C/W

(*) When mounted on a standard single-sided FR-4 board with 100mm^2 of Cu (at least 35µm thick).

CONNECTION DIAGRAM



SO-8

PIN FUNCTIONS

Pin Name	Pin Function
Collector	Collector of the NPN high voltage transistor in the cascode configuration.
Source	Low voltage Power MOSFET source in the cascode configuration and GROUND reference.
diac	Input of the diac block to start the system up at the beginning.
sec	Connection with secondary winding of the voltage transformer, in order to trigger and to supply the device.
osc	Output via to charge external capacitor necessary to set the steady state working frequency.

Obsolete Product(s) - Obsolete Product(s)

ELECTRICAL CHARACTERISTICS (T_{case}=25°C unless otherwise specified)

FORWARD

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{CS(sat)}$	Collector-Source Saturation Voltage	V_{sec}=10V; I_C=300mA		1.4	2.8	V

REVERSE

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CSr}	Collector-Source Reverse Voltage	I_C= -300mA		-1	-1.5	V

OSC

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{OSC}	Osc Output Current	V_{sec}=10V; V_{OSC}=0V	240	300	360	µA
$V_{OSC(th)}$	Osc Turn-off Voltage	V_{sec}=10V		1.6	2	V

DIAC

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{diac(thH)}$	Diac On Threshold		28	31	35	V
$V_{diac(thL)}$	Diac Off Threshold		18			V

SEC

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{sec(clH)}$	Sec Clamp High	I_{sec}=20mA; V_{OSC}=0V		22		V
$V_{sec(clL)}$	Sec Clamp Low	I_{sec}= -10mA		25		V
$V_{sec(on)}$	Sec Turn-on Voltage	I_C=10mA; V_{OSC}=0V	3.5	4.5	5.5	V
$I_{sec(on)}$	Sec On Current	V_{sec}=10V; V_{OSC}=0V; I_C=300mA		4		mA

Obsolete Product(s) - Obsolete Product(s)

APPLICATION DESCRIPTION

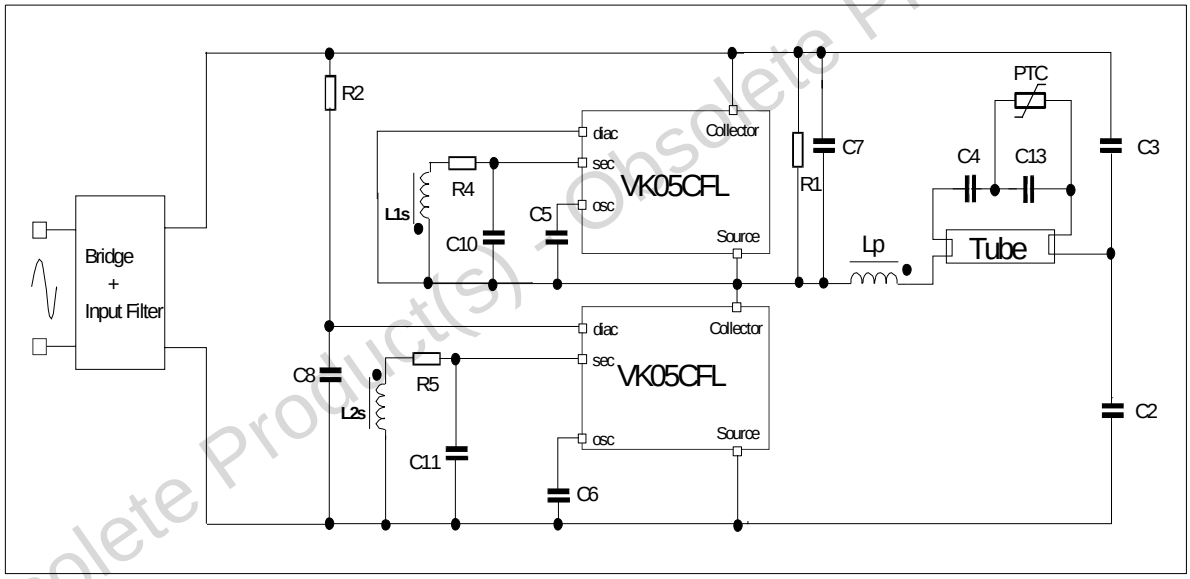
Technology Overview

The VK05CFL is made by using STMicroelectronics proprietary VIPower M3-3 technology. This technology allows the integration in the same chip both of the control part and the power stage. The power stage is the “Emitter Switching”. It is made by putting in cascode configuration a bipolar high voltage darlington with a low voltage MOSFET. This configuration provides a good trade-off between the bipolars low ON drop with high breakdown voltage in OFF state, and the MOSFETS high switching speed. The maximum theoretical working frequency is in the range of 300KHz.

Circuit description

The electrical scheme of the VK05CFL used as a self-oscillating converter to drive fluorescent tubes is shown in Fig. 1.

Figure 1: Application schematic



Obsolete Product(s) - Obsolete Product(s)

This topology does not require the saturable transformer to set the working frequency. Two secondary windings are wound on the main ballast choke Lp. These windings have two functions:1) to trigger the ON state and 2) to provide the power supply to the device. A good trade-off for the ratio between the primary winding Lp and the two secondary windings is 10:1; in order to minimize the power dissipated on the resistors R4 - R5 and to guarantee sufficient voltage to supply the device.

The steady-state working frequency is set by the two capacitor C5 and C6. They are charged by a current I_{cap}≈300µA. When the voltage on the capacitor reaches an internal fixed value the power stage is turned OFF. By choosing the same value for C5 and C6 the circuit will work with a duty-cycle of 50%. During the start-up, as the resonance frequency is higher than the steady-state frequency, the secondary voltage falls lower than the device sustain voltage before the capacitor C5-6 is charged, switching OFF the device. For this reason the circuit can work at different frequencies during the start-up and steady-state phases. The resistor R2 and the capacitor C8 are needed to bias the internal diac in the low side device in order to start-up the system. In the high side device the diac pin must be connected to the midpoint. R1 is the pull-up resistor and C7 is the snubber capacitor.

Input filtering is realized by R4-C10 and R5-C11. It is necessary to have a proper supply voltage on the input pin.

Functional description

When the circuit is supplied, the capacitor C8 is charged by the resistor R2 till the voltage across it reaches the internal diac threshold value (~ 30V). The low side switch is turned ON and consequently current will flow from the HV rail to ground through the path formed by C3//C2, C4 and Lp (in case that the pre-heating network is not present: PTC and C13 are not connected). The voltage drop on Lp is "transferred" to the two secondary windings (wound in opposition) in order to confirm the ON state for the low side device and the OFF state for the high side device. As soon as the low side device switches ON, the capacitor C8 is discharged to ground by an internal HV diode to avoid diac restart.

In this preliminary phase the tube is OFF and the circuit will oscillate at the Lp-C4 series with (C3//C2) resonance frequency

$$f_{st-up} = \frac{1}{2\pi\sqrt{L_c \cdot C_4}}$$ we can neglect C3//C2

As this frequency is higher than the steady-state one, the two devices will switch ON-OFF at this frequency, as the voltage on the two secondary windings falls below the voltage needed to keep the device on.

As soon as the tube is ignited the resonance frequency is reduced ≈(Lp-C3//C2) and the circuit will work at the steady-state frequency fixed by the two capacitors C5 and C6.

It is possible to calculate the steady-state frequency by these formulae:

$$T_{on} = R \cdot C \cdot \ln\frac{5}{2}$$ (R = internal impedance)

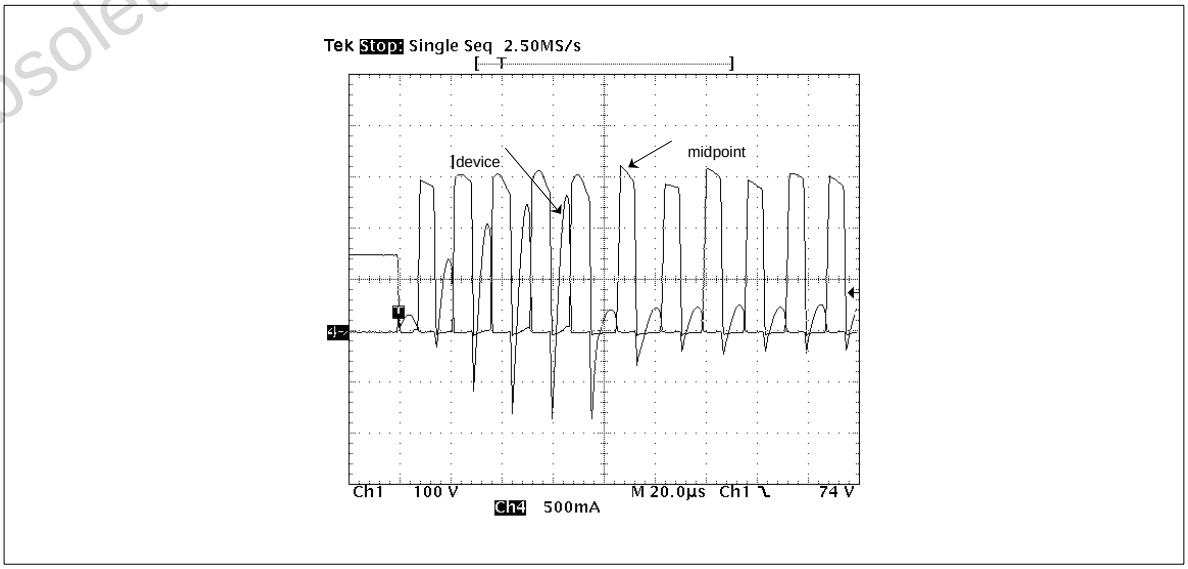
$$\frac{1}{2}T = T_{on} + t_{storage} + t_{(dv)/(dt)}$$

$$f = \frac{1}{T}$$

Considering the VK05CFL board: R=12KΩ; C5=C6=1.2nF; $t_{storage}$≈400nsec; C7=680pF⇒$t_{(dv)/(dt)}$≈800nsec; the working frequency will be: f≈35KHz.

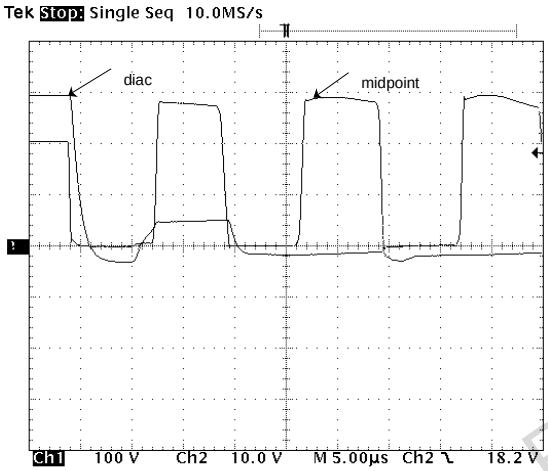
In figure 2 and figure 3, the start-up phase without preheating is reported, while in figure 4 the main waveforms in steady-state are shown.

Figure 2: Start-up phase



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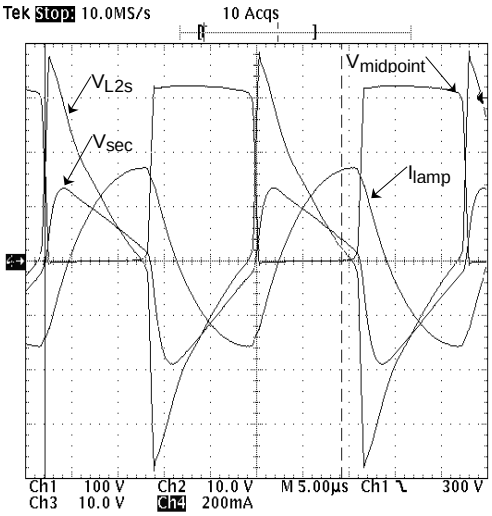
Figure 3: Start-up phase



From figure 4 it can be observed that the value of secondary voltage decreases when the lamp current increases. This happens because increasing the value of the current flowing through the tube, increase the drop on it, consequently decreasing the voltage on the ballast inductor Lp and thereby decreasing also the secondary voltage.

By inserting the filters (R4-C10; R5-C11) between the two secondary windings and the devices, it is possible to guarantee a higher voltage on the input pin of the devices for longer time compared to the secondary signal. In this way it is possible to extend the use of the VK05CFL to all the power range eg.5W – 23W.

Figure 4: Steady state waveforms



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Secondary Filter Design

The design of RC network applied on the sec pin of both devices has to be done taking into account the following considerations:

1) The sec filtered voltage must reach the device ON threshold at the end of the negative dV/dt and before the end of the freewheeling diode conduction in order to avoid hard switching or switching ON delay.

2) The filtered voltage must be high enough (greater than 5V) at the end of T_{on} in order to guarantee the device supply voltage.

A good choice for time constant (τ=RC) is in the range:1.5 µs ÷ 3.3 µs.

The resistor value has chosen in relation to the power dissipated on it during the start-up phase, the worst condition is verified when the preheating is used.

Tube pre-heating

By using the VK05CFL, the tube pre-heating can be done with the classical solution with PTC (see application schematic in figure 1) or with a more reliable low voltage network (see figure 5b). The pre-heating low voltage network allows to obtain an optimum pre-heating avoiding the overstress on the PTC thus improving the ballast reliability and the lamp life-time.

Figure 5a: Pre-heating phase with PTC

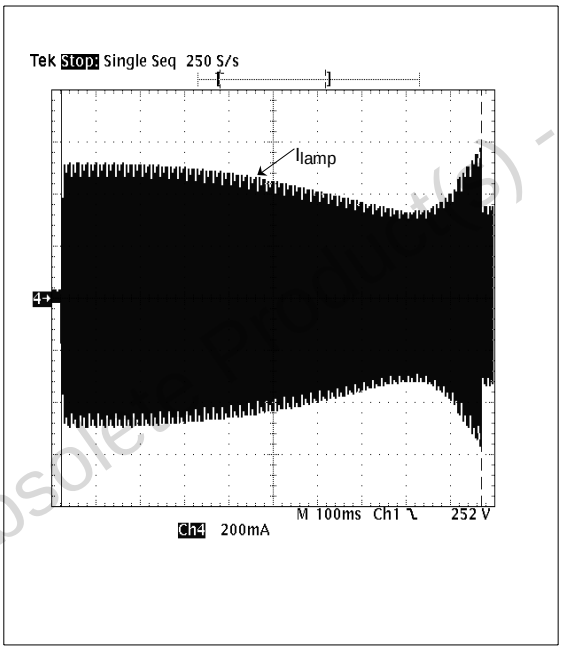
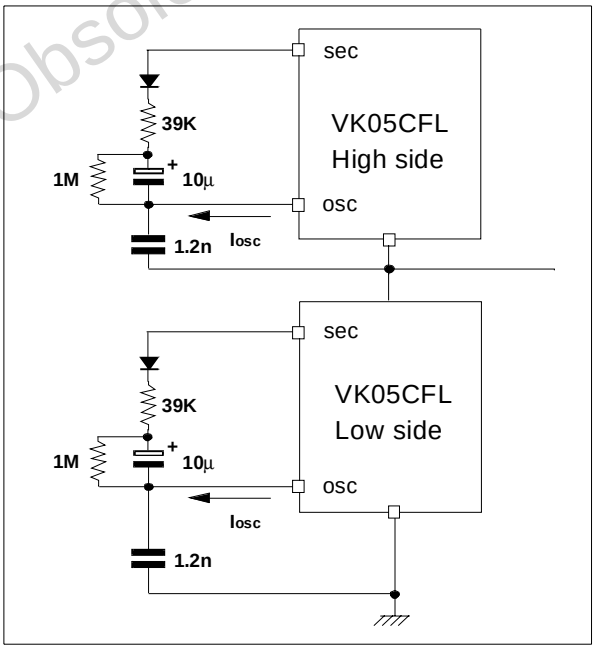


Figure 5b: Pre-heating low voltage network



Obsolete Product(s) - Obsolete Product(s)

APPLICATION BOARD

Please note that this demo can be used for Europe (230Vrms) market as well as for USA (110Vrms) market.

In order to use the demoboard for Europe market the following modification must be done: electrolytic capacitors C1 and C12 must be replaced with only one electrolytic capacitor Cx = 3,3µF/400V connected with the positive pin on the D1 catode and the negative pin on the D3 anode. Also different power range CFL can be driven by using this demoboard; on the left side of the component list reported below you find component values able to drive CFL in the power range 5W to 15W, the component values written in brackets in the table on the right are referred to the power range 15W to 23W.

COMPONENT LIST

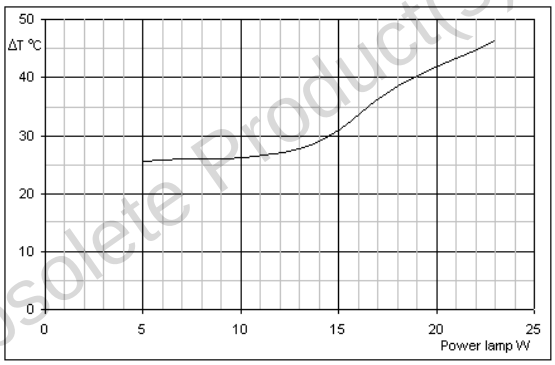
5W to 15W lamp	
Reference	**Value**
T1	Lp=3,1mH, N1/N2=N1/N3=10
L_0	820µH
D0,D1,D2,D3	1N4007
C1, C12	22µF/200V electrolytic (for Europe to replace C1, C12 with Cx=3,3µF/400V)
C2, C3	100nF/250V
C4	2,4nF/400V
C5, C6	1.2nF/63V
C7	470pF/400V
C8	22nF/100V
C10, C11	1.5nF/100V
R0	10Ω 1/2W
R1, R2	1MΩ 1/4W
R4, R5	2.2KΩ 1/4W
U1, U2	VK05CFL

>15W to 23W lamp	
Reference	**Value**
T1	Lp=2,1mH, N1/N2=N1/N3=10
L_0	820µH
D0,D1,D2,D3	1N4007
C1, C12	22µF/200V electrolytic (for Europe Cx=6.8µF/400V)
C2, C3	100nF/250V
C4	2,4nF/400V
C5, C6	1nF/63V
C7	470pF/400V
C8	22nF/100V
C10, C11	1.5nF/100V
R0	10Ω 1/2W
R1, R2	1MΩ 1/4W
R4, R5	1KΩ 1/2W
U1, U2	VK05CFL

Obsolete Product(s) - Obsolete Product(s)

Waveforms below was obtained by using the application demoboard mounted for european market:

Device ΔT (T_{amb}=25 °C) for different power lamps



Device power dissipation Vs. power lamp

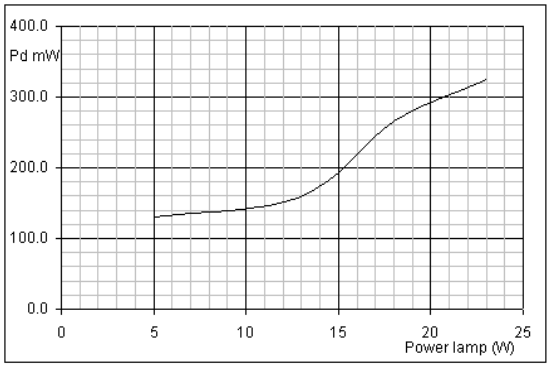
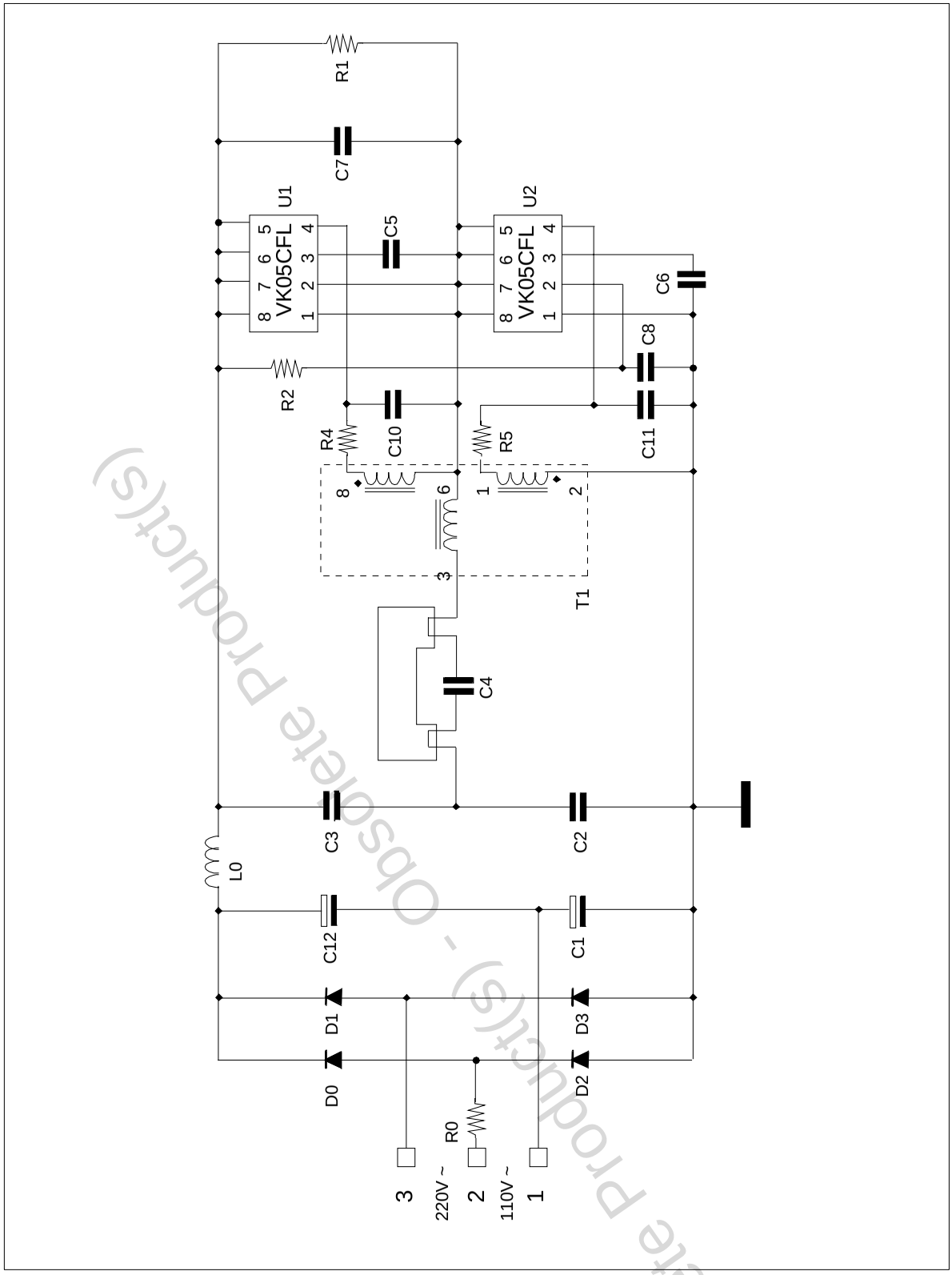


Figure 6: Board electrical scheme



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Figure 7: Printed Circuit Board legend (Component side)

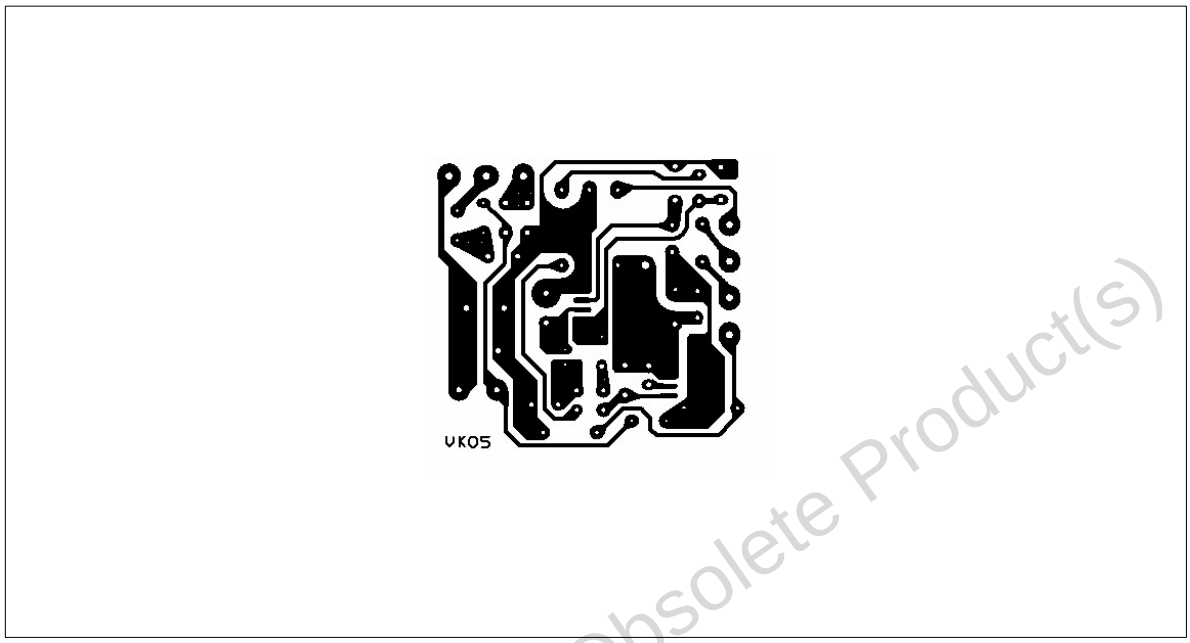
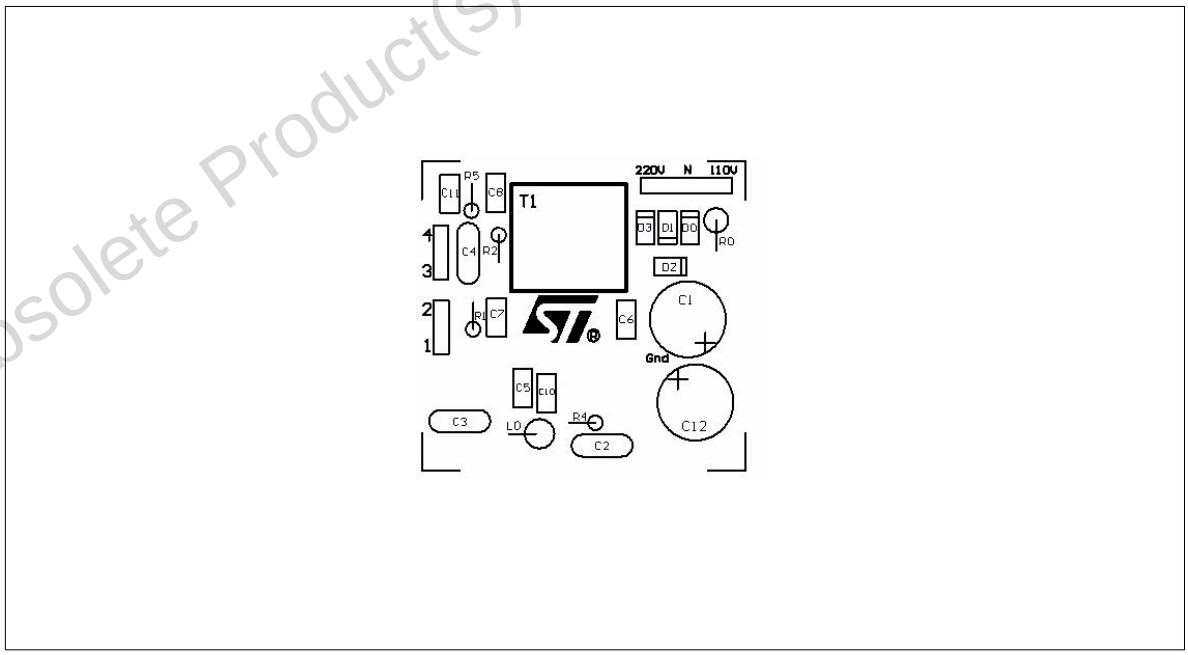
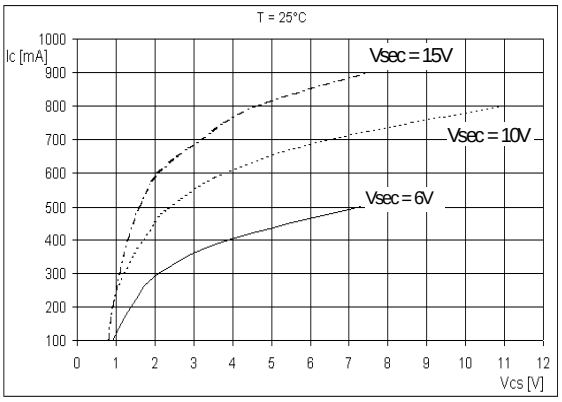


Figure 8: Printed Circuit Board top foil

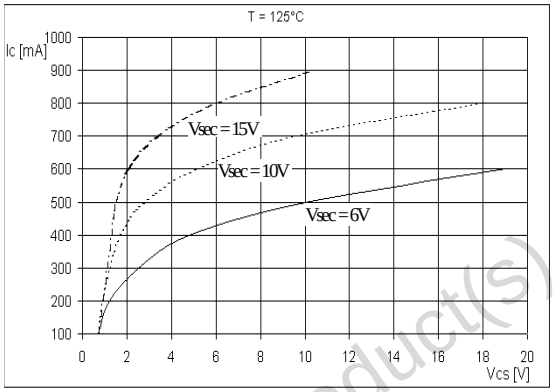


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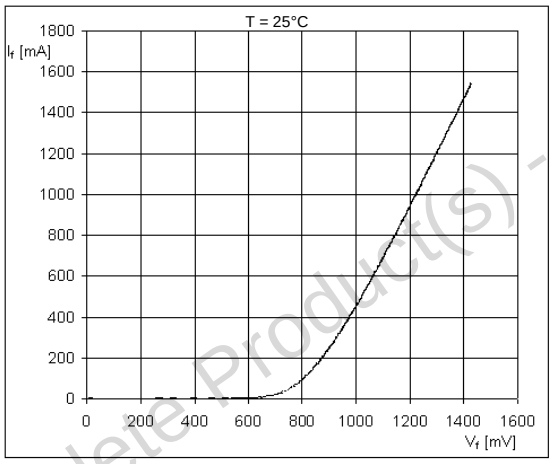
Collector current Vs. collector-source saturation voltage at T_{amb}=25ºC



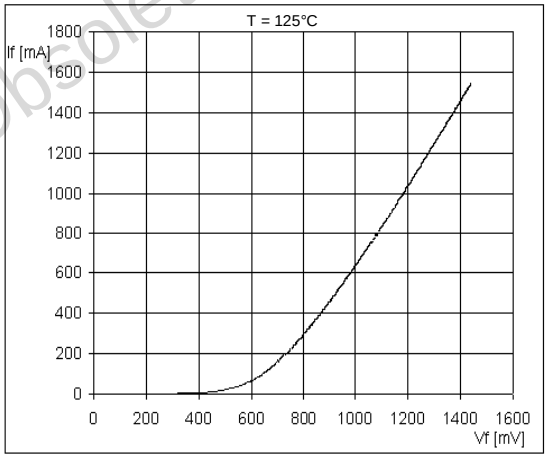
Collector current Vs. collector-source saturation voltage at T_{amb}=125ºC



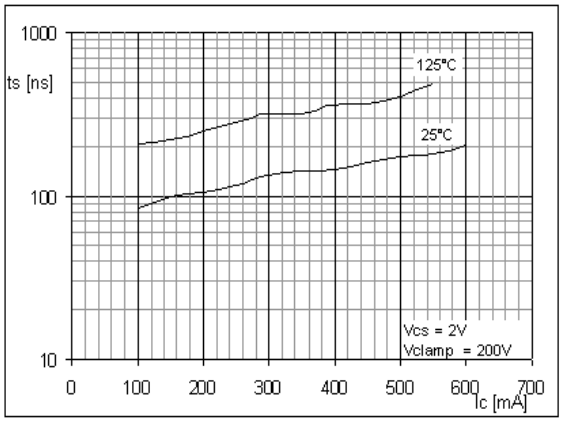
Freewheeling diode I_f=f(V_f) characteristic at T_{amb}=25ºC



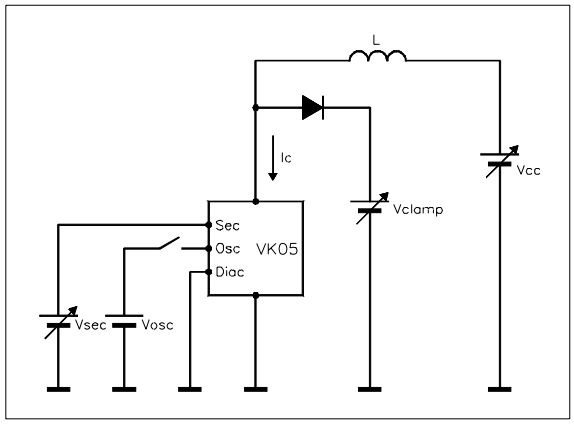
Freewheeling diode I_f=f(V_f) characteristic at T_{amb}=125ºC



Bipolar storage time Vs. collector current



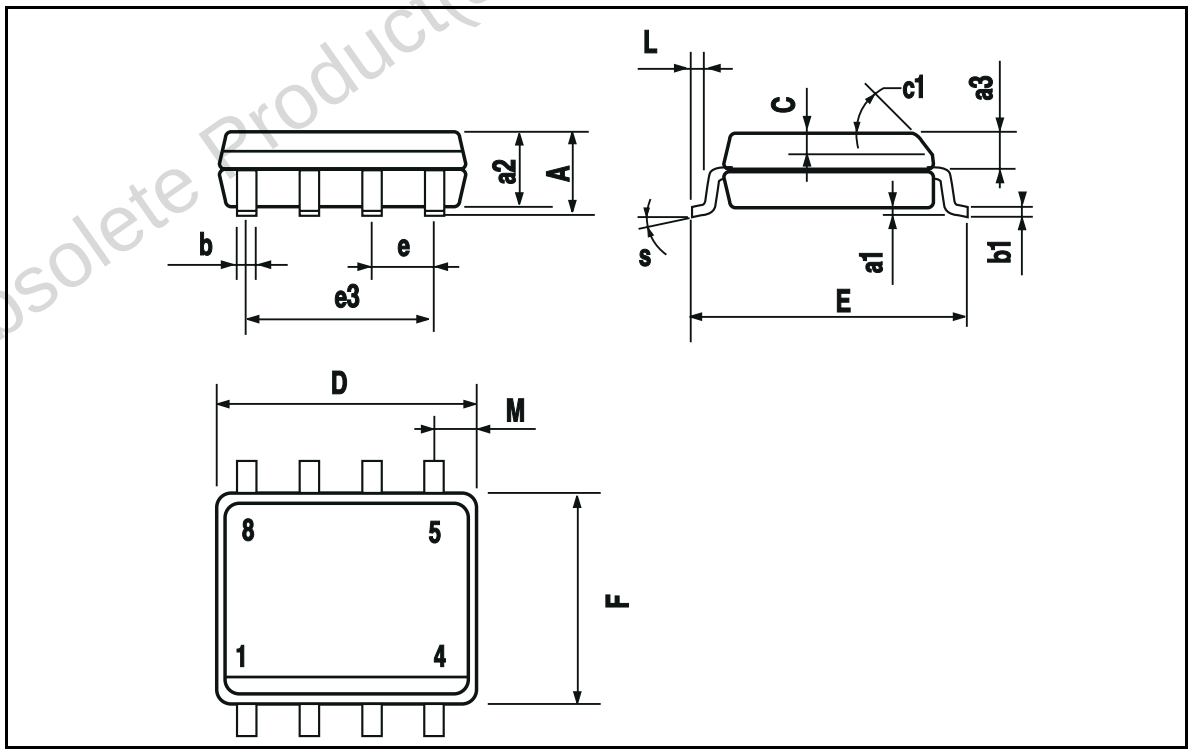
Test circuit



Obsolete Product(s) - Obsolete Product(s)

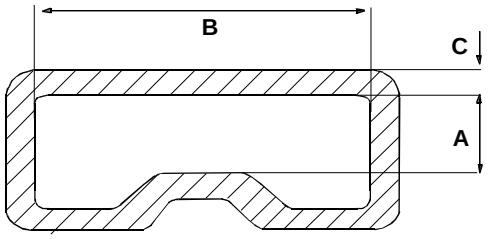
SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					
L1	0.8		1.2	0.031		0.047



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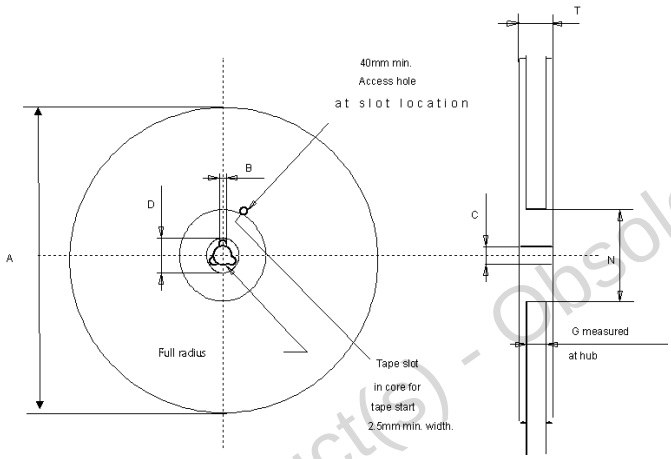
SO-8 TUBE SHIPMENT (no suffix)



Base Q.ty	100
Bulk Q.ty	2000
Tube length (± 0.5)	532
A	3.2
B	6
C (± 0.1)	0.6

All dimensions are in mm.

TAPE AND REEL SHIPMENT (suffix "13TR")



REEL DIMENSIONS

Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

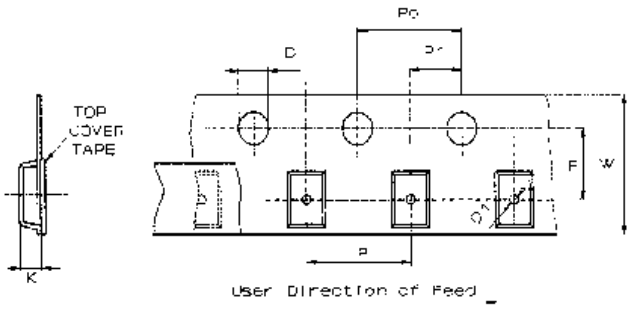
All dimensions are in mm.

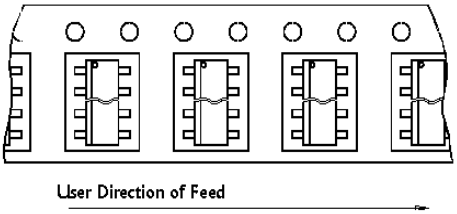
TAPE DIMENSIONS

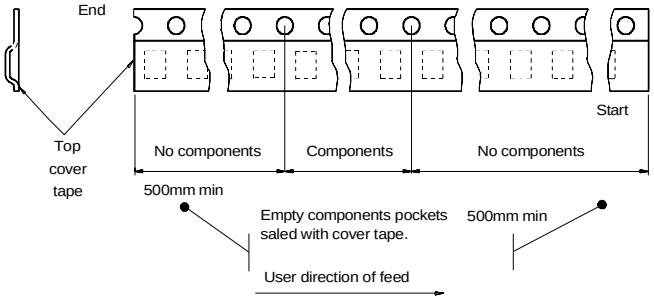
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	12
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	8
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	5.5
Compartment Depth	**K (max)**	4.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







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