

# Reference Manual

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## VL-1260

12-Bit Analog Input Card  
for the STD Bus





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# **VL-1260**

12-Bit Analog Input Card  
for the STD Bus



**Model VL-1260**  
**12-Bit Analog Input Card for the STD Bus**  
**REFERENCE MANUAL**

VL-1260 Rev. 2.01  
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**M1260**



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# Overview

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This manual details the installation and operation of VersaLogic's VL-1260 analog input card. This card interfaces directly with external analog voltages and provides digital readings to the STD Bus with 12-bit accuracy.

## Introduction

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In its standard configuration the VL-1260 provides 16 single-ended, or 8 differential analog input channels. An optional expansion kit increases the number of input channels to 32 single-ended, or 16 differential inputs. It features 12-bit resolution, 25  $\mu$ s conversion time, and an on-board DC to DC converter (requires +5 volt supply only). The board operates with an input range 0 to +10, or  $\pm 10$  volts with an adjustable gain of 1 to 1000. It can accommodate input signals in a single-ended, differential, or pseudo-differential configuration.

Each input channel can be read as desired by the system CPU. The board is capable of 25,000 samples per second throughput at a gain of 1 to 150.

The VL-1260 is plug-in compatible with the Analog Devices RTI-1260 card.

## Features

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- 16 single-ended or 8 differential input channels (expandable to 32 s.e./16 Diff.).
- 12-bit (4096 counts) resolution.
- 25  $\mu$ s input conversion time.
- 25,000 samples per send throughput.
- 0 to +10, or  $\pm 10$  volt input ranges.
- Input gain of 1 to 1000.
- 16-bit memory or I/O addressing.
- MEMEX and IOEXP supported.
- +5 volt single supply operation.
- Plug-in replacement for Analog Devices RTI-1260.

## **Specifications**

Specifications are typical at 25°C with 5.0V supply unless otherwise noted.

Number of Channels: 16 single-ended or 8 differential

Range: 0 to +10V,  $\pm 10V$

Resolution: 12 bits (4096 counts)

Conversion Time: 25  $\mu s$  + settling time

Throughput:

25,000 channels/sec (gain < 150)

20,000 channels/sec (gain = 150 to 300)

11,000 channels/sec (gain = 1000)

Overvoltage Protection:

$\pm 35V$  with power on

$\pm 20V$  with power off

Impedance:  $.6 \times 10^8 \Omega$  min.

Data Format: Binary, offset binary, or two's complement

Common Mode Voltage (CMV):  $\pm 10V$  min

Common Mode Rejection (CMR): 78 dB

Linearity:  $\pm \frac{1}{2}$  LSB

Differential Nonlinearity:  $\pm \frac{1}{2}$  LSB

Temperature Coefficient:

Gain  $\pm 30$  ppm/°C of FSR (gain = 1)

Gain  $\pm 100$  ppm/°C of FSR (gain = 1000)

Offset  $\pm 10$  ppm/°C of FSR (gain = 1)

Offset  $\pm 100$  ppm/°C of FSR (gain = 1000)

Addressing: 16 bits + MEMEX or IOEXP

Mapping: 8-byte memory or I/O block on any 8-byte boundary

Size: Meets all STD 32 Bus mechanical specifications

Storage Temperature:  $-40^\circ$  to  $+75^\circ C$

Free Air Operating Temperature:  $0^\circ$  to  $+65^\circ C$

Power Requirements:

5V  $\pm 5\%$  @ 225 ma typ.

Bus Compatibility:

STD 80: Full compliance, all bus speeds

STD Z80: Full compliance, all bus speeds

STD 32: I/O Slave, SA8

# Configuration

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## Jumper Options

Various options available on the VL-1260 cards are selected using removable jumper blocks (shorting plugs). Features are selected or deselected by installing or removing the jumpers as noted. The terms "In" or "Jumpered" are used to indicate an installed plug; "Out" or "Open" are used to indicate a removed plug.

Figure 2-1 shows the jumper block locations on the VL-1260 card. The figures indicate the position of the jumpers as shipped from the factory.

VL-1260 Jumper Block Locations

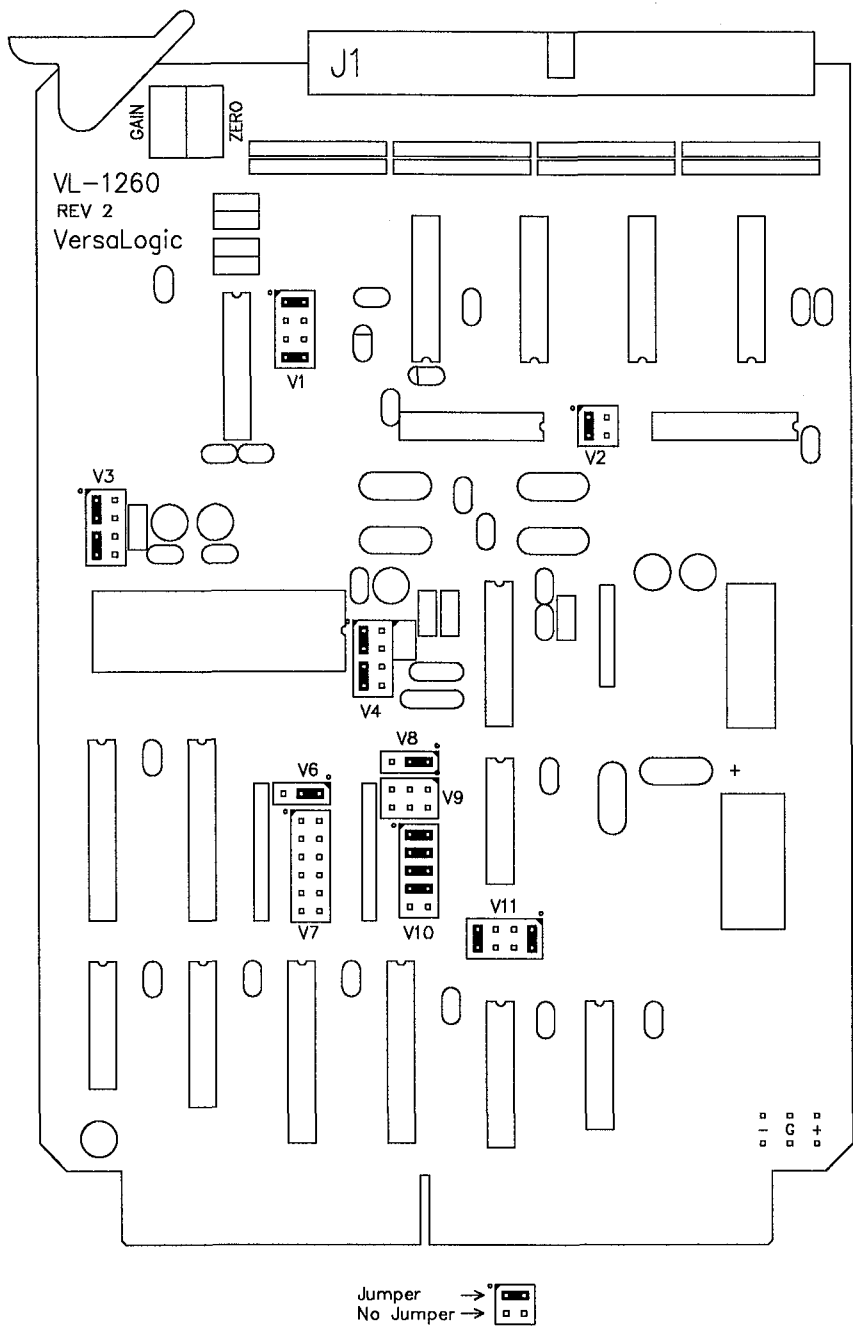


Figure 2-1. Jumper Block Locations for VL-1260

## VL-1260 Jumper Options

| Jumper Block | Description                                                                                                                                                             | As Shipped | Page |
|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|------|
| V1 & V2      | Input Mode ..... S.E.                                                                                                                                                   |            | 2-11 |
|              | V1 <sub>1-2</sub> = In, V1 <sub>3-4</sub> = Out, V1 <sub>5-6</sub> = Out, V1 <sub>7-8</sub> = In, V2 <sub>1-3</sub> = In, V2 <sub>2-4</sub> = Out – Single Ended        |            |      |
|              | V1 <sub>1-2</sub> = Out, V1 <sub>3-4</sub> = In, V1 <sub>5-6</sub> = Out, V1 <sub>7-8</sub> = In, V2 <sub>1-3</sub> = In, V2 <sub>2-4</sub> = Out – Pseudo-Differential |            |      |
|              | V1 <sub>1-2</sub> = Out, V1 <sub>3-4</sub> = Out, V1 <sub>5-6</sub> = In, V1 <sub>7-8</sub> = Out, V2 <sub>1-3</sub> = Out, V2 <sub>2-4</sub> = In – Differential       |            |      |
| V3           | Input Voltage Range Select ..... ±10V                                                                                                                                   |            | 2-14 |
|              | V3 <sub>1-3</sub> = In, V3 <sub>2-4</sub> = Out, V3 <sub>5-7</sub> = In, V3 <sub>6-8</sub> = Out – ±10V                                                                 |            |      |
|              | V3 <sub>1-3</sub> = Out, V3 <sub>2-4</sub> = In, V3 <sub>5-7</sub> = Out, V3 <sub>6-8</sub> = In – 0 to 10V                                                             |            |      |
| V4           | Input Data Format ..... 2's Comp.                                                                                                                                       |            | 2-15 |
|              | V4 <sub>1-3</sub> = In, V4 <sub>2-4</sub> = Out, V4 <sub>5-7</sub> = In, V4 <sub>6-8</sub> = Out – Two's Complement                                                     |            |      |
|              | V4 <sub>1-3</sub> = Out, V4 <sub>2-4</sub> = In, V4 <sub>5-7</sub> = Out, V4 <sub>6-8</sub> = In – Binary / Offset Binary                                               |            |      |
| V5           | External Trigger – Contact Factory                                                                                                                                      |            |      |
| V6           | MEMEX Select ..... Ignore                                                                                                                                               |            | 2-5  |
|              | V6 <sub>1-2</sub> = In, V6 <sub>2-3</sub> = Out – Ignore MEMEX                                                                                                          |            |      |
|              | V6 <sub>1-2</sub> = Out, V6 <sub>2-3</sub> = Out – Enable on MEMEX high                                                                                                 |            |      |
|              | V6 <sub>1-2</sub> = Out, V6 <sub>2-3</sub> = In – Enable on MEMEX low                                                                                                   |            |      |
| V7           | Board Address (A10 – A15) ..... FF08H                                                                                                                                   |            | 2-5  |
|              | V7 <sub>1-2</sub> = In – A15 decoded Low, V7 <sub>1-2</sub> = Out – A15 decoded High                                                                                    |            |      |
|              | V7 <sub>3-4</sub> = In – A14 decoded Low, V7 <sub>3-4</sub> = Out – A14 decoded High                                                                                    |            |      |
|              | V7 <sub>5-6</sub> = In – A13 decoded Low, V7 <sub>5-6</sub> = Out – A13 decoded High                                                                                    |            |      |
|              | V7 <sub>7-8</sub> = In – A12 decoded Low, V7 <sub>7-8</sub> = Out – A12 decoded High                                                                                    |            |      |
|              | V7 <sub>9-10</sub> = In – A11 decoded Low, V7 <sub>9-10</sub> = Out – A11 decoded High                                                                                  |            |      |
|              | V7 <sub>11-12</sub> = In – A10 decoded Low, V7 <sub>11-12</sub> = Out – A10 decoded High                                                                                |            |      |
| V8           | IOEXP Select ..... Ignore                                                                                                                                               |            | 2-5  |
|              | V8 <sub>1-2</sub> = In, V8 <sub>2-3</sub> = Out – Ignore IOEXP                                                                                                          |            |      |
|              | V8 <sub>1-2</sub> = Out, V8 <sub>2-3</sub> = Out – Enable on IOEXP high                                                                                                 |            |      |
|              | V8 <sub>1-2</sub> = Out, V8 <sub>2-3</sub> = In – Enable on IOEXP low                                                                                                   |            |      |
| V9           | Board Address (A8, A9) / 8-Bit Mode Selector ..... FF08H                                                                                                                |            | 2-5  |
|              | V9 <sub>1-3</sub> = In, V9 <sub>2-4</sub> = In, V9 <sub>3-5</sub> = Out, V9 <sub>4-6</sub> = Out – 8-Bit Mode (Ignore A8 & A9)                                          |            |      |
|              | V9 <sub>1-3</sub> = Out, V9 <sub>2-4</sub> = Out, V9 <sub>3-5</sub> = Out, V9 <sub>4-6</sub> = Out – 10- or 16-Bit Decoding (A8 = High, A9 = High)                      |            |      |
|              | V9 <sub>1-3</sub> = Out, V9 <sub>2-4</sub> = Out, V9 <sub>3-5</sub> = In, V9 <sub>4-6</sub> = Out – 10- or 16-Bit Decoding (A8 = High, A9 = Low)                        |            |      |
|              | V9 <sub>1-3</sub> = Out, V9 <sub>2-4</sub> = Out, V9 <sub>3-5</sub> = Out, V9 <sub>4-6</sub> = In – 10- or 16-Bit Decoding (A8 = Low, A9 = High)                        |            |      |
|              | V9 <sub>1-3</sub> = Out, V9 <sub>2-4</sub> = Out, V9 <sub>3-5</sub> = In, V9 <sub>4-6</sub> = In – 10- or 16-Bit Decoding (A8 = Low, A9 = Low)                          |            |      |
| V10          | Board Address (A3 – A7) ..... FF08H                                                                                                                                     |            | 2-5  |
|              | V10 <sub>1-2</sub> = In – A7 decoded Low, V10 <sub>1-2</sub> = Out – A7 decoded High                                                                                    |            |      |
|              | V10 <sub>3-4</sub> = In – A6 decoded Low, V10 <sub>3-4</sub> = Out – A6 decoded High                                                                                    |            |      |
|              | V10 <sub>5-6</sub> = In – A5 decoded Low, V10 <sub>5-6</sub> = Out – A5 decoded High                                                                                    |            |      |
|              | V10 <sub>7-8</sub> = In – A4 decoded Low, V10 <sub>7-8</sub> = Out – A4 decoded High                                                                                    |            |      |
|              | V10 <sub>9-10</sub> = In – A3 decoded Low, V10 <sub>9-10</sub> = Out – A3 decoded High                                                                                  |            |      |
| V11          | Address Type Select ..... Memory                                                                                                                                        |            | 2-5  |
|              | V11 <sub>1-2</sub> = In, V11 <sub>3-4</sub> = Out, V11 <sub>5-6</sub> = Out, V11 <sub>7-8</sub> = In – 16-Bit Memory Mapped                                             |            |      |
|              | V11 <sub>1-2</sub> = In, V11 <sub>3-4</sub> = Out, V11 <sub>5-6</sub> = In, V11 <sub>7-8</sub> = Out – 8- or 10-Bit I/O Mapped                                          |            |      |
|              | V11 <sub>1-2</sub> = Out, V11 <sub>3-4</sub> = In, V11 <sub>5-6</sub> = Out, V11 <sub>7-8</sub> = In – 16-Bit I/O Mapped                                                |            |      |

Figure 2-2. VL-1260 Jumper Functions

## **Board Addressing**

The VL-1260 supports 8-, 10-, and 16-bit I/O addressing, and 16-bit memory addressing. 8-bit I/O addressing is used with most 8-bit processors (Z80, 8085, 6809, etc.) which provide 256 I/O addresses. 10- or 16-bit addressing can be used with 16-bit processors (8088, 80188, 80186, etc.) to decode 1024 or 65536 I/O port addresses. 16-bit memory addressing can be used with most 8-bit processors (Z80, 8085, 6809, etc.) if desired.

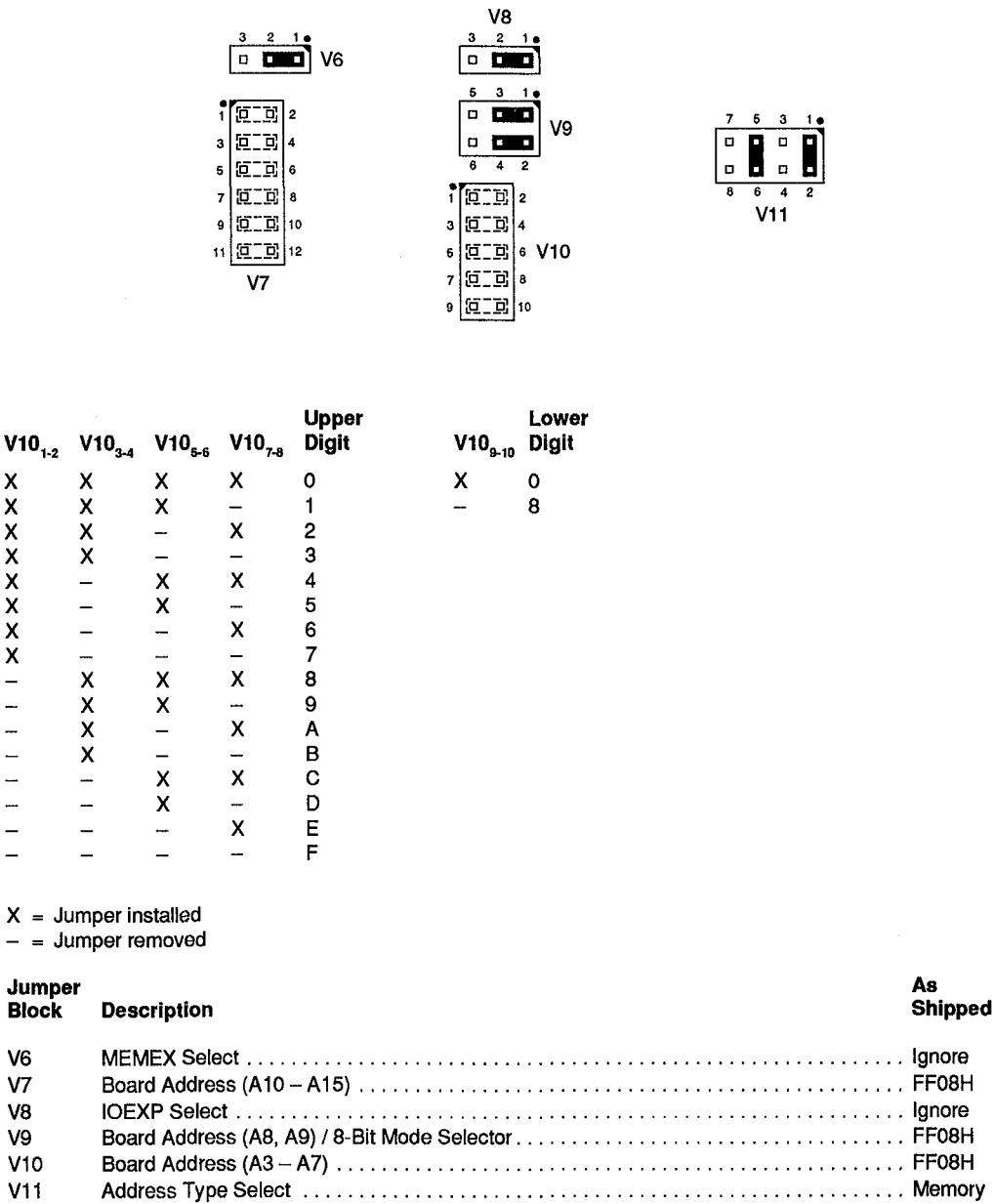
I/O addressing can be extended (capacity doubled) using the IOEXP signal which is decoded by the VL-1260. Memory addressing can be extended (capacity doubled) using the MEMEX signal which is decoded by the VL-1260.

As shipped the board is configured for 16-bit memory addressing with a board address of hex FF08. The card occupies eight consecutive addresses (i.e. FF08H to FF0FH). The VL-1260 uses three of these addresses as control, data, and status registers, the remaining five are inaccessible. See the Register Mapping section on page 4-1 for further information.

8-Bit I/O Addressing

To configure the board for an 8-bit I/O address refer to the figure below. Use the table to select the jumpering for the appropriate upper and lower halves of the desired starting address (i.e., “3” and “0” = hex address 30).

This jumper configuration ignores the state of the IOEXP signal in addressing the board. To use the IOEXP signal refer to page 2-8.



7

5

3

1

V11

X = Jumper installed

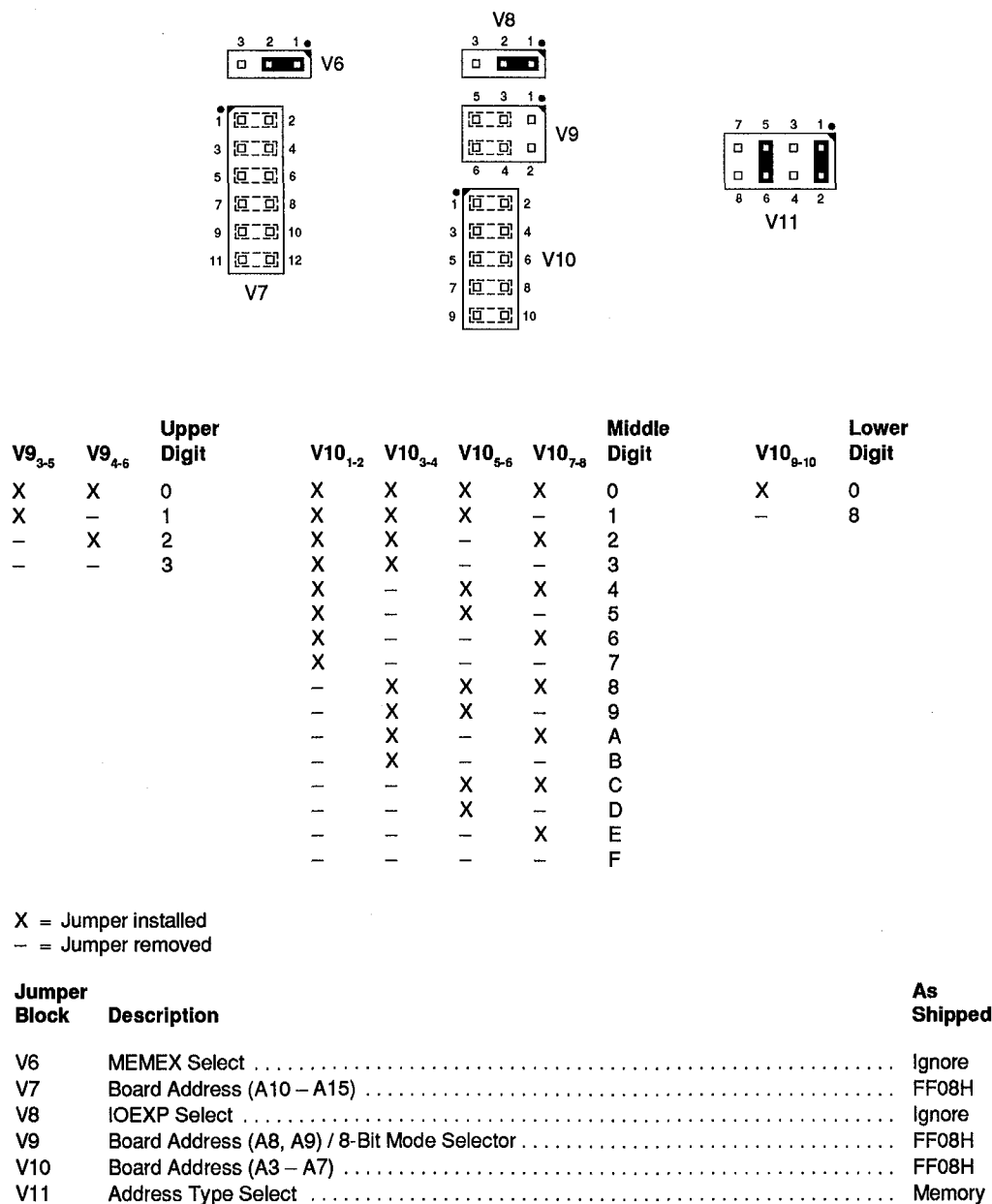
— = Jumper removed

Figure 2-3. 8-Bit I/O Address Jumpers

10-Bit I/O Addressing

To configure the board for a 10-bit I/O address refer to the figure below. Use the table to select the jumpering for the appropriate upper, middle, and lower hex digits of the desired starting address (i.e., “1” and “3” and “0” = hex address 130).

This jumper configuration ignores the state of the IOEXP signal in addressing the board. To use the IOEXP signal refer to page 2-8.



7

5

3

1

V11

X = Jumper installed

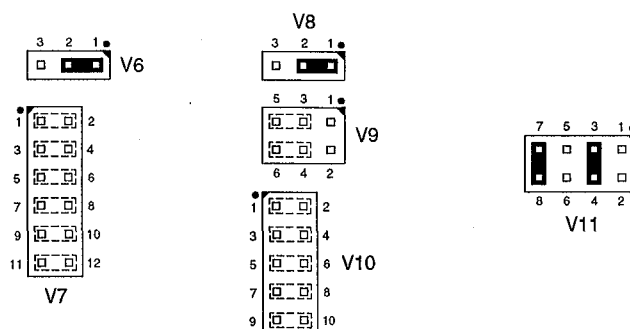
— = Jumper removed

Figure 2-4. 10-Bit I/O Address Jumpers

## 16-Bit I/O Addressing

To configure the board for a 16-bit I/O address refer to the figure below. See the table to select the jumpering for the appropriate four hex digits of the desired starting address (i.e., “6” and “1” and “3” and “0” = hex address 6130).

This jumper configuration ignores the state of the IOEXP signal in addressing the board. To use the IOEXP signal refer to page 2-8.



| Upper Digit       |                   |                   |                   | Second Digit       |                     |                   |                   | Third Digit        |                    |                    |                    | Lower Digit         |     |
|-------------------|-------------------|-------------------|-------------------|--------------------|---------------------|-------------------|-------------------|--------------------|--------------------|--------------------|--------------------|---------------------|-----|
| V7 <sub>1-2</sub> | V7 <sub>3-4</sub> | V7 <sub>5-6</sub> | V7 <sub>7-8</sub> | V7 <sub>9-10</sub> | V7 <sub>11-12</sub> | V9 <sub>3-5</sub> | V9 <sub>4-6</sub> | V10 <sub>1-2</sub> | V10 <sub>3-4</sub> | V10 <sub>5-6</sub> | V10 <sub>7-8</sub> | V10 <sub>9-10</sub> |     |
| X                 | X                 | X                 | X                 | 0                  | X                   | X                 | X                 | 0                  | X                  | X                  | X                  | 0                   | X 0 |
| X                 | X                 | X                 | —                 | 1                  | X                   | X                 | X                 | —                  | 1                  | X                  | X                  | —                   | — 8 |
| X                 | X                 | —                 | X                 | 2                  | X                   | X                 | —                 | X                  | 2                  | X                  | X                  | —                   |     |
| X                 | X                 | —                 | —                 | 3                  | X                   | X                 | —                 | —                  | 3                  | X                  | X                  | —                   |     |
| X                 | —                 | X                 | X                 | 4                  | X                   | —                 | X                 | X                  | 4                  | X                  | —                  | X                   |     |
| X                 | —                 | X                 | —                 | 5                  | X                   | —                 | X                 | —                  | 5                  | X                  | —                  | X                   |     |
| X                 | —                 | —                 | X                 | 6                  | X                   | —                 | —                 | X                  | 6                  | X                  | —                  | —                   |     |
| X                 | —                 | —                 | —                 | 7                  | X                   | —                 | —                 | —                  | 7                  | X                  | —                  | —                   |     |
| —                 | X                 | X                 | X                 | 8                  | —                   | X                 | X                 | X                  | 8                  | —                  | X                  | X                   |     |
| —                 | X                 | X                 | —                 | 9                  | —                   | X                 | X                 | —                  | 9                  | —                  | X                  | X                   |     |
| —                 | X                 | —                 | X                 | A                  | —                   | X                 | —                 | X                  | A                  | —                  | X                  | —                   |     |
| —                 | X                 | —                 | —                 | B                  | —                   | X                 | —                 | —                  | B                  | —                  | X                  | —                   |     |
| —                 | —                 | X                 | X                 | C                  | —                   | —                 | X                 | X                  | C                  | —                  | —                  | X                   |     |
| —                 | —                 | X                 | —                 | D                  | —                   | —                 | —                 | —                  | D                  | —                  | —                  | X                   |     |
| —                 | —                 | —                 | X                 | E                  | —                   | —                 | —                 | X                  | E                  | —                  | —                  | —                   |     |
| —                 | —                 | —                 | —                 | F                  | —                   | —                 | —                 | —                  | F                  | —                  | —                  | —                   |     |

X = Jumper installed  
— = Jumper removed

| Jumper Block | Description                                        | As Shipped |
|--------------|----------------------------------------------------|------------|
| V6           | MEMEX Select .....                                 | Ignore     |
| V7           | Board Address (A10 – A15) .....                    | FF08H      |
| V8           | IOEXP Select .....                                 | Ignore     |
| V9           | Board Address (A8, A9) / 8-Bit Mode Selector ..... | FF08H      |
| V10          | Board Address (A3 – A7) .....                      | FF08H      |
| V11          | Address Type Select .....                          | Memory     |

Figure 2-5. 16-Bit I/O Address Jumpers

IOEXP Signal

The IOEXP (I/O expansion) signal on the STD Bus is normally used to select between two different I/O banks or maps. It can be used to double the number of available I/O addresses in the system (by selecting between two banks of I/O boards). The IOEXP signal is usually controlled by (or jumpered to ground on) the system CPU card.

A low IOEXP signal usually selects the standard or normal I/O map. A high IOEXP signal usually selects the secondary or alternate I/O map. Boards that ignore (or do not decode) IOEXP will appear in both I/O maps.

As shipped the IOEXP jumper is configured to ignore the IOEXP signal. The board will be addressed whether the IOEXP signal is high or low. It can be jumpered for two other modes as shown below.

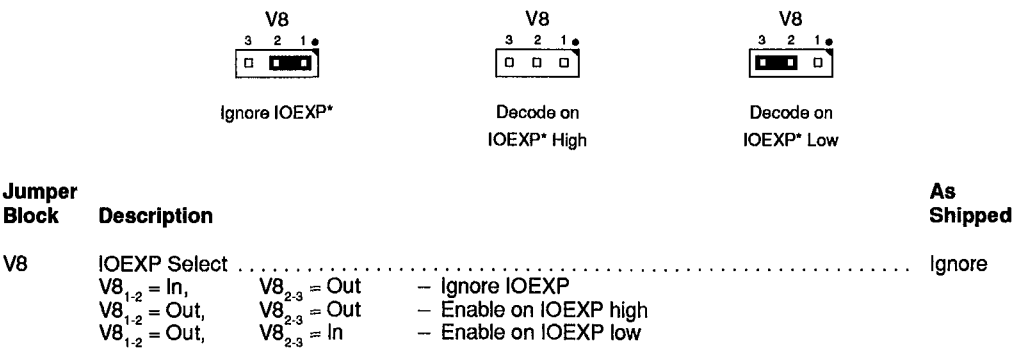
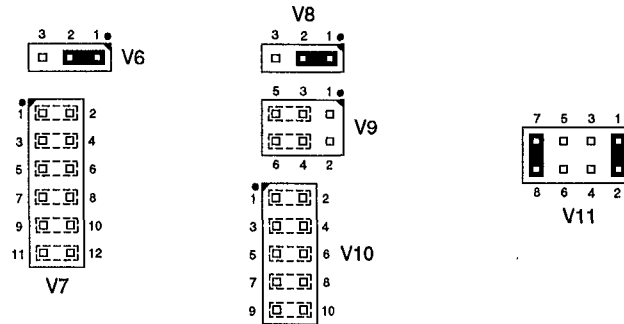


Figure 2-6. IOEXP Options

## 16-Bit Memory Addressing

To configure the board for a 16-bit memory address refer to the figure below. Use the table to select the jumpering for the appropriate four hex digits of the desired starting address (i.e., “6” and “1” and “3” and “0” = hex address 6130).

This jumper configuration ignores the state of the MEMEX signal in addressing the board. To use the MEMEX signal refer to the MEMEX Signal heading in this section.



|                   |                   |                   |                   | Upper Digit |                    |                     |                   |                   | Second Digit |                    |                    |                    |                    | Third Digit | Lower Digit         |   |
|-------------------|-------------------|-------------------|-------------------|-------------|--------------------|---------------------|-------------------|-------------------|--------------|--------------------|--------------------|--------------------|--------------------|-------------|---------------------|---|
| V7 <sub>1-2</sub> | V7 <sub>3-4</sub> | V7 <sub>5-6</sub> | V7 <sub>7-8</sub> |             | V7 <sub>9-10</sub> | V7 <sub>11-12</sub> | V9 <sub>3-5</sub> | V9 <sub>4-6</sub> |              | V10 <sub>1-2</sub> | V10 <sub>3-4</sub> | V10 <sub>5-6</sub> | V10 <sub>7-8</sub> |             | V10 <sub>9-10</sub> |   |
| X                 | X                 | X                 | X                 | 0           | X                  | X                   | X                 | X                 | 0            | X                  | X                  | X                  | X                  | 0           | X                   | 0 |
| X                 | X                 | X                 | –                 | 1           | X                  | X                   | X                 | –                 | 1            | X                  | X                  | X                  | –                  | 1           | –                   | 8 |
| X                 | X                 | –                 | X                 | 2           | X                  | X                   | –                 | X                 | 2            | X                  | X                  | –                  | X                  | 2           |                     |   |
| X                 | X                 | –                 | –                 | 3           | X                  | X                   | –                 | –                 | 3            | X                  | X                  | –                  | –                  | 3           |                     |   |
| X                 | –                 | X                 | X                 | 4           | X                  | –                   | X                 | X                 | 4            | X                  | –                  | X                  | X                  | 4           |                     |   |
| X                 | –                 | X                 | –                 | 5           | X                  | –                   | X                 | –                 | 5            | X                  | –                  | X                  | –                  | 5           |                     |   |
| X                 | –                 | –                 | X                 | 6           | X                  | –                   | –                 | X                 | 6            | X                  | –                  | –                  | X                  | 6           |                     |   |
| X                 | –                 | –                 | –                 | 7           | X                  | –                   | –                 | –                 | 7            | X                  | –                  | –                  | –                  | 7           |                     |   |
| –                 | X                 | X                 | X                 | 8           | –                  | X                   | X                 | X                 | 8            | –                  | X                  | X                  | X                  | 8           |                     |   |
| –                 | X                 | X                 | –                 | 9           | –                  | X                   | X                 | –                 | 9            | –                  | X                  | X                  | –                  | 9           |                     |   |
| –                 | X                 | –                 | X                 | A           | –                  | X                   | –                 | X                 | A            | –                  | X                  | –                  | X                  | A           |                     |   |
| –                 | X                 | –                 | –                 | B           | –                  | X                   | –                 | –                 | B            | –                  | X                  | –                  | –                  | B           |                     |   |
| –                 | –                 | X                 | X                 | C           | –                  | –                   | X                 | X                 | C            | –                  | –                  | X                  | X                  | C           |                     |   |
| –                 | –                 | X                 | –                 | D           | –                  | –                   | X                 | –                 | D            | –                  | –                  | X                  | –                  | D           |                     |   |
| –                 | –                 | –                 | X                 | E           | –                  | –                   | –                 | X                 | E            | –                  | –                  | –                  | X                  | E           |                     |   |
| –                 | –                 | –                 | –                 | F           | –                  | –                   | –                 | –                 | F            | –                  | –                  | –                  | –                  | F           |                     |   |

X = Jumper installed  
– = Jumper removed

| Jumper Block | Description                                        | As Shipped |
|--------------|----------------------------------------------------|------------|
| V6           | MEMEX Select .....                                 | Ignore     |
| V7           | Board Address (A10 – A15) .....                    | FF08H      |
| V8           | IOEXP Select .....                                 | Ignore     |
| V9           | Board Address (A8, A9) / 8-Bit Mode Selector ..... | FF08H      |
| V10          | Board Address (A3 – A7) .....                      | FF08H      |
| V11          | Address Type Select .....                          | Memory     |

Figure 2-7. 16-Bit Memory Address Jumpers

## MEMEX Signal

The MEMEX (memory expansion) signal on the STD Bus is normally used to select between two different memory banks or maps. It can be used to double the number of available memory addresses in the system (by selecting between the two memory banks). The MEMEX signal is usually controlled by (or jumpered to ground on) the system CPU card.

A low MEMEX signal usually selects the standard or normal memory map. A high MEMEX signal usually selects the secondary or alternate memory map. Boards that ignore (or do not decode) MEMEX will appear in both memory maps.

As shipped the MEMEX jumper is configured to ignore the MEMEX signal. The board will be addressed whether the MEMEX signal is high or low. It can be jumpered for two other modes as shown below.

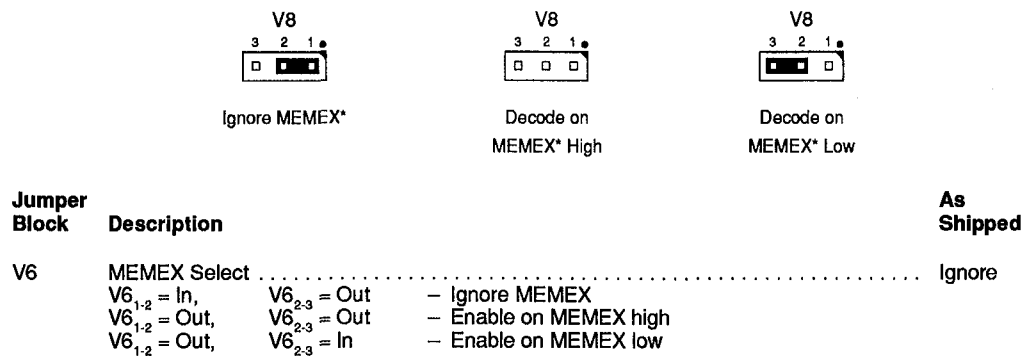


Figure 2-8. MEMEX Options

## Analog Input Configuration

The VL-1260 board accommodates 16 single-ended or 8 differential channels. An option kit for the VL-1260 (Part #9672), expands the board to accommodate 32 single-ended or 16 differential channels.

### Input Mode

The VL-1260 board can be configured for three types of voltage inputs: differential, single-ended, and pseudo-differential. In addition, by adding an external user-supplied 500  $\Omega$  resistor, the VL-1260 can be hooked up to a 4-20 ma current loop. All inputs connected to the boards must be of the same type.

Typical connections for the three input modes are shown in the figures below. Since ground loops (current flowing between various equipment ground lines) affect analog measurements made with reference to ground, careful attention should be paid to the ground connections shown. In particular, the STD Bus power supply logic ground line should never be connected to earth ground when operating in the differential or pseudo-differential modes.

#### Single Ended Mode

The single-ended mode is used for signals that are referenced to a common ground. It is normally used only for higher level signals on short distance runs (less than 10 feet). In this mode up to 16 input channels can be accommodated.

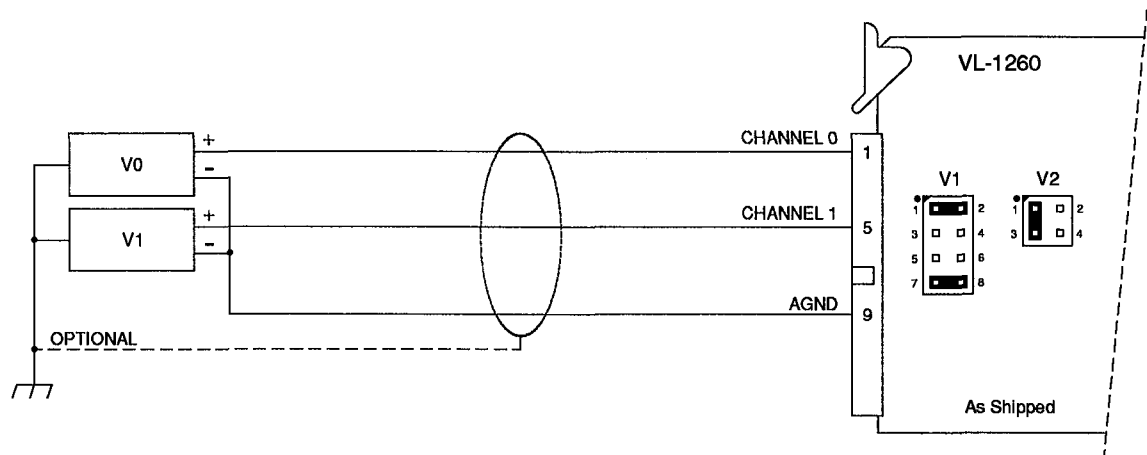


Figure 2-9. Single Ended Input Mode

### Pseudo-Differential Mode

The pseudo-differential mode is used for signals that are not referenced to ground, but are all connected to a single common return line. This mode can provide most of the advantages of full differential input while requiring fewer total wires. In the pseudo-differential mode, 16 input channels can be accommodated.

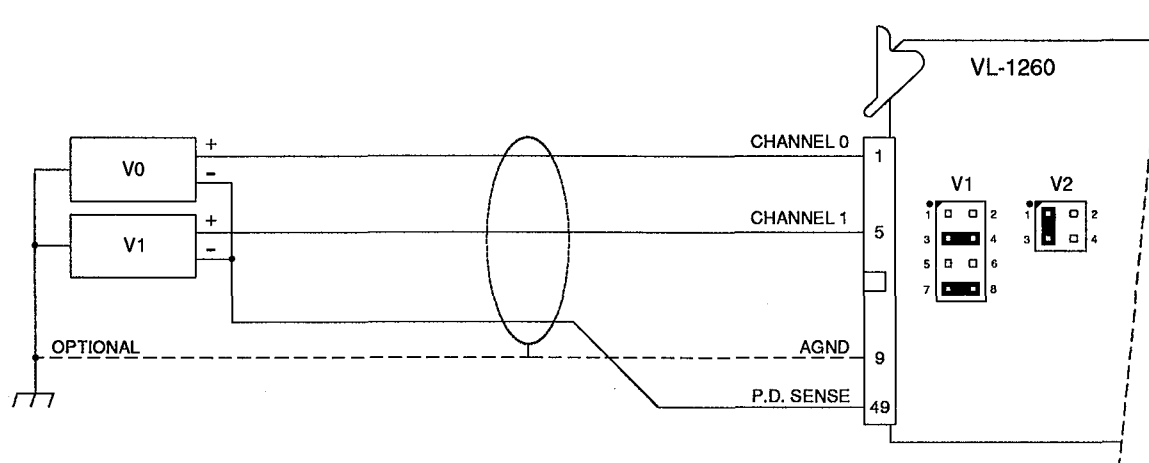


Figure 2-10. Pseudo-Differential Input Mode

### Differential Mode

The differential mode is used for signals that are not referenced to a common or ground point, but simply have a voltage difference between the two input wires (usually a twisted pair). It is desirable to use the differential mode in electrically noisy environments since it reduces the effects of electromagnetically induced noise and ground currents. It is especially useful in eliminating the effects of common mode noise generated on input lines over longer distances. In the differential mode, only eight input channels are available.

Note that in full differential operation a return path must be provided for the bias currents of the input amplifier. This can be accomplished by grounding the voltage source power supply(s) to the VL-1260 board, or by installing a 10K to 100K  $\Omega$  resistor as shown for each channel. These resistors should be located in close proximity to the voltage source.

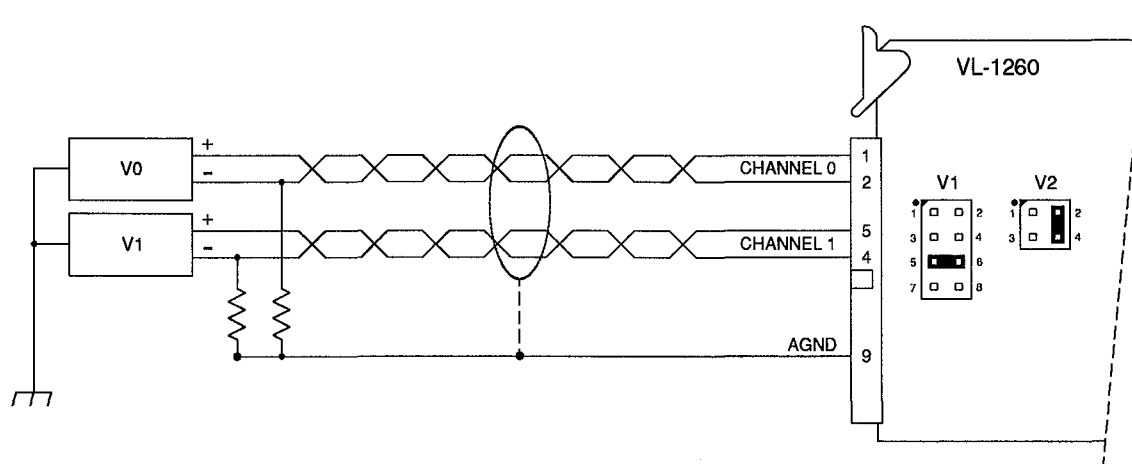


Figure 2-11. Differential Input Mode

**Current Loop Mode**

While the VL-1260 cannot directly hook up to a 4-20 ma current loop, the addition of an external user-supplied 500  $\Omega$  precision dropping resistor can be used to develop a 2-10 volt signal proportional to the 4-20 ma current. This voltage is applied to the VL-1260 as a differential-mode signal. The input range should be jumpered for unipolar 0 to 10V operation. The circuit below can be repeated for all 8 differential input channels.

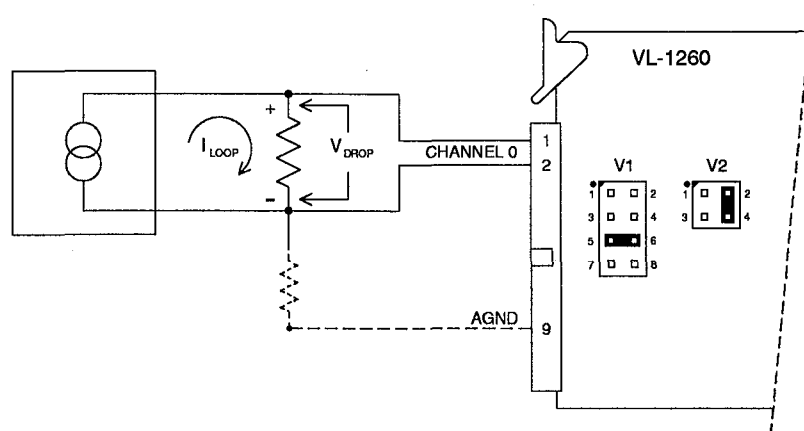
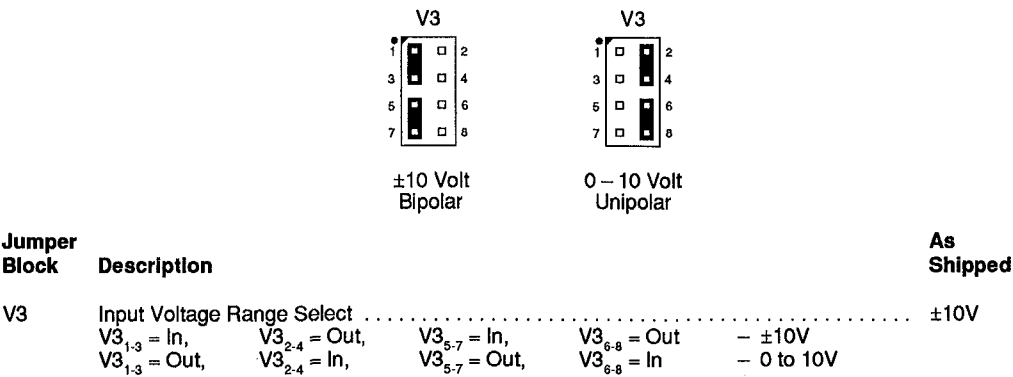


*Figure 2-12. Current Loop Input Mode*

### Input Voltage Range

The board may be operated with an input range of 0 to +10 volts, or ±10 volts. The 0 to +10 volt range is preferred for signals which do not go negative, since the per volt resolution is twice that of the ±10 volt range. Input voltage range selection applies to all input channels.



Input Data Format

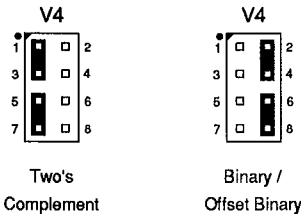
The digital data format for the analog input channels can be jumpered for binary, offset binary, or two's complement. The configuration affects all channels.

The selection is dependent upon the input voltage range selected with jumper V3. Unipolar voltages should use the binary data format. Bipolar voltages can use two's complement or offset binary formats, however, two's complement is the best choice since it "maps" the positive and negative voltages into positive and negative digital values.

See the Input Data Representation section starting on page 4-4 for further information on the various analog input data formats.

| Input Range | Valid Input Data Formats          |
|-------------|-----------------------------------|
| 0 to +10V   | Binary                            |
| ±10V        | Offset Binary or Two's Complement |

Figure 2-15. Valid Input Data Formats



| Jumper Block | Description                                     | As Shipped               |
|--------------|-------------------------------------------------|--------------------------|
| V4           | Input Data Format                               | 2's Complement           |
|              | V4 <sub>1-3</sub> = In, V4 <sub>2-4</sub> = Out | – Two's Complement       |
|              | V4 <sub>1-3</sub> = Out, V4 <sub>2-4</sub> = In | – Binary / Offset Binary |

Figure 2-16. Input Data Format Options



# Installation

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## Handling

**CAUTION:** The VL-1260 card uses chips which are sensitive to static electricity discharges. Normal precautions, such as discharging yourself, work stations, and tools to ground before touching the board should be taken whenever the board is handled.

The board should also be protected during shipment or storage by placing it in a conductive bag (such as the one it was received in) or by wrapping it in metal foil.

## Installation

The VL-1260 card can be installed in any slot of an STD Bus card cage, excluding Slot-X in STD 32 cages, and should only be used with other standard (TTL level bus) STD Bus boards. When inserting or extracting the VL-1260, make sure the system power is off, also make sure the card is properly oriented (ejector pointing up).

## Priority Chain

The VL-1260 card does not use the STD Bus priority interrupt chain signals PCO (P51) and PCI (P52). However, because PCI is connected to PCO on board, the card can be installed between cards using the chain.

## Signal Levels

The maximum non-destructive input voltage applied to any of the inputs on connector J1 is  $\pm 35\text{V}$  with power on ( $\pm 20\text{V}$  with power off). These voltages are measured with respect to analog ground. Each analog channel presents a minimum input impedance of  $.6 \times 10^8 \Omega$ .

# External Connections

J1 is an unlatched 50-pin dual-row (.1" center) header type connector. External connections to the VL-1260 can be made with standard cable assemblies, or with the following mating connectors:

## Mating Connectors

| Connector | Mating Connector                                    |
|-----------|-----------------------------------------------------|
| J1        | 50-pin socket type connectors such as 3M #3425-6650 |

Figure 3-1. Mating Connectors

## Physical Pin Locations

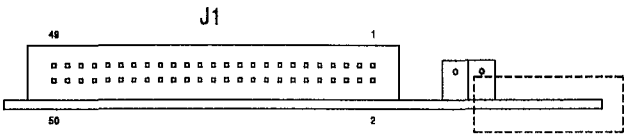


Figure 3-2. I/O Connector Physical Pin Locations

## Connector Pinout

### J1 — Analog Input Connector

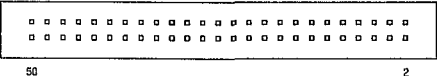
| J1                                                                                 |                                        |               |
|------------------------------------------------------------------------------------|----------------------------------------|---------------|
| 49                                                                                 |                                        | 1             |
|  |                                        |               |
| 50                                                                                 |                                        | 2             |
| J1 Pin                                                                             | Single Ended or<br>Pseudo-Differential | Differential  |
| 1                                                                                  | Channel 0                              | Channel 0+    |
| 2                                                                                  | Channel 8                              | Channel 0–    |
| 3                                                                                  | Analog Ground                          | Analog Ground |
| 4                                                                                  | Channel 9                              | Channel 1–    |
| 5                                                                                  | Channel 1                              | Channel 1+    |
| 6                                                                                  | Analog Ground                          | Analog Ground |
| 7                                                                                  | Channel 2                              | Channel 2+    |
| 8                                                                                  | Channel 10                             | Channel 2–    |
| 9                                                                                  | Analog Ground                          | Analog Ground |
| 10                                                                                 | Channel 11                             | Channel 3–    |
| 11                                                                                 | Channel 3                              | Channel 3+    |
| 12                                                                                 | Analog Ground                          | Analog Ground |
| 13                                                                                 | Channel 4                              | Channel 4+    |
| 14                                                                                 | Channel 12                             | Channel 4–    |
| 15                                                                                 | Analog Ground                          | Analog Ground |
| 16                                                                                 | Channel 13                             | Channel 5–    |
| 17                                                                                 | Channel 5                              | Channel 5+    |
| 18                                                                                 | Analog Ground                          | Analog Ground |
| 19                                                                                 | Channel 6                              | Channel 6+    |
| 20                                                                                 | Channel 14                             | Channel 6–    |
| 21                                                                                 | Analog Ground                          | Analog Ground |
| 22                                                                                 | Channel 15                             | Channel 7–    |
| 23                                                                                 | Channel 7                              | Channel 7+    |
| 24                                                                                 | Analog Ground                          | Analog Ground |
| 25                                                                                 | Channel 16                             | Channel 8+    |
| 26                                                                                 | Channel 24                             | Channel 8–    |
| 27                                                                                 | Analog Ground                          | Analog Ground |
| 28                                                                                 | Channel 25                             | Channel 9–    |
| 29                                                                                 | Channel 17                             | Channel 9+    |
| 30                                                                                 | Analog Ground                          | Analog Ground |
| 31                                                                                 | Channel 18                             | Channel 10+   |
| 32                                                                                 | Channel 26                             | Channel 10–   |
| 33                                                                                 | Analog Ground                          | Analog Ground |
| 34                                                                                 | Channel 27                             | Channel 11–   |
| 35                                                                                 | Channel 19                             | Channel 11+   |
| 36                                                                                 | Analog Ground                          | Analog Ground |
| 37                                                                                 | Channel 20                             | Channel 12+   |
| 38                                                                                 | Channel 28                             | Channel 12–   |
| 39                                                                                 | Analog Ground                          | Analog Ground |
| 40                                                                                 | Channel 29                             | Channel 13–   |
| 41                                                                                 | Channel 21                             | Channel 13+   |
| 42                                                                                 | Analog Ground                          | Analog Ground |
| 43                                                                                 | Channel 22                             | Channel 14+   |
| 44                                                                                 | Channel 30                             | Channel 14–   |
| 45                                                                                 | Analog Ground                          | Analog Ground |
| 46                                                                                 | Channel 31                             | Channel 15–   |
| 47                                                                                 | Channel 23                             | Channel 15+   |
| 48                                                                                 | Analog Ground                          | Analog Ground |
| 49                                                                                 | PD                                     | N/C           |
| 50                                                                                 | Analog Ground                          | Analog Ground |

Figure 3-3. J1 – Analog Input Connector Pinout

**Channel 0 to 31.** Analog voltages are applied to these inputs for A/D conversion. In single-ended configuration, these inputs are referenced to Analog Ground. In pseudo-differential configuration, these inputs are considered “high side” and are referenced to PD.

**Channel 0+ to 15+.** Differential “high side” voltages are applied to these inputs for A/D conversion. Each input is referenced to a corresponding differential “low side” input.

**Channel 0– to 15–.** Differential “low side” voltages are applied to these inputs for A/D conversion. Each input is referenced to a corresponding differential “high side” input.

**PD — Pseudo Differential “Low Side”.** All “low side” pseudo-differential analog voltages are connected together and brought to this pin for differential reference.

**Analog Ground.** This signal is the on-board analog ground. In single-ended mode, all analog inputs are referenced to this signal. The use of multiple ground connections is recommended to maintain a high degree of signal integrity. In differential mode, a return path for the input bias currents of the on-board instrumentation amplifiers must be connected to this pin. This is accomplished by wiring a 10K to 100K W resistor between analog ground and the “low side” of each differential signal source. These resistors should be located in close physical proximity to the signal sources. The cable shield can be used for this purpose.

**N/C — No Connection.** This signal is not connected to on-board circuitry.

# Registers

---

## Introduction

This section includes information about registers, control and status bits, and data formats. It focuses primarily on the individual registers, the bits contained within them, and their functional descriptions.

## Register Mapping

The VL-1260 occupies eight consecutive addresses in the I/O or memory map. The VL-1260 uses three of these addresses as control, data, and status registers; the remaining five are inaccessible.

The locations of the eight ports are determined by the board address, which is jumper selectable. For compatibility with Analog Devices RTI-1260 boards, VersaLogic ships the VL-1260 jumpered to memory address FF08H. However, most users configure the board using I/O mapping rather than memory mapping. For simplicity, this manual uses the as-shipped memory mapped addresses when referring to register locations. If you have reconfigured the card, you should substitute your own address for the FF0XH addresses indicated throughout this manual.

| Input Port | Output Port | Name                          | Port Address      | As Shipped Address | Page |
|------------|-------------|-------------------------------|-------------------|--------------------|------|
| —          | —           | Not Used                      | Board Address + 7 | FF0FH              | —    |
| —          | —           | Not Used                      | Board Address + 6 | FF0EH              | —    |
| IDHIGH     | —           | Input Data High Register      | Board Address + 5 | FF0DH              | 4-3  |
| IDLOW      | —           | Input Data Low Register       | Board Address + 4 | FF0CH              | 4-3  |
| —          | SELECT      | Input Channel Select Register | Board Address + 3 | FF0BH              | 4-2  |
| —          | —           | Not Used                      | Board Address + 2 | FF0AH              | —    |
| —          | —           | Not Used                      | Board Address + 1 | FF09H              | —    |
| —          | —           | Not Used                      | Board Address + 0 | FF08H              | —    |

*Figure 4-1. I/O Port Addresses*

## Analog Input Registers

### Input Channel Select Register

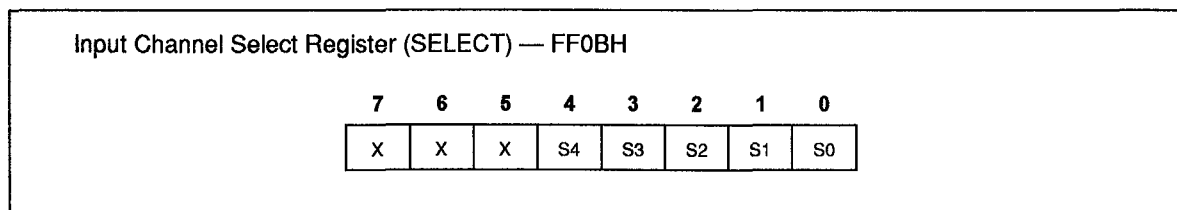


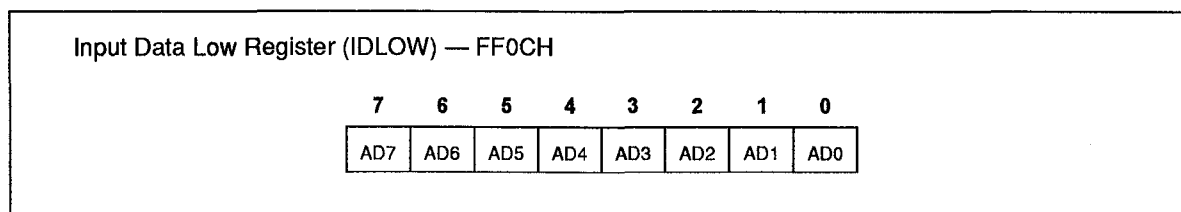
Figure 4-2. Input Channel Select Register

The Channel Select register is a write register used to select the input channel number to be read. Writing a channel number to this register initiates a conversion cycle. Do not write to this register if bit D7 (BUSY) of IDHIGH = 1.

**X — Not Used.** These bits have no function in the VL-1260. It does not matter what value is written to them.

**S4, S3, S2, S1, S0 — Channel Address.** These bits select the analog channel to use for A/D conversion.

| S4 | S3 | S2 | S1 | S0 | Selected Channel |
|----|----|----|----|----|------------------|
| 0  | 0  | 0  | 0  | 0  | Channel 0        |
| 0  | 0  | 0  | 0  | 1  | Channel 1        |
| 0  | 0  | 0  | 1  | 0  | Channel 2        |
| 0  | 0  | 0  | 1  | 1  | Channel 3        |
| 0  | 0  | 1  | 0  | 0  | Channel 4        |
| 0  | 0  | 1  | 0  | 1  | Channel 5        |
| 0  | 0  | 1  | 1  | 0  | Channel 6        |
| 0  | 0  | 1  | 1  | 1  | Channel 7        |
| 0  | 1  | 0  | 0  | 0  | Channel 8        |
| 0  | 1  | 0  | 0  | 1  | Channel 9        |
| 0  | 1  | 0  | 1  | 0  | Channel 10       |
| 0  | 1  | 0  | 1  | 1  | Channel 11       |
| 0  | 1  | 1  | 0  | 0  | Channel 12       |
| 0  | 1  | 1  | 0  | 1  | Channel 13       |
| 0  | 1  | 1  | 1  | 0  | Channel 14       |
| 0  | 1  | 1  | 1  | 1  | Channel 15       |
| 0  | 0  | 0  | 0  | 0  | Channel 16       |
| 0  | 0  | 0  | 0  | 1  | Channel 17       |
| 0  | 0  | 0  | 1  | 0  | Channel 18       |
| 0  | 0  | 0  | 1  | 1  | Channel 19       |
| 0  | 0  | 1  | 0  | 0  | Channel 20       |
| 0  | 0  | 1  | 0  | 1  | Channel 21       |
| 0  | 0  | 1  | 1  | 0  | Channel 22       |
| 0  | 0  | 1  | 1  | 1  | Channel 23       |
| 0  | 1  | 0  | 0  | 0  | Channel 24       |
| 0  | 1  | 0  | 0  | 1  | Channel 25       |
| 0  | 1  | 0  | 1  | 0  | Channel 26       |
| 0  | 1  | 0  | 1  | 1  | Channel 27       |
| 0  | 1  | 1  | 0  | 0  | Channel 28       |
| 0  | 1  | 1  | 0  | 1  | Channel 29       |
| 0  | 1  | 1  | 1  | 0  | Channel 30       |
| 0  | 1  | 1  | 1  | 1  | Channel 31       |

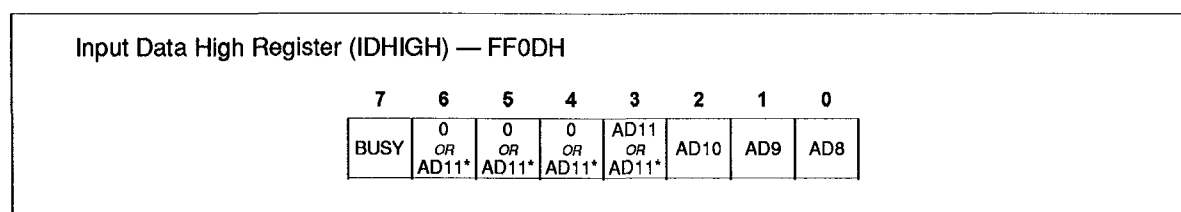
**Input Data Low Register***Figure 4-4. Input Data Low Register*

The Input Data Low register is a read register containing the lower 8 bits of data from the A/D conversion results. It is used in conjunction with the Input Data High register to read the complete 12-bit A/D data word.

The Input Data Low register should always be read after reading the Input Data High register, never first.

See the Polled Mode Analog Input section on page 5-1 for further information on accessing this register.

**AD7-AD0 — A/D Data (Least Significant Bits).** These bits contain data bits D7 through D0 of the A/D conversion results. See the Input Data Representation section for a discussion of input data formats.

**Input Data High Register***Figure 4-3. Input Data High Register*

The Input Data High register is a read register containing the conversion busy bit and the upper order bits of data from the A/D conversion results. It is used in conjunction with the Input Data Low register to read the complete 12-bit A/D data word.

The Input Data High register should always be read before reading the Input Data Low register.

See the Polled Mode Analog Input section on page 5-1 for further information on accessing this register.

**BUSY — Busy.** This bit is set to “1” when an A/D conversion is currently in progress, and automatically resets to “0” when the A/D conversion is complete. Use this bit to determine when the analog input data is valid.

**AD11-AD8 — A/D Data (Most Significant Bits).** These bits contain data bits D11 through D8 of the A/D conversion results. In binary formats, AD11 is true reading with the upper bits equal to 0. In two's complement format, AD11\* is output as indicated. See the Input Data Representation section below for a discussion of input data formats.

## Input Data Representation

The format of the data read from the board varies depending on the input range and the data format that is selected. Each of the data formats is discussed below.

### Input Binary Format (12-Bit Resolution)

Binary format is used only with the unipolar 0 to +10V input range. 12-bit binary format divides the full 10 Volt analog input range into 4096 steps of 2.44 mV each. The code 0000H is associated with an analog input voltage of 0 Volts (ground). The largest code (0FFFH) describes the highest voltage, i.e., +9.9976 Volts. All codes are considered positive. The upper four bits of the Data High register are all zeros.

The formulas for calculating analog or binary digital values are given by:

$$Digital = \left\lceil \frac{Analog}{Step} \right\rceil \qquad Analog = Step \times Digital$$

Where:

|         |   |                     |
|---------|---|---------------------|
| Analog  | = | Applied voltage     |
| Digital | = | A/D Conversion Data |
| Step    | = | 0.00244140          |

Sample values are shown in the table below:

| Input Voltage | Data (Hex) | Data (Decimal) | Comment             |
|---------------|------------|----------------|---------------------|
| +10.0000      | —          | —              | Out of range        |
| +9.9976       | 0FFF       | 4095           | Maximum voltage     |
| +5.0000       | 0800       | 2048           | Half scale          |
| +2.5000       | 0400       | 1024           | Quarter scale       |
| +1.2500       | 0200       | 512            | Eighth scale        |
| +0.00244      | 0001       | 1              | 1 LSB               |
| 0.0000        | 0000       | 0              | Zero (ground input) |

*Figure 4-2. Binary Data Format (12-Bit Resolution)*

**Input Offset Binary Format (12-Bit Resolution)**

Offset binary format is used with the bipolar  $\pm 10\text{V}$  input ranges. 12-bit offset binary format divides the full bipolar analog input range into 4096 steps. The code 0000H is associated with the most negative voltage, i.e.  $-10\text{ Volts}$ . The largest code (0FFFH) describes the most positive voltage, i.e.,  $+9.9951\text{ Volts}$ . An analog input of  $0\text{ Volts}$  (ground) will read as 0800H. The upper four bits of the Data High register are all zeros.

The formulas for calculating analog or offset binary digital values are given by:

$$Digital = \left\lceil \frac{Analog + Span}{Step} \right\rceil \qquad Analog = Step \times (Digital - 1) - Span$$

Where:

|         |   |                                      |
|---------|---|--------------------------------------|
| Analog  | = | Applied voltage                      |
| Digital | = | A/D Conversion Data                  |
| Span    | = | 9.99511718 ( $\pm 10\text{V}$ Range) |
| Step    | = | 0.00488281 ( $\pm 10\text{V}$ Range) |

Sample values are shown in the table below:

| $\pm 10\text{V}$ Input Voltage | Data (Hex) | Data (Decimal) | Comment                  |
|--------------------------------|------------|----------------|--------------------------|
| +10.0000                       | ---        | ---            | Out of range             |
| +9.9951                        | 0FFF       | 4095           | Maximum positive voltage |
| +5.0000                        | 0C00       | 3072           | Positive half scale      |
| +2.5000                        | 0A00       | 2560           | Positive quarter scale   |
| +0.00488                       | 0801       | 2049           | Positive 1 LSB           |
| 0.0000                         | 0800       | 2048           | Zero (ground input)      |
| -0.00488                       | 07FF       | 2047           | Negative 1 LSB           |
| -2.5000                        | 0600       | 1536           | Negative quarter scale   |
| -5.0000                        | 0400       | 1024           | Negative half scale      |
| -10.0000                       | 0000       | 0              | Maximum negative voltage |

*Figure 4-3. Offset Binary Data Format (12-Bit Resolution)*

**Input Two's Complement Format (12-Bit Resolution)**

Two's complement format is used with the  $\pm 10\text{V}$  input ranges. 12-bit two's complement format, like 12-bit offset binary format, divides the full bipolar analog input range into 4096 steps. The code 0000H, however, is associated with an analog input voltage of 0 Volts (ground). Positive analog input voltages are represented by positive digital numbers, whereas negative analog input voltages are represented by negative digital numbers (encoded in a 12-bit field), i.e.,  $-1 = 0\text{FFFH}$ . Two's complement format is the most common format for expressing bipolar analogs.

The formulas for calculating analog or two's complement digital values are given by:

$$\text{Digital} = \left\lceil \frac{\text{Analog}}{\text{Step}} \right\rceil \qquad \text{Analog} = \text{Step} \times \text{Digital}$$

Where:

|         |   |                                      |
|---------|---|--------------------------------------|
| Analog  | = | Applied voltage                      |
| Digital | = | A/D Conversion Data                  |
| Step    | = | 0.00488281 ( $\pm 10\text{V}$ Range) |

Sample values are shown in the table below:

| $\pm 10\text{V}$ Input Voltage | Data (Hex) | Data (Decimal) | Comment                  |
|--------------------------------|------------|----------------|--------------------------|
| +10.0000                       | —          | —              | Out of range             |
| +9.9951                        | 7FF        | 2047           | Maximum positive voltage |
| +5.0000                        | 400        | 1024           | Positive half scale      |
| +2.5000                        | 200        | 512            | Positive quarter scale   |
| +0.01953                       | 001        | 1              | Positive 1 LSB           |
| 0.0000                         | 000        | 0              | Zero (ground input)      |
| -0.01953                       | FFF        | -1             | Negative 1 LSB           |
| -2.5000                        | E00        | -512           | Negative quarter scale   |
| -5.0000                        | C00        | -1024          | Negative half scale      |
| -10.0000                       | 800        | -2048          | Maximum negative voltage |

*Figure 4-4. Two's Complement Data Format (12-Bit Resolution)*

## Operation

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This section describes how to operate the VL-1260. A code example written in 80x86 assembly language is included in the next section.

### Polled Mode Analog Input

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A polled mode of operation is used on the VL-1260. It is the responsibility of the CPU to start each new A/D conversion as desired, and to read the digital results upon completion.

#### Polled Mode Steps

- Channel selection and Trigger
- Wait until done and keep High Data
- Read Low Data
- Sign extend if needed

#### Channel selection and Trigger

Output the desired channel number to the Channel Select register (see page 4-2). This automatically triggers the A/D circuits to begin converting. The conversion will complete in about 40  $\mu$ S. If desired, the CPU is free to execute unrelated code, and then return to the next step in the sequence.

#### Wait until done and keep High Data

Read the Input Data High register until bit D7 (BUSY) = 0. This is best accomplished by reading the contents of this register directly into the CPU's accumulator or into an 8-bit variable. The Input Data High register contains the conversion status bit and some of the high-order data bits of the A/D results. Bit D7 (BUSY) is set to 1 when the conversion is triggered in the previous step. When BUSY = 0, the A/D conversion has completed, signaling that both Input Data High and Input Data Low registers contain valid data. Since the CPU has been reading the Input Data High register in order to test the BUSY bit, the upper-order bits of the A/D results have already been fetched from the VL-1260. It is not necessary to re-read the Input Data High register.

#### Read the Low Data

Read the Input Data Low register directly into another CPU register. See page 4-3.

#### Sign Extension (Optional)

In two's complement mode, if you're handling the A/D data using 16-bit variables or CPU registers, it might be desirable to "sign extend" the input value into 16 bits prior to storage or mathematical manipulation. The sign bit is extended in hardware except for the busy bit location. The process of sign extension fills the busy bit with a "1" or "0" as appropriate. The software examples show how this is done with shift instructions.



# Software Example

This section shows a software example written in Microsoft MASM 5.0 assembly language to assist you in constructing your own software routines.

## Polled Mode Analog Input

The following example reads channel 0 into the AX register. It is assumed that the board is addressed at I/O location 0300H.

The key program sections are:

|             |                                                                      |
|-------------|----------------------------------------------------------------------|
| <b>READ</b> | Reads A/D channel 0 into AX register.                                |
| <b>BUSY</b> | Location where program loops waiting for A/D conversion to complete. |

```

                                ;VL-1225/6 REGISTER ADDRESSES
= 0303          select equ    00303h    ;Input Channel Select Register
= 0304          idlow  equ    00304h    ;Input Data Low Register
= 0305          idhigh equ    00305h    ;Input Data High Register

0000          code    segment para public 'CODE'
               assume  cs:code

0000          read:                                ;READ CHANNEL 0 INTO AX REGISTER

0000 BA 0303          mov     dx,select ;Select channel 0 and Trigger
0003 B0 00          mov     al,00h
0005 EE          out      dx,al

0006 BA 0305          mov     dx,idhigh ;Read BUSY bit and High Data
0009 EC          busy:   in     al,dx
000A A8 80          test    al,10000000b
000C 75 FB          jnz     busy      ;Loop if BUSY = 1

000E 8A E0          mov     ah,al      ;Mask off unused high-order bits
0010 80 E4 03        and     ah,0fh

0013 BA 0304          mov     dx,idlow  ;Read Data Low register second
0016 EC          in     al,dx

0017          signex:                                ;Sign extend to fill 16-bit register
                                   ;The following 3 instructions are
                                   ;optional. They are used in
                                   ;two's complement mode only.

0017 B1 01          mov     cl,1      ;Shift count
0019 D3 E0          sal     ax,cl     ;Shift AD10 or AD11 into bit position D7
001B D3 F8          sar     ax,cl     ;Shift it back, extending sign

001D          code    ends          read      ;AX register contains A/D data
               end

```



# Calibration

The VL-1260 is calibrated before shipment. However, it may be desirable to recalibrate the card after installation, and approximately once each year (depending on the accuracy requirements of the application).

## Required Equipment

- A voltmeter with resolution and accuracy to  $\frac{1}{2}$  LSB of the input range being used.
- A low noise voltage source adjustable over the input range.
- A small flat-blade screwdriver.

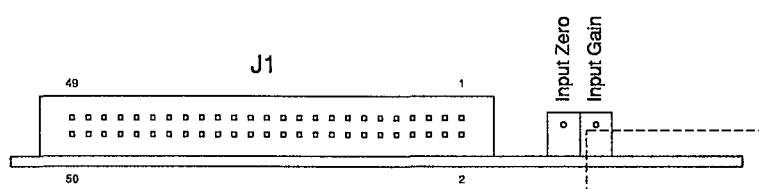


Figure 7-1. Adjustment Pot Locations

## Input Calibration

- Disconnect all inputs to the card and connect the voltage source to any channel.
- Using the voltmeter, adjust the voltage source according to table below:

| $\pm 10V$<br>Range | 0 to 10V<br>Range |
|--------------------|-------------------|
| -9.99756V          | +0.00122V         |

- Using a program to continuously read the input channel, adjust the “Input Zero” pot until the reading toggles between the two values shown in the table below.

| Binary | Offset<br>Binary | Two's<br>Complement |
|--------|------------------|---------------------|
| 0000H  | 0000H            | 0800H               |
| 0001H  | 0001H            | 0801H               |

- Using the voltmeter, adjust the voltage source according to the table below.

| $\pm 10V$<br>Range | 0 to 10V<br>Range |
|--------------------|-------------------|
| +9.99268V          | +9.99634V         |

- Using a program to continuously read the input channel, adjust the “Input Gain” pot until the reading toggles between the two values shown in the table below.

| Binary | Offset<br>Binary | Two's<br>Complement |
|--------|------------------|---------------------|
| 0FFFH  | 0FFFH            | 07FFH               |
| 0FFEH  | 0FFEH            | 07FEH               |



# Reference

## STD 80 Bus Pinout

| COMPONENT SIDE |           |      |                       | SOLDER SIDE |                  |      |                                  |
|----------------|-----------|------|-----------------------|-------------|------------------|------|----------------------------------|
| Pin            | Signal    | Flow | Description           | Pin         | Signal           | Flow | Description                      |
| P01            | +5VDC     | In   | Logic Power           | P02         | +5VDC            | In   | Logic Power                      |
| P03            | GND       | In   | Logic Ground          | P04         | GND              | In   | Logic Ground                     |
| P05            | VBAT      | —    | Battery Power         | P06         | DCPDN*           | —    | DC Power Down                    |
| P07            | A19/D3    | I/O  | Address/Data          | P08         | A23/D7           | I/O  | Address/Data                     |
| P09            | A18/D2    | I/O  | Address/Data          | P10         | A22/D6           | I/O  | Address/Data                     |
| P11            | A17/D1    | I/O  | Address/Data          | P12         | A21/D5           | I/O  | Address/Data                     |
| P13            | A16/D0    | I/O  | Address/Data          | P14         | A20/D4           | I/O  | Address/Data                     |
| P15            | A07       | In   | Address               | P16         | A15              | In   | Address                          |
| P17            | A06       | In   | Address               | P18         | A14              | In   | Address                          |
| P19            | A05       | In   | Address               | P20         | A13              | In   | Address                          |
| P21            | A04       | In   | Address               | P22         | A12              | In   | Address                          |
| P23            | A03       | In   | Address               | P24         | A11              | In   | Address                          |
| P25            | A02       | In   | Address               | P26         | A10              | In   | Address                          |
| P27            | A01       | In   | Address               | P28         | A09              | In   | Address                          |
| P29            | A00       | In   | Address               | P30         | A08              | In   | Address                          |
| P31            | WR*       | In   | Write Mem or I/O      | P32         | RD*              | In   | Read Mem or I/O                  |
| P33            | IORQ*     | In   | I/O Address Select    | P34         | MEMRQ*           | In   | Memory Address Select            |
| P35            | IOEXP     | In   | I/O Expansion         | P36         | BHE* (MEMEX)     | In   | Byte High Enable (Mem Expansion) |
| P37            | INTRQ1*   | —    | Interrupt Request 1   | P38         | ALE*             | —    | Address Latch Enable             |
| P39            | STATUS1*  | —    | CPU Status 1          | P40         | STATUS0*         | —    | CPU Status 0                     |
| P41            | BUSAK*    | —    | Bus Acknowledge       | P42         | BUSRQ*           | —    | Bus Request                      |
| P43            | INTAK*    | —    | Interrupt Acknowledge | P44         | INTRQ*           | —    | Interrupt Request                |
| P45            | WAITRQ*   | —    | Wait Request          | P46         | NMIRQ*           | —    | Non-maskable Interrupt Request   |
| P47            | SYSRESET* | In   | System Reset          | P48         | PBRESET*         | —    | Push-Button Reset                |
| P49            | CLOCK*    | —    | Clock                 | P50         | CNTRL* (INTRQ2*) | —    | Aux Timing                       |
| P51            | PCO       | Out  | Priority Chain Out    | P52         | PCI              | In   | Priority Chain In                |
| P53            | AUX GND   | —    | AUX Ground            | P54         | AUX GND          | —    | AUX Ground                       |
| P55            | AUX +V    | —    | AUX Positive (+12VDC) | P56         | AUX -V           | —    | AUX Negative (-12VDC)            |

\* Denotes an active low signal.

— Denotes signal not used on this board.

Figure 8-1. STD 80 Bus Pinout

## VL-1260 Parts Placement Diagram

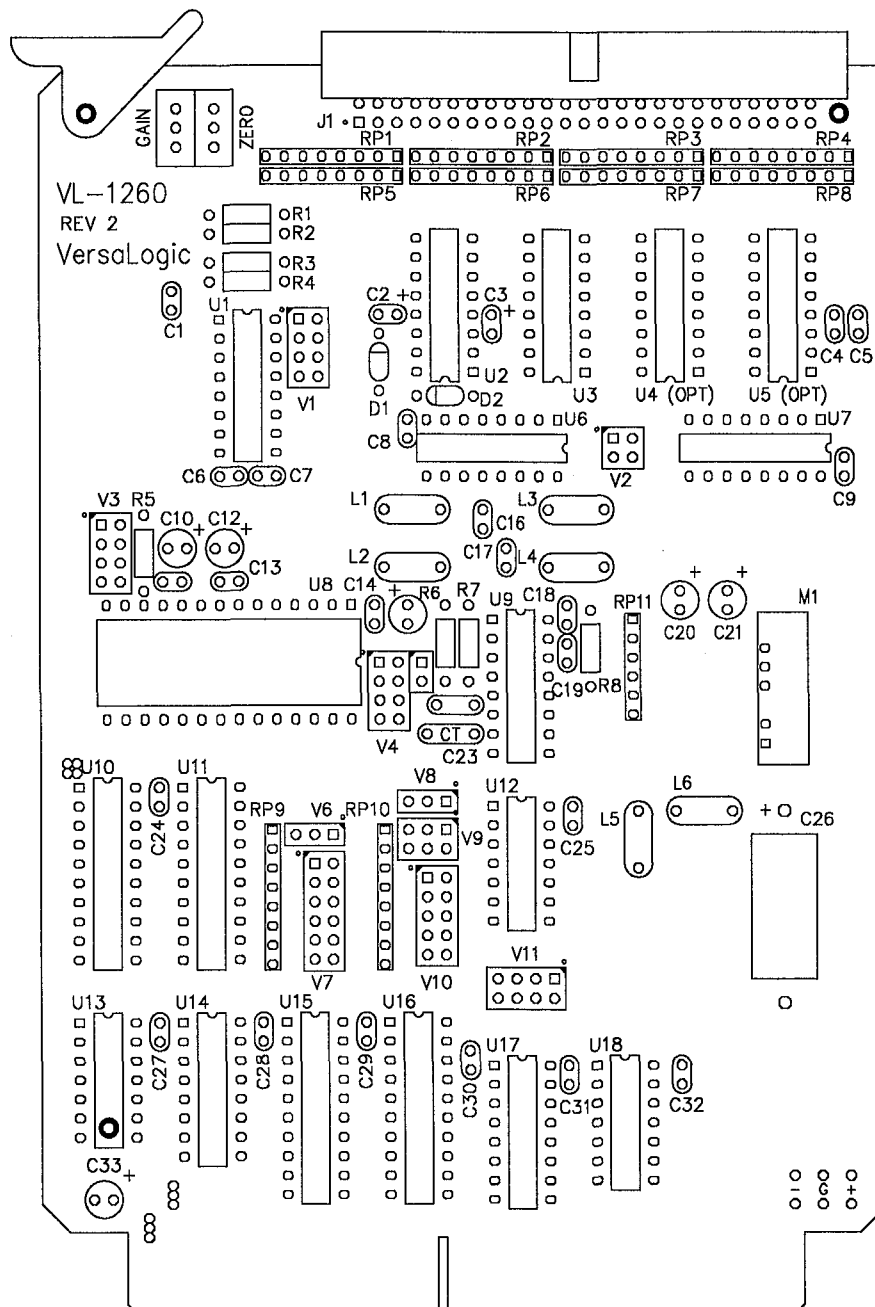
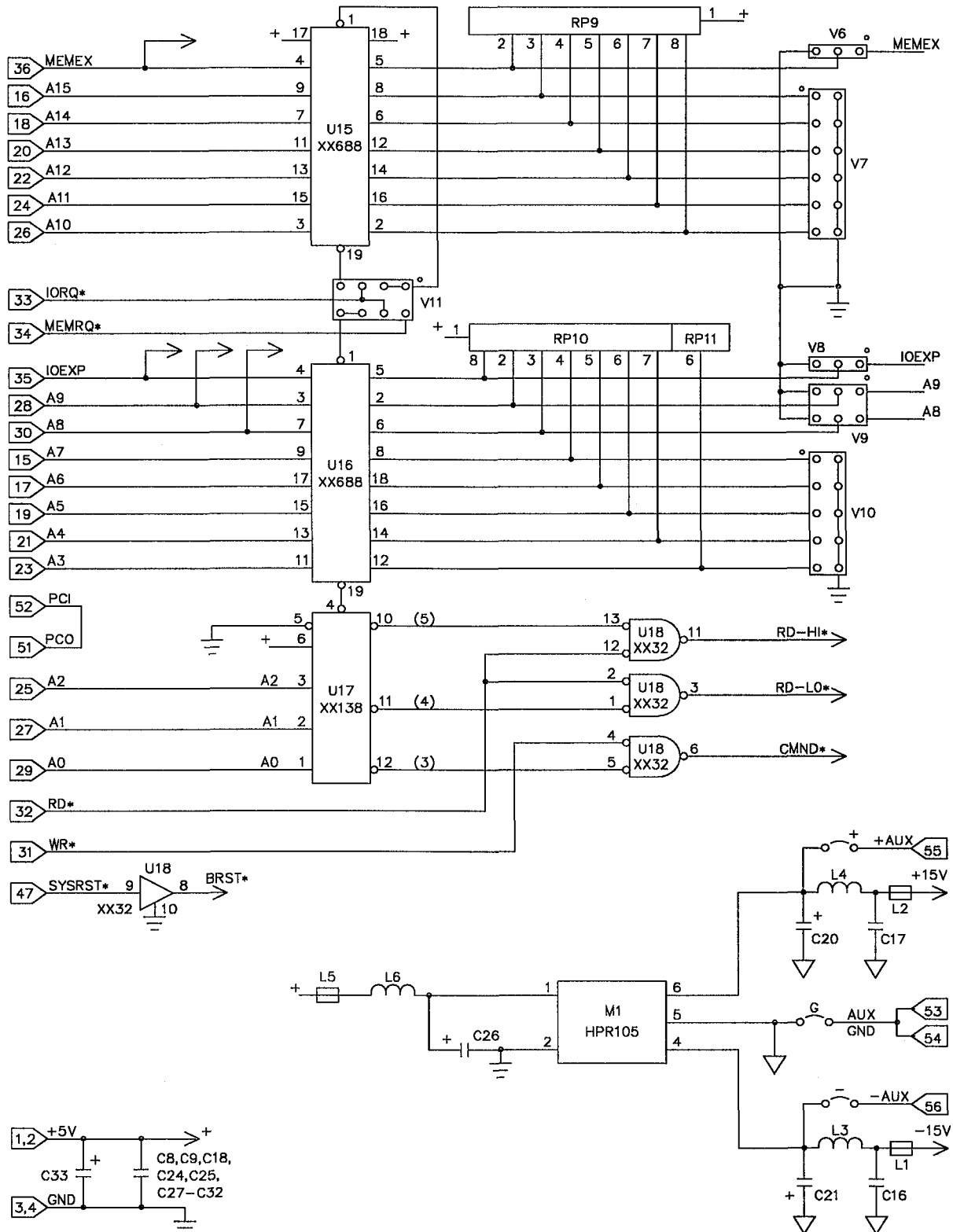


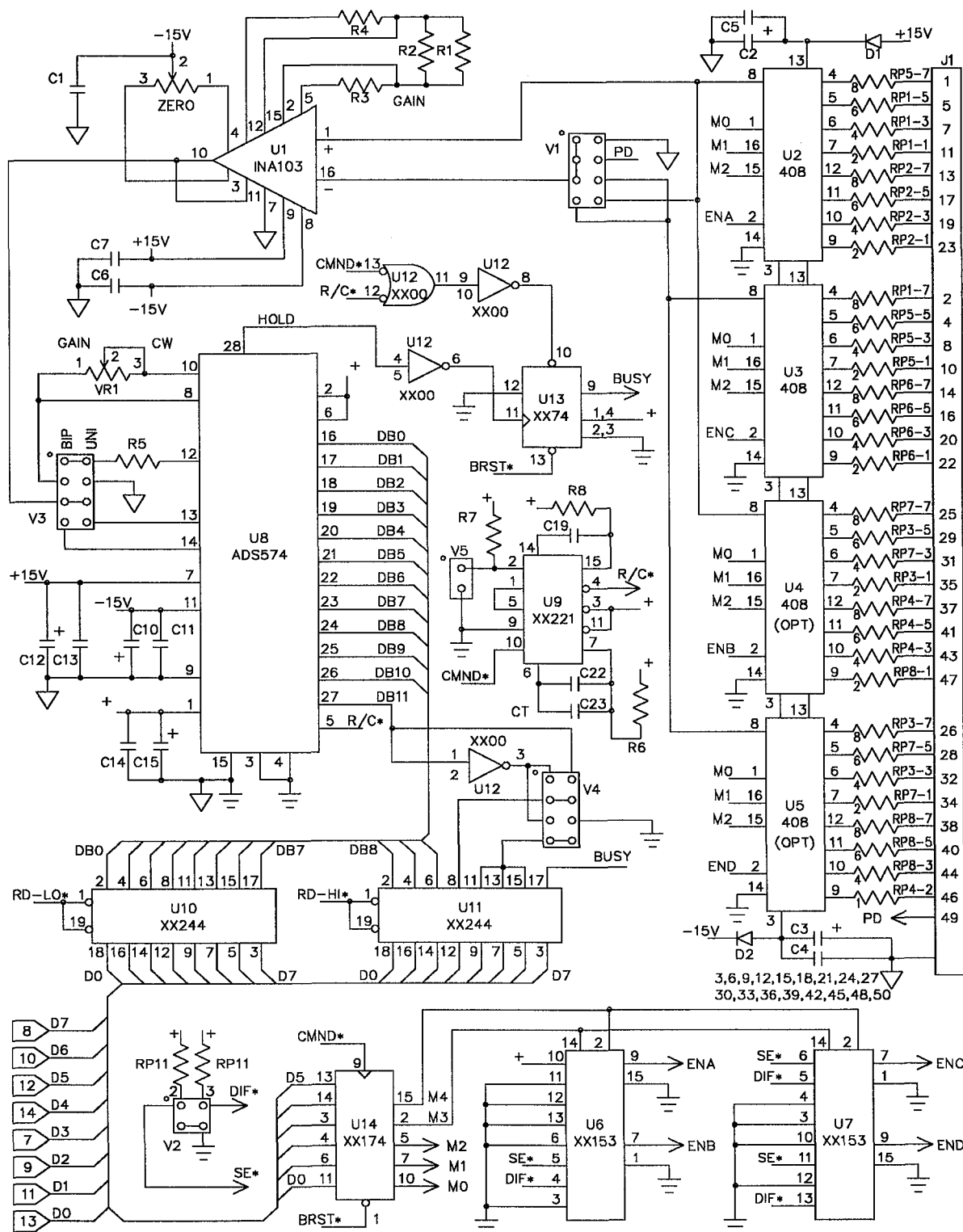
Figure 8-2. VL-1260 Parts Placement Diagram

# VL-1260 Schematic



8/19/92 REV2

# VL-1260 Schematic



8/19/92 REV2

# VL-1260 Parts List

Rev. 2.01

## Capacitors

|                                                                                     |                              |
|-------------------------------------------------------------------------------------|------------------------------|
| C2,C3,C10,C12                                                                       | 1 $\mu$ f, 35V tantalum      |
| C1,C4,C5,C6,C7,C8,C9,C11,C13,C14,<br>C16,C17,C18,C20,C21,C24,C25,C27-C32<br>C15,C33 | .1 $\mu$ f, Z5U              |
| C19                                                                                 | 10 $\mu$ f 16V tantalum      |
| C22                                                                                 | 270 pf NPO                   |
| C26                                                                                 | 2200 pf 50V                  |
|                                                                                     | 220 $\mu$ f 16V electrolytic |

## Inductors

|          |                    |
|----------|--------------------|
| L1,L2,L5 | Ferrite bead       |
| L3,L4    | 10 $\mu$ H, 250 mA |
| L6       | 47 $\mu$ H, 190 mA |

## Integrated Circuits

|         |          |
|---------|----------|
| U1      | INA103   |
| U2,U3   | DG408    |
| U6,U7   | 74LS153  |
| U8      | ADS574KP |
| U9      | 74LS221  |
| U10,U11 | 74LS244  |
| U12     | 74LS00   |
| U13     | 74LS74   |
| U14     | 74LS174  |
| U15,U16 | 74HCT688 |
| U17     | 74LS138  |
| U18     | 74LS32   |

## Resistors

|             |                                     |
|-------------|-------------------------------------|
| R3,R4,R6,R8 | 10K $\Omega$ , 1%, $\frac{1}{4}$ W  |
| R5          | 49.9 $\Omega$ , 1%, $\frac{1}{4}$ W |
| R7          | 4.7K $\Omega$ , 5%, $\frac{1}{4}$ W |
| GAIN        | 100 $\Omega$ pot                    |
| ZERO        | 100K $\Omega$ pot                   |
| RP1-RP8     | 1K $\Omega$ , 4 resistor SIP        |
| RP9,RP10    | 10K $\Omega$ , 7 resistor SIP       |
| RP11        | 10K $\Omega$ , 5 resistor SIP       |

## Semiconductors

|       |        |
|-------|--------|
| D1,D2 | IN4148 |
|-------|--------|

## Miscellaneous

|    |                                 |
|----|---------------------------------|
| M1 | +5V to $\pm$ 15V DC/DC (HPR105) |
|----|---------------------------------|

