1. GENERAL DESCRIPTION

The W6811 is a general-purpose single channel PCM CODEC with pin-selectable u-Law or A-Law companding. The device is compliant with the ITU G.712 specification. It operates off of separated analog (5V) and digital (3V) power supplies and is available in 24-pin SOG, and SSOP package options. Functions performed include digitization and reconstruction of voice signals, and band limiting and smoothing filters required for PCM systems. The filters are compliant with ITU G.712 specification. W6811 performance is specified over the industrial temperature range of –40°C to +85°C.

The W6811 includes an on-chip precision voltage reference and an additional power amplifier, capable of driving 300Ω loads differentially up to a level of 6.3V peak-to-peak. The analog section is fully differential, reducing noise and improving the power supply rejection ratio. The data transfer protocol supports both long-frame and short-frame synchronous communications for PCM applications, and IDL and GCI communications for ISDN applications. W6811 accepts seven master clock rates between 256 kHz and 4.096 MHz, and an on-chip pre-scaler automatically determines the division ratio for the required internal clock.

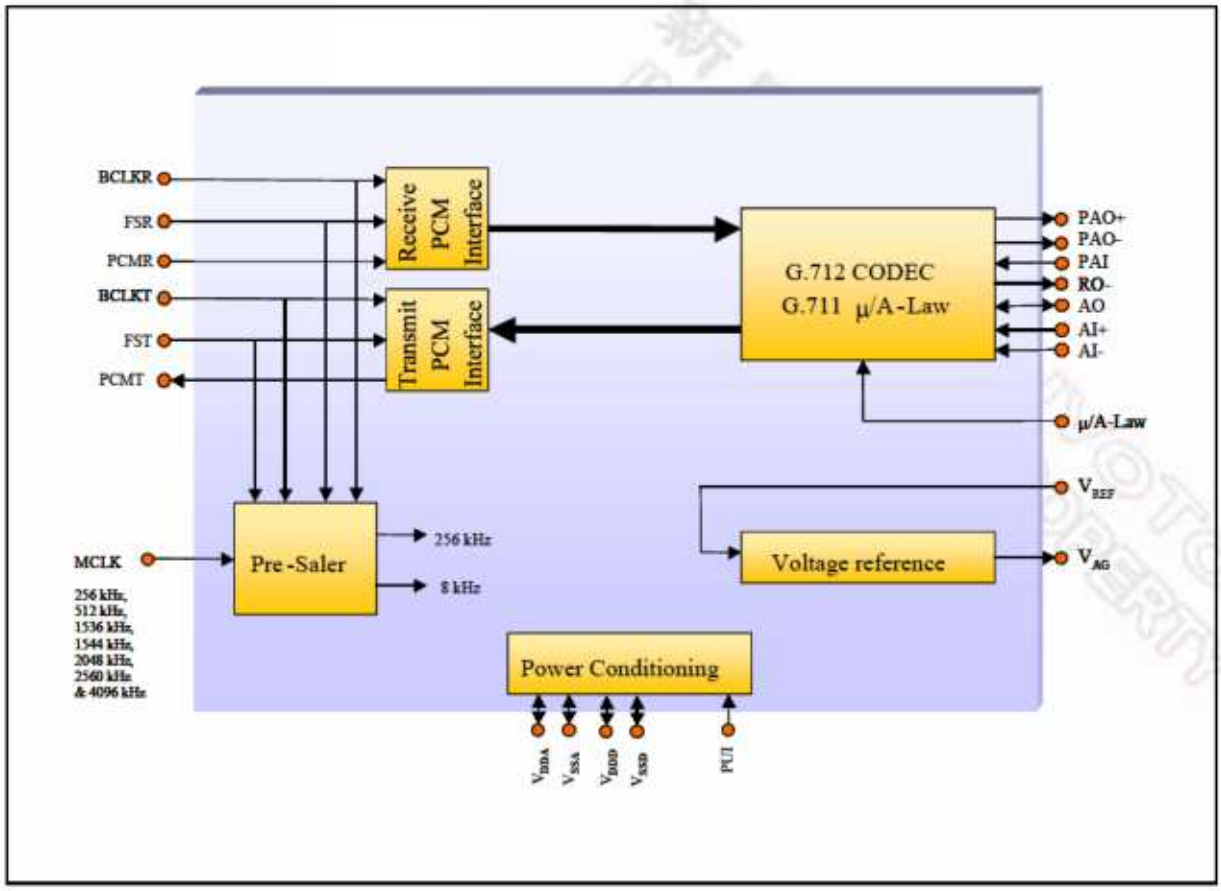
2. FEATURES

- Power supply:
  - Analog 4.5 – 5.5V
  - Digital 2.7 – 3.3V
- Typical power dissipation of 25 mW, power-down mode of 0.5 □ W
- Fully-differential analog circuit design
- On-chip precision reference of 1.575 V for a 0 dBm TLP at 600 Ω
- Push-pull power amplifiers with external gain adjustment with 300 Ω load capability
- Seven master clock rates of 256 kHz to 4.096 MHz
- Pin-selectable □-Law and A-Law companding (compliant with ITU G.711)
- CODEC A/D and D/A filtering compliant with ITU G.712
- Industrial temperature range (–40°C to +85°C)
- Package: 24-pin SOG, and SSOP
- Pb-Free / RoHS package options available

Applications

- Digital Telephone Systems
- Central Office Equipment (Gateways, Switches, Routers)
- PBX Systems (Gateways, Switches)
- PABX/SOHO Systems
- Local Loop card
- SOHO Routers
- VoIP Terminals
- Enterprise Phones
- ISDN Terminals
- Analog line cards
- Digital Voice Recorders

3. BLOCK DIAGRAM



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5. PIN CONFIGURATION



6. PIN DESCRIPTION

Pin Name	Pin No. SSOP SOP	V_{DD}	Functionality
V_{REF}	1	A	This pin is used to bypass the on-chip 2.5V voltage reference. It needs to be decoupled to V_{SSA} through a 0.1 μF ceramic decoupling capacitor. No external loads should be tied to this pin.
RO-	2	A	Inverting output of the receive smoothing filter. This pin can typically drive a 2 kΩ load to 1.575 volt peak referenced to the analog ground level.
PAI	3	A	This pin is the inverting input to the power amplifier. Its DC level is at the V_{AG} voltage.
PAO-	4	A	Inverting power amplifier output. This pin can drive a 300 Ω load to 1.575 volt peak referenced to the V_{AG} voltage level.
PAO+	5	A	Non-inverting power amplifier output. This pin can drive a 300 Ω load to 1.575 Volt peak referenced to the V_{AG} voltage level.
V_{DDA}	6	A	Analog power supply. This pin should be decoupled to V_{SSA} with a 0.1μF ceramic capacitor.
NC	7		Not Connected
V_{DDD}	8	D	Digital power supply. This pin should be decoupled to V_{SSD} with a 0.1μF ceramic capacitor. For correct operation, V_{DDD} value should always be lower than V_{DDA}.
FSR	9	D	8 kHz Frame Sync input for the PCM receive section. This pin also selects channel 0 or channel 1 in the GCI and IDL modes. It can also be connected to the FST pin when transmit and receive are synchronous operations.
PCMR	10	D	PCM input data receive pin. The data needs to be synchronous with the FSR and BCLKR pins.
BCLKR	11	D	PCM receive bit clock input pin. This pin also selects the interface mode. The GCI mode is selected when this pin is tied to V_{SSD}. The IDL mode is selected when this pin is tied to V_{DDD}. This pin can also be tied to the BCLKT when transmit and receive are synchronous operations.
PUI	12	D	Power up input signal. When this pin is tied to V_{DDD}, the part is powered up. When tied to V_{SSD}, the part is powered down.
MCLK	13	D	System master clock input. Possible input frequencies are 256 kHz, 512 kHz, 1536 kHz, 1544 kHz, 2048 kHz, 2560 kHz & 4096 kHz. For a better performance, it is recommended to have the MCLK signal synchronous and aligned to the FST signal. This is a requirement in the case of 256 and 512 kHz frequencies.
BCLKT	14	D	PCM transmit bit clock input pin.
PCMT	15	D	PCM output data transmit pin. The output data is synchronous with the FST and BCLKT pins.
FST	16	D	8 kHz transmit frame sync input. This pin synchronizes the transmit data bytes.

Pin Name	Pin No. SSOP SOP	V_{DD}*	Functionality
V_{SSD}	17	D	This is the digital supply ground. This pin should be connected to 0V.
NC	18		Not Connected
V_{SSA}	19	A	This is the analog supply ground. This pin should be connected to 0V.
µ/A-Law	20	D	Compander mode select pin. µ-Law companding is selected when this pin is tied to V_{DDD}. A-Law companding is selected when this pin is tied to V_{SSD}.
AO	21	A	Analog output of the first gain stage in the transmit path.
AI-	22	A	Inverting input of the first gain stage in the transmit path.
AI+	23	A	Non-inverting input of the first gain stage in the transmit path.
V_{AG}	24	A	Mid-Supply analog ground pin, which supplies a 2.5 Volt reference voltage for all-analog signal processing. This pin should be decoupled to V_{SSA} with a 0.01µF capacitor. This pin becomes high impedance when the chip is powered down.

* These columns represent whether the pin is driven by Analog ('A') or Digital ('D') power supply.

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7. FUNCTIONAL DESCRIPTION

W6811 is a single-rail, single channel PCM CODEC for voiceband applications. The CODEC complies with the specifications of the ITU-T G.712 recommendation. The CODEC also includes a complete μ-Law and A-Law compander. The μ-Law and A-Law companders are designed to comply with the specifications of the ITU-T G.711 recommendation.

The block diagram in section 3 shows the main components of the W6811. The chip consists of a PCM interface, which can process long and short frame sync formats, as well as GCI and IDL formats. The pre-scaler of the chip provides the internal clock signals and synchronizes the CODEC sample rate with the external frame sync frequency. The power conditioning block provides the internal power supply for the digital and the analog section, while the voltage reference block provides a precision analog ground voltage for the analog signal processing. The main CODEC block diagram is shown in section 3.

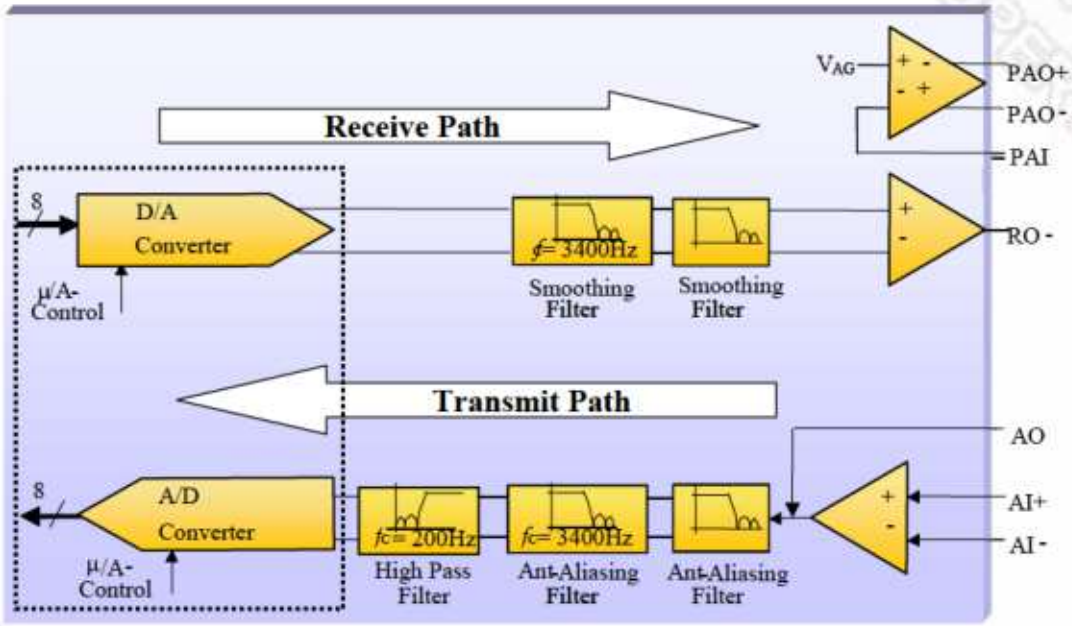


Figure 7.1 The W6811 Signal Path

7.1. TRANSMIT PATH

The A-to-D path of the CODEC contains an analog input amplifier with externally configurable gain setting (see application examples in section 11). The device has an input operational amplifier whose output is the input to the encoder section. If the input amplifier is not required for operation it can be powered down and bypassed. In that case a single ended input signal can be applied to the AO pin or the AI- pin. The AO pin becomes high input impedance when the input amplifier is powered down. The input amplifier can be powered down by connecting

the AI+ pin to V_{DDA} or V_{SSA}. The AO pin is selected as an input when AI+ is tied to V_{DDA} and the AI- pin is selected as an input when AI+ is tied to V_{SSA} (see Table 7.1).

AI+	Input Amplifier	Input
VDDA	Powered Down	AO
1.2 to VDDA-1.2	Powered Up	AI+, AI-
VSSA	Powered Down	AI-

Table 7.1 Input Amplifier Modes of operation

When the input amplifier is powered down, the input signal at AO or AI- needs to be referenced to the analog ground voltage V_{AG}. The output of the input amplifier is fed through a 3.4 kHz switched capacitor low pass filter to prevent aliasing of input signals above 4 kHz, due to the sampling at 8 kHz. The output of the 3.4 kHz low pass filter is filtered by a high pass filter with a 200 Hz cut-off frequency. The filters are designed according to the recommendations in the G.712 ITU-T specification. From the output of the high pass filter the signal is digitized. The signal is converted into a compressed 8-bit digital representation with either μ-Law or A-Law format. The μ-Law or A-Law format is pin-selectable through the μ/A-Law pin. The compression format can be selected according to Table 7.2.

μ/A-Law Pin	Format
VSSA	A-Law
VDDA	μ-Law

Table 7.2. Pin-selectable Compression Format

The digital 8-bit μ-Law or A-Law samples are fed to the PCM interface for serial transmission at the data rate supplied by the external bit clock BCLKT.

7.2. Receive Path

The 8-bit digital input samples for the D-to-A path are serially shifted in by the PCM interface and converted to parallel data bits. During every cycle of the frame sync FSR, the parallel data bits are fed through the pin-selectable μ-Law or A-Law expander and converted to analog samples. The mode of expansion is selected by the μ/A-Law pin as shown in Table 7.2. The analog samples are filtered by a low-pass smoothing filter with a 3.4 kHz cut-off frequency, according to the ITU-T G.712 specification. A sin(x)/x compensation is integrated with the low pass smoothing filter. The output of this filter is buffered to provide the receive output signal RO-. The RO- output can be externally connected to the PAI pin to provide a differential output with high driving capability at the PAO+ and PAO- pins. By using external resistors (see section 11 for examples), various gain settings of this output amplifier can be achieved. If the transmit power amplifier is not in use, it can be powered down by connecting PAI to V_{DDA}.

7.3. Power Management

7.3.1. Analog Supply

The power supply for the analog part of the W6811 needs to be 5V +/- 10%. This supply voltage is connected to the V_{DDA} pin. The V_{DDA} pin needs to be decoupled to ground through a 0.1 μF ceramic capacitor.

7.3.2. Digital Supply

The power supply for the digital part of the W6811 needs to be 3V +/- 10%. This supply voltage is connected to the V_{DDD} pin. The V_{DDD} pin needs to be decoupled to ground through a 0.1 μF ceramic capacitor.

7.3.3. Analog Ground Reference Bypass

The system has an internal precision voltage reference which generates the 2.5V mid-supply analog ground voltage. This voltage needs to be decoupled to V_{SSA} at the V_{REF} pin through a 0.1 μF ceramic capacitor.

7.3.4. Analog Ground Reference Voltage Output

The analog ground reference voltage is available for external reference at the V_{AG} pin. This voltage needs to be decoupled to V_{SSA} through a 0.01 μF ceramic capacitor. The analog ground reference voltage is generated from the voltage on the V_{REF} pin and is also used for the internal signal processing.

7.4. PCM Interface

The PCM interface is controlled by pins BCLKR, FSR, BCLKT & FST. The input data is received through the PCMR pin and the output data is transmitted through the PCMT pin. The modes of operation of the interface are shown in Table 7.3.

BCLKR	FSR	Interface Mode
64 kHz to 4.096 MHz	8 kHz	Long or Short Frame Sync
VSSD	VSSD	ISDN GCI with active channel B1
VSSD	VDDD	ISDN GCI with active channel B2
VDDD	VSSD	ISDN IDL with active channel B1
VDDD	VDDD	ISDN IDL with active channel B2

Table 7.3 PCM Interface mode selections

7.4.1. Long Frame Sync

The Long Frame Sync or Short Frame Sync interface mode can be selected by connecting the BCLKR or BCLKT pin to a 64 kHz to 4.096 MHz clock and connecting the FSR or FST pin to the 8 kHz frame sync. The device synchronizes the data word for the PCM interface and the CODEC sample rate on the positive edge of the Frame Sync signal. It recognizes a Long Frame Sync when the FST pin is held HIGH for two consecutive falling edges of the bit-clock at the BCLKT pin. The length of the Frame Sync pulse can vary from frame to frame, as long as the positive frame sync edge occurs every 125 μsec. During data transmission in the Long Frame Sync mode, the transmit data pin PCMT will become low impedance when the Frame Sync signal FST is HIGH or when the 8 bit data word is being transmitted. The transmit data pin PCMT will become high impedance when the Frame Sync signal FST becomes LOW while the data is transmitted or when half of the LSB is transmitted. The internal decision logic will determine whether the next frame sync is a long or a short frame sync, based on the previous frame sync pulse. To avoid bus collisions, the PCMT pin will be HIGH impedance for two frame sync cycles after every power down state. More detailed timing information can be found in the interface timing section.

7.4.2. Short Frame Sync

The W6811 operates in the Short Frame Sync Mode when the Frame Sync signal at pin FST is HIGH for one and only one falling edge of the bit-clock at the BCLKT pin. On the following rising edge of the bit-clock, the W6811 starts clocking out the data on the PCMT pin, which will also change from high to low impedance state. The data transmit pin PCMT will go back to the high impedance state halfway through the LSB. The Short Frame Sync operation of the W6811 is based on an 8-bit data word. When receiving data on the PCMR pin, the data is clocked in on the first falling edge after the falling edge that coincides with the Frame Sync signal. The internal decision logic will determine whether the next frame sync is a long or a short frame sync, based on the previous frame sync pulse. To avoid bus collisions, the PCMT pin will be high impedance for two frame sync cycles after every power down state. More detailed timing information can be found in the interface timing section.

7.4.3. General Circuit Interface (GCI)

The GCI interface mode is selected when the BCLKR pin is connected to V_{SSD} for two or more frame sync cycles. It can be used as a 2B+D timing interface in an ISDN application. The GCI interface consists of 4 pins : FSC (FST), DCL (BCLKT), Dout (PCMT) & Din (PCMR). The FSR pin selects channel B1 or B2 for transmit and receive. Data transitions occur on the positive edges of the data clock DCL. The Frame Sync positive edge is aligned with the positive edge of the data clock DCLK. The data rate is running half the speed of the bit-clock. The channels B1 and B2 are transmitted consecutively. Therefore, channel B1 is transmitted on the first 16 clock cycles of DCL and B2 is transmitted on the second 16 clock cycles of DCL. For more timing information, see the timing section.

7.4.4. Interchip Digital Link (IDL)

The IDL interface mode is selected when the BCLKR pin is connected to V_{DDD} for two or more frame sync cycles. It can be used as a 2B+D timing interface in an ISDN application. The IDL interface consists of 4 pins : IDL SYNC (FST), IDL CLK (BCLKT), IDL TX (PCMT) & IDL RX (PCMR). The FSR pin selects channel B1 or B2 for transmit and receive. The data for channel B1 is transmitted on the first positive edge of the IDL CLK after the IDL SYNC pulse. The IDL SYNC pulse is one IDL CLK cycle long. The data for channel B2 is transmitted on the eleventh positive edge of the IDL CLK after the IDL SYNC pulse. The data for channel B1 is received on the first negative edge of the IDL CLK after the IDL SYNC pulse. The data for channel B2 is received on the eleventh negative edge of the IDL CLK after the IDL SYNC pulse. The transmit signal pin IDL TX becomes high impedance when not used for data transmission and also in the time slot of the unused channels. For more timing information, see the timing section.

7.4.5. System Timing

The system can work at 256 kHz, 512 kHz, 1536 kHz, 1544 kHz, 2048 kHz, 2560 kHz & 4096 kHz master clock rates. The system clock is supplied through the master clock input MCLK and can be derived from the bit-clock if desired. An internal pre-scaler is used to generate a fixed 256 kHz and an 8 kHz sample clock for the internal CODEC. The pre-scaler measures the master clock frequency versus the Frame Sync frequency and sets the division ratio accordingly. If the Frame Sync is LOW for the entire frame sync period while the MCLK and BCLK pin clock signals are still present, the W6811 will enter the low power standby mode. Another way to power down is to set the PUI pin to LOW. When the system needs to be powered up again, the PUI pin needs to be set to HIGH and the Frame Sync pulse needs to be present. It will take two Frame Sync cycles before the pin PCMT will become low impedance.

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8. TIMING DIAGRAMS

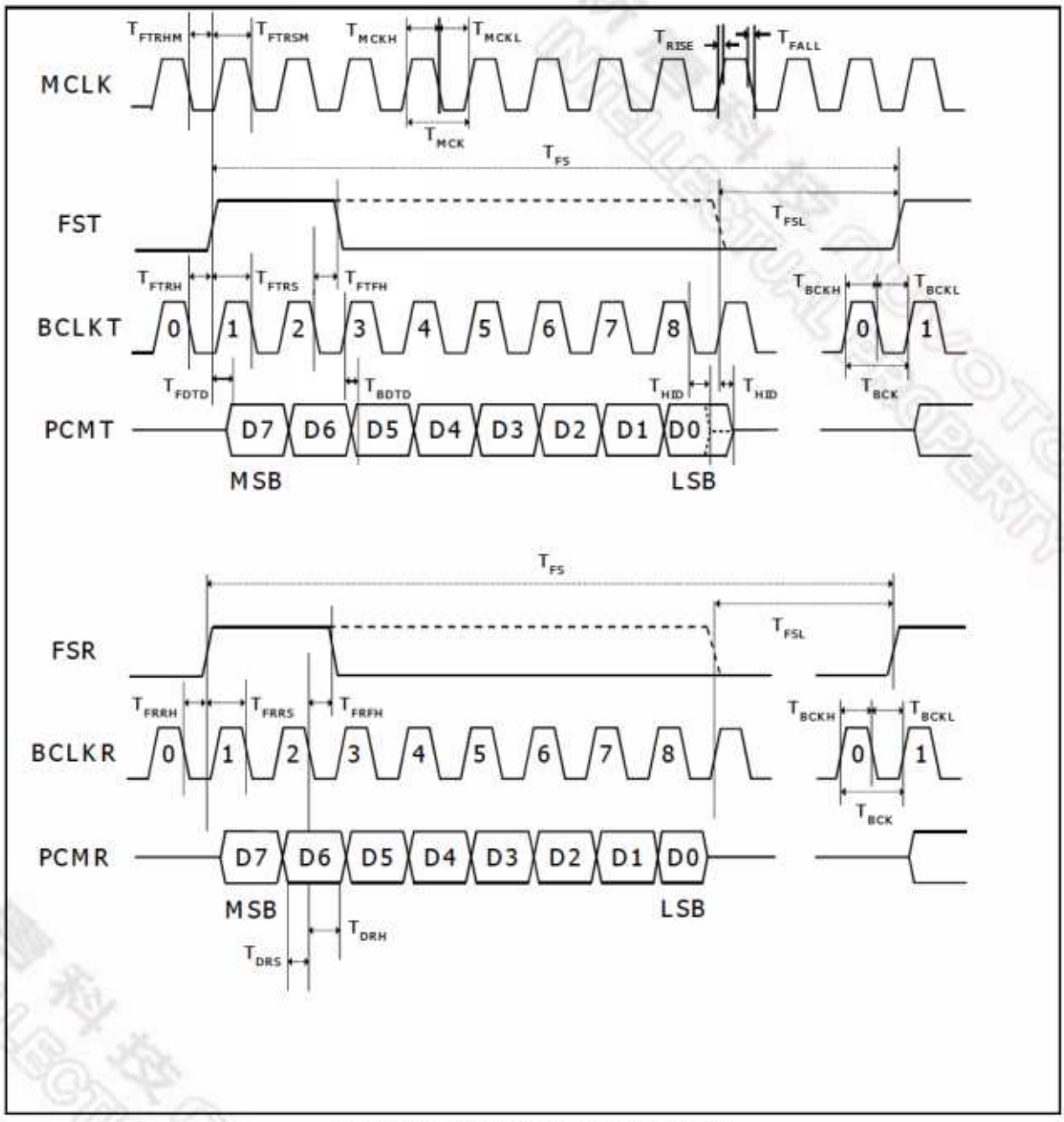


Figure 8.1 Long Frame Sync PCM Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
$1/T_{FS}$	FST, FSR Frequency	---	8	---	kHz
T_{FSL}	FST / FSR Minimum LOW Width [1]	T_{BCK}			sec
$1/T_{BCK}$	BCLKT, BCLKR Frequency	64	---	4096	kHz
T_{BCKH}	BCLKT, BCLKR HIGH Pulse Width	50	---	---	ns
T_{BCKL}	BCLKT, BCLKR LOW Pulse Width	50	---	---	ns
T_{FTRH}	BCLKT 0 Falling Edge to FST Rising Edge Hold Time	20	---	---	ns
T_{FTRS}	FST Rising Edge to BCLKT 1 Falling edge Setup Time	80	---	---	ns
T_{FTFH}	BCLKT 2 Falling Edge to FST Falling Edge Hold Time	50	---	---	ns
T_{FDTD}	FST Rising Edge to Valid PCMT Delay Time	---	---	60	ns
T_{BDTD}	BCLKT Rising Edge to Valid PCMT Delay Time	---	---	60	ns
T_{HID}	Delay Time from the Later of FST Falling Edge, or BCLKT 8 Falling Edge to PCMT Output High Impedance	10	---	60	ns
T_{FRRH}	BCLKR 0 Falling Edge to FSR Rising Edge Hold Time	20	---	---	ns
T_{FRRS}	FSR Rising Edge to BCLKR 1 Falling edge Setup Time	80	---	---	ns
T_{FRFH}	BCLKR 2 Falling Edge to FSR Falling Edge Hold Time	50	---	---	ns
T_{DRS}	Valid PCMR to BCLKR Falling Edge Setup Time	0	---	---	ns
T_{DRH}	PCMR Hold Time from BCLKR Falling Edge	50	---	---	ns

Table 8.1 Long Frame Sync PCM Timing Parameters

[1] T_{FSL} must be at least ≥ T_{BCK}

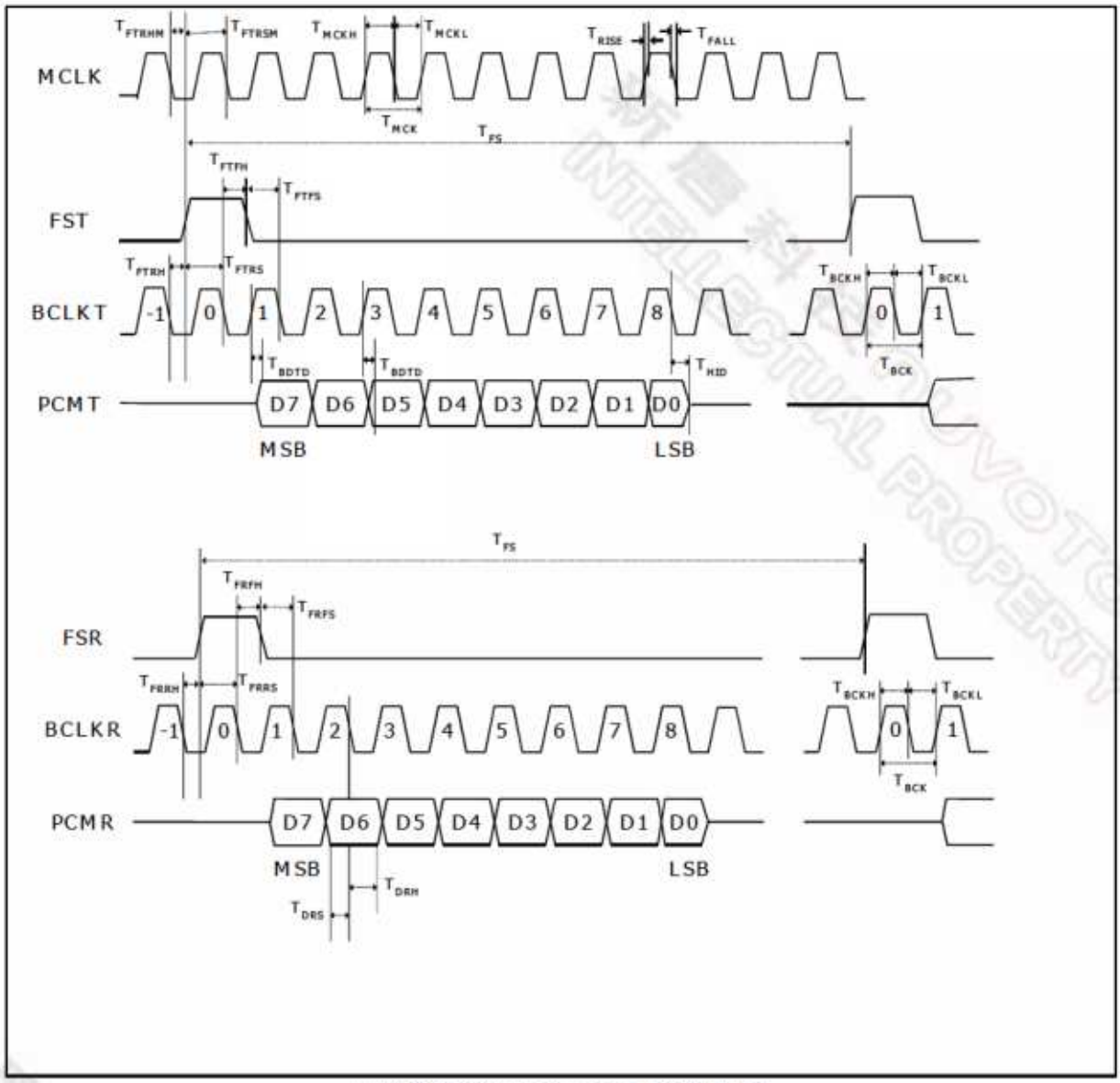


Figure 8.2 Short Frame Sync PCM Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
$1/T_{FS}$	FST, FSR Frequency	---	8	---	kHz
$1/T_{BCK}$	BCLKT, BCLKR Frequency	64	---	4096	kHz
T_{BCKH}	BCLKT, BCLKR HIGH Pulse Width	50	---	---	ns
T_{BCKL}	BCLKT, BCLKR LOW Pulse Width	50	---	---	ns
T_{FTRH}	BCLKT –1 Falling Edge to FST Rising Edge Hold Time	20	---	---	ns
T_{FTRS}	FST Rising Edge to BCLKT 0 Falling edge Setup Time	80	---	---	ns
T_{FTFH}	BCLKT 0 Falling Edge to FST Falling Edge Hold Time	50	---	---	ns
T_{FTFS}	FST Falling Edge to BCLKT 1 Falling Edge Setup Time	50	---	---	ns
T_{BDTD}	BCLKT Rising Edge to Valid PCMT Delay Time	10	---	60	ns
T_{HID}	Delay Time from BCLKT 8 Falling Edge to PCMT Output High Impedance	10	---	60	ns
T_{FRRH}	BCLKR –1 Falling Edge to FSR Rising Edge Hold Time	20	---	---	ns
T_{FRRS}	FSR Rising Edge to BCLKR 0 Falling edge Setup Time	80	---	---	ns
T_{FRFH}	BCLKR 0 Falling Edge to FSR Falling Edge Hold Time	50	---	---	ns
T_{FRFS}	FSR Falling Edge to BCLKR 1 Falling Edge Setup Time	50	---	---	ns
T_{DRS}	Valid PCMR to BCLKR Falling Edge Setup Time	0	---	---	ns
T_{DRH}	PCMR Hold Time from BCLKR Falling Edge	50	---	---	ns

Table 8.2 Short Frame Sync PCM Timing Parameters

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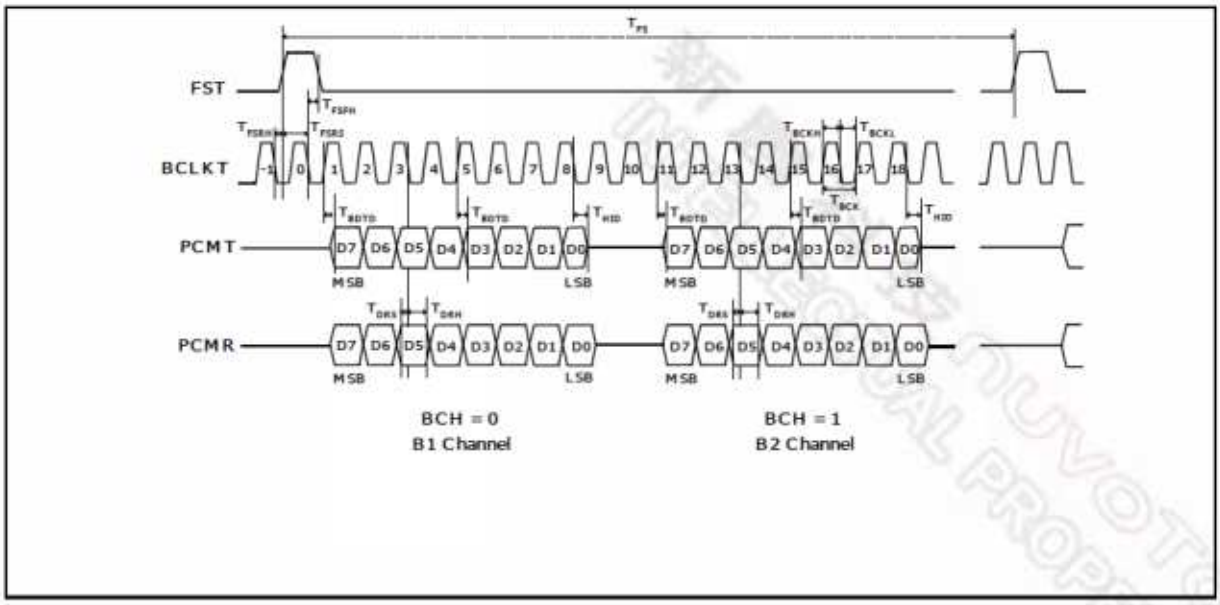


Figure 8.3 IDL PCM Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
$1/T_{FS}$	FST Frequency	---	8	---	kHz
$1/T_{BCK}$	BCLKT Frequency	256	---	4096	kHz
T_{BCKH}	BCLKT HIGH Pulse Width	50	---	---	ns
T_{BCKL}	BCLKT LOW Pulse Width	50	---	---	ns
T_{FSRH}	BCLKT –1 Falling Edge to FST Rising Edge Hold Time	20	---	---	ns
T_{FSRS}	FST Rising Edge to BCLKT 0 Falling edge Setup Time	60	---	---	ns
T_{FSFH}	BCLKT 0 Falling Edge to FST Falling Edge Hold Time	20	---	---	ns
T_{BDTD}	BCLKT Rising Edge to Valid PCMT Delay Time	10	---	60	ns
T_{HID}	Delay Time from the BCLKT 8 Falling Edge (B1 channel) or BCLKT 18 Falling Edge (B2 Channel) to PCMT Output High Impedance	10	---	50	ns
T_{DRS}	Valid PCMR to BCLKT Falling Edge Setup Time	20	---	---	ns
T_{DRH}	PCMR Hold Time from BCLKT Falling Edge	75	---	---	ns

Table 8.3 IDL PCM Timing Parameters

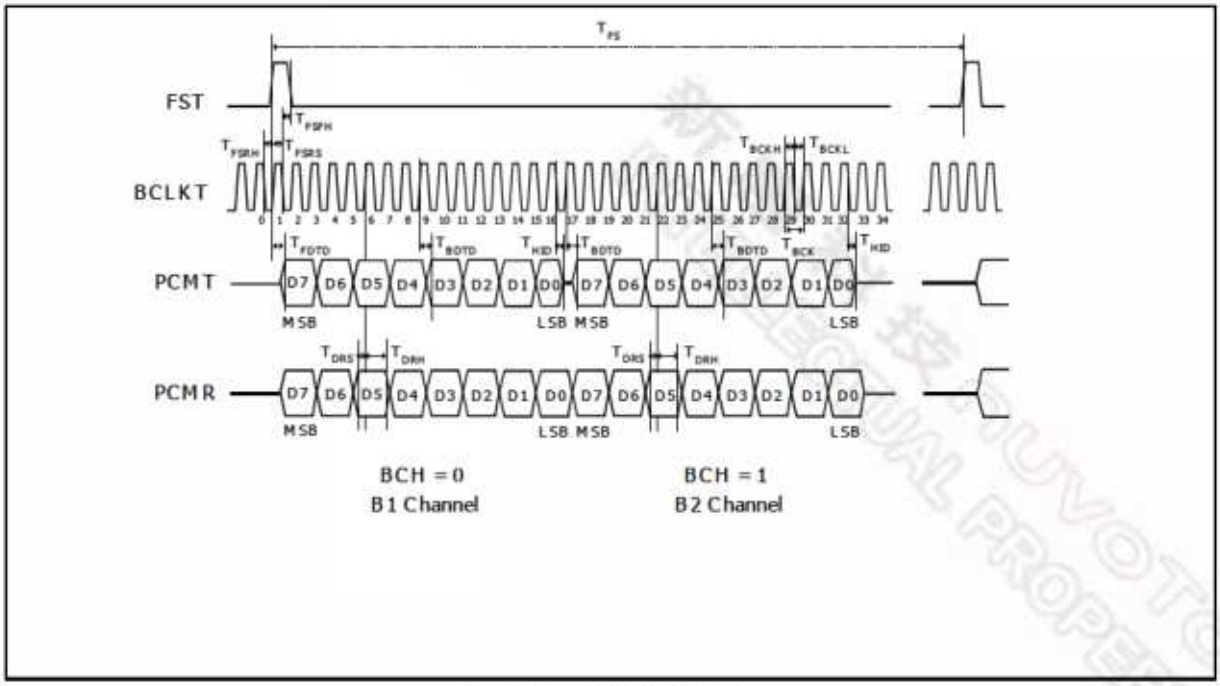


Figure 8.4 GCI PCM Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
$1/T_{FST}$	FST Frequency	---	8	---	kHz
$1/T_{BCK}$	BCLKT Frequency	512	---	6176	kHz
T_{BCKH}	BCLKT HIGH Pulse Width	50	---	---	ns
T_{BCKL}	BCLKT LOW Pulse Width	50	---	---	ns
T_{FSRH}	BCLKT 0 Falling Edge to FST Rising Edge Hold Time	20	---	---	ns
T_{FSRS}	FST Rising Edge to BCLKT 1 Falling edge Setup Time	60	---	---	ns
T_{FSFH}	BCLKT 1 Falling Edge to FST Falling Edge Hold Time	20	---	---	ns
T_{FDTD}	FST Rising Edge to Valid PCMT Delay Time	---	---	60	ns
T_{BDTD}	BCLKT Rising Edge to Valid PCMT Delay Time	---	---	60	ns
T_{HID}	Delay Time from the BCLKT 16 Falling Edge (B1 channel) or BCLKT 32 Falling Edge (B2 Channel) to PCMT Output High Impedance	10	---	50	ns
T_{DRS}	Valid PCMR to BCLKT Rising Edge Setup Time	20	---	---	ns
T_{DRH}	PCMR Hold Time from BCLKT Rising Edge	---	---	60	ns

Table 8.4 GCI PCM Timing Parameters

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
$1/T_{MCK}$	Master Clock Frequency	---	256 512 1536 1544 2048 2560 4096	---	kHz
T_{MCKH} / T_{MCK}	MCLK Duty Cycle for 256 kHz Operation	45%		55%	
T_{MCKH}	Minimum Pulse Width HIGH for MCLK(512 kHz or Higher)	50	---	---	ns
T_{MCKL}	Minimum Pulse Width LOW for MCLK (512 kHz or Higher)	50	---	---	ns
T_{FTRHM}	MCLK falling Edge to FST Rising Edge Hold Time	50	---	---	ns
T_{FTRSM}	FST Rising Edge to MCLK Falling edge Setup Time	50	---	---	ns
T_{RISE}	Rise Time for All Digital Signals	---	---	50	ns
T_{FALL}	Fall Time for All Digital Signals	---	---	50	ns

Table 8.5 General PCM Timing Parameters

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9. ABSOLUTE MAXIMUM RATINGS

9.1. Absolute Maximum Ratings

Condition	Value
Junction temperature	150^0C
Storage temperature range	-65^0C to $+150^0$C
Voltage Applied to any pin Analog Digital	(V_{SSA} - 0.3V) to (V_{DDA} + 0.3V) (V_{SSD} - 0.3V) to (V_{DDD} + 0.3V)
Voltage applied to any pin Analog (Input current limited to +/-20 mA) Digital	(V_{SSA} – 1.0V) to (V_{DDA} + 1.0V) (V_{SSD} – 1.0V) to (V_{DDD} + 1.0V)
V_{DDA} - V_{SSA} ; V_{DDD} - V_{SSD}	-0.5V to +6V
V_{DDD} – V_{DDA}[2]	< 0.3V

1. Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.

2. At any time, the digital power supply should not be higher the 0.3V from the analog power supply.

9.2. Operating Conditions

Condition	Value
Industrial operating temperature	-40^0C to $+85^0$C
Analog supply voltage (V_{DDA})	+4.5V to +5.5V
Digital supply voltage (V_{DDD})	+2.7V to +3.3V
Ground voltage (V_{SSA}, V_{SSD})	0V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

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10. ELECTRICAL CHARACTERISTICS

10.1. General Parameters

Symbol	Parameters	Conditions	Min [2]	Typ [1]	Max [2]	Units
V_{IL}	Input LOW Voltage				0.5	V
V_{IH}	Input HIGH Voltage		2.2			V
V_{OL}	PCMT Output LOW Voltage	I_{OL} = 1.6 mA			0.4	V
V_{OH}	PCMT Output HIGH Voltage	I_{OL} = -1.6 mA	V_{DDD} – 0.5			V
I_{DDA} I_{DDD}	V_{DDA} Current (Operating) -ADC+DAC	PUI = 1 FSX running MCLK running		5.5 25	8 1000	mA µA
I_{SBA} I_{SBD}	V_{CCA} Current (Standby)	PUI = 1 FSX = 0 MCLK running		200 0.2	500 100	nA µA
I_{PDA} I_{PDD}	V_{CCA} Current (Power Down) V_{CCD} Current (Power Down)	PUI = 0 PUI = 0		200 200	500 500	nA nA
I_{IL}	Input Leakage Current	V_{SSD}<V_{IN}<V_{DDD}			+/-10	µA
I_{OL}	PCMT Output Leakage Current	V_{SSA}<PCMT<V_{DDA} High Z State			+/-10	µA
C_{IN}	Digital Input Capacitance				10	pF
C_{OUT}	PCMT Output Capacitance	PCMT High Z			15	pF

1. Typical values: T_A = 25°C , V_{DDA} = 5.0 V, V_{DDD} = 3.0 V

2. All min/max limits are guaranteed by Nuvoton via electrical testing or characterization. Not all specifications are 100 percent tested.

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10.2. Analog Signal Level and Gain Parameters

V_{DDA}=5V ±10%; V_{SSA}=0V; T_A=-40°C to +85°C; all analog signals referred to V_{AG}; MCLK=BCLK= 2.048 MHz; FST=FSR=8kHz Synchronous operation.

PARAMETER	SYM.	CONDITION	TYP.	TRANSMIT (A/D)		RECEIVE (D/A)		UNIT
				MIN.	MAX.	MIN.	MAX.	
Absolute Level	L_{ABS}	0 dBm0 = 0dBm @ 600Ω	1.096	---	---	---	---	V_{PK}
Max. Transmit Level	T_{XMAX}	3.17 dBm0 for μ-Law 3.14 dBm0 for A-Law	1.579 1.573	--- ---	--- ---	--- ---	--- ---	V_{PK} V_{PK}
Absolute Gain (0 dBm0 @ 1020 Hz; T_A=+25°C)	G_{ABS}	0 dBm0 @ 1020 Hz; T_A=+25°C	0	-0.25	+0.25	-0.25	+0.25	dB
Absolute Gain variation with Temperature	G_{ABST}	T_A=0°C to T_A=+70°C T_A=-40°C to T_A=+85°C	0	-0.03 -0.05	+0.03 +0.05	-0.03 -0.05	+0.03 +0.05	dB
Frequency Response, Relative to 0dBm0 @ 1020 Hz	G_{RTV}	15 Hz 50 Hz 60 Hz 200 Hz 300 to 3000 Hz 3300 Hz 3400 Hz 3600 Hz 4000 Hz 4600 Hz to 100 kHz	--- --- --- --- --- --- --- --- --- ---	--- --- --- -1.0 -0.20 -0.35 -0.8 --- --- ---	-40 -30 -26 -0.4 +0.15 +0.15 0 0 -14 -32	-0.5 -0.5 -0.5 -0.5 -0.20 -0.35 -0.8 --- --- ---	0 0 0 0 +0.15 +0.15 0 0 -14 -30	dB
Gain Variation vs. Level Tone (1020 Hz relative to –10 dBm0)	G_{LT}	+3 to –40 dBm0 -40 to –50 dBm0 -50 to –55 dBm0	--- --- ---	-0.3 -0.6 -1.6	+0.3 +0.6 +1.6	-0.2 -0.4 -1.6	+0.2 +0.4 +1.6	dB

10.3. Analog Distortion and Noise Parameters

V_{DDA}=5V ±10%; V_{SSA}=0V; T_A=-40°C to +85°C; all analog signals referred to V_{AG}; MCLK=BCLK= 2.048 MHz; FST=FSR=8kHz Synchronous operation.

PARAMETER	SYM.	CONDITION	TRANSMIT (A/D)			RECEIVE (D/A)			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Total Distortion vs. Level Tone (1020 Hz, μ-Law, C-Message Weighted)	$D_{LT\mu}$	+3 dBm0	36	---	---	34	---	---	dBC
		0 dBm0 to -30 dBm0	36	---	---	36	---	---	
		-40 dBm0	29	---	---	30	---	---	
		-45 dBm0	25	---	---	25	---	---	
Total Distortion vs. Level Tone (1020 Hz, A-Law, Psophometric Weighted)	D_{LTA}	+3 dBm0	36	---	---	34	---	---	dBp
		0 dBm0 to -30 dBm0	36	---	---	36	---	---	
		-40 dBm0	29	---	---	30	---	---	
		-45 dBm0	25	---	---	25	---	---	
Spurious Out-Of-Band at RO- (300 Hz to 3400 Hz @ 0dBm0)	D_{SPO}	4600 Hz to 7600 Hz	---	---	---	---	---	-30	dB
		7600 Hz to 8400 Hz	---	---	---	---	---	-40	
		8400 Hz to 100000 Hz	---	---	---	---	---	-30	
Spurious In-Band (700 Hz to 1100 Hz @ 0dBm0)	D_{SPI}	300 to 3000 Hz	---	---	-47	---	---	-47	dB
Intermodulation Distortion (300 Hz to 3400 Hz –4 to –21 dBm0	D_{IM}	Two tones	---	---	-41	---	---	-41	dB
Crosstalk (1020 Hz @ 0dBm0)	D_{XT}		---	---	-75	---	---	-75	dBm0
Absolute Group Delay	τ_{ABS}	1200 Hz	---	---	360	---	---	240	μsec
Group Delay Distortion (relative to group delay @ 1200 Hz)	τ_D	500 Hz	---	---	750	---	---	750	μsec
		600 Hz	---	---	380	---	---	370	
		1000 Hz	---	---	130	---	---	120	
		2600 Hz	---	---	130	---	---	120	
		2800 Hz	---	---	750	---	---	750	
Idle Channel Noise	N_{IDL}	μ-Law; C-message	---	---	22	---	---	13	dBrnc0
		A-Law; Psophometric	---	---	-68	---	---	-78	dBm0p

10.4. Analog Input and Output Amplifier Parameters

V_{DDA}=5V ±10%; V_{SSA}=0V; T_A=-40°C to +85°C; all analog signals referred to V_{AG};

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT.
AI Input Offset Voltage	$V_{OFF,AI}$	AI+, AI-	---	---	±25	mV
AI Input Current	$I_{IN,AI}$	AI+, AI-	---	±0.1	±1.0	µA
AI Input Resistance	$R_{IN,AI}$	AI+, AI- to V_{AG}	10	---	---	MΩ
AI Input Capacitance	$C_{IN,AI}$	AI+, AI-	---	---	10	pF
AI Common Mode Input Voltage Range	$V_{CM,AI}$	AI+, AI-	1.2	---	V_{DDA}-1.2	V
AI Common Mode Rejection Ratio	$CMRR_{TI}$	AI+, AI-	---	60	---	dB
AI Amp Gain Bandwidth Product	GBW_{TI}	AO, R_{LD}≥10kΩ	---	2150	---	kHz
AI Amp DC Open Loop Gain	G_{TI}	AO, R_{LD}≥10kΩ	---	95	---	dB
AI Amp Equivalent Input Noise	N_{TI}	C-Message Weighted	---	-24	---	dBrnC
AO Output Voltage Range	V_{TG}	R_{LD}=10kΩ to V_{AG} R_{LD}=2kΩ to V_{AG}	0.5 1.0	--- ---	V_{DDA}-0.5 V_{DDA}-1.0	V
Load Resistance	R_{LDTGRO}	AO, RO to V_{AG}	2	---	---	kΩ
Load Capacitance	C_{LDTGRO}	AO, RO	---	---	100	pF
AO & RO Output Current	I_{OUT1}	0.5 ≤AO,RO-≤ V_{DDA}-0.5	±1.0	---	---	mA
RO- Output Resistance	R_{RO-}	RO-, 0 to 3400 Hz	---	1	---	Ω
RO- Output Offset Voltage	$V_{OFF,RO-}$	RO- to V_{AG}	---	---	±25	mV
Analog Ground Voltage	V_{AG}	Relative to V_{SSA}	2.429	2.5	2.573	V
V_{AG} Output Resistance	R_{VAG}	Within ±25mV change	---	2.5	12.5	Ω

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT.
Power Supply Rejection Ratio (0 to 100 kHz to V_{DDA}, C-message)	PSRR	Transmit Receive	30 30	80 75	--- ---	dBC
PAI Input Offset Voltage	$V_{OFF,PAI}$	PAI	---	---	±20	mV
PAI Input Current	$I_{IN,PAI}$	PAI	---	±0.05	±1.0	µA
PAI Input Resistance	$R_{IN,PAI}$	PAI to V_{AG}	10	---	---	MΩ
PAI Amp Gain Bandwidth Product	GBW_{PI}	PAO- no load	---	1000	---	kHz
Output Offset Voltage	$V_{OFF,PO}$	PAO+ to PAO-	---	---	±50	mV
Load Resistance	R_{LDPO}	PAO+, PAO- differentially	300	---	---	Ω
Load Capacitance	C_{LDPO}	PAO+, PAO- differentially	---	---	1000	pF
PO Output Current	I_{OUTPO}	0.5 ≤AO,RO-≤ V_{DDA}-0.5	±10.0	---	---	mA
PO Output Resistance	R_{PO}	PAO+ to PAO-	---	1	---	Ω
PO Differential Gain	G_{PO}	R_{LD}=300Ω, +3dBm0, 1 kHz, PAO+ to PAO-	-0.2	0	+0.2	dB
PO Differential Signal to Distortion C-Message weighted	D_{PO}	Z_{LD}=300Ω Z_{LD}=100nF + 100Ω Z_{LD}=100nF + 20Ω	45 --- ---	60 40 40	--- --- ---	dBC
PO Power Supply Rejection Ratio (0 to 25 kHz to V_{DDA}, Differential out)	$PSRR_{PO}$	0 to 4 kHz 4 to 25 kHz	40 ---	55 40	--- ---	dB

10.5. DIGITAL I/O

10.5.1. μ-Law Encode Decode Chatacteristics

Normalized Encode Decision Levels	Digital Code								Normalized Decode Levels
	D7	D6	D5	D4	D3	D2	D1	D0	
	Sign	Chord	Chord	Chord	Step	Step	Step	Step	
8159	1	0	0	0	0	0	0	0	8031
7903									:
:									
4319	1	0	0	0	1	1	1	1	4191
4063									:
:									
2143	1	0	0	1	1	1	1	1	2079
2015									:
:									
1055	1	0	1	0	1	1	1	1	1023
991									:
:									
511	1	0	1	1	1	1	1	1	495
479									:
:									
239	1	1	0	0	1	1	1	1	231
223									:
:									
103	1	1	0	1	1	1	1	1	99
95									:
:									
35	1	1	1	0	1	1	1	1	33
31									:
:									
3	1	1	1	1	1	1	1	0	2
1	1	1	1	1	1	1	1	1	0
0									

Notes:

Sign bit = 0 for negative values, sign bit = 1 for positive values

10.5.2. A-Law Encode Decode Characteristics

Normalized Encode Decision Levels	Digital Code								Normalized Decode Levels
	D7	D6	D5	D4	D3	D2	D1	D0	
	Sign	Chord	Chord	Chord	Step	Step	Step	Step	
4096	1	0	1	0	1	0	1	0	4032
3968									:
:									
2048	1	0	1	0	0	1	0	1	2112
2048									:
:									
1088	1	0	1	1	0	1	0	1	1056
1024									:
:									
544	1	0	0	0	0	1	0	1	528
512									:
:									
272	1	0	0	1	0	1	0	1	264
256									:
:									
136	1	1	1	0	0	1	0	1	132
128									:
:									
68	1	1	1	0	0	1	0	1	66
64									:
:									
2	1	1	0	1	0	1	0	1	1
0									

Notes:

1. Sign bit = 0 for negative values, sign bit = 1 for positive values
2. Digital code includes inversion of all even number bits

10.5.3. PCM Codes for Zero and Full Scale

Level	μ-Law			A-Law		
	Sign bit (D7)	Chord bits (D6,D5,D4)	Step bits (D3,D2,D1,D0)	Sign bit (D7)	Chord bits (D6,D5,D4)	Step bits (D3,D2,D1,D0)
+ Full Scale	1	000	0000	1	010	1010
+ Zero	1	111	1111	1	101	0101
- Zero	0	111	1111	0	101	0101
- Full Scale	0	000	0000	0	010	1010

10.5.4. PCM Codes for 0dBm0 Output

Sample	μ-Law			A-Law		
	Sign bit (D7)	Chord bits (D6,D5,D4)	Step bits (D3,D2,D1,D0)	Sign bit (D7)	Chord bits (D6,D5,D4)	Step bits (D3,D2,D1,D0)
1	0	001	1110	0	011	0100
2	0	000	1011	0	010	0001
3	0	000	1011	0	010	0001
4	0	001	1110	0	011	0100
5	1	001	1110	1	011	0100
6	1	000	1011	1	010	0001
7	1	000	1011	1	010	0001
8	1	001	1110	1	011	0100

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11. TYPICAL APPLICATION CIRCUIT

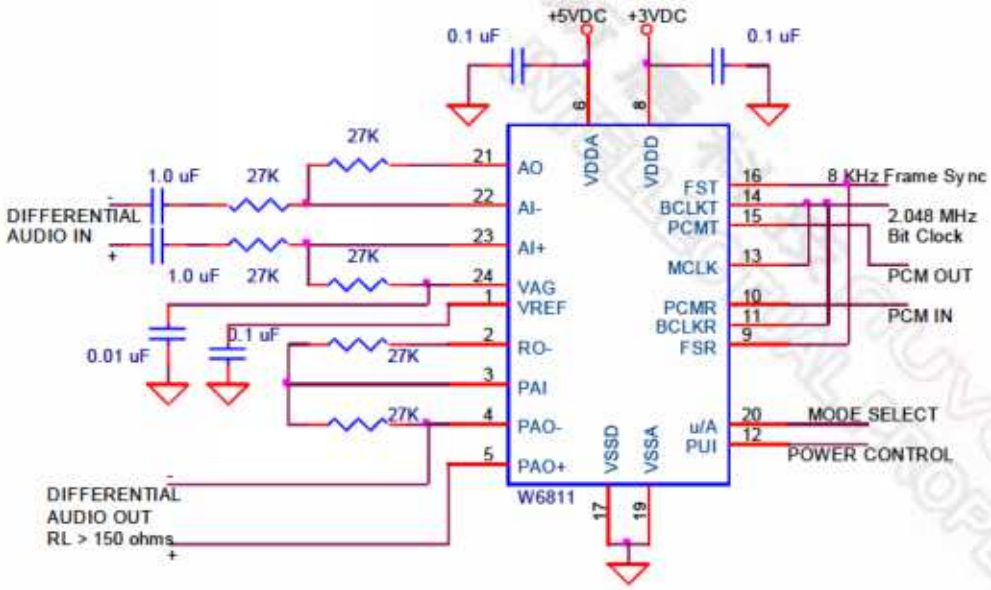


Figure 11.1 Typical circuit for Differential Analog I/O's

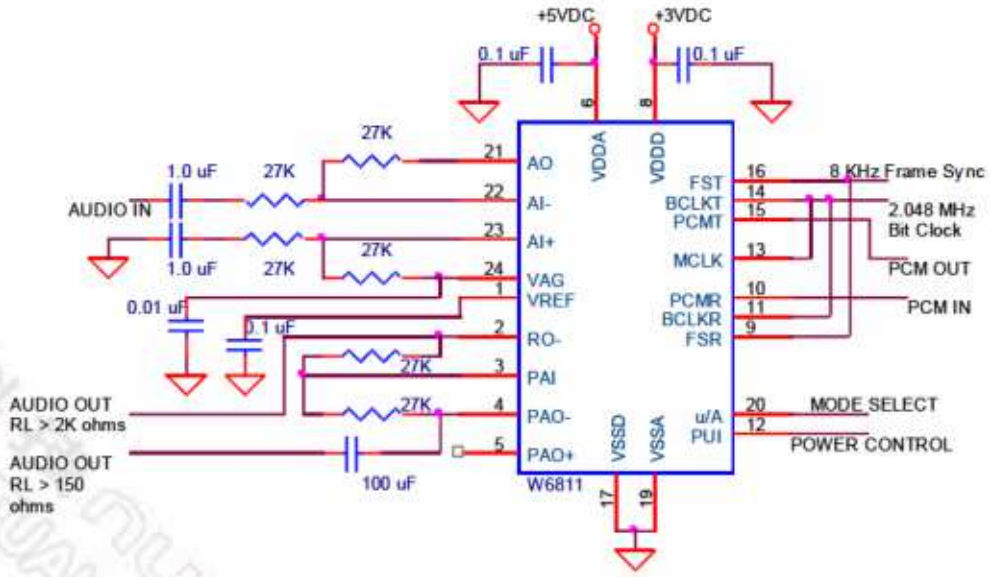


Figure 11.2 Typical circuit for Single Ended Analog I/O's

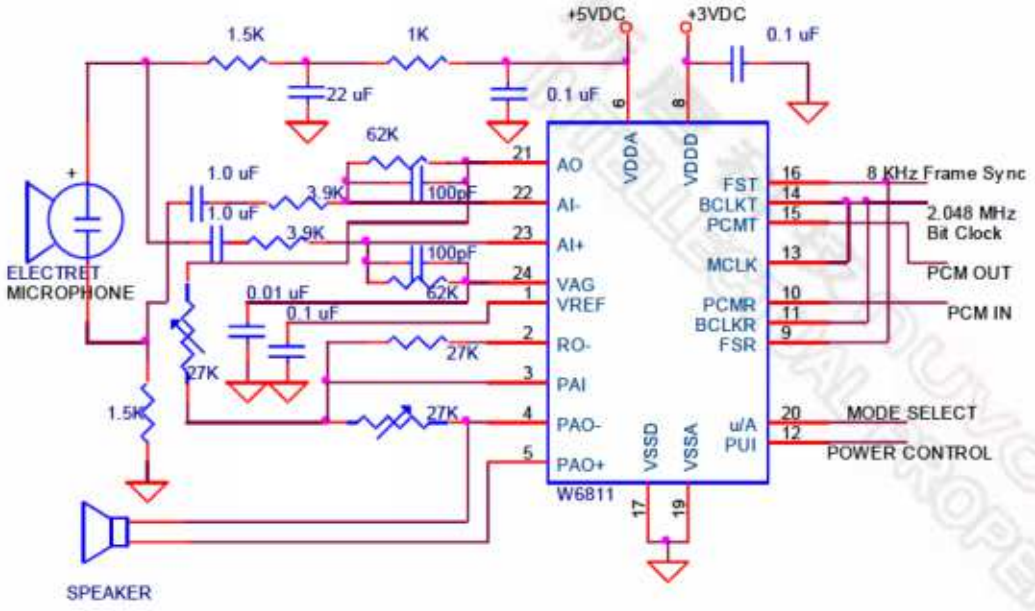


Figure 11.3 Handset Interface

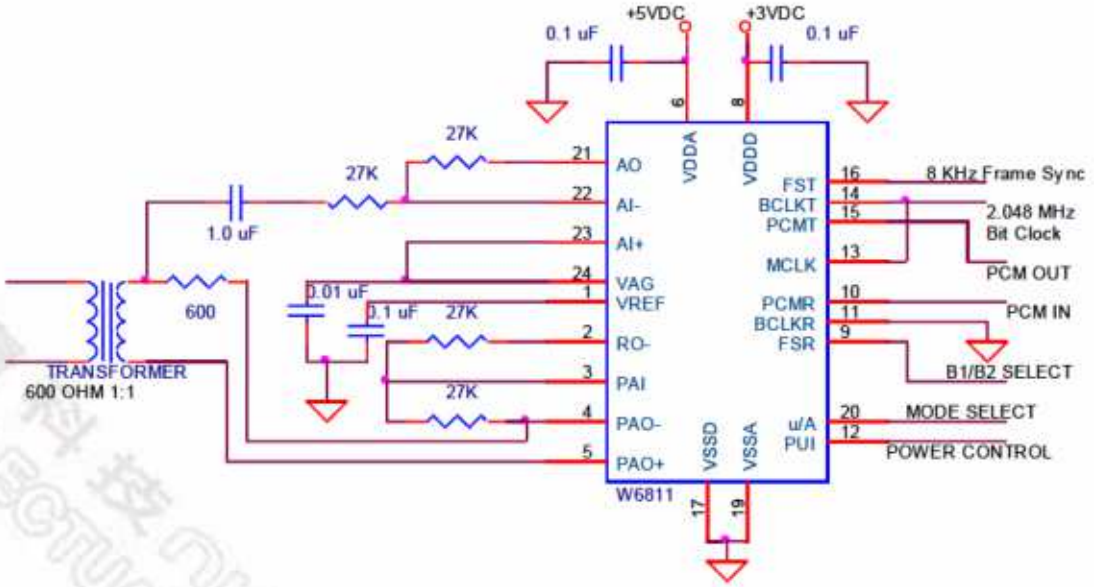
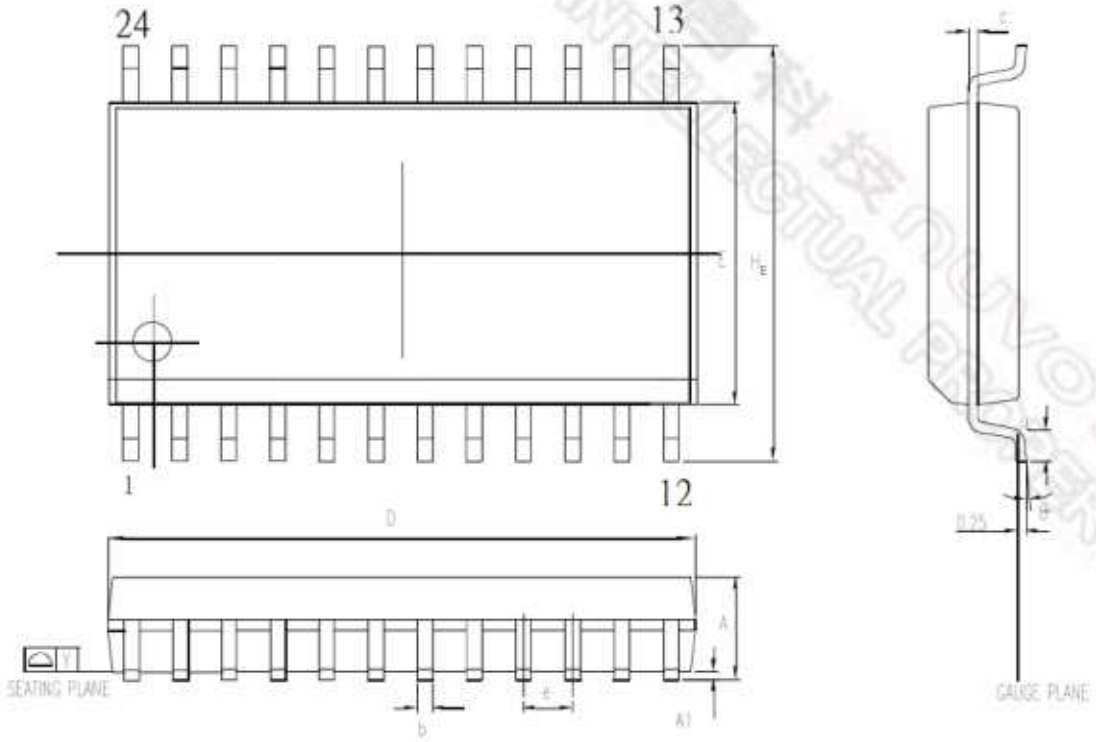


Figure 11.4 Transformer Interface Circuit in GCI mode

12. PACKAGE SPECIFICATION

12.1. 24L SOP-300MIL

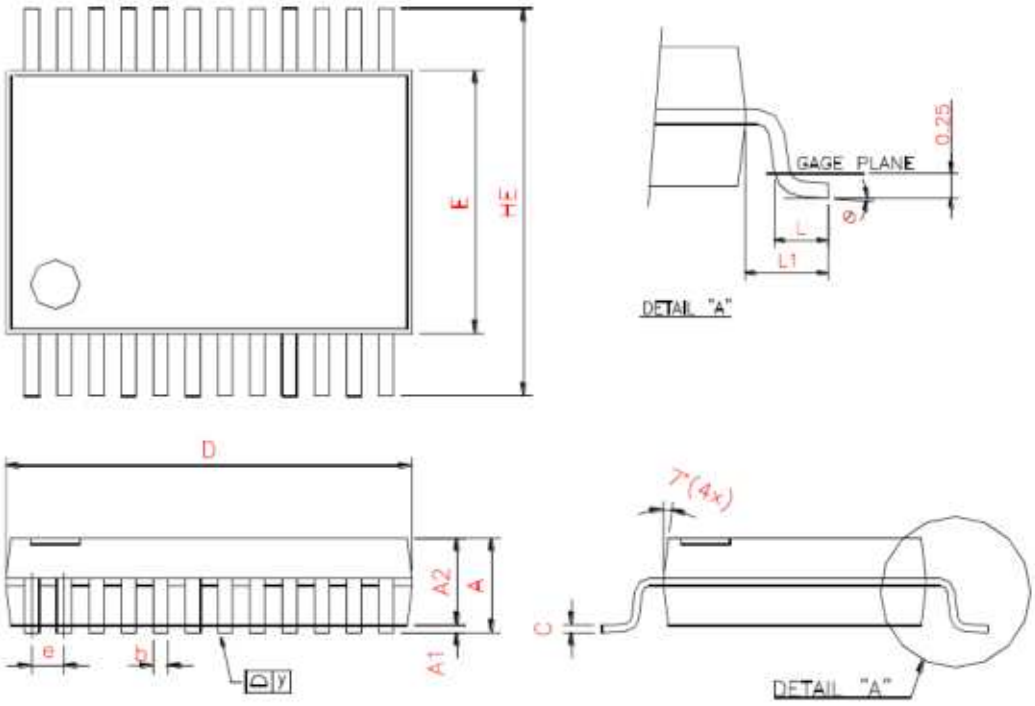
SMALL OUTLINE PACKAGE (SAME AS SOG & SOIC) DIMENSIONS



SYMBOL	DIMENSION (MM)		DIMENSION (INCH)	
	MIN.	MAX.	MIN.	MAX.
A	2.35	2.65	0.093	0.104
A1	0.10	0.30	0.004	0.012
b	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
E	7.40	7.60	0.291	0.299
D	15.20	15.60	0.598	0.614
e	1.27 BSC		0.050 BSC	
H_E	10.00	10.65	0.394	0.419
Y		0.10		0.004
L	0.10	1.27	0.016	0.050
θ	0°	8°	0	8°

12.2. 24L SSOP-209 MIL

SHRINK SMALL OUTLINE PACKAGE
DIMENSIONS

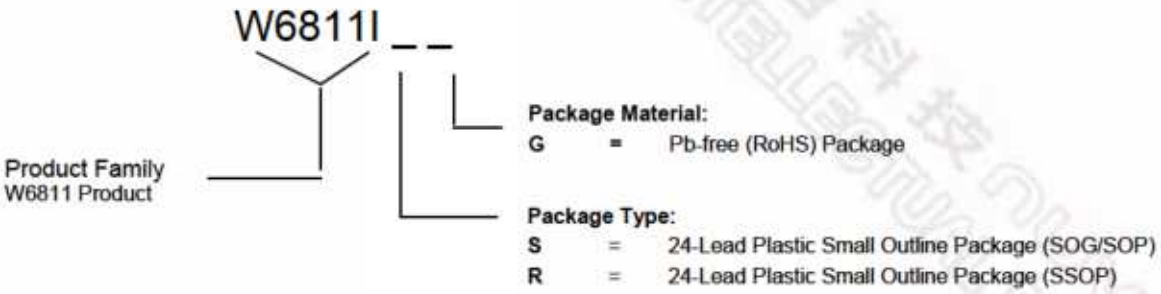


Control dimension are in millimeters

SYMBOLS	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	2.00	—	—	0.079
A1	0.05	—	0.15	0.002	—	0.006
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22	0.30	0.38	0.0086	0.012	0.015
C	0.09	0.15	0.25	0.0035	0.006	0.0098
D	7.90	8.20	8.50	0.311	0.323	0.335
HE	7.40	7.80	8.20	0.291	0.307	0.323
E	5.00	5.30	5.60	0.197	0.209	0.220
e	—	0.65	—	—	0.0256	—
L	0.55	0.75	0.95	0.022	0.030	0.037
L1	—	1.25	—	—	0.0492	—
θ	0°	4°	8°	0°	4°	8°
y	—	—	0.10	—	—	0.004

13. Ordering Information

Nuvoton Part Number Description



When ordering W6811 series devices, please refer to the following part numbers.

Part Number
W6811ISG
W6811IRG

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14. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A10	October 2003	34	Changed the package dimension of the SSOP24 package
A11	April 2005	41	Add Important Notice
A12	September, 2005	2 11, 12 22 23 23 29, 30 35	Added reference to Pb-free RoHS packaging Capitalized logic HIGH/LOW Extended conditions on Table 10.2. Extended conditions on Table 10.3. Corrected Idle Channel Noise min/max and units. Improved Application Diagrams Added G package ordering code
A13	January 2009	24 35 35	Idle Channel Noise value updated PDIP package no long supported Leaded packages no longer supported
A14	March 2010	Various	TSSOP package no longer supported
A15	January 2011	30	SOP-24 package diagram updated

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