Mono Audio Codec with Speaker Driver

emPowerAudio™

1. GENERAL DESCRIPTION

The WAU8812 is a cost effective and low power wideband MONO audio CODEC. It is designed for voice telephony related applications. Functions include Automatic Level Control (ALC) with noise gate, PGA, standard audio interface I²S, PCM with time slot assignment, and on-chip PLL. The device provides one differential microphone input and one single ended auxiliary input (multi purpose). There are few variable gain control stages in the audio path. It also includes MONO line output and integrated BTL speaker driver.

The analog inputs have PGA on the front end, allowing dynamic range optimization with a wide range of input sources. The microphone amplifiers have a programmable gain from -12dB to +35.25dB to handle both amplified microphones. In addition to a digital high pass filter to remove DC offset voltages, the ADC also features voice band digital filtering. Voice-band data is accepted by the audio interface (I²S). The DAC converter path includes filtering and mixing, programmable-gain amplifiers (PGA), and soft muting. The digital interfaces, 2-Wire or SPI, have independent supply voltage to allow integration into multiple supply systems. The WAU8812 operates at supply voltages from 2.5V to 3.6V, although the digital core can operate at voltage as low as 1.71V to save power.

2. FEATURES

24-bit signal processing linear Audio CODEC
- Audio DAC: 93dB SNR and -84dB THD
- Audio ADC: 91dB SNR and -79dB THD
- Support variable sample rates for 8 - 48KHz
- Integrated BTL Speaker Driver 0.8W into 8Ω / 5V
- Integrated Headset Driver 40mW into 16Ω / 3.3V

Analog I/O
- Integrated programmable Microphone Amplifier
- Integrated Line Input and Line Output
- Integrated Audio Switches
- Earphone / Speaker / Line Output selection
- Microphone / Line Inputs selection
- Low Noise bias supplied for microphone
- Digital Playback Limiter
- On-chip PLL

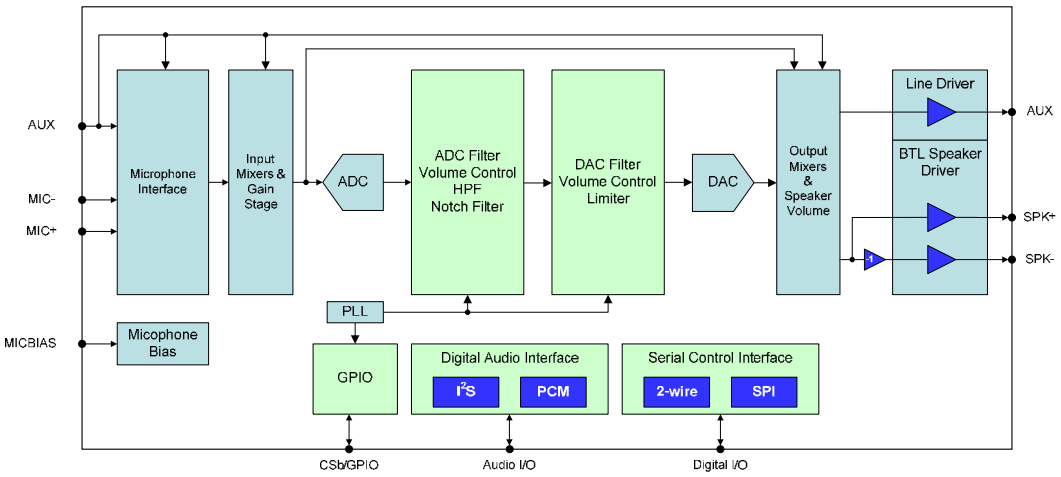
Interfaces
- I²S digital interface
- PCM output with time slot assignment
- SPI & 2-Wire serial control Interface (I²C style; Read/Write capable)

Low Power, Low Voltage
- Analog Supply: 2.5V to 3.6V
- Digital Supply: 1.71V to 1.95V
- Nominal Operating Voltage: 3.3V

Additional features
- Programmable ALC
- ADC Notch Filter
- Programmable High Pass Filter
- Digital A/D-D/A Passthrough
- AEC-Q100 & TS16949 qualification
- Industrial temperature: range: –40°C to +85°C

Applications
- VoIP Telephones
- Conference speaker-phone
- IP PBX
- Mobile Telephone Hands-free Kits
- Residential & Consumer Intercoms
- General Purpose low power audio CODEC

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3. PIN CONFIGURATION

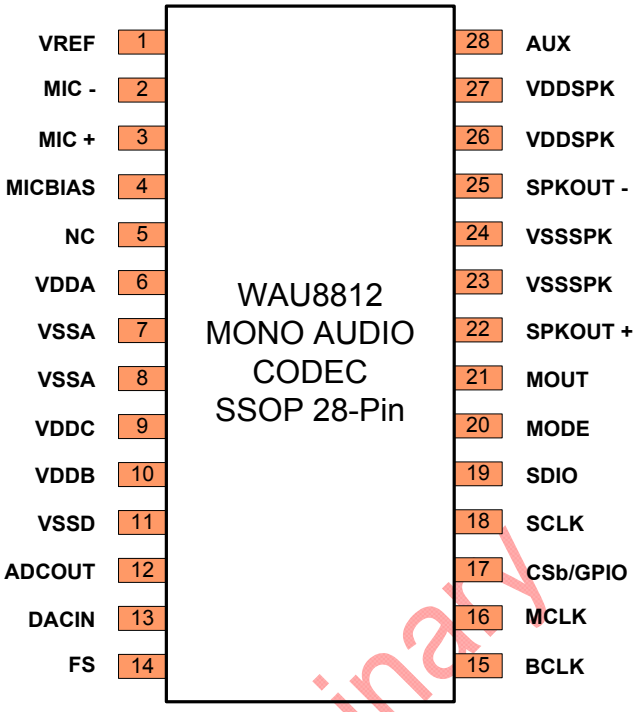


Figure 1: 28-Pin SSOP Package

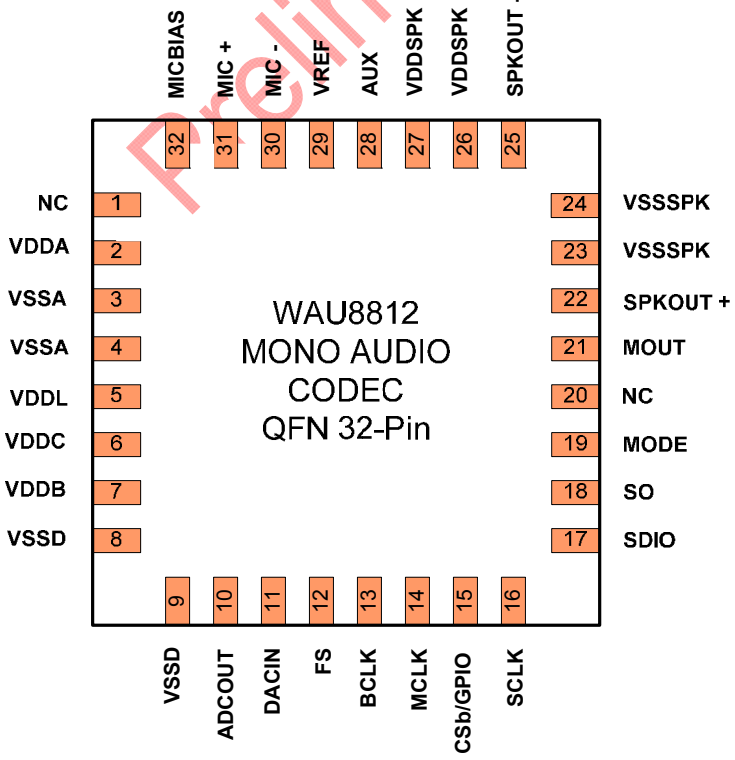


Figure 2: 32-Pin QFN Package

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4. PIN DESCRIPTION

Pin Name	28-Pin	32-Pin	Functionality	A/D	Pin Type
VREF	1	29	Decoupling internal analog mid supply reference	A	O
MIC-	2	30	Microphone Negative Input	A	I
MIC+	3	31	Microphone Positive Input	A	I
MICBIAS	4	32	Microphone Bias	A	O
NC	5	1	No Connect		
VDDA	6	2	Analog Supply	A	I
VSSA	7	3	Analog Ground	A	O
VSSA	8	4	Analog Ground	A	O
VDDL	-	5	Logic supply voltage. This pin should not be hooked up to an external supply	D	O
VDDC	9	6	Digital Supply Core	D	I
VDDB	10	7	Digital Supply Buffer	D	I
VSSD	11	8	Digital Ground	D	O
VSSD	-	9	Digital Ground	D	O
ADCOUT	12	10	Digital Audio Data Output	D	O
DACIN	13	11	Digital Audio Data Input	D	I
FS	14	12	Frame Sync	D	I/O
BCLK	15	13	Bit Clock	D	I/O
MCLK	16	14	Master Clock	D	I
CSb/GPIO	17	15	SPI Chip Select or General Purposes 1 I/O	D	I/O
SCLK	18	16	SPI or 2-Wire Serial Clock	D	I
SDIO	19	17	SPI Data In or 2-Wire I/O	D	O
SO	-	18	SPI Data Output	D	O
MODE	20	19	Interface Select (2-Wire or SPI)	D	I
NC	-	20	No Connect		
MOUT	21	21	MONO Output	A	O
SPKOUT+	22	22	Speaker Positive Output	A	O
VSSSPK	23	23	Speaker Ground	A	O
VSSSPK	24	24	Speaker Ground	A	O
SPKOUT-	25	25	Speaker Negative Output	A	O
VDDSPK	26	26	Speaker Supply	A	I
VDDSPK	27	27	Speaker Supply	A	I
AUX	28	28	Auxiliary Input	A	I

Table 1: Pin Description for SSOP and QFN Packages

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5. BLOCK DIAGRAM

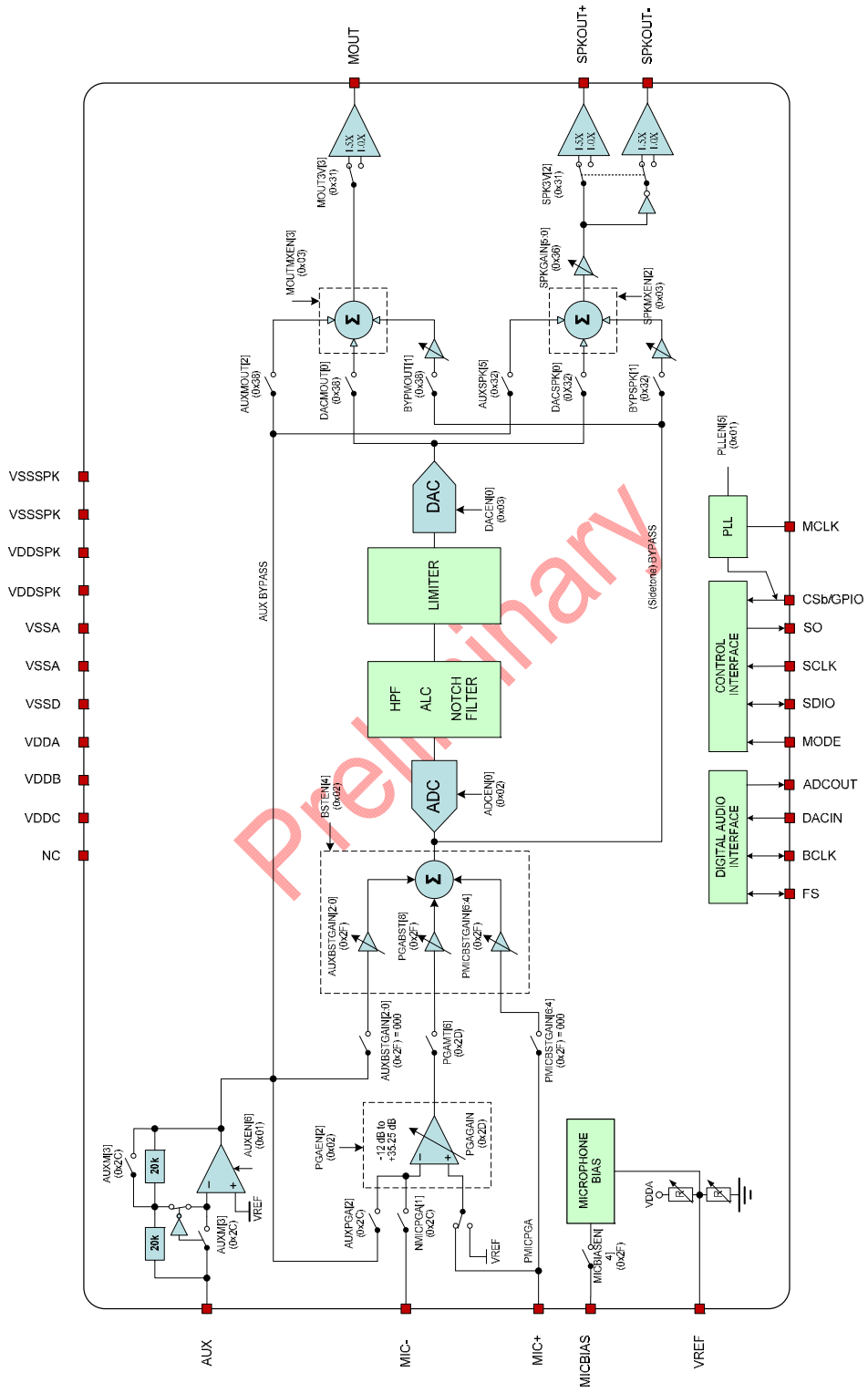


Figure 3: WAU8812 General Block Diagram

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6. REGISTER DESCRIPTION

Register Address		Register Bits									Default
DEC	HEX	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	0x0	RESET (SOFTWARE)									
		POWER MANAGEMENT									
1	0x01	DCBUFEN	0	AUXEN	PLLEN	MICBIASEN	ABIASEN	IOBUFEN	REFIMP		0x000
2	0x02	0	0	0	0	BSTEN	0	PGAEN	0	ADCEN	0x000
3	0x03	0	MOUTEN	NSPKEN	PSPKEN	BIASGEN	MOUTMXEN	SPKMXEN	0	DACEN	0x000
		AUDIO CONTROL									
4	0x04	BCLKP	FSP	WLEN[1:0]		AIFMT[1:0]		DACPHS	ADCPHS	0	0x050
5	0x05	0	0	0	CMB8	DACCM[1:0]		ADCCM[1:0]		ADDAP	0x000
6	0x06	CLKM	MCLKSEL[2:0]			BCLKSEL[2:0]			0	CLKIOEN	0x140
7	0x07	SPIEN	0	0	0	0	SMPLR[2:0]			SCLKEN	0x000
8	0x08	0	0	0	GPIOPLL[1:0]		GPIOPL	GPIOSEL[2:0]			0x000
10	0x0A	0	0	DACMT	DEEMP[1:0]		DACOS	AUTOMT	0	DACPL	0x000
11	0x0B	0	DACGAIN								0x0FF
14	0x0E	HPFEN	HPFAM	HPF[2:0]			ADCOS	0	0	ADCPL	0x100
15	0x0F	0	ADCGAIN								0x0FF
		DIGITAL TO ANALOG (DAC) LIMITER									
24	0x18	DACLIMEN	DACLIMDCY[3:0]				DACLIMATK[3:0]				0x032
25	0x19	0		DACLIMTHL[2:0]			DACLIMBST[3:0]				0x000
		NOTCH FILTER									
27	0x1B	NFCU	NFCEN	NFCA0[13:7]							0x000
28	0x1C	NFCU	0	NFCA0[6:0]							0x000
29	0x1D	NFCU	0	NFCA1[13:7]							0x000
30	0x1E	NFCU	0	NFCA1[6:0]							0x000
		ALC CONTROL									
32	0x20	ALCEN	0	0	ALCMXGAIN[2:0]			ALCMNGAIN[2:0]			0x038
33	0x21	ALCZC	ALCHT[3:0]				ALCSL[3:0]				0x00B
34	0x22	ALCM	ALCDCY[3:0]				ALCATK[3:0]				0x032
35	0x23	0	0	0	0	0	ALCNEN	ALCNTH[2:0]			0x000
		PLL CONTROL									
36	0x24	0	0	0	0	PLLMCLK	PLLN[3:0]				0x008
37	0x25	0	0	0	PLLK[23:18]						0x00C
38	0x26	PLLK[17:9]									0x093
39	0x27	PLLK[8:0]									0x0E9
		INPUT, OUTPUT & MIXER CONTROL									
40	0x28	0	0	0	0	0	0	MOUTATT	SPKATT	MICBIASM	0x000
44	0x2C	MICBIASV		0	0	0	AUXM	AUXPGA	NMICPGA	PMICPGA	0x003
45	0x2D	0	PGAZC	PGAMT	PGAGAIN[5:0]						0x010
47	0x2F	PGABST	0	PMICBSTGAIN			0	AUXBSTGAIN			0x100
49	0x31	0	0	0	0	0	MOUT3V	SPK3V	TSEN	AOUTIMP	0x002
50	0x32	0	0	0	AUXSPK	0	0	0	BYPSPK	DACSPK	0x001
54	0x36	0	SPKZC	SPKMT	SPKGAIN[5:0]						0x039
56	0x38	0	0	MOUTMT	0	0	0	AUXMOUT	BYPMOUT	DACMOUT	0x001
58	0x3A	LPSPKA	LPIPBST	LPADC	LPSPKD	LPDAC	TRIMREG	0	IBADJ	0	0x000
		PCM TIME SLOT CONTROL									
59	0x3B	TSLOT[8:0]									0x000
60	0x3C	PCMTSEN	TRI	PCM8BIT	PUDOEN	PUDPE	PUDPS	0	0	TSLOT[9:8]	0x000
62	0x3E	0	REV[7:0]								0x000
63	0x3F	0	0	0	0	1	1	0	1	0	0x01A

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7. ABSOLUTE MAXIMUM RATINGS

CONDITION	MIN	MAX	Units
VDDB, VDDC, VDDA supply voltages	-0.3	+3.63	V
VDDSPK supply voltage (MOUT3V=0, SPK3V=0)	-0.3	+5.50	V
VDDSPK supply voltage (MOUT3V=1, SPK3V=1)	-0.3	+3.63	V
Core Digital Input Voltage range	VSSD – 0.3	VDDC + 0.30	V
Buffer Digital Input Voltage range	VSSD – 0.3	VDDB + 0.30	V
Analog Input Voltage range	VSSA – 0.3	VDDA + 0.30	V
Industrial operating temperature	-40	+85	^{0}C
Storage temperature range	-65	+150	^{0}C

CAUTION: Do not operate at or near the maximum ratings listed for extended period of time. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty. These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

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8. OPERATING CONDITIONS

Condition	Symbol	Min Value	Typical Value	Max Value	Units
Digital supply range (Core)	VDDC	1.71		3.60	V
Digital supply range (Buffer)	VDDB	1.71		3.60	V
Analogue supplies range	VDDA	2.50		3.60	V
Speaker supply (MOUT3V=0, SPK3V=0)	VDDSPK	2.50		3.60	V
Speaker supply (MOUT3V=1, SPK3V=1)	VDDSPK	2.50		5.50	V
Ground	VSSD, VSSA, VSSSPK		0		V

1. VDDA must be ≥ VDDC.
2. VDDB must be ≥ VDDC.

9. ELECTRICAL CHARACTERISTICS

VDDC = 1.8V, VDDA = VDDB = SPK3V = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue to Digital Converter (ADC)						
Full scale input signal [1]	V_{INFS}	PGABST = 0dB PGAGAIN = 0dB		1.0 0		V_{RMS} dBV
Signal to Noise Ratio [2]	SNR	Gain = 0dB, A-weighted	87	91		dB
Total Harmonic Distortion [3]	THD	Input = -1dBFS, Gain = 0dB		-79	-65	dB

Digital to Analogue Converter (DAC) to MONO output (all data measured with 10kΩ / 50pF load)						
Full Scale output signal [1]		MOUT3V=0		1.5x (V_{REF})		V_{RMS}
		MOUT3V=1		V_{REF}		
Signal to Noise Ratio [2]	SNR	A-weighted (ADC/DAC oversampling rate of 128)	90	93		dB
Total Harmonic Distortion [3]	THD	R_L = 10 kΩ; -1.5dBfs		-84	-70	dB

Auxiliary Analogue Input (AUX)						
Full-scale Input Signal Level[1]	V_{INFS}	Gain = 0dB		1 0		V_{RMS} dBV
Input Resistance	R_{AUX}	AUXM=0		20		kΩ
Input Capacitance	C_{AUX}			10		pF

Microphone Inputs (MICN & MICP) and MIC Input Programmable Gain Amplifier (PGA)						
Full-scale Input Signal Level [1]	V_{INFS}	PGABST = 0dB PGAGAIN = 0dB		1 0		V_{RMS} dBV
Programmable input PGA gain			-12		35.25	dB
Programmable Gain Step Size		Guaranteed monotonic		0.75		dB
Programmable Boost PGA gain		Boost disabled = 0		0		dB
		Boost enabled = 1		20		
Mute Attenuation				100		dB
PGA equivalent output noise		0 to 20kHz, Gain set to 35.25dB		110		µV
Auxiliary Input resistance	R_{AUX}	PGA Gain = 35.25dB		1.6		kΩ
		PGA Gain = 0dB		47		kΩ
		PGA Gain = -12dB		75		kΩ
Positive Microphone Input resistance	R_{MIC+}	PMICPGA = 1		94		kΩ
Input Capacitance	C_{MIC}			10		pF

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VDDC = 1.8V, VDDA = VDDB = SPK3V = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Speaker Output PGA						
Programmable Gain			-57		6	dB
Programmable Gain Step Size		Guaranteed monotonic		1		dB
BTL Speaker Output (SPKOUT+, SPKOUT- with 8Ω bridge tied load)						
Full scale output [7]		SPKBOOST = 0		VCCSPK / 3.3		V_{RMS}
		SPKBOOST = 1		(VCCSPK / 3.3) * 1.5		
Output Power	PO	Output power is very closely correlated with THD; see below				
Signal to Noise Ratio	SNR	SPK3V=3.3V, RL = 8Ω		90		dB
		SPK3V=5V, RL = 8Ω		90		dB
Total Harmonic Distortion (3-stage Output Amplifier)	THD	PO =180mW, RL = 8Ω, SPK3V=3.3V		-85		dB
		PO =400mW, RL = 8Ω, SPK3V=3.3V		-53		dB
		PO =360mW, RL = 8Ω, SPK3V=5V		-85		dB
		PO =800mW, RL = 8Ω, SPK3V=5V		-82		dB
Power Supply Rejection Ratio (50Hz - 22kHz)	PSRR	VDDSPK = 5V (non-boost)		80		dB
		VDDSPK = 3V (boost)		80		dB
Headphone' output (SPKOUTP, SPKOUTN with resistive load to ground)						
Full scale output [7]				V_{REF}		V_{RMS}
Signal to Noise Ratio	SNR	A-weighted		90		dB
Total Harmonic Distortion	THD	Po=20mW, RL = 16Ω, VDDSPK = 3.3V		-84		dB
		Po=20mW, RL = 32Ω, VDDSPK = 3.3V		-85		dB
Microphone Bias						
Bias Voltage	$V_{MICBIAS}$	(MBIASV = 0)		0.9* VDDA		V
		(MBIASV = 1)		0.65* VDDA		V
Bias Current Source	$I_{MICBIAS}$			3		mA
Output Noise Voltage	V_N	MICBIASM = 0 (1kHz to 20kHz)		14		nV/√Hz
		MICBIASM = 1 (1kHz to 20kHz)		4		nV/√Hz

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VDDC = 1.8V, VDDA = VDDB = SPK3V = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Automatic Level Control (ALC)/Limiter – ADC only						
Target Record Level			-28.5		-6	dB
Programmable Gain			-12		35.25	dB
Programmable Gain Step Size		Guaranteed Monotonic		0.75		dB
Gain Hold Time [4, 6]	tHOLD	MCLK=12.288MHz	0 / 2.67 / …/ 43691 (time doubles with each step)			ms
Gain Ramp-Up (Decay) Time [5, 6]	tDCY	ALC Mode ALCM=0 MCLK=12.288MHz	3.3 / 6.6 / 13.1 / … / 3360 (time doubles with each step)			ms
		Limiter Mode ALCM=1 MCLK=12.288MHz	0.73 / 1.45 / 2.91 / … / 744 (time doubles with each step)			ms
Gain Ramp-Down (Attack) Time [5, 6]	tATK	ALC Mode ALCM=0 MCLK=12.288MHz	0.83 / 1.66 / 3.33 / … / 852 (time doubles with each step)			ms
		Limiter Mode ALCM=1 MCLK=12.288MHz	0.18 / 0.36 / 0.73 / … / 186 (time doubles with each step)			ms

Digital Input / Output						
Input HIGH Level	V_{IH}		0.7 × VDDC			V
Input LOW Level	V_{IL}				0.3 × VDDC	V
Output HIGH Level	V_{OH}	I_{OL} = 1mA	0.9 × VDDC			V
Output LOW Level	V_{OL}	I_{OH} = -1mA		3.25	0.1 x VDDC	V

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Notes

1. Full Scale is relative to VDDA (FS = VDDA/3.3.) Input level to RIP and LIP is limited to a maximum of -3dB so that THD+N performance will not be reduced.

2. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full-scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).

3. THD+N (dB) - THD+N are a ratio, of the rms values, of (Noise + Distortion)/Signal.

4. Hold Time is the length of time between a signal detected being too quiet and beginning to ramp up the gain. It does not apply to ramping down the gain when the signal is too loud, which happens without a delay.

5. Ramp-up and Ramp-Down times are defined as the time it takes to change the PGA gain by 6dB of its gain range.

6. All hold, ramp-up and ramp-down times scale proportionally with MCLK

7. The maximum output voltage can be limited by the speaker power supply. If MOUT3V or SPK3V is, set then VDDSPK should be 1.5xVDDA to prevent clipping taking place in the output stage (when PGA gains are set to 0dB).

10. DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter					
Passband	+/- 0.025dB	0		0.454*fs	
	-6dB		0.5*fs		
Passband Ripple				+/-0.025	dB
Stopband		0.546*fs			
Stopband Attenuation	f > 0.546*fs	-60			dB
Group Delay			21/fs		
ADC High Pass Filter					
High Pass Filter Corner Frequency	-3dB		3.7		Hz
	-0.5dB		10.4		
	-0.1dB		21.6		
DAC Filter					
Passband	+/- 0.035dB	0		0.454*fs	
	-6dB		0.5*fs		
Passband Ripple				+/-0.035	dB
Stopband		0.546*fs			
Stopband Attenuation	f > 0.546*fs	-55			dB
Group Delay			29/fs		

Table 57 Digital Filter Characteristics

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1. Stop Band Attenuation (dB) – the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region
3. Note that this delay applies only to the filters and does not include

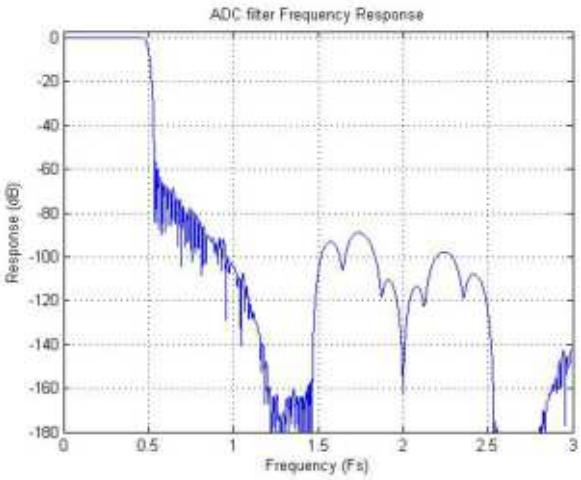


Figure 4: DAC Filter Frequency Response

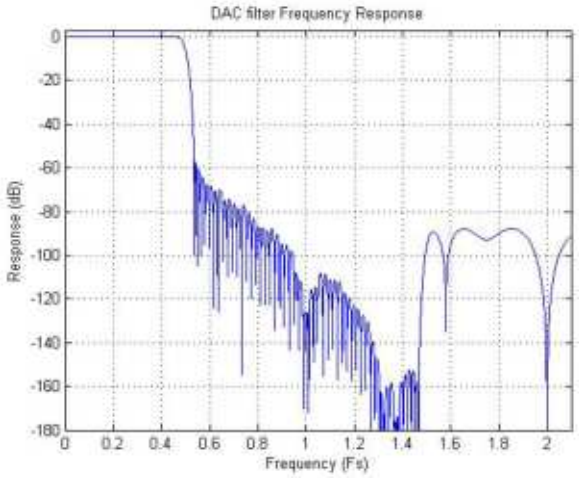


Figure 5: ADC Filter Frequency Response

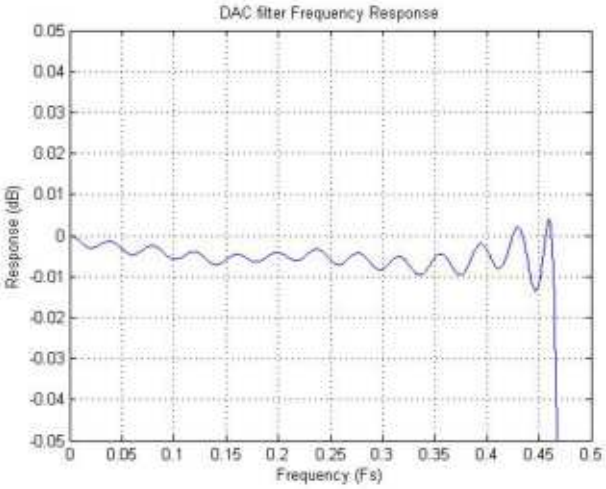


Figure 6: DAC Filter Ripple

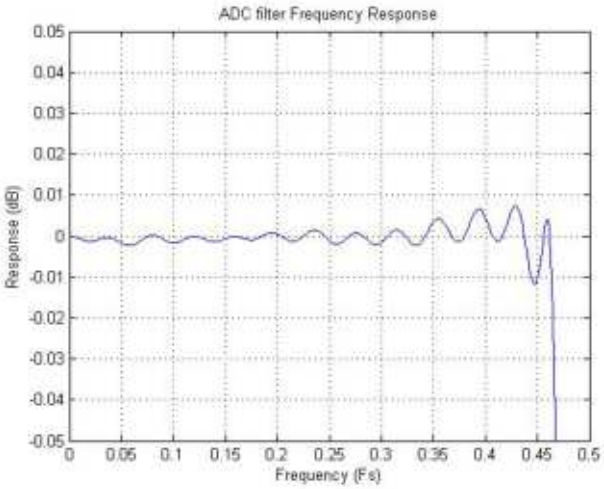


Figure 7: ADC Filter Ripple

11. TYPICAL APPLICATION

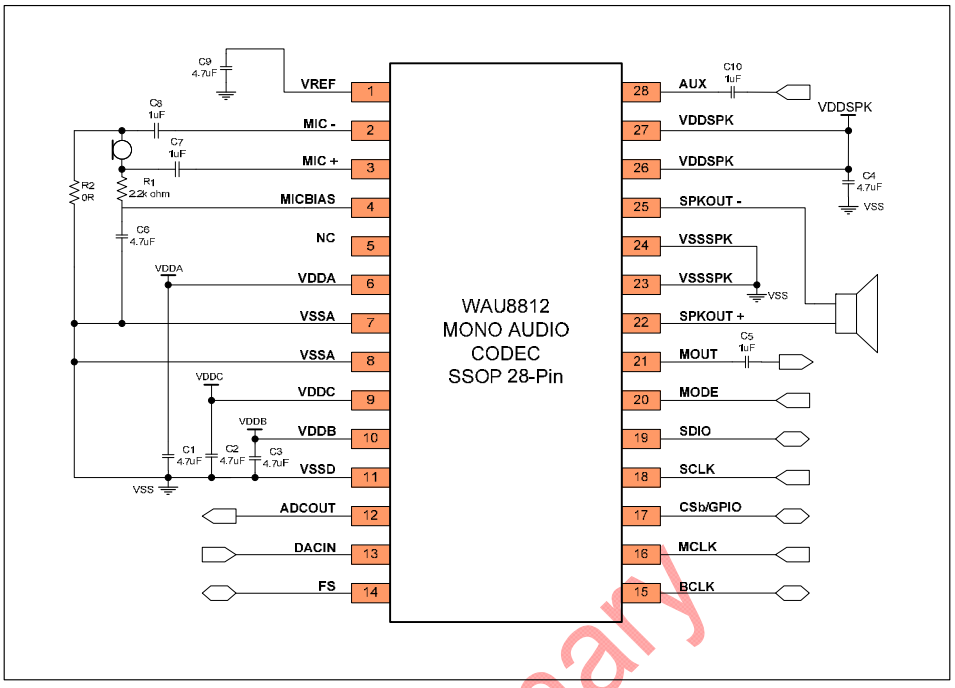


Figure 8: Application Diagram 28-Pin SSOP

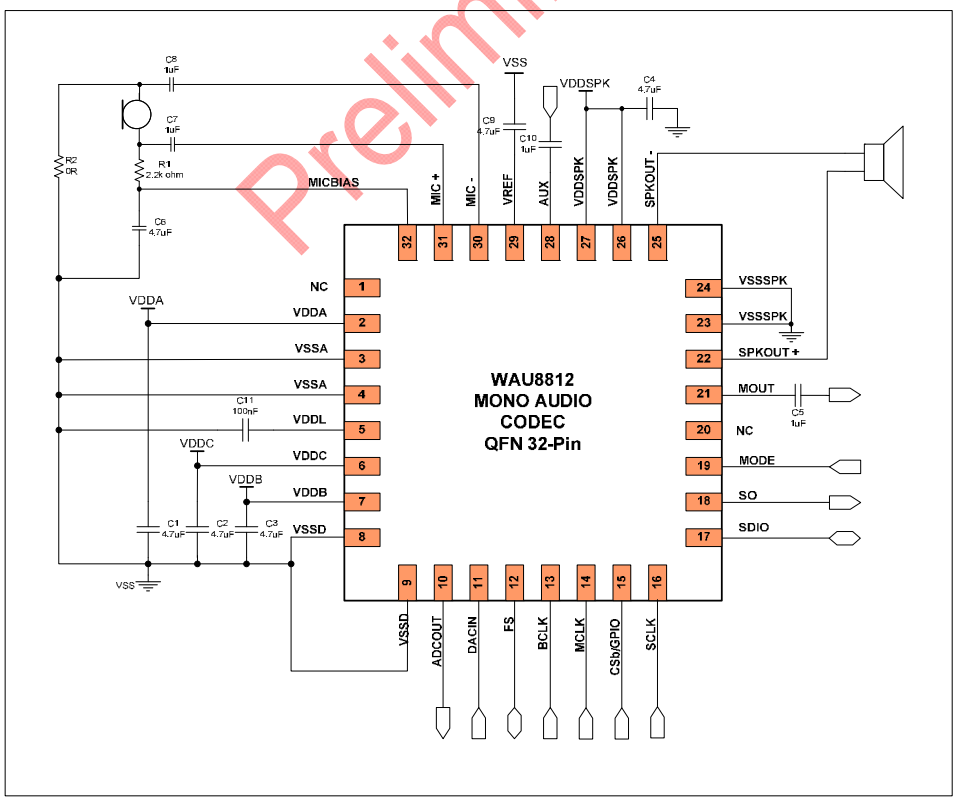
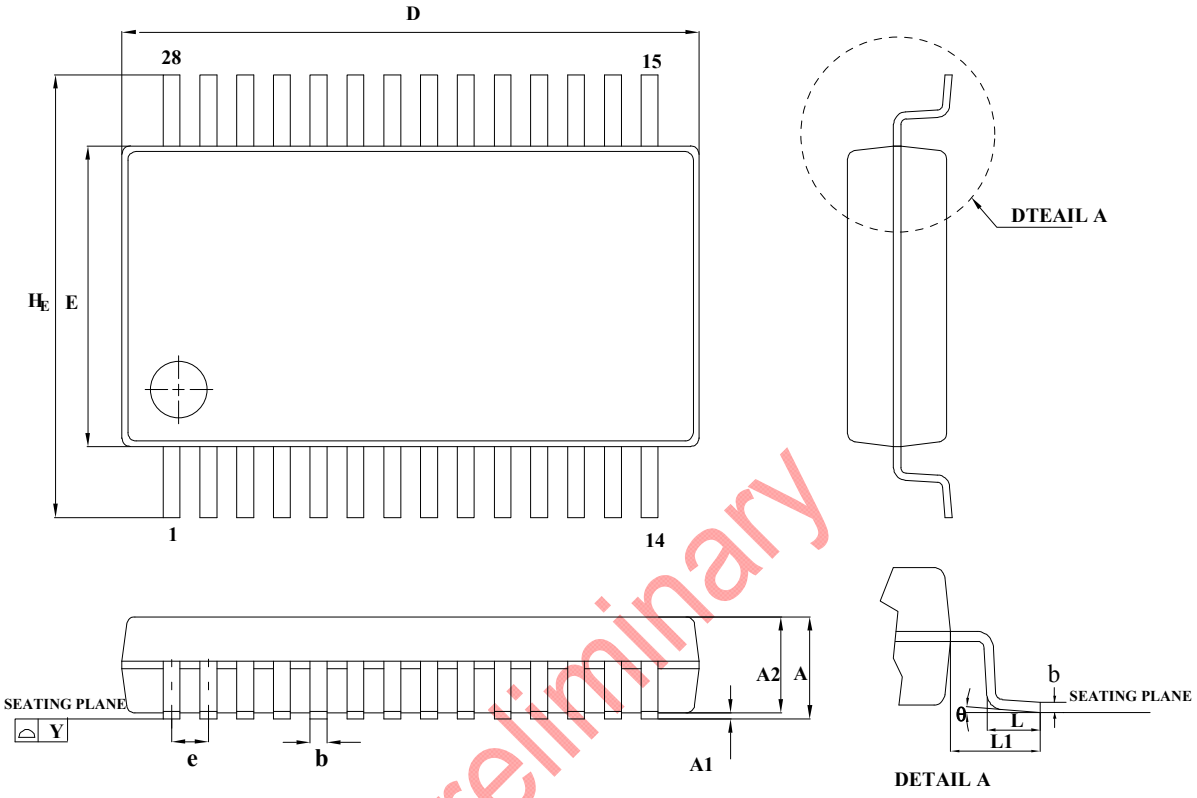


Figure 9: Application Diagram For 32-Pin QFN

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12. PACKAGE SPECIFICATION

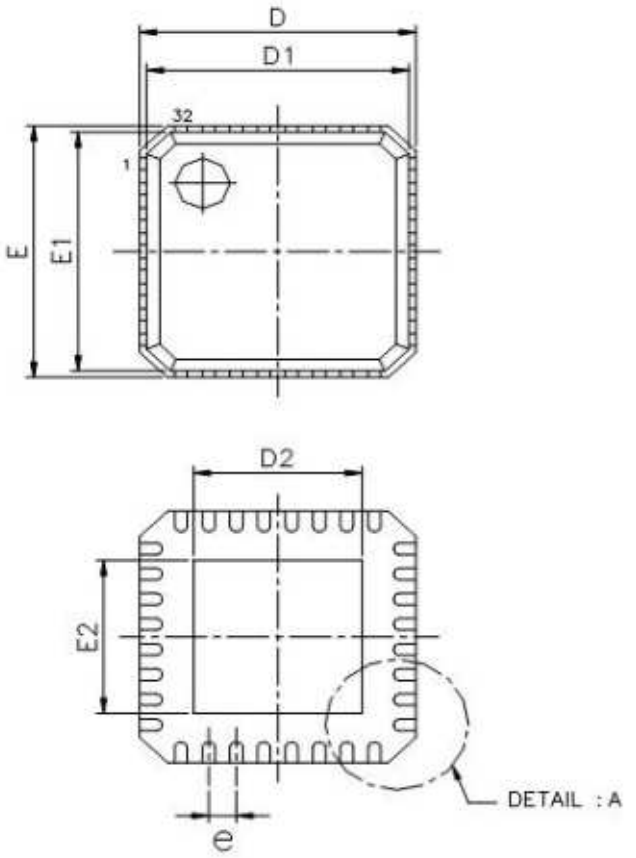
12.1. 28 Pin SSOP

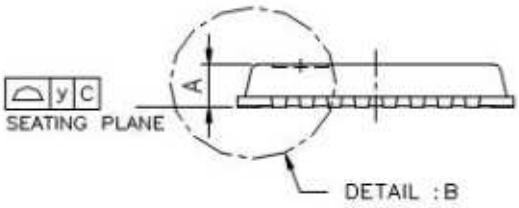


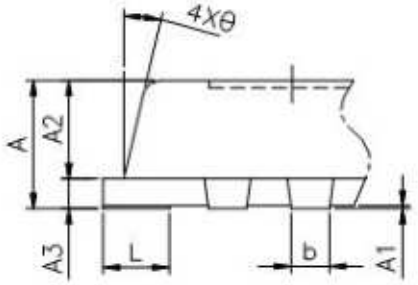
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SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	—	—	2.00	—	—	0.079
A1	0.05	—	—	0.002	—	—
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22	—	0.38	0.009	—	0.015
c	0.09	—	0.25	0.004	—	0.010
D	10.05	10.20	10.35	0.395	0.401	0.407
E	5.00	5.30	5.60	0.197	0.209	0.220
H_E	7.40	7.80	8.20	0.291	0.307	0.323
e	—	0.65	—	—	0.0256	—
L	0.55	0.75	0.95	0.021	0.030	0.037
L1	—	1.25	—	—	0.050	—
Y	—	—	0.10	—	—	0.004
θ	0	—	8	0	—	8

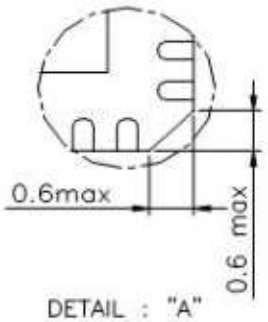
12.2. 32-Pin QFN







DETAIL : "B"



DETAIL : "A"

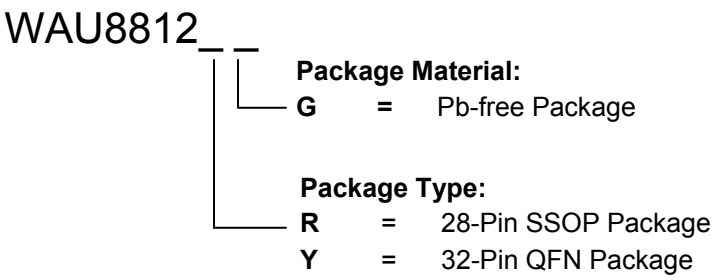
Controlling Dimension :Millimeters

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.60	0.65	0.80	0.024	0.026	0.031
A3		0.20 REF			0.008 REF	
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E		5.00 BSC			0.197 BSC	
D1/E1		4.75 BSC			0.187 BSC	
e		0.50 BSC			0.020 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	---	12°	0°	---	12°
y	---	---	0.08	---	---	0.0031
D2	2.90	3.05	3.20	0.114	0.120	0.126
E2	2.90	3.05	3.20	0.114	0.120	0.126

*D2,*E2:By die size difference

13. ORDERING INFORMATION

Nuvoton Part Number Description



Preliminary