ACS102-6T

AC switch family
Transient protected AC switch (ACS™)

Main product characteristics

$I_{T(RMS)}$	0.2 A
V_{DRM}/V_{RRM}	600 V
I_{GT}	5 mA

- Overvoltage protection by crowbar technology
- High noise immunity - static dV/dt > 300 V/µs

Applications

- AC ON/OFF static switching in appliances and industrial control systems
- Drive of low power high inductive or resistive loads like:
  - relay, valve, solenoid,
  - dispenser, door lock
  - micro-motor

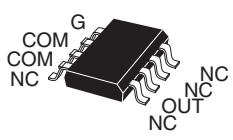
Benefits

- Needs no external protection snubber or varistor.
- Enables equipment to meet IEC 61000-4-5.
- Reduces component count by up to 80%.
- Interfaces directly with the micro-controller.
- Common package tab connection supports connection of several alternating current switches (ACS) on the same cooling pad.
- Integrated structure based on ASD[(a)] technology

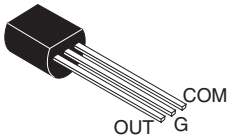
Order code

Part number	Marking
ACS102-6TA	ACS1026T
ACS102-6TA-TR	ACS1026T
ACS102-6T1	ACS1026T
ACS102-6T1-TR	ACS1026T

a. ASD: Application Specific Devices



SO-8
ACS102-6T1



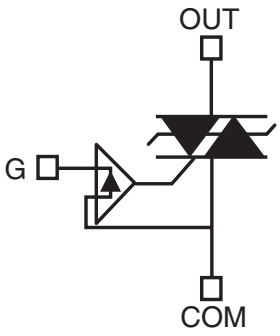
TO-92
ACS102-6TA

Description

The ACS102-6T belongs to the AC line switch family. This high performance switch can control a load of up to 0.2A.

The ACS102-6T switch includes an overvoltage crowbar structure to absorb the overvoltage energy, and a gate level shifter driver to separate the digital controller from the main switch. It is triggered with a negative gate current flowing out of the gate pin.

Functional diagram



COM	Common drive reference to connect to the mains
OUT	Output to connect to the load.
G	Gate input to connect to the controller through gate resistor

TM: ACS is a trademark of STMicroelectronics

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1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25° C, unless otherwise specified)

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	RMS on-state current (full sine wave)	TO-92	T_{amb} = 100° C	0.2	A
		SO-08	T_{amb} = 100° C		
I_{TSM}	Non repetitive surge peak on-state current (full cycle sine wave, T_j initial = 25° C)	f = 60 Hz	t = 16.7 ms	7.6	A
		f = 50 Hz	t = 20 ms	7.3	
I^2t	I^2t Value for fusing	t_p = 10 ms		0.38	A^2s
dI/dt	Critical rate of rise of on-state current $I_G = 2xI_{GT}$, tr ≤ 100 ns	f = 120 Hz	T_j = 125° C	50	A/µs
V_{PP}	Non repetitive line peak mains voltage(1)		T_j = 25° C	2	kV
I_{GM}	Peak gate current	t_p = 20 µs	T_j = 125° C	1	A
V_{GM}	Peak positive gate voltage		T_j = 125° C	10	V
$P_{G(AV)}$	Average gate power dissipation		T_j = 125° C	0.1	W
T_{stg} T_j	Storage junction temperature range Operating junction temperature range			-40 to +150 -30 to +125	°C

1. according to test described by IEC 61000-4-5 standard and *Figure 16*

Table 2. Electrical characteristics (T_j = 25° C, unless otherwise specified)

Symbol	Test conditions	Quadrant		Value	Unit
I_{GT} (1)	V_{OUT} = 12 V, R_L = 33 Ω	II - III	MAX	5	mA
V_{GT}		II - III	MAX	0.9	V
V_{GD}	$V_{OUT} = V_{DRM}$, R_L =3.3 kΩ, T_j = 125° C	II - III	MIN	0.15	V
I_H (2)	I_{OUT} = 100 mA		MAX	20	mA
I_L (2)	$I_G = 1.2 \times I_{GT}$		MAX	25	mA
dV/dt (2)	V_{OUT} = 67% V_{DRM}, gate open, T_j = 125° C		MIN	300	V/µs
(dI/dt)c (2)	Without snubber (15 V/µs), turn-off time ≤ 20 ms, T_j = 125° C		MIN	0.15	A/ms
V_{CL}	I_{CL} = 0.1 mA, t_p = 1 ms, T_j = 125° C		MIN	650	V

1. minimum I_{GT} is guaranteed at 10% of I_{GT} max
2. for both polarities of OUT referenced to COM

Table 3. Static electrical characteristics

Symbol	Test conditions			Value	Unit
V_{TM} (1)	I_{TM}= 0.3 A, t_p = 380 µs	Tj = 25° C	MAX	1.2	V
V_{TO} (1)		Tj = 125° C	MAX	0.80	V
R_D (1)		Tj = 125° C	MAX	500	mΩ
I_{DRM} I_{RRM}	V_{OUT} = 600 V	Tj = 25° C	MAX	2	µA
		Tj = 125° C		0.2	mA

1. for both polarities of OUT referenced to COM

Table 4. Thermal resistance

Symbol	Parameter			Value	Unit
$R_{th\ (j-l)}$	Junction to lead (AC)		TO-92	60	°C/W
$R_{th\ (j-a)}$	Junction to ambient		TO-92	150	
		S = 40 mm²	SO-8	150	

Figure 1. Maximum power dissipation vs RMS on-state current (full cycle)

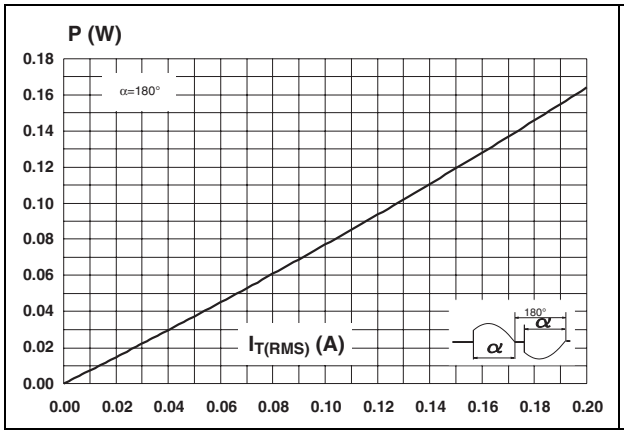


Figure 2. RMS on-state current vs ambient temperature (full cycle)

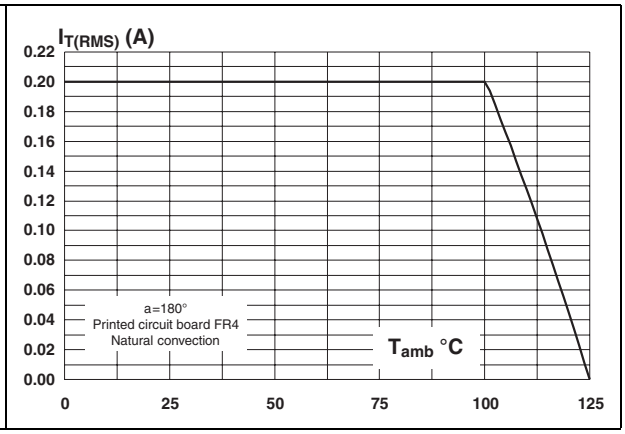


Figure 3. Relative variation of junction to ambient thermal impedance vs pulse duration and package

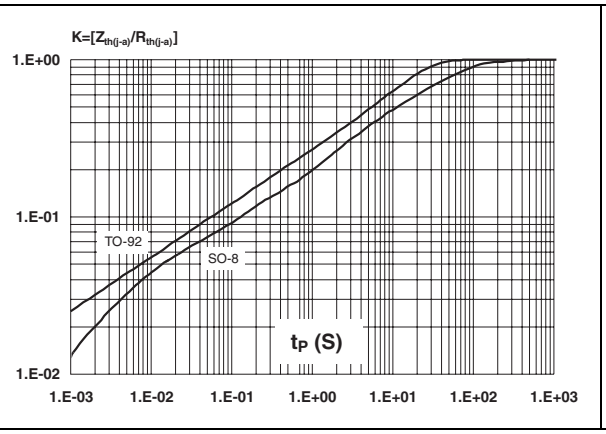


Figure 4. Relative variation of gate trigger current, holding current and latching current vs junction temperature

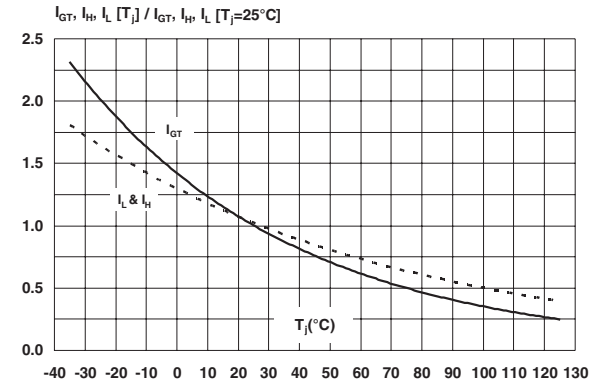


Figure 5. Non repetitive surge peak on-state current vs number of cycles

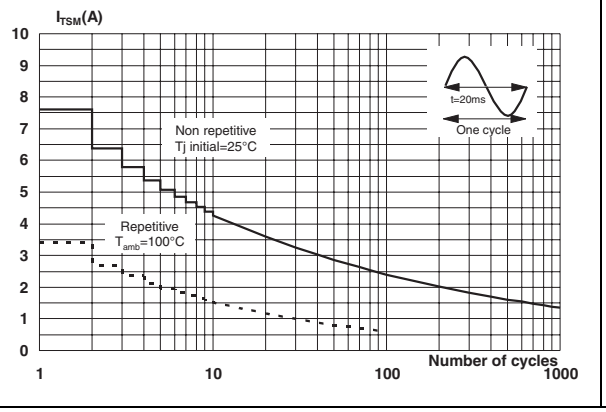


Figure 6. Non repetitive surge peak on-state current for a sinusoidal pulse with width tp<10 ms, and corresponding value of I^2t (T_j initial = 25° C).

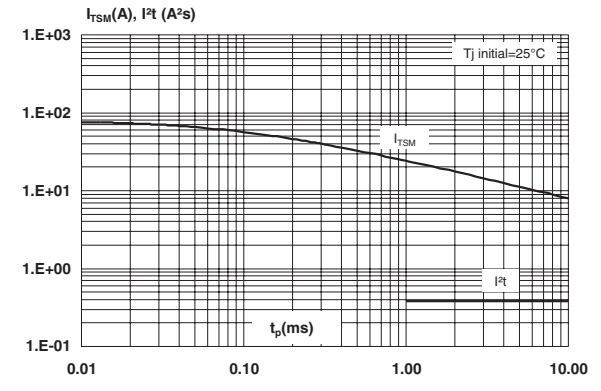


Figure 7. On-state characteristics (maximal values)

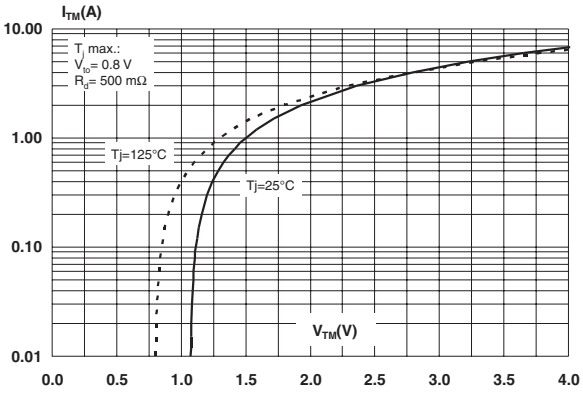


Figure 8. SO-8 junction to ambient thermal resistance versus copper surface under tab (PCB FR4, copper thickness 35 µm)

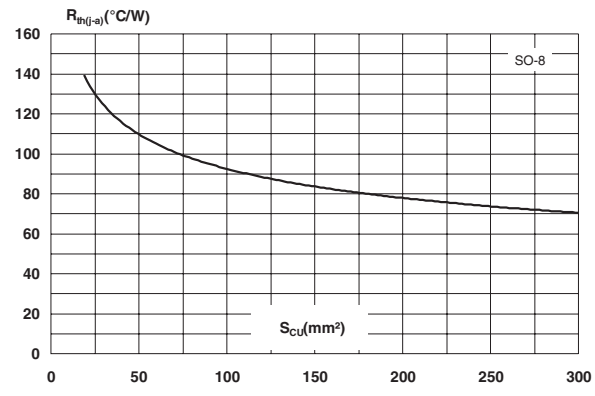


Figure 9. Relative variation of critical rate of decrease of main current (di/dt)c versus junction temperature

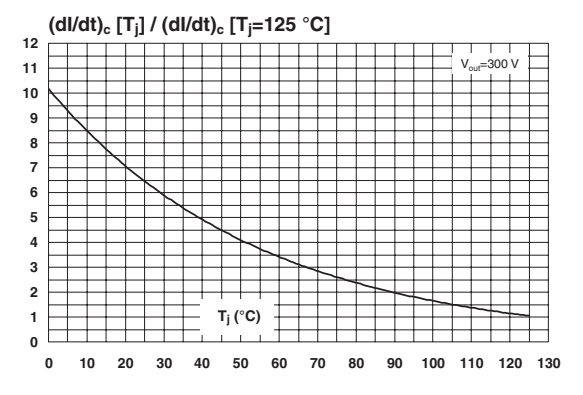


Figure 10. Relative variation of critical rate of decrease of main current (di/dt)c vs (dV/dt)c, with turn-off time < 20 ms

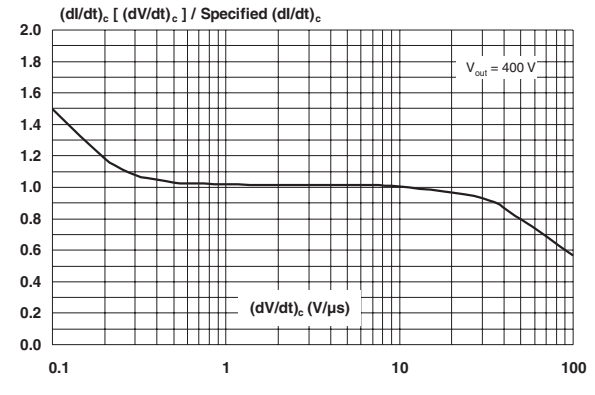


Figure 11. Relative variation of static dV/dt versus junction temperature

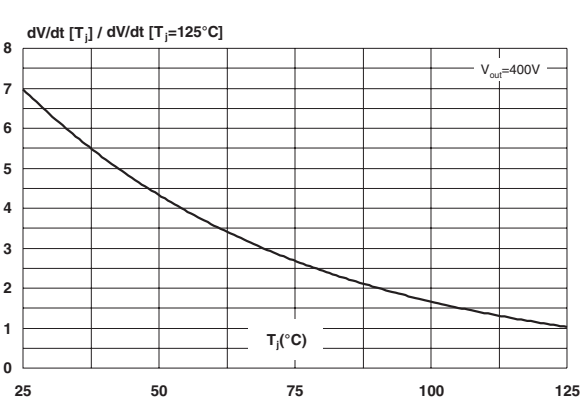
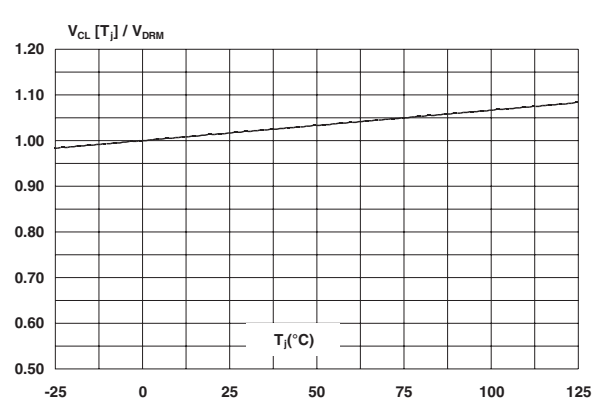


Figure 12. Relative variation of the maximal clamping voltage versus junction temperature (min value)

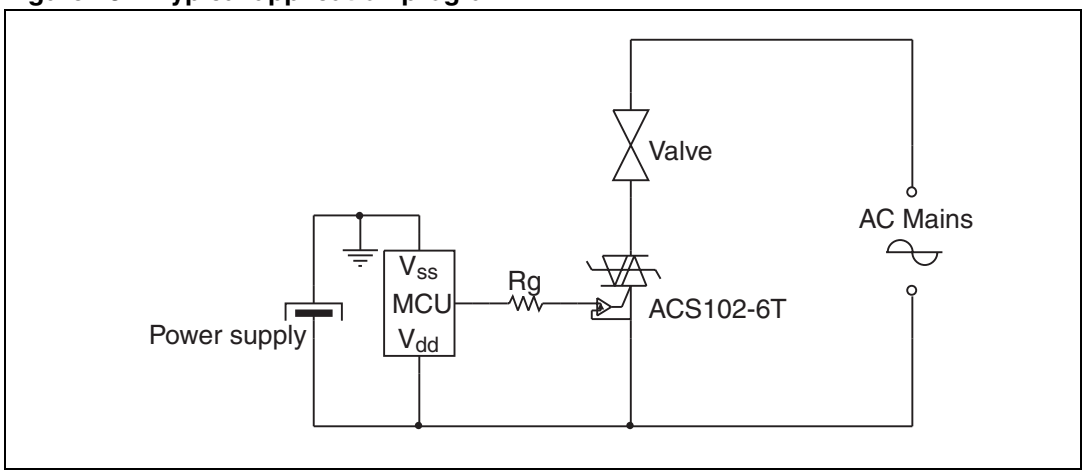


2 AC line switch - basic application

The ACS102-6T switch is triggered by a negative gate current flowing from the gate pin G. The switch can be driven directly by the digital controller through a resistor as shown in *Figure 13*.

Thanks to its overvoltage protection and turn-off commutation performance, the ACS102-6T switch can drive a small power high inductive load with neither varistor nor additional turn-off snubber.

Figure 13. Typical application program



2.1 Protection against overvoltage: the best choice is ACS

In comparison with standard triacs, which are not robust against surge voltage, the ACS102-6T is over-voltage self-protected, specified by the new parameter V_{CL}. This feature is useful in two operating conditions: in case of turn-off of very inductive load, and in case of surge voltage that can occur on the electrical network.

2.1.1 High inductive load switch-off: turn-off overvoltage clamping

With high inductive and low RMS current loads the rate of decrease of the current is very low. An overvoltage can occur when the gate current is removed and the OUT current is lower than I_H.

As shown in *Figure 14* and *Figure 15*, at the end of the last conduction half-cycle, the load current decreases (1). The load current reaches the holding current level I_H (2), and the ACS turns off (3). The water valve, as an inductive load (up to 15 H), reacts as a current generator and an overvoltage is created, which is clamped by the ACS (4). The current flows through the ACS avalanche and decreases linearly to zero. During this time, the voltage across the switch is limited to the clamping voltage V_{CL}. The energy stored in the inductance of the load is dissipated in the clamping section that is designed for this purpose. When the energy has been dissipated, the ACS voltage falls back to the mains voltage value (5).

Figure 14. Effect of the switching off of a high inductive load - typical clamping capability of ACS102-6T

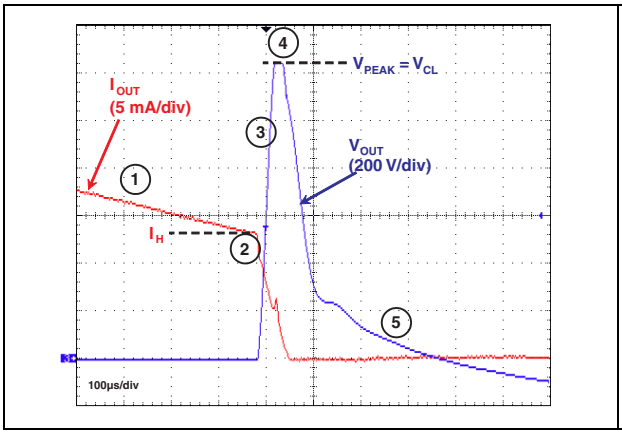
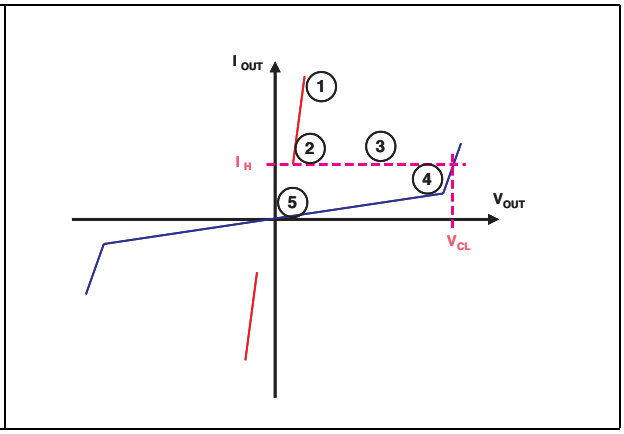


Figure 15. Description of the different steps during switching off of a high inductive load



2.1.2 AC line transient voltage ruggedness

The ACS102-6T switch is able to withstand safely the AC line transients either by clamping the low energy spikes or by breaking over under high energy shocks, even with high turn-on current rises.

The test circuit shown in *Figure 16* is representative of the final ACS102-6T application, and is also used to test the ACS switch according to the IEC 61000-4-5 standard conditions. Thanks to the load limiting the current, the ACS102-6T switch withstands the voltage spikes up to 2 kV above the peak line voltage. The protection is based on an overvoltage crowbar technology. Actually, the ACS102-6T breaks over safely as shown in *Figure 17*. The ACS102-6T recovers its blocking voltage capability after the surge (switch off back at the next zero crossing of the current).

Such non-repetitive tests can be done 10 times on each AC line voltage polarity.

Figure 16. Overvoltage ruggedness test circuit for resistive and inductive loads with conditions equivalent to IEC 61000-4-5 standards

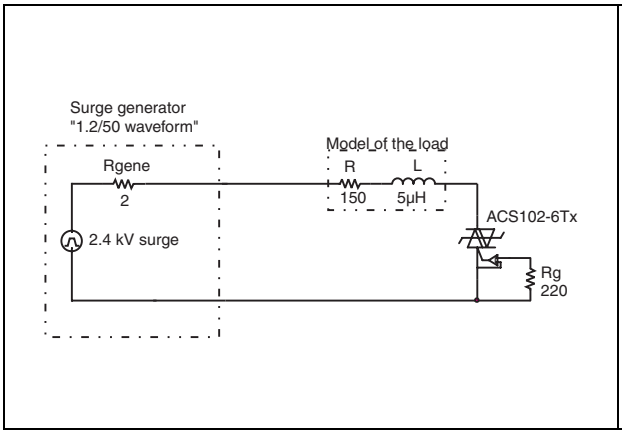
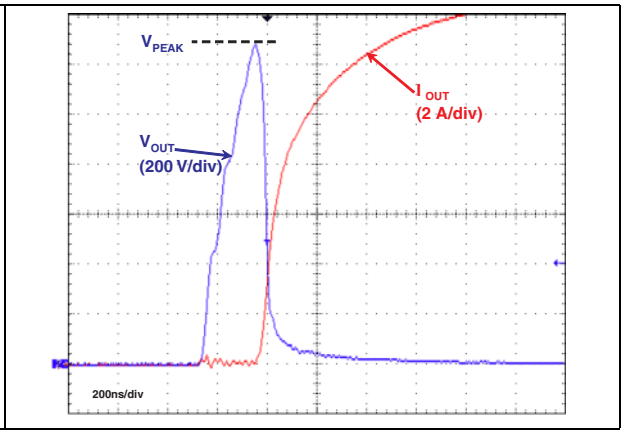
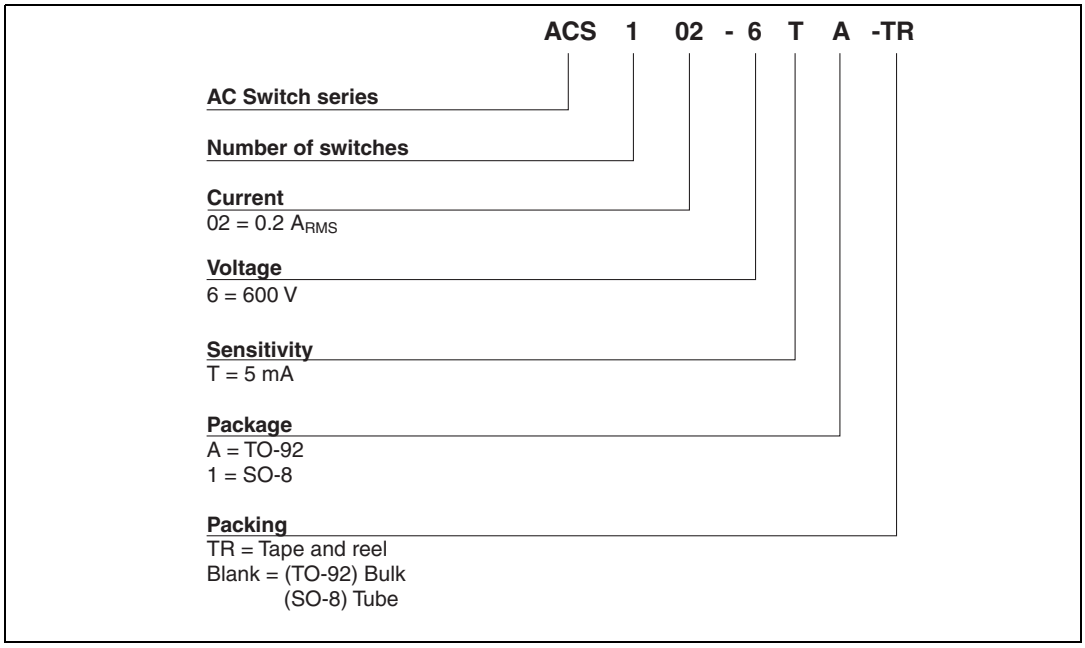


Figure 17. Typical current and voltage waveforms across the ACS102-6T during IEC 61000-4-5 standard test

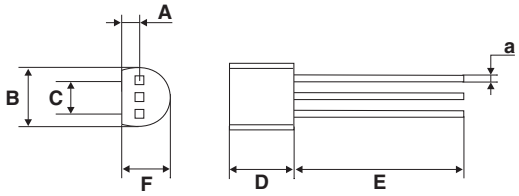


3 Ordering information scheme



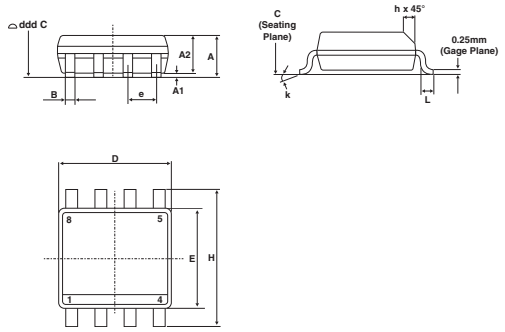
4 Package information

Table 5. TO-92 Mechanical data



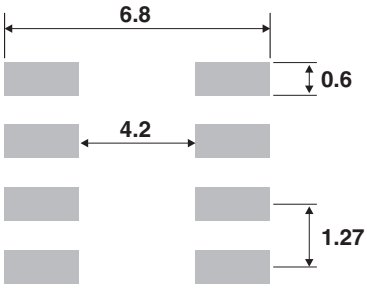
Ref	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		1.35			0.053	
B			4.70			0.185
C		2.54			0.100	
D	4.40			0.173		
E	12.70			0.500		
F			3.70			0.146
a			0.50			0.019

Table 6. SO-8 Mechanical data



REF.	DIMENSIONS					
	Millimetres			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.350		1.75	0.053		0.069
A1	0.100		0.250	0.004		0.010
A2	1.100		1.650	0.043		0.065
B	0.330		0.510	0.013		0.020
C	0.190		0.250	0.008		0.010
D	4.800		5.000	0.189		0.197
E	3.800		4.000	0.150		0.157
e		1.270			0.050	
H	5.800		6.200	0.228		0.244
h	0.250		0.500	0.010		0.020
L	0.400		1.270	0.016		0.050
k	0°		8°	0°		8°
ddd			0.100			0.004

Figure 18. SO-8 Footprint



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

5 Ordering information

Part number	Marking	Package	Weight	Base Qty	Packing mode
ACS102-6TA	ACS1026T	TO-92	0.2 g	2500	Bulk
ACS102-6TA-TR	ACS1026T	TO-92	0.2 g	2000	Tape and Reel
ACS102-6T1	ACS1026T	SO-8	0.11 g	100	Tube
ACS102-6T1-TR	ACS1026T	SO-8	0.11 g	2500	Tape & reel

6 Revision history

Date	Revision	Changes
05-Jan-2006	1	Initial release.
07-Jun-2006	2	Reformatted to current standards. Replaced figure 9.

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