SigmaDSP Digital Audio Processor

Data Sheet

ADAU1472

FEATURES

- 270 MHz, 32-bit Cadence Tensilica HiFi 4 Audio DSP
  - Quad 32-bit × 32-bit MAC support per cycle
  - Single IEEE floating-point multiplier
  - 320 kB L1 SRAM and 160 kB L1 cache
  - Large 2 MB L2 system SRAM
  - Accelerated math instruction extensions
  - C/C++ programmable with complete development toolkit
  - Software compatible with the HiFi DSP family
- Voice detector with low power always listening mode and DSP core wake up
- Low latency audio path
- 4 stereo asynchronous sample rate converters
- Clock oscillator for generating master clock from crystal
- Integer PLL and flexible clock generators
- On-chip regulator for generating 1.2 V from IOVDD supply
- 6 digital audio input and output ports (serial ports) with 32-bit digital input/output supporting 8 kHz to 192 kHz operation
- Flexible serial data configuration with I²S, TDM, left and right justified formats, pulse-code modulation (PCM), and bidirectional modes
- S/PDIF receiver and transmitter—up to 96 kHz sample rate
- 14 digital PDM microphone input channels
- 2 stereo PDM output ports
- SPI flash memory interface—up to 2 GB quad input/output serial flash
- SPI control interfaces—slave and master with single, dual, and quad modes
- I²C master interface
- JTAG debug port
- Boot ROM with self boot from serial memory
- 8 multipurpose pins for digital controls and outputs
- Dedicated event manager for host/driver communication
- 144-ball, 0.5 mm pitch, 6.095 mm × 6.135 mm WLCSP
- 0°C to 85°C temperature range

APPLICATIONS

- Far field voice interface devices
- Audio source separation
- Embedded deep learning for audio
- Commercial and professional audio processing

GENERAL DESCRIPTION

The ADAU1472 is a high quality SigmaDSP® digital audio processor with a large internal memory, enabling efficient audio source separation, far field voice capture, speech processing, deep learning, and advanced audio signal processing. The processor combines the highly optimized Cadence® Tensilica® HiFi® 4 audio/voice processor with custom Analog Devices, Inc., instruction extensions for math acceleration (shown in Table 20 and Table 21), and a flexible input and output architecture. The HiFi 4 processor supports four 32-bit × 32-bit multiplier accumulators (MACs) per cycle with 72-bit accumulators, dual 64-bit memory load, and a native Institute of Electrical and Electronics Engineers (IEEE) single precision, floating-point multiplier.

The ADAU1472 processor offers performance up to 270.336 MHz, supports low latency, sample by sample audio processing, and block by block processing paradigms in parallel. The integer phase-locked loop (PLL) and flexible clock generator hardware can generate up to 15 audio sample rates simultaneously (8 kHz to 192 kHz). These clock generators, along with the on-board asynchronous sample rate converters (ASRCs) and flexible hardware audio routing matrix, greatly simplify the design of complex audio systems.

The HiFi 4 digital signal processor (DSP) core has 480 kB of L1 memory running at the DSP core clock rate, which consists of 256 kB data random access memory (RAM), 64 kB instruction RAM, 128 kB data cache, and 32 kB instruction cache, along with 2 MB of L2 system static random access memory (SRAM) running at one half of the DSP core clock rate. The processor also supports up to 2 GB of external flash memory to enable the storage of large data tables and self boot code.

Dual on-chip power domains allow low power operation, including the capability of routing audio through a flexible audio routing matrix with IOVDD as the only active supply.
The configurable voice detection hardware can detect human speech onset while operating in a low power state and can generate both internal DSP and external wake-up signals.

Continued on Page 4

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REVISION HISTORY

11/2020—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

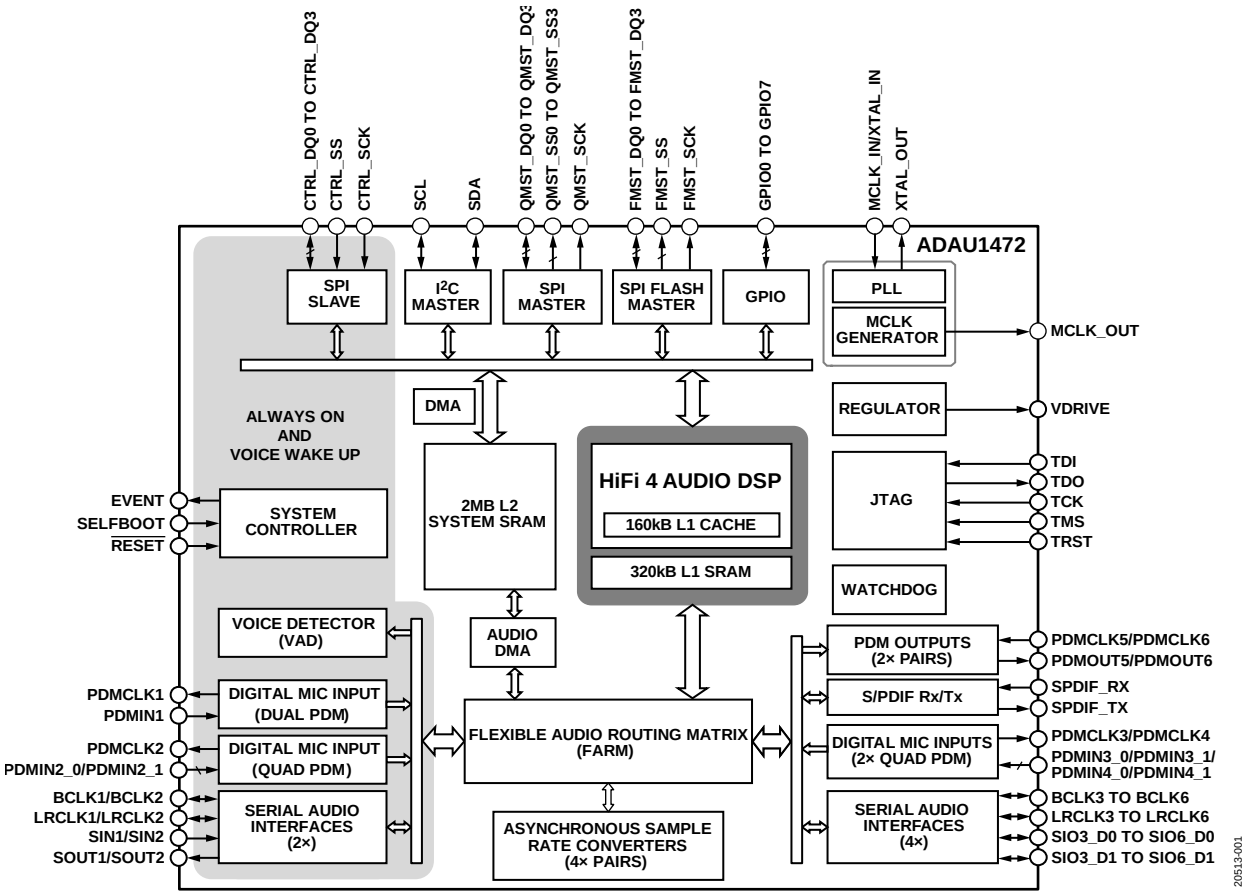


Figure 1.

The ADAU1472 interfaces with a wide range of analog-to-digital converters (ADCs), digital-to-analog converters (DACs), digital audio devices, amplifiers, and control circuitry due to its highly configurable serial ports, Sony/Philips digital interface format (S/PDIF) interfaces, and multipurpose input/output pins. The device can also directly interface with up to 14 pulse density modulated (PDM) output microphones due to integrated decimation filters specifically designed for that purpose. The PDM outputs with integrated interpolation filters provide direct connectivity to PDM input Class D amplifiers.

The processor has two serial peripheral interface (SPI) bus master control ports that allow the device to communicate with multiple SPI-compatible devices including support for single, dual, and quad input/output operation. In addition, the SPI flash port allows direct memory mapped read access with minimal central processing unit (CPU) overhead and standalone self boot operation.

The combined high performance DSP core, large RAM, and small footprint make the ADAU1472 an ideal replacement for large, general-purpose DSPs that consume more power for the same processing load.

Table 1. Processor Features

Processor Feature	Value	Unit
Core Clock	270	MHz
L1 SRAM	320	kB
L1 Cache	160	kB
L2 System SRAM	2	MB

Multifunction pin names may be referenced by their relevant function only.

SPECIFICATIONS

OPERATING CONDITIONS

DVDD = 1.2 V ± 5%, PVDD = 1.2 V ± 5%, IOVDD = 1.8 V − 5% to 3.3 V + 10%, CVDD = 1.2 V ± 5%, T_A = 25°C, MCLK_IN/XTAL_IN = 24.576 MHz, core clock frequency (f_{CORE}) = 270.336 MHz, and input/output pins set to low drive setting, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER					
Supply Voltage					
Digital Voltage (DVDD)	1.14	1.2	1.26	V	Supply for digital circuitry, DSP core, ASRCs, and signal routing
PLL Voltage (PVDD)	1.14	1.2	1.26	V	Supply for PLL circuitry
Input/Output Voltage (IOVDD)	1.71	3.3	3.63	V	Supply for input/output circuitry, including pads and level shifters
Memory Core Voltage (CVDD)					
Operation State[1]	1.14	1.2	1.26	V	Supply for memory circuitry and retention
Power-Down State	0.74	0.8	1.26	V	Supply for memory retention in power-down state
Supply Current					
PLL Current (PVDD)		480		µA	24.576 MHz clock frequency with default PLL settings
Idle State		30		µA	Power applied, PLL not configured
Reset State		7		µA	Power applied, $\overline{\text{RESET}}$ held low
Input/Output Current (IOVDD)					Dependent on active serial ports, clock pins, and external loads
Operation State		20		mA	IOVDD = 3.3 V, all serial ports are clock masters
Reset State		0.6		mA	IOVDD = 3.3 V, $\overline{\text{RESET}}$ held low
Digital Current (DVDD)[1]					
Maximum Program		210		mA	100% CPU utilization, PLL = 270.336 MHz
Typical Program		140		mA	60% CPU utilization, PLL = 270.336 MHz
Idle State		40		mA	Power applied, DSP idle (WAITI)[2], PLL = 270.336 MHz
Minimal Program		25		mA	60% CPU utilization, direct MCLK 24.576 MHz
Reset State		5		mA	Power applied, $\overline{\text{RESET}}$ held low
Circuit Voltage (CVDD)[1]					
Operation State		100		µA	
Memory Retention State		690		µA	CVDD = 1.2 V
		590		µA	CVDD = 0.8 V, power-down state with IOVDD not powered
ASRCs					
Dynamic Range		139		dB	A-weighted, 20 Hz to 20 kHz
Input/Output Sample Rate	8		192	kHz	
Input/Output Sample Rate Ratio	1:8		7.75:1		
Total Harmonic Distortion Plus Noise (THD + N)			−120	dB	
REGULATOR					
DVDD Voltage	1.14	1.2		V	Regulator maintains typical output voltage up to a maximum 800 mA load
CRYSTAL OSCILLATOR					
Transconductance	9.5	11.7	13.8	mS	

[1] CVDD must remain powered when supplying DVDD or it may cause permanent damage to the device. The ADAU1472 supports a low power, memory retention mode. To use memory retention, disconnect DVDD and supply CVDD only with either 1.2 V or 0.8 V.

[2] WAITI is the assembly language command that tells the processor to power down and wait for an interrupt. In this case, WAITI describes that the chip was set to DSP idle by using the WAITI command.

ELECTRICAL CHARACTERISTICS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL INPUT/OUTPUT						
Input Voltage[1]						
High Level	V_{IH}	1.70		3.3	V	IOVDD = 3.3 V
		0.96		1.8	V	IOVDD = 1.8 V
Low Level	V_{IL}	0		1.65	V	IOVDD = 3.3 V
		0		0.88	V	IOVDD = 1.8 V
Output Voltage						
High Level	V_{OH}	3.09		3.3	V	IOVDD = 3.3 V, high output current (I_{OH}) = 1 mA
		1.45		1.8	V	IOVDD = 1.8 V
Low Level	V_{OL}	0		0.26	V	IOVDD = 3.3 V, I_{OH} = 1 mA
		0		0.33	V	IOVDD = 1.8 V
Input Leakage						
High Level	I_{IH}					
		−2		+2	µA	Digital input pins with pull-up resistor [2]
		1		12	µA	Digital input pins with pull-down resistor[2]
		−2		+2	µA	Digital input pins with no pull resistor[2]
		−2		+2	µA	MCLK_IN/XTAL_IN
		48		120	µA	SPDIF_RX
Low Level	I_{IL}					
		−12		−3	µA	Digital input pins with pull-up resistor at 0 V[2]
		−2		+2	µA	Digital input pins with pull-down resistor at 0 V[2]
		−2		+2	µA	Digital input pins with no pull resistor at 0 V[2]
		−2		+2	µA	MCLK_IN/XTAL_IN at 0 V
		−125		−49	µA	SPDIF_RX at 0 V
Input Capacitance	C_{IN}		2		pF	Guaranteed by design, T_A = 25°C
Digital Output Drive[3]				2		Driving low impedance printed circuit board (PCB) traces into a high impedance digital input buffer
IOVDD = 1.8 V						
Lowest Drive Strength Setting				1	mA	
Low Drive Strength Setting				2	mA	
High Drive Strength Setting				3	mA	
Highest Drive Strength Setting				5	mA	
IOVDD = 3.3 V						
Lowest Drive Strength Setting				2	mA	
Low Drive Strength Setting				5	mA	
High Drive Strength Setting				10	mA	
Highest Drive Strength Setting				15	mA	

[1] Digital input pins except SPDIF_RX, which is not a standard digital input.

[2] The digital input pins include the following: BCLKx, MCLK_IN/XTAL_IN, PDMIN1, LRCLKx, SINx, SPDIF_RX, $\overline{\text{RESET}}$, CTRL_DQx, CTRL_SCK, CTRL_SS, PDMIN2_x, SELFBOOT, TRST, TRST_DEBUG, GPIOx, TMS, SIO3_Dx, TMS_DEBUG, SIO5_Dx, TDI, SIO4_Dx, TDI_DEBUG, SDA, TCK, TCK_DEBUG, SCL, SIO6_Dx, PDMIN3_x, QMST_DQx, PDMCLK5, PDMIN4_x, FMST_DQx, and PDMCLK6.

[3] The digital output pins, or all pins listed as output or I/O in Table 19, are not designed for static current draw. Do not use these pins to drive light emitting diodes (LEDs) directly. The digital output pins include: PDMCLKx, BCLKx, SOUTx, VDRIVE, XTAL_OUT, LRCLKx, SPDIF_TX, CVDD_ON, DVDD_ON, CTRL_DQx, MCLK_OUT, EVENT, GPIOx, SIO3_Dx, TDO, SIO5_Dx, TDO_DEBUG, SIO4_Dx, SDA, SCL, QMST_SSx, SIO6_Dx, QMST_DQx, QMST_SCK, PDMOUT5, FMST_DQx, FMST_SS, PDMOUT6, and FMST_SCK.

POWER CONSUMPTION CHARACTERISTICS

Table 4 details power consumption estimates for various operation use cases. T_A = 25°C, MCLK_IN = 24.576 MHz, DVDD = 1.2 V, PVDD = 1.2 V, IOVDD = 3.3 V, and CVDD = 1.2 V, unless otherwise noted.

The estimates are only for the internal logic power consumption. Total system power consumption includes additional IOVDD current, which is highly dependent on the active pins, drive strength settings, and external loads.

Table 4. Power Dissipation Estimates

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER CONSUMPTION					
Lowest Power Voice Detect		10		mW	IOVDD supply only, DVDD supply turned off, DSP off
Direct MCLK, 12.288 MHz		26		mW	DSP core clock domain (SYSCLK) = 12.288 MHz, memory bus clock domain (BUSCLK) = 12.288 MHz, 100% DSP utilization, PLL off (SYSCLK = master clock (MCLK))
Direct MCLK, 24.576 MHz, DSP Idle		25		mW	SYSCLK = 24.576 MHz, BUSCLK = 24.576 MHz, DSP idle (WAITI), PLL off (SYSCLK = MCLK)
Direct MCLK, 24.576 MHz		42		mW	SYSCLK = 24.576 MHz, BUSCLK = 24.576 MHz, 100% DSP utilization, PLL off (SYSCLK = MCLK), lowest power voice trigger word
PLL, 270.336 MHz, DSP Idle		65		mW	SYSCLK = 270.336 MHz, BUSCLK = 135.183 MHz, DSP idle (WAITI), PLL on
Full DSP Utilization		270		mW	SYSCLK = 270.336 MHz, BUSCLK = 135.183 MHz, 100% DSP utilization, PLL on, 2:1 system/bus clock ratio

Table 5 details an estimate for worst case power consumption in a typical use case. DVDD = 1.26 V, PVDD = 1.26 V, IOVDD = 3.6 V, and CVDD = 1.26 V, unless otherwise noted. See the Total Power Dissipation section for more information.

Table 5. Maximum Power Dissipation

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MAXIMUM POWER DISSIPATION					
T_A = 25°C		350		mW	100% DSP utilization, all ASRCs active, all supplies at maximum
T_A = 70°C		420		mW	

TIMING SPECIFICATIONS

Master Clock Input

T_A = 0°C to 70°C, DVDD = 1.2 V ± 5%, CVDD = 1.2 V ± 5%, and IOVDD = 1.8 V − 5% to 3.3 V + 10%, unless otherwise noted.

Table 6.

Parameter	Min	Typ	Max	Unit	Description
MASTER CLOCK INPUT (MCLK_IN/XTAL_IN)					
f_{MCLK}	12.288		24.576	MHz	MCLK_IN/XTAL_IN frequency, IOVDD = 1.8 V
	12.288		24.576	MHz	MCLK_IN/XTAL_IN frequency, IOVDD = 3.3 V
t_{MCLK}	40.69		81.38	ns	MCLK_IN/XTAL_IN period
t_{MCLKD}	30		70	%	MCLK_IN/XTAL_IN duty cycle, not shown in Figure 2
t_{MCLKH}	0.25 × t_{MCLK}		0.75 × t_{MCLK}	ns	MCLK_IN/XTAL_IN width high
t_{MCLKL}	0.25 × t_{MCLK}		0.75 × t_{MCLK}	ns	MCLK_IN/XTAL_IN width low
SYSTEM CLOCK					
f_{CORE}	12.288		270.336	MHz	System (DSP core) clock frequency
	3.699			ns	System (DSP core) clock period

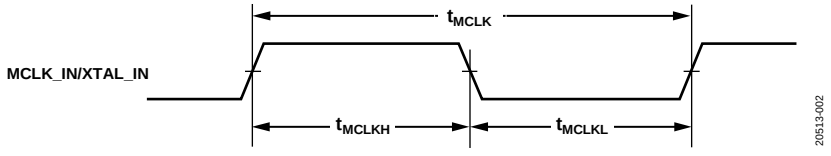


Figure 2. Master Clock Input Timing Specifications

Reset

T_A = 0°C to 70°C, DVDD = 1.2 V ± 5%, CVDD = 1.2 V ± 5%, and IOVDD = 1.8 V − 5% to 3.3 V + 10%.

Table 7.

Parameter	Min	Typ	Max	Unit	Description
$\overline{\text{RESET}}$					
t_{WRST}	500			ns	Reset pulse width low

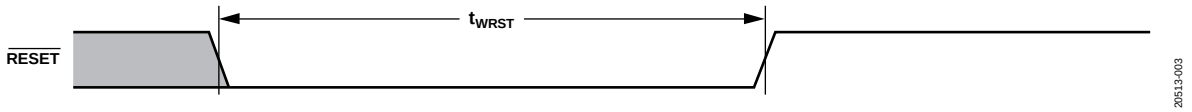


Figure 3. Reset Timing Specification

Serial Ports

T_A = 0°C to 70°C, DVDD = 1.2 V ± 5%, CVDD = 1.2 V ± 5%, and IOVDD = 1.8 V − 5% to 3.3 V + 10%, unless otherwise noted.

Table 8.

Parameter	Min	Typ	Max	Unit	Description[1]
SERIAL PORT					
f_{LRCLK}			192	kHz	LRCLKx frequency, not shown in figures
t_{LRCLK}	5.21			µs	LRCLKx period
f_{BCLK}			24.576	MHz	BCLKx frequency, sample rate ranging from 8 kHz to 192 kHz, not shown in figures
t_{BCLK}	40.7			ns	BCLKx period
t_{BIL}	10			ns	BCLKx low pulse width, slave mode; BCLKx frequency = 24.576 MHz; BCLKx period = 40.6 ns
t_{BIH}	14.5			ns	BCLKx high pulse width, slave mode; BCLKx frequency = 24.576 MHz; BCLKx period = 40.6 ns
t_{LIS}	20			ns	LRCLKx setup to BCLK_INx input rising edge, slave mode; LRCLKx frequency = 192 kHz
t_{LIH}	5			ns	LRCLKx hold from BCLK_INx input rising edge, slave mode; LRCLKx frequency = 192 kHz
t_{SIS}	5			ns	SDATA_INx setup to BCLK_INx input rising edge
t_{SIH}	5			ns	SDATA_INx hold from BCLK_INx input rising edge
t_{TS}			10	ns	BCLK_OUTx output falling edge to LRCLK_OUTx output timing skew, slave
t_{SODS}			35	ns	SDATA_OUTx delay in slave mode from BCLK_OUTx output falling edge; serial outputs function in slave mode at all valid sample rates, provided that the external circuit design provides sufficient electrical signal integrity
t_{SODM}			10	ns	SDATA_OUTx delay in master mode from BCLK_OUTx output falling edge
t_{TM}			5	ns	BCLK falling edge to LRCLK timing skew, master

[1] BCLK_INx is bit clock input, and x is the serial port that it is associated with. Note this is only when BCLK is configured as an input. In addition, SDATA_INx is the serial data input, LRCLK_OUTx is the left/right clock output, SDATA_OUTx is the seral data output, and BCLK_OUTx is the bit clock output.

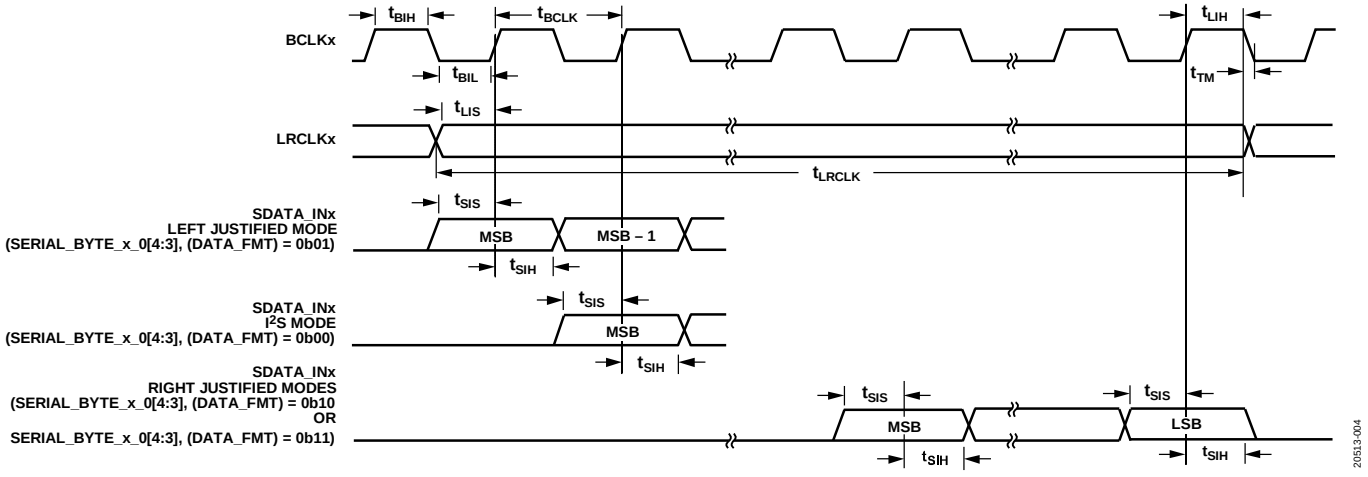


Figure 4. Serial Input Port Timing Specifications

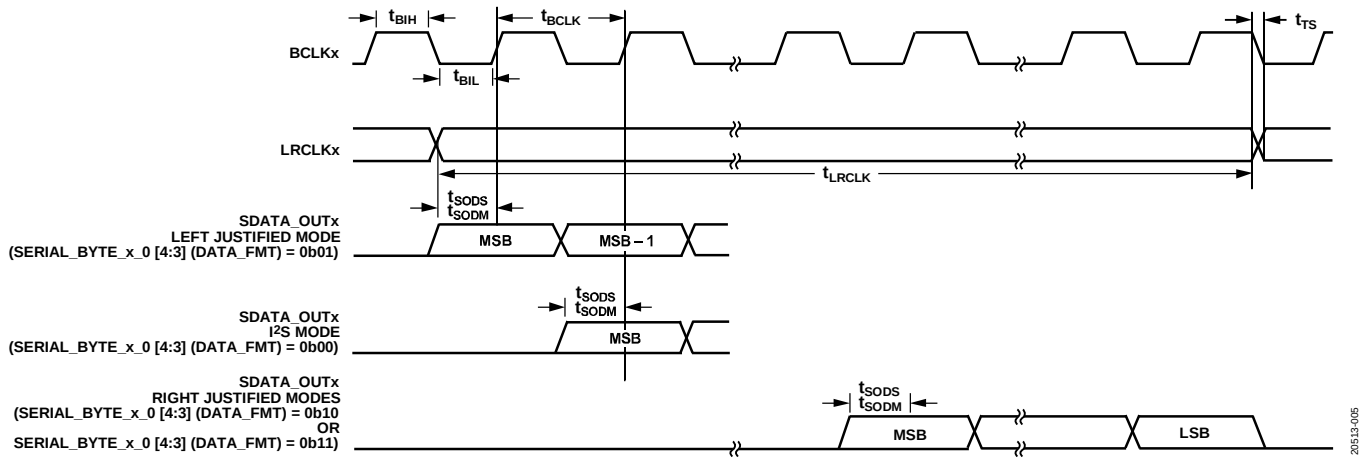


Figure 5. Serial Output Port Timing Specifications

GPIOx Pins

T_A = 0°C to 70°C, DVDD = 1.2 V ± 5%, CVDD = 1.2 V ± 5%, and IOVDD = 1.8 V − 5% to 3.3 V + 10%.

Table 9.

Parameter	Min	Typ	Max	Unit	Description
GENERAL-PURPOSE INPUT/OUTPUT PINS (GPIOx)					
General-Purpose Frequency (f_{GP})[1]			1.0	MHz	Maximum switching rate of general-purpose input or output

[1] Guaranteed by design.

S/PDIF Transmitter

T_A = 0°C to 70°C, DVDD = 1.2 V ± 5%, CVDD = 1.2 V ± 5%, and IOVDD = 1.8 V − 5% to 3.3 V + 10%.

Table 10.

Parameter	Min	Typ	Max	Unit	Description
S/PDIF TRANSMITTER					
Audio Sample Rate	18		96	kHz	Audio sample rate of data output from S/PDIF transmitter

S/PDIF Receiver

T_A = 0°C to 70°C, DVDD = 1.2 V ± 5%, CVDD = 1.2 V ± 5%, and IOVDD = 1.8 V − 5% to 3.3 V + 10%.

Table 11.

Parameter	Min	Typ	Max	Unit	Description
S/PDIF RECEIVER					
Audio Sample Rate	18		96	kHz	Audio sample rate of data input to S/PDIF receiver

PDM Inputs

T_A = 0°C to 70°C, DVDD = 1.2 V ± 5%, CVDD = 1.2 V ± 5%, and IOVDD = 1.8 V − 5% to 3.3 V + 10%.

Table 12.

Parameter	Min	Typ	Max	Unit	Description
TIMING REQUIREMENTS					
t_{SETUP}	20			ns	Data setup time
t_{HOLD}	5			ns	Data hold time

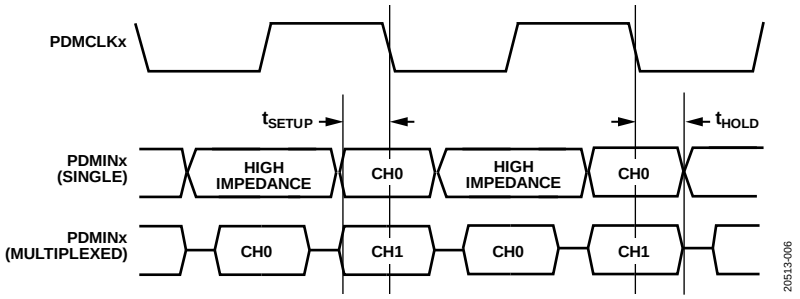


Figure 6. PDM Input Timing Diagram

PDM Outputs

T_A = 0°C to 70°C, DVDD = 1.2 V ± 5%, CVDD = 1.2 V ± 5%, IOVDD = 1.8 V − 5% to 3.3 V + 10%, and PDMCLKx = 3.027 MHz.

Table 13.

Parameter	Min	Typ	Max	Unit	Description
TIMING REQUIREMENTS					
t_{ENABLE}	10			ns	Data driven after clock edge
t_{HOLD}	5		11	ns	Data hold time

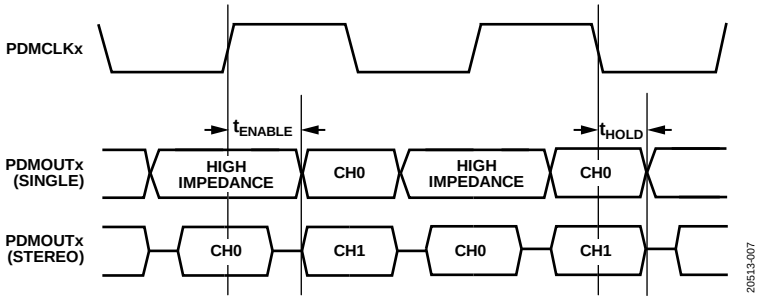


Figure 7. PDM Output Timing Diagram

I²C Interface—Master

T_A = 0°C to 70°C, DVDD = 1.2 V ± 5%, CVDD = 1.2 V ± 5%, and IOVDD = 1.8 V − 5% to 3.3 V + 10%.

Table 14.

Parameter	Min	Typ	Max	Unit	Description
I²C MASTER PORT					
f_{SCL}			500	kHz	SCL clock frequency
t_{SCLH}	0.6			µs	SCL pulse width high
t_{SCLL}	1.3			µs	SCL pulse width low
t_{SCS}	0.6			µs	Start and repeated start condition setup time
t_{SCH}	0.6			µs	Start condition hold time
t_{DS}	100			ns	Data setup time
t_{DH}	0.9			µs	Data hold time
t_{SCLR}			300	ns	SCL rise time
t_{SCLF}			300	ns	SCL fall time
t_{SDR}			300	ns	SDA rise time
t_{SDF}			300	ns	SDA fall time
t_{BFT}	1.3			µs	Bus free time between stop and start
t_{SUSTO}	0.6			µs	Stop condition setup time

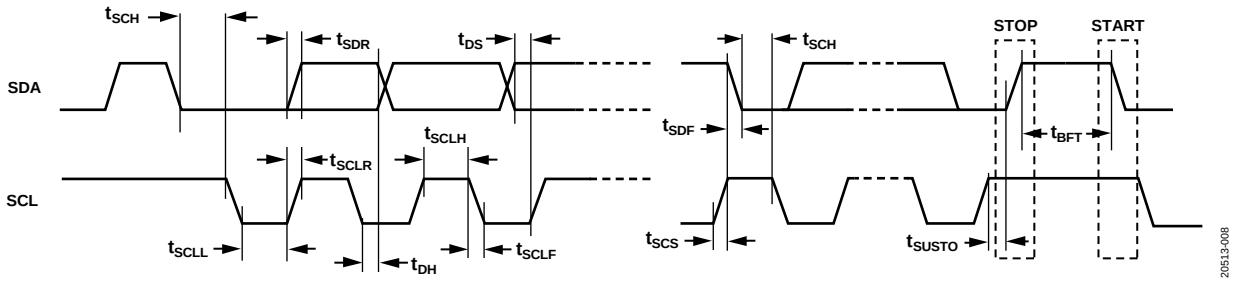


Figure 8. I²C Master Port Timing Specifications

SPI Interface—Slave

T_A = 0°C to 70°C, DVDD = 1.2 V ± 5%, CVDD = 1.2 V ± 5%, and IOVDD = 1.8 V − 5% to 3.3 V + 10%.

Table 15.

Parameter	Min	Typ	Max	Unit	Description
SPI SLAVE PORT					
$f_{SCK_{WRITE}}$	1.7		24.576	MHz	CTRL_SCLK write frequency, cannot exceed MCLK frequency
$f_{SCK_{READ}}$	1.7		12.288	MHz	CTRL_SCLK read frequency, cannot exceed (0.5 × MCLK) frequency
t_{SPICHS}	21			ns	CTRL_SCLK high period (0.5 × 1/f_{SCK} − 1)
t_{SPICLS}	6			ns	CTRL_SCLK low period (0.5 × 1/f_{SCK} − 1)
t_{SPICLK}	49			ns	CTRL_SCLK period (1/f_{SCK} − 1)
t_{HDS}	1			ns	Last CTRL_SCLK edge to CTRL_SS not asserted
t_{SPITDS}	49			ns	Sequential transfer delay (1/f_{SCK} − 1)
t_{SDSCI}	10			ns	CTRL_SS assertion to first CTRL_SCLK edge
t_{SSPID}	1			ns	Data input valid to CTRL_SCLK edge (data input setup)
t_{HSPID}	2			ns	CTRL_SCLK sampling edge to data input invalid

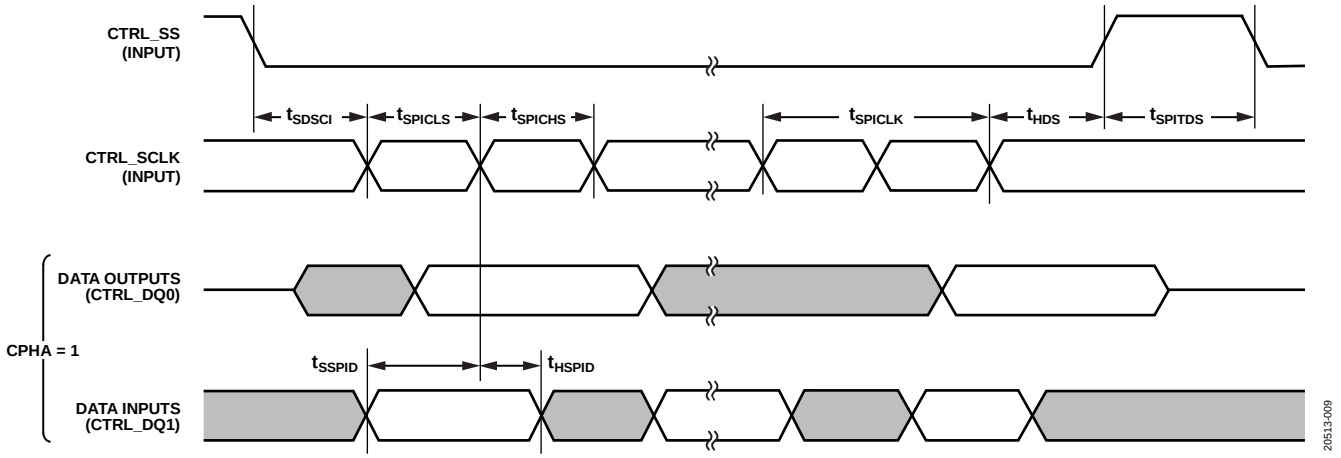


Figure 9. SPI Slave Port Timing Specification

SPI Interface—Master

T_A = 0°C to 70°C, DVDD = 1.2 V ± 5%, CVDD = 1.2 V ± 5%, and IOVDD = 1.8 V − 5% to 3.3 V + 10%.

Table 16.

Parameter	Min	Typ	Max	Unit	Description
SPI MASTER PORT					
f_{SCLK}			24.576	MHz	SPI master clock frequency (QMST_SCK, FMST_SCK)
t_{SSPIDM}	15			ns	Data input valid to QMST_SCK/FMST_SCK edge (data input setup)
t_{HSPIDM}	5			ns	QMST_SCK/FMST_SCK sampling edge to data input invalid
t_{SDSCIM}	38			ns	QMST_SSx/FMST_SS low to first QMST_SCK/FMST_SCK edge ($1/f_{SCLK} - 2$)
t_{SPICLM}	19			ns	QMST_SCK/FMST_SCK low period ($0.5 \times 1/f_{SCLK} - 1$)
t_{SPICHM}	19			ns	QMST_SCK/FMST_SCK high period ($0.5 \times 1/f_{SCLK} - 1$)
t_{SPICLK}	39			ns	QMST_SCK/FMST_SCK period ($1/f_{SCLK} - 1$)
t_{HDSM}	38			ns	Last QMST_SCK/FMST_SCK edge to QMST_SSx/FMST_SS high ($1/f_{SCLK} - 2$)
t_{SPITDM}	39			ns	Sequential transfer delay ($1/f_{SCLK} - 1$)
$t_{HDSPIDM}$	0			ns	QMST_SCK/FMST_SCK edge to data out valid (data out hold)
$t_{DDSPIDM}$			5	ns	QMST_SCK/FMST_SCK edge to data out invalid (data out delay)

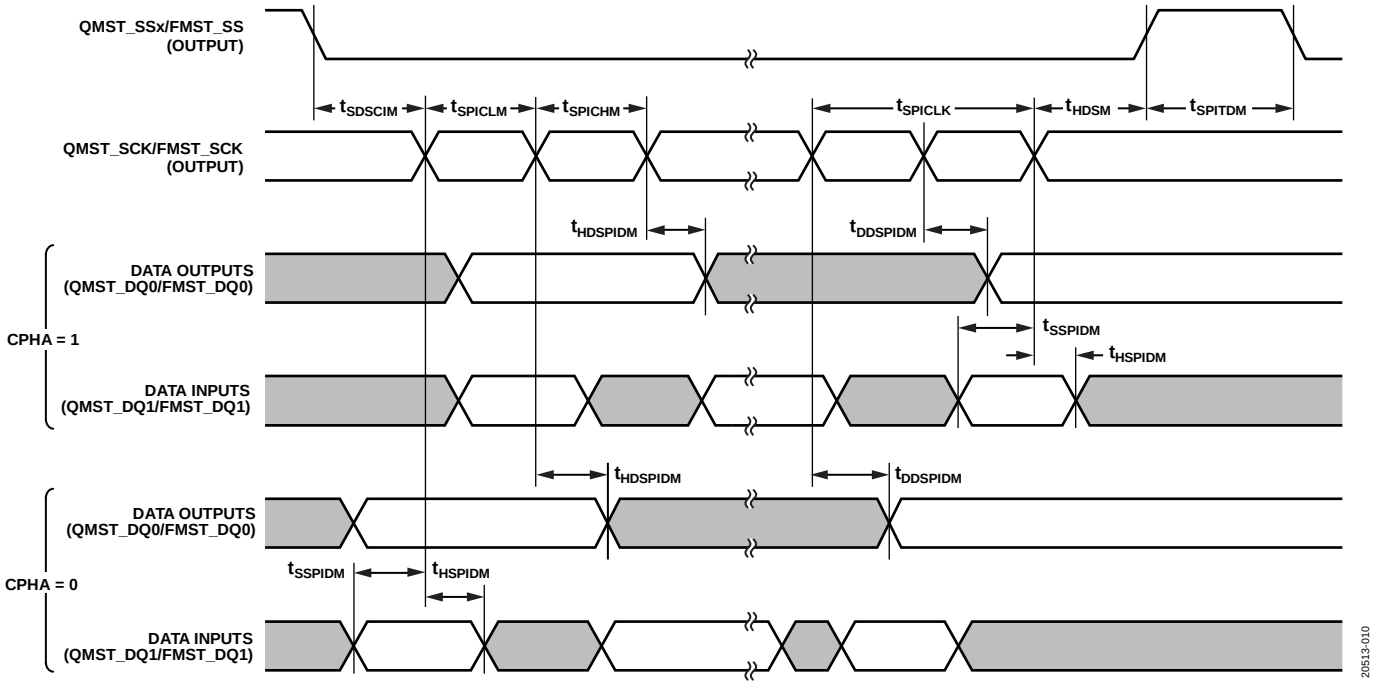


Figure 10. SPI Master Port Timing Specifications

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 17.

Parameter	Rating
DVDD to Ground	0 V to 1.4 V
CVDD to Ground	0 V to 1.4 V
IOVDD to Ground	0 V to 4.0 V
PVDD to Ground	0 V to 4.0 V
Digital Inputs	DGND − 0.3 V to IOVDD + 0.3 V
Temperature	
Ambient Range	0°C to 70°C
Junction Range	0°C to 85°C
Storage Range	−65°C to +150°C
Soldering (10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal resistance values specified in Table 18 are simulated based on JEDEC specifications, unless specified otherwise, and must be used in compliance with JESD51-12.

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} represents the junction to ambient thermal resistance and is specified for recommended conditions, that is, a device soldered on a 4-layer circuit board with filled internal and external planes. $\theta_{JC(TOP)}$ is junction to case (top) and θ_{JB} is junction to board.

Table 18. Thermal Resistance

Package Type	θ_{JA}	$\theta_{JC(TOP)}$[2]	θ_{JB}	Ψ_{JT}	Ψ_{JB}	Unit
CB-144-2[1]	25.01	0.064	1.42	0.024	1.46	°C/W

[1] Using enhanced heat removal (such as PCB, heat sink, and airflow) technique improves thermal resistance values.
[2] For θ_{JC} test, 100 µm thermal interface material (TIM) is used. TIM is assumed to have 3.6 W/mK.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

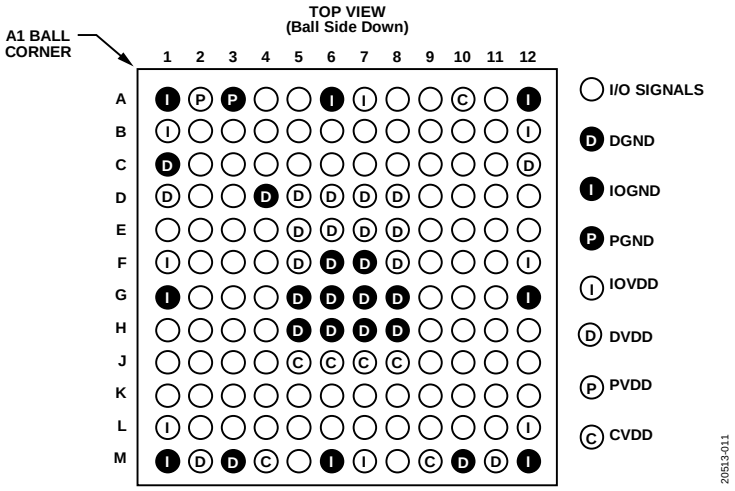


Figure 11. Ball Configuration, Top View (Not to Scale)

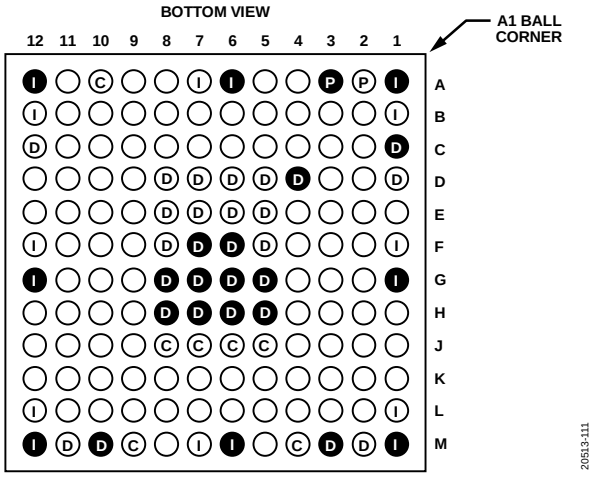


Figure 12. Ball Configuration, Bottom View (Not to Scale)

Table 19. Ball Function Descriptions

Ball No.	Mnemonic	Type[1]	Internal Termination[2]	Description
A1	IOGND	Ground	None	Input/Output Ground Reference. Tie all DGND, IOGND, and PGND pins directly together in a common ground plane.
A2	PVDD	Power	None	PLL Supply, 1.2 V ± 5%. This ball can be supplied externally or by using the internal regulator and external pass transistor. Bypass this ball with decoupling capacitors to PGND.
A3	PGND	Ground	None	PLL Ground Reference. Tie all DGND, IOGND, and PGND pins directly together in a common ground plane.
A4	PDMCLK1	Output	Pull-down	PDM Input 1 Clock. Drives the PDM reference clock. The PDM inputs are always clock slaves.
A5	BCLK2	I/O	Pull-down	Serial Port 2 Bit Clock. Data and frame clock are driven or sampled with respect to this clock. Input is in slave mode, and output is in master mode. Disconnect this ball when not in use.
A6	IOGND	Ground	None	Input/Output Ground Reference. Tie all DGND, IOGND, and PGND pins directly together in a common ground plane.
A7	IOVDD	Power	None	Input/Output Supply, 1.8 V – 5% to 3.3 V + 10%. Bypass this ball with decoupling capacitors to IOGND.
A8	SOUT1	Output	Pull-down	Serial Port 1 Output Data. This ball is configurable from one to eight channels of data. Disconnect this ball when not in use.

Ball No.	Mnemonic	Type[1]	Internal Termination[2]	Description
A9	BCLK1	I/O	Pull-down	Serial Port 1 Bit Clock. Data and frame clock are driven or sampled with respect to this clock. Input is in slave mode, and output is in master mode. Disconnect this ball when not in use.
A10	CVDD	Power	None	Memory Circuitry Supply, 1.2 V ± 5%. This ball can be supplied externally or by using the internal regulator and external pass transistor. Bypass this ball with decoupling capacitors to IOGND.
A11	VDRIVE	Output	None	PNP Bipolar Junction Transistor Base Drive Bias Ball for the Digital Supply Regulator. Connect VDRIVE to the base of an external PNP pass transistor (the STD2805 is recommended). If an external supply is provided directly to DVDD, use a 10 kΩ pull-down resistor to ground on the VDRIVE pin.
A12	IOGND	Ground	None	Input/Output Ground Reference. Tie all DGND, IOGND, and PGND pins directly together in a common ground plane.
B1	IOVDD	Power	None	Input/Output Supply, 1.8 V − 5% to 3.3 V + 10%. Bypass this ball with decoupling capacitors to IOGND.
B2	XTAL_OUT	Output	None	Crystal Oscillator. Circuit output. Disconnect this ball when not in use.
B3	MCLK_IN/XTAL_IN	Input	None	Reference Master Clock Input.
B4	PDMIN1	Input	Pull-down	PDM Input 1 Data.
B5	LRCLK2	I/O	Pull-down	Serial Port 2 Frame Clock. Input is in slave mode, and output is in master mode. Disconnect this ball when not in use.
B6	SIN2	Input	Pull-down	Serial Port 2 Data Input. This ball is configurable from one to eight channels of data. Disconnect this ball when not in use.
B7	SOUT2	Output	Pull-down	Serial Port 2 Data Output. This ball is configurable from one to eight channels of data. Disconnect this ball when not in use.
B8	SIN1	Input	Pull-down	Serial Port 1 Data Input. This ball is configurable from one to eight channels of data. Disconnect this ball when not in use.
B9	LRCLK1	I/O	Pull-down	Serial Port 1 Frame Clock. Input is in slave mode, and output is in master mode. Disconnect this ball when not in use.
B10	SPDIF_RX	Input	None	S/PDIF Receiver. This ball is the input to the integrated S/PDIF receiver. Disconnect this ball when not in use. This ball is internally biased.
B11	SPDIF_TX	Output	Pull-down	S/PDIF Transmitter. This ball is output from the integrated S/PDIF transmitter. Disconnect this ball when not in use.
B12	IOVDD	Power	None	Input/Output Supply, 1.8 V − 5% to 3.3 V + 10%. Bypass this ball with decoupling capacitors to IOGND.
C1	DGND	Ground	None	Digital Ground. Tie all DGND, IOGND, and PGND pins directly together in a common ground plane.
C2	$\overline{\text{RESET}}$	Input	Pull-down	Active Low Reset Input. A reset is triggered on a high to low edge and exited on a low to high edge.
C3	CVDD_ON	Output	None	External CVDD Supply Trigger. This ball requests an external supply to turn the CVDD ball power on or off (active high).
C4	DVDD_ON	Output	None	External DVDD Supply Trigger. This ball requests an external supply to turn the DVDD ball power on or off (active high).
C5	CTRL_DQ3	I/O	Pull-down	SPI Slave Data 3. This ball transfers serial data in quad mode. Disconnect this ball when not in use.
C6	CTRL_DQ2	I/O	Pull-down	SPI Slave Data 2. This ball transfers serial data in quad mode. Disconnect this ball when not in use.
C7	CTRL_DQ1	I/O	Pull-down	SPI Slave Data 1. This ball transfers serial data. Master in, slave out (MISO) or dual/quad mode input/output.
C8	CTRL_DQ0	I/O	Pull-down	SPI Slave Data 0. This ball transfers serial data. Master out, slave in (MOSI) or dual/quad mode input/output.
C9	CTRL_SCLK	Input	Pull-down	SPI Slave Clock. This ball receives the serial clock from the master device on the SPI bus.
C10	CTRL_SS	Input	Pull-up	SPI Slave Select. This ball receives the slave select signal from the master device on the SPI bus.
C11	PDMIN2_1	Input	Pull-down	PDM Input 2 Data (D1).

Ball No.	Mnemonic	Type[1]	Internal Termination[2]	Description
C12	DVDD	Power	None	Digital Supply, 1.2 V ± 5%. This ball can be supplied externally or by using the internal regulator and external pass transistor. Bypass this ball with decoupling capacitors to DGND.
D1	DVDD	Power	None	Digital Supply, 1.2 V ± 5%. This ball can be supplied externally or by using the internal regulator and external pass transistor. Bypass this ball with decoupling capacitors to DGND.
D2	MCLK_OUT	Output	Pull-down	Master Clock Reference Output. Drives a master clock signal to other ICs in the system and can be configured to output a divided down version of the reference clock. Disconnect this ball when not in use.
D3	EVENT	Output	Pull-down	Wake-Up IRQ for External Host. Configurable polarity and output protocol (level sense, edge sense, or continuous pulse).
D4	RESERVED	Ground	Pull-down	Reserved. Connect an external pull-down resistor (1 kΩ) from this ball to ground.
D5	DVDD	Power	None	Digital Supply, 1.2 V ± 5%. This ball can be supplied externally or by using the internal regulator and external pass transistor. Bypass this ball with decoupling capacitors to DGND.
D6	DVDD	Power	None	Digital Supply, 1.2 V ± 5%. This ball can be supplied externally or by using the internal regulator and external pass transistor. Bypass this ball with decoupling capacitors to DGND.
D7	DVDD	Power	None	Digital Supply, 1.2 V ± 5%. This ball can be supplied externally or by using the internal regulator and external pass transistor. Bypass this ball with decoupling capacitors to DGND.
D8	DVDD	Power	None	Digital Supply, 1.2 V ± 5%. This ball can be supplied externally or by using the internal regulator and external pass transistor. Bypass this ball with decoupling capacitors to DGND.
D9	SELFBOOT	Input	Pull-down	Self Boot Select. This ball allows the device to perform a self boot from the external flash connected to the SPI flash port. When connected to IOVDD, a self boot operation is initiated on the next rising edge of $\overline{\text{RESET}}$. This ball must be pulled up or down with a 1.0 kΩ or larger resistor.
D10	TRST	Input	Pull-down	JTAG Test Reset. Joint test action group (JTAG) test access port reset. Connect a 2.0 kΩ pull-up resistor to IOVDD on the line connected to this ball. Connect this ball to DGND when not in use.
D11	PDMIN2_0	Input	Pull-down	PDM Input 2 Data (D0).
D12	PDMCLK2	Output	Pull-down	PDM Input 2 Clock. This ball drives the PDM reference clock. The PDM inputs are always clock slaves.
E1	BCLK3	I/O	Pull-down	Serial Port 3 Bit Clock. Data and frame clock are driven or sampled with respect to this clock. Input is in slave mode, and output is in master mode. Disconnect this ball when not in use.
E2	LRCLK3	I/O	Pull-down	Serial Port 3 Frame Clock. Input is in slave mode, and output is in master mode. Disconnect this ball when not in use.
E3	TRST_DEBUG	Input	Pull-down	JTAG Debug Reset. JTAG debug port reset. Connect a 2.0 kΩ pull-up resistor to IOVDD on the line connected to this ball. Connect this ball to DGND when not in use.
E4	GPIO5	I/O	Pull-down	General-Purpose Input/Output 5. Disconnect this ball when not in use.
E5	DVDD	Power	None	Digital Supply, 1.2 V ± 5%. This ball can be supplied externally or by using the internal regulator and external pass transistor. Bypass this ball with decoupling capacitors to DGND.
E6	DVDD	Power	None	Digital Supply, 1.2 V ± 5%. This ball can be supplied externally or by using the internal regulator and external pass transistor. Bypass this ball with decoupling capacitors to DGND.
E7	DVDD	Power	None	Digital Supply, 1.2 V ± 5%. This ball can be supplied externally or by using the internal regulator and external pass transistor. Bypass this ball with decoupling capacitors to DGND.
E8	DVDD	Power	None	Digital Supply, 1.2 V ± 5%. This ball can be supplied externally or by using the internal regulator and external pass transistor. Bypass this ball with decoupling capacitors to DGND.

Ball No.	Mnemonic	Type[1]	Internal Termination[2]	Description
E9	GPIO0	I/O	Pull-down	General-Purpose Input/Output 0. Disconnect this ball when not in use.
E10	TMS	Input	Pull-down	JTAG Test Master Select. JTAG test access port mode select. Disconnect this ball when not in use.
E11	LRCLK5	I/O	Pull-down	Serial Port 5 Frame Clock. Input is in slave mode, and output is in master mode. Disconnect this ball when not in use.
E12	BCLK5	I/O	Pull-down	Serial Port 5 Bit Clock. Data and frame clock are driven/sampled with respect to this clock. Input is in slave mode, and output is in master mode. Disconnect this ball when not in use.
F1	IOVDD	Power	None	Input/Output Supply, 1.8 V − 5% to 3.3 V + 10%. Bypass this ball with decoupling capacitors to IOGND.
F2	SIO3_D0	I/O	Pull-down	Serial Port 3 Data Input/Output 0. Bidirectional data input/output can be configured as an output to transmit serial data, or as an input to receive serial data. This ball is configurable from one to eight channels of data. Disconnect this ball when not in use.
F3	TMS_DEBUG	Input	Pull-down	JTAG Debug Master. Select JTAG debug mode select. Disconnect this ball when not in use.
F4	GPIO6	I/O	Pull-down	General-Purpose Input/Output 6. Disconnect this ball when not in use.
F5	DVDD	Power	None	Digital Supply, 1.2 V ± 5%. This ball can be supplied externally or by using the internal regulator and external pass transistor. Bypass this ball with decoupling capacitors to DGND.
F6	DGND	Power	None	Digital Ground. Tie all DGND, IOGND, and PGND pins directly together in a common ground plane.
F7	DGND	Power	None	Digital Ground. Tie all DGND, IOGND, and PGND pins directly together in a common ground plane.
F8	DVDD	Power	None	Digital Supply, 1.2 V ± 5%. This ball can be supplied externally or by using the internal regulator and external pass transistor. Bypass this ball with decoupling capacitors to DGND.
F9	GPIO1	I/O	Pull-down	General-Purpose Input/Output 1. Disconnect this ball when not in use.
F10	TDO	Output	Pull-down	JTAG Test Data Output. JTAG test access port data output. Disconnect this ball when not in use.
F11	SIO5_D0	I/O	Pull-down	Serial Port 5 Data Input/Output 0. Bidirectional data input/output can be configured as an output to transmit serial data, or as an input to receive serial data. This ball is configurable from one to eight channels of data. Disconnect this ball when not in use.
F12	IOVDD	Power	None	Input/Output Supply, 1.8 V − 5% to 3.3 V + 10%. Bypass this ball with decoupling capacitors to IOGND.
G1	IOGND	Ground	None	Input/Output Ground Reference. Tie all DGND, IOGND, and PGND pins directly together in a common ground plane.
G2	SIO3_D1	I/O	Pull-down	Serial Port 3 Data Input/Output 1. Bidirectional data input/output can be configured as an output to transmit serial data, or as an input to receive serial data. This ball is configurable from one to eight channels of data. Disconnect this ball when not in use.
G3	TDO_DEBUG	Output	Pull-down	JTAG Test Data Output. JTAG debug port data output. Disconnect this ball when not in use.
G4	GPIO7	I/O	Pull-down	General-Purpose Input/Output 7. Disconnect this ball when not in use.
G5	DGND	Ground	None	Digital Ground. Tie all DGND, IOGND, and PGND pins directly together in a common ground plane.
G6	DGND	Ground	None	Digital Ground. Tie all DGND, IOGND, and PGND pins directly together in a common ground plane.
G7	DGND	Ground	None	Digital Ground. Tie all DGND, IOGND, and PGND pins directly together in a common ground plane.
G8	DGND	Ground	None	Digital Ground. Tie all DGND, IOGND, and PGND pins directly together in a common ground plane.
G9	GPIO2	I/O	Pull-down	General-Purpose Input/Output 2. Disconnect this ball when not in use.

Ball No.	Mnemonic	Type[1]	Internal Termination[2]	Description
G10	TDI	Input	Pull-down	JTAG Test Data Input. JTAG test access port data input. Disconnect this ball when not in use.
G11	SIO5_D1	I/O	Pull-down	Serial Port 5 Data Input/Output 1. Bidirectional data input/output can be configured as an output to transmit serial data, or as an input to receive serial data. This ball is configurable from one to eight channels of data. Disconnect this ball when not in use.
G12	IOGND	Ground	None	Input/Output Ground Reference. Tie all DGND, IOGND, and PGND pins directly together in a common ground plane.
H1	SIO4_D0	I/O	Pull-down	Serial Port 4 Data Input/Output 0. Bidirectional data input/output can be configured as an output to transmit serial data, or as an input to receive serial data. This ball is configurable from one to eight channels of data. Disconnect this ball when not in use.
H2	SIO4_D1	I/O	Pull-down	Serial Port 4 Data Input/Output 1. Bidirectional data input/output can be configured as an output to transmit serial data, or as an input to receive serial data. This ball is configurable from one to eight channels of data. Disconnect this ball when not in use.
H3	TDI_DEBUG	Input	Pull-down	JTAG Debug Data Input. JTAG debug port data input. Disconnect this ball when not in use.
H4	SDA	I/O	Pull-up	I^2C Master Port Serial Data. Connect a 2.0 kΩ pull-up resistor to IOVDD on the line connected to this ball. Disconnect this ball when not in use.
H5	DGND	Ground	None	Digital Ground. Tie all DGND, IOGND, and PGND pins directly together in a common ground plane.
H6	DGND	Ground	None	Digital Ground. Tie all DGND, IOGND, and PGND pins directly together in a common ground plane.
H7	DGND	Ground	None	Digital Ground. Tie all DGND, IOGND, and PGND pins directly together in a common ground plane.
H8	DGND	Ground	None	Digital Ground. Tie all DGND, IOGND, and PGND pins directly together in a common ground plane.
H9	GPIO3	I/O	Pull-down	General-Purpose Input/Output 3. Disconnect this ball when not in use.
H10	TCK	Input	Pull-down	JTAG Test Clock. JTAG test access port clock. Disconnect this ball when not in use.
H11	LRCLK6	I/O	Pull-down	Serial Port 6 Frame Clock. Input is in slave mode, and output is in master mode. Disconnect this ball when not in use.
H12	BCLK6	I/O	Pull-down	Serial Port 6 Bit Clock. The data and frame clock are driven or sampled with respect to this clock. Input is in slave mode, and output is in master mode. Disconnect this ball when not in use.
J1	BCLK4	I/O	Pull-down	Serial Port 4 Bit Clock. The data and frame clock are driven or sampled with respect to this clock. Input is in slave mode, and output is in master mode. Disconnect this ball when not in use.
J2	LRCLK4	I/O	Pull-down	Serial Port 4 Frame Clock. Input is in slave mode, and output is in master mode. Disconnect this ball when not in use.
J3	TCK_DEBUG	Input	Pull-down	JTAG Debug Clock. JTAG debug port clock. Disconnect this ball when not in use.
J4	SCL	I/O	Pull-up	I^2C Master Serial Clock. This ball drives a serial clock to slave devices on the I^2C bus. Connect a 2.0 kΩ to 4.0 kΩ pull-up resistor to IOVDD on the line connected to this ball. Disconnect this ball when not in use.
J5	CVDD	Power	None	Memory Circuitry Supply, 1.2 V ± 5%. This ball can be supplied externally or by using the internal regulator and external pass transistor. Bypass this ball with decoupling capacitors to DGND.
J6	CVDD	Power	None	Memory Circuitry Supply, 1.2 V ± 5%. This ball can be supplied externally or by using the internal regulator and external pass transistor. Bypass this ball with decoupling capacitors to DGND.
J7	CVDD	Power	None	Memory Circuitry Supply, 1.2 V ± 5%. This ball can be supplied externally or by using the internal regulator and external pass transistor. Bypass this ball with decoupling capacitors to DGND.

Ball No.	Mnemonic	Type[1]	Internal Termination[2]	Description
J8	CVDD	Power	None	Memory Circuitry Supply, 1.2 V ± 5%. This ball can be supplied externally or by using the internal regulator and external pass transistor. Bypass this ball with decoupling capacitors to DGND.
J9	GPIO4	I/O	Pull-down	General-Purpose Input/Output 4. Disconnect this ball when not in use.
J10	QMST_SS0	Output	Pull-up	SPI Master Slave Select 0. This ball enables Slave Flash Device 0 on the bus. Disconnect this ball when not in use.
J11	SIO6_D1	I/O	Pull-down	Serial Port 6 Data Input/Output 1. Bidirectional data input/output can be configured as an output to transmit serial data, or as an input to receive serial data. This ball is configurable from one to eight channels of data. Disconnect this ball when not in use.
J12	SIO6_D0	I/O	Pull-down	Serial Port 6 Data Input/Output 0. Bidirectional data input/output can be configured as an output to transmit serial data, or as an input to receive serial data. This ball is configurable from one to eight channels of data. Disconnect this ball when not in use.
K1	PDMCLK3	Output	Pull-down	PDM Input 3 Clock. This ball drives the PDM reference clock. The PDM inputs are always clock slaves.
K2	PDMIN3_0	Input	Pull-down	PDM Input 3 Data (D0).
K3	QMST_SS3	Output	Pull-up	SPI Master Slave Select 3. This ball enables Slave Flash Device 3 on the bus. Disconnect this ball when not in use.
K4	QMST_SS2	Output	Pull-up	SPI Master Slave Select 2. This ball enables Slave Flash Device 2 on the bus. Disconnect this ball when not in use.
K5	QMST_SS1	Output	Pull-up	SPI Master Slave Select 1. This ball enables Slave Flash Device 1 on the bus. Disconnect this ball when not in use.
K6	QMST_DQ3	I/O	Pull-down	SPI Master Data 3. This ball transfers serial data in quad mode. Disconnect this ball when not in use.
K7	QMST_DQ2	I/O	Pull-down	SPI Master Data 2. This ball transfers serial data in quad mode. Disconnect this ball when not in use.
K8	QMST_DQ1	I/O	Pull-down	SPI Master MISO, Dual/Quad SPI Master Data 1. This ball transfers serial data. MISO or dual/quad mode input/output. Disconnect this ball when not in use.
K9	QMST_DQ0	I/O	Pull-down	SPI Master MOSI, Dual/Quad SPI Master Data 0. This ball transfers serial data. MOSI or dual/quad mode input/output. Disconnect this ball when not in use.
K10	QMST_SCK	Output	Pull-down	SPI Master Clock. Quad SPI Master Clock. This ball drives the clock signal to a slave device on the SPI bus. Disconnect this ball when not in use.
K11	PDMOUT5	Output	Pull-down	PDM Output 5 Data.
K12	PDMCLK5	I/O	Pull-down	PDM Output 5 Clock. This ball drives the PDM reference clock. The PDM inputs are always clock slaves.
L1	IOVDD	Power	None	Input/Output Supply, 1.8 V − 5% to 3.3 V + 10%. Bypass this ball with decoupling capacitors to IOGND.
L2	PDMIN3_1	Input	Pull-down	PDM Input 3 Data (D1).
L3	PDMIN4_1	Input	Pull-down	PDM Input 4 Data (D1).
L4	PDMIN4_0	Input	Pull-down	PDM Input 4 Data (D0).
L5	FMST_DQ3	I/O	Pull-down	Flash Quad SPI Master Data 3. This ball transfers serial data in quad mode. Disconnect this ball when not in use.
L6	FMST_DQ2	I/O	Pull-down	Flash Quad SPI Master Data 2. This ball transfers serial data in quad mode. Disconnect this ball when not in use.
L7	FMST_DQ1	I/O	Pull-down	Flash SPI Master MISO, Flash Dual/Quad SPI Master Data 1. This ball transfers serial data. MISO or dual/quad mode input/output. Disconnect this ball when not in use.
L8	FMST_DQ0	I/O	Pull-down	Flash SPI Master MOSI, Flash Dual/Quad SPI Master Data 0. This ball transfers serial data. MOSI or dual/quad mode input/output. Disconnect this ball when not in use.
L9	FMST_SS	Output	Pull-up	Flash SPI Master Slave Select. This ball enables the slave flash device on the bus. Disconnect this ball when not in use.
L10	PDMCLK6	I/O	Pull-down	PDM Output 6 Clock. This ball drives the PDM reference clock. The PDM inputs are always clock slaves.
L11	PDMOUT6	Output	Pull-down	PDM Output 6 Data.

Ball No.	Mnemonic	Type[1]	Internal Termination[2]	Description
L12	IOVDD	Power	None	Input/Output Supply, 1.8 V – 5% to 3.3 V + 10%. Bypass this ball with decoupling capacitors to IOGND.
M1	IOGND	Ground	None	Input/Output Ground Reference. Tie all DGND, IOGND, and PGND pins directly together in a common ground plane.
M2	DVDD	Power	None	Digital Supply, 1.2 V ± 5%. This ball can be supplied externally or by using the internal regulator and external pass transistor. Bypass this ball with decoupling capacitors to DGND.
M3	DGND	Ground	None	Digital Ground.
M4	CVDD	Power	None	Memory Circuitry Supply, 1.2 V ± 5%. This ball can be supplied externally or by using the internal regulator and external pass transistor. Bypass this ball with decoupling capacitors to DGND.
M5	PDMCLK4	Output	Pull-down	PDM Input 4 Clock. This ball drives the PDM reference clock. The PDM inputs are always clock slaves.
M6	IOGND	Ground	None	Input/Output Ground Reference. Tie all DGND, IOGND, and PGND pins directly together in a common ground plane.
M7	IOVDD	Power	None	Input/Output Supply, 1.8 V – 5% to 3.3 V + 10%. Bypass this ball with decoupling capacitors to IOGND.
M8	FMST_SCK	Output	Pull-down	Flash SPI Master Clock. This ball drives the clock signal to a slave flash device on the SPI bus. Disconnect this ball when not in use.
M9	CVDD	Power	None	Memory Circuitry Supply, 1.2 V ± 5%. This ball can be supplied externally or by using the internal regulator and external pass transistor. Bypass this ball with decoupling capacitors to DGND.
M10	DGND	Ground	None	Digital Ground. Tie all DGND, IOGND, and PGND pins directly together in a common ground plane.
M11	DVDD	Power	None	Digital Supply, 1.2 V ± 5%. This ball can be supplied externally or by using the internal regulator and external pass transistor. Bypass this ball with decoupling capacitors to DGND.
M12	IOGND	Ground	None	Input/Output Ground Reference. Tie all DGND, IOGND, and PGND pins directly together in a common ground plane.

[1] I/O means input/output, power means a supply, and NC means a no connect.
[2] Most internal pull-up and pull-down resistors can be user disabled via the pad control registers.

THEORY OF OPERATION

OVERVIEW

The ADAU1472 is based on the Cadence Tensilica HiFi 4 audio processor core operating at frequencies up to 270.336 MHz and integrating 2 MB of SRAM, math accelerators, and up to 96 channels of audio input and output (16 input, 16 output, and 64 bidirectional). The ADAU1472 includes a flexible audio routing matrix (FARM) for hardware routing of all audio signals at various sample rates between all inputs, outputs, HiFi 4 DSP core, and integrated sample rate converters. The HiFi 4 can execute more than 1 billion MAC operations per second using the quadruple MAC datapath.

The audio subsystem supports sample rates up to 192 kHz and includes six serial audio inputs and outputs with I²S and time division multiplexing (TDM), four stereo ASRCs, S/PDIF receiver and transmitter, 14 PDM inputs, and two PDM outputs.

Eight dedicated general-purpose input/output (GPIOx) pins are available, and the DSP core includes four GPIO interrupts.

The processor integrates two power domains, a low power always on (IOVDD) domain, and a full power (DVDD, CVDD, and PVDD) domain. The low power domain requires only the IOVDD supply and includes two serial input ports, two serial output ports, two PDM microphone inputs, a voice detection processor, and internal audio routing. The system memories support data retention in the low power state via the separate memory retention supply (CVDD). The voice detection technology can detect human speech and transition the processor to full speed operating mode for voice processing. The full power domain includes the HiFi 4 DSP core, system memory, PLL, and additional audio input/output.

The device operates in one of two boot modes, as follows:

- Host boot, the settings of the chip can be loaded and dynamically updated through the SPI slave port
- Self boot, the DSP can boot directly from an external flash memory in a system with no host processor

TOTAL POWER DISSIPATION

Total power dissipation has the following two components:

- Static, including leakage current
- Dynamic, due to transistor switching characteristics

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor and memory activity. Static power dissipation is a function of voltage (IOVDD, DVDD, CVDD, and PVDD), temperature, and clock frequency.

The dynamic power component is due to transistor switching in the SYSCLK and BUSCLK and depends on the DSP core and memory utilization of the application code running on the processor core.

HiFi 4 AUDIO DSP CORE

The HiFi 4 core features a 32-bit, audio DSP engine optimized for audio and voice processing and other demanding DSP functions. The HiFi 4 core combines four 32-bit × 32-bit fixed point MACs with 72-bit accumulators, a single 32-bit IEEE floating-point multiplier, and support for dual 64-bit load per cycle. The processor provides on-chip debug support with control of the software state of the processor through an IEEE 1149.1 test access port, also known as JTAG. The ADAU1472 is software-compatible with the comprehensive ecosystem of HiFi architecture optimized audio and voice codecs and audio enhancement software packages.

HiFi 4 Architecture

The HiFi 4 architecture offers the following features:

- 32-bit single instruction, multiple data (SIMD) architecture
- Very long instruction word (VLIW) instruction set with up to four operations in parallel
- Single-cycle, quad MAC (four 32 × 32, four 24 × 24, eight 32 × 16)
- Single precision floating-point unit
- 128-bit data load, 64-bit data store
- 32 kB instruction cache
- 128 kB data cache
- 64 kB L1 instruction RAM
- 256 kB L1 data RAM
- Memory prefetching
- Two general-purpose timers
- Two cycle counters
- Interrupt controller (eight internal and 17 external)
- Tensilica on-chip debug (OCD)

For more information on the HiFi 4 DSP core, refer to the Cadence Tensilica HiFi 4 audio engine documentation.

Math Acceleration

The DSP core includes optimized custom instructions to accelerate basic math, audio, probabilistic, and neural network processing. Extensions support various data formats depending on the instruction, including floating-point format, and 16.16, 9.23, and 1.31 fixed point formats. Some instructions operate on log domain input data. The instructions are shown in Table 20 and Table 21.

Table 20. DSP Instruction Extensions (Fixed Point)

Function	Operation
LOG2(x)	Base 2 logarithm, $\log_2(x)$
LOG2_ABS(x)	$\text{Log}_2(\text{abs}(x))$, returns sign of input
EXP2(x)	Base 2 exponential, 2^x
LOGADD(x, y)	Linear addition for log domain data, $\log_2(\exp_2(x) + \exp_2(y))$
ADDLOG(x, y)	Log domain data addition
SUBLOG(x, y)	Log domain data subtraction
ADDLOGADD(w, x, y, z)	Dual LOGADD with linear addition, $\log_2(\exp_2(w + x) + \exp_2(y + z))$
ATAN2(x, y)	Arctan2, $\tan^{-1}(y/x)$
PRNG()	Pseudorandom number generator
Rectify(x)	Max(0,x)
Leaky Rectify(x)	x < 0 results in small nonzero gradient
Sigmoid(x)	Sigmoid, $1/(1 + e^{-x})$
DualSigmoid(x, y)	Two sigmoid operations in parallel
SIN(x)	Sine
COS(x)	Cosine
SINH(x)	Hyperbolic sine
COSH(x)	Hyperbolic cosine
ATANH(x)	Hyperbolic tangent
TOPOLAR (x, y)	Rectangular to polar conversion

Table 21. DSP Instruction Extensions (Floating-Point)

Function	Operation
SINF(x)	Sine
COSF(x)	Cosine
TANF(x)	Tangent
ASINF(x)	Arcsine
ACOSF(x)	Arccosine
ATANF(x)	Arctangent
EXPF(x)	Exponential, e^x
LNF(x)	Natural logarithm, ln(x)
EXP2F(x)	Base 2 exponential, 2^x
LOG2F(x)	$\text{Log}_2(x)$
SQRTF(x)	Square root
RECIPF(x)	Reciprocal, 1/x
ATAN2F(x, y)	Arctan2, $\tan^{-1}(y/x)$
HYPOTF(x, y)	Hypotenuse, $\sqrt{x^2 + y^2}$
RTOP (x, y)	Rectangular to polar conversion
PTOR (x, y)	Polar to rectangular conversion

PROCESSOR INFRASTRUCTURE

The following sections provide information on the primary infrastructure components of the ADAU1472 processor.

Memory DMA Controller

The processor uses direct memory access (DMA) to transfer data within memory spaces or between a memory space and a peripheral. The processor can specify data transfer operations and return to normal processing, whereas the integrated DMA controller carries out the data transfers.

Audio DMA Controller

The processor contains a dedicated DMA controller for transfer of up to 32 channels of audio data between system memory and any of the audio input/output peripherals (serial ports, PDM ports, ASRCs, and S/PDIFs). The audio DMA supports a circular buffer mode synchronized with audio input/output interrupts for continuous data transfer operation.

System Controller

The system controller manages reset, self boot, clocking, and power management. The event manager provides for two-way communication between an external host processor. The external event pin (EVENT) can trigger a host, whereas the host can set event registers to trigger core interrupt signals.

DSP Core Interrupts

Interrupt events occur asynchronously to the program flow. The interrupts are triggered by input signals, timers, and peripherals, or explicitly in the software running in the DSP core. There are eight internal interrupts including software and timer interrupts, and 17 external interrupts, with four interrupts reserved for GPIO inputs.

GPIO

Each of the eight GPIO port pins (GPIOx) can be individually controlled by the GPIO mode registers as follows:

- GPIO direction specifies the direction of each individual GPIOx pin as an input or an output.
- The GPIO0 to GPIO3 pins as inputs that can generate DSP core interrupts.
- Configurable debounce circuitry is available for the pins configured as inputs.
- The ability to enable or disable output pull-down resistors.

FARM

The audio routing matrix distributes audio signals among the serial inputs and outputs, PDM inputs and outputs, S/PDIF receiver and transmitter, ASRCs, DSP core, and audio DMA. All audio inputs and ASRC channels are available to the DSP core, and all audio outputs can source data either from the DSP core or directly from any audio input. Audio data can be routed directly through the FARM, bypassing the processor core entirely. This flexibility reduces the complexity of signal routing and clocking issues in the audio system and allows routing in hardware instead of in software.

MEMORY ARCHITECTURE

The internal and external memory of the ADAU1472 processor is shown in Figure 13 and described in the following sections.

Internal Memory

The L1 memory system is the highest performance (zero latency) memory available to the processor core and includes the following:

- 64 kB L1 instruction RAM
- 128 kB L1 data RAM 1
- 128 kB L1 data RAM 2

The processor core contains a 32 kB instruction cache and 128 kB data cache and a speculative cache prefetch option. Hardware prefetching is enabled by default but can be manually controlled or disabled using prefetching instructions.

The processor features 2 MB L2 system SRAM. The L2 memory operates at half of the core frequency and can hold any mixture of instruction and data. This space contains the application instructions and literal (constant) data. The L2 memory is accessible by the core through a dedicated 64-bit interface (with dual 64-bit load interfaces) and DMA read/write access for system devices. An internal 128 kB read only memory (ROM) contains boot code and general-purpose constants. The boot ROM executes at system reset.

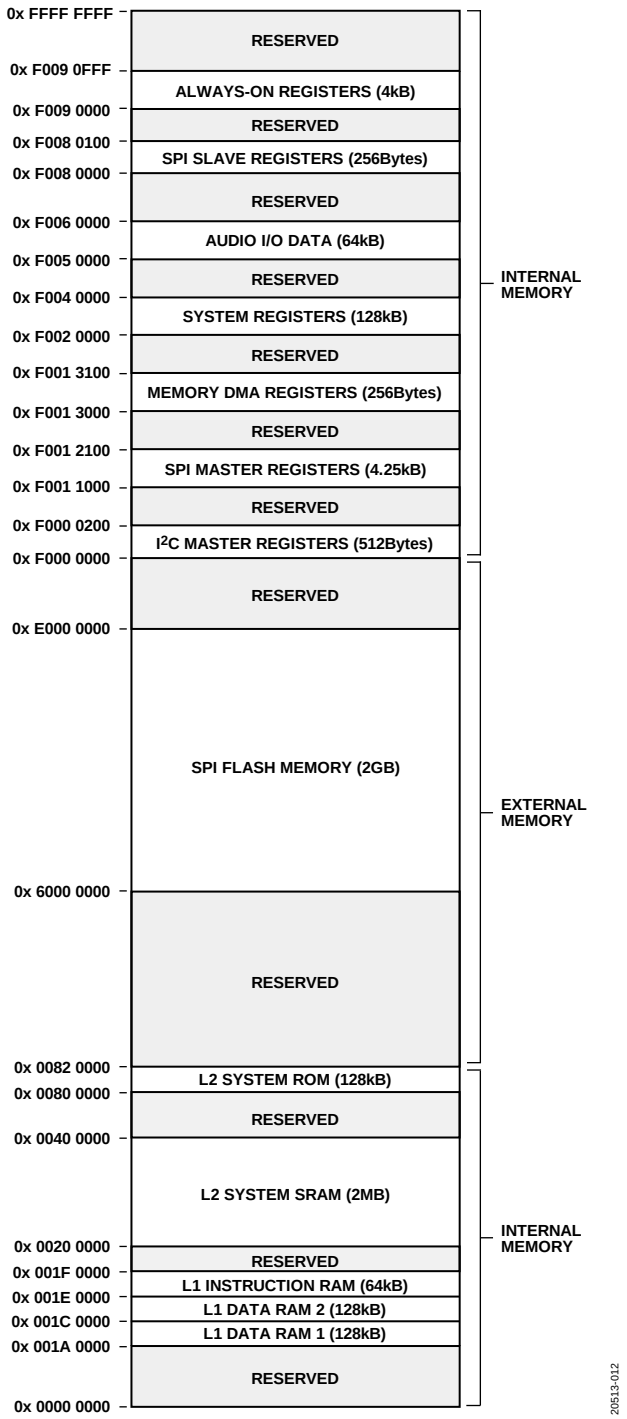


Figure 13. Processor Memory Map

External Memory Space

The processor does not define a separate input/output space. All memory resources are mapped through the 32-bit address space. On-chip input/output devices have their control registers mapped into memory mapped registers at addresses in a region of the 4 GB address space. These addresses are separated into smaller blocks of always on functions, core and audio peripherals, and SPI/I²C port configurations. The memory mapped registers are accessible by the DSP core and externally from the SPI slave control port.

External SPI Flash Region

The ADAU1472 memory address space supports up to 2 GB of external serial quad flash memory optionally connected to the SPI flash port of the processor. DSP core reads from flash memory are directly cached via internal cache, and direct memory mapped reads are permitted via the SPI memory mapped protocol. The SPI flash port is used for self boot mode.

Booting

There are two processor boot modes. In self boot mode, the processor actively loads data from the serial memory. In host boot mode, the processor receives data from the external host devices. The SELFBOOT input pin, sampled during power-on resets and software initiated resets, defines the boot mode.

To initiate a self boot operation, connect the SELFBOOT pin to logic high (IOVDD) and power up the power supplies while the RESET pin is pulled high. The processor boots from external flash memory through the dedicated SPI flash host port. If self boot fails, the EVENT pin is pulled high.

PROCESSOR RELIABILITY FEATURES

The processor provides the reliability features described in the following sections.

Byte Parity Protected Memories

Each byte in the processor L2 system RAM, L1 data RAM, and data cache are protected by a parity bit to detect single event upsets in the RAMs. The L1 instruction RAM and instruction cache have word level parity protection. The panic manager flags parity errors when detected.

Software Watchdog

The on-chip watchdog timer can provide software-based supervision of the ADAU1472 core.

MIPS Estimator

Two independent hardware cycle counters under full software control allow unobtrusive software performance profiling and run-time monitoring of utilized DSP clock cycles. Each counter supports stop, start, and pause/unpause via register controls. In addition to cycle counters, each unit has a peak cycle register that stores the highest cycle count over multiple start and stop sequences.

Panic Manager

The panic manager can receive many sources of system panic, mask them, trigger an event output pin signal, generate a core interrupt, and generate an internal reset for device reboot. The panic manager consists of a number of panic channels, each capable of recording a panic event and a 32-bit panic code register.

TIMERS

General-Purpose Timers

The timer unit provides three general-purpose software programmable timers. The timers can generate interrupts to the processor core, providing periodic events for synchronization to the system clock signal.

Watchdog Timer

The core includes a 32-bit timer that can implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state, via generation of a hardware reset, or core interrupt, if the timer expires before resetting by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before counting to zero from the programmed value. The watchdog reset protects the system from remaining in an unknown state where any software that is running in the DSP core, which normally resets the timer, has stopped running due to an external noise condition or software error. After a reset, the software can determine if the watchdog was the source of the hardware reset by interrogating the watchdog error flag in the panic manager.

SERIAL PORTS

The six serial data interfaces provide audio input and output to the processor and peripherals. Serial port data is transferred directly to and from the DSP audio input/output registers and to system memory using the audio DMA channels. Audio data can be routed directly between serial ports via the FARM.

Serial ports support the following configurable data formats:

- I²S
- Multichannel (TDM)
- Packed I²S
- Left justified
- Right justified
- 16-, 24-, and 32-bit TDM mode slot width

Each serial port consists of a clock, a frame sync, and two data lines. Serial Port 1 and Serial Port 2 in the always on domain have dedicated input and output data lines. The remaining four DVDD power domain serial ports have data lines that are bidirectional and programmable to either transmit or receive.

Table 22. Serial Data Pins and Serial Input/Output Ports Mapping

Serial Data Pin	Serial Port	Function
SIN1[1]	Serial Input Port 1	Input
SIN2[1]	Serial Input Port 2	Input
SOUT1[1]	Serial Output Port 1	Output
SOUT2[1]	Serial Output Port 2	Output
SIO3_D0	Serial Input/Output Port 3_0	Bidirectional
SIO3_D1	Serial Input/Output Port 3_1	Bidirectional
SIO4_D0	Serial Input/Output Port 4_0	Bidirectional
SIO4_D1	Serial Input/Output Port 4_1	Bidirectional
SIO5_D0	Serial Input/Output Port 5_0	Bidirectional
SIO5_D1	Serial Input/Output Port 5_1	Bidirectional
SIO6_D0	Serial Input/Output Port 6_0	Bidirectional
SIO6_D1	Serial Input/Output Port 6_1	Bidirectional

[1] IOVDD power domain.

There are 80 channels of serial audio data inputs and 80 channels of serial audio data outputs. The 80 audio input channels and 80 audio output channels are distributed among two dedicated serial data input pins, two dedicated serial data output pins, and eight bidirectional serial input/output data pins. Each data pin is capable of 2-channel (I^2S), 4-channel, and 8-channel (TDM) modes. A 16-channel TDM mode is supported using two data pins (eight channels per pin) for 16-channel data transfer. The maximum sample rate for the serial audio data on the serial ports is 192 kHz. The minimum sample rate is 8 kHz.

The serial ports have a flexible configuration scheme that allows independent configuration of clock waveform type, clock polarity, channel count, position of the data bits within the stream, audio word length, slave or master operation, and sample rate.

Serial Clock Domains

Six serial clock domains consist of a pair of frame clock (LRCLKx) and bit clock (BCLKx) pins, which synchronize the transmission of audio data to and from the device. In master mode, each clock domain corresponds to exactly one LRCLKx pin, one BCLKx pin, and a pair of data pins. In slave mode, a serial port can be clocked by any clock domain.

ASRCs

The ADAU1472 includes eight channels of integrated ASRCs that handle input and output signals with different sample rates. These sample rate converters are capable of receiving audio input data signals and clocks and resynchronizing the data stream to an arbitrary target sample rate. The sample rate converters include filtering. Therefore, the data output from the sample rate converter is not a bit accurate representation of the data input.

The sample rate converters are grouped into four stereo pairs, and each of the four converters is individually configurable with two input/output channels belonging to each ASRC. The ASRC is connected to the FARM for flexible routing to and from the DSP core, PDM ports, serial ports, and audio DMA.

Sample rate converter configuration and routing is configured using the ASRC control registers.

ASRC Group Delay

The group delay of the sample rate converter is dependent on the input and output sampling frequencies as described in the following equations.

For S_OUT signal frequency (f_{S_OUT}) > S_IN signal frequency (f_{S_IN}),

$$GDS = \frac{16}{f_{S_IN}} + \frac{32}{f_{S_IN}}$$

where *GDS* is the group delay in seconds.

For $f_{S_OUT} < f_{S_IN}$,

$$GDS = \frac{16}{f_{S_IN}} + \left(\frac{32}{f_{S_IN}}\right) \times \left(\frac{f_{S_IN}}{f_{S_OUT}}\right)$$

DIGITAL PDM MICROPHONE INTERFACE

Up to 14 PDM microphones can be connected to the four dedicated digital microphone interfaces. Each PDM interface consists of a clock line and data line(s). Two microphones can share a single data line and be used along with a clock line to create a dual input microphone port. Two dual input lines can share a single clock line to create a quad microphone input port.

There are two PDM microphone interfaces in the IOVDD power domain (one dual input and one quad input) and two additional quad PDM microphones interfaces in the full power domain.

PDM microphone interface bit clocks are generated at a fixed frequency, typically 3.072 MHz, corresponding to audio sampling rates of 24 kHz or 48 kHz. The PDM microphone inputs include internal decimation filters and are routed through the FARM for input to the DSP core, the ASRCs, and directly to serial output ports.

PDM OUTPUTS

Two PDM output interfaces provide direct connectivity to Class D amplifiers and other PDM input devices. A PDM output port consists of a clock line and single data line, and two channels can share a single data line for stereo output. The PDM output clock can operate in either master or slave configurations depending on the application.

S/PDIF INTERFACE

The on-chip S/PDIF receiver and transmitter ports provide stereo audio connectivity to S/PDIF-compatible equipment. The S/PDIF receiver consists of two audio channels input on one hardware pin (SPDIF_RX). The S/PDIF transmitter consists of two audio channels output on one hardware pin (SPDIF_TX). The clock signal is embedded in the data using biphase mark code. The S/PDIF input and output word lengths can be independently set to 16, 20, or 24 bits. The S/PDIF interface meets the S/PDIF consumer performance specification. It does not meet the Audio Engineering Society (AES3) professional specification jitter tolerance.

S/PDIF Receiver

Because the S/PDIF input data is typically asynchronous to the DSP core, the input data must be routed through an ASRC. The S/PDIF receiver works at a wide range of sampling frequencies between 18 kHz and 96 kHz.

In addition to audio data, S/PDIF streams contain user data, channel status, a validity bit, a virtual left right clock (LRCLK), and block start information. The receiver decodes audio data and sends the data to the corresponding registers in the control register map, where the information is read.

The S/PDIF ports meet the following AES and European Broadcasting Union (EBU) specifications: a jitter of 0.25 UI p-p at 8 kHz and above, a jitter of 10 UI p-p below 200 Hz, and a minimum signal voltage of 200 mV.

S/PDIF Transmitter

The S/PDIF transmitter outputs two channels of audio data either directly from the DSP core at the core rate or passes through directly from the S/PDIF receiver. The extra nonaudio data bits can be copied directly from the S/PDIF receiver or programmed manually by using the corresponding registers in the control register map.

SPI

The processor contains three SPI-compatible interfaces that allow the processor to communicate with multiple SPI-compatible devices. The SPI baud rate and clock phase and polarities are programmable. Each SPI-compatible interface has integrated DMA channels for both transmit and receive data streams.

The baseline SPI is a synchronous, 4-wire interface consisting of two data pins, one device select pin, and a gated clock pin. The two data pins allow full duplex operation to other SPI-compatible devices. Two additional (optional) data pins are provided to support quad SPI operation.

SPI Slave Interface

The SPI slave interface enables a host processor to write directly to memory and configure control registers with support for access in both single address mode and burst mode. The slave interface is part of the IOVDD power domain and is available during low power operation. The SPI slave interface operates only in SPI Mode 1, Clock Polarity 0, and Clock Phase 1, and can optionally be configured for dual or quad SPI mode operation. The maximum clock baud rate is limited by the master clock rate and the maximum read speed is one-half the master clock frequency.

SPI Master Interface

The SPI master supports up to four slave devices (via the QMST_SSx pins) and speeds between 2.3 kHz and 25 MHz. For high data rates on the SPI master interface (≥10 MHz), design PCB traces to be as short as possible to minimize current draw. SPI commands can optionally operate in dual or quad SPI mode.

SPI Flash Interface

The processor includes one dedicated SPI flash host interface intended for a single external flash memory connection, which features memory mapped registers with support for direct read of SPI flash memory from the DSP core. This host interface includes support for prefetch and caching. Always use the SPI flash interface for self boot operation. The SPI flash interface can be configured optionally for dual or quad SPI mode operation.

I²C Master Interface

The processor includes an I²C bus standard-compatible master module. The I²C master is 7-bit addressable and supports standard and fast mode operation with speeds between 20 kHz and 500 kHz. The I²C interface uses two dedicated pins for transferring clock (SCL) and data (SDA), and data transfers are 8-bit aligned. No error detection or correction is supported, and the serial camera control bus (SCCB) and power management bus (PMBus) protocols are not supported.

Voice Detector

The ADAU1472 includes a configurable voice onset detector for detecting speech energy in the environment. The voice detection unit operates independently of the DSP core at low power in the IOVDD power domain, and the main purpose of the voice detector is to save system power. The voice detector can respond to speech signals and power on the DSP core out of the low power operating mode. In addition, an event pin (EVENT) signal can notify an external host of voice detection.

By default, the voice detector is configured in voice onset detection mode and detects the presence of speech at a programmable threshold. The voice detector can optionally be configured for voice activity detection or voice formant detection modes for advanced voice wake-up applications.

The voice detector can process either one or two audio inputs depending on the configuration. In low power operation, audio input can come from PDM Input 1 and PDM Input 2 and/or Serial Input Port 1 and Serial Input Port 2. The voice detector is connected to the FARM, all audio sources, and the DSP output are fully routable to the detector input when in full power operation.

The detector can buffer up to 1024 samples of audio data from a single input in a dedicated memory, permitting the DSP core to reanalyze audio detected to contain speech while the core processor was in an inactive state.

CLOCK AND POWER MANAGEMENT

Clocking Overview

The processor can be clocked by a sine wave input, a buffered and shaped clock derived from an external clock oscillator, or an external crystal. If an external clock is used, the clock must be a TTL-compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. Connect the clock source directly to the MCLK_IN pin to supply the master clock. Alternatively, connect an external crystal and drive the crystal from the on-chip oscillator circuit.

Using the Crystal Oscillator

The ADAU1472 includes an on-board oscillator that uses an external crystal circuit connected to the XTAL_IN and XTAL_OUT pins to generate its master clock. For the external crystal in the circuit, use an AT-cut parallel resonance device operating at a fundamental frequency of 12.288 MHz or 24.576 MHz. Quartz crystals are recommended. Do not use ceramic resonators due to the poor jitter performance of the resonators. Figure 14 shows the external crystal oscillator circuit that is required for proper operation.

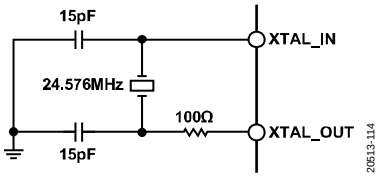


Figure 14. External Crystal Oscillator Circuit

The capacitor and resistor values shown in Figure 14 are typical values only. The required capacitor values are dependent upon the load capacitance recommendations from the crystal manufacturers and the PCB physical layout. The resistor value depends on the drive level specified by the crystal manufacturer. The user must customize and verify the values based on the measurements of the multiple devices over the required operating temperature range.

Place the crystal as close to the XTAL_OUT pin as possible and minimize all oscillator circuit trace lengths to decrease stray capacitance that may cause crystal start-up problems.

Do not use XTAL_OUT to directly drive the crystal signal to another IC. A separate pin, MCLK_OUT, is provided for this purpose. If an external clock signal is provided to the MCLK_IN/XTAL_IN pin, the crystal resonator circuit is not necessary, and the XTAL_OUT pin must be left disconnected.

Master Clock and PLL Mode

The master clock generators generate all on-chip clocks and synchronization signals. An integer PLL is available to generate the core system clock from the master clock input signal. Three clock generator units with programmable multiplication factors and dividers generate clocks for the audio system and output clocks.

The PLL generates the nominal (and maximum) 270.336 MHz system clock to run the DSP core. The nominal input frequency to the PLL is 12.288 MHz.

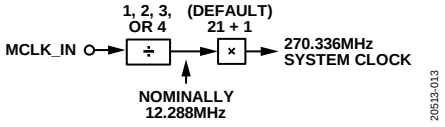


Figure 15. PLL Functional Block Diagram

For systems operating at a 16 kHz, 48 kHz, 96 kHz, or 192 kHz audio sample rate, the recommended master clock input frequencies are 12.288 MHz, 16.384 MHz, or 24.576 MHz. The flexibility of the PLL allows other clock frequencies as well.

Typically, the PLL locks in less than 500 µs. When the PLL locks to an input clock and creates a stable output clock, a lock flag sets.

Master Clock Generators

The master clock generator consists of three separate clock generator units, and each clock generator can generate a base frequency and several fractions of the base frequency for a total of 15 audio clock rates available in the system.

Each of the 15 clock domains can create the appropriate bit clock (BCLK) and audio frame clock (LRCLK) signals required for the serial ports. Bit clock signals are generated at frequencies of 32 BCLKs per sample, 64 BCLKs per sample, 128 BCLKs per sample, 256 BCLKs per sample, and 512 BCLKs per sample to support various audio sampling rates and multichannel TDM clocking requirements.

Determine the nominal audio sampling rate of each clock generator by using the following equation:

$$Output\ Frequency = (Input\ Frequency \times N)/(512 \times M)$$

where:
Output Frequency is the audio frame clock output frequency.
Input Frequency is the PLL output (typically 270.336 MHz).
Each clock generator has a clock divider with configurable numerator and denominator values, *N* and *M*.
N and *M* are integers that are configured by writing to the clock generator configuration registers. Clock Generator 2 has an additional fixed 2/3 fractional divider of the input clock.

For Clock Generator 1 and Clock Generator 2, the integer numerator (N) and the integer denominator (M) are each nine bits long. For Clock Generator 3, N and M are each 16 bits long, allowing a higher precision when generating arbitrary clock frequencies. Figure 16 shows a basic block diagram of the PLL and clock generators.

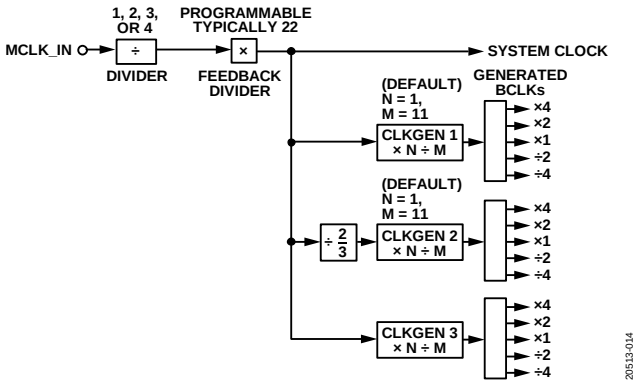


Figure 16. PLL and Master Clock Generators Block Diagram

Figure 17 shows an example of the master clock generator with an MCLK_IN input has a frequency of 24.576 MHz, and the default settings of the PLL predivider, feedback divider, and the three clock generators.

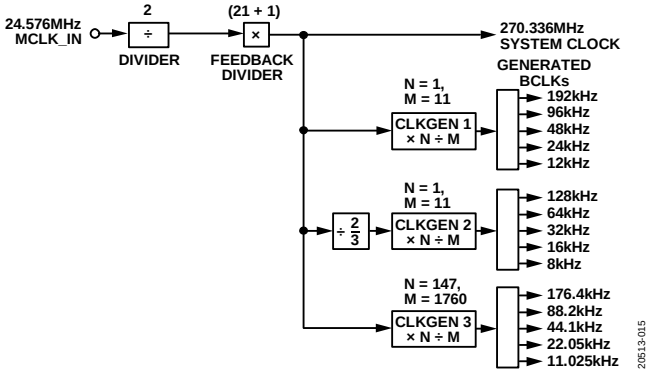


Figure 17. Typical PLL and Master Clock Generators, MCLK_IN = 24.576 MHz

Audio Clock Generator

The audio clock generator is a separate master clock generator unit located in the IOVDD power domain and provides the audio clock to the always on serial ports and PDM ports. The audio clock generator runs directly off the MCLK_IN clock and contains two clock generator units, creating up to 10 clock rates total for frame clock (LRCLK) and bit clock (BCLK) signals. The maximum generated bit clock frequency of the audio clock generator is limited to 3.072 MHz, which limits the maximum serial port clock rates in master mode for Serial Port 1 and Serial Port 2 (48 kHz I^2S). Figure 18 shows a block diagram of the audio clock generator.

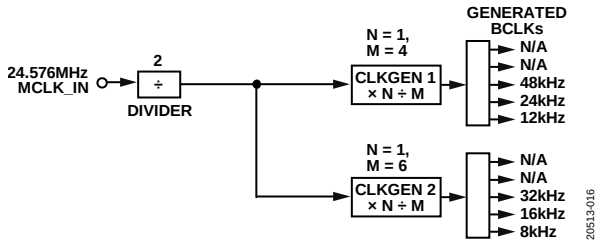


Figure 18. Audio Clock Generators, MCLK_IN = 24.576 MHz

Master Clock Output

The master clock output pin (MCLK_OUT) is provided for use cases where a master clock must be supplied to other ICs in the system. The master clock output pin has programmable options to output a divided down version of the predivided PLL reference clock. The MCLK_OUT pin can drive more than one external slave IC if the drive strength is sufficient to drive the traces and external receiver circuitry, but the MCLK_OUT pin is not designed to drive long cables or other high impedance transmission lines. MCLK_OUT is only functional when the PLL is enabled. Determine the MCLK_OUT frequency by the following:

$$MCLK\ Output\ Frequency = (PLL\ Nominal\ Input/4) \times N$$

where:

MCLK Output Frequency is the MCLK_OUT clock frequency.
PLL Nominal Input is the PLL input clock after PLL input divider.
N is selectable in the MCLK_OUT frequency selection register.

Dejitter Circuitry

To account for jitter between ICs in the system and to safely handle interfacing between internal and external clocks, dejitter circuits are included to guarantee that jitter related clocking errors are avoided. The dejitter circuitry is automated and does not require interaction or control from the user.

PIN DRIVE STRENGTH, SLEW RATE, AND PULL CONFIGURATION

Every digital output pin has configurable drive strength and slew rate. This configurability allows the current sourcing ability of the driver to be modified to fit the application circuit. In general, higher drive strength is needed to improve signal integrity when driving high frequency clocks over long distances. Use lower drive strength for lower frequency clock signals, shorter traces, or in cases where reduced system electromagnetic interference (EMI) is desired. Slew rate can be increased if the edges of the clock signal have rise or fall times that are too long. To achieve adequate signal integrity and minimize electromagnetic emissions, use the drive strength and slew rate settings in combination with good mixed signal PCB design practices.

POWER SUPPLIES, VOLTAGE REGULATOR, AND HARDWARE RESET

Power Supplies

Four power supplies (IOVDD, DVDD, CVDD, and PVDD) supply the ADAU1472 as follows:

- IOVDD (input/output supply) sets the reference voltage for all digital input and output pins. IOVDD can be any value ranging from 1.8 V − 5% to 3.3 V + 10%. IOVDD also supplies the low power operation always on domain circuitry.
- DVDD (digital supply) powers the DSP core and supporting digital logic circuitry. DVDD must be 1.2 V ± 5%.
- CVDD (memory supply) powers the memory and memory retention circuitry. CVDD must be supplied anytime DVDD is supplied. CVDD must be 1.2 V ± 5% during normal operation but can be lowered to 0.8 V during low power standby for reduced power consumption memory retention.
- PVDD (PLL supply) powers the PLL and acts as a reference for the voltage controlled oscillator (VCO). PVDD must be supplied even if the PLL is not in use. PVDD must be 1.2 V ± 5%.

Table 23. Power Supply Details

Supply	Voltage	Externally Supplied	Description
IOVDD (Input/Output)	1.8 V − 5% to 3.3 V + 10%	Yes	Input/output support and always on power domain supply
DVDD (Digital), CVDD (Analog), PVDD (PLL)	1.2 V ± 5%	Optional	Can be derived from IOVDD using the internal LDO regulator

Voltage Regulator

The on-chip linear regulator can generate the 1.2 V supply required by the DSP core and other internal digital circuitry from an external source supply. For lowest power operation, turn off the on-chip regulator and use an external switching regulator. Source the linear regulator from the input/output supply (IOVDD), which can range from 1.8 V − 5% to 3.3 V + 10%. A simplified block diagram of the internal structure of the regulator is shown in Figure 19.

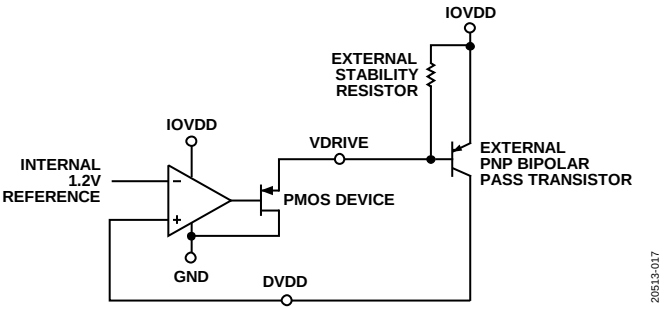


Figure 19. Simplified Block Diagram of Regulator Internal Structure, Including External Components

For proper operation, the linear regulator requires several external components. A PNP bipolar junction transistor acts as an external pass device to bring the higher IOVDD voltage down to the lower DVDD voltage, thus externally dissipating the power of the IC package. Choose a pass transistor with a current gain of the transistor (β) of 200 or greater that dissipates at least 800 mW in the worst case and allows a maximum VDRIVE current sink of 10 mA when IOVDD = 3.3 V or a maximum VDRIVE current sink of 5 mA when IOVDD = 1.8 V. Place a 1 kΩ resistor between the transistor emitter and the base to stabilize the regulator for varying loads. This resistor placement also guarantees that current is always flowing into the VDRIVE pin, even for minimal regulator loads. Figure 20 shows the connection of the external components.

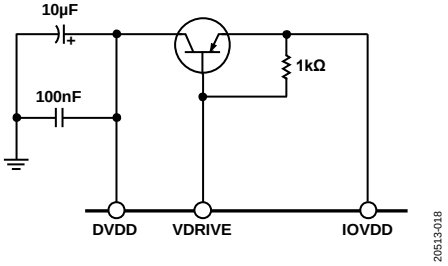


Figure 20. External Components Required for Voltage Regulator Circuit

If an external supply is provided to DVDD, connect an external pull-down resistor (in the range of 10 kΩ) between the VDRIVE pin and ground. Unless the LDO is disabled in the power configuration register, the regulator continues to draw a small amount of current (around 100 µA) from the IOVDD supply.

Do not use the regulator to provide a voltage supply to external ICs. There are no control registers associated with the regulator.

Power Modes

The on-chip power manager manages four typical power states for the processor: off, hard reset, always on mode, or on. Memory mapped registers provide control of the system power states and boot modes.

Always On Operation

Always on operation allows reduced functionality at lower power consumption. Always on capabilities include serial audio input and output routing between Serial Port 1 and Serial Port 2, six PDM microphone inputs, and voice activity detection.

In this mode, only IOVDD is supplied and DVDD is shut off. Only the low power chip peripherals are powered, including the first two serial ports, two PDM microphone inputs, the voice detection, system event controller, audio clock generator, and the SPI slave interface. All other system blocks, including the DSP core, are shut off. The optional memory supply (CVDD) can be supplied in this mode to retain the state of the system memory in between sleep/wake cycling of the system.

To transition to full power mode, a wake-up signal can be generated internally by the voice detector. For this operation mode, two dedicated pins signal the external supply when a power state transition is required. The CVDD_ON pin is pulled high when the CVDD supply is on, and the DVDD_ON pin is pulled high when the DVDD supply is turned on.

Power Reduction

All sections of the IC have a clock gating functionality that allows individual functional blocks to be disabled for power savings. Functional blocks that can optionally be powered down include the following:

- Master clock generator units
- S/PDIF receiver and transmitter
- Serial data input and output ports
- ASRCs
- PDM microphone inputs and outputs

Hardware Reset

An active low hardware reset pin ($\overline{\text{RESET}}$) is available for externally triggering a reset of the device. When this pin is tied to ground, all functional blocks in the device are disabled, and the current consumption decreases dramatically. When the $\overline{\text{RESET}}$ pin is connected to IOVDD, all control registers are reset to their power-on default values. The state of the RAM is not guaranteed to be cleared after a reset. Therefore, the memory must be manually cleared either from an external host processor or by a DSP program.

To ensure that no chatter exists on the $\overline{\text{RESET}}$ signal line, implement an external reset generation circuit in the system hardware design. Figure 21 shows an example of the ADM811 microprocessor supervisory circuit with a push-button connected, providing a method for manually generating a clean $\overline{\text{RESET}}$ signal. For reliability purposes on the application level, place a weak pull-down resistor (in the range of several kΩ) on the $\overline{\text{RESET}}$ line to guarantee that the device is held in reset in the event that the reset supervisory circuitry fails.

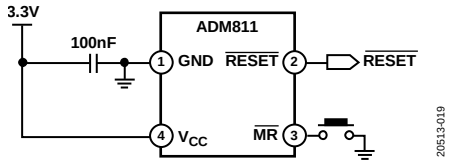


Figure 21. Example Manual Reset Generation Circuit

If the hardware reset function is not required in a system, pull the $\overline{\text{RESET}}$ pin high to the IOVDD supply, using a weak pull-up resistor (in the range of several kΩ). The device is designed to boot properly even when the $\overline{\text{RESET}}$ pin is permanently pulled high.

Software Reset

A soft reset signal is generated by software and allows the device to enter a state similar to when the hardware $\overline{\text{RESET}}$ pin is connected to ground. All control registers are reset to their default values, except the PLL, power control, and the panic manager registers.

A reset can also be generated by the panic manager to reset automatically after an error condition.

INITIALIZATION

Power-Up Sequence

Supply IOVDD prior to any other supply. When IOVDD is stable, then supply CVDD, DVDD, and PVDD. CVDD can be supplied before or at the same time as DVDD and must be supplied any time DVDD is supplied. It is recommended to simultaneously supply DVDD and PVDD. If the internal regulator is used, DVDD, CVDD, and PVDD are generated by the regulator, in combination with an external pass transistor, after IOVDD is supplied. See the Power Supplies section for more information.

Each power supply domain has its own power-on reset circuits to ensure that the supplies reach their nominal level before system operation. The digital circuits are kept in reset until the IOVDD, DVDD, and CVDD supplies meet power-on conditions.

SYSTEM DEBUG

The JTAG debug port provides connectivity for the OCD functions of the DSP core. A list of supported JTAG probes is available on the Cadence Tensilica website. A dedicated JTAG test port is also available for chip boundary scan functions.

DEVELOPMENT TOOLS

The Xtensa® Xplorer IDE provides a graphic interface based on the Eclipse™ platform and includes the optimizing Xtensa C/C++ compiler. Refer to the Cadence Tensilica development tool documentation for more information.

APPLICATIONS INFORMATION

PCB DESIGN CONSIDERATIONS

Ground Plane

A solid ground plane is necessary for maintaining signal integrity and minimizing EMI radiation. If the PCB has two ground planes, the planes can be connected using vias that are spread evenly throughout the board.

Power Supply Planes and Bypass Capacitors

Each of the named supplies (IOVDD, DVDD, CVDD, and PVDD) must be a separate plane.

Bypass each power supply pin to its nearest appropriate ground pin or to the ground plane with a single 100 nF capacitor. Make the connections to each side of the capacitor as short as possible and keep the trace on a single layer with no vias, wherever it is possible. It is important to have bypass capacitors at all four corners of the package. For power pins located on the external perimeter of the ball grid, place the capacitor on the same PCB side and either equidistant from the power or ground pins or, when equidistant placement is not possible, slightly closer to the power pin (see Figure 22). Establish the thermal connections to the planes on the far side of the capacitor.

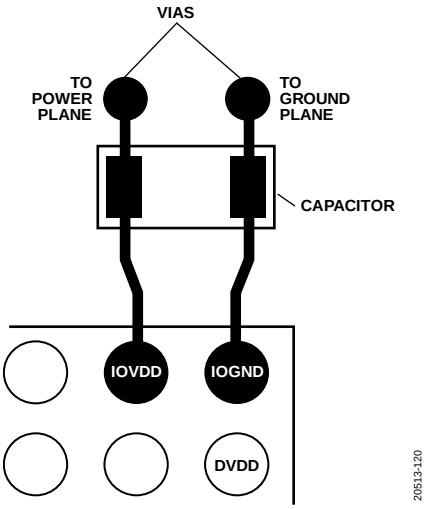


Figure 22. Recommended Power Supply Bypass Capacitor Layout

For power pins located inside the ball grid, place the capacitor on the opposite PCB side. Use a via in the pad for connections to the power and ground planes. It is possible to reduce the number of bypass capacitors to two per each power rail, but the capacitors must be placed on opposite sides of the power pin clusters (see Figure 23).

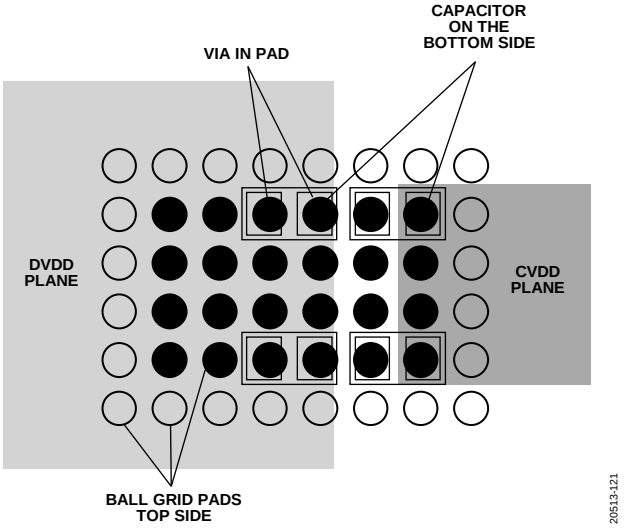


Figure 23. Inside Grid Power Supply Bypass Capacitor Layout

Typically, a single 100 nF capacitor for each power ground pin pair is sufficient. However, if there is excessive high frequency noise in the system, use an additional 10 nF capacitor in parallel. In that case, place the 10 nF capacitor between the ADAU1472 and the 100 nF capacitor and establish the thermal connections on the far side of the 100 nF capacitor.

To provide a current reservoir in case of sudden current spikes, use a 1 µF capacitor at each corner of the chip for each power rail. For example, as DVDD, IOVDD, PVDD, and CVDD power pins are located in each quadrant of the ball grid, there are four 1 µF bulk capacitors for each of the corresponding power planes.

Power Supply Isolation with Ferrite Beads

Ferrite beads can be used for supply isolation. When using ferrite beads, always place the beads outside the local high frequency decoupling capacitors, as shown in Figure 24. If the ferrite beads are placed between the supply pin and the decoupling capacitor, high frequency noise is reflected back into the IC because there is no suitable return path to ground. As a result, EMI increases, creating noisy supplies.

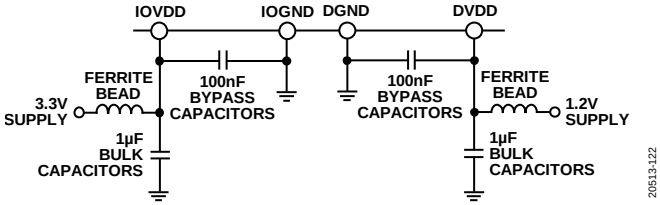


Figure 24. Ferrite Bead Power Supply Isolation Circuit

PCB MANUFACTURING GUIDELINES

Refer to the AN-617 Application Note for wafer level chip scale package (WLCSP) package recommendations. Underfill is recommended and improves WLCSP package reliability.

TYPICAL APPLICATIONS BLOCK DIAGRAMS

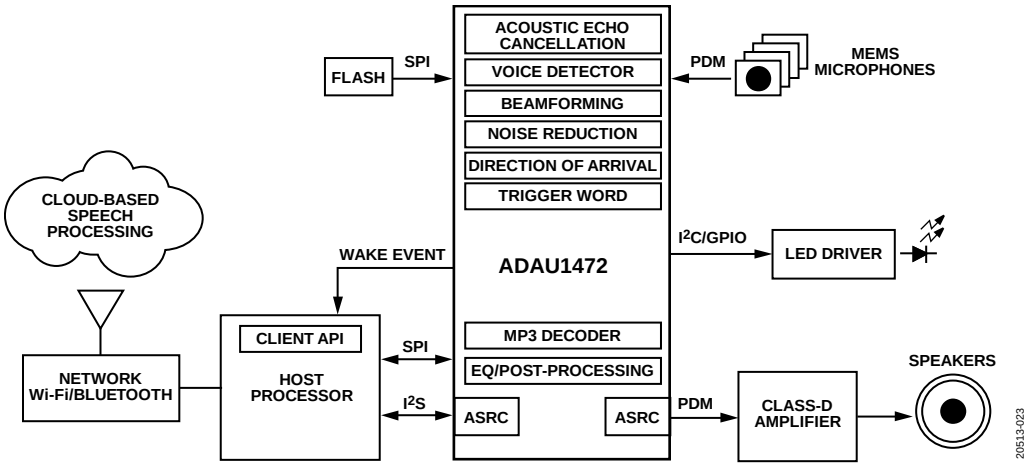


Figure 25. Example of a Voice Interface System, PDM Input/Output

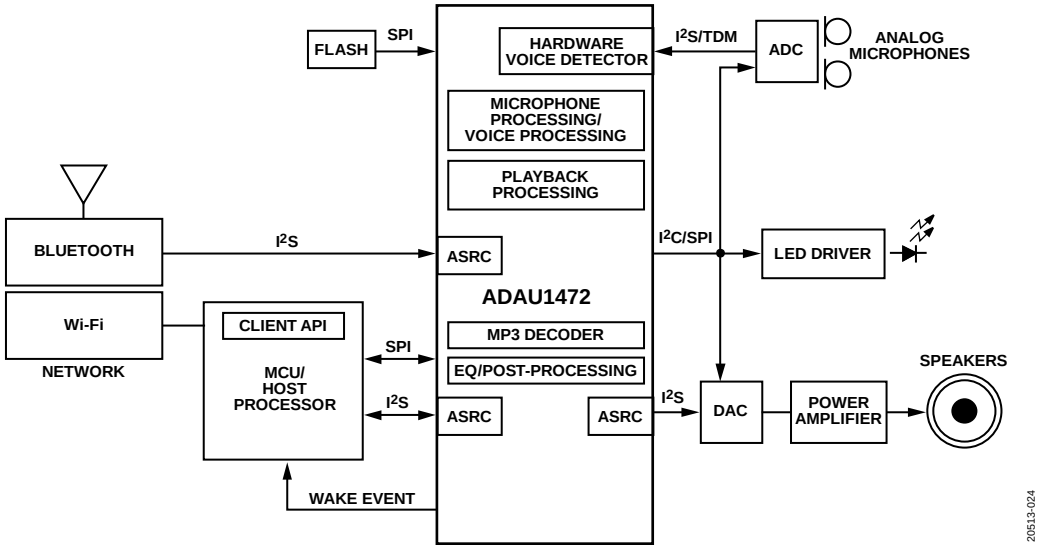


Figure 26. Example of a Voice Interface System, External ADC/DAC

OUTLINE DIMENSIONS

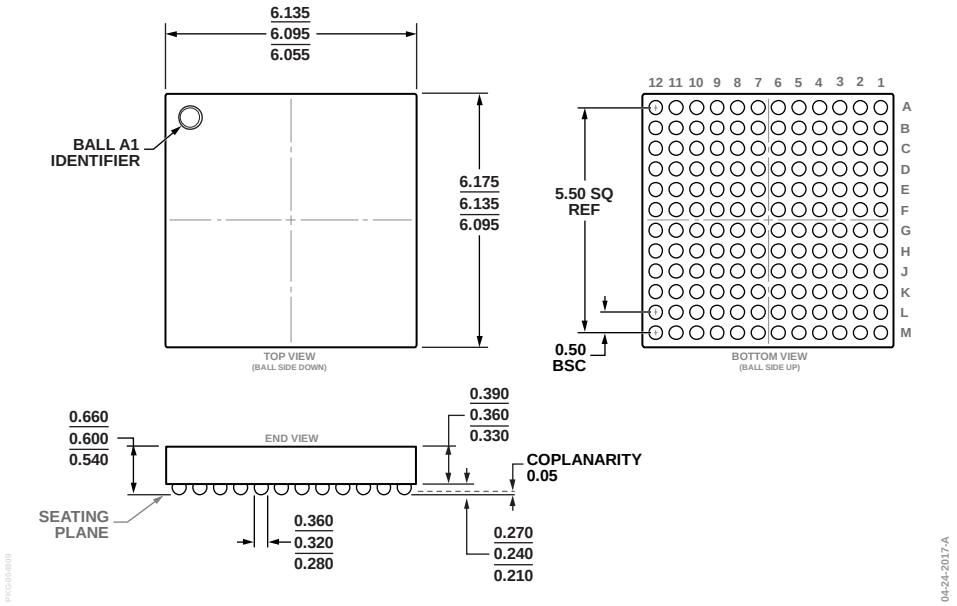


Figure 27. 144-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-144-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADAU1472BCBZRL	0°C to 85°C	144-Ball Wafer Level Chip Scale Package [WLCSP]	CB-144-2
EVAL-ADAU1472Z		Evaluation Board	

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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