ADC08100 8-Bit, 20 Msps to 100 Msps, 1.3 mW/Msps A/D Converter

Check for Samples: ADC08100

FEATURES

- **Single-ended Input**
- **Internal Sample-and-hold Function**
- **Low Voltage (Single +3V) Operation**
- **Small Package**
- **Power-down Feature**

APPLICATIONS

- **Flat Panel Displays**
- **Projection Systems**
- **Set-top Boxes**
- **Battery-powered Instruments**
- **Communications**
- **Medical Scan Converters**
- **X-ray Imaging**
- **High Speed Viterbi Decoders**
- **Astronomy**

KEY SPECIFICATIONS

- **Resolution 8 bits**
- **Maximum Sampling Frequency 100 Msps (Min)**
- **DNL 0.4 LSB (Typ)**
- **ENOB 7.4 Bits (Typ) at f_{IN} = 41 MHz**
- **THD –60 dB (Typ)**
- **Power Consumption**
  - **Operating 1.3 mW/Msps (Typ)**
  - **Power Down: 1 mW (Typ)**

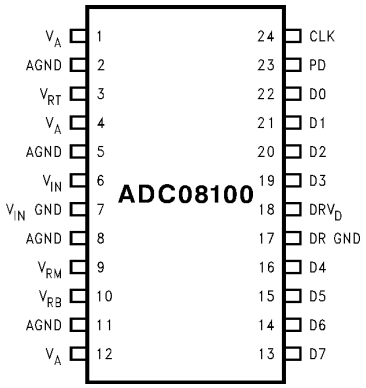
DESCRIPTION

The ADC08100 is a low-power, 8-bit, monolithic analog-to-digital converter with an on-chip track-and-hold circuit. Optimized for low cost, low power, small size and ease of use, this product operates at conversion rates of 20 Msps to 100 Msps with outstanding dynamic performance over its full operating range while consuming just 1.3 mW per MHz of clock frequency. That's just 130 mW of power at 100 Msps. Raising the PD pin puts the ADC08100 into a Power Down mode where it consumes just 1 mW.

The unique architecture achieves 7.4 Effective Bits with 41 MHz input frequency. The excellent DC and AC characteristics of this device, together with its low power consumption and single +3V supply operation, make it ideally suited for many imaging and communications applications, including use in portable equipment. Furthermore, the ADC08100 is resistant to latch-up and the outputs are short-circuit proof. The top and bottom of the ADC08100's reference ladder are available for connections, enabling a wide range of input possibilities. The digital outputs are TTL/CMOS compatible with a separate output power supply pin to support interfacing with 3V or 2.5V logic. The digital inputs (CLK and PD) are TTL/CMOS compatible. The output format is straight binary

The ADC08100 is offered in a 24-lead plastic package (TSSOP) and is specified over the industrial temperature range of −40°C to +85°C.

PIN CONFIGURATION



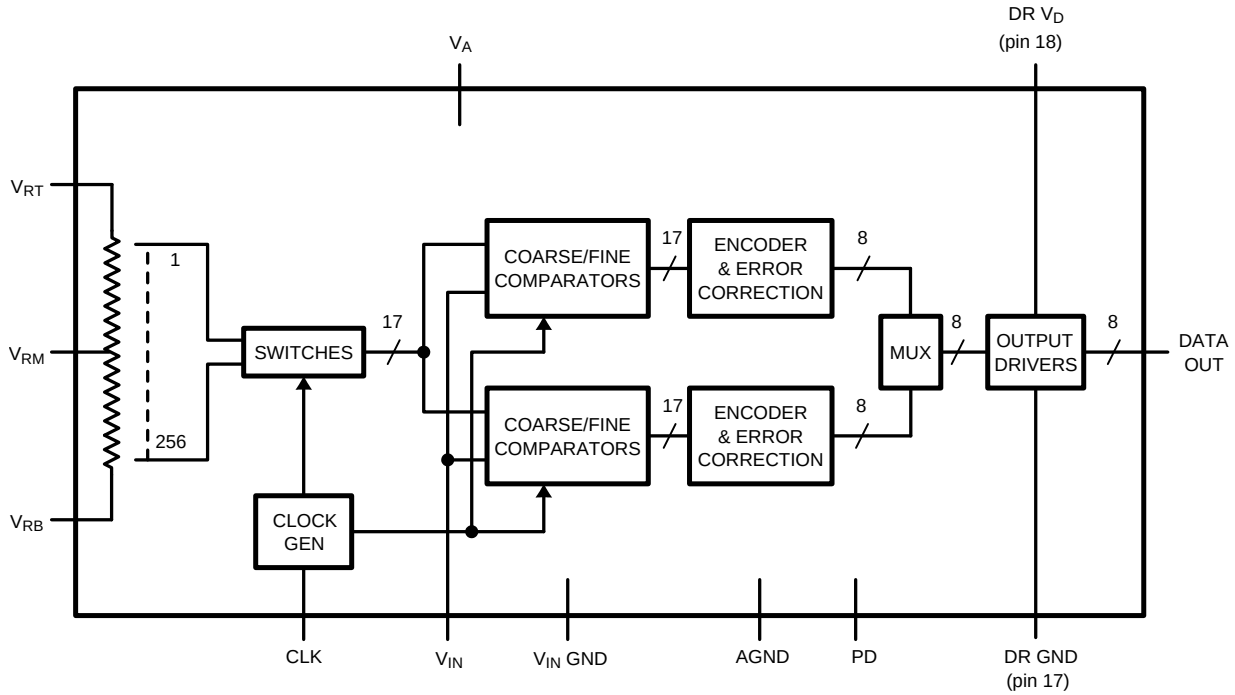
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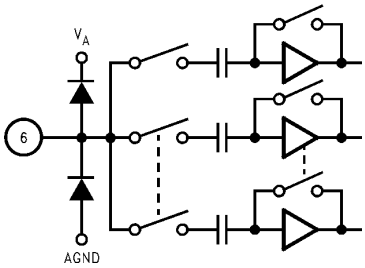
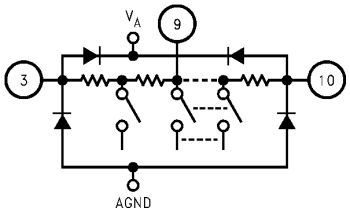
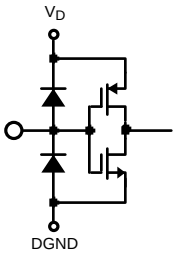
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Block Diagram

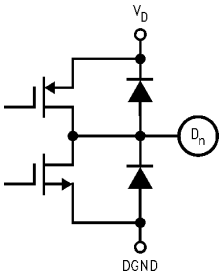


PIN DESCRIPTIONS AND EQUIVALENT CIRCUITS

Pin No.	Symbol	Equivalent Circuit	Description
6	V_{IN}		Analog signal input. Conversion range is V_{RB} to V_{RT}.
3	V_{RT}		Analog Input that is the high (top) side of the reference ladder of the ADC. Nominal range is 1.0V to V_A. Voltage on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See THE ANALOG INPUT for more information.
9	V_{RM}		Mid-point of the reference ladder. This pin should be bypassed to a clean, quiet point in the analog ground plane with a 0.1 µF capacitor.
10	V_{RB}		Analog Input that is the low side (bottom) of the reference ladder of the ADC. Nominal range is 0.0V to (V_{RT} – 1.0V). Voltage on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See THE ANALOG INPUT for more information.
23	PD		Power Down input. When this pin is high, the converter is in the Power Down mode and the data output pins hold the last conversion result.
24	CLK		CMOS/TTL compatible digital clock Input. V_{IN} is sampled on the falling edge of CLK input.

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PIN DESCRIPTIONS AND EQUIVALENT CIRCUITS (continued)

Pin No.	Symbol	Equivalent Circuit	Description
13 thru 16 and 19 thru 22	D0–D7		Conversion data digital Output pins. D0 is the LSB, D7 is the MSB. Valid data is output just after the rising edge of the CLK input.
7	V_{IN} GND		Reference ground for the single-ended analog input, V_{IN}.
1, 4, 12	V_A		Positive analog supply pin. Connect to a clean, quiet voltage source of +3V. V_A should be bypassed with a 0.1 µF ceramic chip capacitor for each pin, plus one 10 µF capacitor. See POWER SUPPLY CONSIDERATIONS for more information.
18	DR V_D		Power supply for the output drivers. If connected to V_A, decouple well from V_A.
17	DR GND		The ground return for the output driver supply.
2, 5, 8, 11	AGND		The ground return for the analog supply.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2][3]

Supply Voltage (V_A)		3.8V
Driver Supply Voltage (DR V_D)		V_A + 0.3V
Voltage on Any Input or Output Pin		−0.3V to V_A
Reference Voltage (V_{RT}, V_{RB})		V_A to AGND
CLK, $\overline{OE}$ Voltage Range		−0.3V to (V_A + 0.3V)
Digital Output Voltage (V_{OH}, V_{OL})		DR GND to DR V_D
Input Current at Any Pin[4]		±25 mA
Package Input Current[4]		±50 mA
Power Consumption at T_A = 25°C		See[5]
ESD Susceptibility[6]	Human Body Model	2500V
	Machine Model	250V
Soldering Temperature, Infrared, 10 seconds		235°C
Storage Temperature		−65°C to +150°C

(1) All voltages are measured with respect to GND = AGND = DR GND = 0V, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see Converter Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) When the input voltage at any pin exceeds the power supplies (that is, less than AGND or DR GND, or greater than V_A or DR V_D), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.
(5) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A) / \theta_{JA}$. In the 24-pin TSSOP, θ_{JA} is 92°C/W. The power consumption of this device under normal operating conditions is far below the package limit, which will be reached only when the ADC08100 is operated in a severe fault condition (e.g., when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.
(6) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through ZERO Ohms.

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Operating Ratings (1) (2)

Operating Temperature Range	$-40°C \le T_A \le +85°C$
Supply Voltage (V_A)	+2.7V to +3.6V
Driver Supply Voltage (DR V_D)	+2.4V to V_A
Ground Difference |GND - DR GND|	0V to 300 mV
Upper Reference Voltage (V_{RT})	1.0V to (V_A + 0.1V)
Lower Reference Voltage (V_{RB})	0V to (V_{RT} − 1.0V)
V_{IN} Voltage Range	V_{RB} to V_{RT}

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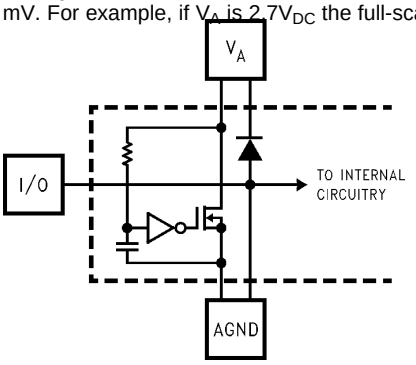
Converter Electrical Characteristics

The following specifications apply for V_A = DR V_D = +3.0V_{DC}, V_{RT} = +1.9V, V_{RB} = 0.3V, C_L = 10 pF, f_{CLK} = 100 MHz at 50% duty cycle. **Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}**: all other limits T_J = 25°C(1)(2)(3)

Symbol	Parameter	Conditions		Typical (4)	Limits (4)	Units (Limits)
DC ACCURACY						
	Resolution with no missing codes				**8**	Bits
INL	Integral Non-Linearity			±0.5	**±1.3**	LSB (max)
DNL	Differential Non-Linearity			±0.4	**+1.0** **−0.95**	LSB (max) LSB (min)
FSE	Full Scale Error			18	±28	mV (max)
V_{OFF}	Zero Scale Offset Error			26	±35	mV (max)
ANALOG INPUT AND REFERENCE CHARACTERISTICS						
V_{IN}	Input Voltage			1.6	**V_{RB}**	V (min)
					V_{RT}	V (max)
C_{IN}	V_{IN} Input Capacitance	V_{IN} = 0.75V +0.5 Vrms	(CLK LOW)	3		pF
			(CLK HIGH)	4		pF
R_{IN}	R_{IN} Input Resistance			>1		MΩ
BW	Full Power Bandwidth			200		MHz
V_{RT}	Top Reference Voltage			1.9	V_A	V (max)
					1.0	V (min)
V_{RB}	Bottom Reference Voltage			0.3	V_{RT} − 1.0	V (max)
					0	V (min)
V_{RT} - V_{RB}	Reference Delta			1.6	1.0	V (min)
					2.3	V (max)
R_{REF}	Reference Ladder Resistance	V_{RT} to V_{RB}		220	**150**	Ω (min)
					300	Ω (max)
I_{REF}	Reference Ladder Current			7.3	**5.3**	mA (min)
					10.6	mA (max)

(1) The Electrical characteristics tables list ensured specifications under the listed Recommended Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations for room temperature only and are not ensured.

(2) The analog inputs are protected as shown below. Input voltage magnitudes up to V_A + 300 mV or to 300 mV below GND will not damage this device. However, errors in the A/D conversion can occur if the input goes above DR V_D or below GND by more than 100 mV. For example, if V_A is 2.7V_{DC} the full-scale input voltage must be ≤2.6V_{DC} to ensure accurate conversions.



(3) To ensure accuracy, it is required that V_A and DR V_D be well bypassed. Each supply pin must be decoupled with separate bypass capacitors.

(4) Typical figures represent most likely parametric norms at T_J = 25°C. Test limits are ensured to TI's AOQL (Average Outgoing Quality Level).

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Converter Electrical Characteristics (continued)

The following specifications apply for V_A = DR V_D = +3.0V_{DC}, V_{RT} = +1.9V, V_{RB} = 0.3V, C_L = 10 pF, f_{CLK} = 100 MHz at 50% duty cycle. **Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}**: all other limits T_J = 25°C(1)(2)(3)

Symbol	Parameter	Conditions	Typical (4)	Limits (4)	Units (Limits)
CLK, PD DIGITAL INPUT CHARACTERISTICS					
V_{IH}	Logical High Input Voltage	DR V_D = V_A = 3.3V		**2.0**	V (min)
V_{IL}	Logical Low Input Voltage	DR V_D = V_A = 2.7V		**0.8**	V (max)
I_{IH}	Logical High Input Current	V_{IH} = DR V_D = V_A = 3.3V	10		nA
I_{IL}	Logical Low Input Current	V_{IL} = 0V, DR V_D = V_A = 2.7V	−50		nA
C_{IN}	Logic Input Capacitance		3		pF
DIGITAL OUTPUT CHARACTERISTICS					
V_{OH}	High Level Output Voltage	V_A = DR V_D = 2.7V, I_{OH} = −400 µA	2.6	**2.4**	V (min)
V_{OL}	Low Level Output Voltage	V_A = DR V_D = 2.7V, I_{OL} = 1.0 mA	0.4	**0.5**	V (max)
DYNAMIC PERFORMANCE					
ENOB	Effective Number of Bits	f_{IN} = 4 MHz, V_{IN} = −0.25 dBFS	7.5		Bits
		f_{IN} = 10 MHz, V_{IN} = −0.25 dBFS	7.5	**7.0**	Bits (min)
		f_{IN} = 41 MHz, V_{IN} = −0.25 dBFS, T_A= 25°C	7.3	6.9	Bits (min)
		f_{IN} = 41 MHz, V_{IN} = −0.25 dBFS, T_A = T_{MIN} to T_{MAX}	7.3	**6.8**	Bits (min)
		f_{IN} = 49.8 MHz, V_{IN} = −0.25 dBFS	7.2		Bits
SINAD	Signal-to-Noise & Distortion	f_{IN} = 4 MHz, V_{IN} = −0.25 dBFS	47		dB
		f_{IN} = 10 MHz, V_{IN} = −0.25 dBFS	47	**43.9**	dB (min)
		f_{IN} = 41 MHz, V_{IN} = −0.25 dBFS, T_A= 25°C	46	43.3	dB (min)
		f_{IN} = 41 MHz, V_{IN} = −0.25 dBFS, T_A = T_{MIN} to T_{MAX}	46	**42.7**	dB (min)
		f_{IN} = 49.8 MHz, V_{IN} = −0.25 dBFS	45		dB
SNR	Signal-to-Noise Ratio	f_{IN} = 4 MHz, V_{IN} = −0.25 dBFS	47		dB
		f_{IN} = 10 MHz, V_{IN} = −0.25 dBFS	47	**44**	dB (min)
		f_{IN} = 41 MHz, V_{IN} = −0.25 dBFS	46.5	**42.8**	dB (min)
		f_{IN} = 49.8 MHz, V_{IN} = −0.25 dBFS	45.8		dB
SFDR	Spurious Free Dynamic Range	f_{IN} = 4 MHz, V_{IN} = −0.25 dBFS	61		dBc
		f_{IN} = 10 MHz, V_{IN} = −0.25 dBFS	60		dBc
		f_{IN} = 41 MHz, V_{IN} = −0.25 dBFS	63		dBc
		f_{IN} = 49.8 MHz, V_{IN} = −0.25 dBFS	54		dBc
THD	Total Harmonic Distortion	f_{IN} = 4 MHz, V_{IN} = −0.25 dBFS	−61		dBc
		f_{IN} = 10 MHz, V_{IN} = −0.25 dBFS	−60		dBc
		f_{IN} = 41 MHz, V_{IN} = −0.25 dBFS	-60		dBc
		f_{IN} = 49.8 MHz, V_{IN} = −0.25 dBFS	−54		dBc
HD2	2nd Harmonic Distortion	f_{IN} = 4 MHz, V_{IN} = −0.25 dBFS	-62		dBc
		f_{IN} = 10 MHz, V_{IN} = −0.25 dBFS	−60		dBc
		f_{IN} = 41 MHz, V_{IN} = −0.25 dBFS	-63		dBc
		f_{IN} = 49.8 MHz, V_{IN} = −0.25 dBFS	−54		dBc
HD3	3rd Harmonic Distortion	f_{IN} = 4 MHz, V_{IN} = FS − 0.25 dB	−68		dBc
		f_{IN} = 10 MHz, V_{IN} = −0.25 dBFS	−65		dBc
		f_{IN} = 41 MHz, V_{IN} = −0.25 dBFS	-64		dBc
		f_{IN} = 49.8 MHz, V_{IN} = −0.25 dBFS	−68		dBc
IMD	Intermodulation Distortion	f_1 = 9 MHz, V_{IN} = −6.25 dBFS f_2 = 10 MHz, V_{IN} = −6.25 dBFS	-48		dBc

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Converter Electrical Characteristics (continued)

The following specifications apply for V_A = DR V_D = +3.0V_{DC}, V_{RT} = +1.9V, V_{RB} = 0.3V, C_L = 10 pF, f_{CLK} = 100 MHz at 50% duty cycle. **Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}**: all other limits T_J = 25°C(1)(2)(3)

Symbol	Parameter	Conditions	Typical (4)	Limits (4)	Units (Limits)
POWER SUPPLY CHARACTERISTICS					
I_A	Analog Supply Current	DC Input	41	50	mA (max)
		f_{IN} = 10 MHz, V_{IN} = −3 dBFS	41		mA (max)
DR I_D	Output Driver Supply Current(5)	DC Input	1	2	mA (max)
		f_{IN} = 10 MHz, V_{IN} = −3 dBFS	8		mA (max)
I_A + DR I_D	Total Operating Current	DC Input	42	52	mA (max)
		f_{IN} = 10 MHz, V_{IN} = −3 dBFS, PD = Low	49		
		CLK Low, PD = Hi	0.2		
PC	Power Consumption	DC Input	126	**156**	mW (max)
		f_{IN} = 10 MHz, V_{IN} = −3 dBFS, PD = Low	147		mW
		CLK Low, PD = Hi	0.6		mW
$PSRR_1$	Power Supply Rejection Ratio	FSE change with 2.7V to 3.3V change in V_A	54		dB
$PSRR_2$	Power Supply Rejection Ratio	Rejection of 150 mV at 9.8 MHz riding upon supply	33		dB
AC ELECTRICAL CHARACTERISTICS					
f_{C1}	Maximum Conversion Rate		125	**100**	MHz (min)
f_{C2}	Minimum Conversion Rate		20		MHz
t_{CL}	Minimum Clock Low Time			**4.5**	ns (min)
t_{CH}	Minimum Clock High Time			**4.5**	ns (min)
t_{OH}	Output Hold Time	CLK Rise to Data Invalid	4.4		ns
t_{OD}	Output Delay	CLK Rise to Data Valid	5.9	**8.5**	ns (max)
	Pipeline Delay (Latency)		2.5		Clock Cycles
t_{AD}	Sampling (Aperture) Delay	CLK Fall to Acquisition of Data	1.5		ns
t_{AJ}	Aperture Jitter		2		ps rms

(5) I_{DR} is the current consumed by the switching of the output drivers and is primarily determined by the load capacitance on the output pins, the supply voltage, V_{DR}, and the rate at which the outputs are switching (which is signal dependent), $I_{DR} = V_{DR} (C_O \times f_O + C_1 \times f_1 + \ldots + C_{71} \times f_7)$ where V_{DR} is the output driver power supply voltage, C_n is the total capacitance on any given output pin, and f_n is the average frequency at which that pin is toggling.

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Specification Definitions

APERTURE (SAMPLING) DELAY is that time required after the fall of the clock input for the sampling switch to open. The Sample/Hold circuit effectively stops capturing the input signal and goes into the "hold" mode t_{AD} after the clock goes low.

APERTURE JITTER is the variation in aperture delay from sample to sample. Aperture jitter shows up as input noise.

BOTTOM OFFSET is the difference between the input voltage that just causes the output code to transition to the first code and the negative reference voltage. Bottom Offset is defined as $E_{OB} = V_{ZT} – V_{RB}$, where V_{ZT} is the first code transition input voltage. V_{RB} is the lower reference voltage. Note that this is different from the normal Zero Scale Error.

CLOCK DUTY CYCLE is the ratio of the time that the clock waveform is at a logic high to the total time of one clock period.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB. Measured at 100 Msps with a ramp input.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as (SINAD – 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input. The test is performed with f_{IN} equal to 100 kHz plus integer multiples of f_{CLK}. The input frequency at which the output is −3 dB relative to the low frequency input signal is the full power bandwidth.

FULL-SCALE ERROR is a measure of how far the last code transition is from the ideal 1½ LSB below V_{RT} and is defined as:

$$V_{max} + 1.5 \text{ LSB} – V_{RT}$$

where

- $_{max}$ is the voltage at which the transition to the maximum (full scale) code occurs. (1)

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from zero scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value. The end point test method is used. Measured at 100 Msps with a ramp input.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the second and third order intermodulation products to the power in one of the original frequencies. IMD is usually expressed in dBFS.

MISSING CODE are those output codes that are skipped and will never appear at the ADC outputs. These codes cannot be reached with any input value.

OUTPUT DELAY is the time delay after the rising edge of the input clock before the data update is present at the output pins.

OUTPUT HOLD TIME is the length of time that the output data is valid after the rise of the input clock.

PIPELINE DELAY (LATENCY) is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. New data is available at every clock cycle, but the data lags the conversion by the Pipeline Delay plus the Output Delay.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or DC.

SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding D.C.

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SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal at the output and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB, of the total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$THD = 20 \times \log \sqrt{\frac{f_2^2+f_3^2+f_4^2+f_5^2+f_6^2+f_7^2+f_8^2+f_9^2+f_{10}^2}{f_1^2}} \quad (2)$$

where

- where F_1 is the RMS power of the fundamental (input) frequency and f_2 through f_{10} is the power in the first 9 harmonics in the output spectrum.

ZERO SCALE OFFSET ERROR is the error in the input voltage required to cause the first code transition. It is defined as

$$V_{OFF} = V_{ZT} - V_{RB} \quad (3)$$

where

- where V_{ZT} is the first code transition input voltage.

Timing Diagram

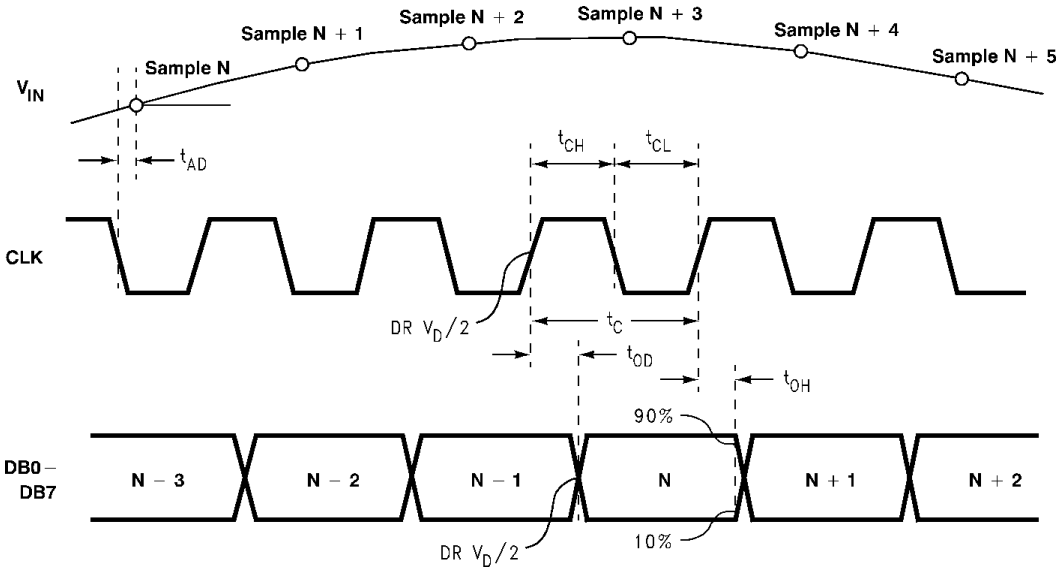


Figure 1. ADC08100 Timing Diagram

Typical Performance Characteristics

V_A = DR V_D = 3V, f_{CLK} = 100 MHz, f_{IN} = 41 MHz, unless otherwise stated

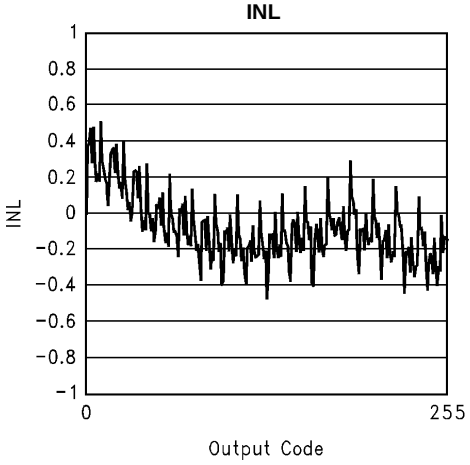


Figure 2.

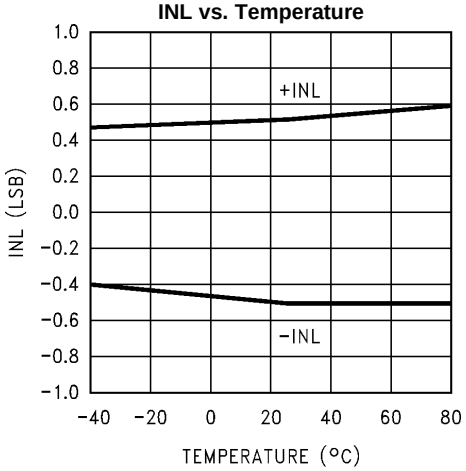


Figure 3.

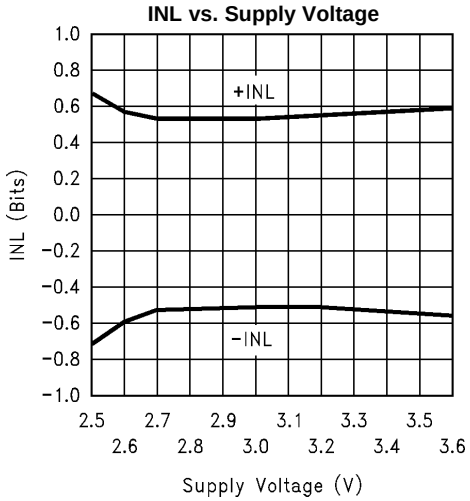


Figure 4.

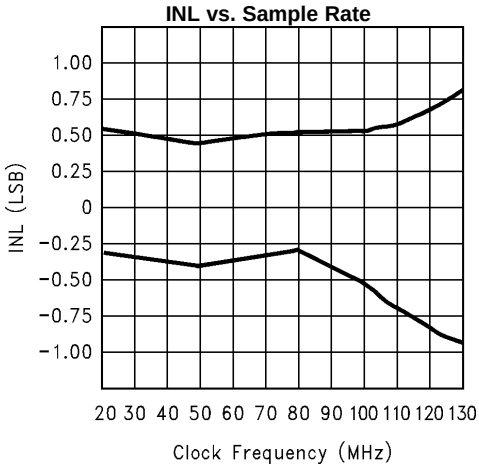


Figure 5.

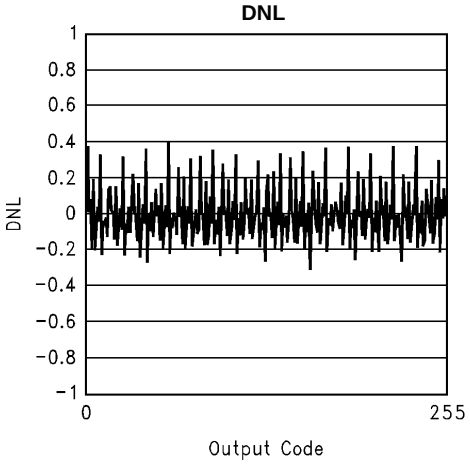


Figure 6.

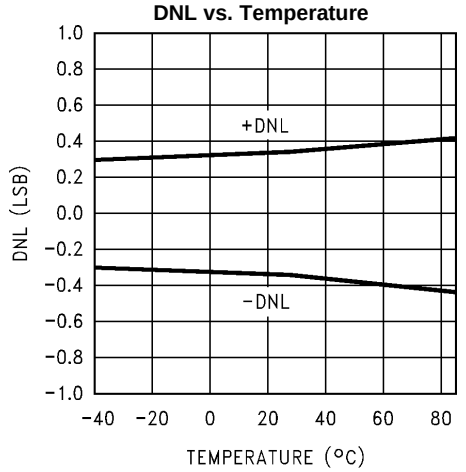


Figure 7.

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Typical Performance Characteristics (continued)

V_A = DR V_D = 3V, f_{CLK} = 100 MHz, f_{IN} = 41 MHz, unless otherwise stated

DNL vs. Supply Voltage

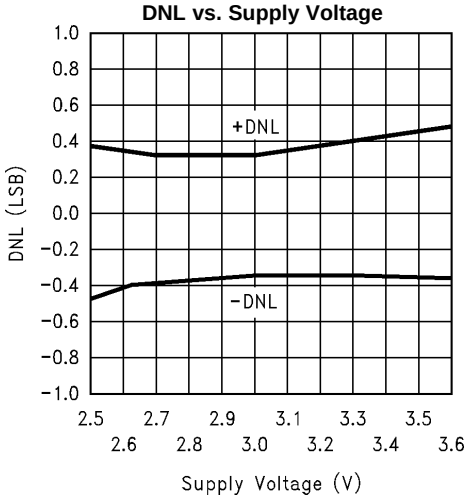


Figure 8.

DNL vs. Sample Rate

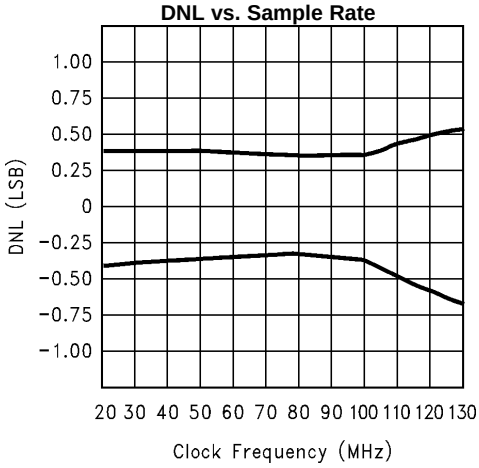


Figure 9.

SNR vs. Temperature

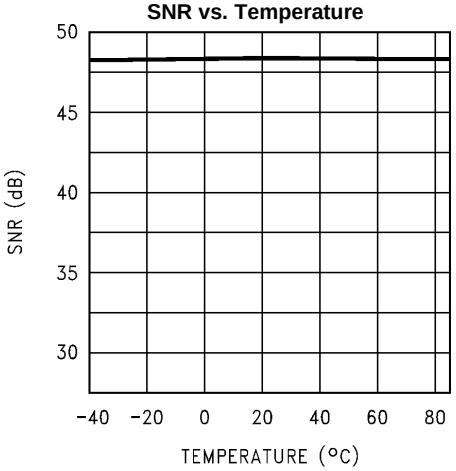


Figure 10.

SNR vs. Supply Voltage

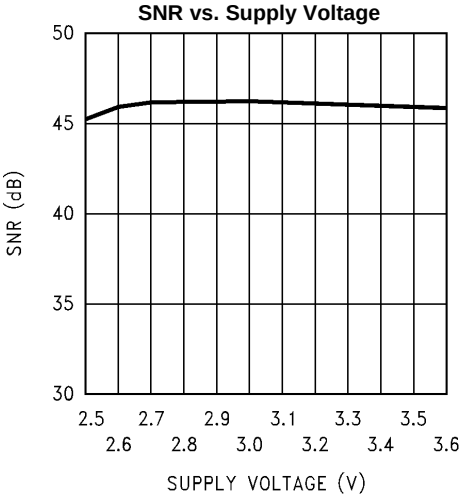


Figure 11.

SNR vs. Sample Rate

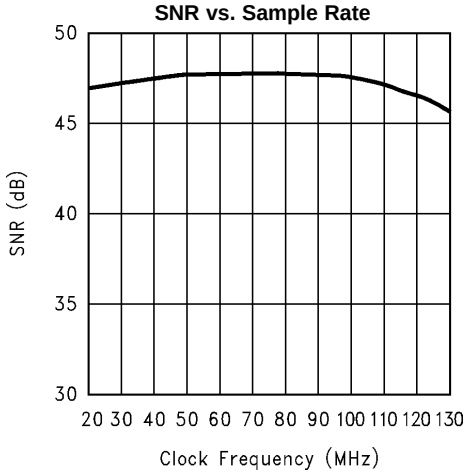


Figure 12.

SNR vs. Input Frequency

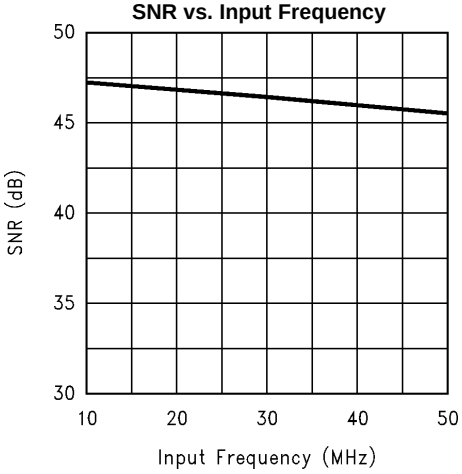


Figure 13.

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Typical Performance Characteristics (continued)

V_A = DR V_D = 3V, f_{CLK} = 100 MHz, f_{IN} = 41 MHz, unless otherwise stated

SNR vs. Clock Duty Cycle

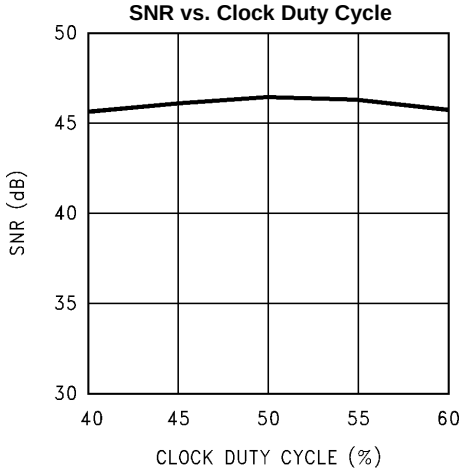


Figure 14.

Distortion vs. Temperature

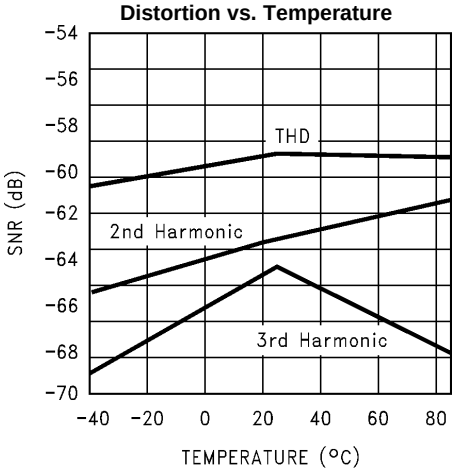


Figure 15.

Distortion vs. Supply Voltage

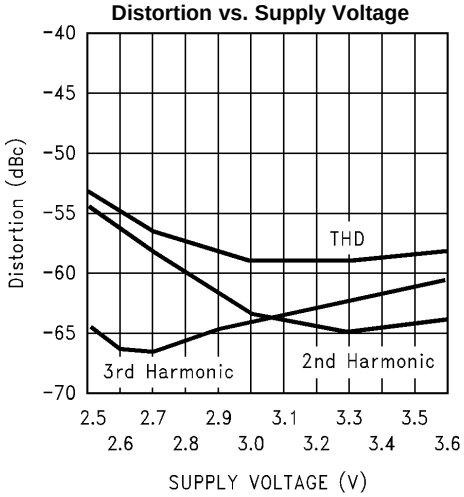


Figure 16.

Distortion vs. Sample Rate

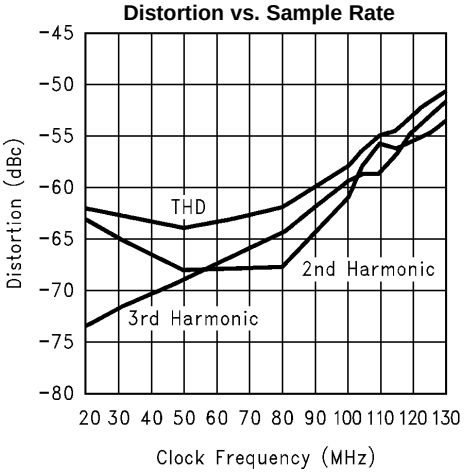


Figure 17.

Distortion vs. Input Frequency

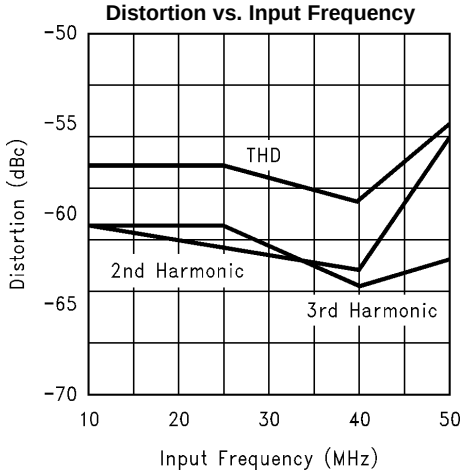


Figure 18.

Distortion vs. Clock Duty Cycle

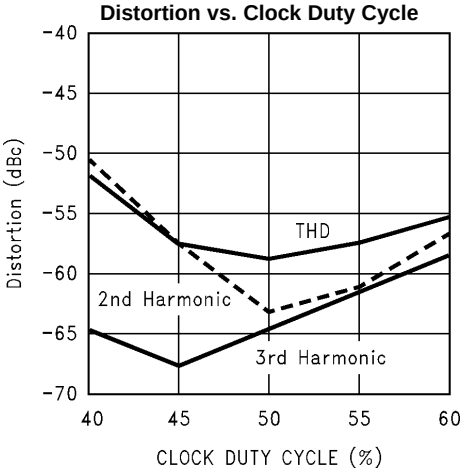


Figure 19.

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Typical Performance Characteristics (continued)

V_A = DR V_D = 3V, f_{CLK} = 100 MHz, f_{IN} = 41 MHz, unless otherwise stated

SINAD/ENOB vs. Temperature

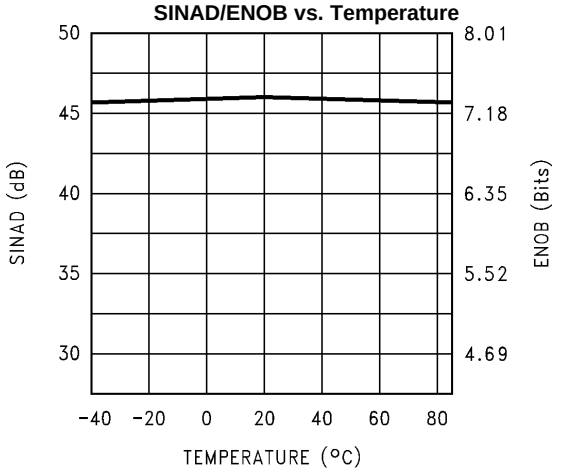


Figure 20.

SINAD/ENOB vs. Supply Voltage

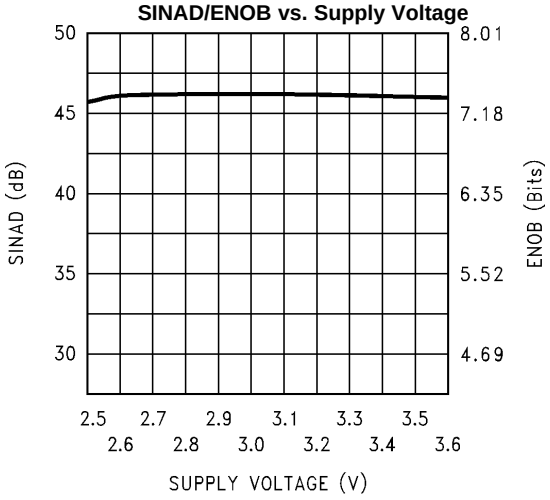


Figure 21.

SINAD/ENOB vs. Sample Rate

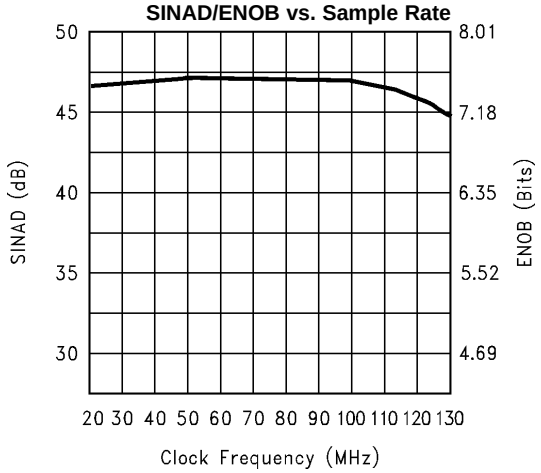


Figure 22.

SINAD/ENOB vs. Input Frequency

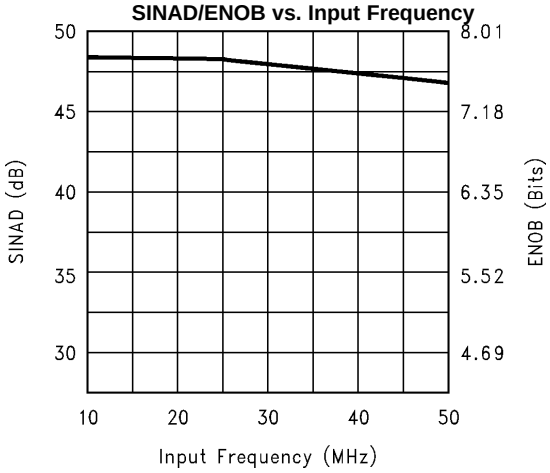


Figure 23.

SINAD/ENOB vs. Clock Duty Cycle

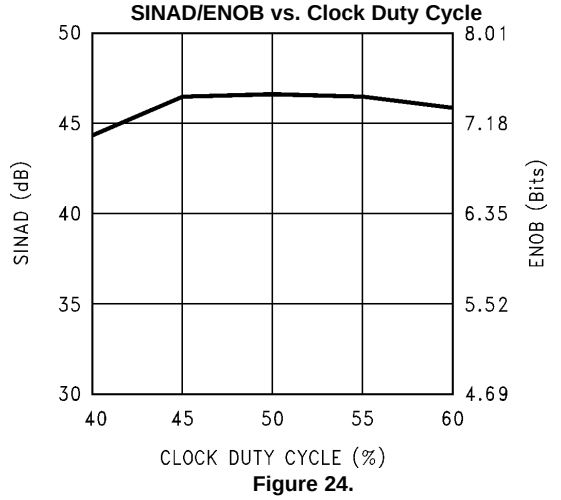


Figure 24.

Power Consumption vs. Sample Rate

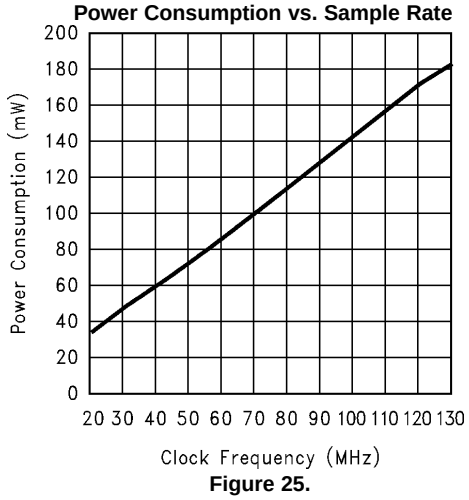


Figure 25.

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Typical Performance Characteristics (continued)

V_A = DR V_D = 3V, f_{CLK} = 100 MHz, f_{IN} = 41 MHz, unless otherwise stated

Spectral Response @ f_{IN} = 10 MHz

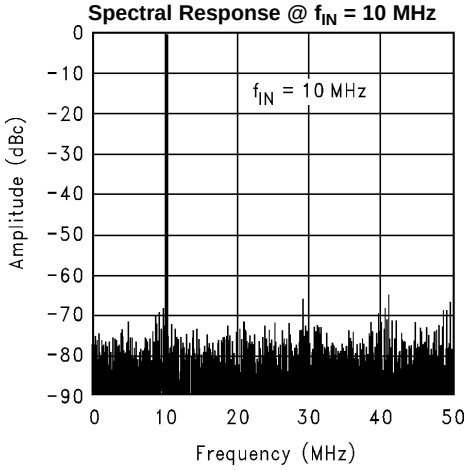


Figure 26.

Spectral Response @ f_{IN} = 41 MHz

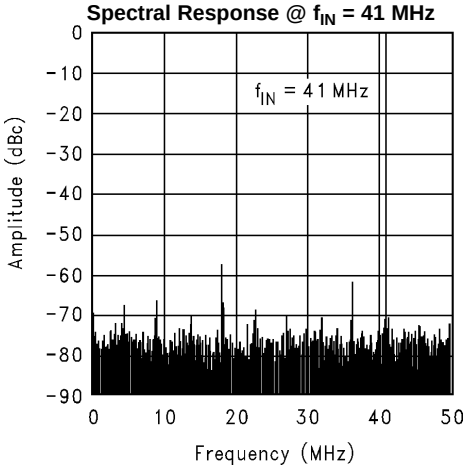


Figure 27.

Spectral Response @ f_{IN} = 76 MHz

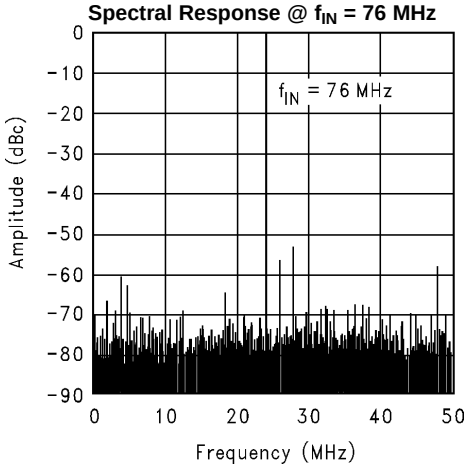


Figure 28.

Intermodulation Distortion (IMD)

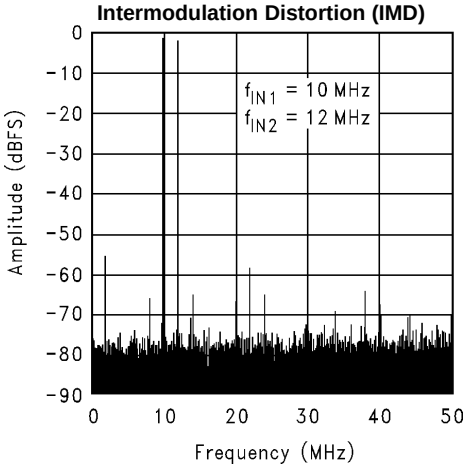


Figure 29.

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FUNCTIONAL DESCRIPTION

The ADC08100 uses a new, unique architecture that achieves over 7 effective bits at input frequencies up to and beyond 50 MHz.

The analog input signal that is within the voltage range set by V_{RT} and V_{RB} is digitized to eight bits. Input voltages below V_{RB} will cause the output word to consist of all zeroes. Input voltages above V_{RB} will cause the output word to consist of all ones.

Incorporating a switched capacitor bandgap, the ADC08100 exhibits a power consumption that is proportional to frequency, limiting power consumption to what is needed at the clock rate that is used. This and its excellent performance over a wide range of clock frequencies makes it an ideal choice as a single ADC for many 8-bit needs.

Data is acquired at the falling edge of the clock and the digital equivalent of that data is available at the digital outputs 2.5 clock cycles plus t_{OD} later. The ADC08100 will convert as long as the clock signal is present. The output coding is straight binary.

The device is in the active state when the Power Down pin (PD) is low. When the PD pin is high, the device is in the power down mode, where the output pins hold the last conversion before the PD pin went high and the device consumes just 1 mW.

Applications Information

REFERENCE INPUTS

The reference inputs V_{RT} and V_{RB} are the top and bottom of the reference ladder, respectively. Input signals between these two voltages will be digitized to 8 bits. External voltages applied to the reference input pins should be within the range specified in Operating Ratings. Any device used to drive the reference pins should be able to source sufficient current into the V_{RT} pin and sink sufficient current from the V_{RB} pin.

The reference bias circuit of Figure 30 is very simple and the performance is adequate for many applications. However, circuit tolerances will lead to a wide reference voltage range. Superior performance can generally be achieved by driving the reference pins with low impedance sources.

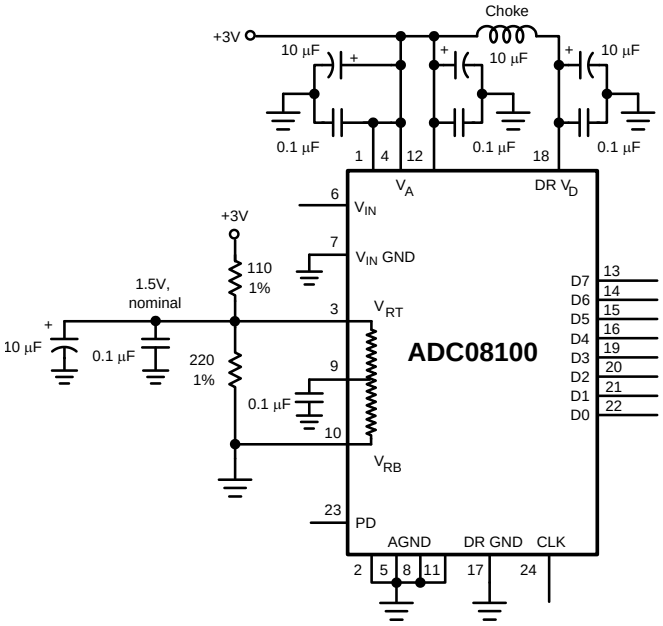
The circuit of Figure 31 will allow a more accurate setting of the reference voltages. The upper amplifier must be able to source the reference current as determined by the value of the reference resistor and the value of (V_{RT} − V_{RB}). The lower amplifier must be able to sink this reference current. Both should be stable with a capacitive load. The *LM8272* was chosen because of its rail-to-rail input and output capability, its high current output and its ability to drive large capacitance loads.

The divider resistors at the inputs to the amplifiers could be changed to suit the application reference voltage needs, or the divider can be replaced with potentiometers or DACs for precise settings. The bottom of the ladder (V_{RB}) may be returned to ground if the minimum input signal excursion is 0V.

V_{RT} should always be more positive than V_{RB} by the minimum V_{RT} - V_{RB} difference in the Electrical Characteristics table to minimize noise. Furthermore, the difference between V_{RT} and V_{RB} should not exceed the maximum value specified in Converter Electrical Characteristics to avoid signal distortion.

The V_{RM} pin is the center of the reference ladder and should be bypassed to a clean, quiet point in the analog ground plane with a 0.1 µF capacitor. DO NOT allow this pin to float.

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Because of the ladder and external resistor tolerances, the reference voltage can vary too much for some applications.

Figure 30. Simple, Low Component Count Reference Biasing

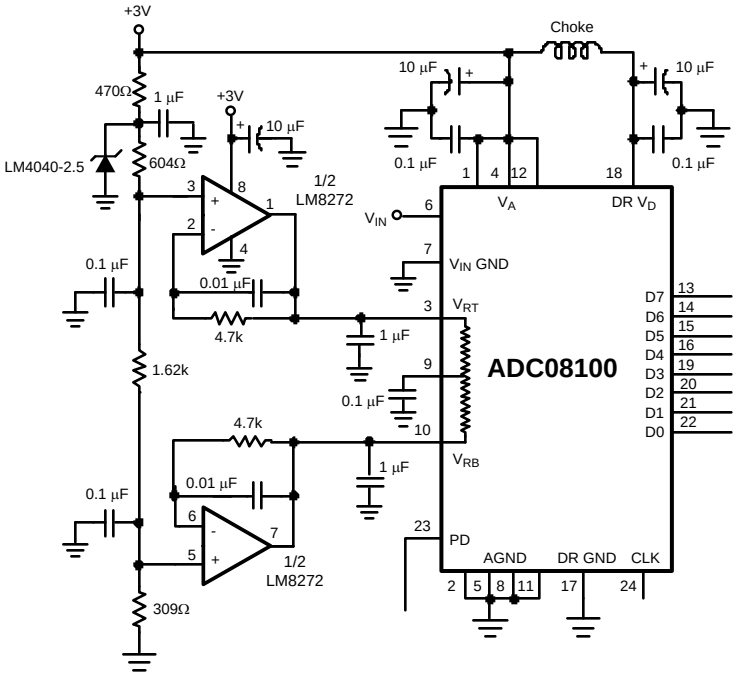


Figure 31. Driving the Reference to Force Desired Values Requires Driving With a Low Impedance Source

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THE ANALOG INPUT

The analog input of the ADC08100 is a switch followed by an integrator. The input capacitance changes with the clock level, appearing as 3 pF when the clock is low, and 4 pF when the clock is high. The sampling nature of the analog input causes current spikes at the input that result in voltage spikes there. Any amplifier used to drive the analog input must be able to settle within the clock high time. The LMH6702 and the LMH6628 have been found to be good amplifiers to drive the ADC08100.

Figure 32 shows an example of an input circuit using the LMH6702. Any input amplifier should incorporate some gain as operational amplifiers exhibit better phase margin and transient response with gains above 2 or 3 than with unity gain. If an overall gain of less than 3 is required, attenuate the input and operate the amplifier at a higher gain, as shown in Figure 32.

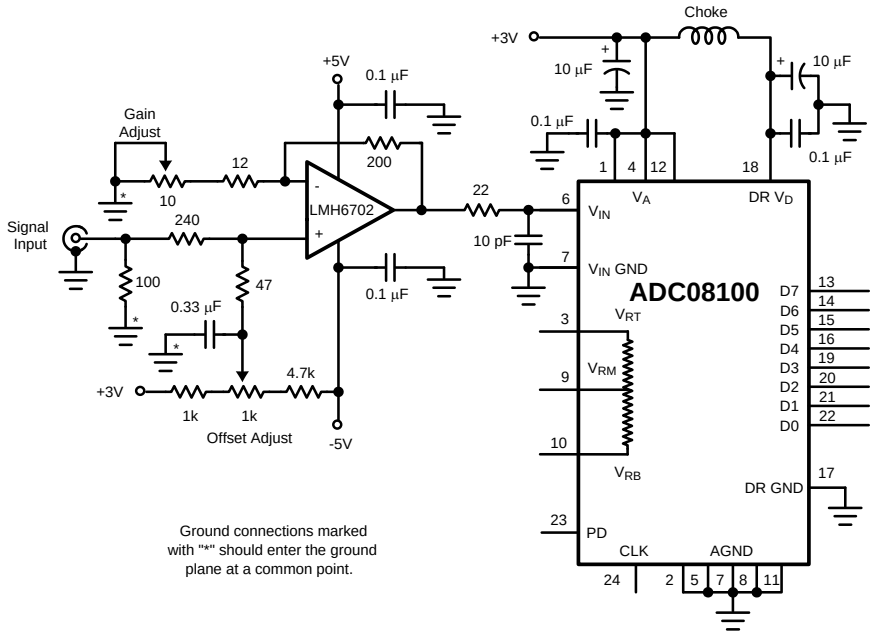


Figure 32. The Input Amplifier Should Incorporate Some Gain for Best Performance (see text)

The RC at the amplifier output filters the clock rate energy that comes out of the analog input due to the input sampling circuit. The optimum time constant for this circuit depends not only upon the amplifier and ADC, but also on the circuit layout and board material. A resistor value should be chosen between 18Ω and 47Ω and the capacitor value chose according to the formula:

$$C = \frac{1}{2 \bullet \pi \bullet R \bullet f_{CLK}} \quad (4)$$

The value of "C" in the formula above should include the ADC input capacitance when the clock is high.

This will provide optimum SNR performance for Nyquist applications. Best THD performance is realized when the capacitor and resistor values are both zero, but this would compromise SNR and SINAD performance. Generally, there should be no resistor or capacitor between the ADC input and any amplifier for undersampling applications.

The circuit of Figure 32 has both gain and offset adjustments. If you eliminate these adjustments normal circuit tolerances may cause signal clipping unless care is exercised in the worst case analysis of component tolerance and the input signal excursion is appropriately limited to account for the worst case conditions. Of course, this means that the designer will not be able to depend upon getting a full scale output with maximum signal input.

Full scale and offset adjustments may also be made by adjusting V_{RT} and V_{RB}, perhaps with the aid of a pair of DACs.

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POWER SUPPLY CONSIDERATIONS

A/D converters draw sufficient transient current to corrupt their own power supplies if not adequately bypassed. A 10 µF tantalum or aluminum electrolytic capacitor should be placed within an inch (2.5 cm) of the A/D power pins, with a 0.1 µF ceramic chip capacitor placed within one centimeter of the converter's power supply pins. Leadless chip capacitors are preferred because they have low lead inductance.

While a single voltage source is recommended for the V_A and DR V_D supplies of the ADC08100, these supply pins should be well isolated from each other to prevent any digital noise from being coupled into the analog portions of the ADC. A choke or 27Ω resistor is recommended between these supply lines with adequate bypass capacitors close to the supply pins.

As is the case with all high speed converters, the ADC08100 should be assumed to have little power supply rejection. None of the supplies for the converter should be the supply that is used for other digital circuitry in any system with a lot of digital power being consumed. The ADC supplies should be the same supply used for other analog circuitry.

No pin should ever have a voltage on it that is in excess of the supply voltage or below ground by more than 300 mV, not even on a transient basis. This can be a problem upon application of power and power shut-down. Be sure that the supplies to circuits driving any of the input pins, analog or digital, do not come up any faster than does the voltage at the ADC08100 power pins.

THE DIGITAL INPUT PINS

The ADC08100 has two digital input pins: The PD pin and the Clock pin.

The PD Pin

The Power Down (PD) pin, when high, puts the ADC08100 into a low power mode where power consumption is reduced to 1 mW. Output data is valid and accurate about 1 microsecond after the PD pin is brought low.

The digital output pins retain the last conversion output code when either the clock is stopped or the PD pin is high.

The ADC08100 Clock

Although the ADC08100 is tested and its performance is ensured with a 100 MHz clock, it typically will function well with clock frequencies from 20 MHz to 125 MHz.

Halting the clock will provide nearly as much power saving as raising the PD pin high. Typical power consumption with a stopped clock is 3 mW, compared to 1 mW when PD is high. The digital outputs will remain in the same state as they were before the clock was halted.

Once the clock is restored (or the PD pin is brought low), there is a time of about 1 microsecond before the output data is valid. However, because of the linear relationship between total power consumption and clock frequency, the part requires about one microsecond after the clock is restarted or substantially changed in frequency before the part returns to its specified accuracy.

The low and high times of the clock signal can affect the performance of any A/D Converter. Because achieving a precise duty cycle is difficult, the ADC08100 is designed to maintain performance over a range of duty cycles. While it is specified and performance is ensured with a 50% clock duty cycle and 100 Msps, ADC08100 performance is typically maintained with clock high and low times of 2 ns, corresponding to a clock duty cycle range of 20% to 80% with a 100 MHz clock. Note that the clock high and low times of 2 ns may not be asserted together.

The **CLOCK** line should be series terminated at the clock source in the characteristic impedance of that line. If the clock line is longer than

$$\frac{t_r}{6 \times t_{PD}}$$

where

- t_r is the clock rise time
- t_{PD} is the propagation rate of the signal along the trace (5)

The **CLOCK** pin should be a.c. terminated with a series RC to ground such that the resistor value is equal to the characteristic impedance of the clock line and the capacitor value is:

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$$C \geq \frac{4 \times t_{PD} \times L}{Z_o}$$

where

- t_{PD} is the signal propagation rate down the clock line (6)

"L" is the line length and Z_o is the characteristic impedance of the clock line. This termination should be located as close as possible to, but within one centimeter of, the ADC08100 clock pin. Typical t_{PD} is about 150 ps/inch on FR-4 board material. For FR-4 board material, the value of C becomes

$$C \geq \frac{6 \times 10^{-10} \times L}{Z_o}$$

where

- L is the length of the clock line in inches. (7)

LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. A combined analog and digital ground plane should be used.

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise because of the skin effect. Total surface area is more important than is total ground plane volume. Capacitive coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance that may seem impossible to isolate and remedy. The solution is to keep the analog circuitry well separated from the digital circuitry.

High power digital components should not be located on or near a straight line between the ADC or any linear component and the power supply area as the resulting common return current path could cause fluctuation in the analog input “ground” return of the ADC.

The DR Gnd connection to the ground plane should not use the same feedthrough use by other ground connections.

Generally, analog and digital lines should cross each other at 90° to avoid getting digital noise into the analog path. In high frequency systems, however, avoid crossing analog and digital lines altogether. Clock lines should be isolated from ALL other lines, analog AND digital. Even the generally accepted 90° crossing should be avoided as even a little coupling can cause problems at high frequencies. Best performance at high frequencies is obtained with a straight signal path.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input and ground should be connected to a very clean point in the analog ground plane.

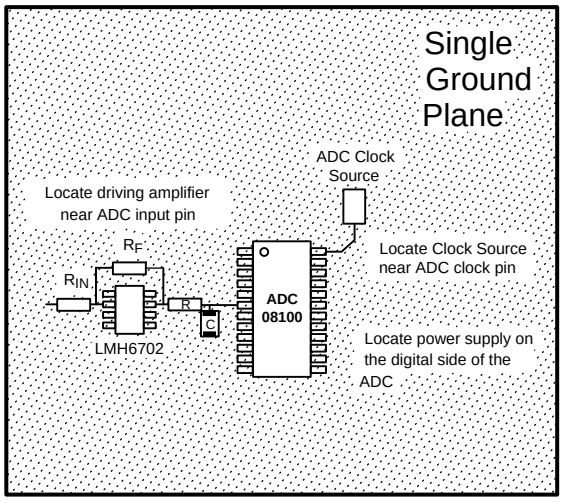


Figure 33. Layout Example

Figure 33 gives an example of a suitable layout. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed together away from any digital components.

DYNAMIC PERFORMANCE

The ADC08100 is AC tested and its dynamic performance is ensured. To meet the published specifications, the clock source driving the CLK input must exhibit less than 3 ps (rms) of jitter. For best AC performance, isolating the ADC clock from any digital circuitry should be done with adequate buffers, as with a clock tree. See Figure 34.

It is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce jitter into the clock signal. The clock signal can also introduce noise into the analog path.

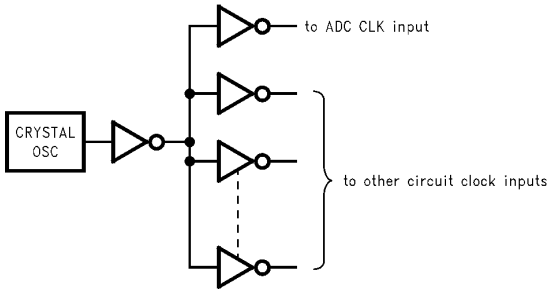


Figure 34. Isolating the ADC Clock from Digital Circuitry

COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For proper operation, all inputs should not go more than 300 mV below the ground pins or 300 mV above the supply pins. Exceeding these limits on even a transient basis may cause faulty or erratic operation. It is not uncommon for high speed digital circuits (e.g., 74F and 74AC devices) to exhibit undershoot that goes more than a volt below ground. A 51Ω resistor in series with the offending digital input will usually eliminate the problem.

Care should be taken not to overdrive the inputs of the ADC08100. Such practice may lead to conversion inaccuracies and even to device damage.

Attempting to drive a high capacitance digital data bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current is required from DR V_D and DR GND. These large charging current spikes can couple into the analog section, degrading dynamic performance. Buffering the digital data outputs (with a 74F541, for example) may be necessary if the data bus capacitance exceeds 10 pF. Dynamic performance can also be improved by adding 100Ω series resistors at each digital output, reducing the energy coupled back into the converter input pins.

Using an inadequate amplifier to drive the analog input. As explained in THE ANALOG INPUT, the capacitance seen at the input alternates between 3 pF and 4 pF with the clock. This dynamic capacitance is more difficult to drive than is a fixed capacitance, and should be considered when choosing a driving device. The LMH6702 and the LMH6628 have been found to be good devices for driving the ADC08100.

Driving the V_{RT} pin or the V_{RB} pin with devices that can not source or sink the current required by the ladder. As mentioned in REFERENCE INPUTS, care should be taken to see that any driving devices can source sufficient current into the V_{RT} pin and sink sufficient current from the V_{RB} pin. If these pins are not driven with devices than can handle the required current, these reference pins will not be stable, resulting in a reduction of dynamic performance.

Using a clock source with excessive jitter, using an excessively long clock signal trace, or having other signals coupled to the clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR performance. The use of simple gates with RC timing is generally inadequate as a clock source.

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REVISION HISTORY

Changes from Revision H (May 2013) to Revision I	Page
• Changed layout of National Data Sheet to TI format	20

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC08100CIMTC/NOPB	Active	Production	TSSOP (PW) | 24	61 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	ADC08100 CIMTC
ADC08100CIMTC/NOPB.A	Active	Production	TSSOP (PW) | 24	61 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	ADC08100 CIMTC
ADC08100CIMTC/NOPB.B	Active	Production	TSSOP (PW) | 24	61 | TUBE	-	Call TI	Call TI	-40 to 85	
ADC08100CIMTCX/NO.A	Active	Production	TSSOP (PW) | 24	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	ADC08100 CIMTC
ADC08100CIMTCX/NO.B	Active	Production	TSSOP (PW) | 24	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
ADC08100CIMTCX/NOPB	Active	Production	TSSOP (PW) | 24	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	ADC08100 CIMTC

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

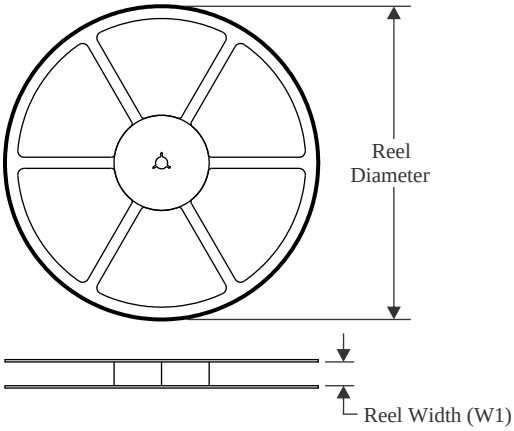
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

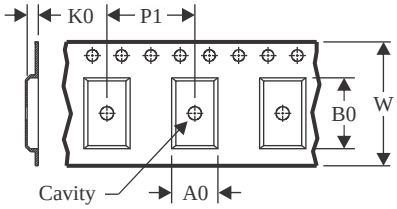
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

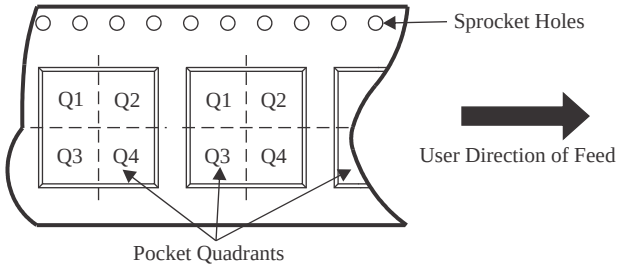


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

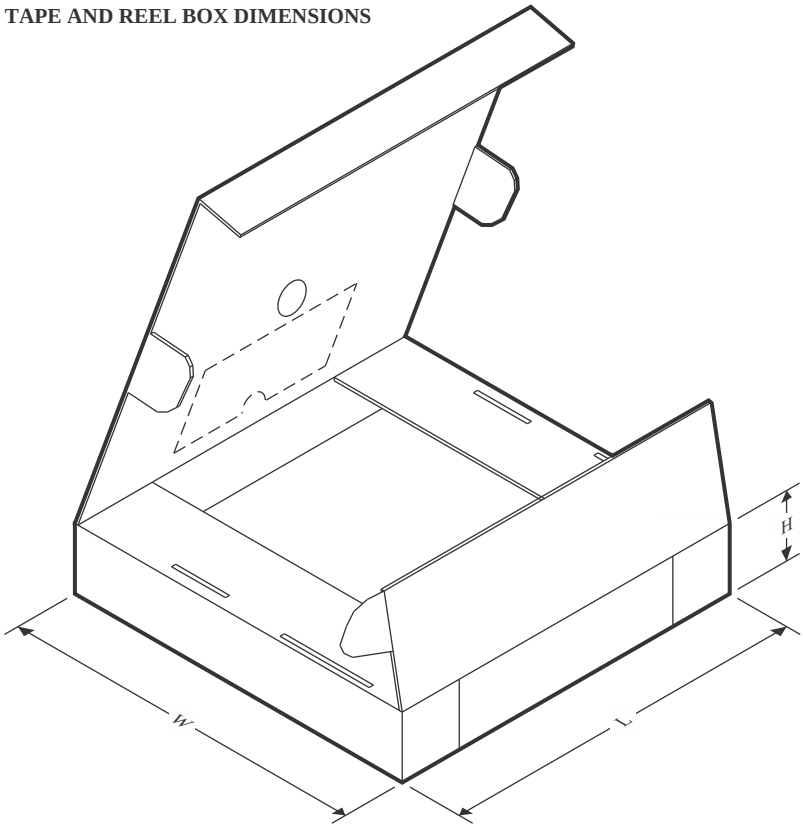
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC08100CIMTCX/NOPB	TSSOP	PW	24	2500	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

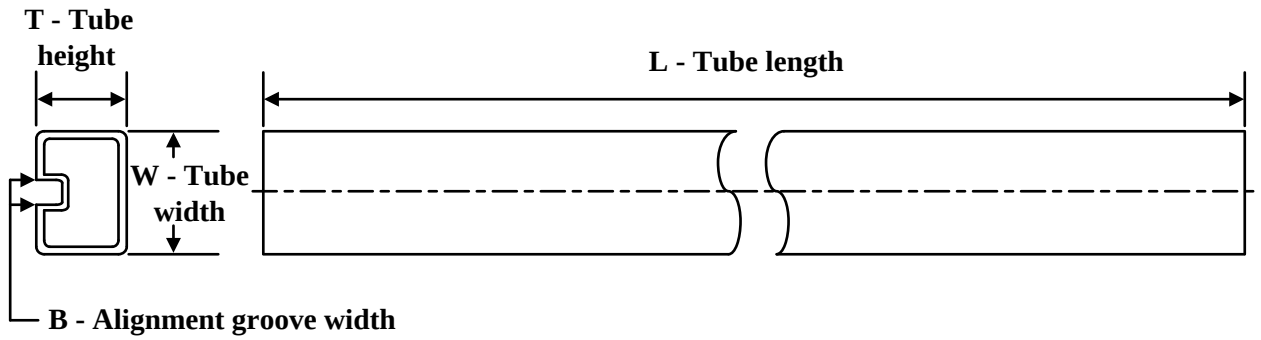
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC08100CIMTCX/NOPB	TSSOP	PW	24	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

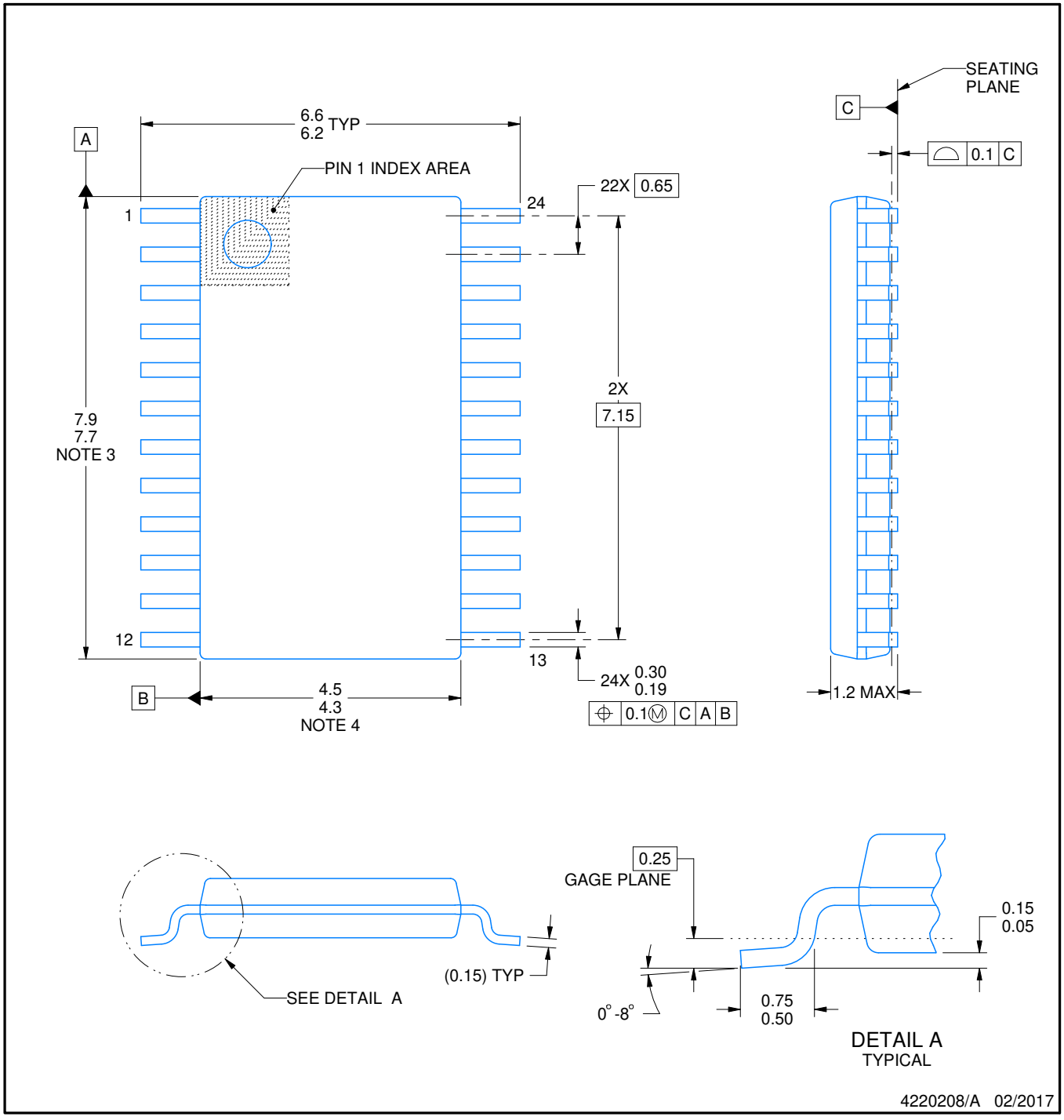
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ADC08100CIMTC/NOPB	PW	TSSOP	24	61	495	8	2514.6	4.06
ADC08100CIMTC/NOPB.A	PW	TSSOP	24	61	495	8	2514.6	4.06

PACKAGE OUTLINE

PW0024A

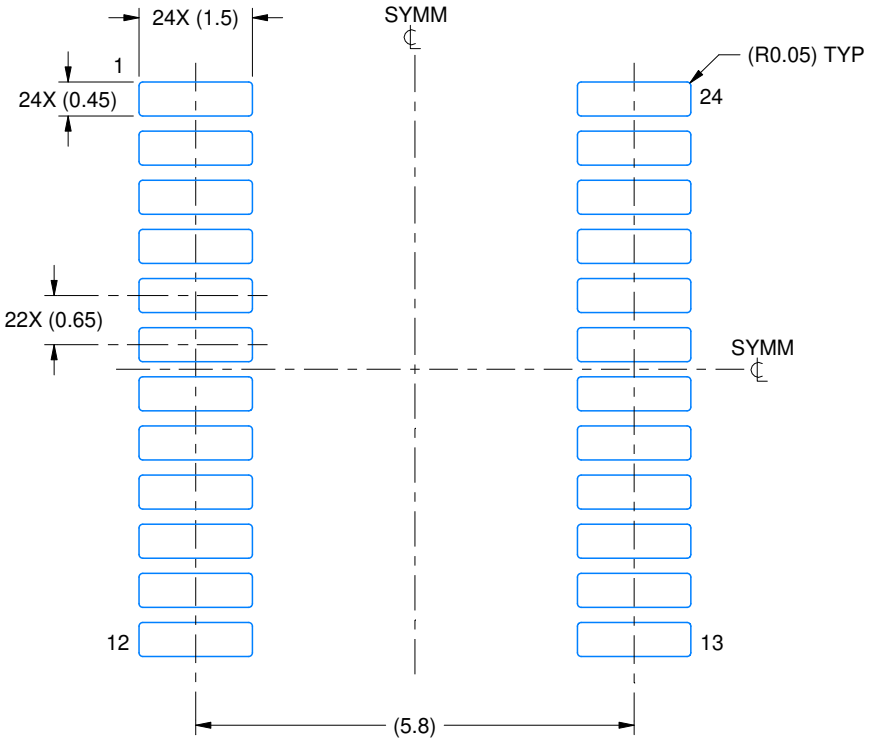
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

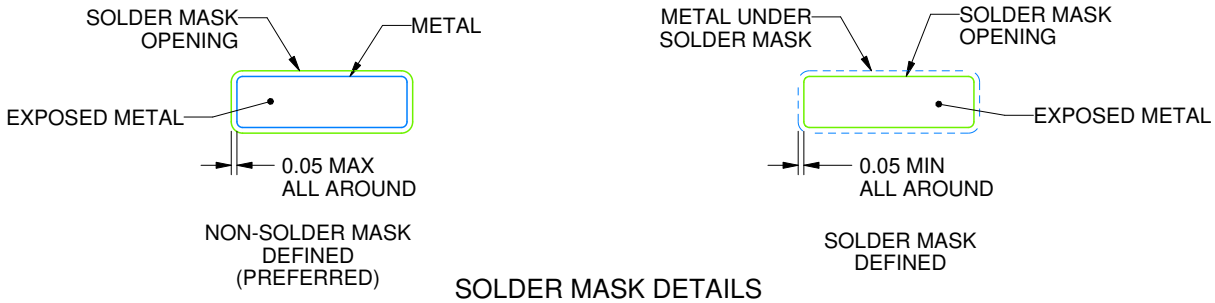


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

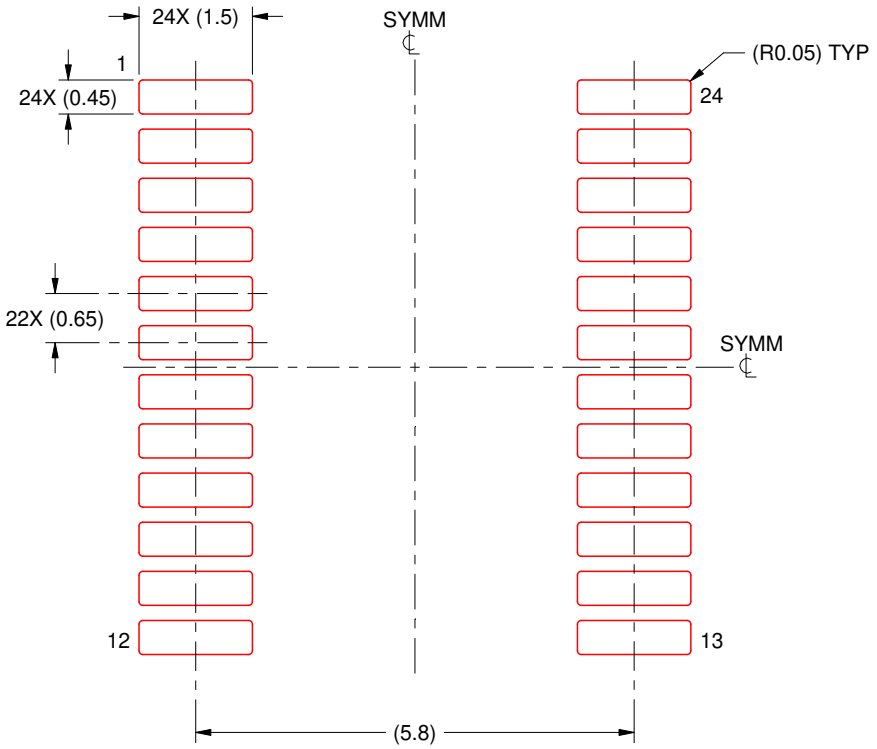


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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