ADC08DL500 Low Power, 8-Bit, Dual 500 MSPS A/D Converter

Check for Samples: ADC08DL500

FEATURES

- **Single +1.9V ±0.1V Operation**
- **Duty Cycle Corrected Sample Clock**

APPLICATIONS

- **Satellite Modems**
- **Digital Oscilloscopes**
- **Direct RF Down Conversion**
- **Communications Systems**
- **Test Instrumentation**

DESCRIPTION

The ADC08DL500 is a dual, low power, high performance, CMOS analog-to-digital converter. The ADC08DL500 digitizes signals to 8 bits of resolution at sample rates up to 500 MSPS. Consuming a typical 1.2 Watts in demultiplex mode at 500 MSPS from a single 1.9 Volt supply, this device is guaranteed to have no missing codes over the full operating temperature range. The unique folding and interpolating architecture, the fully differential comparator design, the innovative design of the internal sample-and-hold amplifier and the calibration schemes enable a very flat response of all dynamic parameters beyond Nyquist, producing a high 7.2 Effective Number of Bits (ENOB) with a 125 MHz input signal and a 500 MHz sample rate while providing a 10^{-18} Code Error Rate (C.E.R.)

The converter typically consumes 3.3 mW in the Power Down Mode and is available in a lead-free 144-lead LQFP and operates over the modified Industrial (-40°C ≤ T_A ≤ +70°C) temperature range.

Table 1. Key Specifications

		VALUE	UNIT
Resolution		8	Bits
Max Conversion Rate		500	MSPS
Code Error Rate		10^{-18}	(typ)
ENOB @ 125 MHz Input		7.2	Bits (typ)
DNL		±0.15	LSB (typ)
Power Consumption	Operating in 1:2 Demux Output	1.25	W (typ)
	Power Down Mode	3.3	mW (typ)

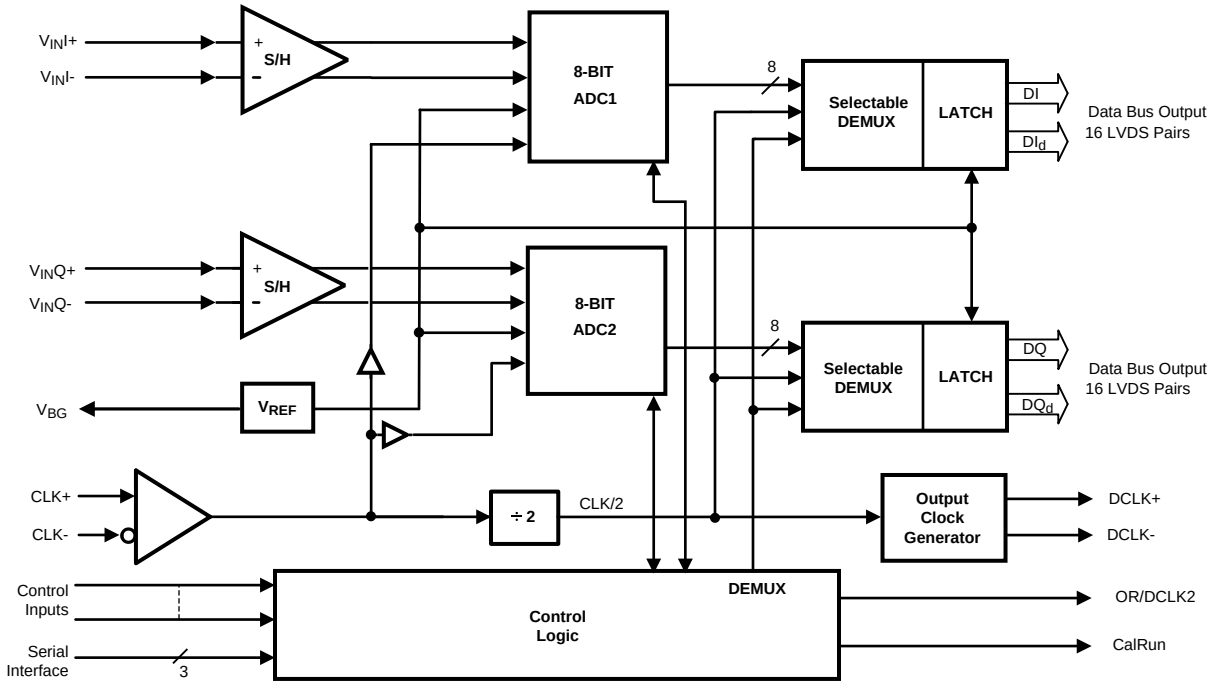
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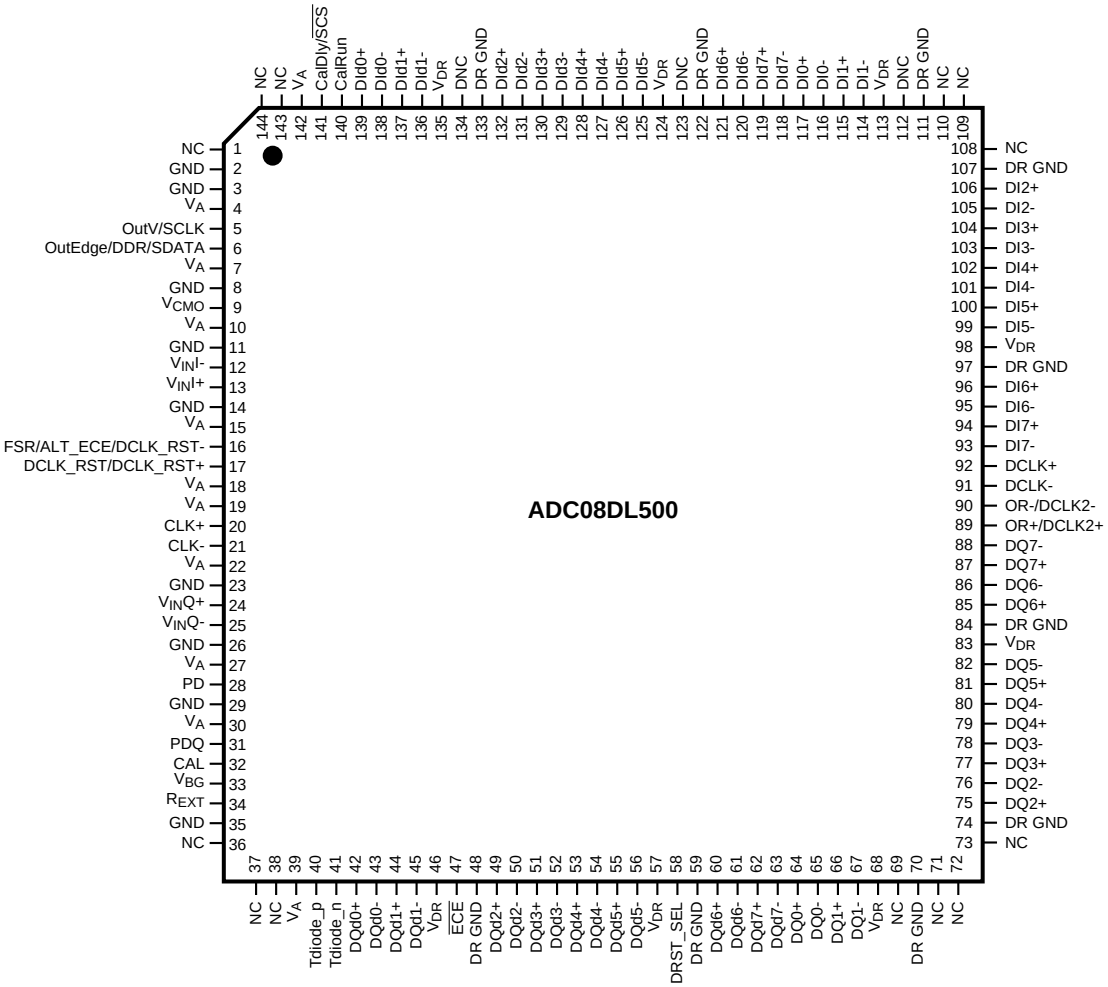
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Block Diagram

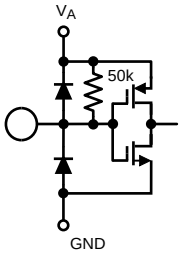


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Pin Configuration

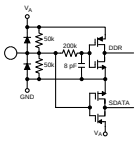
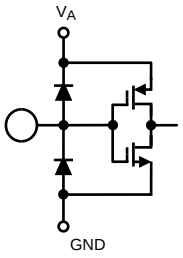
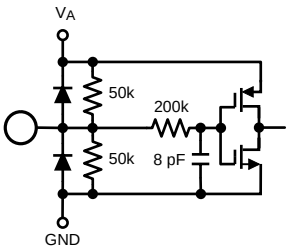


Pin Descriptions and Equivalent Circuits

Pin Functions			
Pin No.	**Symbol**	**Equivalent Circuit**	**Description**
5	OutV / SCLK		Output Voltage Amplitude and Serial Interface Clock. Tie this pin high for normal differential DCLK and data amplitude. Ground this pin for a reduced differential output amplitude and reduced power consumption. When the extended control mode is enabled, this pin functions as the SCLK input which clocks in the serial data. OutV functionality: (1)
31	PDQ		A logic high on the PDQ pin puts only the "Q" ADC into the Power Down mode. PDQ functionality: (1)

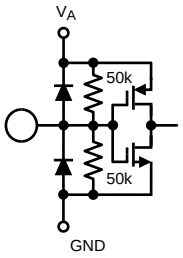
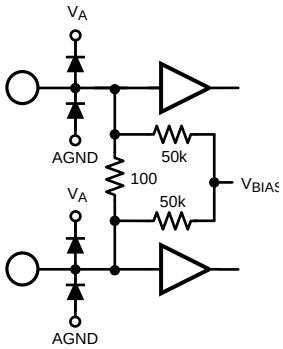
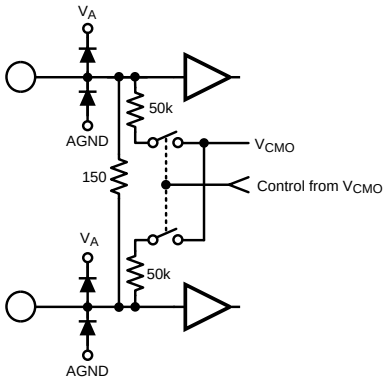
(1) This pin/bit functionality is not tested in production test; performance is tested in the specified/default mode only.

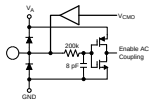
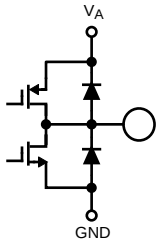
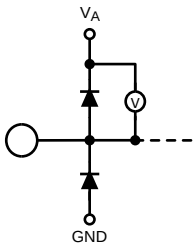
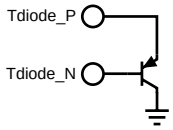
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Pin Functions			
Pin No.	**Symbol**	**Equivalent Circuit**	**Description**
6	OutEdge / DDR / SDATA		DCLK Edge Select, Double Data Rate Enable and Serial Data Input. This input sets the output edge of DCLK+ at which the output data transitions. When this pin is floating or connected to 1/2 the supply voltage, DDR clocking is enabled. When the extended control mode is enabled, this pin functions as the SDATA input. OutEdge functionality: (2)
17	DCLK_RST / DCLK_RST+		DCLK Reset. When single-ended DCLK_RST is selected by floating or setting pin 58 logic high, a positive pulse on this pin is used to reset and synchronize the DCLK outputs of multiple converters. When differential DCLK_RST is selected by setting pin 58 logic low, this pin receives the positive polarity of a differential pulse signal used to reset and synchronize the DCLK outputs of multiple converters. DCLK_RST, DCLK_RST+ functionality: (3)
28	PD		Power Down Pins. A logic high on the PD pin puts the entire device into the Power Down Mode. PD functionality: (3)
32	CAL		Calibration Cycle Initiate. A minimum t_{CAL_L} input clock cycles logic low followed by a minimum of t_{CAL_H} input clock cycles high on this pin initiates the calibration sequence.
16	FSR/ALT_ECE/DCLK_RST-		Full Scale Range Select, Alternate Extended Control Enable and DCLK_RST-. This pin has three functions. It can conditionally control the ADC full-scale voltage, enable the extended control mode, or become the negative polarity signal of a differential pair in differential DCLK_RST mode. If pin 58 and pin 47 are floating or at logic high, this pin can be used to set the full-scale-range or can be used as an alternate extended control enable pin . When used as the FSR pin, a logic low on this pin sets the full-scale differential input range to a reduced V_{IN} input level. A logic high on this pin sets the full-scale differential input range to a higher V_{IN} input level. To enable the extended control mode, whereby the serial interface and control registers are employed, allow this pin to float or connect it to a voltage equal to $V_A/2$. Note that pin 47 overrides the extended control enable of this pin. When pin 58 is held at logic low, this pin acts as the DCLK_RST- pin. When in differential DCLK_RST mode, there is no pin-controlled FSR and the full-scale-range is defaulted to the higher V_{IN} input level. FSR, ALT_ECE, DCLK_RST- functionality: (3)

(2) This pin/bit functionality is not tested in production test; performance is tested in the specified/default mode only.
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Pin Functions			
Pin No.	**Symbol**	**Equivalent Circuit**	**Description**
141	CalDly / $\overline{SCS}$		Calibration Delay and Serial Interface Chip Select. With a logic high or low on pin 16, and a logic high on pin 47, this pin functions as Calibration Delay and sets the number of input clock cycles after power up before calibration begins With pin 16 floating, and a logic low on pin 47, this pin acts as the enable pin for the serial interface input and the CalDly value becomes "0" (short delay with no provision for a long power-up calibration delay). CalDly functionality: (3)
20 21	CLK+ CLK−		LVDS Clock input pins for the ADC. The differential clock signal must be a.c. coupled to these pins. The input signal is sampled on the falling edge of CLK+.
13 12 24 25	$V_{IN}I+$ $V_{IN}I-$ $V_{IN}Q+$ $V_{IN}Q-$		Analog signal inputs to the ADC. The differential full-scale input range of this input is programmable using the FSR pin 16 in normal mode and the Input Full-Scale Voltage Adjust register in the extended control mode. Refer to the V_{IN} specification in the Converter Electrical Characteristics for the full-scale input range in the normal mode.

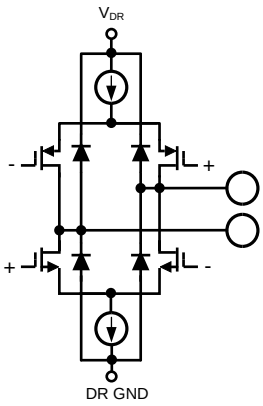
Pin Functions			
Pin No.	**Symbol**	**Equivalent Circuit**	**Description**
9	V_{CMO}		Common Mode Voltage. This pin is the common mode output in d.c. coupling mode and also serves as the a.c. coupling mode select pin. When d.c. coupling is used, the voltage output at this pin is required to be the common mode input voltage at V_{IN}+ and V_{IN}− when d.c. coupling is used. This pin should be grounded when a.c. coupling is used at the analog inputs. This pin is capable of sourcing or sinking 100 µA.
33	V_{BG}		Bandgap output voltage capable of 100 µA source/sink and can drive a load up to 80 pF. V_{BG} functionality: (4)
140	CalRun		Calibration Running indication. This pin is at a logic high when calibration is running. CalRun functionality: (4)
34	R_{EXT}		External bias resistor connection. Nominal value is 4.7 kΩ (±0.1%) to ground.
40 41	Tdiode_P Tdiode_N		Temperature Diode Positive (Anode) and Negative (Cathode). These pins may be used for die temperature measurements, however no specified accuracy is implied or guaranteed. Noise coupling from adjacent output data signals has been shown to affect temperature measurements using this feature. Tdiode_P, Tdiode_N functionality: (5)

(4) This pin/bit functionality is not tested in production test; performance is tested in the specified/default mode only.
(5) This pin/bit functionality is not tested in production test; performance is tested in the specified/default mode only.

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Pin Functions			
Pin No.	**Symbol**	**Equivalent Circuit**	**Description**
47	$\overline{\text{ECE}}$		Extended Control Enable. This pin always enables and disables Extended Control Enable. When this pin is set logic high, the extended control mode is inactive and all control of the device must be through control pins only . When it is set logic low, the extended control mode is active. This pin overrides the Extended Control Enable signal set using pin 16.
58	DRST_SEL		DCLK_RST select. This pin selects whether the DCLK is reset using a single-ended or differential signal. When this pin is floating or logic high, the DCLK_RST operation is single-ended and pin 16 functions as FSR/ALT_ECE. When this pin is logic low, the DCLK_RST operation becomes differential with functionality on pin 17 (DCLK_RST+) and pin 16 (DCLK_RST-). When in differential DCLK_RST mode, there is no pin-controlled FSR and the full-scale-range is defaulted to the higher V_{IN} input level. When pin 47 is set logic low, the extended control mode is active and the Full-Scale Voltage Adjust registers can be programmed. DRST_SEL functionality: (5)

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Pin Functions			
Pin No.	**Symbol**	**Equivalent Circuit**	**Description**
93 / 88 94 / 87 95 / 86 96 / 85 99 / 82 100 / 81 101 / 80 102 / 79 103 / 78 104 / 77 105 / 76 106 / 75 114 / 67 115 / 66 116 / 65 117 / 64	DI7− / DQ7− DI7+ / DQ7+ DI6− / DQ6− DI6+ / DQ6+ DI5− / DQ5− DI5+ / DQ5+ DI4− / DQ4− DI4+ / DQ4+ DI3− / DQ3− DI3+ / DQ3+ DI2− / DQ2− DI2+ / DQ2+ DI1− / DQ1− DI1+ / DQ1+ DI0− / DQ0− DI0+ / DQ0+		I and Q channel LVDS Data Outputs that are not delayed in the output demultiplexer. Compared with the DId and DQd outputs, these outputs represent the later time samples. These outputs should always be terminated with a 100 Ω differential resistor.
118 / 63 119 / 62 120 / 61 121 / 60 125 / 56 126 / 55 127 / 54 128 / 53 129 / 52 130 / 51 131 / 50 132 / 49 136 / 45 137 / 44 138 / 43 139 / 42	DId7− / DQd7− DId7+ / DQd7+ DId6− / DQd6− DId6+ / DQd6+ DId5− / DQd5− DId5+ / DQd5+ DId4− / DQd4− DId4+ / DQd4+ DId3− / DQd3− DId3+ / DQd3+ DId2− / DQd2− DId2+ / DQd2+ DId1− / DQd1− DId1+ / DQd1+ DId0− / DQd0− DId0+ / DQd0+		I and Q channel LVDS Data Outputs that are delayed by one CLK cycle in the output demultiplexer. Compared with the DI/DQ outputs, these outputs represent the earlier time sample. These outputs should be terminated with a 100 Ω differential resistor when enabled. In non-demultiplexed mode, these outputs are disabled and are high impedance when enabled. When disabled, these outputs must be left floating.
89 90	OR+/DCLK2+ OR-/DCLK2-		Out Of Range output. A differential high at these pins indicates that the differential input is out of range (outside the range $\pm V_{IN}/2$ as programmed by the FSR pin in non-extended control mode or the Input Full-Scale Voltage Adjust register setting in the extended control mode). DCLK2 is the exact mirror of DCLK and should output the same signal at the same rate. DCLK2+/- functionality: (6)
92 91	DCLK+ DCLK-		Data Clock. Differential Clock outputs used to latch the output data. Delayed and non-delayed data outputs are supplied synchronous to this signal. In 1:2 demultiplexed mode, this signal is at 1/2 the input clock rate in SDR mode and at 1/4 the input clock rate in the DDR mode. By default, the DCLK outputs are not active during the termination resistor trim section of the calibration cycle. If a system requires DCLK to run continuously during a calibration cycle, the termination resistor trim portion of the cycle can be disabled by setting the Resistor Trim Disable (RTD) bit to logic high in the Extended Configuration Register (address 9h). This disables all subsequent termination resistor trims after the initial trim which occurs during the power on calibration. Therefore, this output is not recommended as a system clock unless the resistor trim is disabled. When the device is in the non-demultiplexed mode, DCLK can only be in DDR mode and the signal is at 1/2 the input clock rate.
4, 7, 10, 15, 18, 19, 22, 27, 30, 39, 142	V_A	NONE	Analog power supply pins. Bypass these pins to ground.
46, 57, 68, 83, 98, 113, 124, 135	V_{DR}	NONE	Output Driver power supply pins. Bypass these pins to DR GND.

(6) This pin/bit functionality is not tested in production test; performance is tested in the specified/default mode only.

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Pin Functions			
Pin No.	**Symbol**	**Equivalent Circuit**	**Description**
2, 3, 8, 11, 14, 23, 26, 29, 35	GND	NONE	Ground return for V_A.
48, 59, 70, 74, 84, 97, 107, 111, 122, 133	DR GND	NONE	Ground return for V_{DR}.
1, 36, 37, 38, 69, 71, 72, 73, 108, 109, 110, 143, 144	NC	NONE	Not Connected. These pins are not bonded and may be left floating or connected to any potential.
112, 123, 134	DNC	NONE	Do Not Connect. These pins are used for internal purposes and should not be connected, i.e. left floating. Do not ground.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2)

Supply Voltage (V_A, V_{DR})	2.2V
Supply Difference V_{DR} - V_A	0V to 100 mV
Voltage on Any Input Pin (Except V_{IN}+, V_{IN}-)	−0.15V to (V_A +0.15V)
Voltage on V_{IN}+, V_{IN}- (Maintaining Common Mode)	-0.15 to 2.5V
Ground Difference |GND - DR GND|	0V to 100 mV
Input Current at Any Pin (3)	±25 mA
Package Input Current (3)	±50 mA
Junction Temperature	$T_J \le 145°C$
ESD Susceptibility (4) Human Body Model Machine Model Charged Device Model	 2500V 250V 1000V
Storage Temperature	−65°C to +150°C

(1) All voltages are measured with respect to GND = DR GND = 0V, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. There is no guarantee of operation at the Absolute Maximum Ratings. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) When the input voltage at any pin exceeds the power supply limits (that is, less than GND or greater than V_A), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two. This limit is not placed upon the power, ground and digital output pins.
(4) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through ZERO Ohms. Charged device model simulates a pin slowly acquiring charge (such as from a device sliding down the feeder in an automated assembler) then rapidly being discharged.

Operating Ratings (1) (2)

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. There is no guarantee of operation at the Absolute Maximum Ratings. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = DR GND = 0V, unless otherwise specified.

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Operating Ratings (1) (2) (continued)

Ambient Temperature Range (3)	−40°C ≤ T_A ≤ +70°C
Supply Voltage (V_A)	+1.8V to +2.0V
Driver Supply Voltage (V_{DR})	+1.8V to V_A
Common Mode Input Voltage	V_{CMO} ± 50 mV
V_{IN}+, V_{IN}− Voltage Range (Maintaining Common Mode)	0V to 2.15V (100% duty cycle) 0V to 2.5V (10% duty cycle)
Ground Difference (|GND − DR GND|)	0V
CLK Pins Voltage Range	0V to V_A
Differential CLK Amplitude	0.4V_{P-P} to 2.0V_{P-P}
Common Mode Input Voltage	V_{CMO} - 50mV < V_{CMI} < V_{CMO} + 50mV

(3) The 4-layer standard JEDEC thermal test board or 4LJEDEC is 4"x3" in size. The board has two embedded copper layers which cover roughly the same size as the board. The copper thickness for the four layers, starting from the top one, is 2 oz., 1 oz., 1 oz., 2 oz. Detailed description of the board can be found in the JESD 51-7 standard.

Package Thermal Resistance (1) (2)

Package	θ_{JA}	θ_{JC}	psi_{JB}
144-Lead, LQFP	43.6°C / W	12.5°C / W	39.0°C / W

(1) *Soldering process must comply with National Semiconductor's Reflow Temperature Profile specifications. Refer to* www.national.com/packaging.

(2) Reflow temperature profiles are different for lead-free and non-lead-free packages.

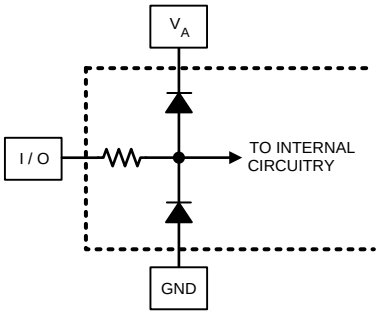
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Converter Electrical Characteristics Static Converter Characteristics

The following specifications apply after calibration for $V_A = V_{DR} = 1.9V$; OutV = 1.9V; V_{IN} FSR (a.c. coupled) = differential 840 mV_{P-P}; C_L = 10 pF; Differential, a.c. coupled Sine Wave Input Clock, f_{CLK} = 500 MHz at 0.5 V_{P-P} with 50% duty cycle; V_{BG} = Floating; Extended Control Mode default values; DDR 0° Mode; R_{EXT} = 4700 Ω ±0.1%; 1:2 Output Demultiplex; Duty Cycle Stabilizer on. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}.** All other limits T_A = 25°C, unless otherwise noted. (1) (2).

Symbol	Parameter	Conditions	Typ(3)	Lim	Units (Limits)
	Resolution with No Missing Codes			**8**	Bits
INL	Integral Non-Linearity (Best fit)	DC Coupled, 1 MHz Sine Wave Overanged, SDR, Non-ECM, FSR = High	±0.3	**±0.9**	LSB (max)
DNL	Differential Non-Linearity	DC Coupled, 1 MHz Sine Wave Overanged, SDR, Non-ECM, FSR = High	±0.15	**±0.75**	LSB (max)
V_{OFF}	Offset Error	SDR, Non-ECM Mode	−0.45		LSB
V_{OFF}_ADJ	Input Offset Adjustment Range (4)	Extended Control Mode	±45		mV
PFSE	Positive Full-Scale Error	(5)		**±25**	mV (max)
NFSE	Negative Full-Scale Error	(5)		**±25**	mV (max)
	Out of Range Output Code	$(V_{IN}+) - (V_{IN}-) >$ + Full Scale		**255**	
		$(V_{IN}+) - (V_{IN}-) <$ − Full Scale		**0**	

(1) The analog inputs are protected as shown below. Input voltage magnitudes beyond the Absolute Maximum Ratings may damage this device.



(2) To guarantee accuracy, it is required that V_A and V_{DR} be well bypassed. Each supply pin must be decoupled with separate bypass capacitors. Additionally, achieving rated performance requires that the backside exposed pad be well grounded.
(3) Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
(4) Only the end points of the range, not the full sweep, are tested in production test.
(5) Calculation of Full-Scale Error for this device assumes that the actual reference voltage is exactly its nominal value. Full-Scale Error for this device, therefore, is a combination of Full-Scale Error and Reference Voltage Error. For relationship between Gain Error and Full-Scale Error, see Specification Definitions for Gain Error.

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Converter Electrical Characteristics Dynamic Converter Characteristics

Symbol	Parameter	Conditions	Typ(1)	Lim	Units (Limits)
FPBW	Full Power Bandwidth		2.0		GHz
	Gain Flatness	d.c. to 248 MHz	±0.8		dBFS
		d.c. to 500 MHz	±1.0		dBFS
C.E.R.	Code Error Rate		10^{-18}		Error/Sample
NPR	Noise Power Ratio	(2)	38.4		dB
IMD3	3rd order Intermodulation Distortion	f_{IN1} =111.47 MHz @ −7dBFS f_{IN2} =121.47 MHz @ −7dBFS	71.4		dBFS
			64.4		dBc
	Noise Floor	(3)	-135.4		dBm/Hz
			-133.3		dBFS/Hz
ENOB	Effective Number of Bits	A_{IN} = 125 MHz @ -0.5dBFS	7.2	**6.8**	bits
		A_{IN} = 248 MHz @ -0.5dBFS	7.2		bits (min)
SINAD	Signal-to-Noise Plus Distortion Ratio	A_{IN} = 125 MHz @ -0.5dBFS	45.1	**42.4**	dB
		A_{IN} = 248 MHz @ -0.5dBFS	45.1		dB (min)
SNR	Signal-to-Noise Ratio	A_{IN} = 125 MHz @ -0.5dBFS	46	**43.5**	dB
		A_{IN} = 248 MHz @ -0.5dBFS	46		dB (min)
THD	Total Harmonic Distortion	A_{IN} = 125 MHz @ -0.5dBFS	−52	**-49**	dB
		A_{IN} = 248 MHz @ -0.5dBFS	-52		dB (max)
2nd Harm	Second Harmonic Distortion	A_{IN} = 125 MHz @ -0.5dBFS	−63		dB
		A_{IN} = 248 MHz @ -0.5dBFS	-63		dB
3rd Harm	Third Harmonic Distortion	A_{IN} = 125 MHz @ -0.5dBFS	−65		dB
		A_{IN} = 248 MHz @ -0.5dBFS	-65		dB
SFDR	Spurious-Free dynamic Range	A_{IN} = 125 MHz @ -0.5dBFS	55	**49**	dB
		A_{IN} = 248 MHz @ -0.5dBFS	55		dB (min)

(1) Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

(2) The NPR was measured using an Agilent N6030A Arbitrary Waveform Generator (ARB) to generate the input signal. The "noise" portion of the signal was created by tones spaced at 500 kHz and the "notch" was a 12.5 MHz absence of tones centered at 175 MHz.

(3) For the case where the inputs are shorted or terminted with 50Ω, the LSB of the ADC never transitions because the Noise Floor is limited by quantization noise, not thermal noise. Therefore, the Noise Floor was measured with a low-level wideband input from 10 MHz to 30 MHz; the noise floor was measured in the band from 126 MHz to 175 MHz.

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Converter Electrical Characteristics Analog Input/Output and Reference Characteristics

Symbol	Parameter	Conditions	Typ(1)	Lim	Units (Limits)
Analog Inputs					
V_{IN_FSR}	Analog Differential Input Full Scale Range	**Non-Extended Control Mode**(2)			
		FSR Pin High, SDR	840	**900**	mV_{P-P}
		FSR Pin Low, SDR	650		mV_{P-P}
		Extended Control Mode(3)			
		FS_ADJ(15:7) = 1111 1111 1**b**	840		mV_{P-P}
		FS_ADJ(15:7) = 1000 0000 0**b** (default)	700		mV_{P-P}
		FS_ADJ(15:7) = 0000 0000 0**b**	560		mV_{P-P}
C_{IN}	Analog Input Capacitance(4)(5) (6)	Differential	0.02		pF
		Each input pin to ground	1.6		pF
R_{IN}	Differential Input Resistance	Measured at D.C.	140		Ω
Common Mode Output					
V_{CMO}	Common Mode Output Voltage	I_{CMO} = ±100 µA	1.26	**0.9**	V (min)
				1.6	V (max)
Bandgap Reference					
V_{BG}	Bandgap Reference Output Voltage	I_{BG} = ±100 µA	1.26		V
TC_V_{BG}	Bandgap Reference Voltage Temperature Coefficient	T_A = −40°C to +70°C, 182456 I_{BG} = ±100 µA	28		ppm/°C
C_{LOAD} V_{BG}	Maximum Bandgap Reference load Capacitance			80	pF

(1) Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
(2) This pin/bit functionality is not tested in production test; performance is tested in the specified/default mode only.
(3) Only the end points of the range, not the full sweep, are tested in production test.
(4) The analog and clock input capacitances are die capacitances only. Additional package capacitances of 0.65 pF differential and 0.95 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.
(5) This parameter is guaranteed by design and is not tested in production.
(6) The differential and pin-to-ground input capacitances are lumped capacitance values from design; they are defined as shown below.

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Converter Electrical Characteristics I-Channel to Q-Channel Characteristics

Symbol	Parameter	Conditions	Typ(1)	Lim	Units (Limits)
	Offset Match		1		LSB
	Positive Full-Scale Match	Zero offset selected in Control Register	1		LSB
	Negative Full-Scale Match	Zero offset selected in Control Register	1		LSB
	Phase Matching (I, Q)	f_{IN} = 500 MHz	< 1		Degree
X-TALK	Crosstalk from I (Aggressor) to Q (Victim) Channel	Aggressor = 467 MHz F.S. Victim = 100 MHz F.S.	−65		dB
	Crosstalk from Q (Aggressor) to I (Victim) Channel	Aggressor = 467 MHz F.S. Victim = 100 MHz F.S.	−65		dB

(1) Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

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Converter Electrical Characteristics Sampling Clock Characteristics

Symbol	Parameter	Conditions	Typ(1)	Lim	Units (Limits)
V_{IN_CLK}	Differential Clock Input Level	Sine Wave Clock	0.6	**0.4**	V_{P-P} (min)
				2.0	V_{P-P} (max)
		Square Wave Clock	0.6	**0.4**	V_{P-P} (min)
				2.0	V_{P-P} (max)
R_{IN_CLK}	Sampling Clock Input Impedance	Measured at D.C.	100		Ω
C_{IN_CLK}	Input Capacitance (2) (3)	Differential	0.02		pF
		Each input to ground	1.5		pF
V_{OSI}	Input Offset Voltage		1.2		V

(1) Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
(2) The analog and clock input capacitances are die capacitances only. Additional package capacitances of 0.65 pF differential and 0.95 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.
(3) This parameter is guaranteed by design and is not tested in production.

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Converter Electrical Characteristics Digital Control and Output Pin Characteristics

Symbol	Parameter	Conditions	Typ(1)	Lim	Units (Limits)
Digital Control Pins					
V_{IH}	Logic High Input Voltage (2)	PD,CAL, OutV, PDQ, ECEb, DRST_SEL		**0.69 x V_A**	V (min)
		OUTEDGE, FSR, CalDly		**0.815 x V_A**	V (min)
V_{IL}	Logic Low Input Voltage (2)	PD,CAL, OutV, PDQ, ECEb, DRST_SEL		**0.28 x V_A**	V (max)
		OUTEDGE, FSR, CalDly		**0.21 x V_A**	V (max)
C_{IN_DIG}	Input Capacitance (3) (4)	Each input to ground	1.2		pF
Digital Output Pins					
V_{OD}	LVDS Differential Output Voltage	Measured differentially, OutV = V_A, V_{BG} = Floating (5) (6)	590	**400**	mV_{P-P} (min)
				850	mV_{P-P} (max)
		Measured differentially, OutV = GND, V_{BG} = Floating (5) (6)	432		mV_{P-P}
$\Delta V_{O\ DIFF}$	Change in LVDS Output Swing Between Logic Levels		±1		mV
V_{OS}	Output Offset Voltage	V_{BG} = Floating	0.8		V
		V_{BG} = V_A (5) (6)	1.2		V
ΔV_{OS}	Output Offset Voltage Change Between Logic Levels		±1		mV
I_{OS}	Output Short Circuit Current	Output+ & Output− connected to 0.8V	±4		mA
Z_O	Differential Output Impedance		100		Ω
V_{OH}	CalRun H level output	I_{OH} = −400 µA (2)	1.65		V
V_{OL}	CalRun L level output	I_{OH} = 400 µA (2)	0.15		V
Differential DCLK Reset Pins (DCLK_RST) (7)					
V_{CMI_DRST}	DCLK_RST Common Mode Input Voltage		1.25		V
V_{ID_DRST}	Differential DCLK_RST Input Voltage		V_{IN_CLK}		V_{P-P}
R_{IN_DRST}	Differential DCLK_RST Input Resistance		100		Ω

(1) Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
(2) This parameter is guaranteed by design and/or characterization and is not tested in production.
(3) This parameter is guaranteed by design and is not tested in production.
(4) The digital control pin capacitances are die capacitances only. Additional package capacitance of 1.6 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.
(5) Tying V_{BG} to the supply rail will increase the output offset voltage (V_{OS}) by 400 mV (typical), as shown in the V_{OS} specification above. Tying V_{BG} to the supply rail will also affect the differential LVDS output voltage (V_{OD}), causing it to increase by 40 mV (typical).
(6) This pin/bit functionality is not tested in production test; performance is tested in the specified/default mode only.
(7) This feature functionality is not tested in production test; performance is tested in the specified/default mode only.

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Converter Electrical Characteristics Power Supply Characteristics

Symbol	Parameter	Conditions	Typ(1)	Lim	Units (Limits)
I_A	Analog Supply Current	**1:2 Demux Output**			
		PD = Low	494	**650**	mA (max)
		PD = High	1.7		mA
I_{DR}	Output Driver Supply Current	**1:2 Demux Output**			
		PD = Low	168	**275**	mA (max)
		PD = High	0.054		mA
P_C	Power Consumption	**1:2 Demux Output**			
		PD = Low	1.25	**1.61**	W (max)
		PD = High	3.3		mW

(1) Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

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Converter Electrical Characteristics AC Electrical Characteristics

Symbol	Parameter	Conditions	Typ(1)	Lim	Units (Limits)
Sampling Clock (CLK)					
$f_{CLK\ (max)}$	Maximum Sampling Clock Frequency			**500**	MHz
$f_{CLK\ (min)}$	Minimum Sampling Clock Frequency			**200**	MHz
	Sampling Clock Duty Cycle	200 MHz ≤ f_{CLK} ≤ 500 MHz (2)	50	20	% (min)
				80	% (max)
t_{CL}	Sampling Clock Low Time	(3)	1000	**400**	ps (min)
t_{CH}	Sampling Clock High Time	(3)	1000	**400**	ps (min)
DCLK_RST (4)					
t_{SR}	Setup Time DCLK_RST±	(2) Differential DCLK_RST	90		ps
t_{HR}	Hold Time DCLK_RST±	(2) Differential DCLK_RST	30		ps
t_{PWR}	Pulse Width DCLK_RST±	(3)		**4**	CLK± Cycles (min)
Data Clock (DCLK)					
	DCLK Duty Cycle	(3)	50	**45**	% (min)
				55	% (max)
t_{LHT}	Differential Low-to-High Transition Time	10% to 90%	150		ps
t_{HLT}	Differential High-to-Low Transition Time	10% to 90%	150		ps
t_{OSK}	DCLK-to-Data Output Skew	50% of DCLK transition to 50% of Data transition	±50		ps
t_{SU}	Data-to-DCLK Set-Up Time	DDR Mode, 90° DCLK (3)	750		ps
t_H	DCLK-to-Data Hold Time	DDR Mode, 90° DCLK (3)	890		ps
Data Input-to-Output					
t_{AD}	Sampling (Aperture) Delay	Input CLK+ Fall to Acquisition of Data	1.6		ns
t_{AJ}	Aperture Jitter		0.4		ps (rms)
t_{OD}	Input Clock-to Data Output Delay (in addition to Pipeline Delay)	50% of Input Clock transition to 50% of Data transition	4.0		ns
t_{LAT}	Pipeline Delay (Latency) in 1:2 Demux Mode (3) (5)	DI Outputs		**13**	Sampling Clock Cycles
		DId Outputs		**14**	
		DQ Outputs		**13**	
		DQd Outputs		**14**	
	Pipeline Delay (Latency) in Non-Demux Mode (3) (5)	DI Outputs		**13**	
		DQ Outputs		**13**	
t_{ORR}	Over Range Recovery Time	Differential V_{IN} step from ±1.2V to 0V to get accurate conversion	1		Sampling Clock Cycle
t_{WU}	PD low to Rated Accuracy Conversion (Wake-Up Time)	(3)	500		ns

(1) Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
(2) This parameter is guaranteed by design and/or characterization and is not tested in production.
(3) This parameter is guaranteed by design and is not tested in production.
(4) This feature functionality is not tested in production test; performance is tested in the specified/default mode only.
(5) Each of the two converters of the ADC08DL500 has two LVDS output buses, which each clock data out at one half the sample rate. The data at each bus is clocked out at one half the sample rate. The second bus (D0 through D7) has a pipeline latency that is one Input Clock cycle less than the latency of the first bus (Dd0 through Dd7) in 1:2 demux mode.

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Converter Electrical Characteristics Serial Port Interface

Symbol	Parameter	Conditions	Typ(1)	Lim	Units (Limits)
f_{SCLK}	Serial Clock Frequency	(2)	15		MHz
	Serial Clock Low Time			**33.3**	ns (min)
	Serial Clock High Time			**33.3**	ns (min)
t_{SSU}	Serial Data to Serial Clock Rising Setup Time	(2)	2.5		ns (min)
t_{SH}	Serial Data to Serial Clock Rising Hold Time	(2)	1		ns (min)
t_{SCS}	$\overline{CS}$ to Serial Clock Rising Setup Time		2.5		ns
t_{HCS}	$\overline{CS}$ to Serial Clock Falling Hold Time		1.5		ns

(1) Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
(2) This parameter is guaranteed by design and is not tested in production.

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Converter Electrical Characteristics Calibration

Symbol	Parameter	Conditions	Typ(1)	Lim	Units (Limits)
t_{CAL}	Calibration Cycle Time	Rtrim enabled	1.4×10^6	**1.62×10^6**	Clock Cycles (max)
		Rtrim disabled	1.2×10^6	**1.35×10^6**	
t_{CAL_L}	CAL Pin Low Time	(2)		1280	Clock Cycles (min)
t_{CAL_H}	CAL Pin High Time	(2)		1280	
t_{CalDly}	Calibration Delay determined by CalDly pin (2)	CalDly = Low (3)		2^{26}	Clock Cycles (max)
		CalDly = High (3)		2^{32}	

(1) Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
(2) This parameter is guaranteed by design and is not tested in production.
(3) This pin/bit functionality is not tested in production test; performance is tested in the specified/default mode only.

Specification Definitions

APERTURE (SAMPLING) DELAY is the amount of delay, measured from the sampling edge of the Clock input, after which the signal present at the input pin is sampled inside the device.

APERTURE JITTER (t_{AJ}) is the variation in aperture delay from sample to sample. Aperture jitter shows up as input noise.

CODE ERROR RATE (C.E.R.) is the probability of error and is defined as the probable number of word errors on the ADC output per unit of time divided by the number of words seen in that amount of time. A C.E.R. of 10^{-18} corresponds to a statistical error in one word about every four (4) years.

CLOCK DUTY CYCLE is the ratio of the time that the clock waveform is at a logic high to the total time of one clock period.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB. Measured at sample rate = 500 MSPS with a 1MHz input sinewave.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as (SINAD − 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH (FPBW) is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full-scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated from Offset and Full-Scale Errors:

Positive Gain Error = Offset Error − Positive Full-Scale Error

Negative Gain Error = −(Offset Error − Negative Full-Scale Error)

Gain Error = Negative Full-Scale Error − Positive Full-Scale Error = Positive Gain Error + Negative Gain Error

INTEGRAL NON-LINEARITY (INL) is a measure of worst case deviation of the ADC transfer function from an ideal straight line drawn through the ADC transfer function. The deviation of any given code from this straight line is measured from the center of that code value step. The best fit method is used

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the second and third order intermodulation products to the power in one of the original frequencies. IMD is usually expressed in dBFS.

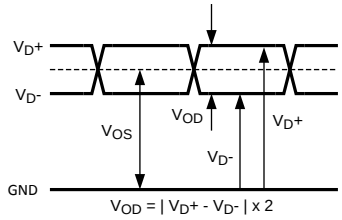
LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is

$$V_{FS} / 2^N \quad (1)$$

where V_{FS} is the differential full-scale amplitude V_{IN} as set by the FSR input and "n" is the ADC resolution in bits, and which is 8 for the ADC08DL500.

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LOW VOLTAGE DIFFERENTIAL SIGNALING (LVDS) DIFFERENTIAL VOLTAGE (V_{ID} and V_{OD}) is two times the absolute value of the difference between the V_D+ and V_D − signals; each measured with respect to Ground.



LVDS OUTPUT OFFSET VOLTAGE (V_{OS}) is the midpoint between the D+ and D− pins output voltage with respect to ground, i.e., [(V_D+) + (V_D−)] / 2.

MISSING CODES are those output codes that are skipped and will never appear at the ADC outputs. These codes cannot be reached with any input value.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL-SCALE ERROR (NFSE) is a measure of how far the first code transition is from the ideal 1/2 LSB above a differential −V_{IN}/2. For the ADC08DL500 the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

OFFSET ERROR (V_{OFF}) is a measure of how far the mid-scale point is from the ideal zero voltage differential input.

Offset Error = Actual Input causing average of 8k samples to result in an average code of 127.5.

OUTPUT DELAY (t_{OD}) is the time delay (in addition to Pipeline Delay) after the falling edge of CLK+ before the data update is present at the output pins.

OVER-RANGE RECOVERY TIME is the time required after the differential input voltages goes from ±1.2V to 0V for the converter to recover and make a conversion with its rated accuracy.

PIPELINE DELAY (LATENCY) is the number of input clock cycles between initiation of conversion and when that data is presented to the output driver stage. New data is available at every clock cycle, but the data lags the conversion by the Pipeline Delay plus the t_{OD}.

POSITIVE FULL-SCALE ERROR (PFSE) is a measure of how far the last code transition is from the ideal 1-1/2 LSB below a differential +V_{IN}/2. For the ADC08DL500 the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

POWER SUPPLY REJECTION RATIO (PSRR) can be one of two specifications. PSRR1 (DC PSRR) is the ratio of the change in full-scale error that results from a power supply voltage change from 1.8V to 2.0V. PSRR2 (AC PSRR) is a measure of how well an a.c. signal injected on the power supply is rejected from the output and is measured with a 125 MHz, 50 mV_{P-P} signal riding upon the power supply. It is the ratio of the output amplitude of that signal at the output to its amplitude on the power supply pin. PSRR is expressed in dB.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of all of the other spectral components below half the input clock frequency, including harmonics but excluding d.c.

SPURIOUS-FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal at the output and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input, excluding d.c.

TOTAL HARMONIC DISTORTION (THD) is the ratio expressed in dB, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$THD = 20 \times \log \sqrt{\frac{A_{f2}^2 + \ldots + A_{f10}^2}{A_{f1}^2}} \quad (2)$$

where A_{f1} is the RMS power of the fundamental (output) frequency and A_{f2} through A_{f10} are the RMS power of the first 9 harmonic frequencies in the output spectrum.

– Second Harmonic Distortion (2nd Harm) is the difference, expressed in dB, between the RMS power in the input frequency seen at the output and the power in its 2nd harmonic level at the output.

– Third Harmonic Distortion (3rd Harm) is the difference expressed in dB between the RMS power in the input frequency seen at the output and the power in its 3rd harmonic level at the output.

Transfer Characteristic

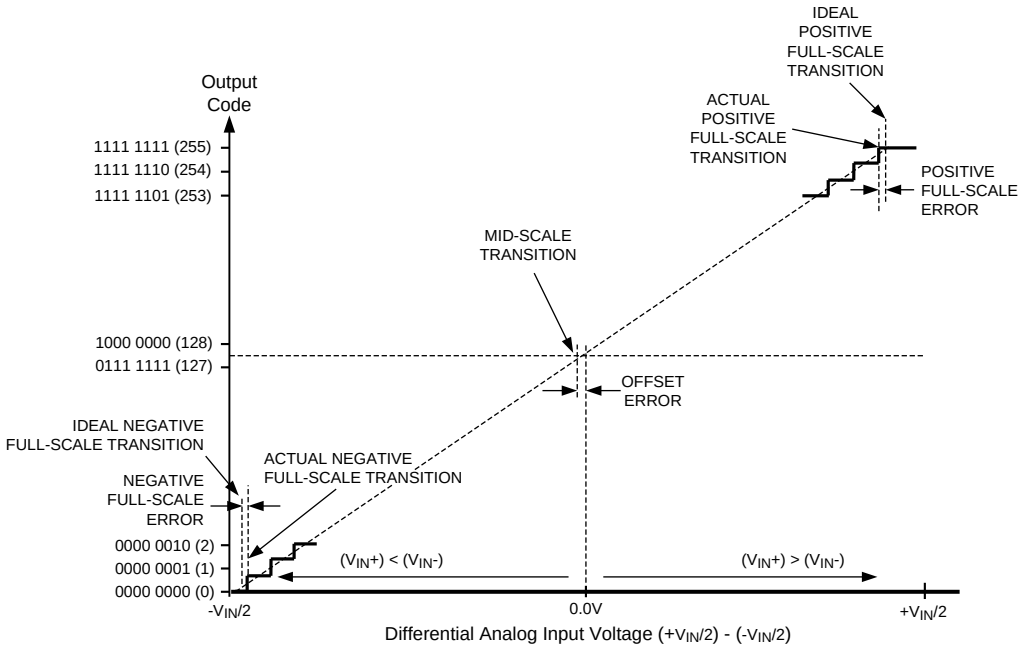


Figure 1. Input / Output Transfer Characteristic

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TEST CIRCUIT DIAGRAMS

Timing Diagrams

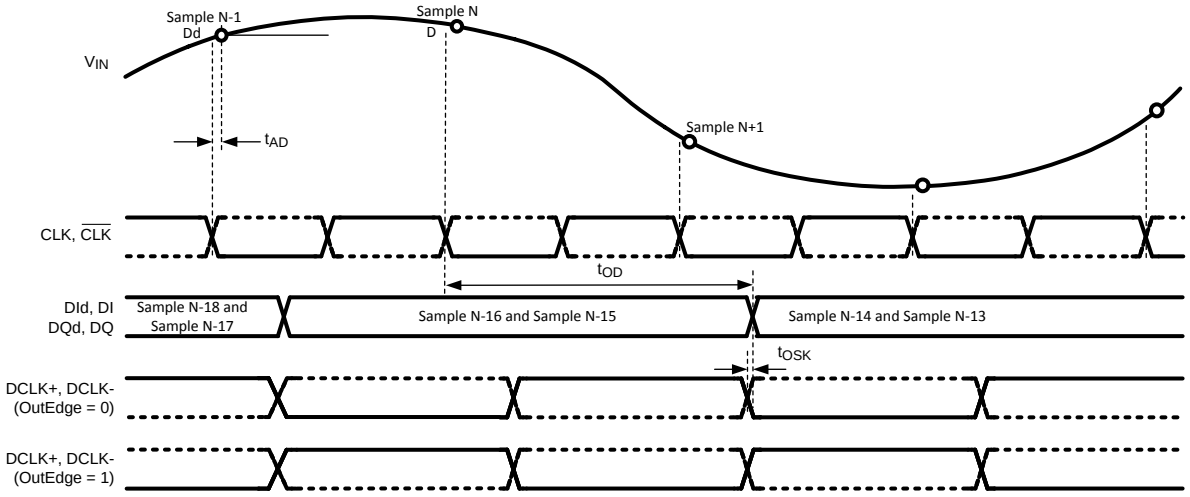


Figure 2. ADC08DL500 Timing — SDR Clocking in 1:2 Demultiplexed Mode

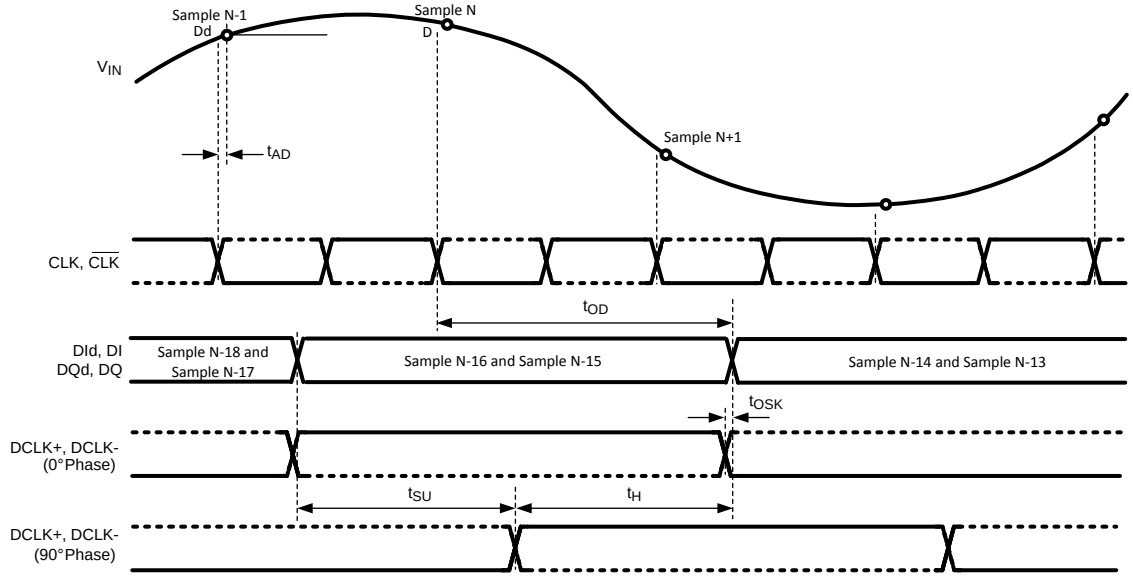


Figure 3. ADC08DL500 Timing — DDR Clocking in 1:2 Demultiplexed Mode

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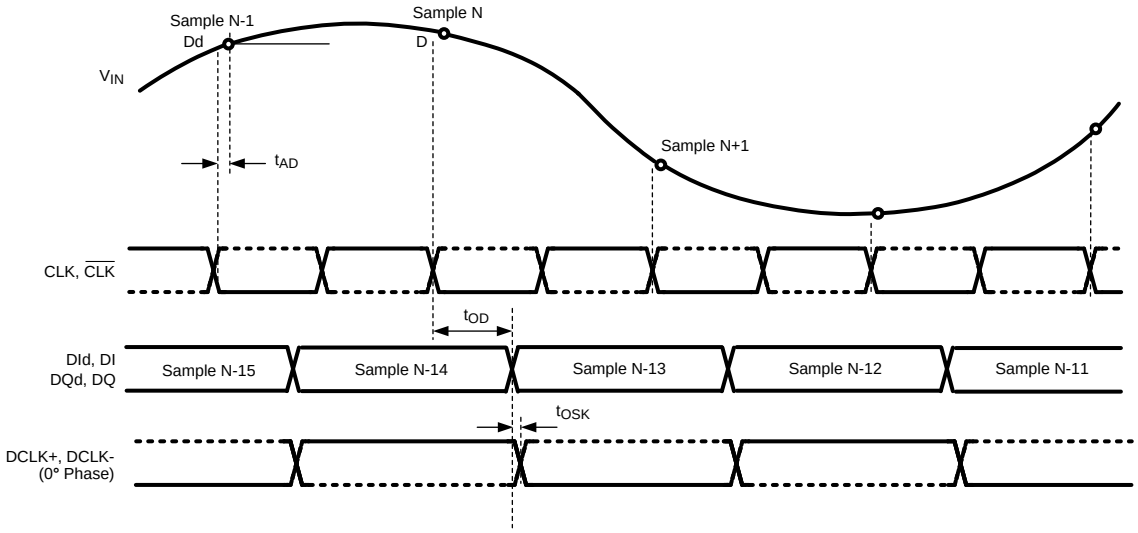


Figure 4. ADC08DL500 Timing — DDR Clocking in Non-Demultiplexed Mode

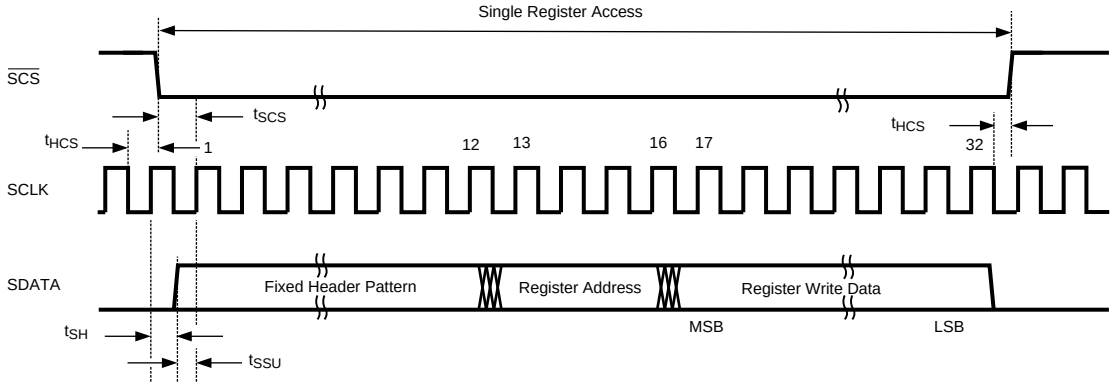


Figure 5. Serial Interface Timing

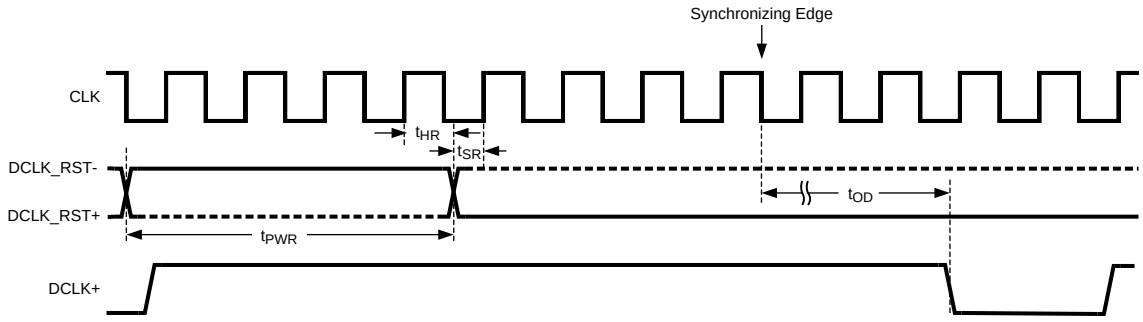


Figure 6. Clock Reset Timing in DDR Mode

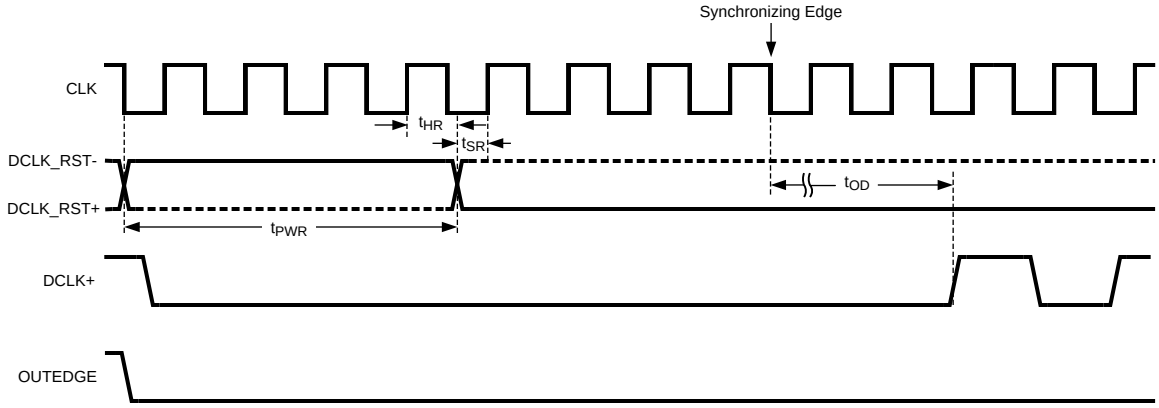


Figure 7. Clock Reset Timing in SDR Mode with OUTEDGE Low

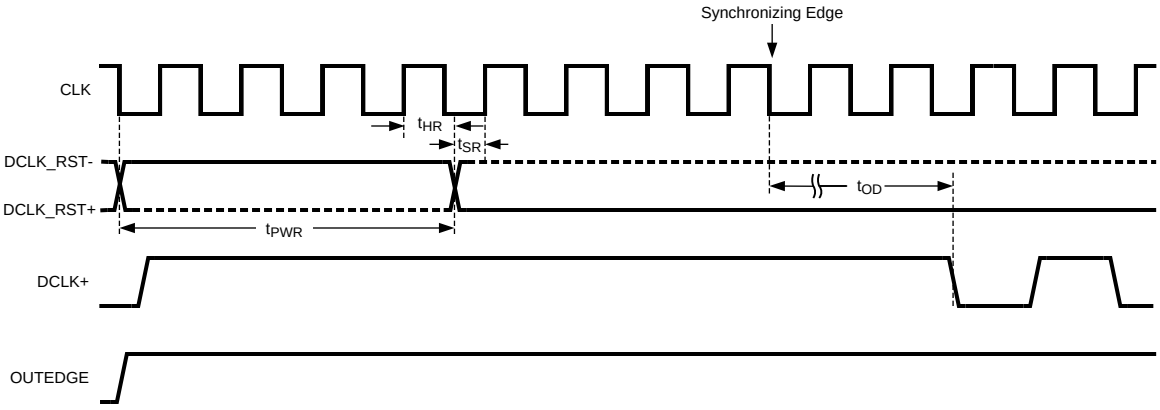


Figure 8. Clock Reset Timing in SDR Mode with OUTEDGE High

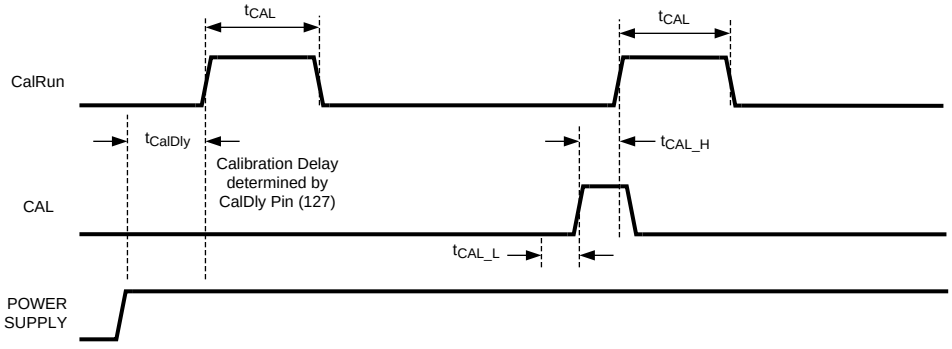


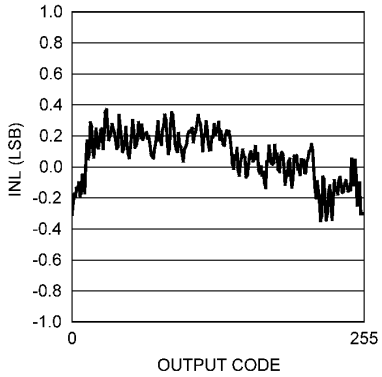
Figure 9. Power-up Calibration and On-Command Calibration Timing

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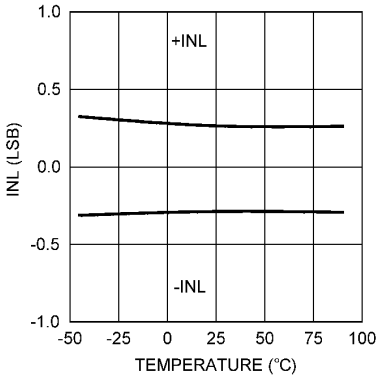
Typical Performance Characteristics

$V_A = V_{DR} = 1.9V$, $f_{CLK} = 500$ MHz, $f_{IN} = 125$ MHz, $T_A = 25°C$, I channel, 1:2 Demux Mode (1:1 Demux Mode has similar performance), unless otherwise stated.

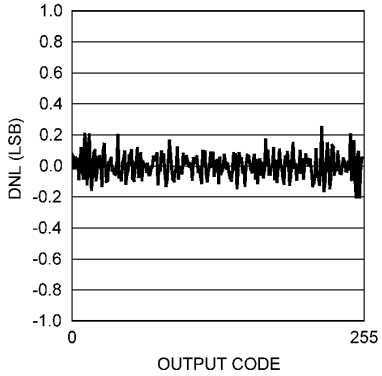
INL vs. CODE



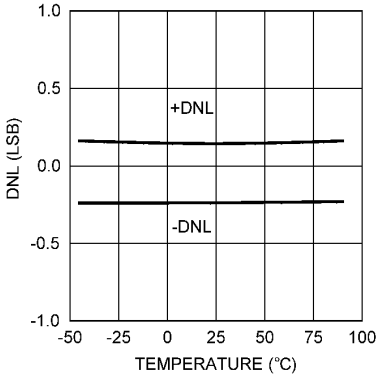
INL vs. AMBIENT TEMPERATURE



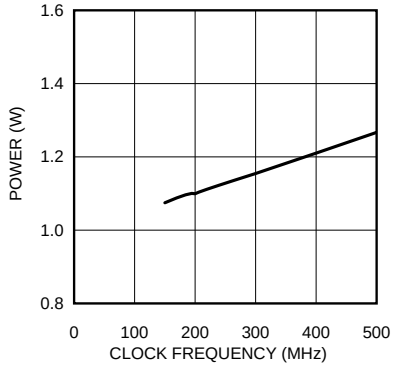
DNL vs. CODE



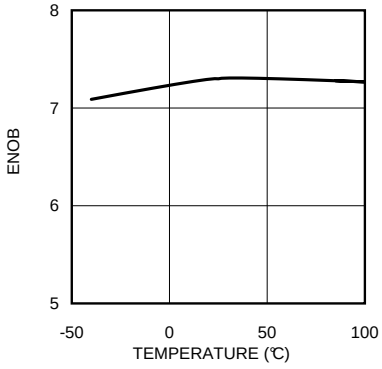
DNL vs. AMBIENT TEMPERATURE



POWER CONSUMPTION vs. CLOCK FREQUENCY



ENOB vs. AMBIENT TEMPERATURE

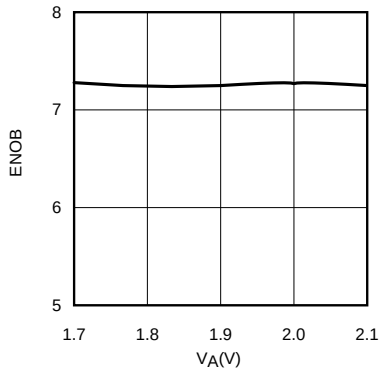


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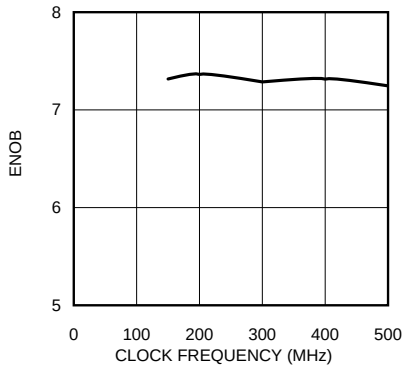
Typical Performance Characteristics (continued)

$V_A = V_{DR} = 1.9V$, $f_{CLK} = 500$ MHz, $f_{IN} = 125$ MHz, $T_A = 25°C$, I channel, 1:2 Demux Mode (1:1 Demux Mode has similar performance), unless otherwise stated.

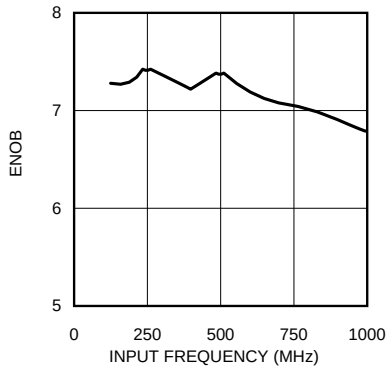
ENOB vs. SUPPLY VOLTAGE



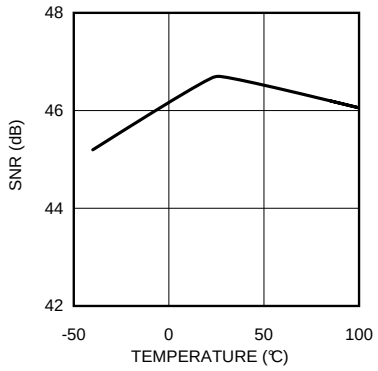
ENOB vs. CLOCK FREQUENCY



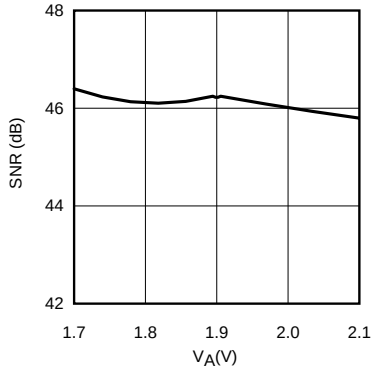
ENOB vs. INPUT FREQUENCY



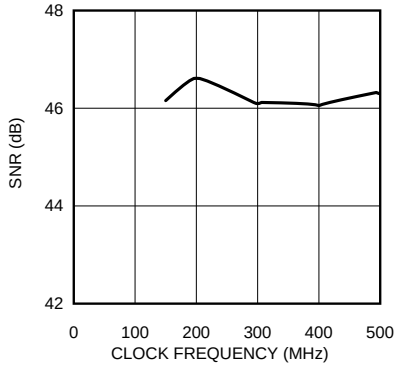
SNR vs. AMBIENT TEMPERATURE



SNR vs. SUPPLY VOLTAGE



SNR vs. CLOCK FREQUENCY

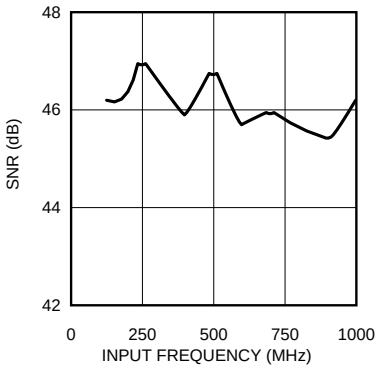


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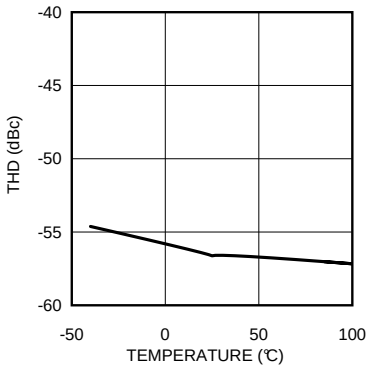
Typical Performance Characteristics (continued)

$V_A = V_{DR} = 1.9V$, $f_{CLK} = 500$ MHz, $f_{IN} = 125$ MHz, $T_A = 25°C$, I channel, 1:2 Demux Mode (1:1 Demux Mode has similar performance), unless otherwise stated.

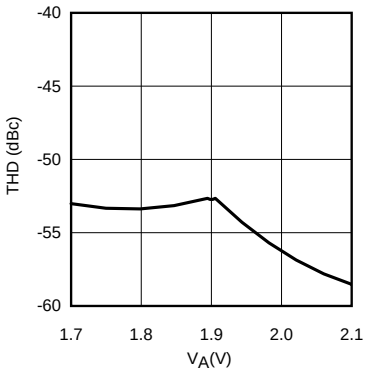
SNR vs. INPUT FREQUENCY



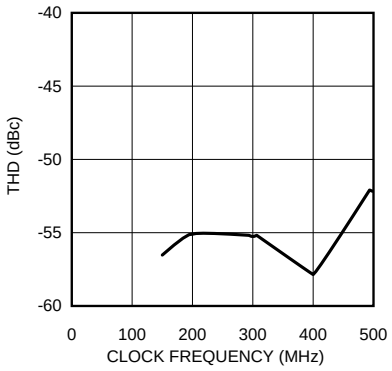
THD vs. AMBIENT TEMPERATURE



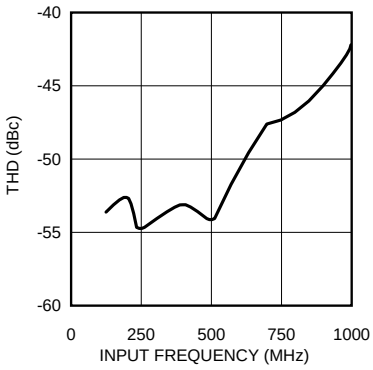
THD vs. SUPPLY VOLTAGE



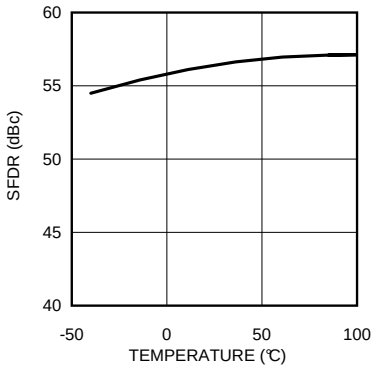
THD vs. CLOCK FREQUENCY



THD vs. INPUT FREQUENCY



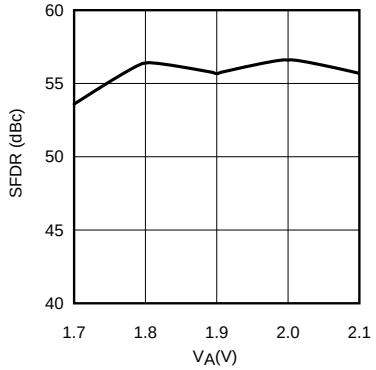
SFDR vs. AMBIENT TEMPERATURE



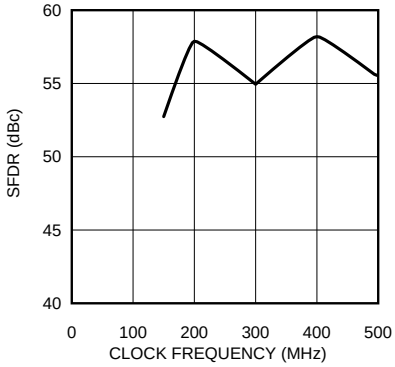
Typical Performance Characteristics (continued)

V_A = V_{DR} = 1.9V, f_{CLK} = 500 MHz, f_{IN} = 125 MHz, T_A= 25°C, I channel, 1:2 Demux Mode (1:1 Demux Mode has similar performance), unless otherwise stated.

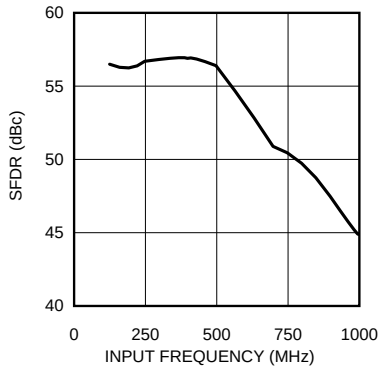
SFDR vs. SUPPLY VOLTAGE



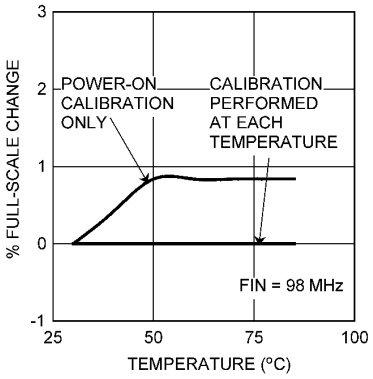
SFDR vs. CLOCK FREQUENCY



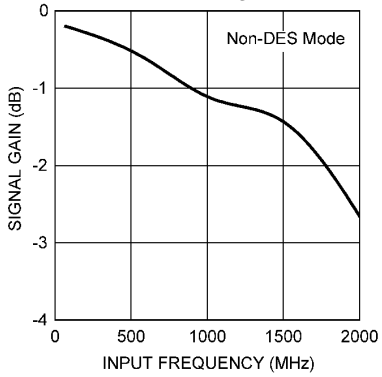
SFDR vs. INPUT FREQUENCY



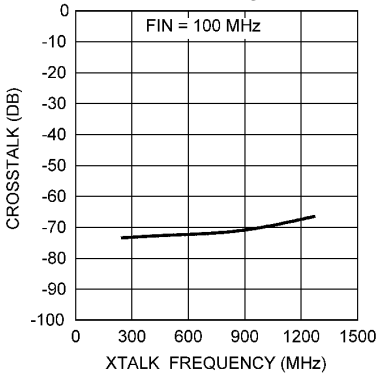
GAIN STABILITY vs. DIE TEMPERATURE



SIGNAL GAIN vs. INPUT FREQUENCY



CROSSTALK vs. SOURCE FREQUENCY

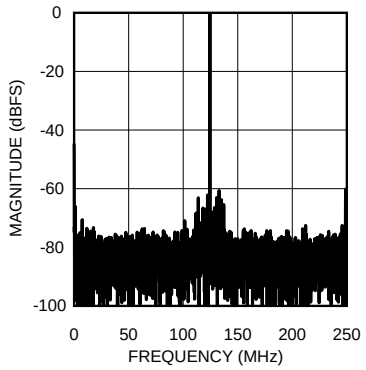


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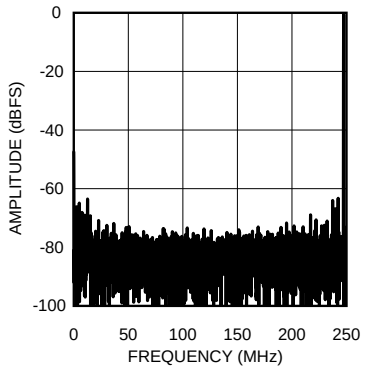
Typical Performance Characteristics (continued)

V_A = V_{DR} = 1.9V, f_{CLK} = 500 MHz, f_{IN} = 125 MHz, T_A= 25°C, I channel, 1:2 Demux Mode (1:1 Demux Mode has similar performance), unless otherwise stated.

SPECTRAL RESPONSE AT f_{IN} = 125 MHz



SPECTRAL RESPONSE AT f_{IN} = 248 MHz



Functional Description

NOT ALL OF THE PINS, BITS, AND FEATURES WHICH ARE MENTIONED IN THIS SECTION ARE TESTED IN PRODUCTION TEST. SEE (1) (2) (3) (4) IN THE PIN DESCRIPTIONS, THE CONVERTER ELECTRICAL CHARACTERISTICS, Table 4, Table 5, AND THE REGISTER DESCRIPTION FOR A DETAILED EXPLANATION OF WHAT IS TESTED. IF THE SYSTEM APPLICATION REQUIRES ADDITIONAL FEATURES OF THE PRODUCT TO BE TESTED, CONTACT YOUR NATIONAL SALES REPRESENTATIVE.

The ADC08DL500 is a versatile A/D Converter with an innovative architecture permitting very high speed operation. The controls available ease the application of the device to circuit solutions. Optimum performance requires adherence to the provisions discussed here and in the Applications Information Section.

While it is generally poor practice to allow an active pin to float, pins 6 and 16 of the ADC08DL500 are designed to be left floating without jeopardy. In all discussions throughout this data sheet, whenever a function is called by allowing a control pin to float, connecting that pin to a potential of one half the V_A supply voltage will have the same effect as allowing it to float.

OVERVIEW

The ADC08DL500 uses a calibrated folding and interpolating architecture that achieves 7.2 effective bits. The use of folding amplifiers greatly reduces the number of comparators and power consumption. Interpolation reduces the number of front-end amplifiers required, minimizing the load on the input signal and further reducing power requirements. In addition to other things, on-chip calibration reduces the INL bow often seen with folding architectures. The result is an extremely fast, high performance, low power converter.

The analog input signal that is within the converter's input voltage range is digitized to eight bits at speeds of 200 MSPS to 500 MSPS. Differential input voltages below negative full-scale will cause the output word to consist of all zeroes. Differential input voltages above positive full-scale will cause the output word to consist of all ones. Either of these conditions at either the "I" or "Q" input will cause the OR (Out of Range) output to be activated. This single OR output indicates when the output code from one or both of the channels is below negative full scale or above positive full scale.

Each converter has a selectable output demultiplexer which feeds two LVDS buses. If the 1:2 demultiplexed mode is selected, the output data rate is reduced to half the input sample rate on each bus. When non-demultiplexed mode is selected, that output data rate on channels DI and DQ are at the same rate as the input sample clock.

The output levels may be selected to be normal or reduced. Using reduced levels saves power but could result in erroneous data capture of some or all of the bits, especially at higher sample rates and in marginally designed systems.

(1) This pin/bit functionality is not tested in production test; performance is tested in the specified/default mode only.
(2) This feature functionality is not tested in production test; performance is tested in the specified/default mode only.
(3) Only the end points of the range, not the full sweep, are tested in production test.
(4) Coarse and intermediate step size are tested in major steps only in production test; fine step size is not tested.

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Calibration

A calibration is performed upon power-up and can also be invoked by the user upon command. Calibration trims the analog input differential termination resistor and minimizes full-scale error, offset error, DNL and INL, resulting in maximizing SNR, THD, SINAD (SNDR) and ENOB. Internal bias currents are also set with the calibration process. All of this is true whether the calibration is performed upon power up or is performed upon command. Running the calibration is an important part of this chip's functionality and is required in order to obtain adequate performance. In addition to the requirement to be run at power-up, an on-command calibration must be run whenever the sense of the FSR pin is changed. For best performance, we recommend that an on-command calibration be run 20 seconds or more after application of power and whenever the operating temperature changes significantly relative to the specific system performance requirements. See On-Command Calibration for more information. Calibration can not be initiated or run while the device is in the power-down mode. See Power Down for information on the interaction between Power Down and Calibration.

In normal operation, calibration is performed just after application of power and whenever a valid calibration command is given, which is holding the CAL pin low for at least t_{CAL_L} clock cycles, then hold it high for at least another t_{CAL_H} clock cycles as defined in the Converter Electrical Characteristics. The time taken by the calibration procedure is specified as t_{CAL}in Converter Electrical Characteristics. Holding the CAL pin high upon power up will prevent the calibration process from running until the CAL pin experiences the above-mentioned t_{CAL_L} clock cycles followed by t_{CAL_H} clock cycles.

CalDly (pin 141) is used to select one of two delay times that apply from the application of power to the start of calibration. This calibration delay time is depedent on the setting of the CalDly pin and is specified as t_{CalDly} in the Converter Electrical Characteristics. These delay values allow the power supply to come up and stabilize before calibration takes place. If the PD pin is high upon power-up, the calibration delay counter will be disabled until the PD pin is brought low. Therefore, holding the PD pin high during power up will further delay the start of the power-up calibration cycle. The best setting of the CalDly pin depends upon the power-on settling time of the power supply.

The CAL bit does not reset itself to zero automatically, but must be manually reset before another calibration event can be initiated. If no further calibration event is desired, the CAL bit may be left high indefinitely, with no negative consequences. The RTD bit setting is critical for running a calibration event with the Clock Phase Adjust enabled. If initiating a calibration event while the Clock Phase Adjust is enabled, the RTD bit must be set to high, or no calibration will occur. If initiating a calibration event while the Clock Phase Adjust is not enabled, a normal calibration will occur, regardless of the setting of the RTD bit.

Acquiring the Input

In 1:2 demux mode, data is acquired at the falling edge of CLK+ (pin 20) and the digital equivalent of that data is available at the digital outputs 13 input clock cycles later for the DI and DQ output buses and 14 input clock cycles later for the DId and DQd output buses. There is an additional internal delay called t_{OD} before the data is available at the outputs. See the Timing Diagram. The ADC08DL500 will convert as long as the input clock signal is present. The fully differential comparator design and the innovative design of the sample-and-hold amplifier, together with calibration, enables a very flat SINAD/ENOB response beyond 1 GHz. The ADC08DL500 output data signaling is LVDS and the output format is offset binary.

Control Modes

Much of the user control can be accomplished with several control pins that are provided. Examples include initiation of the calibration cycle, power down mode and full scale range setting. However, the ADC08DL500 also provides an Extended Control mode whereby a serial interface is used to access register-based control of several advanced features. The Extended Control mode is not intended to be enabled and disabled dynamically. Rather, the user is expected to employ either the normal control mode or the Extended Control mode at all times. When the device is in the Extended Control mode, pin-based control of several features is replaced with register-based control and those pin-based controls are disabled. These pins are OutV (pin 5), OutEdge/DDR (pin 6), FSR (pin 16) and CalDly (pin 141). See NORMAL/EXTENDED CONTROL for details on the Extended Control mode.

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The Analog Inputs

The ADC08DL500 must be driven with a differential input signal. Operation with a single-ended signal is not allowed. It is important that the inputs either be a.c. coupled to the inputs with the V_{CMO} pin grounded, or d.c. coupled with the V_{CMO} pin left floating. An input common mode voltage equal to the V_{CMO} output must be provided when d.c. coupling is used.

Two full-scale range settings are provided with pin 16 (FSR). A high on pin 16 causes an input full-scale range setting of a higher V_{IN} input level, while grounding pin 16 causes an input full-scale range setting of a reduced V_{IN} input level. The full-scale range setting operates equally on both ADCs.

In the Extended Control mode, programming the Input Full-Scale Voltage Adjust register allows the input full-scale range to be adjusted as described in REGISTER DESCRIPTION and THE ANALOG INPUT.

Clocking

The ADC08DL500 must be driven with an a.c. coupled, differential clock signal. 2.3 THE CLOCK INPUTS describes the use of the clock input pins. A differential LVDS output clock is available for use in latching the ADC output data into whatever device is used to receive the data.

The ADC08DL500 offers two output clocking options. These are a choice of which DCLK edge the output data transitions on, and a choice of Single Data Rate (SDR) or Double Data Rate (DDR) outputs.

The ADC08DL500 also has the option to use a duty cycle corrected clock receiver as part of the input clock circuit. This feature is enabled by default and provides improved ADC clocking. This circuitry allows the ADC to be clocked with a signal source having a duty cycle ratio of 20% / 80% (worst case).

Table 2. Input Channel Samples Produced at Data Outputs in 1:2 Demultiplexed Mode(1)

Data Outputs (Always sourced with respect to fall of DCLK+)	
DI	"I" Input Sampled with Fall of CLK 13 cycles earlier.
DId	"I" Input Sampled with Fall of CLK 14 cycles earlier.
DQ	"Q" Input Sampled with Fall of CLK 13 cycles earlier.
DQd	"Q" Input Sampled with Fall of CLK 14 cycles after being sampled.

(1) Note that, in the non-demultiplexed mode, the DId and DQd outputs are disabled and are high impedance.

Table 3. Input Channel Samples Produced at Data Outputs in Non-Demultiplexed Mode

Data Outputs (Sourced with respect to fall of DCLK+)	
DI	"I" Input Sampled with Fall of CLK 13 cycles earlier.
DId	No output.
DQ	"Q" Input Sampled with Fall of CLK 13 cycles earlier.
DQd	No output.

OutEdge and Demultiplex Control Setting

To help ease data capture in the SDR mode, the output data may be caused to transition on either the positive or the negative edge of the output data clock (DCLK). In the non-extended control mode, this is chosen with the OutEdge input (pin 6). A high on the OutEdge input pin causes the output data to transition on the rising edge of DCLK+, while grounding this input causes the output to transition on the falling edge of DCLK+. See Output Edge Synchronization. When in the extended control mode, the OutEdge is selected using the OED bit in the Configuration Register. This bit has two functions. In the single data rate (SDR) mode, the bit functions as OutEdge and selects the DCLK edge with which the data transitions. In the Double Data Rate (DDR) mode, this bit selects whether the device is in non-demultiplex or 1:2 demultiplex mode. In the DDR case, the DCLK has a 0° phase relationship with the output data independent of the demultiplexer selection. For 1:2 Demux DDR 0° Mode, there are four, as opposed to three cycles of CLK systematic delay from the Synchronizing Edge to the start of t_{OD}. See MULTIPLE ADC SYNCHRONIZATIONfor more details.

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1Single Data Rate and Double Data Rate

A choice of single data rate (SDR) or double data rate (DDR) output is offered. With single data rate the output clock (DCLK) frequency is the same as the data rate of the two output buses. With double data rate the DCLK frequency is half the data rate and data is sent to the outputs on both edges of DCLK. DDR clocking is enabled in non-Extended Control mode by allowing pin 6 to float.

The LVDS Outputs

The data outputs, the Out Of Range (OR) and DCLK, are LVDS. The electrical specifications of the LVDS outputs are compatible with typical LVDS receivers available on ASIC and FPGA chips; but they are not IEEE or ANSI communications standards compliant due to the low +1.9V supply used this chip. User is given the choice of a lower signal amplitude mode with OutV control pin or the OV control register bit. For short LVDS lines and low noise systems, satisfactory performance may be realized with the OutV input low, which results in lower power consumption. If the LVDS lines are long and/or the system in which the ADC08DL500 is used is noisy, it may be necessary to tie the OutV pin high.

The LVDS data output have a typical common mode voltage when the V_{BG} pin is unconnected and floating. This common mode voltage can be increased by tying the V_{BG} pin to V_A if a higher common mode is required.

IMPORTANT NOTE: Tying the V_{BG} pin to V_A will also increase the differential LVDS output voltage by up to 40 mV.

Power Down

The ADC08DL500 is in the active state when the Power Down pin (PD) is low. When the PD pin is high, the device is in the power down mode. In this power down mode the data output pins (positive and negative) are put into a high impedance state and the devices power consumption is reduced to a minimal level. The DCLK+/- and OR +/- are not tri-stated, they are weakly pulled down to ground internally. Therefore when both I and Q are powered down the DCLK +/- and OR +/- should not be terminated to a DC voltage.

A high on the PDQ pin will power down the "Q" channel and leave the "I" channel active. There is no provision to power down the "I" channel independently of the "Q" channel. Upon return to normal operation, the pipeline will contain meaningless information.

If the PD input is brought high while a calibration is running, the device will not go into power down until the calibration sequence is complete. However, if power is applied and PD is already high, the device will not begin the calibration sequence until the PD input goes low. If a manual calibration is requested while the device is powered down, the calibration will not begin at all. That is, the manual calibration input is completely ignored in the power down state. Calibration will function with the "Q" channel powered down, but that channel will not be calibrated if PDQ is high. If the "Q" channel is subsequently to be used, it is necessary to perform a calibration after PDQ is brought low.

NORMAL/EXTENDED CONTROL

The ADC08DL500 may be operated in one of two modes. In the simpler standard control mode, the user affects available configuration and control of the device through several control pins. The "extended control mode" provides additional configuration and control options through a serial interface and a set of 9 registers. Extended control mode is selected by setting pin 47 to logic low. If pin 47 is floating and pin 58 is floating or logic high, pin 16 can be used to enable the extended control mode. The choice of control modes is required to be a fixed selection and is not intended to be switched dynamically while the device is operational.

Table 4 shows how several of the device features are affected by the control mode chosen.

Table 4. Features and Modes

Feature	Normal Control Mode	Extended Control Mode
SDR or DDR Clocking	Selected with pin 6	Selected with nDE in the Configuration Register (Addr-1h; bit-10).
DDR Clock Phase (1)	Not Selectable (0° Phase Only)	Selected with DCP in the Configuration Register (Addr-1h; bit-11).

(1) This feature functionality is not tested in production test; performance is tested in the specified/default mode only.

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Table 4. Features and Modes (continued)

SDR Data transitions with rising or falling DCLK edge	SDR Data transitions with rising edge of DCLK+ when pin 6 is high and on falling edge when low.	Selected with OED in the Configuration Register (Addr-1h; bit-8).
LVDS output level (1)	Normal differential data and DCLK amplitude selected when pin 5 is high and reduced amplitude selected when low.	Selected with OV in the Configuration Register (Addr-1h; bit-9).
Power-On Calibration Delay (1)	Short delay selected when pin 141 is low and longer delay selected when high.	Short delay only.
Full-Scale Range (2)	Normal input full-scale range selected when pin 16 is high and reduced range when low. Selected range applies to both channels.	Up to 512 step adjustments over a nominal range specified in REGISTER DESCRIPTION. Separate range selected for I- and Q-Channels. Selected using Full Range Registers (Addr-3h and Bh; bit-7 thru 15).
Input Offset Adjust (2)	Not possible	512 steps of adjustment using the Input Offset register specified in REGISTER DESCRIPTION for each channel using Input Offset Registers (Addr-2h and Ah; bit-7 thru 15).
Test Pattern	Not possible	A test pattern can be made present at the data outputs by setting TPO to 1b in Extended Configuration Register (Addr-9h; bit-15).
Resistor Trim Disable	Not possible	The DCLK outputs will continuously be present when RTD is set to 1b in Extended Configuration Register (Addr-9h; bit-14 to 7).
Selectable Output Demultiplexer	Not possible	If the device is set in DDR, the output can be programmed to be non-demultiplex. When OED in Configuration Register is set 1b (Addr-1h; bit-8), this selects non-demultiplex. If OED is set 0b, this selects 1:2 demultiplex.
Second DCLK Output (3)	Not possible	The OR outputs can be programmed to become a second DCLK output when nSD is set 0b in Configuration Register (Addr-1h; bit-13).
Sampling Clock Phase Adjust (4)	Not possible	The sampling clock phase can be manually adjusted through the Coarse and Intermediate Register (Addr-Fh; bit-15–7) and Fine Register (Addr-Eh; bit-15 to 8).

(2) Only the end points of the range, not the full sweep, are tested in production test.
(3) This feature functionality is not tested in production test; performance is tested in the specified/default mode only.
(4) Coarse and intermediate step size are tested in major steps only in production test; fine step size is not tested.

The default state of the Extended Control Mode is set upon power-on reset (internally performed by the device) and is shown in Table 5.

Table 5. Extended Control Mode Operation (Pin 41 Logic Low or Pin 14 Floating)

Feature	Extended Control Mode Default State
SDR or DDR Clocking	DDR Clocking
DDR Clock Phase (1)	Data changes with DCLK edge (0° phase)
LVDS Output Amplitude (1)	Higher value indicated in Electrical Table
Calibration Delay (1)	Short Delay
Full-Scale Range (2)	700 mV nominal for both channels
Input Offset Adjust (2)	No adjustment for either channel
Test Pattern	Not present at output
Resistor Trim Disable	Trim enabled, DCLK not continuously present at output
Selectable Output Demultiplexer	1:2 demultiplex
Second DCLK Output (1)	Not present, pins 89 and 90 function as OR+ and OR-
Sampling Clock Phase Adjust (3)	No adjustment for fine, intermediate or coarse

(1) This feature functionality is not tested in production test; performance is tested in the specified/default mode only.
(2) Only the end points of the range, not the full sweep, are tested in production test.
(3) Coarse and intermediate step size are tested in major steps only in production test; fine step size is not tested.

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THE SERIAL INTERFACE

IMPORTANT NOTE: During the initial write using the serial interface, all nine registers must be written with desired or default values. Subsequent writes to single registers are allowed.

The 3-pin serial interface is enabled only when the device is in the Extended Control mode. The pins of this interface are Serial Clock (SCLK), Serial Data (SDATA) and Serial Interface Chip Select ($\overline{SCS}$). Nine write only registers are accessible through this serial interface.

$\overline{SCS}$: This signal should be asserted low while accessing a register through the serial interface. Setup and hold times with respect to the SCLK must be observed.

SCLK: Serial data input is accepted at the rising edge of this signal. There is no minimum frequency requirement for SCLK.

SDATA: Each register access requires a specific 32-bit pattern at this input. This pattern consists of a header, register address and register value. The data is shifted in MSB first. Setup and hold times with respect to the SCLK must be observed. See the Timing Diagram.

Each Register access consists of 32 bits, as shown in Figure 5 of the Timing Diagrams. The fixed header pattern is 0000 0000 0001 (eleven zeros followed by a 1). The loading sequence is such that a "0" is loaded first. These 12 bits form the header. The next 4 bits are the address of the register that is to be written to and the last 16 bits are the data written to the addressed register. The addresses of the various registers are indicated in Table 6.

Refer to the Register Description (REGISTER DESCRIPTION) for information on the data to be written to the registers.

Subsequent register accesses may be performed immediately, starting with the 33rd SCLK. This means that the $\overline{SCS}$ input does not have to be de-asserted and asserted again between register addresses. It is possible, although not recommended, to keep the $\overline{SCS}$ input permanently enabled (at a logic low) when using extended control.

Control register contents are retained when the device is put into power-down mode.

IMPORTANT NOTE: Do not write to the Serial Interface when calibrating the ADC. Doing so will impair the performance of the device until it is re-calibrated correctly. Programming the serial registers will also reduce dynamic performance of the ADC for the duration of the register access time.

Table 6. Register Addresses

4-Bit Address					
Loading Sequence: A3 loaded after Fixed Header pattern, A0 loaded last					
A3	**A2**	**A1**	**A0**	**Hex**	**Register Addressed**
0	0	0	0	0h	Calibration
0	0	0	1	1h	Configuration
0	0	1	0	2h	"I" Ch Offset
0	0	1	1	3h	"I" Ch Full-Scale Voltage Adjust
0	1	0	0	4h	Reserved
0	1	0	1	5h	Reserved
0	1	1	0	6h	Reserved
0	1	1	1	7h	Reserved
1	0	0	0	8h	Reserved
1	0	0	1	9h	Extended Configuration
1	0	1	0	Ah	"Q" Ch Offset
1	0	1	1	Bh	"Q" Ch Full-Scale Voltage Adjust
1	1	0	0	Ch	Reserved
1	1	0	1	Dh	Reserved
1	1	1	0	Eh	Sampling Clock Phase Fine Adjust
1	1	1	1	Fh	Sample Clock Phase Intermediate and Coarse Adjust

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REGISTER DESCRIPTION

NOT ALL OF THE PINS, BITS, AND FEATURES WHICH ARE MENTIONED IN THIS SECTION ARE TESTED IN PRODUCTION TEST. SEE (1) (2) (3) (4) IN THE PIN DESCRIPTIONS, THE CONVERTER ELECTRICAL CHARACTERISTICS, Table 4, Table 5, AND THE REGISTER DESCRIPTION FOR A DETAILED EXPLANATION OF WHAT IS TESTED. IF THE SYSTEM APPLICATION REQUIRES ADDITIONAL FEATURES OF THE PRODUCT TO BE TESTED, CONTACT YOUR NATIONAL SALES REPRESENTATIVE.

Nine write-only registers provide several control and configuration options in the Extended Control Mode. These registers have no effect when the device is in the Normal Control Mode. Each register description below also shows the Power-On Reset (POR) state of each control bit.

Table 7. Calibration Register

Addr: 0h (0000b)	**Write only (0x7FFF)**

(1) This pin/bit functionality is not tested in production test; performance is tested in the specified/default mode only.
(2) This feature functionality is not tested in production test; performance is tested in the specified/default mode only.
(3) Only the end points of the range, not the full sweep, are tested in production test.
(4) Coarse and intermediate step size are tested in major steps only in production test; fine step size is not tested.

D15	D14	D13	D12	D11	D10	D9	D8
CAL	1	1	1	1	1	1	1

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Bit 15	CAL: Calibration Enable. When this bit is set 1b, an on-command calibration cycle is initiated. This function is exactly the same as issuing an on-command calibration using the CAL pin. (1)
	POR State: 0b
Bits 14:0	Must be set to 1b

(1) This pin/bit functionality is not tested in production test; performance is tested in the specified/default mode only.

Table 8. Configuration Register

Addr: 1h (0001b)	**Write only (0xB2FF)**

D15	D14	D13	D12	D11	D10	D9	D8
1	0	nSD	DCS	DCP	nDE	OV	OED

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Bit 15	Must be set to 1b
Bit 14	Must be set to 0b
Bit 13	nSD: Second DCLK Output Enable. When this bit is 1b, the device only has one DCLK output and one OR output. When this bit is 0b, the device has two identical DCLK outputs and no OR output. (1)
	POR State: 1b
Bit 12	DCS: Duty Cycle Stabilizer. When this bit is set to 1b, a duty cycle stabilization circuit is applied to the clock input. When this bit is set to 0b the stabilization circuit is disabled. (1)
	POR State: 1b
Bit 11	DCP: DDR Clock Phase. This bit only has an effect in the DDR mode. When this bit is set to 0b, the DCLK edges are time-aligned with the data bus edges ("0° Phase"). When this bit is set to 1b, the DCLK edges are placed in the middle of the data bit-cells ("90° Phase"), using the one-half speed DCLK shown in Figure 3 as the phase reference. (1)
	POR State: 0b

(1) This pin/bit functionality is not tested in production test; performance is tested in the specified/default mode only.

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Bit 10	nDE: DDR Enable. When this bit is set to 0b, data bus clocking follows the DDR (Double Data Rate) mode whereby a data word is output with each rising and falling edge of DCLK. When this bit is set to a 1b, data bus clocking follows the SDR (single data rate) mode whereby each data word is output with either the rising or falling edge of DCLK , as determined by the OutEdge bit.
	POR State: 0b
Bit 9	OV: Output Voltage. This bit determines the LVDS outputs' voltage amplitude and has the same function as the OutV pin that is used in the normal control mode. When this bit is set to 1b, the standard output amplitude is used. When this bit is set to 0b, the reduced output amplitude is used. (1)
	POR State: 1b
Bit 8	OED: Output Edge and Demultiplex Control. This bit has two functions. When the device is in SDR mode, this bit selects the DCLK edge with which the data words transition and has the same effect as the OutEdge pin in the Non-extended control mode. When this bit is set to 1b, the data outputs change with the rising edge of DCLK+. When this bit is set to 0b, the data output changes with the falling edge of DCLK+. When the device is in DDR mode, this bit selects the non-demultiplexed mode when set to 1b. When the bit set to 0b, the device is programmed into the Demultiplexed mode. If the device is in DDR and Non-Demultiplexed Mode, then the DCLK has a 0° phase relationship with the data; it is not possible to select the 90° phase relationship.
	POR State: 0b
Bits 7:0	Must be set to 1b

IMPORTANT NOTE: It is recommended that this register should only be written upon power-up initialization as writing it may cause disturbance on the DCLK output as this signal's basic configuration is changed.

Table 9. I-Channel Offset (1)

Addr: 2h (0010b)	**Write only (0x007F)**

(1) Only the end points of the range, not the full sweep, are tested in production test.

D15	D14	D13	D12	D11	D10	D9	D8
(MSB)		Offset Value					(LSB)

D7	D6	D5	D4	D3	D2	D1	D0
Sign	1	1	1	1	1	1	1

Bits 15:8	Offset Value. The input offset of the I-Channel ADC is adjusted linearly and monotonically by the value in this field. 00h provides a nominal zero offset, while FFh provides a nominal 45 mV of offset. Thus, each code step provides 0.176 mV of offset.
	POR State: 0000 0000 b
Bit 7	Sign bit. 0b gives positive offset, 1b gives negative offset, resulting in total offset adjustment of ±45 mV.
	POR State: 0b
Bits 6:0	Must be set to 1b

Table 10. I-Channel Full-Scale Voltage Adjust (1)

Addr: 3h (0011b)	**Write only (0x807F)**

(1) Only the end points of the range, not the full sweep, are tested in production test.

D15	D14	D13	D12	D11	D10	D9	D8
(MSB)	Adjust Value						

D7	D6	D5	D4	D3	D2	D1	D0
(LSB)	1	1	1	1	1	1	1

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Bits 15:7	Full Scale Voltage Adjust Value. The input full-scale voltage or gain of the I-Channel ADC is adjusted linearly and monotonically with a 9 bit data value. The adjustment range is ±20% of the nominal 700 mV_{P-P} differential value.	
	0000 0000 0	560 mV_{P-P}
	1000 0000 0 Default Value	700 mV_{P-P}
	1111 1111 1	840 mV_{P-P}
	For best performance, it is recommended that the value in this field be limited to the range of 0110 0000 0b to 1110 0000 0b. i.e., limit the amount of adjustment to ±15%. The remaining ±5% headroom allows for the ADC's own full scale variation. A gain adjustment does not require ADC re-calibration.	
	POR State: 1000 0000 0b (no adjustment)	
Bits 6:0	Must be set to 1b	

Table 11. Extended Configuration Register

Addr: 9h (1001b)	**Write only (0x03FF)**

D15	D14	D13	D12	D11	D10	D9	D8
TPO	RTD	0	0	0	0	1	1

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Bit 15	TPO: Test Pattern Output. When this bit is set 1b, the ADC is disengaged and a test pattern generator is connected to the outputs including OR. This test pattern will work with the device in the SDR, DDR and the non-demultiplex output modes.
	POR State: 0b
Bit 14	RTD: Resistor Trim Disable. When this bit is set to 1b, the input termination resistor is not trimmed during the calibration cycle and the DCLK output remains enabled. Note that the ADC is calibrated regardless of this setting.
	POR State: 0b
Bit 13:10	Must be set to 0b
Bits 9:0	Must be set to 1b

Table 12. Q-Channel Offset (1)

Addr: Ah (1010b)	**Write only (0x007F)**

(1) Only the end points of the range, not the full sweep, are tested in production test.

D15	D14	D13	D12	D11	D10	D9	D8
(MSB)		Offset Value					(LSB)

D7	D6	D5	D4	D3	D2	D1	D0
Sign	1	1	1	1	1	1	1

Bits 15:8	Offset Value. The input offset of the Q-Channel ADC is adjusted linearly and monotonically by the value in this field. 00h provides a nominal zero offset, while FFh provides a nominal 45 mV of offset. Thus, each code step provides about 0.176 mV of offset.
	POR State: 0000 0000 b
Bit 7	Sign bit. 0b gives positive offset, 1b gives negative offset.
	POR State: 0b
Bits 6:0	Must be set to 1b

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Table 13. Q-Channel Full-Scale Voltage Adjust (1)

Addr: Bh (1011b)	Write only (0x807F)

(1) Only the end points of the range, not the full sweep, are tested in production test.

D15	D14	D13	D12	D11	D10	D9	D8
(MSB)	Adjust Value						

D7	D6	D5	D4	D3	D2	D1	D0
(LSB)	1	1	1	1	1	1	1

Bits 15:7	Full Scale Voltage Adjust Value. The input full-scale voltage or gain of the I-Channel ADC is adjusted linearly and monotonically with a 9 bit data value. The adjustment range is ±20% of the nominal 700 mV_{P-P} differential value.	
	0000 0000 0	560 mV_{P-P}
	1000 0000 0	700 mV_{P-P}
	1111 1111 1	840 mV_{P-P}
	For best performance, it is recommended that the value in this field be limited to the range of 0110 0000 0b to 1110 0000 0b. i.e., limit the amount of adjustment to ±15%. The remaining ±5% headroom allows for the ADC's own full scale variation. A gain adjustment does not require ADC re-calibration.	
	POR State: 1000 0000 0b (no adjustment)	
Bits 6:0	Must be set to 1b	

Table 14. Sample Clock Phase Fine Adjust (1)

Addr: 1110	Write only (0x00FF)

(1) Coarse and intermediate step size are tested in major steps only in production test; fine step size is not tested.

D15	D14	D13	D12	D11	D10	D9	D8
(MSB)		Fine Phase Adjust					(LSB)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Bits 15:8	Fine Phase Adjust. The phase of the ADC sampling clock is adjusted monotonically by the value in this field. 00h provides a nominal zero phase adjustment, while FFh provides a nominal 50 ps of delay. Thus, each code step provides approximately 0.2 ps of delay.
	POR State: 0000 0000b
Bits 7:0	Must be set to 1b

Table 15. Sample Clock Phase Intermediate/Coarse Adjust (1)

Addr: Fh (1111b)	Write only (0x007F)

(1) Coarse and intermediate step size are tested in major steps only in production test; fine step size is not tested.

D15	D14	D13	D12	D11	D10	D9	D8
POL	(MSB) Coarse Phase Adjust					IPA	

D7	D6	D5	D4	D3	D2	D1	D0
(LSB)	1	1	1	1	1	1	1

Bit 15	Polarity Select. When this bit is selected, the polarity of the ADC sampling clock is inverted. POR State: 0b
Bits 14:10	Coarse Phase Adjust. Each code value in this field delays the sample clock by approximately 65 ps. A value of 00000b in this field causes zero adjustment. POR State: 00000b

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Bits 9:7	Intermediate Phase Adjust. Each code value in this field delays the sample clock by approximately 11 ps. A value of 000b in this field causes zero adjustment. Maximum combined adjustment using Coarse Phase Adjust and Intermediate Phase adjust is approximately 2.1ns. POR State: 000b
Bits 6:0	Must be set to 1b

Note Regarding Clock Phase Adjust

This is a feature intended to help the system designer remove small imbalances in clock distribution traces at the board level when multiple ADCs are used. Please note, however, that enabling this feature will reduce the dynamic performance (ENOB, SNR, SFDR) some finite amount. The amount of degradation increases with the amount of adjustment applied. The user is strongly advised to (a) use the minimal amount of adjustment; and (b) verify the net benefit of this feature in his system before relying on it.

Note Regarding Extended Mode Offset Correction

When using the I or Q channel Offset Adjust registers, the following information should be noted.

For offset values of +0000 0000 and −0000 0000, the actual offset is not the same. By changing only the sign bit in this case, an offset step in the digital output code of about 1/10th of an LSB is experienced. This is shown more clearly in the Figure below.

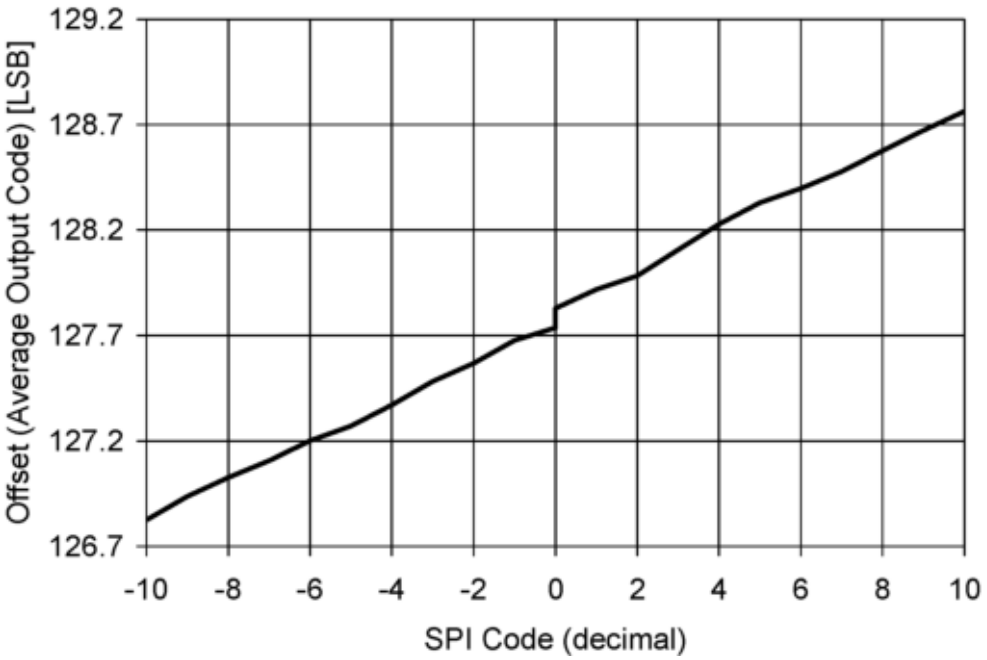


Figure 10. Extended Mode Offset Behavior

MULTIPLE ADC SYNCHRONIZATION

The ADC08DL500 has the capability to precisely reset its sampling clock input to DCLK output relationship as determined by the user-supplied DCLK_RST pulse. This allows multiple ADCs in a system to have their DCLK (and data) outputs transition at the same time with respect to the shared CLK input that all the ADCs use for sampling.

The DCLK_RST signal must observe some timing requirements that are shown in Figure 6, Figure 7 and Figure 8 of the Timing Diagrams. The DCLK_RST pulse must be of a minimum width and its deassertion edge must observe setup and hold times with respect to the CLK input rising edge. The duration of the DCLK_RST pulse affects the length of time that the digital output will take before providing valid data again after the end of the reset condition. Therefore, the DCLK_RST pulse width should be made reasonably short within the system application constraints. These timing specifications are listed as t_{RH}, t_{RS}, and t_{PWR} in the Converter Electrical Characteristics.

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The DCLK_RST signal can be asserted asynchronous to the input clock. If DCLK_RST is asserted, the DCLK output is held in a designated state. The state in which DCLK is held during the reset period is determined by the mode of operation (SDR/DDR) and the setting of the Output Edge configuration pin or bit. (Refer to Figure 6, Figure 7 and Figure 8 for the DCLK reset state conditions). Therefore, depending upon when the DCLK_RST signal is asserted, there may be a narrow pulse on the DCLK line during this reset event. When the DCLK_RST signal is de-asserted in synchronization with the CLK rising edge, there are three or four CLK cycles of systematic delay and the next CLK falling edge synchronizes the DCLK output with those of other ADC08DL500s in the system. The DCLK output is enabled again after a constant delay (relative to the input clock frequency) which is equal to the CLK input to DCLK output delay (t_{OD}). The device always exhibits this delay characteristic in normal operation. The user has the option of using a single-ended DCLK_RST signal, but a differential DCLK_RST is strongly recommended due to its superior timing specifications.

As shown in Figure 6, Figure 7, and Figure 8 of the Timing Diagrams, there is a delay from the deassertion of DCLK_RST to the reappearance of DCLK, which is equal to several cycles of CLK plus t_{OD}. Note that the deassertion of DCLK_RST is not latched in until the next falling edge of CLK. For 1:2 Demux DDR 0° Mode, there are four CLK cycles of delay; for all other modes, there are three CLK cycles of delay.

If the device is not programmed to allow DCLK to run continuously, DCLK will become inactive during a calibration cycle. Therefore, it is strongly recommended that DCLK only be used as a data capture clock and not as a system clock.

The DCLK_RST pin should NOT be brought high while the calibration process is running (while CalRun is high). Doing so could cause a digital glitch in the digital circuitry, resulting in corruption and invalidation of the calibration.

ADC TEST PATTERN

To aid in system debug, the ADC08DL500 has the capability of providing a test pattern at the four output ports completely independent of the input signal. The ADC is disengaged and a test pattern generator is connected to the outputs including OR. Each port is given a unique 8-bit word, alternating between 1's and 0's as described in Table 16 and Table 17.

Table 16. Test Pattern by Output Port in 1:2 Demultiplex Mode

Time	Qd	Id	Q	I	OR	Comments
T0	01h	02h	03h	04h	0	Pattern Sequence n
T1	FEh	FDh	FCh	FBh	1	
T2	01h	02h	03h	04h	0	
T3	FEh	FDh	FCh	FBh	1	
T4	01h	02h	03h	04h	0	
T5	01h	02h	03h	04h	0	Pattern Sequence n+1
T6	FEh	FDh	FCh	FBh	1	
T7	01h	02h	03h	04h	0	
T8	FEh	FDh	FCh	FBh	1	
T9	01h	02h	03h	04h	0	
T10	01h	02h	03h	04h	0	Pattern Sequence n+2
T11	...	...	...	...	...	

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With the part programmed into the non-demultiplex mode, the test pattern's order will be as described in Table 17.

Table 17. Test Pattern by Output Port in Non-demultiplex Mode

Time	Q	I	OR	Comments
T0	01h	02h	0	Pattern Sequence n
T1	FEh	FDh	1	
T2	01h	02h	0	
T3	01h	02h	0	
T4	FEh	FDh	1	
T5	FEh	FDh	1	
T6	01h	02h	0	
T7	01h	02h	0	
T8	FEh	FDh	1	
T9	01h	02h	0	
T10	01h	02h	0	Pattern Sequence n+1
T11	FEh	FDh	1	
T12	01h	02h	0	
T13	01h	02h	0	
T14	FEh	FDh	1	
T15	...	...	...	

It is possible for the I and the Q channels' test patterns to be not synchronized. Either I and Id or Q and Qd patterns may be slipped by one DCLK.

To ensure that the test pattern starts synchronously in each port, set DCLK_RST while writing the Test Pattern Output bit in the Extended Configuration Register. The pattern appears at the data output ports when DCLK_RST is cleared low. The test pattern will work at speed and will work with the device in the SDR, DDR and the non-demultiplex output modes.

Applications Information

THE REFERENCE VOLTAGE

The voltage reference for the ADC08DL500 is derived from a 1.254V bandgap reference, a buffered version of which is made available at pin 33, V_{BG}, for user convenience.

This output has an output current capability of ±100 µA and should be buffered if more current than this is required.

There is no provision for the use of an external reference voltage, but the full-scale input voltage can be adjusted through a Configuration Register in the Extended Control mode, as explained in NORMAL/EXTENDED CONTROL.

Differential input signals up to the chosen full-scale level will be digitized to 8 bits. Signal excursions beyond the full-scale range will be clipped at the output. These large signal excursions will also activate the OR output for the time that the signal is out of range. See 2.2.2 Out Of Range (OR) Indication.

One extra feature of the V_{BG} pin is that it can be used to raise the common mode voltage level of the LVDS outputs. The output offset voltage (V_{OS}) is at its nominal value when the V_{BG} pin is used as an output or left unconnected. To raise the LVDS offset voltage, the V_{BG} pin can be connected directly to the supply rails.

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THE ANALOG INPUT

The analog input is a differential one to which the signal source may be a.c. coupled or d.c. coupled. In the normal mode, the full-scale input range is selected using the FSR pin as specified in the Converter Electrical Characteristics. In the Extended Control mode, the full-scale input range is selected by programming the Full-Scale Voltage Adjust register through the Serial Interface. For best performance when adjusting the input full-scale range in the Extended Control, refer to REGISTER DESCRIPTION for guidelines on limiting the amount of adjustment

Table 18 gives the input to output relationship with the FSR pin high when the normal (non-extended) mode is used. With the FSR pin grounded, the millivolt values in Table 18 are reduced to 75% of the values indicated. In the Enhanced Control Mode, these values will be determined by the full scale range and offset settings in the Control Registers.

Table 18. Differential Input To Output Relationship (Non-Extended Control Mode, FSR High)

V_{IN}+	V_{IN}−	Output Code
V_{CM} − 217.5 mV	V_{CM} + 217.5 mV	0000 0000
V_{CM} − 109 mV	V_{CM} + 109 mV	0100 0000
V_{CM}	V_{CM}	0111 1111 / 1000 0000
V_{CM} + 109 mV	V_{CM} − 109 mV	1100 0000
V_{CM} + 217.5 mV	V_{CM} − 217.5 mV	1111 1111

The buffered analog inputs simplify the task of driving these inputs and the RC pole that is generally used at sampling ADC inputs is not required. If it is desired to use an amplifier circuit before the ADC, use care in choosing an amplifier with adequate noise and distortion performance and adequate gain at the frequencies used for the application.

Note that a precise d.c. common mode voltage must be present at the ADC inputs. This common mode voltage, V_{CMO}, is provided on-chip when a.c. input coupling is used and the input signal is a.c. coupled to the ADC.

When the inputs are a.c. coupled, the V_{CMO} output *must* be grounded, as shown in Figure 11. This causes the on-chip V_{CMO} voltage to be connected to the inputs through on-chip 50 kΩ resistors.

IMPORTANT NOTE: An Analog input channel that is not used should be connected to ac-ground (ie, capacitors to ground) when the inputs are a.c. coupled. Do not connect an unused analog input directly to ground.

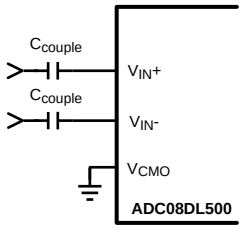


Figure 11. Differential Input Drive

When the d.c. coupled mode is used, a common mode voltage must be provided at the differential inputs. This common mode voltage should track the V_{CMO} output pin. Note that the V_{CMO} output potential will change with temperature. The common mode output of the driving device should track this change.

IMPORTANT NOTE: An analog input channel that is not used should be tied to the V_{CMO} voltage when the inputs are d.c. coupled. Do not connect unused analog inputs to ground.

Full-scale distortion performance falls off rapidly as the input common mode voltage deviates from V_{CMO}. This is a direct result of using a very low supply voltage to minimize power. Keep the input common voltage within 50 mV of V_{CMO}.

Performance is as good in the d.c. coupled mode as it is in the a.c. coupled mode, provided the input common mode voltage at both analog inputs remain within 50 mV of V_{CMO}.

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Handling Single-Ended Input Signals

There is no provision for the ADC08DL500 to adequately process single-ended input signals. The best way to handle single-ended signals is to convert them to differential signals before presenting them to the ADC. The easiest way to accomplish single-ended to differential signal conversion is with an appropriate balun-connected transformer, as shown in Figure 12.

a.c. Coupled Input

The easiest way to accomplish single-ended a.c. input to differential a.c. signal is by using an appropriate balun, as shown in Figure 12.

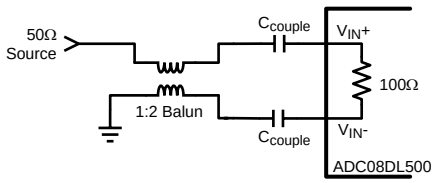


Figure 12. Single-Ended to Differential Signal Conversion Using a Balun

Figure 12 is a generic depiction of a single-ended to differential signal conversion using a balun. The circuitry specific to the balun will depend upon the type of balun selected and the overall board layout. It is recommended that the system designer contact the manufacturer of the balun they have selected to aid in designing the best performing single-ended to differential conversion circuit using that particular balun.

When selecting a balun, it is important to understand the input architecture of the ADC. There are specific balun parameters of which the system designer should be mindful. A designer should match the impedance of their analog source to the ADC08DL500's on-chip differential input termination resistor. The range of this termination resistor is described in the electrical table as the specification R_{IN}.

Also, the phase and amplitude balance are important. The lowest possible phase and amplitude imbalance is desired when selecting a balun. The phase imbalance should be no more than ±2.5° and the amplitude imbalance should be limited to less than 1dB at the desired input frequency range. Finally, when selecting a balun, the VSWR (Voltage Standing Wave Ratio), bandwidth and insertion loss of the balun should also be considered. The VSWR aids in determining the overall transmission line termination capability of the balun when interfacing to the ADC input. The insertion loss should be considered so that the signal at the balun output is within the specified input range of the ADC as described in the Converter Electrical Characteristics as the specification V_{IN}.

d.c. Coupled Input

When d.c. coupling to the ADC08DL500 analog inputs is required, single-ended to differential conversion may be easily accomplished with the LMH6555, as shown inFigure 13. In such applications, the LMH6555 performs the task of single-ended to differential conversion while delivering low distortion and noise, as well as output balance, that supports the operation of the ADC08DL500. Connecting the ADC08DL500 V_{CMO} pin to the V_{CM_REF} pin of the LMH6555, through an appropriate buffer, will ensure that the common mode input voltage is as needed for optimum performance of the ADC08DL500. The LMV321 was chosen to buffer V_{CMD} for its low voltage operation and reasonable offset voltage.

Be sure to limit output current from the ADC08DL500 V_{CMO} pin to 100 µA

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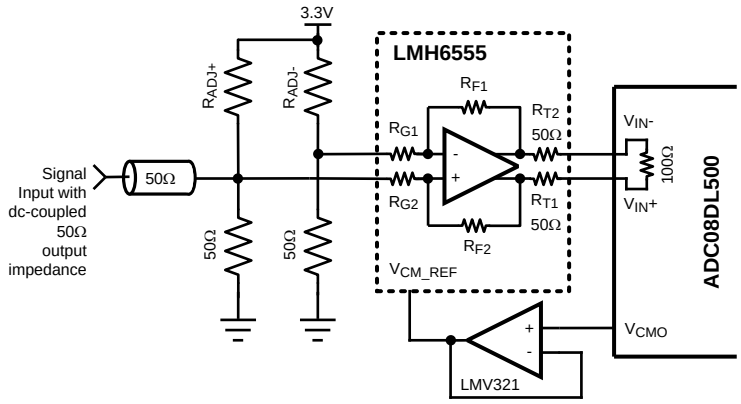


Figure 13. Example of Servoing the Analog Input with V_{CMO}

In Figure 13, R_{ADJ-} and R_{ADJ+} are used to adjust the differential offset that can be measured at the ADC inputs V_{IN+} / V_{IN-} with LMH6555's input terminated to ground as shown but not driven and with no R_{ADJ} resistors applied. An unadjusted positive offset with reference to V_{IN-} greater than |15mV| should be reduced with a resistor in the R_{ADJ-} position. Likewise, an unadjusted negative offset with reference to V_{IN-} greater than |15mV| should be reduced with a resistor in the R_{ADJ+} position. Table 19 gives suggested R_{ADJ-} and R_{ADJ+} values for various unadjusted differential offsets to bring the V_{IN+} / V_{IN-} offset back to within |15mV|.

Table 19. D.C. Coupled Offset Adjustment

Unadjusted Offset Reading	Resistor Value
0mV to 10mV	no resistor needed
11mV to 30mV	20.0kΩ
31mV to 50mV	10.0kΩ
51mV to 70mV	6.81kΩ
71mV to 90mV	4.75kΩ
91mV to 110mV	3.92kΩ

2.2.2 Out Of Range (OR) Indication

When the conversion result is clipped the Out of Range output is activated such that OR+ goes high and OR- goes low. This output is active as long as accurate data on either or both of the buses would be outside the range of 00h to FFh. Note that when the device is programmed to provide a second DCLK output, the OR signals become DCLK2. Refer to REGISTER DESCRIPTION

2.2.3 Full-Scale Input Range

As with all A/D Converters, the input range is determined by the value of the ADC's reference voltage. The reference voltage of the ADC08DL500 is derived from an internal band-gap reference. The FSR pin controls the effective reference voltage of the ADC08DL500 such that the differential full-scale input range at the analog inputs is a normal amplitude with the FSR pin high, or a reduced amplitude with FSR pin low as defined by the specification V_{IN} in the Converter Electrical Characteristics. Best SNR is obtained with FSR high, but better distortion and SFDR are obtained with the FSR pin low. The LMH6555 of is Figure 13 suitable for any Full Scale Range.

2.3 THE CLOCK INPUTS

The ADC08DL500 has differential LVDS clock inputs, CLK+ and CLK−, which must be driven with an a.c. coupled, differential clock signal. Although the ADC08DL500 is tested and its performance is guaranteed with a differential 1 GHz clock, it typically will function well with input clock frequencies indicated in the Converter Electrical Characteristics. The clock inputs are internally terminated and biased. The input clock signal must be capacitively coupled to the clock pins as indicated in Figure 14.

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Operation up to the sample rates indicated in the Converter Electrical Characteristics is typically possible if the maximum ambient temperatures indicated are not exceeded. Operating at higher sample rates than indicated for the given ambient temperature may result in reduced device reliability and product lifetime. This is because of the higher power consumption and die temperatures at high sample rates. Important also for reliability is proper thermal management . See Thermal Management.

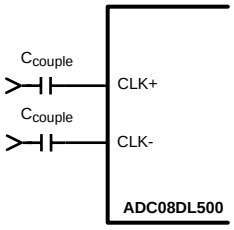


Figure 14. Differential (LVDS) Input Clock Connection

The differential input clock line pair should have a characteristic impedance of 100 Ω and (when using a balun), be terminated at the clock source in that (100 Ω) characteristic impedance. The input clock line should be as short and as direct as possible. The ADC08DL500 clock input is internally terminated with an untrimmed 100 Ω resistor.

Insufficient input clock levels will result in poor dynamic performance. Excessively high clock levels could cause a change in the analog input offset voltage. To avoid these problems, keep the clock level within the range specified as V_{ID} in the Converter Electrical Characteristics.

The low and high times of the input clock signal can affect the performance of any A/D Converter. The ADC08DL500 features a duty cycle clock correction circuit which can maintain performance over temperature. The ADC will meet its performance specification if the input clock high and low times are maintained within the duty cycle range as specified in the Converter Electrical Characteristics.

High speed, high performance ADCs such as the ADC08DL500 require a very stable input clock signal with minimum phase noise or jitter. ADC jitter requirements are defined by the ADC resolution (number of bits), maximum ADC input frequency and the input signal amplitude relative to the ADC input full scale range. The maximum jitter (the sum of the jitter from all sources) allowed to prevent a jitter-induced reduction in SNR is found to be

$$t_{J(MAX)} = (V_{INFSR} / V_{IN(P-P)}) \times (1/(2^{(N+1)} \times \pi \times f_{IN})) \quad (3)$$

where $t_{J(MAX)}$ is the rms total of all jitter sources in seconds, $V_{IN(P-P)}$ is the peak-to-peak analog input signal, V_{INFSR} is the full-scale range of the ADC, "N" is the ADC resolution in bits and f_{IN} is the maximum input frequency, in Hertz, at the ADC analog input.

Note that the maximum jitter described above is the RSS sum of the jitter from all sources, including that in the ADC input clock, that added by the system to the ADC input clock and input signals and that added by the ADC itself. Since the effective jitter added by the ADC is beyond user control, the best the user can do is to keep the sum of the externally added input clock jitter and the jitter added by the analog circuitry to the analog signal to a minimum.

Input clock amplitudes above those specified in the Converter Electrical Characteristics may result in increased input offset voltage. This would cause the converter to produce an output code other than the expected 127/128 when both input pins are at the same potential.

CONTROL PINS

Six control pins (without the use of the serial interface) provide a wide range of possibilities in the operation of the ADC08DL500 and facilitate its use. These control pins provide Full-Scale Input Range setting, Calibration, Calibration Delay, Output Edge Synchronization choice, LVDS Output Level choice and a Power Down feature.

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Full-Scale Input Range Setting

The input full-scale range can be selected with the FSR control input (pin 16) in the normal mode of operation. The input full-scale range is specified as V_{IN} in the Converter Electrical Characteristics. In the extended control mode, the input full-scale range may be programmed using the Full-Scale Adjust Voltage register. See THE ANALOG INPUT for more information.

Calibration

The ADC08DL500 calibration must be run to achieve specified performance. The calibration procedure is run upon power-up and can be run any time on command. The calibration procedure is exactly the same whether there is an input clock present upon power up or if the clock begins some time after application of power. The CalRun output indicator is high while a calibration is in progress. Note that the DCLK outputs are not active during a calibration cycle by default and therefore are not recommended as system clock unless the Resistor Trim Disable feature is used (Reg.9h). The DCLK outputs are continuously present at the output only when the Resistor Trim Disable is active.

Power-On Calibration

Power-on calibration begins after a time delay following the application of power. This time delay is determined by the setting of CalDly, as described in the Calibration Delay Section, below.

The calibration process will be not be performed if the CAL pin is high at power up. In this case, the calibration cycle will not begin until the on-command calibration conditions are met. The ADC08DL500 will function with the CAL pin held high at power up, but no calibration will be done and performance will be impaired. A manual calibration, however, may be performed after powering up with the CAL pin high. See On-Command Calibration On-Command Calibration.

The internal power-on calibration circuitry comes up in an unknown logic state. If the input clock is not running at power up and the power on calibration circuitry is active, it will hold the analog circuitry in power down and the power consumption will typically be less than 200 mW. The power consumption will be normal after the clock starts.

On-Command Calibration

To initiate an on-command calibration, bring the CAL pin high for a minimum of t_{CAL_H} input clock cycles after it has been low for a minimum of t_{CAL_L} input clock cycles. Holding the CAL pin high upon power up will prevent execution of power-on calibration until the CAL pin is low for a minimum of t_{CAL_L} input clock cycles, then brought high for a minimum of another t_{CAL_H} input clock cycles. The calibration cycle will begin t_{CAL_H} input clock cycles after the CAL pin is thus brought high. The CalRun signal should be monitored to determine when the calibration cycle has completed.

The minimum t_{CAL_L} and t_{CAL_H} input clock cycle sequence is required to ensure that random noise does not cause a calibration to begin when it is not desired. As mentioned for best performance, a calibration should be performed 20 seconds or more after power up and repeated when the operating temperature changes significantly relative to the specific system design performance requirements.

By default, On-Command calibration also includes calibrating the input termination resistance and the ADC. However, since the input termination resistance, once trimmed at power-up, changes marginally with temperature, the user has the option to disable the input termination resistor trim, which will guarantee that the DCLK is continuously present at the output during subsequent calibration. The Resistor Trim Disable can be programmed in register (address: 1h, bit 13) when in the Extended Control mode. Refer to REGISTER DESCRIPTION for register programming information.

Calibration Delay

The CalDly input (pin 141) is used to select one of two delay times after the application of power to the start of calibration, as described in Calibration. The calibration delay values allow the power supply to come up and stabilize before calibration takes place. With no delay or insufficient delay, calibration would begin before the power supply is stabilized at its operating value and result in non-optimal calibration coefficients. If the PD pin is high upon power-up, the calibration delay counter will be disabled until the PD pin is brought low. Therefore, holding the PD pin high during power up will further delay the start of the power-up calibration cycle. The best setting of the CalDly pin depends upon the power-on settling time of the power supply.

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Note that the calibration delay selection is not possible in the Extended Control mode and the short delay time is used.

Output Edge Synchronization

DCLK signals are available to help latch the converter output data into external circuitry. The output data can be synchronized with either edge of these DCLK signals. That is, the output data transition can be set to occur with either the rising edge or the falling edge of the DCLK signal, so that either edge of that DCLK signal can be used to latch the output data into the receiving circuit.

When OutEdge (pin 6) is high, the output data is synchronized with (changes with) the rising edge of the DCLK+ (pin 92). When OutEdge is low, the output data is synchronized with the falling edge of DCLK+.

At the very high speeds of which the ADC08DL500 is capable, slight differences in the lengths of the DCLK and data lines can mean the difference between successful and erroneous data capture. The OutEdge pin is used to capture data on the DCLK edge that best suits the application circuit and layout.

Reliable data capture can be achieved by using just one DCLK+/- signal for the full 32 signal data bus. However, if desired, the user may configure the OR+/- output as the second DCLK+/- output instead.

LVDS Output Level Control

The output level can be set to one of two levels with OutV (pin 5). The strength of the output drivers is greater with OutV high. With OutV low there is less power consumption in the output drivers, but the lower output level means decreased noise immunity.

For short LVDS lines and low noise systems, satisfactory performance may be realized with the OutV input low. If the LVDS lines are long and/or the system in which the ADC08DL500 is used is noisy, it may be necessary to tie the OutV pin high.

Power Down Feature

The Power Down pins (PD and PDQ) allow the ADC08DL500 to be entirely powered down (PD) or the "Q" channel to be powered down and the "I" channel to remain active. See Power Down for details on the power down feature.

The digital data (+/-) output pins are put into a high impedance state when the PD pin for the respective channel is high. Upon return to normal operation, the pipeline will contain meaningless information and must be flushed.

If the PD input is brought high while a calibration is running, the device will not go into power down until the calibration sequence is complete. However, if power is applied and PD is already high, the device will not begin the calibration sequence until the PD input goes low. If a manual calibration is requested while the device is powered down, the calibration will not begin at all. That is, the manual calibration input is completely ignored in the power down state.

THE DIGITAL OUTPUTS

The ADC08DL500 normally demultiplexes the output data of each of the two ADCs on the die onto two LVDS output buses (total of four buses, two for each ADC). For each of the two converters, the results of successive conversions started on the odd falling edges of the CLK+ pin are available on one of the two LVDS buses, while the results of conversions started on the even falling edges of the CLK+ pin are available on the other LVDS bus. This means that, the word rate at each LVDS bus is 1/2 the ADC08DL500 input clock rate and the two buses must be multiplexed to obtain the entire 1 GSPS conversion result.

Since the minimum recommended input clock rate for this device is 200 MSPS, the effective rate can be reduced to as low as 100 MSPS by using the results available on just one of the the two LVDS buses and a 200 MHz input clock, decimating the 200 MSPS data by two.

There is one LVDS output clock pair (DCLK+/−) available for use to latch the LVDS outputs on all buses. However, the user has the option to configure the OR+/- output as a second DCLK+/- pair. Whether the data is sent at the rising or falling edge of DCLK is determined by the sense of the OutEdge pin, as described in Output Edge Synchronization.

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DDR (Double Data Rate) clocking can also be used. In this mode a word of data is presented with each edge of DCLK, reducing the DCLK frequency to 1/4 the input clock frequency. See the Timing Diagram section for details.

The OutV pin is used to set the LVDS differential output levels. See LVDS Output Level Control.

The output format is Offset Binary. Accordingly, a full-scale input level with V_{IN}+ positive with respect to V_{IN}− will produce an output code of all ones, a full-scale input level with V_{IN}− positive with respect to V_{IN}+ will produce an output code of all zeros and when V_{IN}+ and V_{IN}− are equal, the output code will vary between codes 127 and 128. A non-multiplexed mode of operation is available for those cases where the digital ASIC is capable of higher speed operation.

POWER CONSIDERATIONS

A/D converters draw sufficient transient current to corrupt their own power supplies if not adequately bypassed. A 33 µF capacitor should be placed within an inch (2.5 cm) of the A/D converter power pins. A 0.1 µF capacitor should be placed as close as possible to each V_A pin, preferably within one-half centimeter. Leadless chip capacitors are preferred because they have low lead inductance.

The V_A and V_{DR} supply pins should be isolated from each other to prevent any digital noise from being coupled into the analog portions of the ADC. A ferrite choke, such as the JW Miller FB20009-3B, is recommended between these supply lines when a common source is used for them.

As is the case with all high speed converters, the ADC08DL500 should be assumed to have little power supply noise rejection. Any power supply used for digital circuitry in a system where a lot of digital power is being consumed should not be used to supply power to the ADC08DL500. The ADC supplies should be the same supply used for other analog circuitry, if not a dedicated supply.

Supply Voltage

The ADC08DL500 is specified to operate with a supply voltage of 1.9V ±0.1V. It is very important to note that, while this device will function with slightly higher supply voltages, these higher supply voltages may reduce product lifetime.

No pin should ever have a voltage on it that is in excess of the supply voltage or below ground by more than 150 mV, not even on a transient basis. This can be a problem upon application of power and power shut-down. Be sure that the supplies to circuits driving any of the input pins, analog or digital, do not come up any faster than does the voltage at the ADC08DL500 power pins.

The Absolute Maximum Ratings should be strictly observed, even during power up and power down. A power supply that produces a voltage spike at turn-on and/or turn-off of power can destroy the ADC08DL500. The circuit of Figure 15 will provide supply overshoot protection.

Many linear regulators will produce output spiking at power-on unless there is a minimum load provided. Active devices draw very little current until their supply voltages reach a few hundred millivolts. The result can be a turn-on spike that can destroy the ADC08DL500, unless a minimum load is provided for the supply. The 100 Ω resistor at the regulator output provides a minimum output current during power-up to ensure there is no turn-on spiking.

In the circuit of Figure 15, an LM317 linear regulator is satisfactory if its input supply voltage is 4V to 5V . If a 3.3V supply is used, an LM1086 linear regulator is recommended.

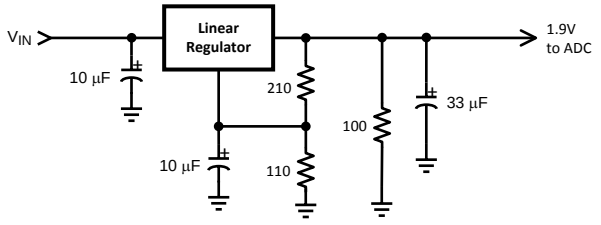


Figure 15. Non-Spiking Power Supply

The output drivers should have a supply voltage, V_{DR}, that is within the range specified in the Operating Ratings table. This voltage should not exceed the V_A supply voltage.

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If the power is applied to the device without an input clock signal present, the current drawn by the device might be below 200 mA. This is because the ADC08DL500 gets reset through clocked logic and its initial state is unknown. If the reset logic comes up in the "on" state, it will cause most of the analog circuitry to be powered down, resulting in less than 100 mA of current draw. This current is greater than the power down current because not all of the ADC is powered down. The device current will be normal after the input clock is established.

Thermal Management

The ADC08DL500 is capable of impressive speeds and performance at very low power levels for its speed. However, the power consumption is still high enough to require attention to thermal management. For reliability reasons, the die temperature should be kept to a maximum of 130°C. That is, T_A (ambient temperature) plus ADC power consumption times θ_{JA} (junction to ambient thermal resistance) should not exceed 130°C. This is not a problem if the ambient temperature is kept to a maximum of +70°C as specified in the Operating Ratings section.

To help minimize junction temperature, it is recommended that a simple heat sink be built into the PCB. This is done by including a copper area of about 2 square inches (6.5 square cm) on the opposite side of the PCB. This copper area may be plated or solder coated to prevent corrosion, but should not have a conformal coating, which could provide some thermal insulation. Thermal vias should be used to connect this bottom copper area to a copper pour on top of the PCB in the area underneath the ADC, where room allows. These thermal vias act as "heat pipes" to carry the thermal energy from the device side of the board to the opposite side of the board where it can be more effectively dissipated. The use of 9 to 16 thermal vias is recommended.

The thermal vias should be placed on a 1.2 mm grid spacing and have a diameter of 0.30 to 0.33 mm. Such voids could increase the thermal resistance between the device and the thermal land on the board, which would cause the device to run hotter.

LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. A single ground plane should be used, instead of splitting the ground plane into analog and digital areas.

Since digital switching transients are composed largely of high frequency components, the skin effect tells us that total ground plane copper weight will have little effect upon the logic-generated noise. Total surface area is more important than is total ground plane volume. Coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance that may seem impossible to isolate and remedy. The solution is to keep the analog circuitry well separated from the digital circuitry.

High power digital components should not be located on or near any linear component or power supply trace or plane that services analog or mixed signal components as the resulting common return current path could cause fluctuation in the analog input “ground” return of the ADC, causing excessive noise in the conversion result.

Generally, we assume that analog and digital lines should cross each other at 90° to avoid getting digital noise into the analog path. In high frequency systems, however, avoid crossing analog and digital lines altogether. The input clock lines should be isolated from ALL other lines, analog AND digital. The generally-accepted 90° crossing should be avoided as even a little coupling can cause problems at high frequencies. Best performance at high frequencies is obtained with a straight signal path.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. This is especially important with the low level drive required of the ADC08DL500. Any external component (e.g., a filter capacitor) connected between the converter's input and ground should be connected to a very clean point in the analog ground plane. All analog circuitry (input amplifiers, filters, etc.) should be separated from any digital components.

DYNAMIC PERFORMANCE

The ADC08DL500 is a.c. tested and its dynamic performance is guaranteed. To meet the published specifications and avoid jitter-induced noise, the clock source driving the CLK input must exhibit low rms jitter. The allowable jitter is a function of the input frequency and the input signal level, as described in 2.3 THE CLOCK INPUTS.

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It is good practice to keep the ADC input clock line as short as possible, to keep it well away from any other signals and to treat it as a transmission line. Other signals can introduce jitter into the input clock signal. The clock signal can also introduce noise into the analog path if not isolated from that path.

Best dynamic performance is obtained when the exposed pad at the back of the package has a good connection to ground. This is because this path from the die to ground is a lower impedance than offered by the package pins.

USING THE SERIAL INTERFACE

The ADC08DL500 may be operated in the non-extended control (non-Serial Interface) mode or in the extended control mode. Table 20 and Table 21 describe the functions of pins 5, 6, 16 and 141 in the non-extended control mode and the extended control mode, respectively.

Non-Extended Control Mode Operation

Non-extended control mode operation means that the Serial Interface is not active and all controllable functions are controlled with various pin settings. Pin 47 is the primary control of the extended control enable function. When pin 47 is logic high, the device is in the non-extended control mode. If pin 47 is floating and pin 58 is floating or logic high, the extended control enable function is controlled by pin 16. The device has functions which are pin programmable when in the non-extended control mode. An example is the full-scale range is controlled in the non-extended control mode by setting pin 16 high or low. Table 20 indicates the pin functions of the ADC08DL500 in the non-extended control mode.

Table 20. Non-Extended Control Mode Operation (Pin 47 Floating and Pin 58 Floating or Logic High)

Pin	Low	High	Floating
5	Reduced V_{OD}	Normal V_{OD}	n/a
6	OutEdge = Neg	OutEdge = Pos	DDR
141	CalDly Short	CalDly Long	n/a
16	Reduced V_{IN}	Normal V_{IN}	Extended Control Mode

Pin 5 can be either high or low in the non-extended control mode. See NORMAL/EXTENDED CONTROL for more information.

Pin 6 can be high or low or can be left floating in the non-extended control mode. In the non-extended control mode, pin 6 high or low defines the edge at which the output data transitions. See Output Edge Synchronization for more information. If this pin is floating, the output clock (DCLK) is a DDR (Double Data Rate) clock (see 1Single Data Rate and Double Data Rate) and the output edge synchronization is irrelevant since data is clocked out on both DCLK edges.

Pin 141, if it is high or low in the non-extended control mode, sets the calibration delay.

Table 21. Extended Control Mode Operation (Pin 47 Logic Low or Pin 16 Floating and Pin 58 Floating or Logic High)

Pin	Function
5	SCLK (Serial Clock)
6	SDATA (Serial Data)
141	$\overline{SCS}$ (Serial Interface Chip Select)

COMMON APPLICATION PITFALLS

Failure to write all register locations when using extended control mode. When using the serial interface, all nine address locations must be written at least once with the default or desired values before calibration and subsequent use of the ADC.

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Driving the inputs (analog or digital) beyond the power supply rails. For device reliability, no input should go more than 150 mV below the ground pins or 150 mV above the supply pins. Exceeding these limits on even a transient basis may not only cause faulty or erratic operation, but may impair device reliability. It is not uncommon for high speed digital circuits to exhibit undershoot that goes more than a volt below ground. Controlling the impedance of high speed lines and terminating these lines in their characteristic impedance should control overshoot.

Care should be taken not to overdrive the inputs of the ADC08DL500. Such practice may lead to conversion inaccuracies and even to device damage.

Incorrect analog input common mode voltage in the d.c. coupled mode. As discussed in The Analog Inputs and THE ANALOG INPUT, the Input common mode voltage must remain within 50 mV of the V_{CMO} output , which has a variability with temperature that must also be tracked. Distortion performance will be degraded if the input common mode voltage is more than 50 mV from V_{CMO} .

Using an inadequate amplifier to drive the analog input. Use care when choosing a high frequency amplifier to drive the ADC08DL500 as many high speed amplifiers will have higher distortion than will the ADC08DL500, resulting in overall system performance degradation.

Driving the V_{BG} pin to change the reference voltage. As mentioned in THE REFERENCE VOLTAGE, the reference voltage is intended to be fixed by FSR pin or Full-Scale Voltage Adjust register settings. Over driving this pin will not change the full scale value, but can otherwise upset operation.

Driving the clock input with an excessively high level signal. The ADC input clock level should not exceed the level described in the Operating Ratings Table or the input offset could change.

Inadequate input clock levels. As described in 2.3 THE CLOCK INPUTS, insufficient input clock levels can result in poor performance. Excessive input clock levels could result in the introduction of an input offset.

Using a clock source with excessive jitter, using an excessively long input clock signal trace, or having other signals coupled to the input clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR performance.

Failure to provide adequate heat removal. As described in Thermal Management, it is important to provide adequate heat removal to ensure device reliability. This can be done either with adequate air flow or the use of a simple heat sink built into the board.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC08DL500CIVV/NO.A	NRND	Production	LQFP (PGE) | 144	60 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 70	ADC08DL500CIVV
ADC08DL500CIVV/NOPB	NRND	Production	LQFP (PGE) | 144	60 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 70	ADC08DL500CIVV

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

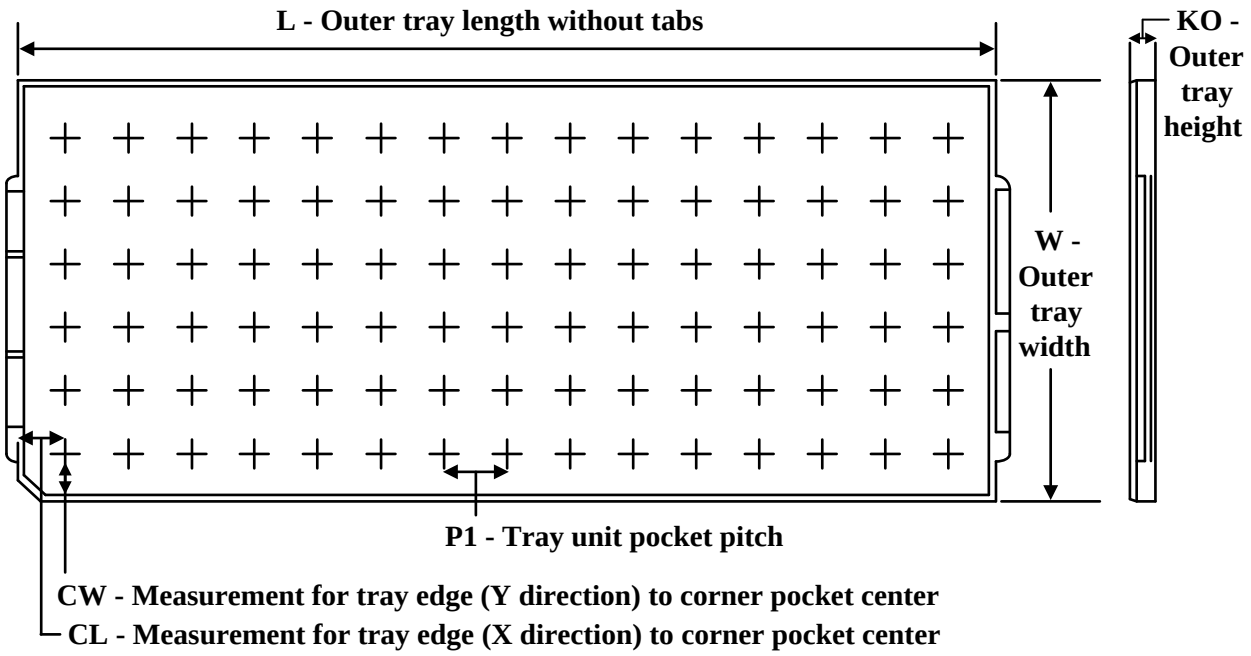
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TRAY



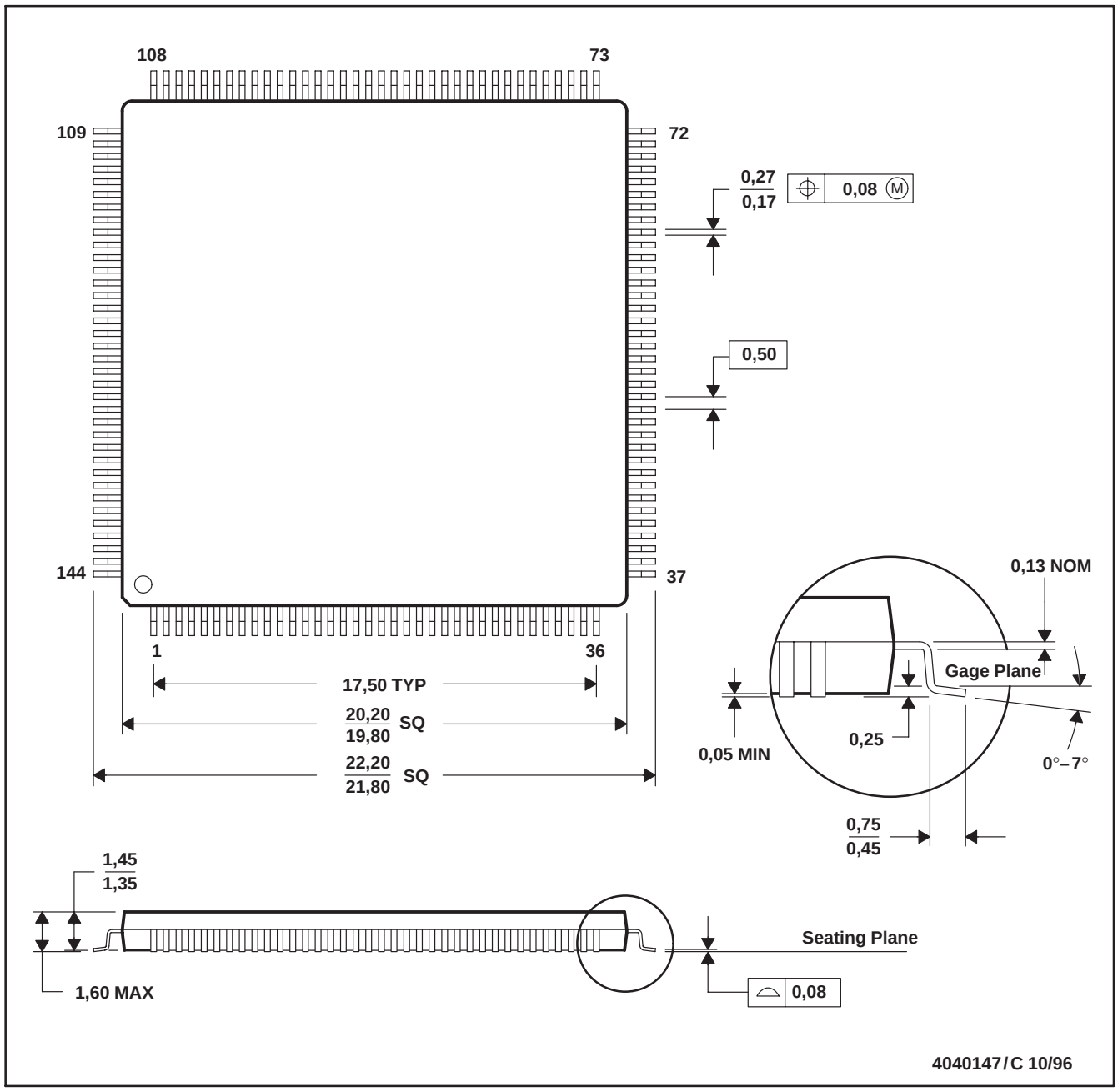
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADC08DL500CIVV/ NO.A	PGE	LQFP	144	60	5 X 12	150	322.6	135.9	7620	25.4	17.8	17.55
ADC08DL500CIVV/ NOPB	PGE	LQFP	144	60	5 X 12	150	322.6	135.9	7620	25.4	17.8	17.55

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PGE (S-PQFP-G144) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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