# ADC12C080 12-Bit, 65/80 MSPS A/D Converter

**Check for Samples: ADC12C080**

## FEATURES

- **1 GHz Full Power Bandwidth**
- **Internal Reference and Sample-and-Hold Circuit**
- **Low Power Consumption**
- **Data Ready Output Clock**
- **Clock Duty Cycle Stabilizer**
- **Single +3.0V Supply Operation**
- **Power-Down Mode**
- **32-Pin WQFN Package, (5x5x0.8mm, 0.5mm Pin-Pitch)**

## APPLICATIONS

- **High IF Sampling Receivers**
- **Wireless Base Station Receivers**
- **Test and Measurement Equipment**
- **Communications Instrumentation**
- **Portable Instrumentation**

## KEY SPECIFICATIONS

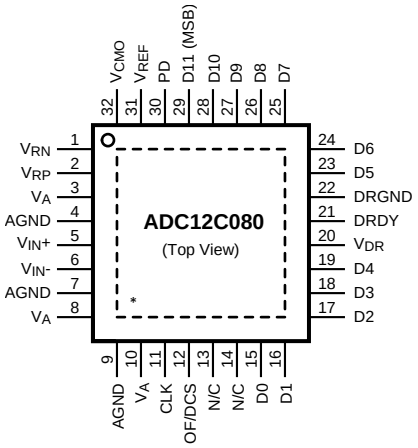
- **Resolution 12 Bits**
- **Conversion Rate 80 MSPS**
- **SNR ($f_{IN}$ = 170 MHz) 68 dBFS (typ)**
- **SFDR ($f_{IN}$ = 170 MHz) 86 dBFS (typ)**
- **Full Power Bandwidth 1 GHz (typ)**
- **Power Consumption 300 mW (typ)**

## DESCRIPTION

The ADC12C080 is a high-performance CMOS analog-to-digital converter capable of converting analog input signals into 12-bit digital words at rates up to 80 Mega Samples Per Second (MSPS). This converter uses a differential, pipelined architecture with digital error correction and an on-chip sample-and-hold circuit to minimize power consumption and the external component count, while providing excellent dynamic performance. A unique sample-and-hold stage yields a full-power bandwidth of 1 GHz. The ADC12C080 may be operated from a single +3.0V power supply and consumes low power. A separate +2.5V supply may be used for the digital output interface which allows lower power operation with reduced noise. A power-down feature reduces the power consumption to very low levels while still allowing fast wake-up time to full operation. The differential inputs accept a 2V full scale differential input swing. A stable 1.2V internal voltage reference is provided, or the ADC12C080 can be operated with an external 1.2V reference. Output data format (offset binary versus 2's complement) and duty cycle stabilizer are pin-selectable. The duty cycle stabilizer maintains performance over a wide range of clock duty cycles.

The ADC12C080 is available in a 32-lead WQFN package and operates over the industrial temperature range of −40°C to +85°C.

### Connection Diagram



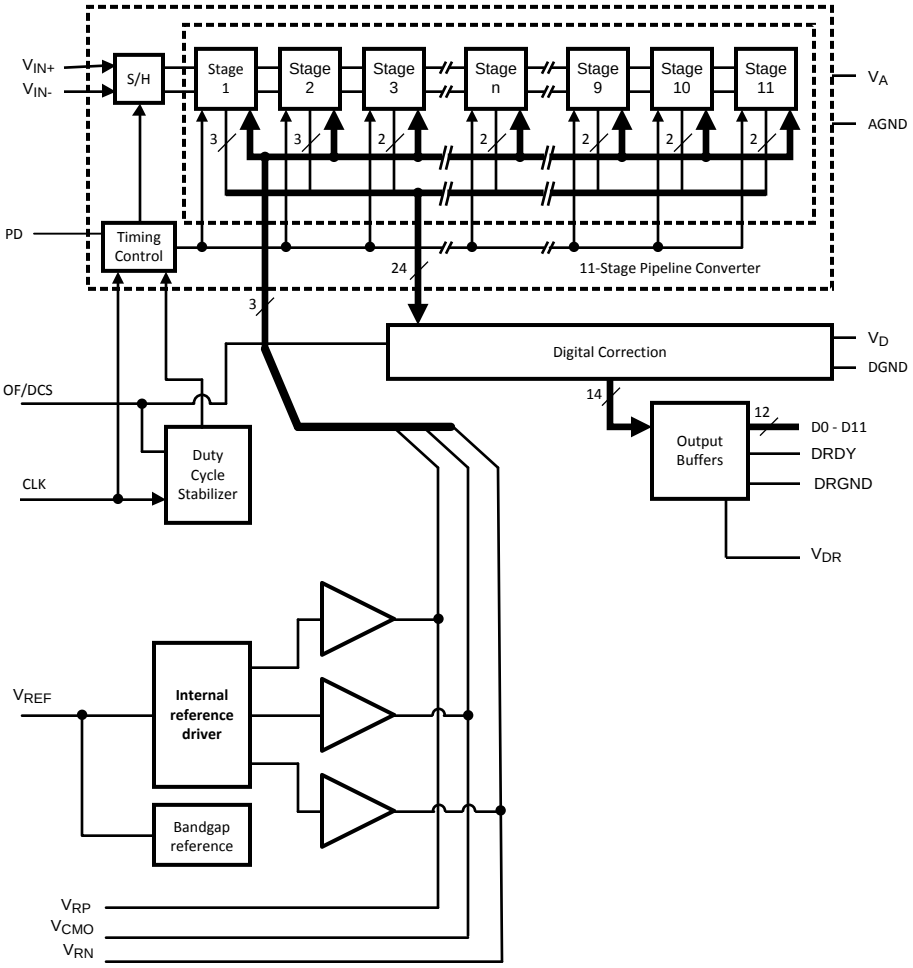

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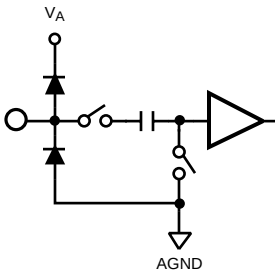
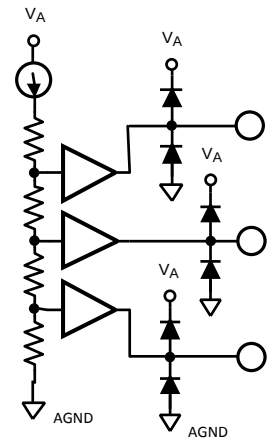
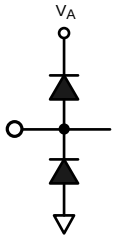
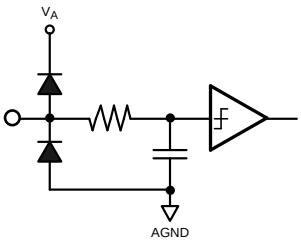
## Block Diagram



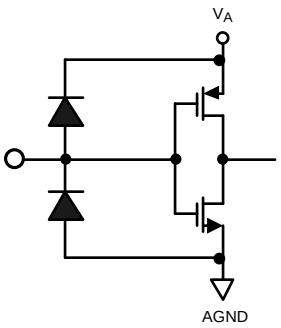
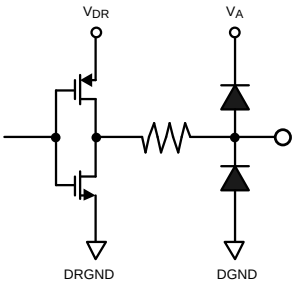


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## Pin Descriptions and Equivalent Circuits

| Pin No. | Symbol | Equivalent Circuit | Description |
|---|---|---|---|
| **ANALOG I/O** | | | |
| 5 | $V_{IN}$+ |  | Differential analog input pins. The differential full-scale input signal level is $2V_{P-P}$ with each input pin signal centered on a common mode voltage, $V_{CM}$. |
| 6 | $V_{IN}$- | | |
| 2 | $V_{RP}$ |  | These pins should each be bypassed to AGND with a low ESL (equivalent series inductance) 0.1 µF capacitor placed very close to the pin to minimize stray inductance. A 0.1 µF capacitor should be placed between $V_{RP}$ and $V_{RN}$ as close to the pins as possible, and a 1 µF capacitor should be placed in parallel.<br>$V_{RP}$ and $V_{RN}$ should not be loaded. $V_{CMO}$ may be loaded to 1mA for use as a temperature stable 1.5V reference.<br>It is recommended to use $V_{CMO}$ to provide the common mode voltage, $V_{CM}$, for the differential analog inputs, $V_{IN}$+ and $V_{IN}$−. |
| 32 | $V_{CMO}$ | | |
| 1 | $V_{RN}$ | | |
| 31 | $V_{REF}$ |  | Reference Voltage. This device provides an internally developed 1.2V reference. When using the internal reference, $V_{REF}$ should be decoupled to AGND with a 0.1 µFand a 1 µF low equivalent series inductance (ESL) capacitor.<br>This pin may be driven with an external 1.2V reference voltage.<br>This pin should not be used to source or sink current. |
| 12 | OF/DCS |  | This is a four-state pin controlling the input clock mode and output data format.<br>OF/DCS = $V_A$, output data format is 2's complement without duty cycle stabilization applied to the input clock<br>OF/DCS = AGND, output data format is offset binary, without duty cycle stabilization applied to the input clock.<br>OF/DCS = (2/3)*$V_A$, output data is 2's complement with duty cycle stabilization applied to the input clock<br>OF/DCS = (1/3)*$V_A$, output data is offset binary with duty cycle stabilization applied to the input clock. |

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| Pin No. | Symbol | Equivalent Circuit | Description |
|---|---|---|---|
| **DIGITAL I/O** | | | |
| 11 | CLK |  | The clock input pin.<br>The analog input is sampled on the rising edge of the clock input. |
| 30 | PD | | This is a two-state input controlling Power Down.<br>PD = $V_A$, Power Down is enabled and power dissipation is reduced.<br>PD = AGND, Normal operation. |
| 15-19, 23-29 | D0–D11 |  | Digital data output pins that make up the 12-bit conversion result. D0 (pin 15) is the LSB, while D11 (pin 29) is the MSB of the output word. Output levels are CMOS compatible. |
| 21 | DRDY | | Data Ready Strobe. The data output transition is synchronized with the falling edge of this signal. This signal switches at the same frequency as the CLK input. |
| **ANALOG POWER** | | | |
| 3, 8, 10 | $V_A$ | | Positive analog supply pins. These pins should be connected to a quiet voltage source and be bypassed to AGND with 0.1 µF capacitors located close to the power pins. |
| 4, 7, 9, Exposed Pad | AGND | | The ground return for the analog supply.<br>The exposed pad on back of package must be soldered to ground plane to ensure rated performance. |
| **DIGITAL POWER** | | | |
| 20 | $V_{DR}$ | | Positive driver supply pin for the output drivers. This pin should be connected to a quiet voltage source and be bypassed to DRGND with a 0.1 µF capacitor located close to the power pin. |
| 22 | DRGND | | The ground return for the digital output driver supply. This pins should be connected to the system digital ground, but not be connected in close proximity to the ADC's AGND pins. |



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.


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## Absolute Maximum Ratings (1) (2) (3)

| | | |
|---|---|---|
| Supply Voltage ($V_A$, $V_{DR}$) | | −0.3V to 4.2V |
| Voltage on Any Pin (Not to exceed 4.2V) | | −0.3V to ($V_A$ +0.3V) |
| Input Current at Any Pin other than Supply Pins (4) | | ±5 mA |
| Package Input Current (4) | | ±50 mA |
| Max Junction Temp ($T_J$) | | +150°C |
| Thermal Resistance ($\theta_{JA}$) (5) | | 30°C/W |
| ESD Rating | Human Body Model (6) | 2500V |
| | Machine Model (6) | 250V |
| Storage Temperature | | −65°C to +150°C |
| *Soldering process must comply with TI's Reflow Temperature Profile specifications. Refer to* www.ti.com/packaging. (7) | | |

(1) All voltages are measured with respect to GND = AGND = DRGND = 0V, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is specified to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(4) When the input voltage at any pin exceeds the power supplies (that is, $V_{IN}$ < AGND, or $V_{IN}$ > $V_A$), the current at that pin should be limited to ±5 mA. The ±50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of ±5 mA to 10.
(5) The maximum allowable power dissipation is dictated by $T_{J,max}$, the junction-to-ambient thermal resistance, ($\theta_{JA}$), and the ambient temperature, ($T_A$), and can be calculated using the formula $P_{D,max} = (T_{J,max} - T_A)/\theta_{JA}$. The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Such conditions should always be avoided.
(6) Human Body Model is 100 pF discharged through a 1.5 kΩ resistor. Machine Model is 220 pF discharged through 0 Ω
(7) Reflow temperature profiles are different for lead-free and non-lead-free packages.

## Operating Ratings (1) (2)

| | | |
|---|---|---|
| Operating Temperature | | −40°C ≤ $T_A$ ≤ +85°C |
| Supply Voltage ($V_A$) | | +2.7V to +3.6V |
| Output Driver Supply ($V_{DR}$) | | +2.4V to $V_A$ |
| Clock Duty Cycle | (DCS Enabled) | 30/70 % |
| | (DCS disabled) | 45/55 % |
| $V_{CM}$ | | 1.4V to 1.6V |
| \|AGND-DRGND\| | | ≤100mV |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is specified to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.
(2) All voltages are measured with respect to GND = AGND = DRGND = 0V, unless otherwise specified.

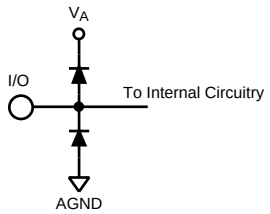
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## ADC12C080 Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, $V_A$ = +3.0V, $V_{DR}$ = +2.5V, Internal $V_{REF}$ = +1.2V, $f_{CLK}$ = 80 MHz, 50% Duty Cycle, DCS Disabled, $V_{CM}$ = $V_{CMO}$, $C_L$ = 5 pF/pin. Typical values are for $T_A$ = 25°C. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for $T_A$ = 25°C (1) (2)

| Symbol | Parameter | Conditions | | Typical (3) | Limits | Units (Limits) |
|---|---|---|---|---|---|---|
| **STATIC CONVERTER CHARACTERISTICS** | | | | | | |
| | Resolution with No Missing Codes | | | | **12** | Bits (min) |
| INL | Integral Non Linearity | | | ±0.5 | **1.2** | LSB (max) |
| | | | | | **-1.2** | LSB (min) |
| DNL | Differential Non Linearity | | | ±0.35 | **0.7** | LSB (max) |
| | | | | | **-0.6** | LSB (min) |
| PGE | Positive Gain Error | | | 0.25 | **±1.25** | %FS (max) |
| NGE | Negative Gain Error | | | 0.15 | **±1.25** | %FS (max) |
| TC PGE | Positive Gain Error Tempco | −40°C ≤ $T_A$ ≤ +85°C | | -7 | | ppm/°C |
| TC NGE | Negative Gain Error Tempco | −40°C ≤ $T_A$ ≤ +85°C | | -6 | | ppm/°C |
| $V_{OFF}$ | Offset Error | | | 0.065 | **±0.55** | %FS (max) |
| TC $V_{OFF}$ | Offset Error Tempco | −40°C ≤ $T_A$ ≤ +85°C | | 7.5 | | ppm/°C |
| | Under Range Output Code | | | 0 | **0** | |
| | Over Range Output Code | | | 4095 | **4095** | |
| **REFERENCE AND ANALOG INPUT CHARACTERISTICS** | | | | | | |
| $V_{CMO}$ | Common Mode Output Voltage | | | 1.5 | **1.40**<br>**1.56** | V (min)<br>V (max) |
| $V_{CM}$ | Analog Input Common Mode Voltage | | | 1.5 | 1.4<br>1.6 | V (min)<br>V (max) |
| $C_{IN}$ | $V_{IN}$ Input Capacitance (each pin to GND) (4) | $V_{IN}$ = 1.5 Vdc ± 0.5 V | (CLK LOW) | 8.5 | | pF |
| | | | (CLK HIGH) | 3.5 | | pF |
| $V_{REF}$ | Internal Reference Voltage | | | 1.18 | | V |
| TC $V_{REF}$ | Internal Reference Voltage Tempco | −40°C ≤ $T_A$ ≤ +85°C | | 18 | | ppm/°C |
| $V_{RP}$ | Internal Reference top | See (5) | | 1.98 | 1.89<br>2.06 | V (min)<br>V (max) |
| $V_{RN}$ | Internal Reference bottom | See (5) | | 0.98 | 0.89<br>1.06 | V (min)<br>V (max) |
| EXT $V_{REF}$ | External Reference Voltage | See (5) | | 1.20 | 1.176<br>1.224 | V (min)<br>V (max) |

(1) The inputs are protected as shown below. Input voltage magnitudes above $V_A$ or below GND will not damage this device, provided current is limited per Note 4 under Absolute Maximum Ratings. However, errors in the A/D conversion can occur if the input goes above 2.6V or below GND as described in the Operating Ratings section.




(2) With a full scale differential input of $2V_{P-P}$ , the 12-bit LSB is 488 µV.
(3) Typical figures are at $T_A$ = 25°C and represent most likely parametric norms at the time of product characterization. The typical specifications are not ensured.
(4) The input capacitance is the sum of the package/pin capacitance and the sample and hold circuit capacitance.
(5) This parameter is specified by design and/or characterization and is not tested in production.

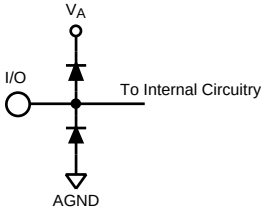

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## ADC12C080 Dynamic Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, $V_A$ = +3.0V, $V_{DR}$ = +2.5V, Internal $V_{REF}$ = +1.2V, $f_{CLK}$ = 80 MHz, 50% Duty Cycle, DCS Disabled, $V_{CM}$ = $V_{CMO}$, $C_L$ = 5 pF/pin, . Typical values are for $T_A$ = 25°C. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for $T_A$ = 25°C (1) (2)

| Symbol | Parameter | Conditions | Typical (3) | Limits | Units (Limits) (4) |
|---|---|---|---|---|---|
| **DYNAMIC CONVERTER CHARACTERISTICS, $A_{IN}$= -1dBFS** | | | | | |
| FPBW | Full Power Bandwidth | -1 dBFS Input, −3 dB Corner | 1.0 | | GHz |
| SNR | Signal-to-Noise Ratio | $f_{IN}$ = 10 MHz | 71.2 | | dBFS |
| | | $f_{IN}$ = 70 MHz | 70.5 | | dBFS |
| | | $f_{IN}$ = 170 MHz | 68.5 | **67.8** | dBFS |
| SFDR | Spurious Free Dynamic Range | $f_{IN}$ = 10 MHz | 90 | | dBFS |
| | | $f_{IN}$ = 70 MHz | 88 | | dBFS |
| | | $f_{IN}$ = 170 MHz | 86 | **82** | dBFS |
| ENOB | Effective Number of Bits | $f_{IN}$ = 10 MHz | 11.5 | | Bits |
| | | $f_{IN}$ = 70 MHz | 11.3 | | Bits |
| | | $f_{IN}$ = 170 MHz | 11.1 | **10.9** | Bits |
| THD | Total Harmonic Disortion | $f_{IN}$ = 10 MHz | −88 | | dBFS |
| | | $f_{IN}$ = 70 MHz | −86 | | dBFS |
| | | $f_{IN}$ = 170 MHz | −85 | **-80.5** | dBFS |
| H2 | Second Harmonic Distortion | $f_{IN}$ = 10 MHz | −95 | | dBFS |
| | | $f_{IN}$ = 70 MHz | −90 | | dBFS |
| | | $f_{IN}$ = 170 MHz | −86 | **-82** | dBFS |
| H3 | Third Harmonic Distortion | $f_{IN}$ = 10 MHz | −90 | | dBFS |
| | | $f_{IN}$ = 70 MHz | −88 | | dBFS |
| | | $f_{IN}$ = 170 MHz | −86 | **-82** | dBFS |
| SINAD | Signal-to-Noise and Distortion Ratio | $f_{IN}$ = 10 MHz | 71.1 | | dBFS |
| | | $f_{IN}$ = 70 MHz | 70 | | dBFS |
| | | $f_{IN}$ = 170 MHz | 68.5 | **67.6** | dBFS |
| IMD | Intermodulation Distortion | $f_{IN}$ = 19.5MHz and 20.5MHz, each -7dBFS | -82 | | dBFS |

(1) The inputs are protected as shown below. Input voltage magnitudes above $V_A$ or below GND will not damage this device, provided current is limited per Note 4 under Absolute Maximum Ratings. However, errors in the A/D conversion can occur if the input goes above 2.6V or below GND as described in the Operating Ratings section.




(2) With a full scale differential input of $2V_{P-P}$ , the 12-bit LSB is 488 µV.
(3) Typical figures are at $T_A$ = 25°C and represent most likely parametric norms at the time of product characterization. The typical specifications are not ensured.
(4) Parameters specified in dBFS indicate the value that would be attained with a full-scale input signal.

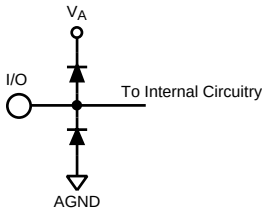
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## ADC12C080 Logic and Power Supply Electrical Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, $V_A$ = +3.0V, $V_{DR}$ = +2.5V, Internal $V_{REF}$ = +1.2V, $f_{CLK}$ = 80 MHz, 50% Duty Cycle, DCS Disabled, $V_{CM}$ = $V_{CMO}$, $C_L$ = 5 pF/pin. Typical values are for $T_A$ = 25°C. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for $T_A$ = 25°C (1) (2)

| Symbol | Parameter | Conditions | Typical (3) | Limits | Units (Limits) |
|---|---|---|---|---|---|
| **DIGITAL INPUT CHARACTERISTICS (CLK, PD)** | | | | | |
| $V_{IN(1)}$ | Logical “1” Input Voltage | $V_D$ = 3.6V | | **2.0** | V (min) |
| $V_{IN(0)}$ | Logical “0” Input Voltage | $V_D$ = 3.0V | | **0.8** | V (max) |
| $I_{IN(1)}$ | Logical “1” Input Current | $V_{IN}$ = 3.3V | 10 | | µA |
| $I_{IN(0)}$ | Logical “0” Input Current | $V_{IN}$ = 0V | −10 | | µA |
| $C_{IN}$ | Digital Input Capacitance | | 5 | | pF |
| **DIGITAL OUTPUT CHARACTERISTICS (D0–D11, DRDY)** | | | | | |
| $V_{OUT(1)(1)}$ | Logical “1” Output Voltage | $I_{OUT}$ = −0.5 mA , $V_{DR}$ = 2.4V | | **2.0** | V (min) |
| $V_{OUT(0)(0)}$ | Logical “0” Output Voltage | $I_{OUT}$ = 1.6 mA, $V_{DR}$ = 2.4V | | **0.4** | V (max) |
| $+I_{SC}$ | Output Short Circuit Source Current | $V_{OUT}$ = 0V | −10 | | mA |
| $-I_{SC}$ | Output Short Circuit Sink Current | $V_{OUT}$ = $V_{DR}$ | 10 | | mA |
| $C_{OUT}$ | Digital Output Capacitance | | 5 | | pF |
| **POWER SUPPLY CHARACTERISTICS** | | | | | |
| $I_A$ | Analog Supply Current | Full Operation | 100 | **123** | mA (max) |
| $I_{DR}$ | Digital Output Supply Current | Full Operation (4) | 12 | | mA |
| | Power Consumption | Excludes $I_{DR}$ (4) | 300 | **369** | mW (max) |
| | Power Down Power Consumption | Clock disabled | 7 | | mW |

(1) The inputs are protected as shown below. Input voltage magnitudes above $V_A$ or below GND will not damage this device, provided current is limited per Note 4 under Absolute Maximum Ratings. However, errors in the A/D conversion can occur if the input goes above 2.6V or below GND as described in the Operating Ratings section.




(2) With a full scale differential input of $2V_{P-P}$ , the 12-bit LSB is 488 µV.

(3) Typical figures are at $T_A$ = 25°C and represent most likely parametric norms at the time of product characterization. The typical specifications are not ensured.

(4) $I_{DR}$ is the current consumed by the switching of the output drivers and is primarily determined by load capacitance on the output pins, the supply voltage, $V_{DR}$, and the rate at which the outputs are switching (which is signal dependent). $I_{DR}=V_{DR}(C_0 \times f_0 + C_1 \times f_1 + ....C_{11} \times f_{11})$ where $V_{DR}$ is the output driver power supply voltage, $C_n$ is total capacitance on the output pin, and $f_n$ is the average frequency at which that pin is toggling.

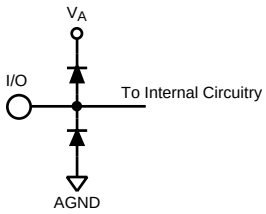

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## ADC12C080 Timing and AC Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, $V_A$ = +3.0V, $V_{DR}$ = +2.5V, Internal $V_{REF}$ = +1.2V, $f_{CLK}$ = 80 MHz, 50% Duty Cycle, DCS Disabled, $V_{CM}$ = $V_{CMO}$, $C_L$ = 5 pF/pin. Typical values are for $T_A$ = 25°C. Timing measurements are taken at 50% of the signal amplitude. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for $T_A$ = 25°C (1) (2)

| Symb | Parameter | Conditions | Typical (3) | Limits | Units (Limits) |
|---|---|---|---|---|---|
| | Maximum Clock Frequency | | | **80** | MHz (max) |
| | Minimum Clock Frequency | | | **20** | MHz (min) |
| $t_{CH}$ | Clock High Time | | 6 | | ns |
| $t_{CL}$ | Clock Low Time | | 6 | | ns |
| $t_{CONV}$ | Conversion Latency | | | **7** | Clock Cycles |
| $t_{OD}$ | Output Delay of CLK to DATA | Relative to rising edge of CLK (4) | 5.5 | 3<br>7.3 | ns (min)<br>ns(max) |
| $t_{SU}$ | Data Output Setup Time | Relative to DRDY | 6.5 | **5.5** | ns (min) |
| $t_H$ | Data Output Hold Time | Relative to DRDY | 6 | **5** | ns (min) |
| $t_{AD}$ | Aperture Delay | | 0.6 | | ns |
| $t_{AJ}$ | Aperture Jitter | | 0.1 | | ps rms |

(1) The inputs are protected as shown below. Input voltage magnitudes above $V_A$ or below GND will not damage this device, provided current is limited per Note 4 under Absolute Maximum Ratings. However, errors in the A/D conversion can occur if the input goes above 2.6V or below GND as described in the Operating Ratings section.




(2) With a full scale differential input of $2V_{P-P}$ , the 12-bit LSB is 488 µV.
(3) Typical figures are at $T_A$ = 25°C and represent most likely parametric norms at the time of product characterization. The typical specifications are not ensured.
(4) This parameter is specified by design and/or characterization and is not tested in production.

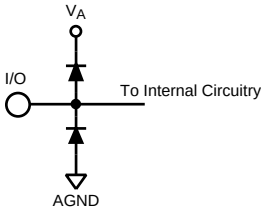
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## Dynamic Converter Electrical Characteristics at 65MSPS

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, $V_A$ = +3.0V, $V_{DR}$ = +2.5V, Internal $V_{REF}$ = +1.2V, $f_{CLK}$ = 65 MHz, 50% Duty Cycle, DCS Disabled, $V_{CM}$ = $V_{CMO}$, $C_L$ = 5 pF/pin, . Typical values are for $T_A$ = 25°C. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for $T_A$ = 25°C (1) (2)

| Symbol | Parameter | Conditions | Typical (3) | Limits | Units (Limits) (4) |
|---|---|---|---|---|---|
| **DYNAMIC CONVERTER CHARACTERISTICS, $A_{IN}$= -1dBFS** | | | | | |
| SNR | Signal-to-Noise Ratio | $f_{IN}$ = 10 MHz | 71.2 | | dBFS |
| | | $f_{IN}$ = 70 MHz | 70.5 | | dBFS |
| | | $f_{IN}$ =170 MHz | 68.5 | | dBFS |
| SFDR | Spurious Free Dynamic Range | $f_{IN}$ = 10 MHz | 90 | | dBFS |
| | | $f_{IN}$ = 70 MHz | 88 | | dBFS |
| | | $f_{IN}$ = 170 MHz | 86 | | dBFS |
| ENOB | Effective Number of Bits | $f_{IN}$ = 10 MHz | 11.5 | | Bits |
| | | $f_{IN}$ = 70 MHz | 11.3 | | Bits |
| | | $f_{IN}$ = 170 MHz | 11 | | Bits |
| THD | Total Harmonic Disortion | $f_{IN}$ = 10 MHz | −88 | | dBFS |
| | | $f_{IN}$ = 70 MHz | −85 | | dBFS |
| | | $f_{IN}$ = 170 MHz | −80 | | dBFS |
| H2 | Second Harmonic Distortion | $f_{IN}$ = 10 MHz | -100 | | dBFS |
| | | $f_{IN}$ = 70 MHz | −95 | | dBFS |
| | | $f_{IN}$ = 170 MHz | −85 | | dBFS |
| H3 | Third Harmonic Distortion | $f_{IN}$ = 10 MHz | −90 | | dBFS |
| | | $f_{IN}$ = 70 MHz | −88 | | dBFS |
| | | $f_{IN}$ = 170 MHz | −83 | | dBFS |
| SINAD | Signal-to-Noise and Distortion Ratio | $f_{IN}$ = 10 MHz | 71.1 | | dBFS |
| | | $f_{IN}$ = 70 MHz | 69.8 | | dBFS |
| | | $f_{IN}$ = 170 MHz | 67.7 | | dBFS |
| **POWER SUPPLY CHARACTERISTICS** | | | | | |
| $I_A$ | Analog Supply Current | Full Operation | 90 | | mA (max) |
| $I_{DR}$ | Digital Output Supply Current | Full Operation (5) | 14.5 | | mA |
| | Power Consumption | Excludes $I_{DR}$ (5) | 270 | | mW (max) |

(1) The inputs are protected as shown below. Input voltage magnitudes above $V_A$ or below GND will not damage this device, provided current is limited per Note 4 under Absolute Maximum Ratings. However, errors in the A/D conversion can occur if the input goes above 2.6V or below GND as described in the Operating Ratings section.




(2) With a full scale differential input of $2V_{P-P}$ , the 12-bit LSB is 488 µV.
(3) Typical figures are at $T_A$ = 25°C and represent most likely parametric norms at the time of product characterization. The typical specifications are not ensured.
(4) Parameters specified in dBFS indicate the value that would be attained with a full-scale input signal.
(5) $I_{DR}$ is the current consumed by the switching of the output drivers and is primarily determined by load capacitance on the output pins, the supply voltage, $V_{DR}$, and the rate at which the outputs are switching (which is signal dependent). $I_{DR}=V_{DR}(C_0 \times f_0 + C_1 \times f_1 + ....C_{11} \times f_{11})$ where $V_{DR}$ is the output driver power supply voltage, $C_n$ is total capacitance on the output pin, and $f_n$ is the average frequency at which that pin is toggling.


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## Specification Definitions

**APERTURE DELAY** is the time after the falling edge of the clock to when the input signal is acquired or held for conversion.

**APERTURE JITTER (APERTURE UNCERTAINTY)** is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

**CLOCK DUTY CYCLE** is the ratio of the time during one cycle that a repetitive digital waveform is high to the total time of one period. The specification here refers to the ADC clock input signal.

**COMMON MODE VOLTAGE ($V_{CM}$)** is the common DC voltage applied to both input terminals of the ADC.

**CONVERSION LATENCY** is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. Data for any given sample is available at the output pins the Pipeline Delay plus the Output Delay after the sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

**DIFFERENTIAL NON-LINEARITY (DNL)** is the measure of the maximum deviation from the ideal step size of 1 LSB.

**EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS)** is another method of specifying Signal-to-Noise and Distortion Ratio or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

**FULL POWER BANDWIDTH** is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

**GAIN ERROR** is the deviation from the ideal slope of the transfer function. It can be calculated as:

Gain Error = Positive Full Scale Error − Negative Full Scale Error (1)

It can also be expressed as Positive Gain Error and Negative Gain Error, which are calculated as:

PGE = Positive Full Scale Error - Offset Error NGE = Offset Error - Negative Full Scale Error (2)

**INTEGRAL NON LINEARITY (INL)** is a measure of the deviation of each individual code from a best fit straight line. The deviation of any given code from this straight line is measured from the center of that code value.

**INTERMODULATION DISTORTION (IMD)** is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the intermodulation products to the total power in the original frequencies. IMD is usually expressed in dBFS.

**LSB (LEAST SIGNIFICANT BIT)** is the bit that has the smallest value or weight of all bits. This value is $V_{FS}/2^n$, where "$V_{FS}$" is the full scale input voltage and "n" is the ADC resolution in bits.

**MISSING CODES** are those output codes that will never appear at the ADC outputs. The ADC is ensured not to have any missing codes.

**MSB (MOST SIGNIFICANT BIT)** is the bit that has the largest value or weight. Its value is one half of full scale.

**NEGATIVE FULL SCALE ERROR** is the difference between the actual first code transition and its ideal value of ½ LSB above negative full scale.

**OFFSET ERROR** is the difference between the two input voltages [($V_{IN}$+) – ($V_{IN}$-)] required to cause a transition from code 2047 to 2048.

**OUTPUT DELAY** is the time delay after the falling edge of the clock before the data update is presented at the output pins.

**PIPELINE DELAY (LATENCY)** See CONVERSION LATENCY.

**POSITIVE FULL SCALE ERROR** is the difference between the actual last code transition and its ideal value of 1½ LSB below positive full scale.

**POWER SUPPLY REJECTION RATIO (PSRR)** is a measure of how well the ADC rejects a change in the power supply voltage. PSRR is the ratio of the Full-Scale output of the ADC with the supply at the minimum DC supply limit to the Full-Scale output of the ADC with the supply at the maximum DC supply limit, expressed in dB.

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**SIGNAL TO NOISE RATIO (SNR)** is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or DC.

**SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD)** Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

**SPURIOUS FREE DYNAMIC RANGE (SFDR)** is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

**TOTAL HARMONIC DISTORTION (THD)** is the ratio, expressed in dB, of the rms total of the first six harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$THD = 20 \times \log \sqrt{\frac{f_2^2 + \ldots + f_7^2}{f_1^2}} \tag{3}$$

where $f_1$ is the RMS power of the fundamental (output) frequency and $f_2$ through $f_7$ are the RMS power of the first six harmonic frequencies in the output spectrum.

**SECOND HARMONIC DISTORTION (2ND HARM)** is the difference expressed in dB, between the RMS power in the input frequency at the output and the power in its 2nd harmonic level at the output.

**THIRD HARMONIC DISTORTION (3RD HARM)** is the difference, expressed in dB, between the RMS power in the input frequency at the output and the power in its 3rd harmonic level at the output.

## Timing Diagram

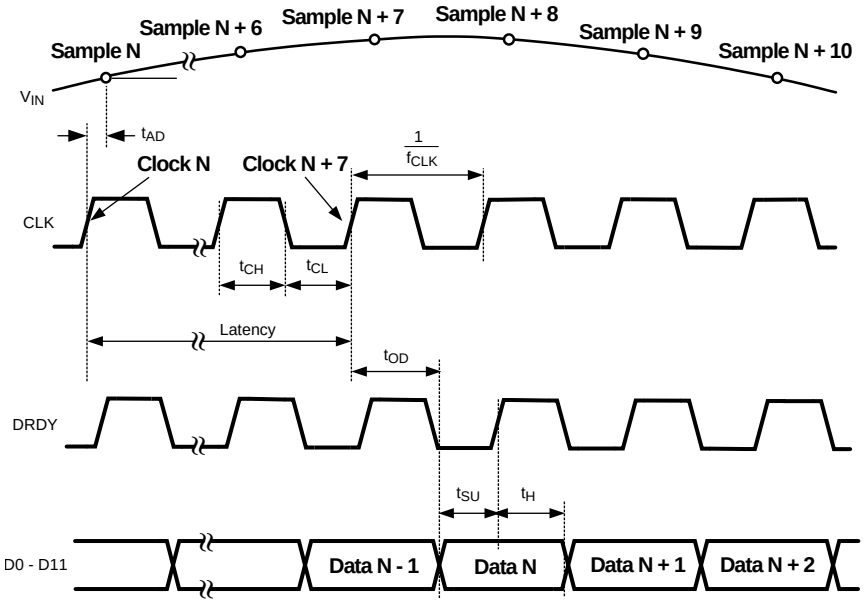



**Figure 1. Output Timing**


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## Transfer Characteristic

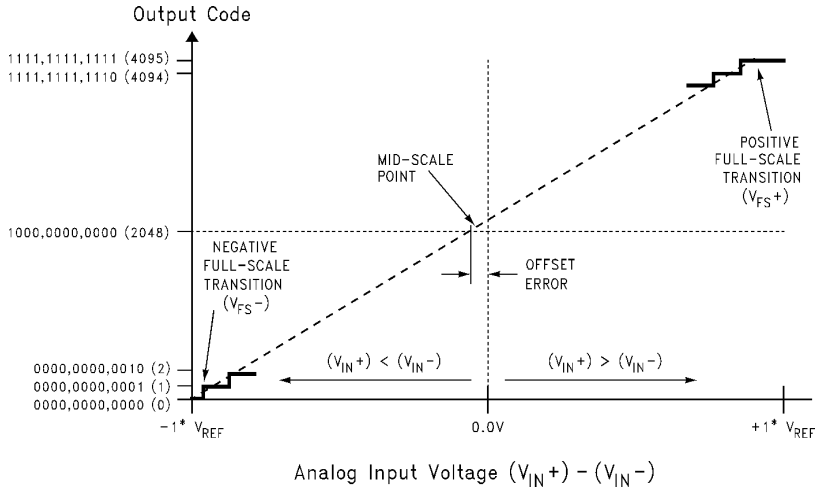



**Figure 2. Transfer Characteristic**

## Typical Performance Characteristics DNL, INL

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, $V_A$ = +3.0V, $V_{DR}$ = +2.5V, Internal $V_{REF}$ = +1.2V, $f_{CLK}$ = 80 MHz, 50% Duty Cycle, DCS disabled, $V_{CM}$ = $V_{CMO}$, $C_L$ = 5 pF/pin. $T_A$ = 25°C.

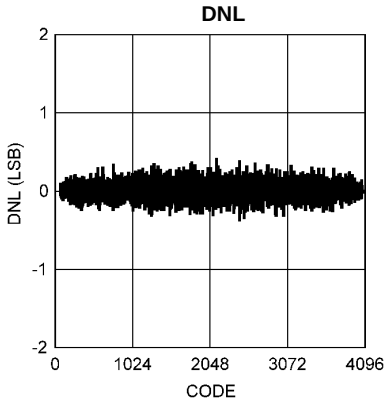



**Figure 3.**

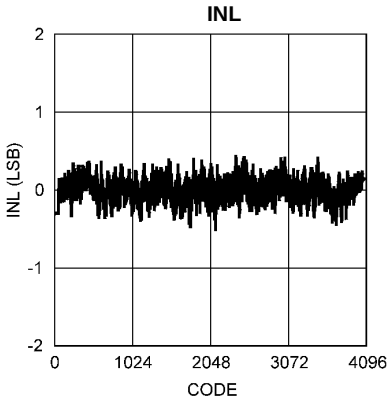



**Figure 4.**

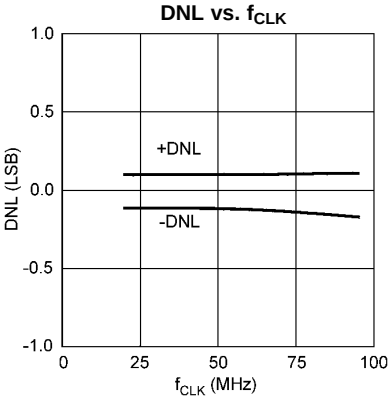



**Figure 5.**

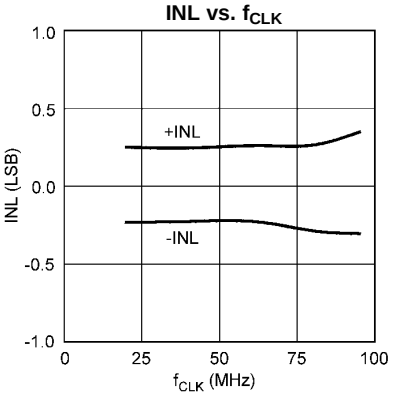



**Figure 6.**

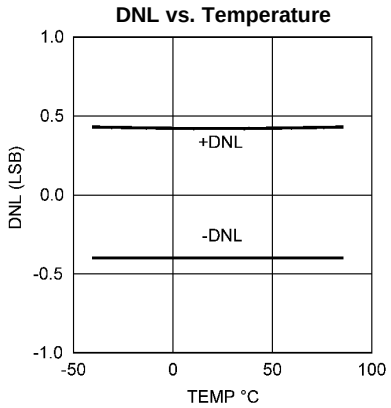



**Figure 7.**

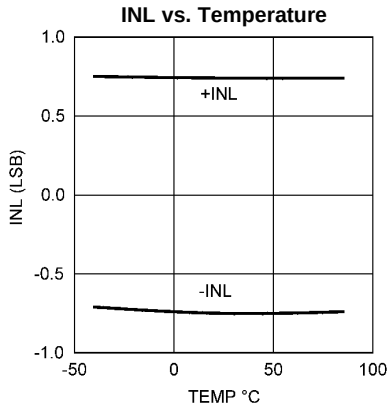



**Figure 8.**


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## Typical Performance Characteristics DNL, INL (continued)

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, $V_A$ = +3.0V, $V_{DR}$ = +2.5V, Internal $V_{REF}$ = +1.2V, $f_{CLK}$ = 80 MHz, 50% Duty Cycle, DCS disabled, $V_{CM}$ = $V_{CMO}$, $C_L$ = 5 pF/pin. $T_A$ = 25°C.

**DNL vs. $V_A$**

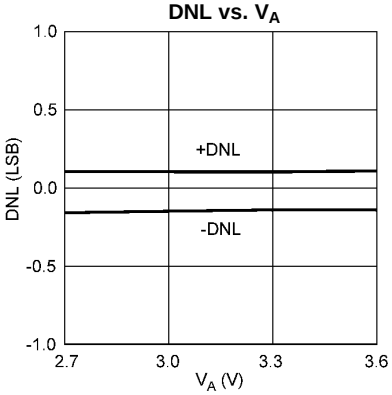



**Figure 9.**

**INL vs. $V_A$**

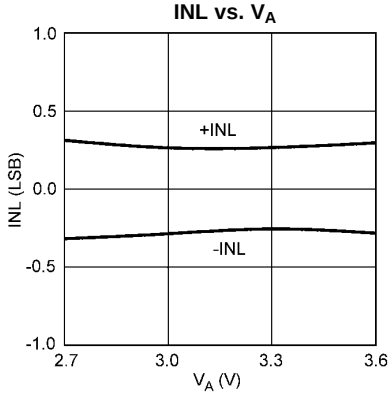



**Figure 10.**

## Typical Performance Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, $V_A$ = +3.0V, $V_{DR}$ = +2.5V, Internal $V_{REF}$ = +1.2V, $f_{CLK}$ = 80 MHz, 50% Duty Cycle, DCS disabled, $V_{CM}$ = $V_{CMO}$, $f_{IN}$ = 10 MHz, $C_L$ = 5 pF/pin. $T_A$ = 25°C.

**SNR, SINAD, SFDR vs. $V_A$**

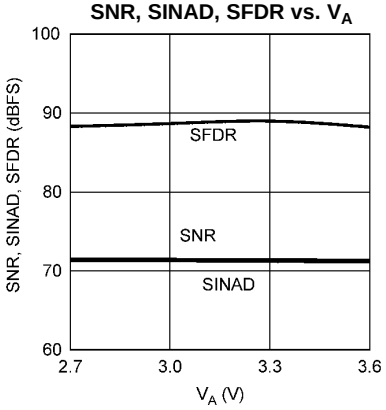



**Figure 11.**

**Distortion vs. $V_A$**

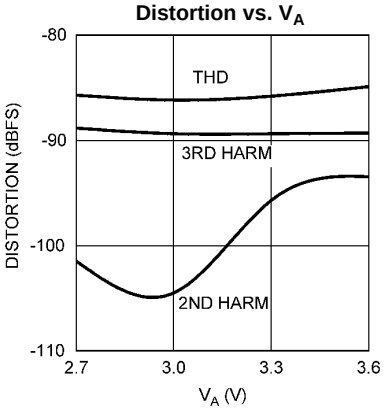



**Figure 12.**

**SNR, SINAD, SFDR vs. $V_{DR}$**

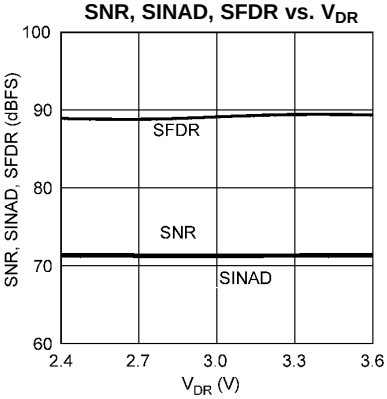



**Figure 13.**

**Distortion vs. $V_{DR}$**

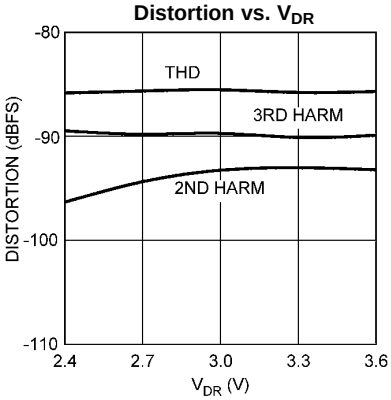



**Figure 14.**

**SNR, SINAD, SFDR vs. $f_{CLK}$**

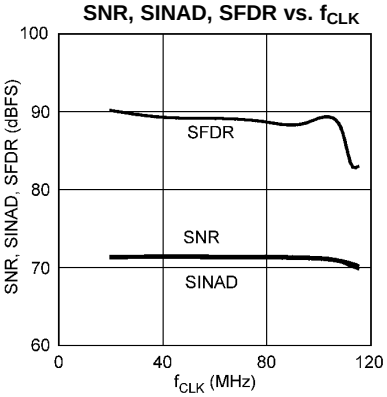



**Figure 15.**

**Distortion vs. $f_{CLK}$**

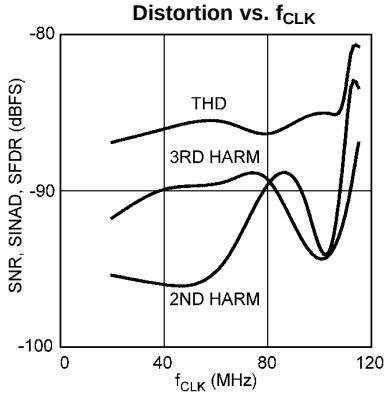



**Figure 16.**


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## Typical Performance Characteristics (continued)

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, $V_A$ = +3.0V, $V_{DR}$ = +2.5V, Internal $V_{REF}$ = +1.2V, $f_{CLK}$ = 80 MHz, 50% Duty Cycle, DCS disabled, $V_{CM}$ = $V_{CMO}$, $f_{IN}$ = 10 MHz, $C_L$ = 5 pF/pin. $T_A$ = 25°C.

**SNR, SINAD, SFDR vs. Clock Duty Cycle**

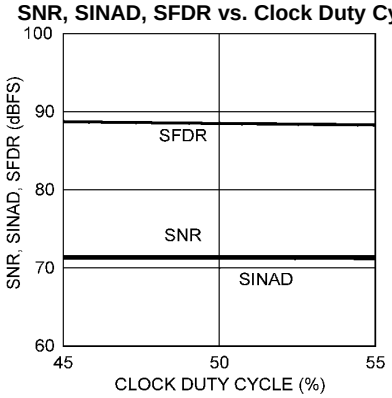



**Figure 17.**

**Distortion vs. Clock Duty Cycle**

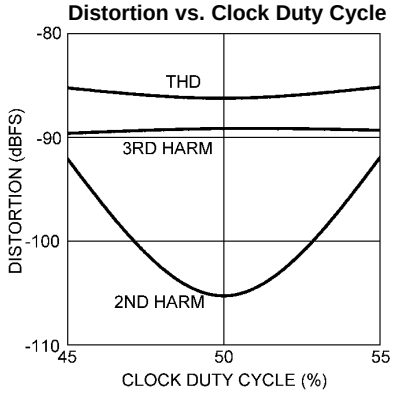



**Figure 18.**

**SNR, SINAD, SFDR vs. Clock Duty Cycle, DCS Enabled**

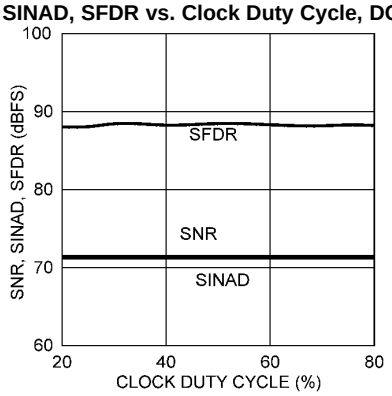



**Figure 19.**

**Distortion vs. Clock Duty Cycle, DCS Enabled**

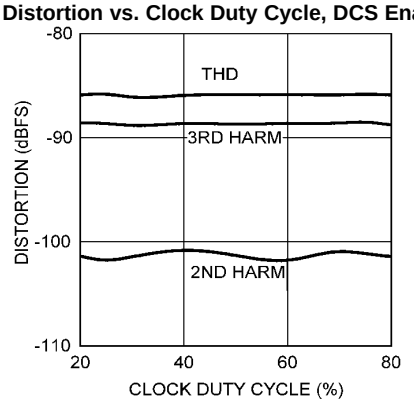



**Figure 20.**

**SNR, SINAD, SFDR vs. $f_{IN}$**

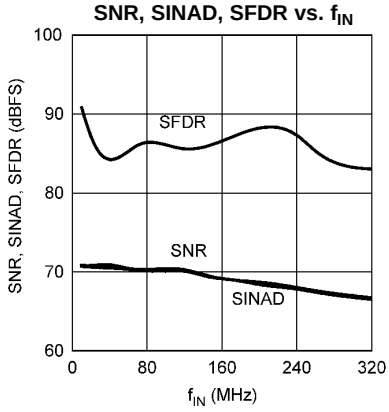



**Figure 21.**

**Distortion vs. $f_{IN}$**

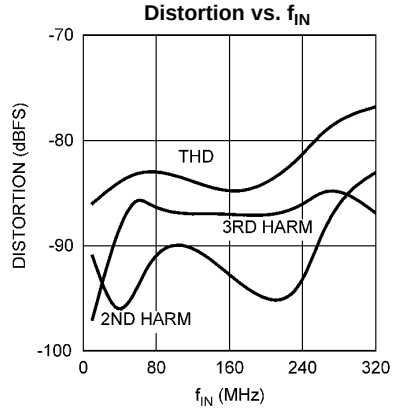



**Figure 22.**

## Typical Performance Characteristics (continued)

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, $V_A$ = +3.0V, $V_{DR}$ = +2.5V, Internal $V_{REF}$ = +1.2V, $f_{CLK}$ = 80 MHz, 50% Duty Cycle, DCS disabled, $V_{CM}$ = $V_{CMO}$, $f_{IN}$ = 10 MHz, $C_L$ = 5 pF/pin. $T_A$ = 25°C.

**SNR, SINAD, SFDR vs. Temperature**

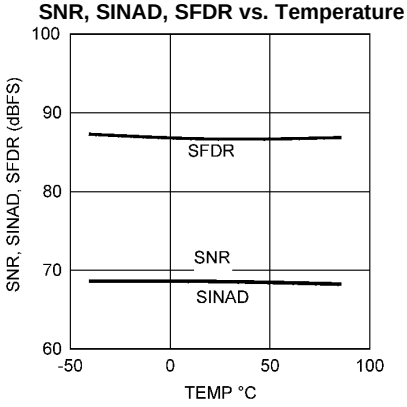



**Figure 23.**

**Distortion vs. Temperature**

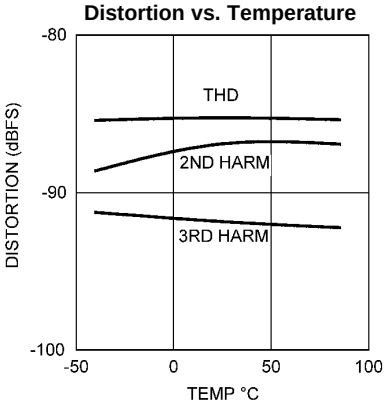



**Figure 24.**

**Spectral Response @ 10 MHz input**

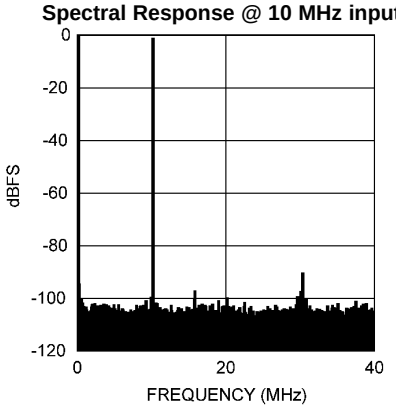



**Figure 25.**

**Spectral Response @ 70 MHz input**

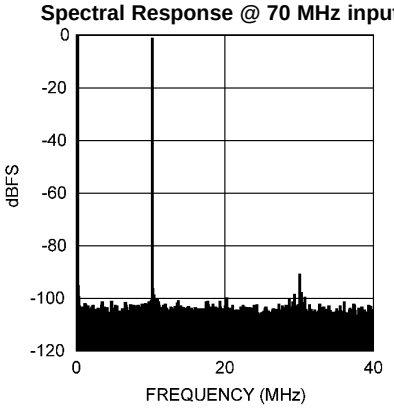



**Figure 26.**

**Spectral Response @ 170 MHz input**

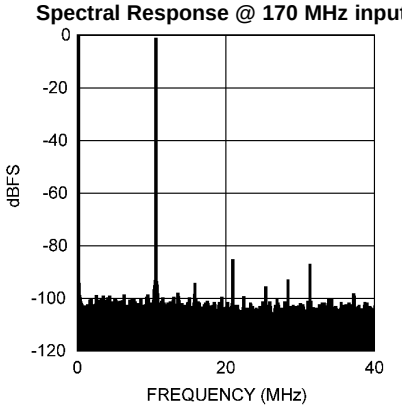



**Figure 27.**

**Intermodulation Distortion, $f_{IN}1$= 19.5 MHz, $f_{IN}2$ = 20.5 MHz**

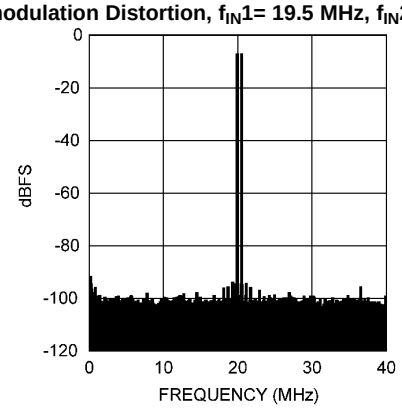



**Figure 28.**


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## Typical Performance Characteristics (continued)

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, $V_A$ = +3.0V, $V_{DR}$ = +2.5V, Internal $V_{REF}$ = +1.2V, $f_{CLK}$ = 80 MHz, 50% Duty Cycle, DCS disabled, $V_{CM}$ = $V_{CMO}$, $f_{IN}$ = 10 MHz, $C_L$ = 5 pF/pin. $T_A$ = 25°C.

**Power vs. $f_{CLK}$**

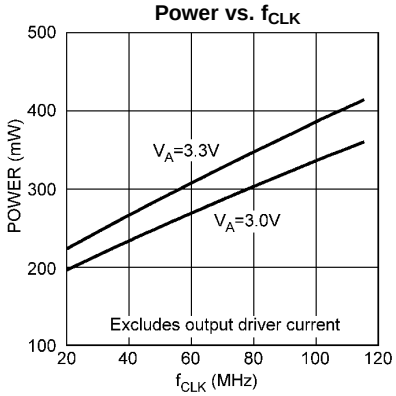



**Figure 29.**

# FUNCTIONAL DESCRIPTION

Operating on a single +3.0V supply, the ADC12C080 uses a pipeline architecture and has error correction circuitry to help ensure maximum performance. The differential analog input signal is digitized to 12 bits. The user has the choice of using an internal 1.2V stable reference, or using an external 1.2V reference. Any external reference is buffered on-chip to ease the task of driving that pin.

The output word rate is the same as the clock frequency. The analog input is acquired at the rising edge of the clock and the digital data for a given sample is delayed by the pipeline for 7 clock cycles. The digital outputs are CMOS compatible signals that are clocked by a synchronous data ready output signal (DRDY, pin 21) at the same rate as the clock input. Duty cycle stabilization and output data format are selectable using the quad state function OF/DCS pin (pin 12). The output data can be set for offset binary or two's complement.

Power-down is selectable using the PD pin (pin 30). A logic high on the PD pin reduces the converter power consumption. For normal operation, the PD pin should be connected to the analog ground (AGND).

# APPLICATIONS INFORMATION

## OPERATING CONDITIONS

We recommend that the following conditions be observed for operation of the ADC12C080:

$2.7V \le V_A \le 3.6V$

$2.4V \le V_{DR} \le V_A$

$20\ MHz \le f_{CLK} \le 80\ MHz$

1.2V internal reference

$V_{REF}$ = 1.2V (for an external reference)

$V_{CM}$ = 1.5V (from $V_{CMO}$)

## ANALOG INPUTS

### Signal Inputs

#### *Differential Analog Input Pins*

The ADC12C080 has one pair of analog signal input pins, $V_{IN}$+ and $V_{IN}$−, which form a differential input pair. The input signal, $V_{IN}$, is defined as

$$V_{IN} = (V_{IN}+) - (V_{IN}-) \quad (4)$$

Figure 30 shows the expected input signal range. Note that the common mode input voltage, $V_{CM}$, should be 1.5V. Using $V_{CMO}$ (pin 32) for $V_{CM}$ will ensure the proper input common mode level for the analog input signal. The positive peaks of the individual input signals should each never exceed 2.6V. Each analog input pin of the differential pair should have a maximum peak-to-peak voltage of 1V, be 180° out of phase with each other and be centered around $V_{CM}$. The peak-to-peak voltage swing at each analog input pin should not exceed the 1V or the output data will be clipped.

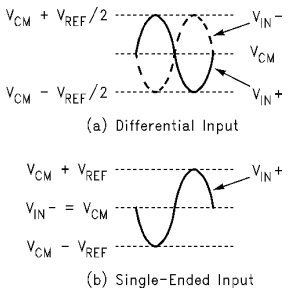



**Figure 30. Expected Input Signal Range**

For single frequency sine waves the full scale error in LSB can be described as approximately


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$$E_{FS} = 4096 ( 1 - \sin (90° + dev)) \quad (5)$$

Where dev is the angular difference in degrees between the two signals having a 180° relative phase relationship to each other (see Figure 30). For single frequency inputs, angular errors result in a reduction of the effective full scale input. For complex waveforms, however, angular errors will result in distortion.

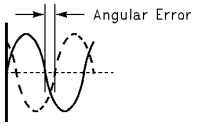



**Figure 31. Angular Errors Between the Two Input Signals Will Reduce the Output Level or Cause Distortion**

It is recommended to drive the analog inputs with a source impedance less than 100Ω. Matching the source impedance for the differential inputs will improve even ordered harmonic performance (particularly second harmonic).

Table 1 indicates the input to output relationship of the ADC12C080.

**Table 1. Input to Output Relationship**

| $V_{IN}^+$ | $V_{IN}^-$ | Binary Output | 2's Complement Output | |
|---|---|---|---|---|
| $V_{CM} - V_{REF}/2$ | $V_{CM} + V_{REF}/2$ | 0000 0000 0000 | 1000 0000 0000 | Negative Full-Scale |
| $V_{CM} - V_{REF}/4$ | $V_{CM} + V_{REF}/4$ | 0100 0000 0000 | 1100 0000 0000 | |
| $V_{CM}$ | $V_{CM}$ | 1000 0000 0000 | 0000 0000 0000 | Mid-Scale |
| $V_{CM} + V_{REF}/4$ | $V_{CM} - V_{REF}/4$ | 1100 0000 0000 | 0100 0000 0000 | |
| $V_{CM} + V_{REF}/2$ | $V_{CM} - V_{REF}/2$ | 1111 1111 1111 | 0111 1111 1111 | Positive Full-Scale |

### *Driving the Analog Inputs*

The $V_{IN}$+ and the $V_{IN}$− inputs of the ADC12C080 have an internal sample-and-hold circuit which consists of an analog switch followed by a switched-capacitor amplifier.

Figure 32 and Figure 33 show examples of single-ended to differential conversion circuits. The circuit in Figure 32 works well for input frequencies up to approximately 70MHz, while the circuit in Figure 33 works well above 70MHz.

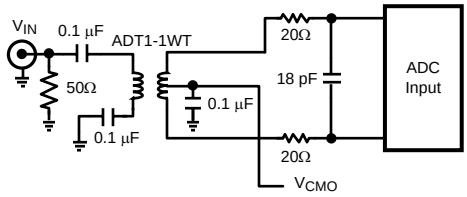



**Figure 32. Low Input Frequency Transformer Drive Circuit**

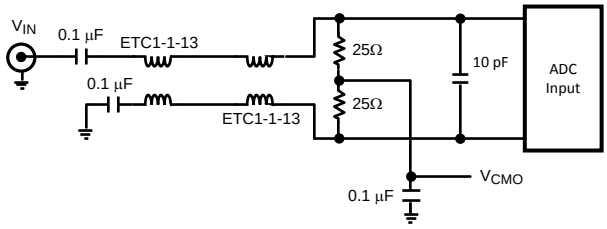



**Figure 33. High Input Frequency Transformer Drive Circuit**

One short-coming of using a transformer to achieve the single-ended to differential conversion is that most RF transformers have poor low frequency performance. A differential amplifier can be used to drive the analog inputs for low frequency applications. The amplifier must be fast enough to settle from the charging glitches on the analog input resulting from the sample-and-hold operation before the clock goes high and the sample is passed to the ADC core.

The SFDR performance of the converter depends on the external signal conditioning circuity used, as this affects how quickly the sample-and-hold charging glitch will settle. An external resistor and capacitor network as shown in Figure 34 should be used to isolate the charging glitches at the ADC input from the external driving circuit and to filter the wideband noise at the converter input. These components should be placed close to the ADC inputs because the analog input of the ADC is the most sensitive part of the system, and this is the last opportunity to filter that input. For Nyquist applications the RC pole should be at the ADC sample rate. The ADC input capacitance in the sample mode should be considered when setting the RC pole. For wideband undersampling applications, the RC pole should be set at least 1.5 to 2 times the maximum input frequency to maintain a linear delay response.

### *Input Common Mode Voltage*

The input common mode voltage, $V_{CM}$, should be in the range of 1.4V to 1.6V and be a value such that the peak excursions of the analog signal do not go more negative than ground or more positive than 2.6V. It is recommended to use $V_{CMO}$ (pin 32) as the input common mode voltage.

If the ADC12C080 is operated with $V_A$=3.6V, a resistor of approximately 1KΩ should be used from the $V_{CMO}$ pin to AGND.This will help maintain stability over the entire temperature range when using a high supply voltage.

### Reference Pins

The ADC12C080 is designed to operate with an internal or external 1.2V reference. The internal 1.2 Volt reference is the default condition when no external reference input is applied to the $V_{REF}$ pin. If a voltage is applied to the $V_{REF}$ pin, then that voltage is used for the reference. The $V_{REF}$ pin should always be bypassed to ground with a 0.1 µF capacitor close to the reference input pin.

It is important that all grounds associated with the reference voltage and the analog input signal make connection to the ground plane at a single, quiet point to minimize the effects of noise currents in the ground path.

The Reference Bypass Pins ($V_{RP}$, $V_{CMO}$, and $V_{RN}$) are made available for bypass purposes. These pins should each be bypassed to AGND with a low ESL (equivalent series inductance) 1 µF capacitor placed very close to the pin to minimize stray inductance. A 0.1 µF capacitor should be placed between $V_{RP}$ and $V_{RN}$ as close to the pins as possible, and a 1 µF capacitor should be placed in parallel. This configuration is shown in Figure 34. It is necessary to avoid reference oscillation, which could result in reduced SFDR and/or SNR. $V_{CMO}$ may be loaded to 1mA for use as a temperature stable 1.5V reference. The remaining pins should not be loaded.

Smaller capacitor values than those specified will allow faster recovery from the power down mode, but may result in degraded noise performance. Loading any of these pins, other than $V_{CMO}$ may result in performance degradation.

The nominal voltages for the reference bypass pins are as follows:

$V_{CMO}$ = 1.5 V

$V_{RP}$ = 2.0 V

$V_{RN}$ = 1.0 V

## OF/DCS Pin

Duty cycle stabilization and output data format are selectable using this quad state function pin. When enabled, duty cycle stabilization can compensate for clock inputs with duty cycles ranging from 30% to 70% and generate a stable internal clock, improving the performance of the part. With OF/DCS = $V_A$ the output data format is 2's complement and duty cycle stabilization is not used. With OF/DCS = AGND the output data format is offset binary and duty cycle stabilization is not used. With OF/DCS = (2/3)*$V_A$ the output data format is 2's complement and duty cycle stabilization is applied to the clock. If OF/DCS is (1/3)*$V_A$ the output data format is offset binary and duty cycle stabilization is applied to the clock. While the sense of this pin may be changed "on the fly," doing this is not recommended as the output data could be erroneous for a few clock cycles after this change is made.


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## DIGITAL INPUTS

Digital CMOS compatible inputs consist of CLK, and PD.

### Clock Input

The CLK controls the timing of the sampling process. To achieve the optimum noise performance, the clock input should be driven with a stable, low jitter clock signal in the range indicated in the Electrical Table. The clock input signal should also have a short transition region. This can be achieved by passing a low-jitter sinusoidal clock source through a high speed buffer gate. The trace carrying the clock signal should be as short as possible and should not cross any other signal line, analog or digital, not even at 90°.

The clock signal also drives an internal state machine. If the clock is interrupted, or its frequency is too low, the charge on the internal capacitors can dissipate to the point where the accuracy of the output data will degrade. This is what limits the minimum sample rate.

The clock line should be terminated at its source in the characteristic impedance of that line. Take care to maintain a constant clock line impedance throughout the length of the line. Refer to Application Note AN-905 (SNLA035) for information on setting characteristic impedance.

It is highly desirable that the the source driving the ADC clock pins only drive that pin. However, if that source is used to drive other devices, then each driven pin should be AC terminated with a series RC to ground, such that the resistor value is equal to the characteristic impedance of the clock line and the capacitor value is

$$C \geq \frac{4 \times t_{PD} \times L}{Z_o} \tag{6}$$

where $t_{PD}$ is the signal propagation rate down the clock line, "L" is the line length and $Z_O$ is the characteristic impedance of the clock line. This termination should be as close as possible to the ADC clock pin but beyond it as seen from the clock source. Typical $t_{PD}$ is about 150 ps/inch (60 ps/cm) on FR-4 board material. The units of "L" and $t_{PD}$ should be the same (inches or centimeters).

The duty cycle of the clock signal can affect the performance of the A/D Converter. Because achieving a precise duty cycle is difficult, the ADC12C080 has a Duty Cycle Stabilizer.

### Power-Down (PD)

The PD pin, when high, holds the ADC12C080 in a power-down mode to conserve power when the converter is not being used. The power consumption in this state is 5 mW if the clock is stopped when PD is high. The output data pins are undefined and the data in the pipeline is corrupted while in the power down mode.

The Power Down Mode Exit Cycle time is determined by the value of the components on pins 1, 2, and 32 and is about 3 ms with the recommended components on the $V_{RP}$, $V_{CMO}$ and $V_{RN}$ reference bypass pins. These capacitors loose their charge in the Power Down mode and must be recharged by on-chip circuitry before conversions can be accurate. Smaller capacitor values allow slightly faster recovery from the power down mode, but can result in a reduction in SNR, SINAD and ENOB performance.

## DIGITAL OUTPUTS

Digital outputs consist of the CMOS signals D0-D11, and DRDY.

The ADC12C080 has 13 CMOS compatible data output pins corresponding to the converted input value and a data ready (DRDY) signal that should be used to capture the output data. Valid data is present at these outputs while the PD pin is low. Data should be captured and latched with the rising edge of the DRDY signal.

Be very careful when driving a high capacitance bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current flows through $V_{DR}$ and DRGND. These large charging current spikes can cause on-chip ground noise and couple into the analog circuitry, degrading dynamic performance. Adequate bypassing, limiting output capacitance and careful attention to the ground plane will reduce this problem. The result could be an apparent reduction in dynamic performance.

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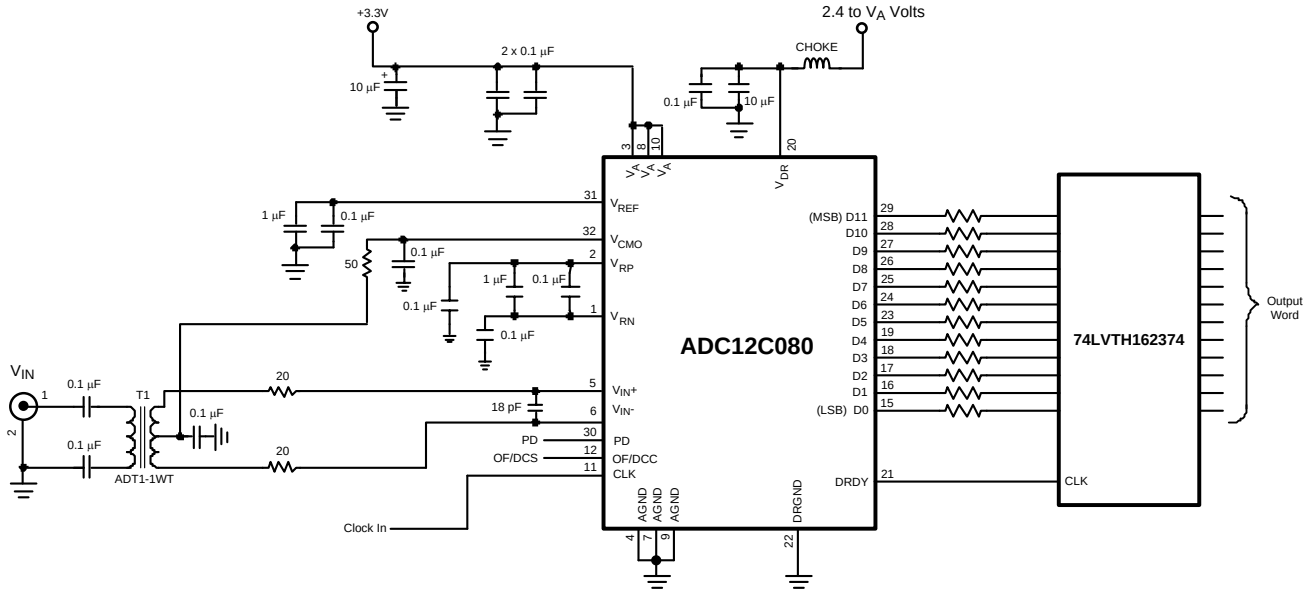



**Figure 34. Application Circuit**

## POWER SUPPLY CONSIDERATIONS

The power supply pins should be bypassed with a 0.1 µF capacitor and with a 100 pF ceramic chip capacitor close to each power pin. Leadless chip capacitors are preferred because they have low series inductance.

As is the case with all high-speed converters, the ADC12C080 is sensitive to power supply noise. Accordingly, the noise on the analog supply pin should be kept below 100 $mV_{P-P}$.

No pin should ever have a voltage on it that is in excess of the supply voltages, not even on a transient basis. Be especially careful of this during power turn on and turn off.

The $V_{DR}$ pin provides power for the output drivers and may be operated from a supply in the range of 2.4V to $V_A$. This enables lower power operation, reduces the noise coupling effects from the digital outputs to the analog circuitry and simplifies interfacing to lower voltage devices and systems.

## LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. Maintaining separate analog and digital areas of the board, with the ADC12C080 between these areas, is required to achieve specified performance.

The ground return for the data outputs (DRGND) carries the ground current for the output drivers. The output current can exhibit high transients that could add noise to the conversion process. To prevent this from happening, the DRGND pins should NOT be connected to system ground in close proximity to any of the ADC12C080's other ground pins.

Capacitive coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry, and to keep the clock line as short as possible.

The effects of the noise generated from the ADC output switching can be minimized through the use of 22Ω resistors in series with each data output line. Locate these resistors as close to the ADC output pins as possible.

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise. This is because of the skin effect. Total surface area is more important than is total ground plane area.


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Generally, analog and digital lines should cross each other at 90° to avoid crosstalk. To maximize accuracy in high speed, high resolution systems, however, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. Even the generally accepted 90° crossing should be avoided with the clock line as even a little coupling can cause problems at high frequencies. This is because other lines can introduce jitter into the clock line, which can lead to degradation of SNR. Also, the high speed clock can introduce noise into the analog chain.

Best performance at high frequencies and at high resolution is obtained with a straight signal path. That is, the signal path through all components should form a straight line wherever possible.

Be especially careful with the layout of inductors and transformers. Mutual inductance can change the characteristics of the circuit in which they are used. Inductors and transformers should *not* be placed side by side, even with just a small part of their bodies beside each other. For instance, place transformers for the analog input and the clock input at 90° to one another to avoid magnetic coupling.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference input pin and ground should be connected to a very clean point in the ground plane.

All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed in the analog area of the board. All digital circuitry and dynamic I/O lines should be placed in the digital area of the board. The ADC12C080 should be between these two areas. Furthermore, all components in the reference circuitry and the input signal chain that are connected to ground should be connected together with short traces and enter the ground plane at a single, quiet point. All ground connections should have a low inductance path to ground.

## DYNAMIC PERFORMANCE

To achieve the best dynamic performance, the clock source driving the CLK input must have a sharp transition region and be free of jitter. Isolate the ADC clock from any digital circuitry with buffers, as with the clock tree shown in Figure 35. The gates used in the clock tree must be capable of operating at frequencies much higher than those used if added jitter is to be prevented.

As mentioned in LAYOUT AND GROUNDING, it is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce jitter into the clock signal, which can lead to reduced SNR performance, and the clock can introduce noise into other lines. Even lines with 90° crossings have capacitive coupling, so try to avoid even these 90° crossings of the clock line.

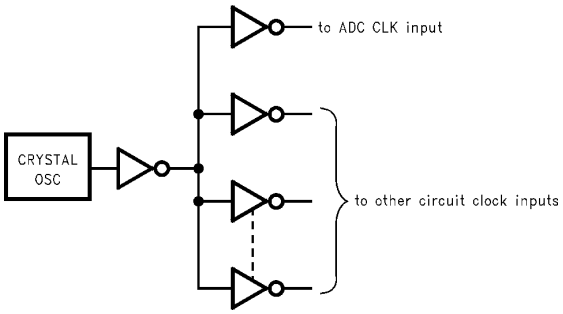



**Figure 35. Isolating the ADC Clock from other Circuitry with a Clock Tree**

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## REVISION HISTORY

| Changes from Revision B (April 2013) to Revision C | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 25 |


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| ADC12C080CISQ/NOPB | Active | Production | WQFN (RTV) \| 32 | 1000 \| LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 85 | 12C080 |
| ADC12C080CISQ/NOPB.A | Active | Production | WQFN (RTV) \| 32 | 1000 \| LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 85 | 12C080 |
| ADC12C080CISQE/NO.A | Active | Production | WQFN (RTV) \| 32 | 250 \| SMALL T&R | Yes | SN | Level-3-260C-168 HR | -40 to 85 | 12C080 |
| ADC12C080CISQE/NOPB | Active | Production | WQFN (RTV) \| 32 | 250 \| SMALL T&R | Yes | SN | Level-3-260C-168 HR | -40 to 85 | 12C080 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

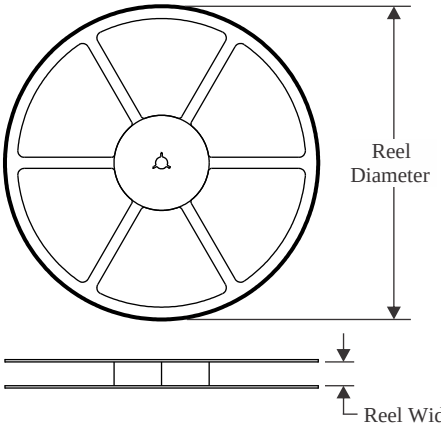
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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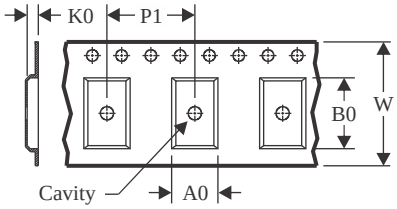
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

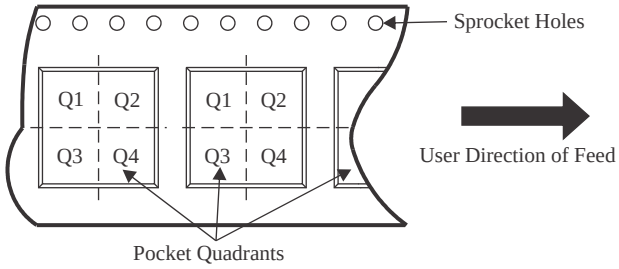



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

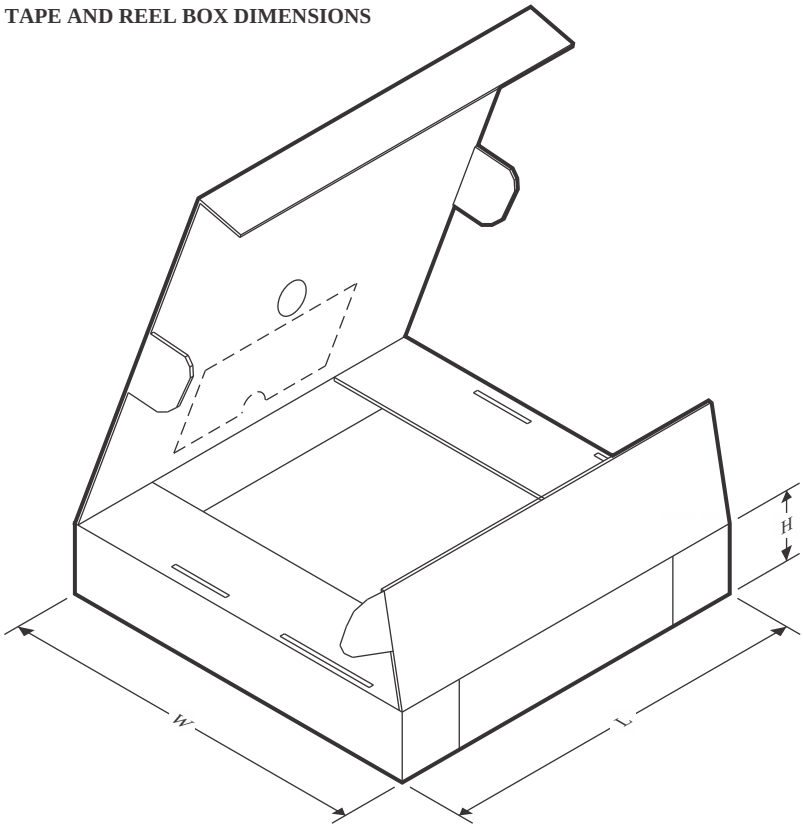
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADC12C080CISQ/NOPB | WQFN | RTV | 32 | 1000 | 177.8 | 12.4 | 5.3 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| ADC12C080CISQE/NOPB | WQFN | RTV | 32 | 250 | 177.8 | 12.4 | 5.3 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

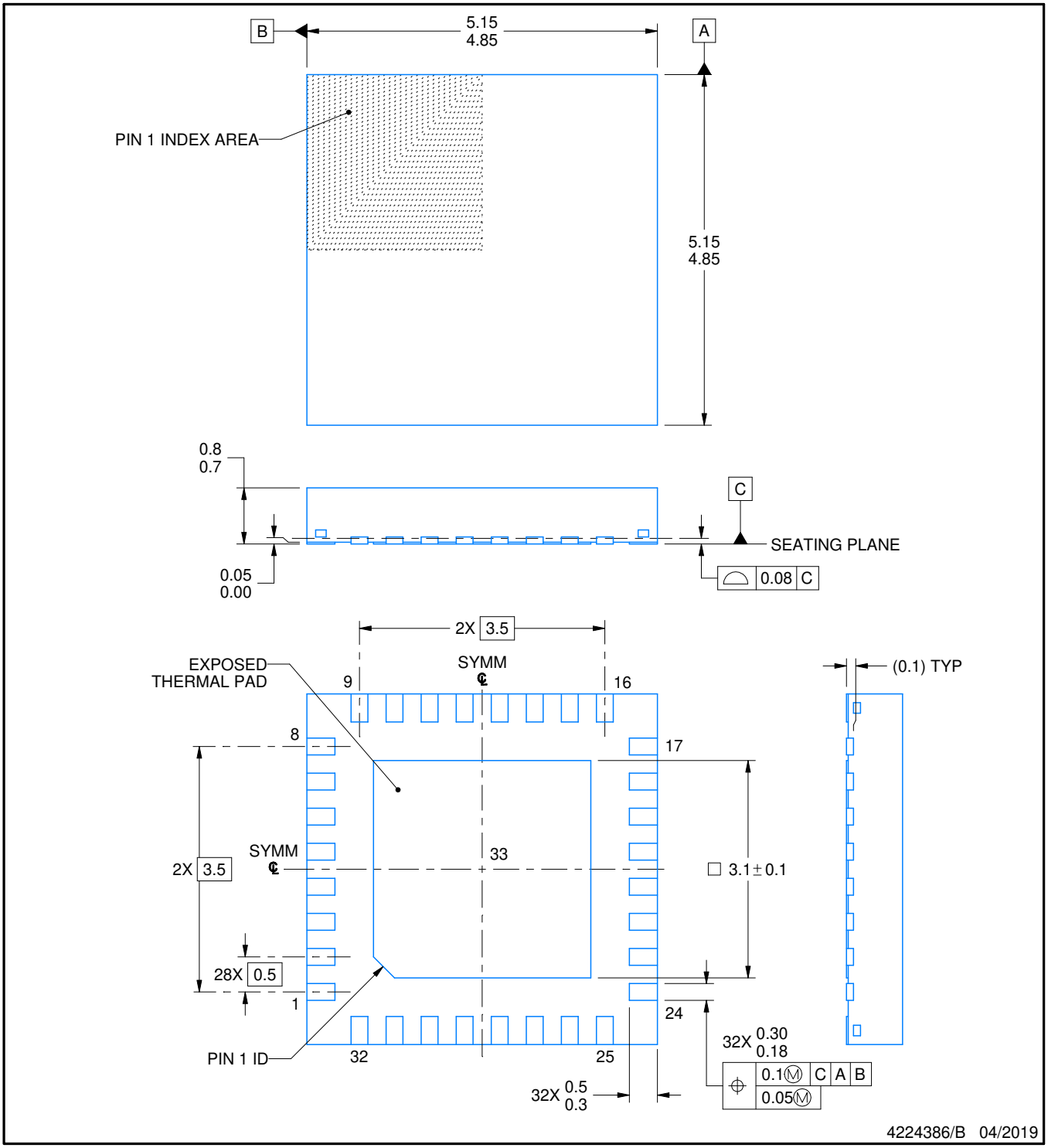
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ADC12C080CISQ/NOPB | WQFN | RTV | 32 | 1000 | 208.0 | 191.0 | 35.0 |
| ADC12C080CISQE/NOPB | WQFN | RTV | 32 | 250 | 208.0 | 191.0 | 35.0 |

# PACKAGE OUTLINE

## RTV0032A

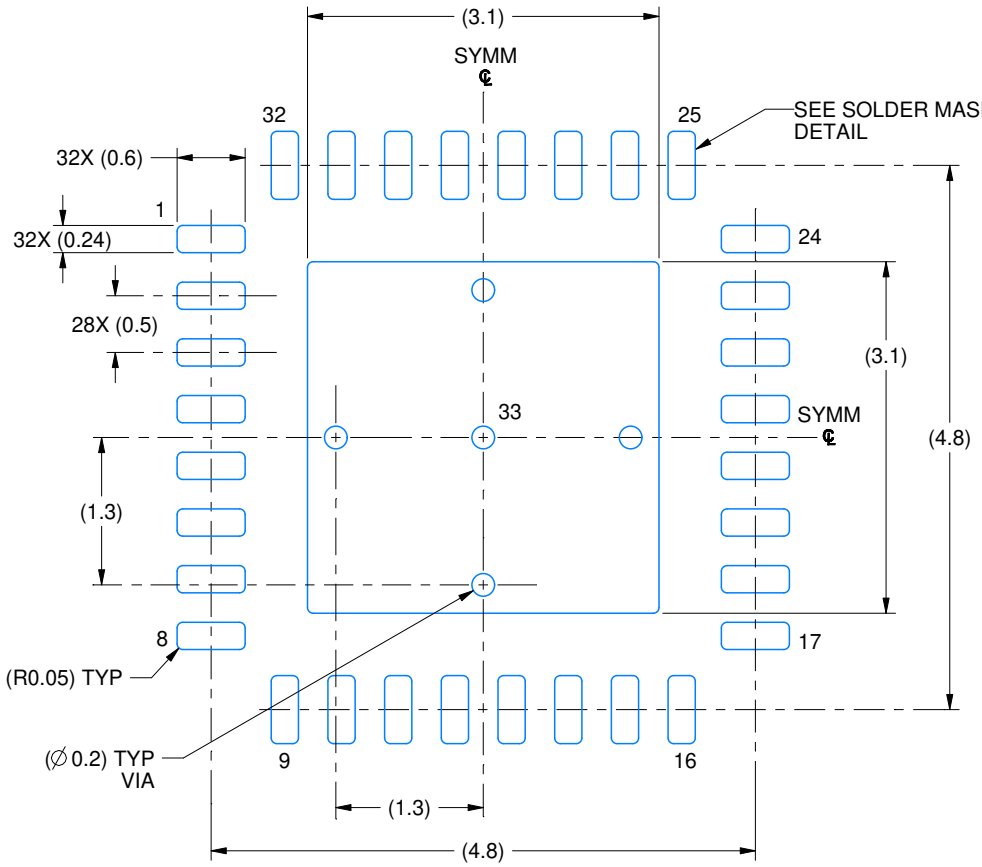
## WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

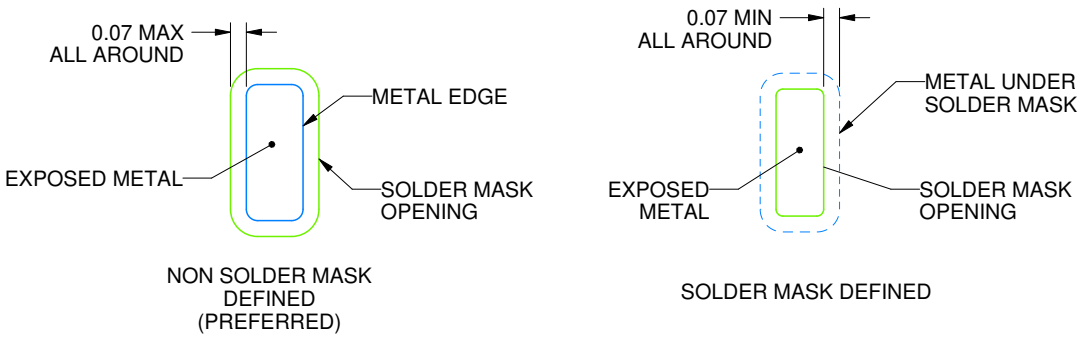



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X




SOLDER MASK DETAILS

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NOTES: (continued)

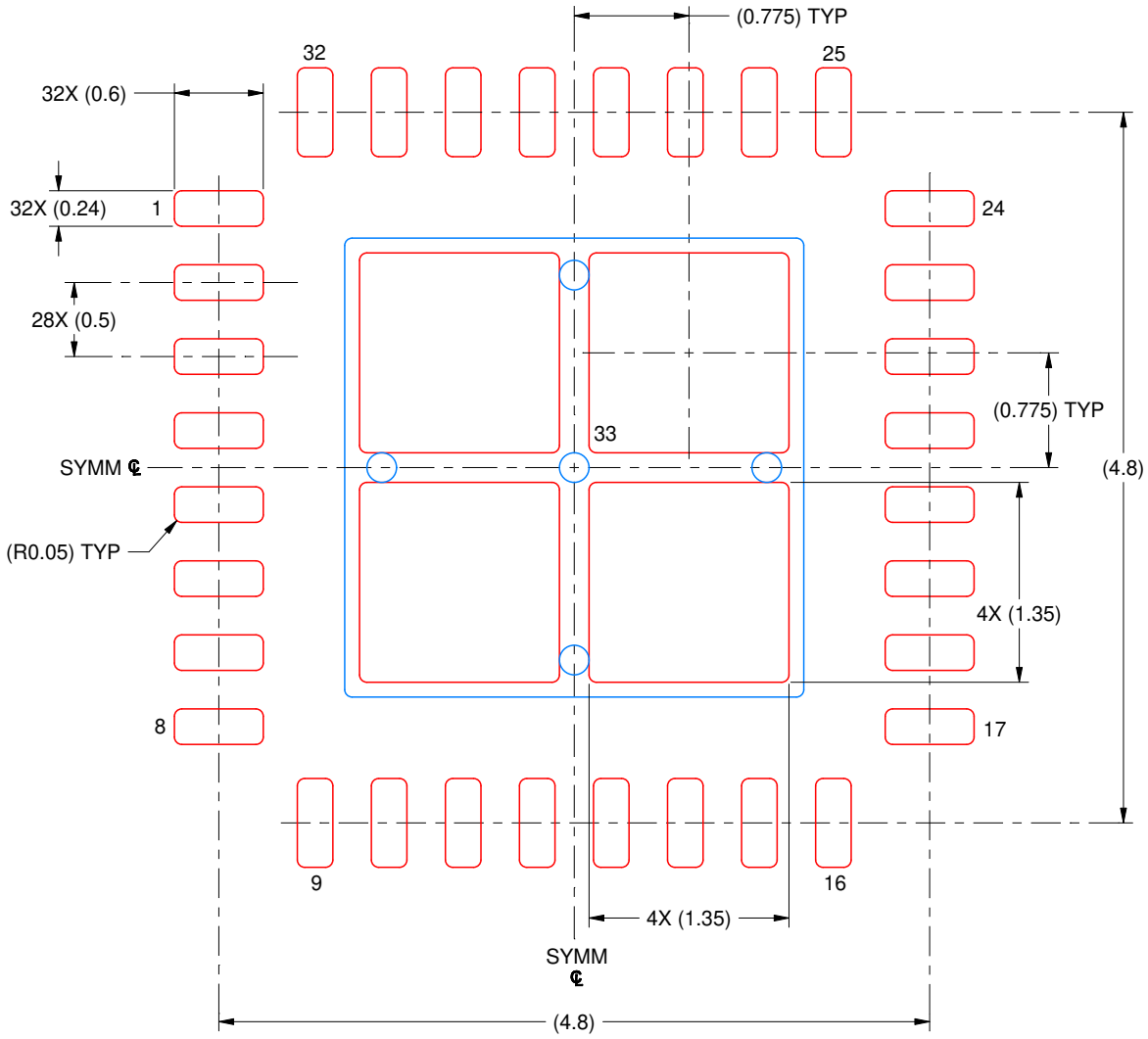
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

## RTV0032A

## WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 33
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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