ADC141S626 14-Bit, 50 kSPS to 250 kSPS, Differential Input, Micro Power A/D Converter

Check for Samples: ADC141S626

FEATURES

- **True Differential Inputs**
- **Guaranteed Performance from 50 kSPS to 250 kSPS**
- **External Reference**
- **Zero-Power Track Mode**
- **Wide Input Common-Mode Voltage Range**
- **Operating Temperature Range of −40°C to +85°C**
- **SPI™/QSPI™/MICROWIRE/DSP Compatible Serial Interface**

APPLICATIONS

- **Automotive Navigation**
- **Portable Systems**
- **Medical Instruments**
- **Instrumentation and Control Systems**
- **Motor Control**
- **Direct Sensor Interface**

KEY SPECIFICATIONS

- **Conversion Rate: 50 kSPS to 250 kSPS**
- **INL: ± 0.95 LSB (Max)**
- **DNL: ± 0.95 LSB (Max)**
- **SNR: 82 dBc (Max)**
- **THD: -90 dBc (Typ)**
- **ENOB: 13.3 Bits(Min)**
- **Power Consumption:**
  - **200 kSPS, 3V: 2.0 mW (Typ)**
  - **250 kSPS, 5V: 4.8 mW (Typ)**
  - **Power-Down, 3V: 4 µW (Typ)**
  - **Power-Down, 5V: 13 µW (Typ)**

DESCRIPTION

The ADC141S626 is a 14-bit, 50 kSPS to 250 kSPS sampling Analog-to-Digital (A/D) converter. The converter is based on a successive-approximation register (SAR) architecture where the differential nature of the analog inputs is maintained from the internal sample-and-hold circuits throughout the A/D converter to provide excellent common-mode signal rejection. The ADC141S626 features an external reference that can be varied from 1.0V to V_A. It also features a zero-power track mode where the ADC is consuming the minimum amount of supply current while the internal sampling capacitor is tracking the applied analog input voltage.

The serial data output is binary 2's complement and is compatible with several standards, such as SPI™, QSPI™, MICROWIRE, and many common DSP serial interfaces. The conversion result is clocked out by the serial clock input and is the result of the conversion currently in progress; thus, ADC141S626 has no latency.

The ADC141S626 may be operated with independent analog (V_A) and digital input/output (V_{IO}) supplies. V_A and V_{IO} can range from 2.7V to 5.5V and can be set independent of each other. This allows a user to maximize performance and minimize power consumption by operating the analog portion of the ADC at a V_A of 5V while communicating with a 3V controller on the digital side. With a 3V source, the power consumption when operating at 200 kSPS is 2.0 mW. With a 5V source, the power consumption when operating at 250 kSPS is 4.8 mW. The power consumption drops down to 4 µW and 13 µW respectively when the ADC141S626 enters acquisition (power-down) mode. The differential input, low power consumption, and small size make the ADC141S626 ideal for direct connection to bridge sensors and transducers in battery operated systems or remote data acquisition applications.

Operation is guaranteed over the temperature range of −40°C to +85°C and clock rates of 0.9 MHz to 4.5 MHz. The ADC141S626 is available in a 10-lead VSSOP package.

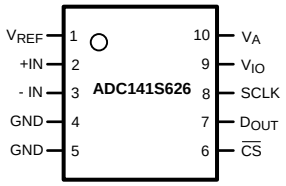
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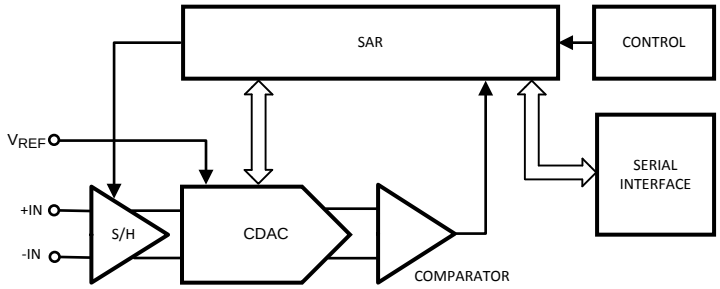
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Connection Diagram



Block Diagram



PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	V_{REF}	Voltage Reference Input. A voltage reference between 1V and V_A must be applied to this input. V_{REF} must be decoupled to GND with a minimum ceramic capacitor value of 0.1 µF. A bulk capacitor value of 1.0 µF to 10 µF in parallel with the 0.1 µFcapacitor is recommended for enhanced performance.
2	+IN	Non-Inverting Input. +IN is the positive analog input for the differential signal applied to the ADC141S626.
3	−IN	Inverting Input. −IN is the negative analog input for the differential signal applied to the ADC141S626.
4	GND	Ground. GND is the ground reference point for all signals applied to the ADC141S626.
5	GND	Ground. GND is the ground reference point for all signals applied to the ADC141S626.
6	$\overline{CS}$	Chip Select Bar. $\overline{CS}$ must be active LOW during an SPI conversion, which begins on the falling edge of $\overline{CS}$. The ADC141S626 is in acquisition mode when $\overline{CS}$ is HIGH.
7	D_{OUT}	Serial Data Output. The conversion result is provided on D_{OUT}. The serial data output word is comprised of 2 null bits followed by 14 data bits (MSB first). During a conversion, the data is output on the falling edges of SCLK and is valid on the subsequent rising edges.
8	SCLK	Serial Clock. SCLK is used to control data transfer and serves as the conversion clock.
9	V_{IO}	Digital Input/Output Power Supply Input. A voltage source between 2.7V and 5.5V must be applied to this input. V_{IO} must be decoupled to GND with a ceramic capacitor value of 0.1 µF in parallel with a bulk capacitor value of 1.0 µF to 10 µF.
10	V_A	Analog Power Supply Input. A voltage source between 2.7V and 5.5V must be applied to this input. V_A must be decoupled to GND with a ceramic capacitor value of 0.1 µF in parallel with a bulk capacitor value of 1.0 µF to 10 µF.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings[1][2][3]

Analog Supply Voltage V_A		−0.3V to 6.5V
Digital I/O Supply Voltage V_{IO}		−0.3V to 6.5V
Voltage on Any Analog Input Pin to GND		−0.3V to (V_A + 0.3V)
Voltage on Any Digital Input Pin to GND		−0.3V to (V_{IO} + 0.3V)
Input Current at Any Pin[4]		±10 mA
Package Input Current[4]		±50 mA
Power Consumption at T_A = 25°C		See[5]
ESD Susceptibility[6]	Human Body Model	4000V
	Machine Model	300V
	Charge Device Model	1250V
Junction Temperature		+150°C
Storage Temperature		−65°C to +150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.
(2) All voltages are measured with respect to GND = 0V, unless otherwise specified.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < GND or V_{IN} > V_A), the current at that pin should be limited to 10 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to five.
(5) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A)/\theta_{JA}$. The values for maximum power dissipation listed above will be reached only when the ADC141S626 is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Such conditions should always be avoided.
(6) Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is a 220 pF capacitor discharged through 0 Ω. Charge device model simulates a pin slowly acquiring charge (such as from a device sliding down the feeder in an automated assembler) then rapidly being discharged.

Operating Ratings[1][2]

Operating Temperature Range	−40°C ≤ T_A ≤ +85°C
Supply Voltage, V_A	+2.7V to +5.5V
Supply Voltage, V_{IO}	+2.7V to +5.5V
Reference Voltage, V_{REF}	1.0V to V_A
Analog Input Pins Voltage Range	0 to V_A
Differential Analog Input Voltage	$-V_{REF}$ to $+V_{REF}$
Input Common-Mode Voltage, V_{CM}	See Figure 41
Digital Input Pins Voltage Range	0 to V_{IO}
Clock Frequency	0.9 MHz to 4.5 MHz

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.
(2) All voltages are measured with respect to GND = 0V, unless otherwise specified.

Package Thermal Resistance[1][2]

Package	θ_{JA}
10-lead VSSOP	240°C / W

(1) Soldering process must comply with TI's Reflow Temperature Profile specifications. Refer to www.ti.com/packaging.
(2) Reflow temperature profiles are different for lead-free packages.

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ADC141S626 Converter Electrical Characteristics(1)

The following specifications apply for $V_A = V_{IO} = V_{REF}$ = +2.7V to 5.5V and f_{SCLK} = 0.9 to 3.6 MHz or $V_A = V_{IO} = V_{REF}$ = +4.5V to 5.5V and f_{SCLK} = 3.6 to 4.5 MHz; f_{IN} = 20 kHz and C_L = 25 pF, unless otherwise noted. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**; all other limits are at T_A = 25°C.

Symbol	Parameter	Conditions		Typical	Limits	Units
STATIC CONVERTER CHARACTERISTICS						
	Resolution with No Missing Codes				**14**	Bits
INL	Integral Non-Linearity			±0.5	**±0.95**	LSB (max)
DNL	Differential Non-Linearity			±0.5	**±0.95**	LSB (max)
OE	Offset Error			−1	**±5**	LSB (max)
FSE	Positive Full-Scale Error			−3	**±7**	LSB (max)
	Negative Full-Scale Error			0.5	**±4**	LSB (max)
GE	Positive Gain Error			−1.5	**±6**	LSB (max)
	Negative Gain Error			1.5	**±6**	LSB (max)
DYNAMIC CONVERTER CHARACTERISTICS						
SINAD	Signal-to-Noise Plus Distortion Ratio	$V_A = V_{IO} = V_{REF}$ = +3V, −0.1 dBFS		81.9	**80.1**	dBc (min)
		$V_A = V_{IO} = V_{REF}$ = +5V, −0.1 dBFS		84.2	**82**	dBc (min)
SNR	Signal-to-Noise Ratio	$V_A = V_{IO} = V_{REF}$ = +3V, −0.1 dBFS		82	**80.2**	dBc (min)
		$V_A = V_{IO} = V_{REF}$ = +5V, −0.1 dBFS		84.3	**82**	dBc (min)
THD	Total Harmonic Distortion	$V_A = V_{IO} = V_{REF}$ = +3V, −0.1 dBFS		−102		dBc
		$V_A = V_{IO} = V_{REF}$ = +5V, −0.1 dBFS		−102		dBc
SFDR	Spurious-Free Dynamic Range	$V_A = V_{IO} = V_{REF}$ = +3V, −0.1 dBFS		97		dBc
		$V_A = V_{IO} = V_{REF}$ = +5V, −0.1 dBFS		101		dBc
ENOB	Effective Number of Bits	$V_A = V_{IO} = V_{REF}$ = +3V, −0.1 dBFS		13.3	**13.0**	bits (min)
		$V_A = V_{IO} = V_{REF}$ = +5V, −0.1 dBFS		13.7	**13.3**	bits (min)
FPBW	−3 dB Full Power Bandwidth	Output at 70.7%FS with FS Input	Differential Input	26		MHz
			Single-Ended Input	22		MHz
ANALOG INPUT CHARACTERISTICS						
V_{IN}	Differential Input Range				**$-V_{REF}$**	V (min)
					$+V_{REF}$	V (max)
I_{DCL}	DC Leakage Current	$V_{IN} = V_{REF}$ or $V_{IN} = -V_{REF}$			**±1**	µA (max)
C_{INA}	Input Capacitance	In Acquisition Mode		30		pF
		In Conversion Mode		3		pF
CMRR	Common Mode Rejection Ratio	See the Specification Definitions for the test condition		76		dB
DIGITAL INPUT CHARACTERISTICS						
V_{IH}	Input High Voltage	V_{IO} = +2.7V to 5.5V		1.9	**2.3**	V (min)
V_{IL}	Input Low Voltage	V_{IO} = +2.7V to 5.5V		1.0	**0.7**	V (max)
I_{IN}	Input Current	V_{IN} = 0V or V_A			**±1**	µA (max)
C_{IND}	Input Capacitance			2	**4**	pF (max)
DIGITAL OUTPUT CHARACTERISTICS						
V_{OH}	Output High Voltage	I_{SOURCE} = 200 µA		V_A − 0.05	**V_A − 0.2**	V (min)
		I_{SOURCE} = 1 mA		V_A − 0.16		V
V_{OL}	Output Low Voltage	I_{SINK} = 200 µA		0.01	**0.4**	V (max)
		I_{SINK} = 1 mA		0.05		V
I_{OZH}, I_{OZL}	TRI-STATE Leakage Current	Force 0V or V_A			**±1**	µA (max)
C_{OUT}	TRI-STATE Output Capacitance	Force 0V or V_A		2	**4**	pF (max)
	Output Coding			Binary 2'S Complement		

(1) Typical values are at T_J = 25°C and represent most likely parametric norms. Test limits are guaranteed to TI's AOQL (Average Outgoing Quality Level).

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ADC141S626 Converter Electrical Characteristics(1) (continued)

The following specifications apply for $V_A = V_{IO} = V_{REF}$ = +2.7V to 5.5V and f_{SCLK} = 0.9 to 3.6 MHz or $V_A = V_{IO} = V_{REF}$ = +4.5V to 5.5V and f_{SCLK} = 3.6 to 4.5 MHz; f_{IN} = 20 kHz and C_L = 25 pF, unless otherwise noted. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**; all other limits are at T_A = 25°C.

Symbol	Parameter	Conditions	Typical	Limits	Units
POWER SUPPLY CHARACTERISTICS					
V_A	Analog Supply Voltage Range			**2.7**	V (min)
				5.5	V (max)
V_{IO}	Digital Input/Output Supply Voltage Range	See(2)		**2.7**	V (min)
				5.5	V (max)
V_{REF}	Reference Voltage Range			**1.0**	V (min)
				V_A	V (max)
I_{VA} (Conv)	Analog Supply Current, Conversion Mode	f_{SCLK} = 3.6 MHz, V_A = 3V, f_S = 200 kSPS, f_{IN} = 20 kHz	540	**760**	µA (max)
		f_{SCLK} = 4.5 MHz, V_A = 5V, f_S = 250 kSPS, f_{IN} = 20 kHz	740	**970**	µA (max)
I_{VIO} (Conv)	Digital I/O Supply Current, Conversion Mode	f_{SCLK} = 3.6 MHz, V_A = 3V, f_S = 200 kSPS, f_{IN} = 20 kHz	90	**190**	µA (max)
		f_{SCLK} = 4.5 MHz, V_A = 5V, f_S = 250 kSPS, f_{IN} = 20 kHz	170	**260**	µA (max)
I_{VREF} (Conv)	Reference Current, Conversion Mode	f_{SCLK} = 3.6 MHz, V_A = 3V, f_S = 200 kSPS, f_{IN} = 20 kHz	25	**60**	µA (max)
		f_{SCLK} = 4.5 MHz, V_A = 5V, f_S = 250 kSPS, f_{IN} = 20 kHz	45	**80**	µA (max)
I_{VA} (PD)	Analog Supply Current, Power Down Mode ($\overline{CS}$ high)	f_{SCLK} = 4.5 MHz, V_A = 5V	8		µA
		f_{SCLK} = 0(3)	2	**3**	µA (max)
I_{VIO} (PD)	Digital I/O Supply Current, Power Down Mode ($\overline{CS}$ high)	f_{SCLK} = 4.5 MHz, V_A = 5V	3		µA
		f_{SCLK} = 0(3)	0.1	**0.3**	µA (max)
I_{VREF} (PD)	Reference Current, Power Down Mode ($\overline{CS}$ high)	f_{SCLK} = 4.5 MHz, V_A = 5V	0.1		µA
		f_{SCLK} = 0(3)	0.1	**0.2**	µA (max)
PWR (Conv)	Power Consumption, Conversion Mode	f_{SCLK} = 3.6 MHz, f_S = 200 kSPS, f_{IN} = 20 kHz, $V_A = V_{IO} = V_{REF}$ = 3.0V	2.0	**3.0**	mW
		f_{SCLK} = 4.5 MHz, f_S = 250 kSPS, f_{IN} = 20 kHz, $V_A = V_{IO} = V_{REF}$ = 5.0V	4.8	**6.5**	mW
PWR (PD)	Power Consumption, Power Down Mode ($\overline{CS}$ high)	f_{SCLK} = 0, $V_A = V_{IO} = V_{REF}$ = 3.0V(3)	3	**4**	µW (max)
		f_{SCLK} = 0, $V_A = V_{IO} = V_{REF}$ = 5.0V(3)	13	**17**	µW (max)
PSRR	Power Supply Rejection Ratio	See the Specification Definitions for the test condition.	−85		dB
AC ELECTRICAL CHARACTERISTICS					
f_{SCLK}	Maximum Clock Frequency	$V_A = V_{IO} = V_{REF}$ = +2.7V to 5.5V	4.8	**4.5**	MHz (min)
f_{SCLK}	Minimum Clock Frequency			**0.9**	MHz (max)
f_S	Maximum Sample Rate(4)			**250**	kSPS (min)
t_{ACQ}	Acquisition/Track Time			**667**	ns (min)
t_{CONV}	Conversion/Hold Time			**15**	SCLK cycles
t_{AD}	Aperture Delay	See the Specification Definitions.	6		ns

(2) The value of V_{IO} is independent of the value of V_A. For example, V_{IO} could be operating at 5V while V_A is operating at 3V or V_{IO} could be operating at 3V while V_A is operating at 5V.
(3) This parameter is guaranteed by design and/or characterization and is not tested in production.
(4) While the maximum sample rate is f_{SCLK}/18, the actual sample rate may be lower than this by having the $\overline{CS}$ rate slower than f_{SCLK}/18.

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ADC141S626 Timing Specifications(1)

The following specifications apply for $V_A = V_{IO} = V_{REF}$ = +2.7V to 5.5V and f_{SCLK} = 0.9 to 4.5 MHz, C_L = 25 pF, **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**: all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Typical	Limits	Units
t_{CSS}	$\overline{CS}$ Setup Time prior to an SCLK rising edge		3	**6**	ns (min)
			$1/f_{SCLK}$ - 3	**$1/f_{SCLK}$ - 6**	ns (max)
t_{DH}	D_{OUT} Hold Time after an SCLK falling edge		10	**6**	ns (min)
t_{DA}	D_{OUT} Access Time after an SCLK falling edge		28	**40**	ns (max)
t_{DIS}	D_{OUT} Disable Time after the rising edge of $\overline{CS}$(2)		10	**20**	ns (max)
t_{CS}	Minimum $\overline{CS}$ Pulse Width		5	**20**	ns (min)
t_{EN}	D_{OUT} Enable Time after the falling edge of $\overline{CS}$		32	**51**	ns (max)
t_{CH}	SCLK High Time		67	**89**	ns (min)
t_{CL}	SCLK Low Time		67	**89**	ns (min)
t_r	D_{OUT} Rise Time		7		ns
t_f	D_{OUT} Fall Time		7		ns

(1) Typical values are at T_J = 25°C and represent most likely parametric norms. Test limits are guaranteed to TI's AOQL (Average Outgoing Quality Level).
(2) t_{DIS} is the time for D_{OUT} to change 10% while being loaded by the Timing Test Circuit.

Timing Diagrams

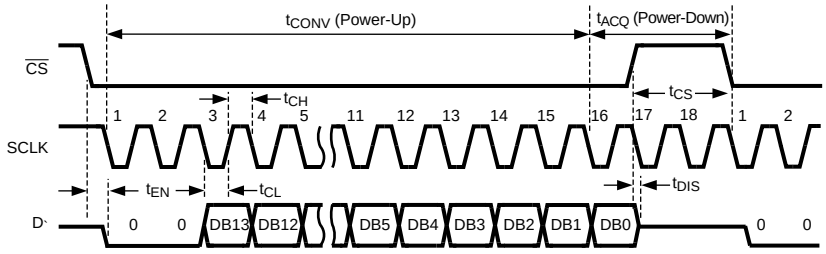


Figure 1. ADC141S626 Single Conversion Timing Diagram

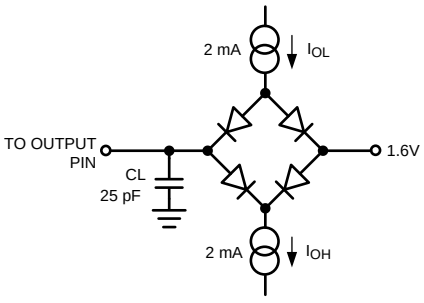


Figure 2. Timing Test Circuit

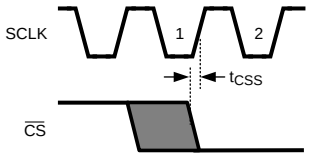


Figure 3. Valid $\overline{CS}$ Assertion Times

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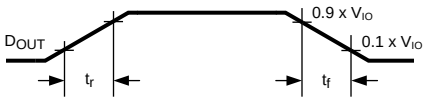


Figure 4. D_{OUT} Rise and Fall Times

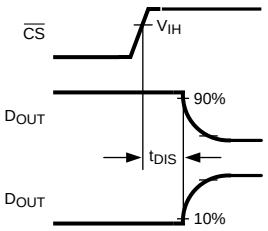


Figure 5. Voltage Waveform for t_{DIS}

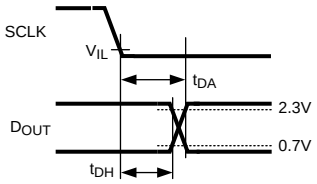


Figure 6. D_{OUT} Hold and Access Times

Specification Definitions

APERTURE DELAY is the time between the first falling edge of SCLK and the time when the input signal is sampled for conversion.

COMMON MODE REJECTION RATIO (CMRR) is a measure of how well in-phase signals common to both input pins are rejected.

To calculate CMRR, the change in output offset is measured while the common mode input voltage is changed from 2V to 3V.

CMRR = 20 LOG (Δ Common Input / Δ Output Offset) (1)

CONVERSION TIME is the time required, after the input voltage is acquired, for the ADC to convert the input voltage to a digital word.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DUTY CYCLE is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the SCLK.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD − 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It is the difference between Positive Full-Scale Error and Negative Full-Scale Error and can be calculated as:

Gain Error = Positive Full-Scale Error − Negative Full-Scale Error (2)

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from ½ LSB below the first code transition through ½ LSB above the last code transition. The deviation of any given code from this straight line is measured from the center of that code value.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC141S626 is guaranteed not to have any missing codes.

NEGATIVE FULL-SCALE ERROR is the difference between the differential input voltage at which the output code transitions from negative full scale to the next code and $-V_{REF}$ + 1 LSB

NEGATIVE GAIN ERROR is the difference between the negative full-scale error and the offset error.

OFFSET ERROR is the difference between the differential input voltage at which the output code transitions from code 0000h to 0001h and 1 LSB.

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POSITIVE FULL-SCALE ERROR is the difference between the differential input voltage at which the output code transitions to positive full scale and V_{REF} minus 1 LSB.

POSITIVE GAIN ERROR is the difference between the positive full-scale error and the offset error.

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well a change in the analog supply voltage is rejected. PSRR is calculated from the ratio of the change in offset error for a given change in supply voltage, expressed in dB. For the ADC141S626, V_A is changed from 4.5V to 5.5V.

$$PSRR = 20 \text{ LOG } (\Delta \text{Output Offset} / \Delta V_A) \quad (3)$$

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below one-half the sampling frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the desired signal amplitude to the amplitude of the peak spurious spectral component below one-half the sampling frequency, where a spurious spectral component is any signal present in the output spectrum that is not present at the input and may or may not be a harmonic.

TOTAL HARMONIC DISTORTION (THD) is the ratio of the rms total of the first five harmonic components at the output to the rms level of the input signal frequency as seen at the output, expressed in dB. THD is calculated as

$$THD = 20 \cdot \log_{10} \sqrt{\frac{A_{f2}^2 + \cdots + A_{f6}^2}{A_{f1}^2}} \quad (4)$$

where A_{f1} is the RMS power of the input frequency at the output and A_{f2} through A_{f6} are the RMS power in the first 5 harmonic frequencies.

THROUGHPUT TIME is the minimum time required between the start of two successive conversion.

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Typical Performance Characteristics

$V_A = V_{IO} = V_{REF} = +5V$, $f_{SCLK} = 4.5$ MHz, $f_{SAMPLE} = 250$ kSPS, $T_A = +25°C$, and $f_{IN} = 20$ kHz unless otherwise stated.

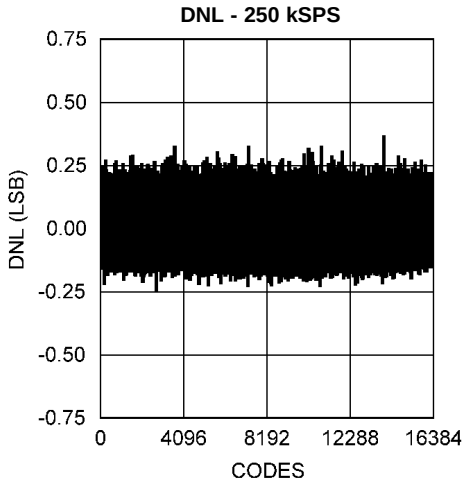


Figure 7.

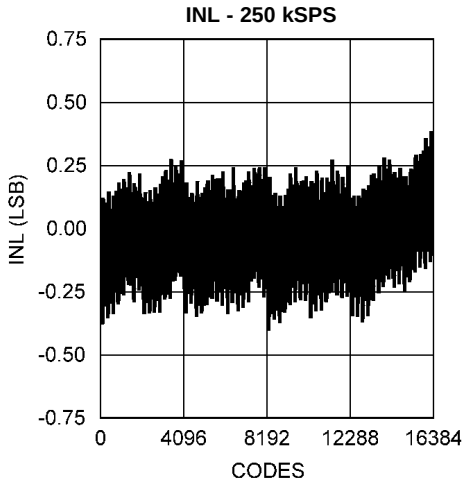


Figure 8.

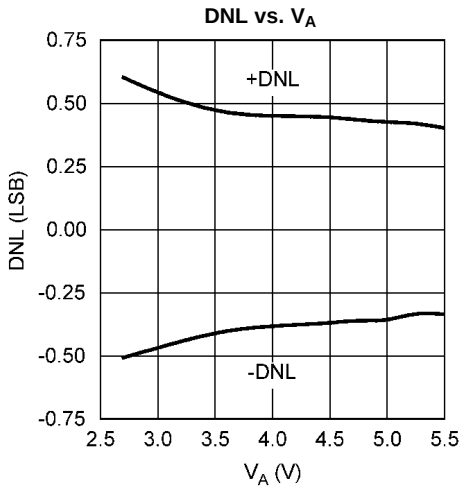


Figure 9.

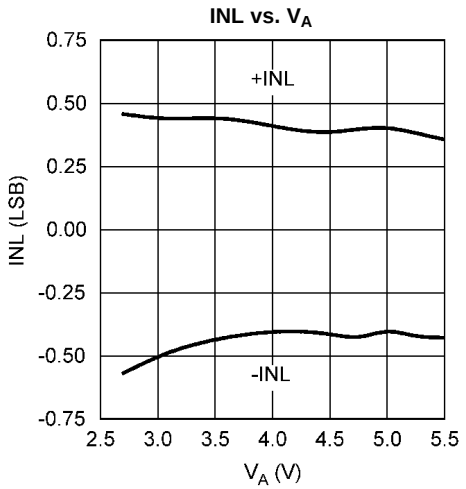


Figure 10.

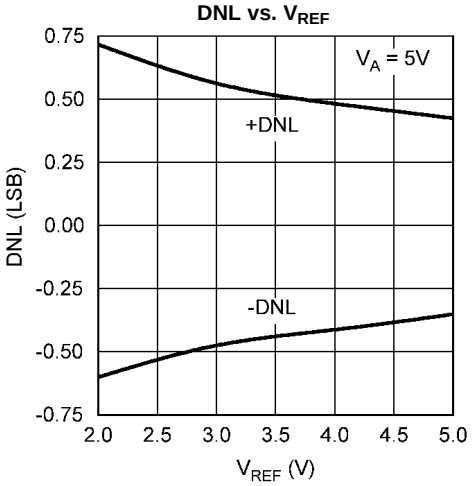


Figure 11.

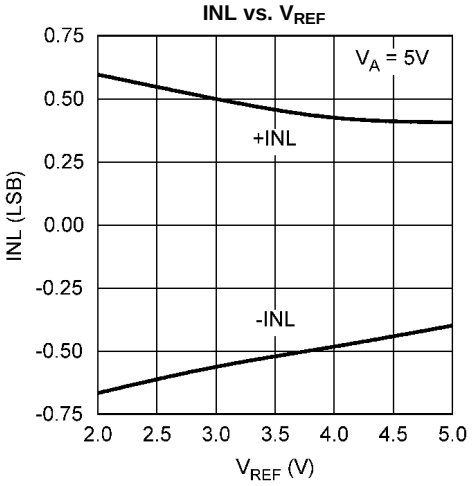


Figure 12.

Typical Performance Characteristics (continued)

$V_A = V_{IO} = V_{REF} = +5V$, $f_{SCLK} = 4.5$ MHz, $f_{SAMPLE} = 250$ kSPS, $T_A = +25°C$, and $f_{IN} = 20$ kHz unless otherwise stated.

DNL vs. SCLK FREQUENCY

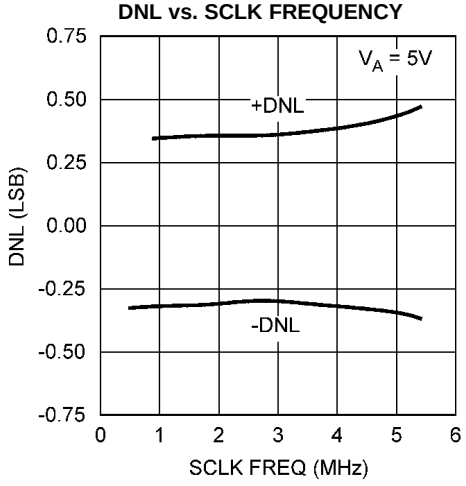


Figure 13.

INL vs. SCLK FREQUENCY

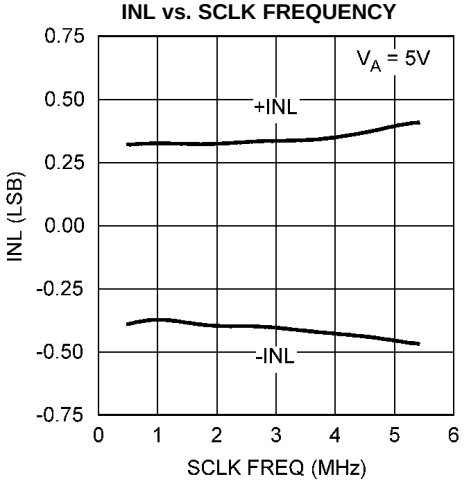


Figure 14.

DNL vs. TEMPERATURE

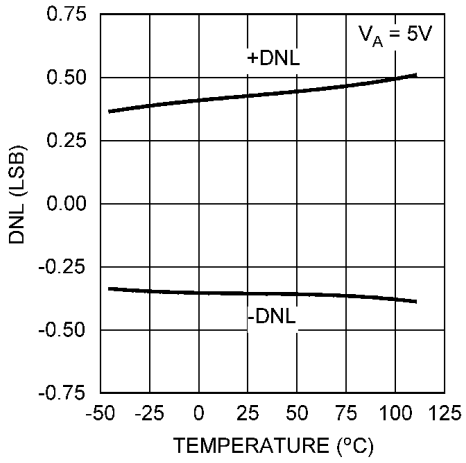


Figure 15.

INL vs. TEMPERATURE

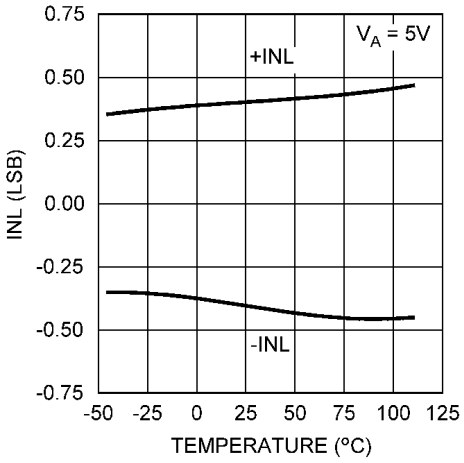


Figure 16.

SINAD vs. V_A

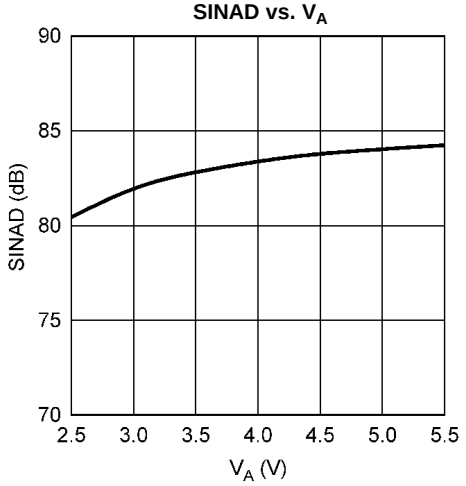


Figure 17.

THD vs. V_A

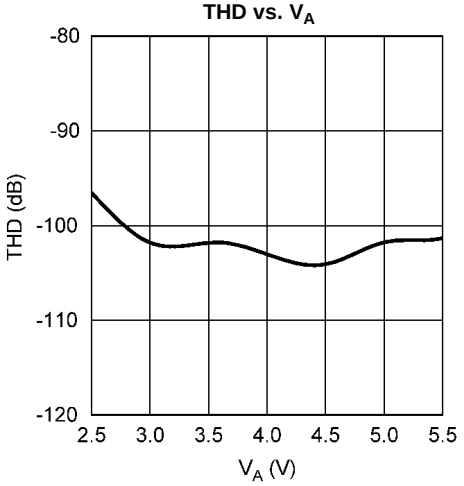


Figure 18.

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Typical Performance Characteristics (continued)

$V_A = V_{IO} = V_{REF}$ = +5V, f_{SCLK} = 4.5 MHz, f_{SAMPLE} = 250 kSPS, T_A = +25°C, and f_{IN} = 20 kHz unless otherwise stated.

SINAD vs. V_{REF}

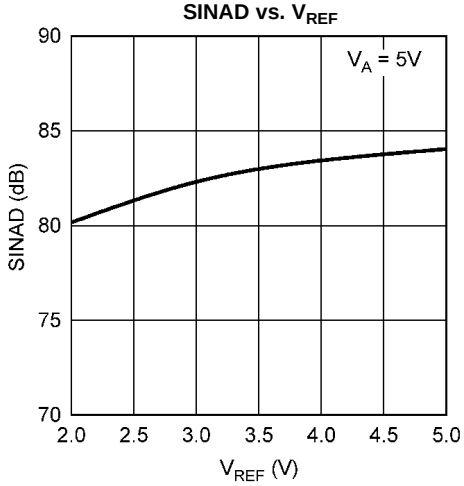


Figure 19.

THD vs. V_{REF}

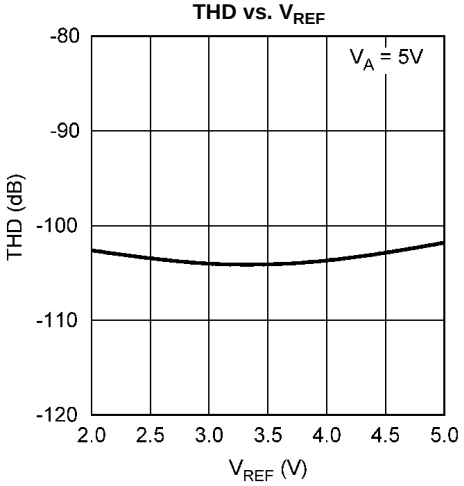


Figure 20.

SINAD vs. SCLK FREQUENCY

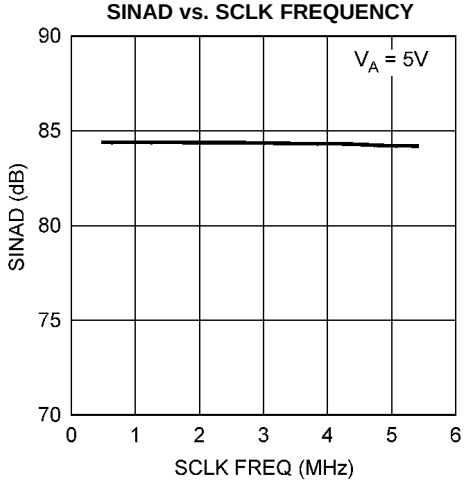


Figure 21.

THD vs. SCLK FREQUENCY

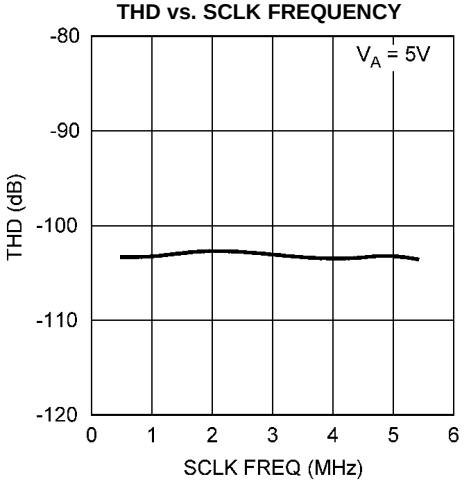


Figure 22.

SINAD vs. INPUT FREQUENCY

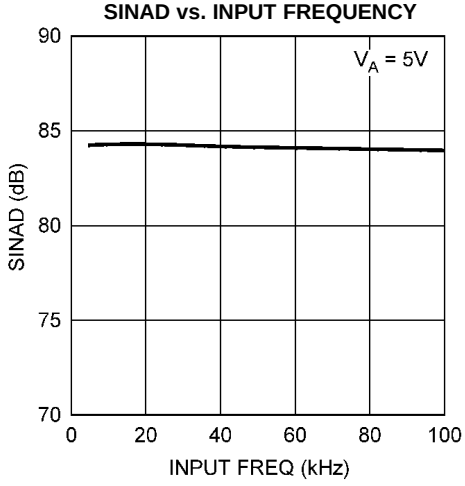


Figure 23.

THD vs. INPUT FREQUENCY

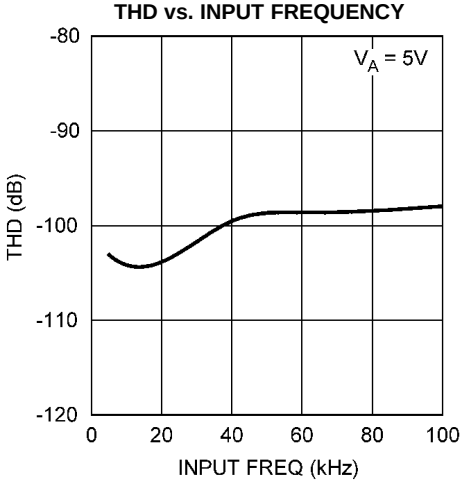


Figure 24.

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Typical Performance Characteristics (continued)

$V_A = V_{IO} = V_{REF}$ = +5V, f_{SCLK} = 4.5 MHz, f_{SAMPLE} = 250 kSPS, T_A = +25°C, and f_{IN} = 20 kHz unless otherwise stated.

SINAD vs. TEMPERATURE

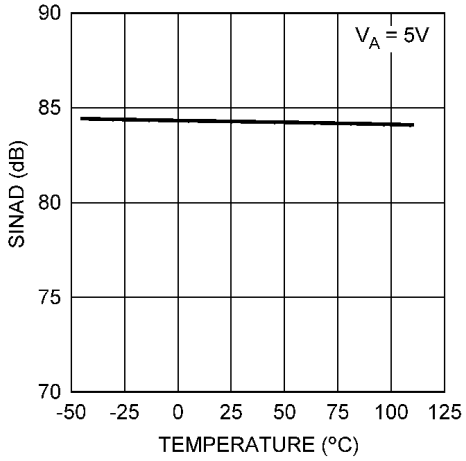


Figure 25.

THD vs. TEMPERATURE

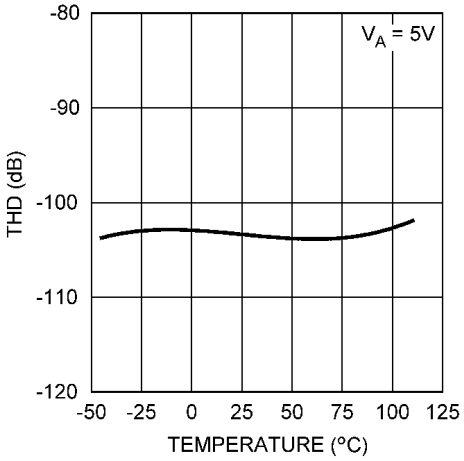


Figure 26.

V_A CURRENT vs. V_A

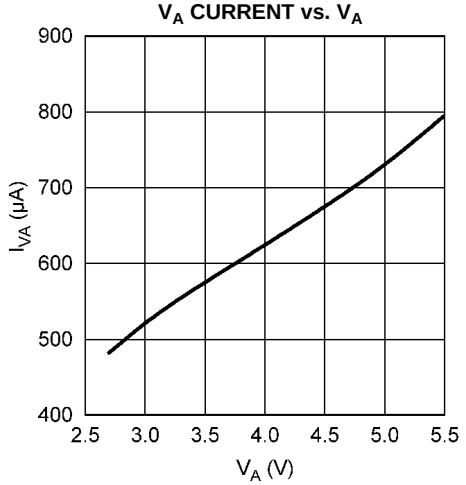


Figure 27.

V_A CURRENT vs. SCLK FREQUENCY

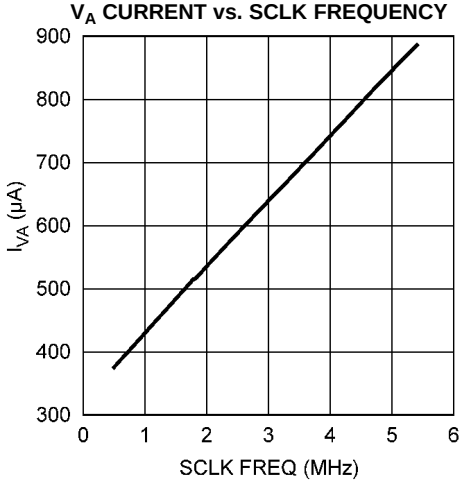


Figure 28.

V_A CURRENT vs. TEMPERATURE

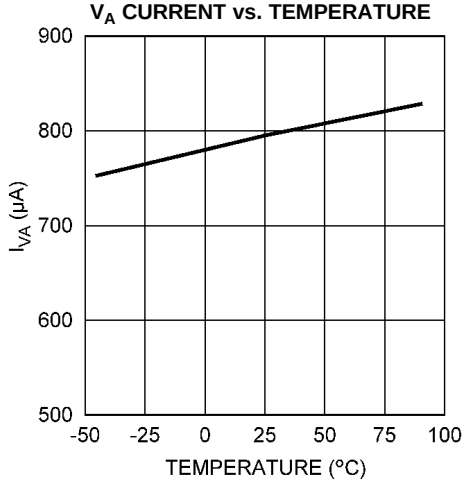


Figure 29.

V_{REF} CURRENT vs. V_{REF}

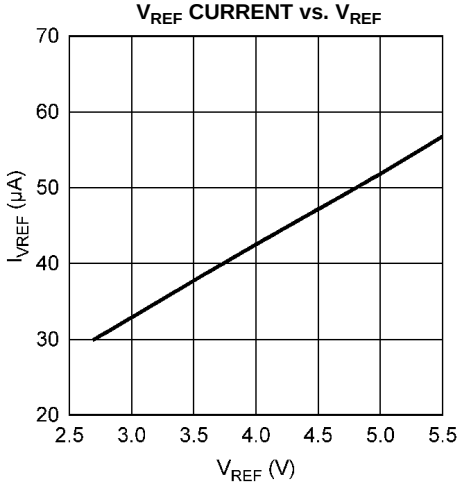


Figure 30.

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Typical Performance Characteristics (continued)

$V_A = V_{IO} = V_{REF} = +5V$, $f_{SCLK} = 4.5$ MHz, $f_{SAMPLE} = 250$ kSPS, $T_A = +25°C$, and $f_{IN} = 20$ kHz unless otherwise stated.

V_{REF} CURRENT vs. SCLK FREQUENCY

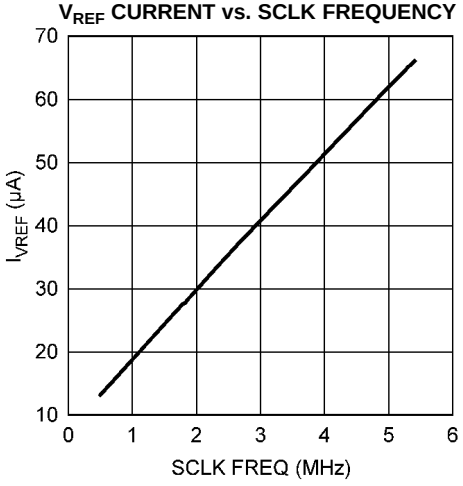


Figure 31.

V_{REF} CURRENT vs. TEMPERATURE

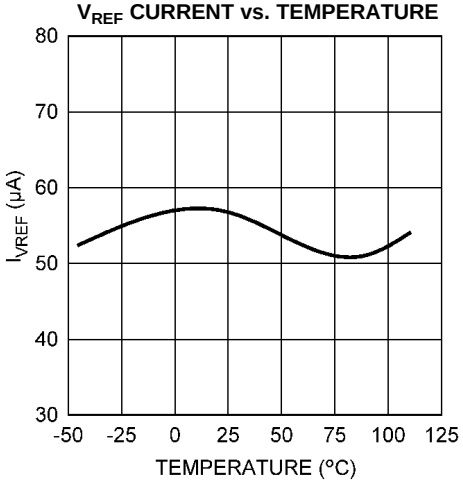


Figure 32.

V_{IO} CURRENT vs. V_{IO}

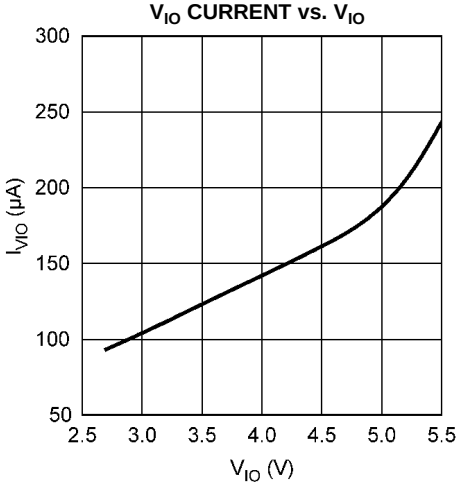


Figure 33.

V_{IO} CURRENT vs. SCLK FREQUENCY

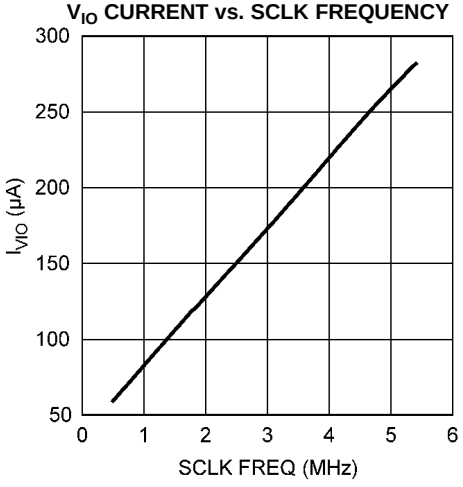


Figure 34.

V_{IO} CURRENT vs. TEMPERATURE

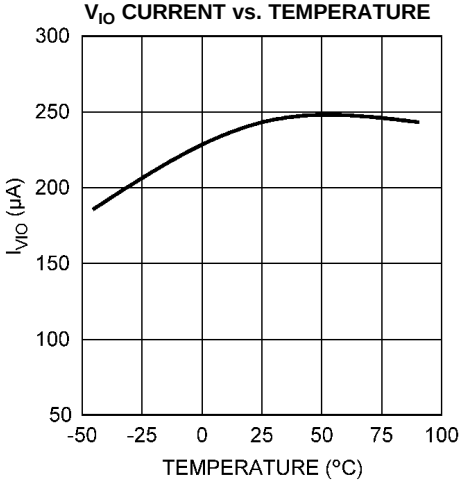


Figure 35.

SPECTRAL RESPONSE - 250 kSPS

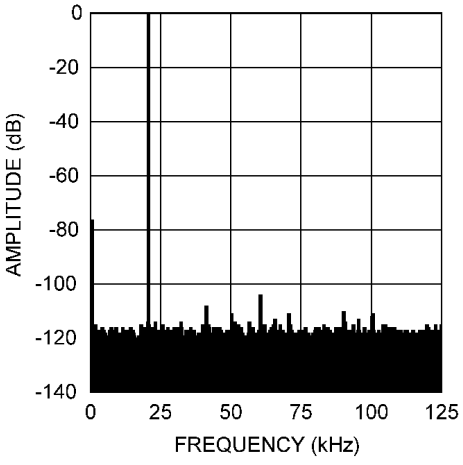


Figure 36.

FUNCTIONAL DESCRIPTION

The ADC141S626 is a 14-bit, 50 kSPS to 250 kSPS sampling Analog-to-Digital (A/D) converter. The converter uses a successive approximation register (SAR) architecture based upon capacitive redistribution containing an inherent sample-and-hold function. The differential nature of the analog inputs is maintained from the internal sample-and-hold circuits throughout the A/D converter to provide excellent common-mode signal rejection.

The ADC141S626 operates from independent analog and digital supplies. The analog supply (V_A) can range from 2.7V to 5.5V and the digital input/output supply (V_{IO}) can range from 2.7V to 5.5V. The ADC141S626 utilizes an external reference (V_{REF}), which can be any voltage between 1V and V_A. The value of V_{REF} determines the range of the analog input, while the reference input current (I_{REF}) depends upon the conversion rate.

The analog input is presented to two input pins: +IN and –IN. Upon initiation of a conversion, the differential input at these pins is sampled on the internal capacitor array. The inputs are disconnected from the internal circuitry while a conversion is in progress. The ADC141S626 features a zero-power track mode where the ADC is consuming the minimum amount of supply current while the internal sampling capacitor is tracking the applied analog input voltage. Zero-power track mode is exercised by bringing chip select bar ($\overline{CS}$) high or low after the conversion is complete (after the 16^{th} falling edge of the serial clock).

The ADC141S626 communicates with other devices via Serial Peripheral Interface (SPI™) , a synchronous serial interface that operates using three pins: chip select bar ($\overline{CS}$), serial clock (SCLK), and serial data out (D_{OUT}). The external SCLK controls data transfer and serves as the conversion clock. The duty cycle of SCLK is essentially unimportant, provided the minimum clock high and low times are met. The minimum SCLK frequency is set by internal capacitor leakage. Each conversion requires 18 SCLK cycles to complete. If less than 14 bits of conversion data are required, $\overline{CS}$ can be brought high at any point during the conversion. This procedure of terminating a conversion prior to completion is commonly referred to as short cycling.

The digital conversion result is clocked out by the SCLK input and is provided serially, most significant bit (MSB) first, at the D_{OUT} pin. The digital data that is provided at the D_{OUT} pin is that of the conversion currently in progress and thus there is no pipe line delay.

REFERENCE INPUT (V_{REF})

The externally supplied reference voltage (V_{REF}) sets the analog input range. The ADC141S626 will operate with V_{REF} in the range of 1V to V_A.

Operation with V_{REF} below 1V is also possible with slightly diminished performance. As V_{REF} is reduced, the range of acceptable analog input voltages is reduced. Assuming a proper common-mode input voltage (V_{CM}), the differential peak-to-peak input range is limited to (2 x V_{REF}). See Input Common Mode Voltage for more details.

Reducing V_{REF} also reduces the size of the least significant bit (LSB). The size of one LSB is equal to [(2 x V_{REF}) / 2^n], which is 16,384 where n is 14 bits. When the LSB size goes below the noise floor of the ADC141S626, the noise will span an increasing number of codes and overall performance will suffer. For example, dynamic signals will have their SNR degrade, while D.C. measurements will have their code uncertainty increase. Since the noise is Gaussian in nature, the effects of this noise can be reduced by averaging the results of a number of consecutive conversions.

Additionally, since offset and gain errors are specified in LSB, any offset and/or gain errors inherent in the A/D converter will increase in terms of LSB size as V_{REF} is reduced.

V_{REF} and analog inputs (+IN and -IN) are connected to the capacitor array through a switch matrix when the input is sampled. Hence, I_{REF}, I_{+IN}, and I_{-IN} are a series of transient spikes that occur at a frequency dependent on the operating sample rate of the ADC141S626.

I_{REF} changes only slightly with temperature. See Figure 31 and Figure 32 in Typical Performance Characteristics for additional details.

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ANALOG SIGNAL INPUTS

The ADC141S626 has a differential input where the effective input voltage that is digitized is (+IN) − (−IN). By using this differential input, small signals common to both inputs are rejected. As shown in Figure 37, noise is immune at low frequencies where the common-mode rejection ratio (CMRR) is 90 dB. As the frequency increases to 1 MHz, the CMRR rolls off to 40 dB . In general, operation with a fully differential input signal or voltage will provide better performance than with a single-ended input. However, if desired, the ADC141S626 can be presented with a single-ended input.

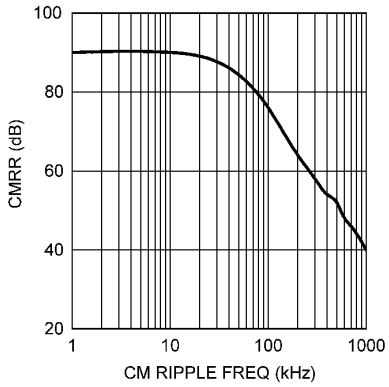


Figure 37. Analog Input CMRR vs. Frequency

The current required to recharge the input sampling capacitor will cause voltage spikes at +IN and −IN. Do not try to filter out these noise spikes. Rather, ensure that the transient settles out during the acquisition period.

Differential Input Operation

As shown in Figure 38 for a fully differential input signal, a positive full scale output code (01 1111 1111 1111b or 1FFFh or 8191d) will be obtained when (+IN) − (−IN) is greater than or equal to (V_{REF} − 1 LSB). A negative full scale code (10 0000 0000 0000b or 2000h or -8192d) will be obtained when (+IN) − (−IN) is less than or equal to (−V_{REF} + 1 LSB). This ignores gain, offset and linearity errors, which will affect the exact differential input voltage that will determine any given output code. Both inputs should be biased at a common mode voltage (V_{CM}), which will be thoroughly discussed in Input Common Mode Voltage . Figure 39 shows the ADC141S626 being driven by a full-scale differential source.

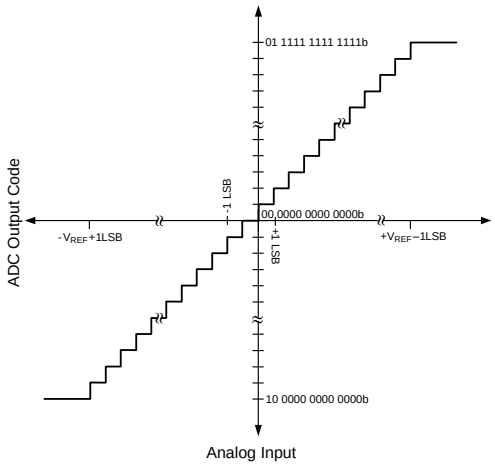


Figure 38. ADC Output vs. Input for a Differential Input Operation

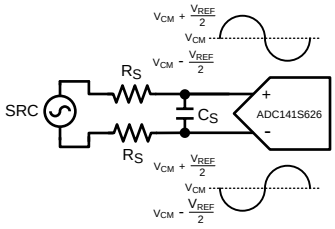


Figure 39. Differential Input

Single-Ended Input Operation

For single-ended operation, the non-inverting input (+IN) of the ADC141S626 can be driven with a signal that has a peak-to-peak range that is equal to or less than (2 x V_{REF}). The inverting input (−IN) should be biased at a stable V_{CM} that is halfway between these maximum and minimum values. In order to utilize the entire dynamic range of the ADC141S626, V_{REF} is limited to V_A / 2. This allows +IN a maximum swing range of ground to V_A. Figure 40 shows the ADC141S626 being driven by a full-scale single-ended source.

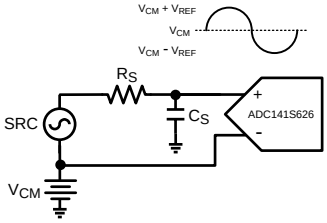


Figure 40. Single-Ended Input

Since the design of the ADC141S626 is optimized for a differential input, the performance degrades slightly when driven with a single-ended input. Linearity characteristics such as INL and DNL typically degrade by 0.1 LSB and dynamic characteristics such as SINAD typically degrade by 2 dB. Note that single-ended operation should only be used if the performance degradation (compared with differential operation) is acceptable.

Input Common Mode Voltage

The allowable input common mode voltage (V_{CM}) range depends upon V_A and V_{REF} used for the ADC141S626. The ranges of V_{CM} are depicted in Figure 41 and Figure 42. Note that these figures only apply to a V_A of 5V. Equations for calculating the minimum and maximum V_{CM} for differential and single-ended operations are shown in Table 1.

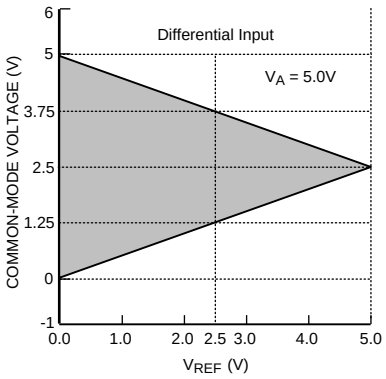


Figure 41. V_{CM} range for Differential Input operation

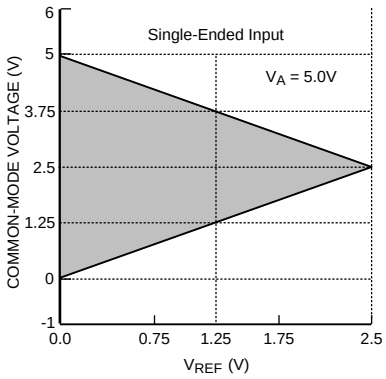


Figure 42. V_{CM} range for single-ended operation

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Table 1. Allowable V_{CM} Range

Input Signal	Minimum V_{CM}	Maximum V_{CM}
Differential	V_{REF} / 2	$V_A - V_{REF}$ / 2
Single-Ended	V_{REF}	$V_A - V_{REF}$

SERIAL DIGITAL INTERFACE

The ADC141S626 communicates via a synchronous 3-wire serial interface as shown in Figure 1 or re-shown in Figure 43 for convenience. $\overline{CS}$, chip select bar, initiates conversions and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. D_{OUT} is the serial data output pin, where a conversion result is sent as a serial data stream, MSB first.

A serial frame is initiated on the falling edge of $\overline{CS}$ and ends on the rising edge of $\overline{CS}$. The ADC141S626's D_{OUT} pin is in a high impedance state when $\overline{CS}$ is high and is active when $\overline{CS}$ is low; thus. $\overline{CS}$ acts as an output enable.

The ADC141S626 samples the differential input upon the assertion of $\overline{CS}$. Assertion is defined as bringing the $\overline{CS}$ pin to a logic low state. For the first 15 periods of the SCLK following the assertion of $\overline{CS}$, the ADC141S626 is converting the analog input voltage. On the 16th falling edge of SCLK, the ADC141S626 enters acquisition (t_{ACQ}) mode. For the next three periods of SCLK, the ADC141S626 is operating in acquisition mode where the ADC input is tracking the analog input signal applied across +IN and -IN. During acquisition mode, the ADC141S626 is consuming a minimal amount of power.

The ADC141S626 can enter conversion mode (t_{CONV}) under three different conditions. The first condition involves $\overline{CS}$ going low (asserted) with SCLK high. In this case, the ADC141S626 enters conversion mode on the first falling edge of SCLK after $\overline{CS}$ is asserted. In the second condition, $\overline{CS}$ goes low with SCLK low. Under this condition, the ADC141S626 automatically enters conversion mode and the falling edge of $\overline{CS}$ is seen as the first falling edge of SCLK. In the third condition, $\overline{CS}$ and SCLK go low simultaneously and the ADC141S626 enters conversion mode. While there is no timing restriction with respect to the falling edges of $\overline{CS}$ and SCLK, there is a minimum and maximum setup time requirements for the falling edge of $\overline{CS}$ with respect to the rising edge of SCLK. See Figure 3 in the Timing Diagrams section for more information.

$\overline{CS}$ Input

The $\overline{CS}$ (chip select bar) input is active low and is TTL and CMOS compatible. The ADC141S626 enters conversion mode when $\overline{CS}$ is asserted and the SCLK pin is in a logic low state. When $\overline{CS}$ is high, the ADC141S626 is always in acquisition mode and thus consuming the minimum amount of power. Since $\overline{CS}$ must be asserted to begin a conversion, the sample rate of the ADC141S626 is equal to the assertion rate of $\overline{CS}$.

Proper operation requires that the fall of $\overline{CS}$ not occur simultaneously with a rising edge of SCLK. If the fall of $\overline{CS}$ occurs during the rising edge of SCLK, the data might be clocked out one bit early. Whether or not the data is clocked out early depends upon how close the $\overline{CS}$ transition is to the SCLK transition, the device temperature, and the characteristics of the individual device. To ensure that the MSB is always clocked out at a given time (the 3rd falling edge of SCLK), it is essential that the fall of $\overline{CS}$ always meet the timing requirement specified in the Timing Specifications.

SCLK Input

The SCLK (serial clock) is used as the conversion clock to shift out the conversion result. SCLK is TTL and CMOS compatible. Internal settling time requirements limit the maximum clock frequency while internal capacitor leakage limits the minimum clock frequency. The ADC141S626 offers guaranteed performance with the clock rates indicated in the Electrical Characteristics.

The ADC141S626 enters acquisition mode on the 16th falling edge of SCLK during a conversion frame. Assuming that the LSB is clocked into a controller on the 16th rising edge of SCLK, there is a minimum acquisition time period that must be met before a new conversion frame can begin. Other than the 16th rising edge of SCLK that was used to latch the LSB into a controller, there is no requirement for the SCLK to transition during acquisition mode. Therefore, it is acceptable to idle SCLK after the LSB has been latched into the controller.

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Data Output

The data output format of the ADC141S626 is two's complement as shown in Figure 38. This figure indicates the ideal output code for a given input voltage and does not include the effects of offset, gain error, linearity errors, or noise. Each data output bit is output on the falling edges of SCLK. The 1st and 2nd SCLK falling edges clock out leading zeros while the 3rd to 16th SCLK falling edges clock out the conversion result, MSB first.

While most receiving systems will capture the digital output bits on the rising edges of SCLK, the falling edges of SCLK may be used to capture the conversion result if the minimum hold time for D_{OUT} is acceptable. See Figure 6 for D_{OUT} hold (t_{DH}) and access (t_{DA}) times.

D_{OUT} is enabled on the falling edge of $\overline{CS}$ and disabled on the rising edge of $\overline{CS}$. If $\overline{CS}$ is raised prior to the 16th falling edge of SCLK, the current conversion is aborted and D_{OUT} will go into its high impedance state. A new conversion will begin when $\overline{CS}$ is driven LOW.

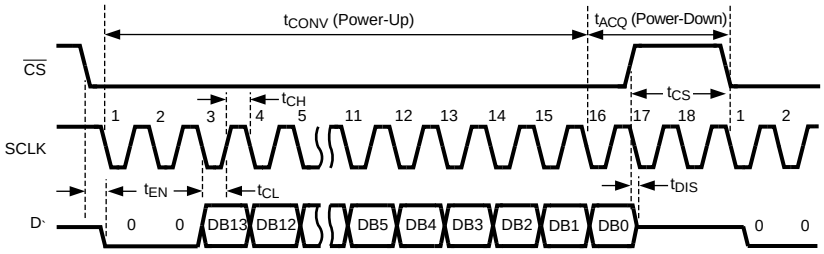


Figure 43. ADC141S626 Single Conversion Timing Diagram

Applications Information

OPERATING CONDITIONS

We recommend that the following conditions be observed for operation of the ADC141S626:

$-40°C \le T_A \le +85°C$

$+2.7V \le V_A \le +5.5V$

$+2.7V \le V_{IO} \le +5.5V$

$1V \le V_{REF} \le V_A$

$0.9\ MHz \le f_{SCLK} \le 4.5\ MHz$

V_{CM}: See Input Common Mode Voltage

POWER CONSUMPTION

The architecture, design, and fabrication process allow the ADC141S626 to operate at conversion rates up to 250 kSPS while consuming very little power. The ADC141S626 consumes the least amount of power while operating in acquisition (power-down) mode. For applications where power consumption is critical, the ADC141S626 should be operated in acquisition mode as often as the application will tolerate. To further reduce power consumption, stop the SCLK while $\overline{CS}$ is high.

Short Cycling

Short cycling refers to the process of halting a conversion after the last needed bit is outputted. Short cycling can be used to lower the power consumption in those applications that do not need a full 14-bit resolution, or where an analog signal is being monitored until some condition occurs. In some circumstances, the conversion could be terminated after the first few bits. This will lower power consumption in the converter since the ADC141S626 spends more time in acquisition mode and less time in conversion mode.

Short cycling is accomplished by pulling $\overline{CS}$ high after the last required bit is received from the ADC141S626 output. This is possible because the ADC141S626 places the latest converted data bit on D_{OUT} as it is generated. If only 10-bits of the conversion result are needed, for example, the conversion can be terminated by pulling $\overline{CS}$ high after the 10th bit has been clocked out.

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Burst Mode Operation

Normal operation of the ADC141S626 requires the SCLK frequency to be 18 times the sample rate and the $\overline{CS}$ rate to be the same as the sample rate. However, in order to minimize power consumption in applications requiring sample rates below 250 kSPS, the ADC141S626 should be run with an SCLK frequency of 4.5 MHz and a $\overline{CS}$ rate as slow as the system requires. When this is accomplished, the ADC141S626 is operating in burst mode. The ADC141S626 enters into acquisition mode at the end of each conversion, minimizing power consumption. This causes the converter to spend the longest possible time in acquisition mode. Since power consumption scales directly with conversion rate, minimizing power consumption requires determining the lowest conversion rate that will satisfy the requirements of the system.

PCB LAYOUT AND CIRCUIT CONSIDERATIONS

For best performance, care should be taken with the physical layout of the printed circuit board. This is especially true with a low V_{REF} or when the conversion rate is high. At high clock rates there is less time for settling, so it is important that any noise settles out before the conversion begins.

Analog and Digital Power Supplies

Any ADC architecture is sensitive to spikes on the power supply, reference, and ground pins. These spikes may originate from switching power supplies, digital logic, high power devices, and other sources. Power to the ADC141S626 should be clean and well bypassed. A 0.1 µF ceramic bypass capacitor and a 1 µF to 10 µF capacitor should be used to bypass the ADC141S626 supply, with the 0.1 µF capacitor placed as close to the ADC141S626 package as possible.

Since the ADC141S626 has both the V_A and V_{IO} pins, the user has three options on how to connect these pins. The first option is to tie V_A and V_{IO} together and power them with the same power supply. This is the most cost effective way of powering the ADC141S626 but is also the least ideal. As stated previously, noise from V_{IO} can couple into V_A and adversely affect performance. The other two options involve the user powering V_A and V_{IO} with separate supply voltages. These supply voltages can have the same amplitude or they can be different. They may be set independent of each other to any value between 2.7V and 5.5V.

Best performance will typically be achieved with V_A operating at 5V and V_{IO} at 3V. Operating V_A at 5V offers the best linearity and dynamic performance when V_{REF} is also set to 5V; while operating V_{IO} at 3V reduces the power consumption of the digital logic. Operating the digital interface at 3V also has the added benefit of decreasing the noise created by charging and discharging the capacitance of the digital interface pins.

Voltage Reference

The reference source must have a low output impedance and needs to be bypassed with a minimum capacitor value of 0.1 µF. A larger capacitor value of 1 µF to 10 µF placed in parallel with the 0.1 µF is preferred. While the ADC141S626 draws very little current from the reference on average, there are higher instantaneous current spikes at the reference.

V_{REF} of the ADC141S626, like all A/D converters, does not reject noise or voltage variations. Keep this in mind if V_{REF} is derived from the power supply. Any noise and/or ripple from the supply that is not rejected by the external reference circuitry will appear in the digital results. The use of an active reference source is recommended. The LM4040 and LM4050 shunt reference families and the LM4132 and LM4140 series reference families are excellent choices for a reference source.

PCB Layout

Capacitive coupling between the noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry and the clock line as short as possible. Digital circuits create substantial supply and ground current transients. The logic noise generated could have significant impact upon system noise performance. To avoid performance degradation of the ADC141S626 due to supply noise, avoid using the same supply for the V_A and V_{REF} of the ADC141S626 that is used for digital circuitry on the board.

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Generally, analog and digital lines should cross each other at 90° to avoid crosstalk. However, to maximize accuracy in high resolution systems, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. In addition, the clock line should also be treated as a transmission line and be properly terminated. The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference input pin and ground should be connected to a very clean point in the ground plane.

A single, uniform ground plane and the use of split power planes are recommended. The power planes should be located within the same board layer. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed over the analog power plane. All digital circuitry should be placed over the digital power plane. Furthermore, the GND pins on the ADC141S626 and all the components in the reference circuitry and input signal chain that are connected to ground should be connected to the ground plane at a quiet point. Avoid connecting these points too close to the ground point of a microprocessor, microcontroller, digital signal processor, or other high power digital device.

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APPLICATION CIRCUITS

The following figures are examples of the ADC141S626 in typical application circuits. These circuits are basic and will generally require modification for specific circumstances.

Data Acquisition

Figure 44 shows a typical connection diagram for the ADC141S626 operating at V_A of +5V. V_{REF} is connected to a 4.1V shunt reference, the LM4040-4.1, to define the analog input range of the ADC141S626 independent of supply variation on the +5V supply line. The V_{REF} pin should be de-coupled to the ground plane by a 0.1 µF ceramic capacitor and a tantalum capacitor of 10 µF. It is important that the 0.1 µF capacitor be placed as close as possible to the V_{REF} pin while the placement of the tantalum capacitor is less critical. It is also recommended that the V_A and V_{IO} pins of the ADC141S626 be de-coupled to ground by a 0.1 µF ceramic capacitor in parallel with a 10 µF tantalum capacitor.

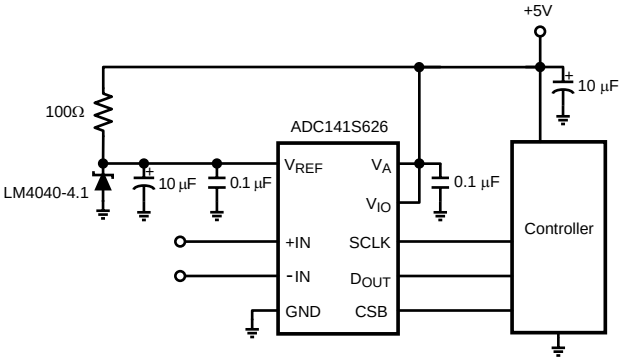


Figure 44. Low cost, low power Data Acquisition System

Bridge Sensor Application

Figure 45 shows an example of interfacing a bridge sensor to the ADC141S626. The application assumes that the bridge sensor requires buffering and amplification to fully utilize the dynamic range of the ADC and thus optimize the performance of the entire signal path. The amplification stage consists of the LMP7702, a dual precision amplifier, and some gain setting passive components. The amplification stage offers the benefit of high input impedance and high amplification capability. On the other hand, it offers no common-mode rejection of common-mode noise or DC-voltage coming from the bridge sensor.

The DAC081S101, a digital-to-analog converter (DAC), is used to bias the bridge sensor. The DAC provides a mean for dynamically adjusting the gain of the bridge sensor relative to actual maximum and minimum output conditions. Another option for biasing the bridge sensor would be powering it from the same +5V power supply voltage as the V_A pin on the ADC141S626. This option has the benefit of providing the ideal common-mode input voltage for the ADC141S626 while keeping design complexity and cost to a minimum. However, any fluctuation in the +5V supply will still be visible in the converted result. The LM4132-4.1, a 4.1V series reference, is used as the reference voltage in the application. The ADC141S626, DAC081S101, and the LM4132-4.1 are all powered from the same +5V voltage source.

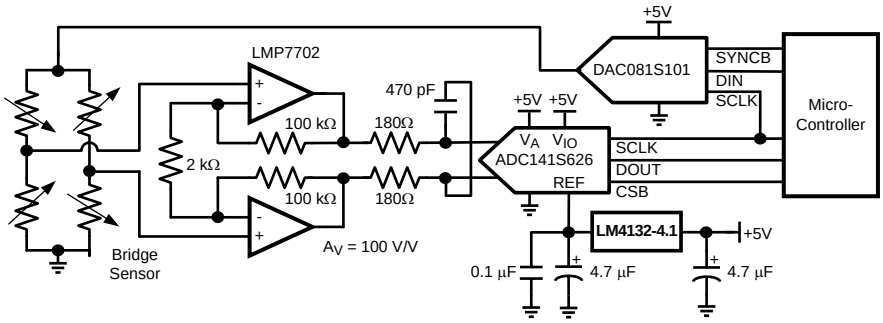


Figure 45. Interfacing the ADC141S626 to a Bridge Sensor

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Current Sensing Application

Figure 46 shows an example of interfacing a current transducer to the ADC141S626. The current transducer converts an input current into a voltage that is converted by the ADC. Since the output voltage of the current transducer is single-ended and centered around a common-mode voltage (V_{CM}) of 2.5V, the ADC141S626 is configured with the output of the transducer driving the non-inverting input and V_{CM} of the transducer driving the inverting input. The output of the transducer has an output range of ±2V around V_{CM} of 2.5V. As a result, a series reference voltage of 2.0V is connected to the ADC141S626. This will allow all of the codes of the ADC141S626 to be available for the application. This configuration of the ADC141S626 is referred to as a single-ended application of a differential ADC. All of the elements in the application are conveniently powered by the same +5V power supply, keeping circuit complexity and cost to a minimum.

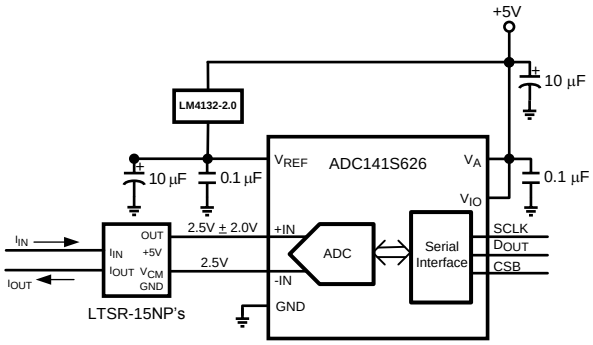


Figure 46. Interfacing the ADC141S626 to a Current Transducer

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REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	22

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC141S626CIMM/NO.A	Active	Production	VSSOP (DGS) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X94C
ADC141S626CIMM/NOPB	Active	Production	VSSOP (DGS) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X94C
ADC141S626CIMMX/NO.A	Active	Production	VSSOP (DGS) | 10	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X94C
ADC141S626CIMMX/NO.B	Active	Production	VSSOP (DGS) | 10	3500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
ADC141S626CIMMX/NOPB	Active	Production	VSSOP (DGS) | 10	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X94C

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

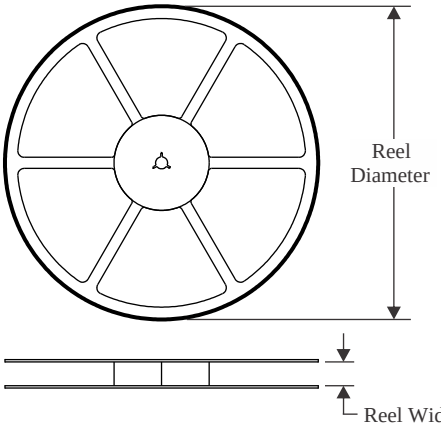
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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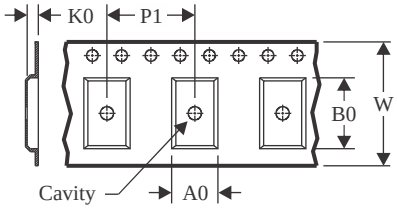
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

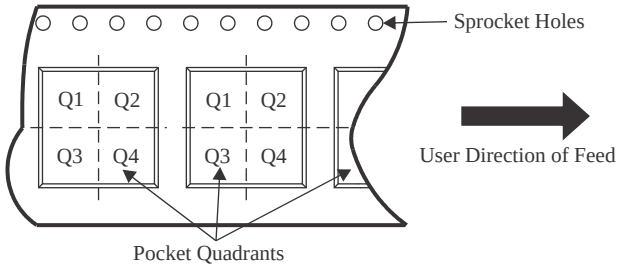


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

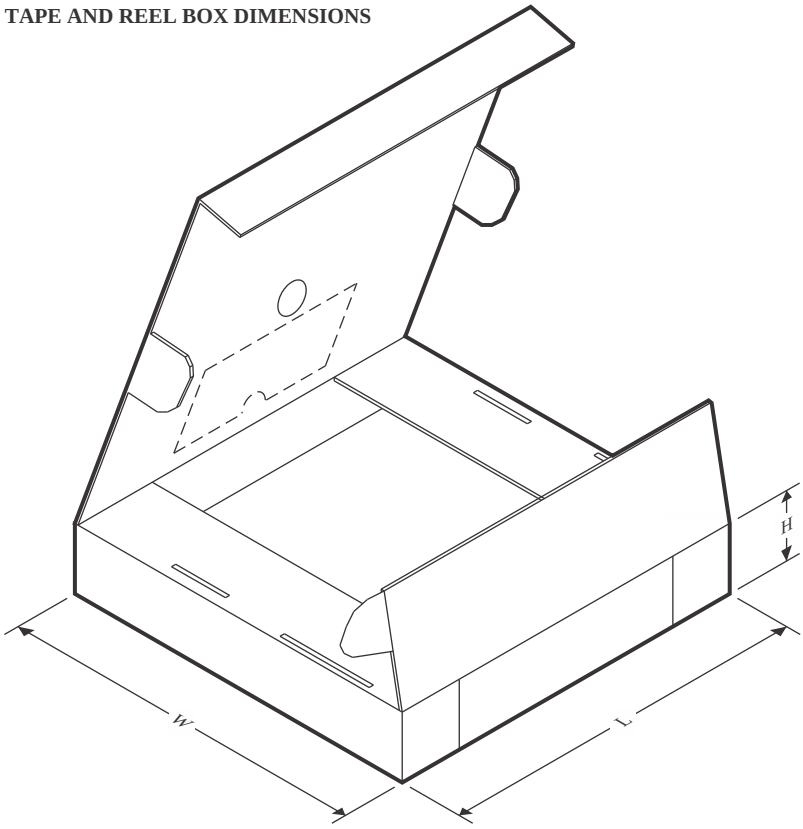
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC141S626CIMM/NOPB	VSSOP	DGS	10	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADC141S626CIMMX/ NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC141S626CIMM/NOPB	VSSOP	DGS	10	1000	210.0	185.0	35.0
ADC141S626CIMMX/ NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0

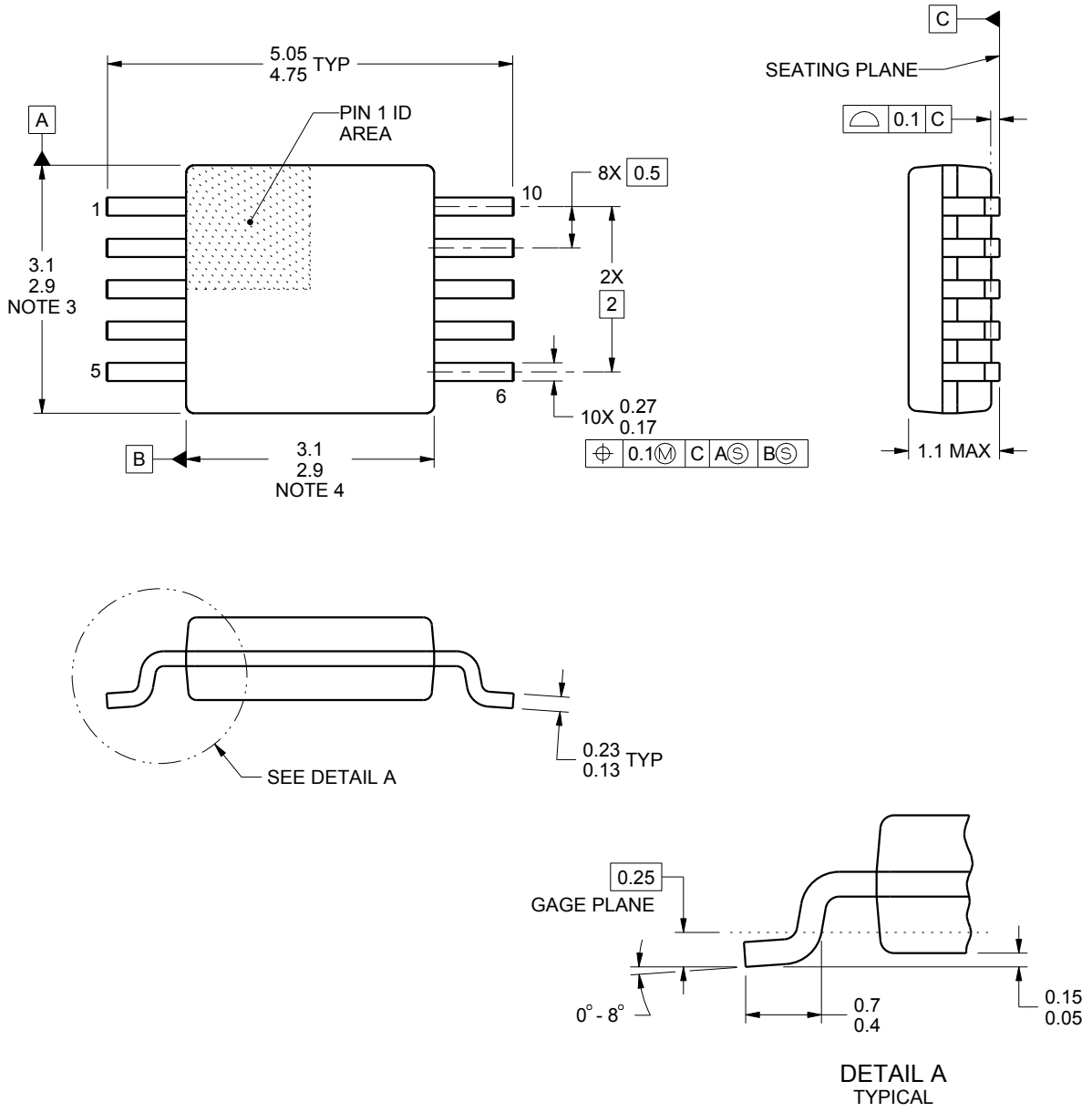


PACKAGE OUTLINE

DGS0010A

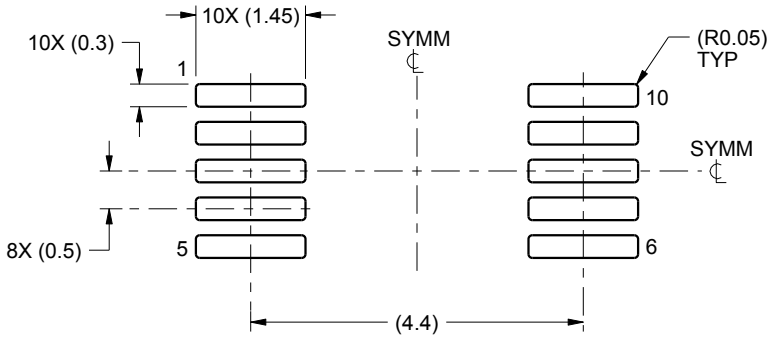
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

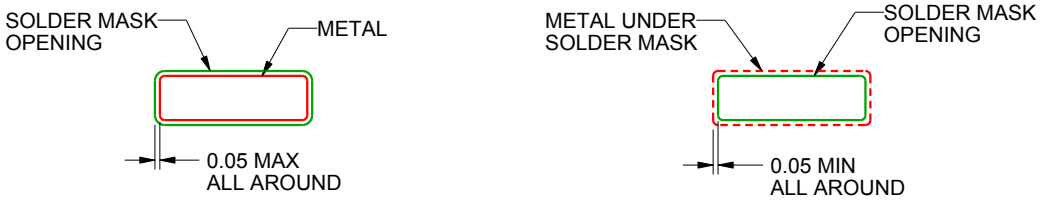


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

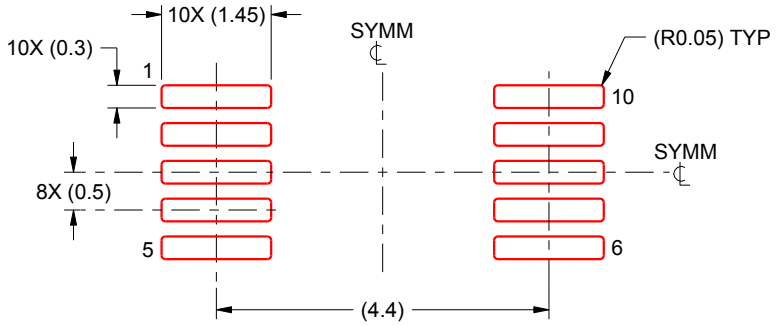


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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