45.0 dBm (35 W), 4.8 GHz to 6.0 GHz, GaN Power Amplifier

Data Sheet **ADPA1107**

FEATURES

P_{OUT} with P_{IN} = 27.0 dBm: 45.0 dBm typical at 5.4 GHz to 6.0 GHz
Small signal gain: 30.5 dB typical at 4.8 GHz to 5.4 GHz
Frequency range: 4.8 GHz to 6.0 GHz
PAE with P_{IN} = 27.0 dBm: 56.5% typical at 5.4 GHz to 6.0 GHz
V_{DD}: 28 V at I_{DQ} = 350 mA with a 10% duty cycle
40-lead, 6 mm × 6 mm, LFCSP

APPLICATIONS

Weather radars
Marine radars
Military radars

FUNCTIONAL BLOCK DIAGRAM

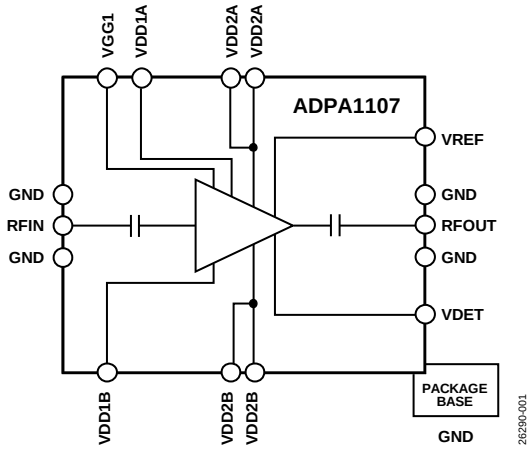


Figure 1.

GENERAL DESCRIPTION

The ADPA1107 is a gallium nitride (GaN), broadband power amplifier, delivering 45.0 dBm (35 W) with 56.5% typical power added efficiency (PAE) across a bandwidth of 4.8 GHz to 6.0 GHz. The ADPA1107 provides ±0.5 dB gain flatness from 5.4 GHz to 6.0 GHz.

The ADPA1107 is ideal for pulsed applications such as radar, public mobile radio, and general-purpose amplification.

The ADPA1107 is housed in a 40-lead, 6 mm × 6 mm, lead frame chip scale package (LFCSP).

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TABLE OF CONTENTS

Features 1
Applications 1
Functional Block Diagram 1
General Description 1
Revision History 2
Specifications 3
Electrical Specifications 3
Absolute Maximum Ratings 5
Thermal Resistance 5
Electrostatic Discharge (ESD) Ratings 5
ESD Caution 5
Pin Configuration and Function Descriptions 6
Interface Schematics 7
Typical Performance Characteristics 8
Theory of Operation 16
Applications Information 17
Basic Connections 17
Thermal Management 19
Outline Dimensions 20
Ordering Guide 20

REVISION HISTORY

7/2021—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

Base temperature (T_{BASE}) = 25°C, supply voltage (V_{DD}) = 28 V, quiescent current (I_{DQ}) = 350 mA, pulse width = 100 µs, 10% duty cycle, and frequency range = 4.8 GHz to 5.4 GHz, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	4.8		5.4	GHz	
GAIN					
Small Signal Gain	28.0	30.5		dB	
Gain Flatness		±1.3		dB	
RETURN LOSS					
Input		16.0		dB	
Output		13.5		dB	
POWER					
Output Power (P_{OUT})					
Input Power (P_{IN}) = 25.0 dBm		45.5		dBm	
P_{IN} = 27.0 dBm	43.5	45.5		dBm	
Power Gain					
P_{IN} = 25.0 dBm		20.5		dB	
P_{IN} = 27.0 dBm	16.5	18.5		dB	
Power Added Efficiency (PAE)					
P_{IN} = 25.0 dBm		56.5		%	
P_{IN} = 27.0 dBm		55.0		%	
QUIESCENT CURRENT (I_{DQ})		350		mA	Adjust the gate control voltage (VGG1) between −4 V and −2 V to achieve an I_{DQ} = 350 mA typical

T_{BASE} = 25°C, V_{DD} = 28 V, I_{DQ} = 350 mA, pulse width = 100 µs, 10% duty cycle, and frequency range = 5.4 GHz to 6.0 GHz, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	5.4		6.0	GHz	
GAIN					
Small Signal Gain	27.0	29.5		dB	
Gain Flatness		±0.5		dB	
RETURN LOSS					
Input		7.5		dB	
Output		12.0		dB	
POWER					
P_{OUT}					
P_{IN} = 25.0 dBm		45.0		dBm	
P_{IN} = 27.0 dBm	43.0	45.0		dBm	
Power Gain					
P_{IN} = 25.0 dBm		20.3		dB	
P_{IN} = 27.0 dBm	16.0	18.0		dB	
PAE					
P_{IN} = 25.0 dBm		56.0		%	
P_{IN} = 27.0 dBm		56.5		%	
I_{DQ}		350		mA	Adjust the gate control voltage (VGG1) between −4 V and −2 V to achieve an I_{DQ} = 350 mA typical

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Drain Bias Voltage (V_{DD1A}, V_{DD1B}, V_{DD2A}, and V_{DD2B})	35 V dc
Negative Gate Bias Voltage (V_{GG1}), V_{DD} = 28 V (Nominal Drain Voltage)	−8 V dc to −1 V dc
RF Input Power (RFIN)	31 dBm
Drain and Gate Bias	
Pulse Width	1000 µs
Duty Cycle	40%
Maximum Pulsed Power Dissipation (P_{DISS})	
Drain Bias Pulse Width = 100 µs and T_{BASE} = 85°C	
At 10% Duty Cycle, Derate 581 mW/°C Above 85°C	81.4 W
At 40% Duty Cycle, Derate 538 mW/°C Above 85°C	75.2 W
Drain Bias Pulse Width = 1000 µs and T_{BASE} = 85°C	
At 10% Duty Cycle, Derate 459 mW/°C Above 85°C	64.2 W
Temperature	
Nominal Pulsed Peak Channel, T_{BASE} = 85°C, P_{IN} = 27 dBm	
Drain Bias Pulse Width = 100 µs	
P_{DISS} = 27.9 W at 5.4 GHz, and at 10% Duty Cycle	133°C
P_{DISS} = 29.2 W at 5.4 GHz and at 40% Duty Cycle	139.3°C
Drain Bias Pulse Width = 1000 µs	
P_{DISS} = 28.3 W at 5.4 GHz and at 10% Duty Cycle	146.7°C
Maximum Channel	225°C
Maximum Peak Reflow for Moisture Sensitivity Level (MSL) 3[1]	260°C
Storage Range	−60°C to +125°C
Operating Range	−40°C to +85°C

[1] See the Ordering Guide section.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Overall thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the channel to case thermal resistance (channel to exposed metal on the underside of the device).

Table 4. Thermal Resistance

Package Type[1]	θ_{JC}	Unit
CP-40-7		
Drain Bias Pulse Width = 100 µs at 10% Duty Cycle	1.72	°C/W
Drain Bias Pulse Width = 100 µs at 40% Duty Cycle	1.86	°C/W
Drain Bias Pulse Width = 1000 µs at 10% Duty Cycle	2.18	°C/W

[1] θ_{JC} was determined under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADPA1107

Table 5. ADPA1107, 40-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	500	1B

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

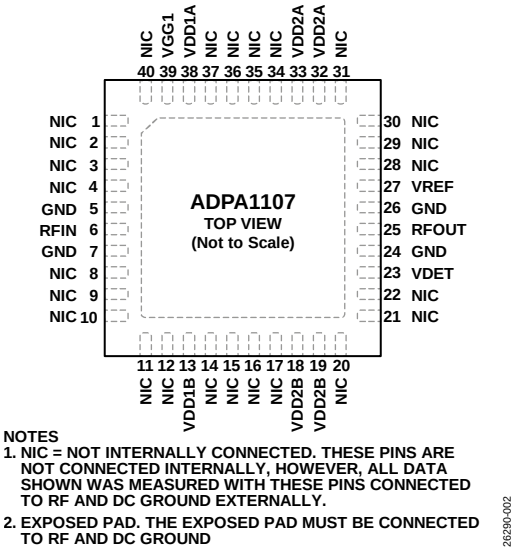


Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4, 8 to 12, 14 to 17, 20 to 22, 28 to 31, 34 to 37, 40	NIC	Not Internally Connected. These pins are not connected internally, however, all data shown was measured with the NIC pins connected to RF and dc ground externally.
5, 7, 24, 26	GND	The GND pins must be connected to RF and dc ground. See Figure 3 for the interface schematic.
6	RFIN	RF Input. The RFIN pin is ac-coupled and matched to 50 Ω. See Figure 4 for the interface schematic.
13, 38	VDD1B, VDD1A	Power Supply Voltage for the Amplifier. First stage drain bias. See Figure 4 for the interface schematic.
18, 19, 32, 33	VDD2B, VDD2A	Power Supply Voltage for the Amplifier. Second stage drain bias. See Figure 5 for the interface schematic.
23	VDET	Detector Diode to Measure RF Output Power. Output power detection via the VDET pin requires the application of a dc bias voltage through an external series resistor. Used in combination with the VREF pin, the difference voltage ($V_{REF} - V_{DET}$) is a temperature compensated dc voltage that is proportional to the RF output power. See Figure 5 for the interface schematic.
25	RFOUT	RF Output. The RFOUT pin is ac-coupled and matched to 50 Ω. See Figure 5 for the interface schematic.
27	VREF	Reference Diode for Temperature Compensation of VDET RF Output Power Measurements. See Figure 6 for the interface schematic.
39	VGG1	Gate Control Voltage Pin. See Figure 4 and Figure 5 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to RF and dc ground.

INTERFACE SCHEMATICS



Figure 3. GND Interface Schematic

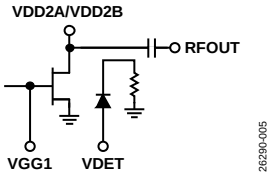


Figure 5. RFOUT, VGG1, VDD2A, VDD2B, and VDET Interface Schematic

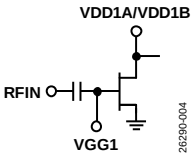


Figure 4. RFIN, VGG1, VDD1A, and VDD1B Interface Schematic

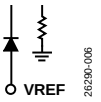


Figure 6. VREF Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

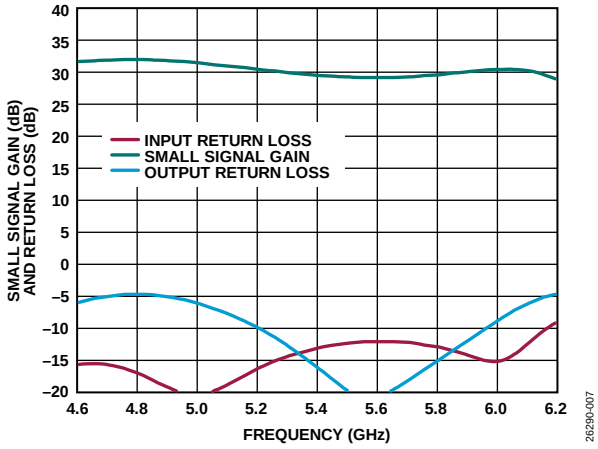


Figure 7. Small Signal Gain and Return Loss (Response) vs. Frequency

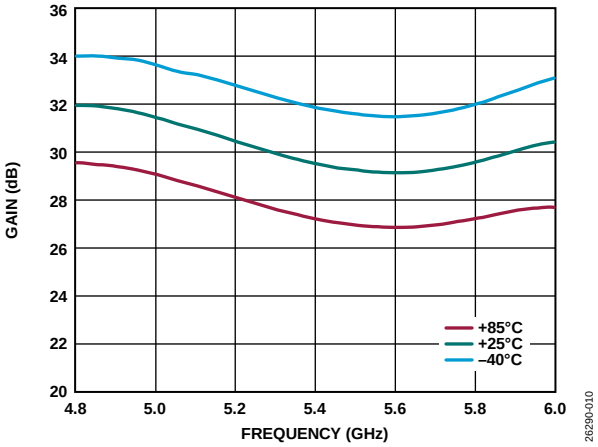


Figure 10. Small Signal Gain vs. Frequency at Various Temperatures

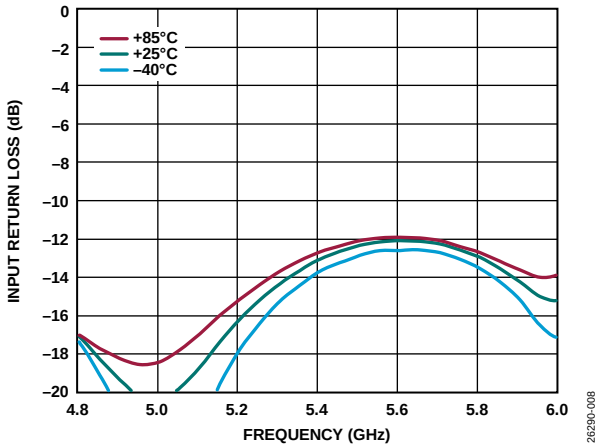


Figure 8. Input Return Loss vs. Frequency at Various Temperatures

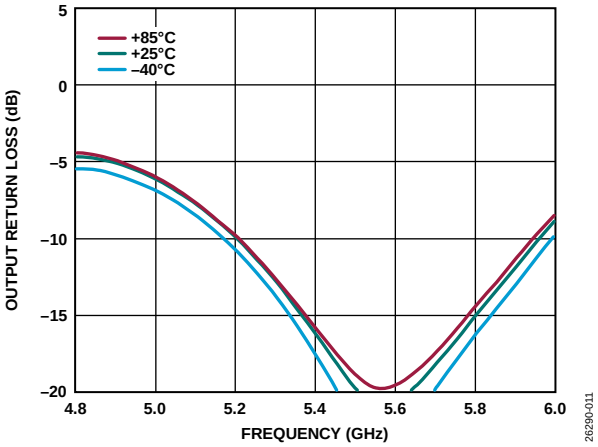


Figure 11. Output Return Loss vs. Frequency at Various Temperatures

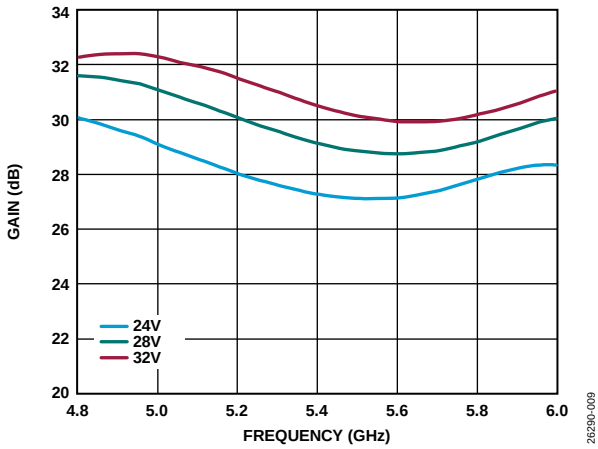


Figure 9. Small Signal Gain vs. Frequency at Various Supply Voltages and I_{DQ} = 350 mA

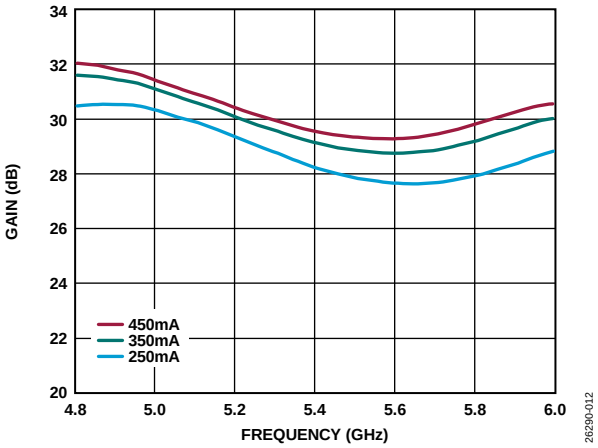


Figure 12. Small Signal Gain vs. Frequency at Various Quiescent Currents and VDD1x and VDD2x = 28 V

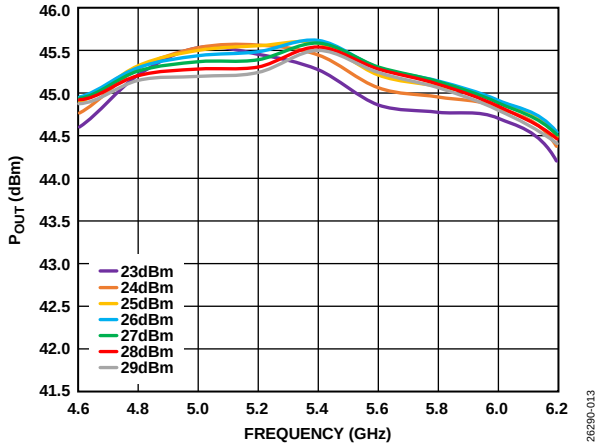


Figure 13. P_{OUT} vs. Frequency at Various P_{IN} Levels

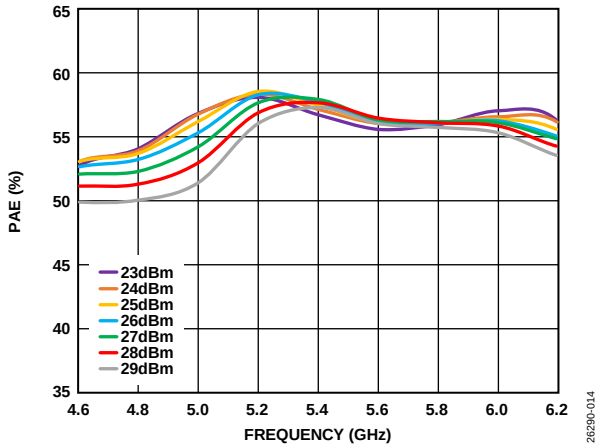


Figure 14. PAE vs Frequency at Various P_{IN} Levels

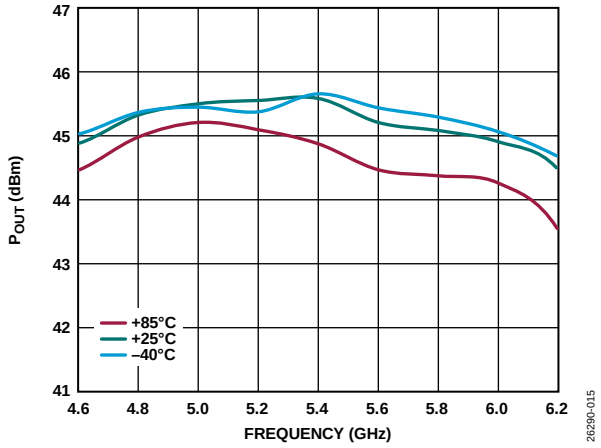


Figure 15. P_{OUT} vs. Frequency at Various Temperatures and P_{IN} = 25 dBm

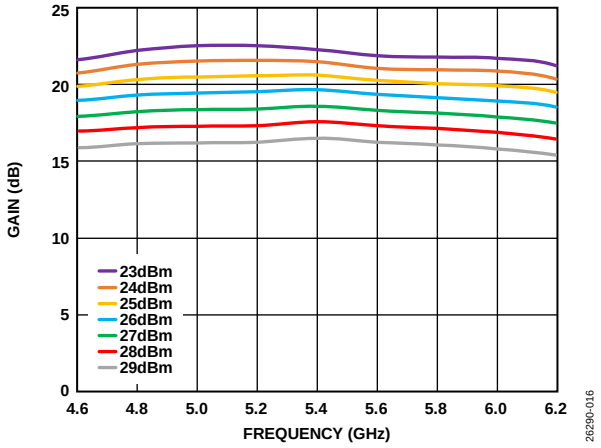


Figure 16. Gain vs. Frequency at Various P_{IN} Levels

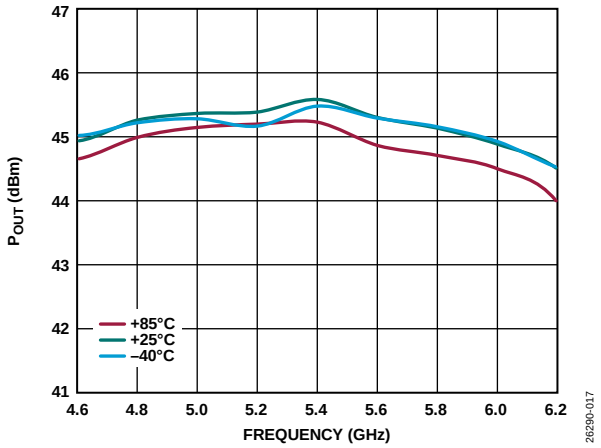


Figure 17. P_{OUT} vs. Frequency at Various Temperatures and P_{IN} = 27 dBm

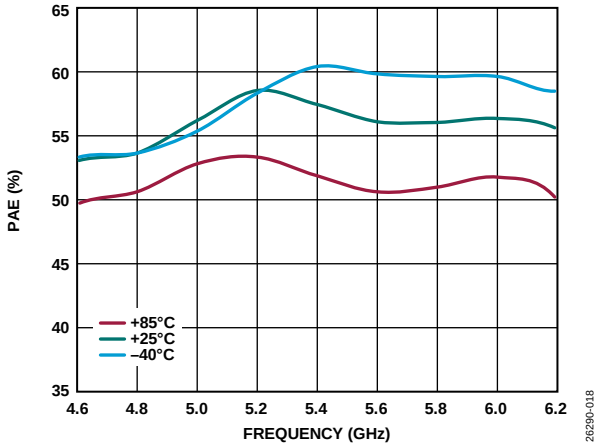


Figure 18. PAE vs. Frequency at Various Temperatures and P_{IN} = 25 dBm

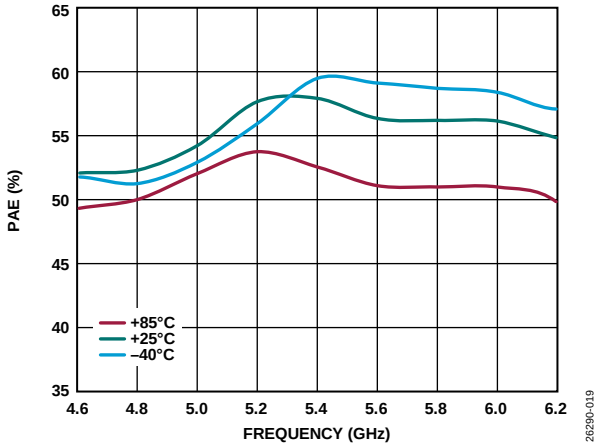


Figure 19. PAE vs. Frequency at
Various Temperatures and P_{IN} = 27 dBm

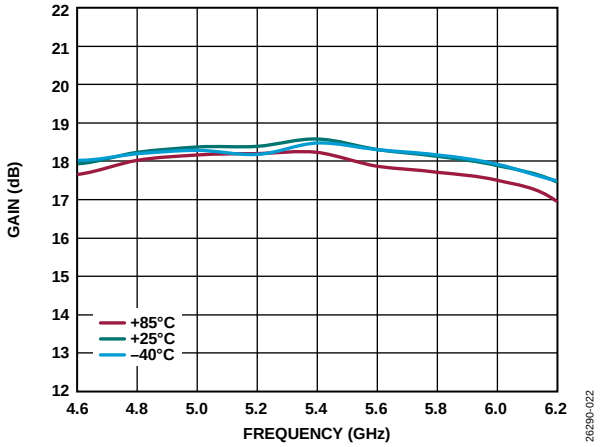


Figure 22. Gain vs. Frequency at
Various Temperatures and P_{IN} = 27 dBm

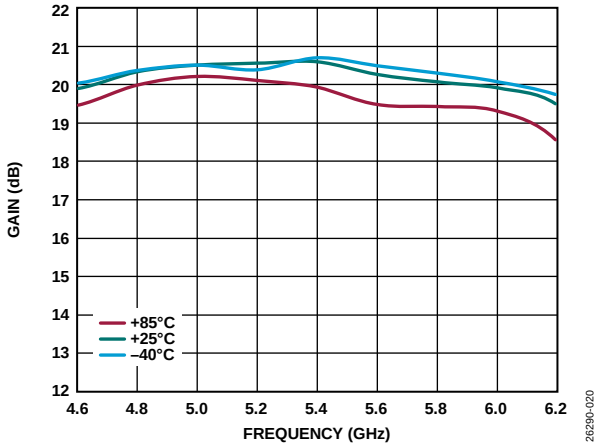


Figure 20. Gain vs. Frequency at
Various Temperatures and P_{IN} = 25 dBm

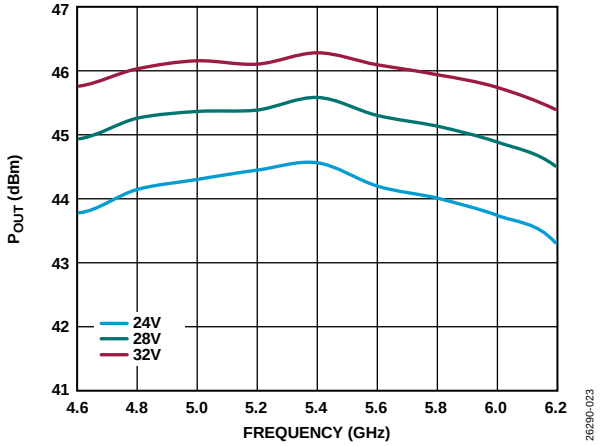


Figure 23. P_{OUT} vs. Frequency at
Various Supply Voltages and P_{IN} = 27 dBm, I_{DQ} = 350 mA

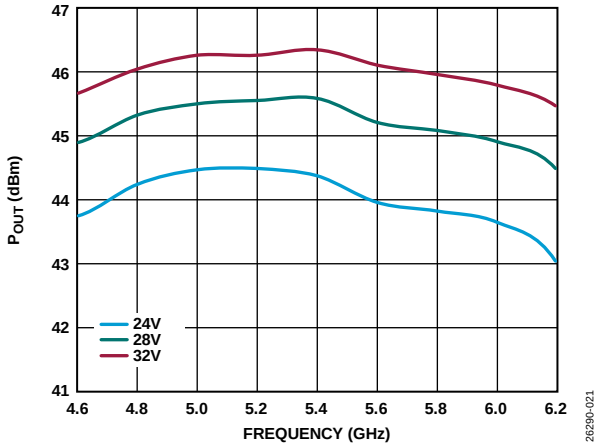


Figure 21. P_{OUT} vs. Frequency at
Various Supply Voltages, P_{IN} = 25 dBm, and I_{DQ} = 350 mA

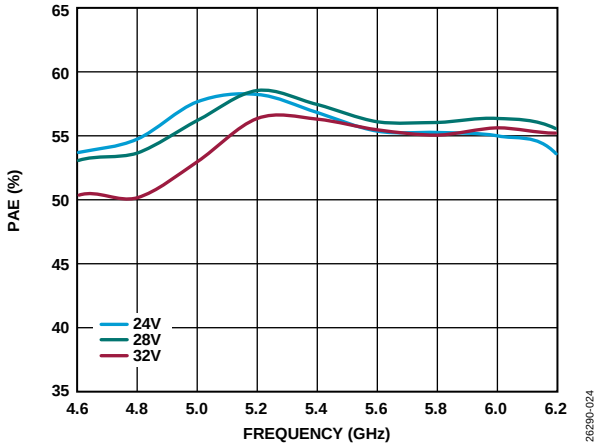


Figure 24. PAE vs. Frequency at
Various Supply Voltages, P_{IN} = 25 dBm, and I_{DQ} = 350 mA

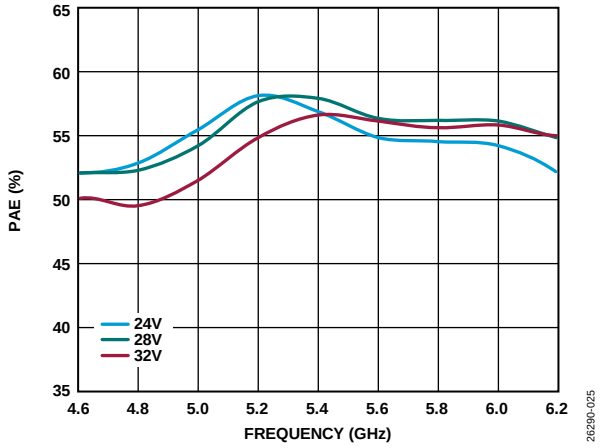


Figure 25. PAE vs. Frequency at
Various Supply Voltages, P_{IN} = 27 dBm, and I_{DQ} = 350 mA

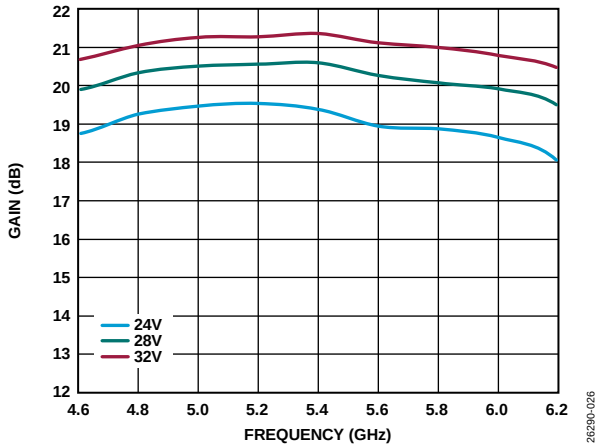


Figure 26. Gain vs. Frequency at
Various Supply Voltages, P_{IN} = 25 dBm, and I_{DQ} = 350 mA

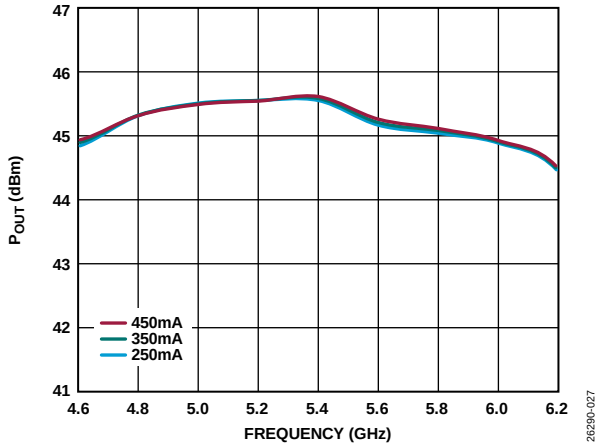


Figure 27. P_{OUT} vs. Frequency at
Various Quiescent Currents, P_{IN} = 25 dBm, and V_{DD} = 28 V

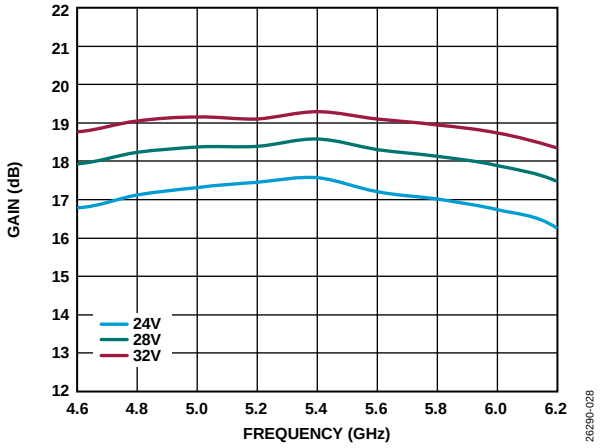


Figure 28. Gain vs. Frequency at
Various Supply Voltages, P_{IN} = 27 dBm, and I_{DQ} = 350 mA

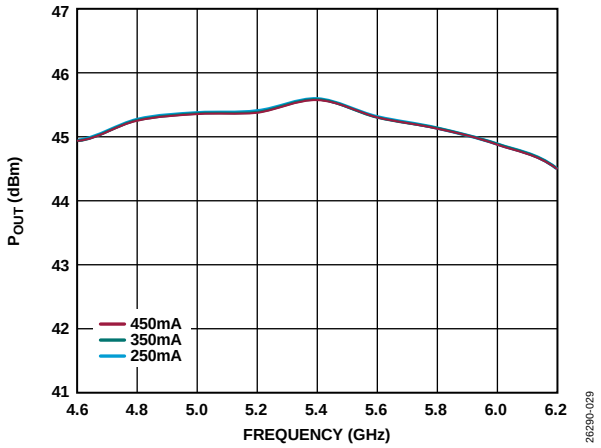


Figure 29. P_{OUT} vs. Frequency at
Various Quiescent Currents, P_{IN} = 27 dBm, and V_{DD} = 28 V

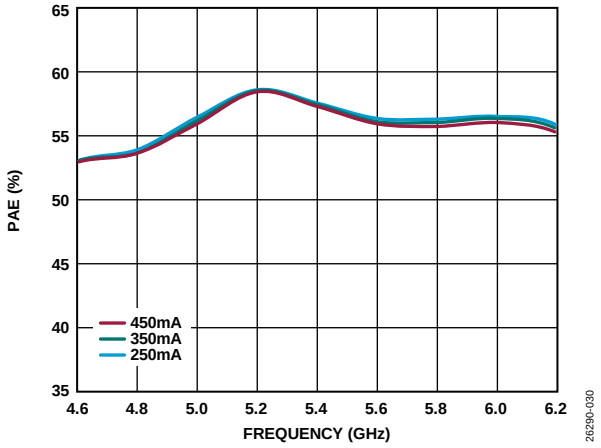


Figure 30. PAE vs. Frequency at
Various Quiescent Currents, P_{IN} = 25 dBm, and V_{DD} = 28 V

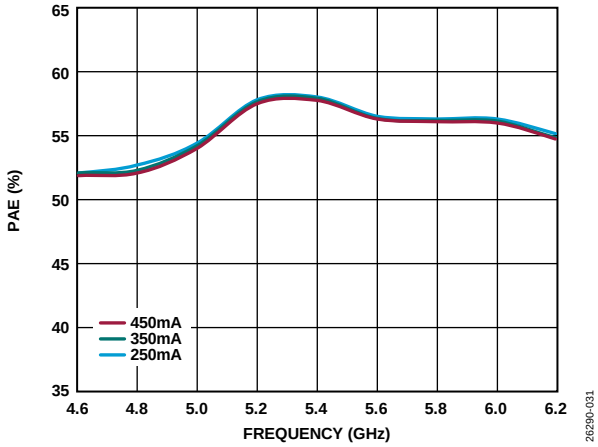


Figure 31. PAE vs. Frequency at
Various Quiescent Currents, P_{IN} = 27 dBm, and V_{DD} = 28 V

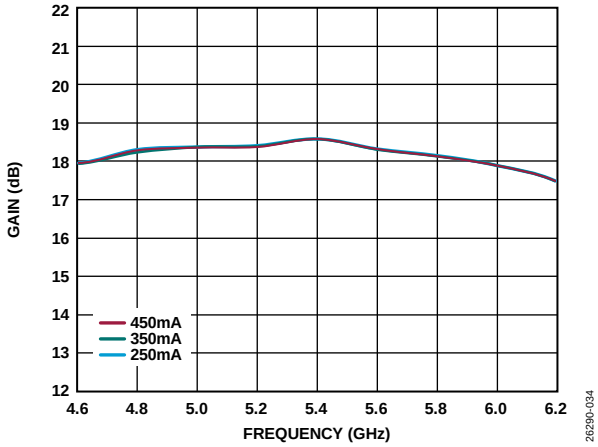


Figure 34. Gain vs. Frequency at
P_{IN} = 27 dBm and Various Quiescent Currents

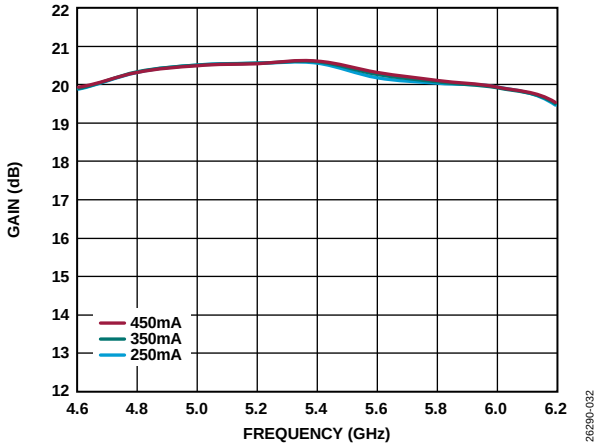


Figure 32. Gain vs. Frequency at
Various Quiescent Currents, P_{IN} = 25 dBm, and V_{DD} = 28 V

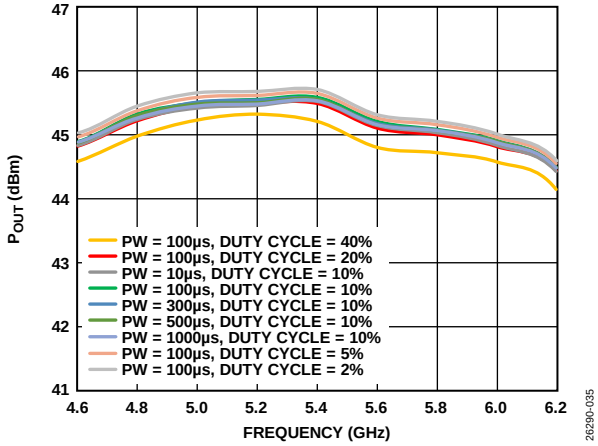


Figure 35. P_{OUT} vs. Frequency at
P_{IN} = 27 dBm and Various Pulse Widths (PW) and Duty Cycles

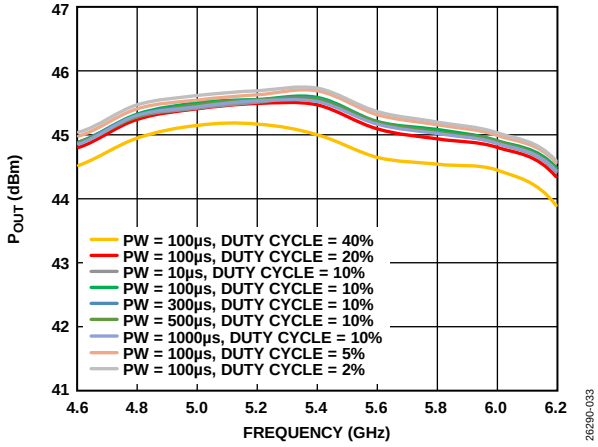


Figure 33. P_{OUT} vs. Frequency at
P_{IN} = 25 dBm and Various Pulse Widths (PW) and Duty Cycles

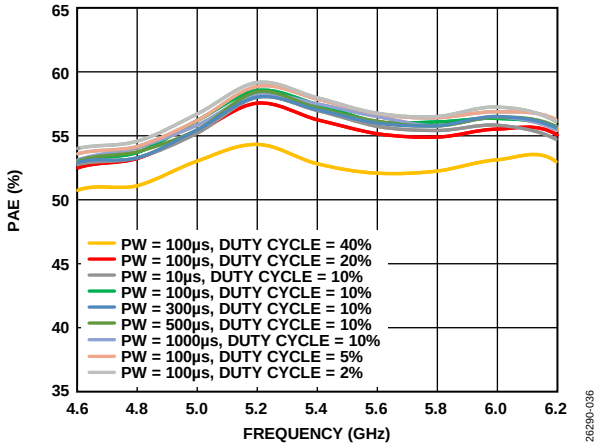


Figure 36. PAE vs. Frequency at
P_{IN} = 25 dBm and Various Pulse Widths (PW) and Duty Cycles

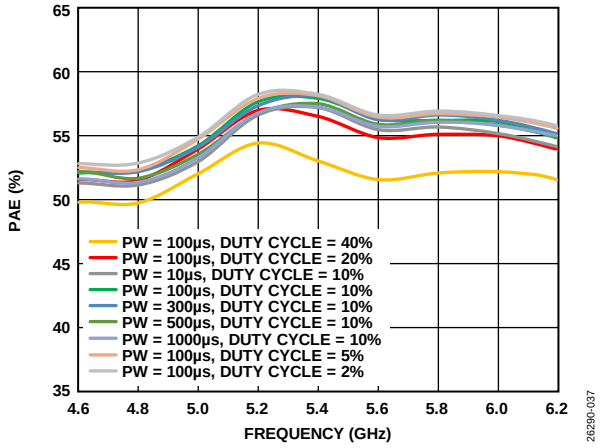


Figure 37. PAE vs. Frequency at
P_{IN} = 27 dBm and Various Pulse Widths (PW) and Duty Cycles

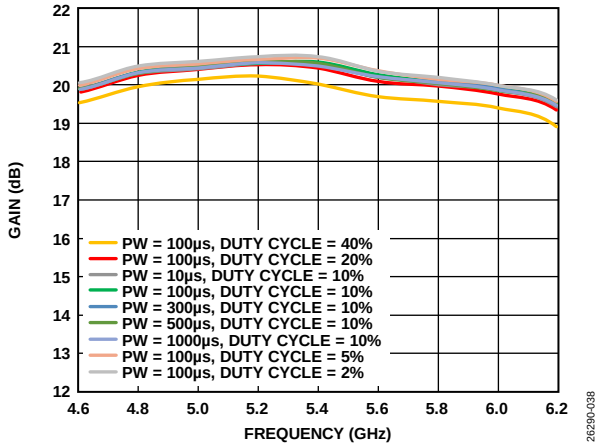


Figure 38. Gain vs. Frequency at
P_{IN} = 25 dBm and Various Pulse Widths (PW) and Duty Cycles

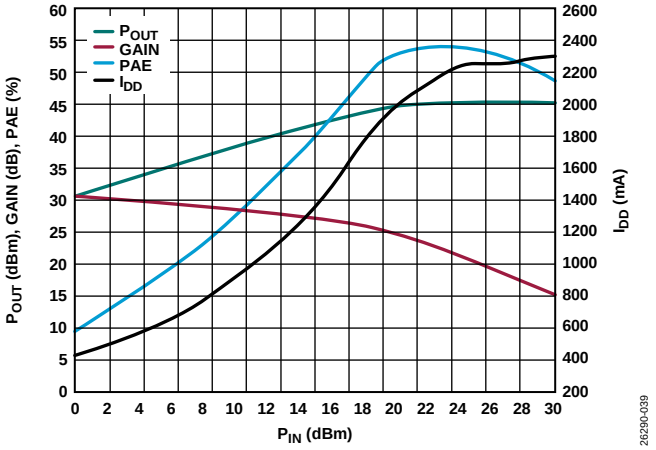


Figure 39. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN} at 4.8 GHz

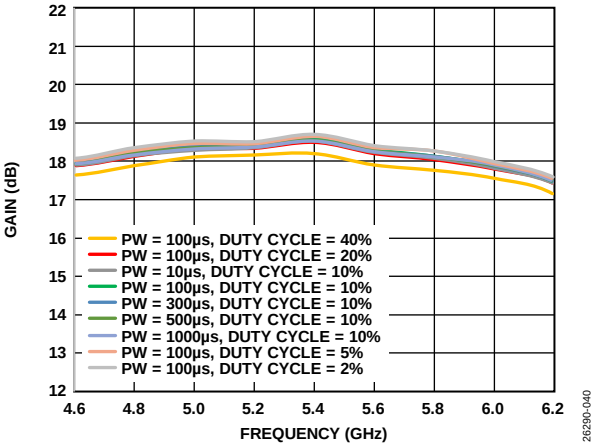


Figure 40. Gain vs. Frequency at
P_{IN} = 27 dBm and Various Pulse Widths (PW) and Duty Cycles

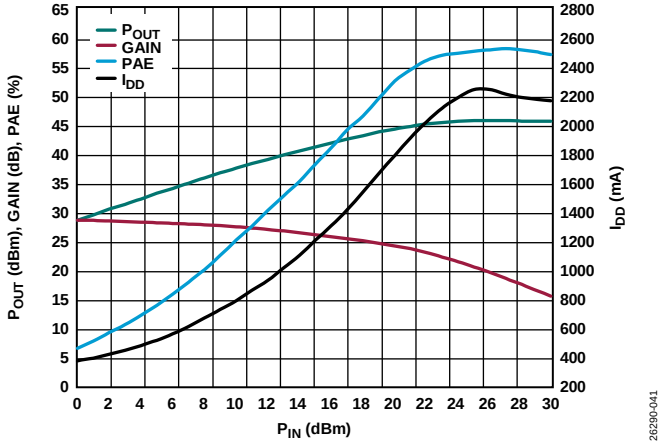


Figure 41. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN} at 5.4 GHz

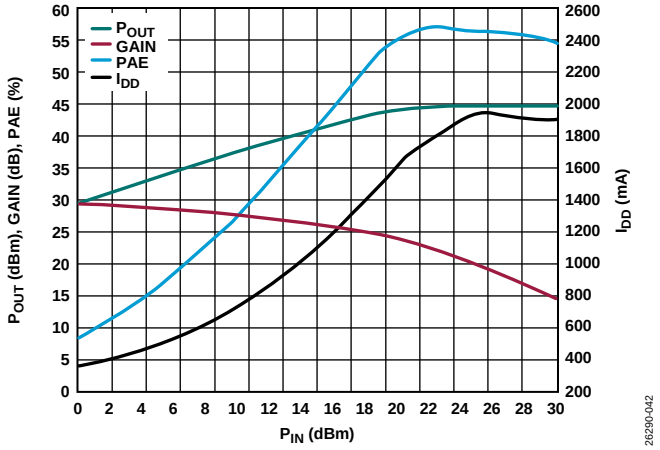


Figure 42. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN} at 6.0 GHz

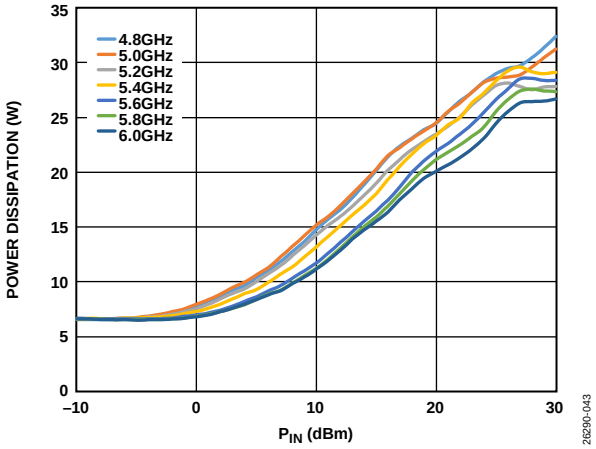


Figure 43. Power Dissipation vs. P_{IN}, Drain Bias Pulse Width = 100 µs, 10% Duty Cycle, and T_{BASE} = 85°C

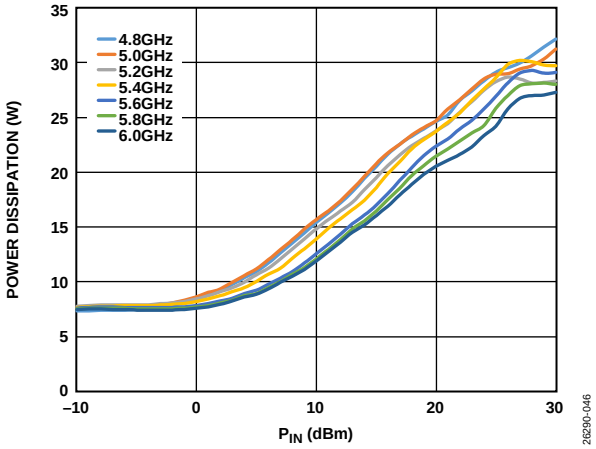


Figure 46. Power Dissipation vs. P_{IN}, Drain Bias Pulse Width = 100 µs, 20% Duty Cycle, and T_{BASE} = 85°C

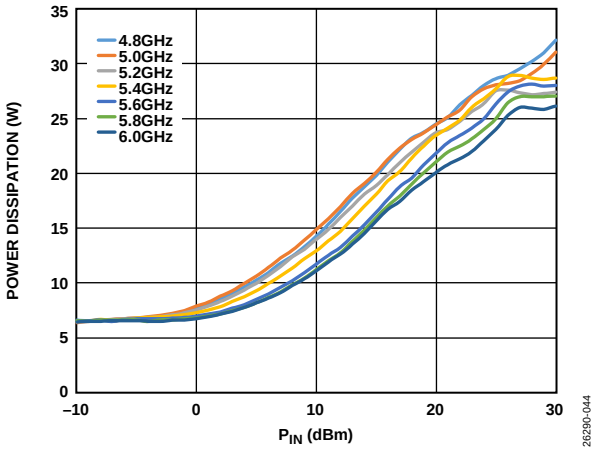


Figure 44. Power Dissipation vs. P_{IN}, Drain Bias Pulse Width = 100 µs, 2% Duty Cycle, and T_{BASE} = 85°C

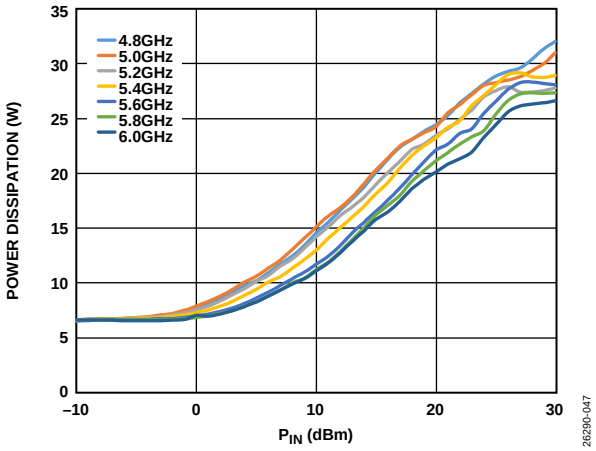


Figure 47. Power Dissipation vs. P_{IN}, Drain Bias Pulse Width = 100 µs, 5% Duty Cycle, and T_{BASE} = 85°C

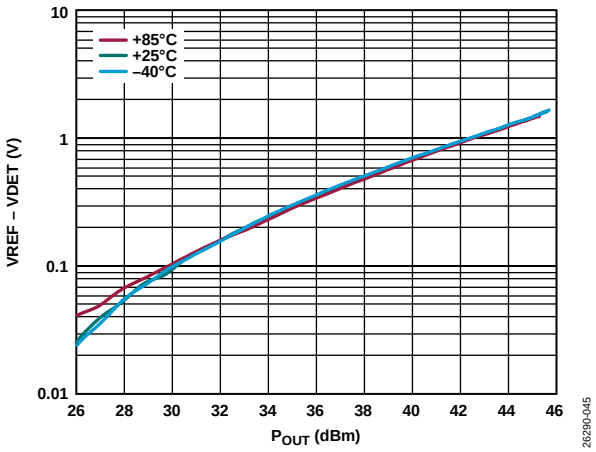


Figure 45. Detector Voltage (VREF – VDET) vs. P_{OUT} at Various Temperatures and 5.4 GHz

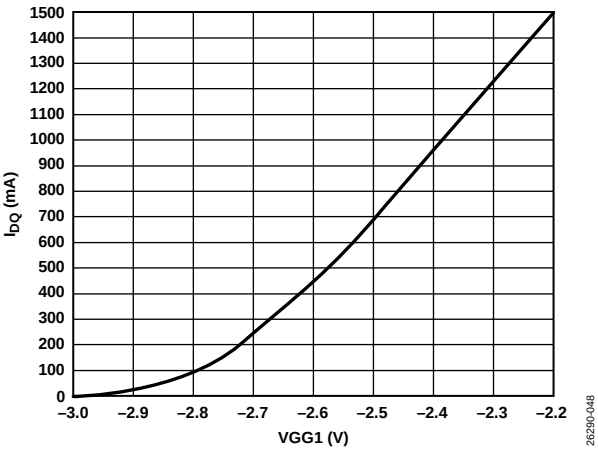


Figure 48. I_{DQ} vs. VGG1, VDD1x and VDD2x = 28 V, Representative of a Typical Device

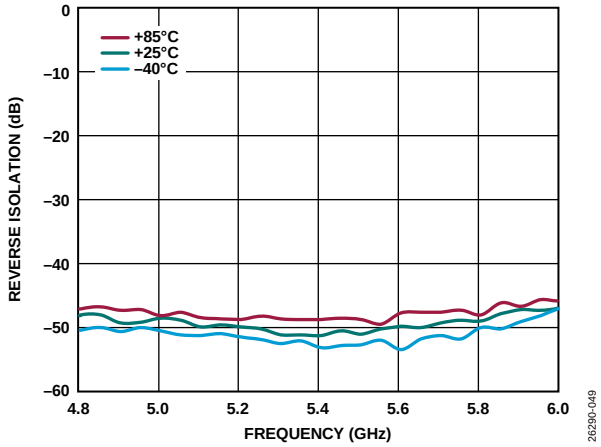


Figure 49. Reverse Isolation vs. Frequency at Various Temperatures at VDD1x and VDD2x = 28 V

THEORY OF OPERATION

The ADPA1107 is a GaN, broadband power amplifier that delivers 45 dBm (35 W) of pulsed power. The device consists of two cascaded gain stages. A simplified block diagram is shown in Figure 50.

The ADPA1107 has single-ended RFIN and RFOUT ports that are ac-coupled. The impedances of these ports are nominally 50 Ω over the 4.8 GHz to 6.0 GHz frequency range. Consequently, the ADPA1107 can be directly inserted into a 50 Ω system without the need for external impedance matching components or ac coupling capacitors.

The drain bias voltage applied to the VDD1A, VDD1B, VDD2A, and VDD2B pins biases the drains of the first and the second gain stages, respectively (a single common supply voltage must be used). The negative dc voltage applied to the VGG1 pin biases the gates of the first and the second gain stages, respectively, to allow control of the drain currents of each stage

A portion of the RF output signal is directionally coupled to a diode for detection of the RF output power. When the diode is dc biased, the diode rectifies the RF power and makes the RF power available for measurement as a dc voltage at the VDET pin. To allow temperature compensation of VDET, an identical and symmetrically located circuit, minus the coupled RF power, is available via VREF. Taking the difference of VREF – VDET provides a temperature compensated signal that is proportional to the RF output power (see Figure 51).

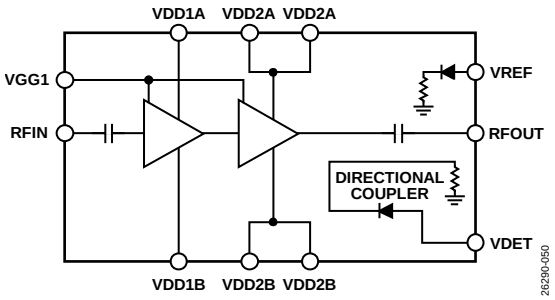


Figure 50. Simplified Block Diagram

APPLICATIONS INFORMATION

BASIC CONNECTIONS

The basic connections for operating the ADPA1107 are shown in Figure 51. Apply a power supply voltage of between 28 V and 32 V on all VDDxA and VDDxB pins. Decouple the VDDxA and VDDxB pins with the capacitor values shown in Figure 51. The VDD1x pins require a 2.55 Ω resistor in series with the decoupling capacitor to assist with making the ADPA1107 unconditionally stable. The VGG1 pin is used to set the I_{DQ} of all stages. The decoupling capacitors on the VDDxA, VDDxB, and VGG1 lines represent the configuration that was used to characterize and qualify the ADPA1107.

Pin 1 through Pin 4, Pin 8 through Pin 12, Pin 14 through Pin 17, Pin 20 through Pin 22, Pin 28 through Pin 31, Pin 34 through Pin 37, and Pin 40 are designated as no internal connection (NIC) pins. Although the NIC pins are not internally connected, the NIC pins were all connected to ground during the characterization of the device.

Apply a voltage between −2 V and −4 V to the VGG1 line to set the drain current. The device can be operated by pulsing either the gate voltage or the drain voltage.

In gate pulsed mode, VDDxA and VDDxB are held at a fixed level (nominally +28 V), while the gate voltage is pulsed between −4 V (off) and approximately −2.6 V (on). The exact on level can be adjusted to achieve the desired I_{DQ}.

In drain pulsed mode, VDDxA and VDDxB are pulsed on and off while the gate voltage is held at a fixed negative level between −2 V and −4 V. Because high currents and voltages are being switched on and off, a metal-oxide semiconductor field effect transistor (MOSFET) and a MOSFET switch driver are required in the circuit. Large capacitors are also required, which act as local reservoirs of charge and help provide the drain current required by the ADPA1107 while maintaining a steady drain voltage during the on time of the pulse.

The ADPA1107-EVALZ includes a plug-in pulser board that contains the required circuitry to implement drain pulsed mode. See the ADPA1107A-EVALZ user guide (UG-1962) for additional information.

To safely turn power on, the VGG1 voltage must be set to −4 V before the VDDxA and the VDDxB voltages are applied. After VGG1 is increased to achieve the desired I_{DQ}, the RF input can be applied.

To safely turn power off, remove the RF input signal and decrease VGG1 to −4 V. VDDxA and VDDxB can then be decreased to 0 V before increasing VGG1 to 0 V.

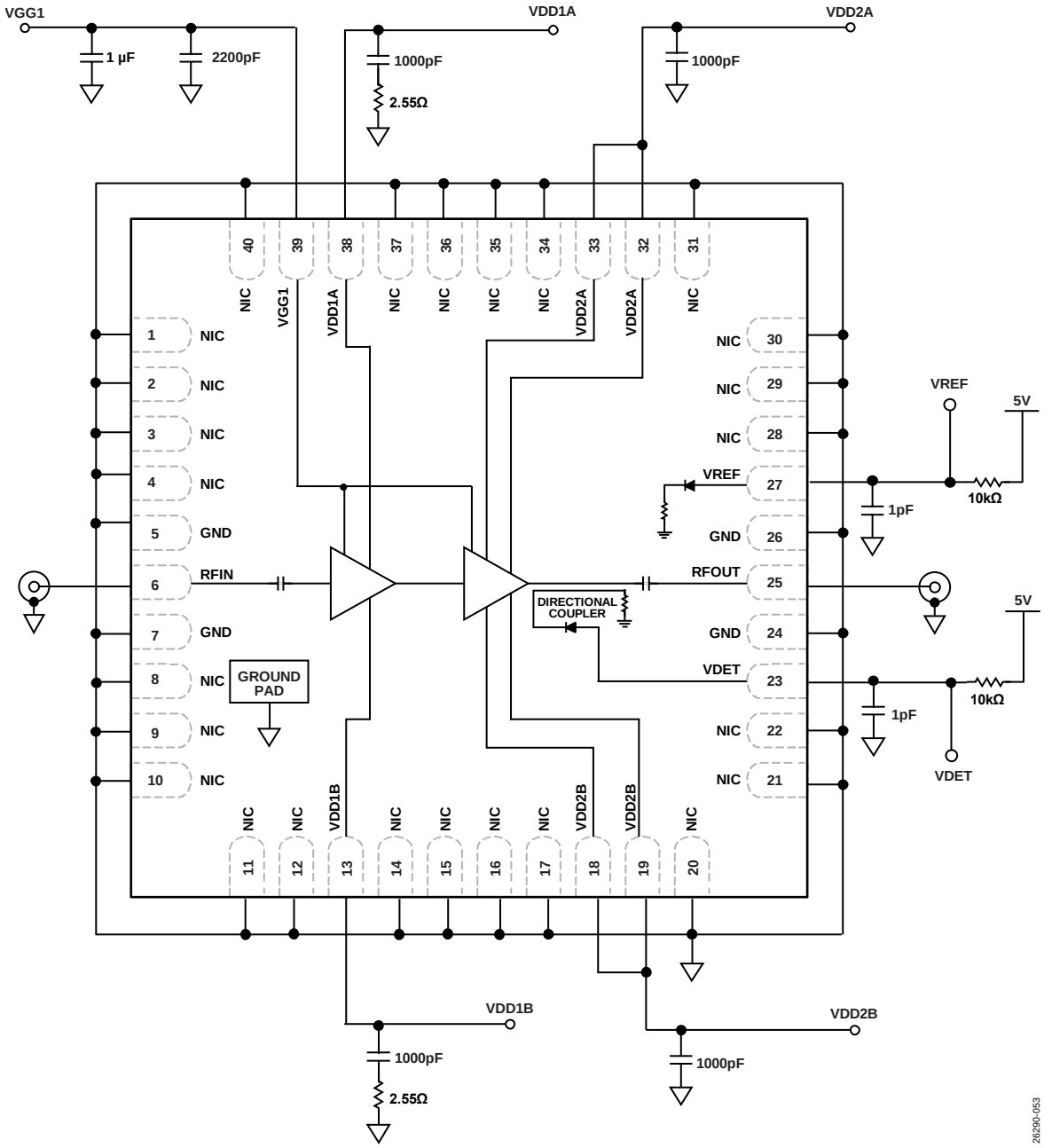


Figure 51. Basic Connections

THERMAL MANAGEMENT

Proper thermal management is critical to achieve the specified performance and rated operating life. Pulsed biasing limits the average power dissipated and maintains a safe channel temperature. The channel (or die) temperature correlates closely with the mean time to failure (MTTF).

Consider a continuous bias condition (see Figure 52). When bias is applied, the channel temperature (T_{CHAN}) of the device rises through a turn on transient interval and eventually settles to a steady state value. The θ_{JC} of the device is the rise in T_{CHAN} above the starting T_{BASE} divided by the total device P_{DISS}, which is calculated by

$$\theta_{JC} = t_{RISE}/P_{DISS} \quad (1)$$

where:
t_{RISE} is the rise in T_{CHAN} of the device above the T_{BASE} (°C).
P_{DISS} is the power dissipation (W) of the device.

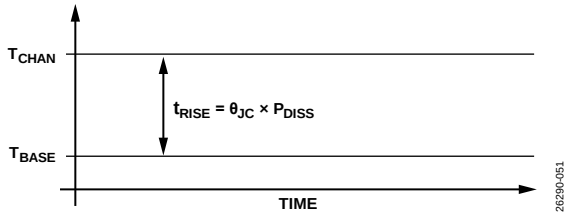


Figure 52. Channel Temperature Rise for Continuous Bias Condition

Next, consider a pulsed bias condition at a low duty cycle (see Figure 53). When bias is applied, the T_{CHAN} of the device can be described as a series of exponentially rising and decaying pulses. The peak channel temperature reached during consecutive pulses increases during the turn on transient interval, and eventually, settles to a steady state condition where peak channel temperatures from pulse to pulse stabilize.

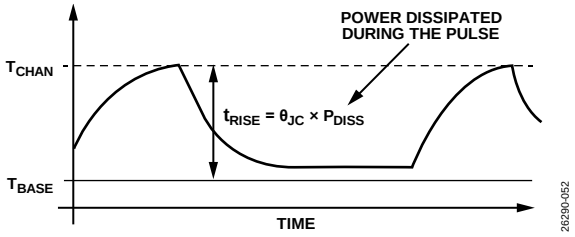


Figure 53. Pulsed Bias Condition at a Low Duty Cycle

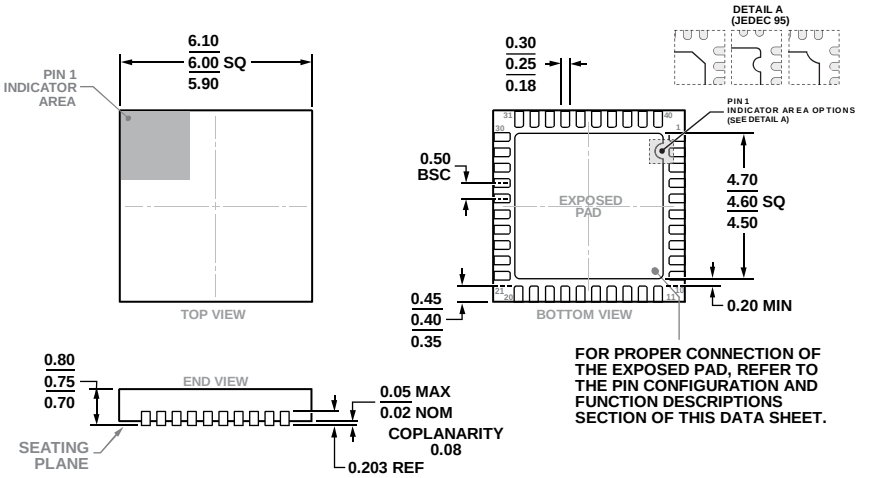
Table 7 shows the thermal resistance values for various pulse conditions.

Table 7. Pulse Settings and Thermal Resistance Values

Pulse Settings		
Pulse Width (µs)	**Duty Cycle (%)**	**θ_{JC} (°C/W)**
100	10	1.72
100	20	1.76
500	10	2.10

Narrower pulse widths and/or lower duty cycles can result in greater reliability.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WJJD-5

Figure 54. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.75 mm Package Height
(CP-40-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature	MSL Rating[2]	Description[3]	Package Option
ADPA1107ACPZN	−40°C to +85°C	MSL3	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-7
ADPA1107ACPZN-R7	−40°C to +85°C	MSL3	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-7
ADPA1107-EVALZ			Evaluation Board	

[1] The ADPA1107ACPZN and ADPA1107ACPZN-R7 models are RoHS compliant parts.
[2] See the Absolute Maximum Ratings section for additional information.
[3] The lead finish of ADPA1107ACPZN and ADPA1107ACPZN-R7 is nickel palladium gold (NiPdAu).

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