Dual-Channel, 3.3 GHz to 4.0 GHz, 20 W Receiver Front End

Data Sheet **ADRF5515**

FEATURES

- Integrated dual-channel RF front end
  - 2-stage LNA and high power silicon SPDT switch
  - On-chip bias and matching
  - Single-supply operation
- Gain
  - High gain mode: 33 dB typical at 3.6 GHz
  - Low gain mode: 16 dB typical at 3.6 GHz
- Low noise figure
  - High gain mode: 1.0 dB typical at 3.6 GHz
  - Low gain mode: 1.0 dB typical at 3.6 GHz
- High isolation
  - RXOUT-CHA and RXOUT-CHB: 45 dB typical
  - TERM-CHA and TERM-CHB: 60 dB typical
- Low insertion loss: 0.45 dB typical at 3.6 GHz
- High power handling at T_{CASE} = 105°C
  - Full lifetime
    - LTE average power (9 dB PAR): 43 dBm
- High OIP3 (high gain mode): 32 dBm typical
- Power-down mode and low gain mode for LNA
- Low supply current
  - High gain mode: 86 mA typical at 5 V
  - Low gain mode: 36 mA typical at 5 V
  - Power-down mode: 12 mA typical at 5 V
- Positive logic control
- 6 mm × 6 mm, 40-lead LFCSP
- Pin compatible with the ADRF5545A, 10 W version

APPLICATIONS

- Wireless infrastructure
- TDD massive multiple input and multiple output and active antenna systems
- TDD-based communication systems

FUNCTIONAL BLOCK DIAGRAM

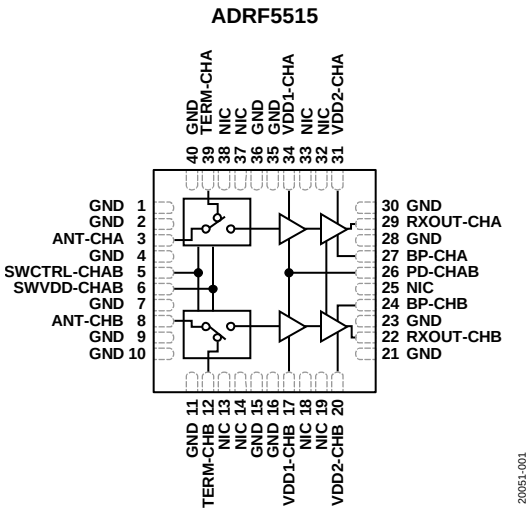


Figure 1.

GENERAL DESCRIPTION

The ADRF5515 is a dual-channel, integrated RF, front-end, multichip module designed for time division duplexing (TDD) applications. The device operates from 3.3 GHz to 4.0 GHz. The ADRF5515 is configured in dual channels with a cascading, two-stage, LNA and a high power silicon SPDT switch.

In high gain mode, the cascaded two-stage LNA and switch offer a low noise figure of 1.0 dB and a high gain of 33 dB at 3.6 GHz with an output third-order intercept point (OIP3) of 32 dBm (typical). In low gain mode, one stage of the two-stage LNA is in bypass, providing 16 dB of gain at a lower current of 36 mA. In power-down mode, the LNAs are turned off and the device draws 12 mA.

In transmit operation, when RF inputs are connected to a termination pin (TERM-CHA or TERM-CHB), the switch provides low insertion loss of 0.45 dB and handles long-term evolution (LTE) average power (9 dB peak to average ratio (PAR)) of 43 dBm for full lifetime operation.

The ADRF5515 is pin-compatible with the ADRF5545A, 10 W version, which operates from 2.4 GHz to 4.2 GHz.

The ADRF5515 does not require any matching components at the RF ports that are internally matched to 50 Ω. The ANT and TERM ports are also internally ac-coupled. Therefore, only receiver ports require external dc blocking capacitors.

The device comes in an RoHS compliant, compact, 6 mm × 6 mm, 40-lead LFCSP.

Rev. 0 Document Feedback
Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 Technical Support
©2020 Analog Devices, Inc. All rights reserved.
www.analog.com

TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Functional Block Diagram ... 1
Revision History ... 2
Specifications ... 3
  Electrical Specifications ... 3
Absolute Maximum Ratings ... 5
  Thermal Resistance ... 5
  Electrostatic Discharge (ESD) Ratings ... 5
  ESD Caution ... 5
Pin Configuration and Function Descriptions ... 6
  Interface Schematics ... 7
Typical Performance Characteristics ... 8
  Receive Operation, High Gain Mode ... 8
  Receive Operation, Low Gain Mode ... 10
  Transmit Operation ... 12
Theory of Operation ... 13
  Signal Path Select ... 13
  Biasing Sequence ... 13
Applications Information ... 14
Outline Dimensions ... 15
  Ordering Guide ... 15

REVISION HISTORY

11/2020—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

VDD1-CHA, VDD1-CHB, VDD2-CHA, VDD2-CHB, and SWVDD-CHAB = 5 V, SWCTRL-CHAB = 0 V or SWVDD-CHAB, BP-CHA = VDD1-CHA or 0 V, BP-CHB = VDD1-CHB or 0 V, PD-CHAB = 0 V or VDD1-CHA, T_{CASE} = 25°C, and 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		3.3		4.0	GHz
GAIN[1]	Receive operation at 3.6 GHz				
High Gain Mode			33		dB
Low Gain Mode			16		dB
GAIN FLATNESS[1]	Receive operation in any 100 MHz bandwidth				
High Gain Mode			0.6		dB
Low Gain Mode			0.2		dB
NOISE FIGURE[1]	Receive operation at 3.6 GHz				
High Gain Mode			1.0		dB
Low Gain Mode			1.0		dB
OUTPUT THIRD-ORDER INTERCEPT POINT (OIP3)[1]	Receive operation, two-tone output power = 8 dBm per tone at 1 MHz tone spacing				
High Gain Mode			32		dBm
Low Gain Mode			29		dBm
OUTPUT 1 dB COMPRESSION (OP1dB)					
High Gain Mode			18		dBm
Low Gain Mode			15		dBm
INSERTION LOSS[1]	Transmit operation at 3.6 GHz		0.45		dB
Channel to Channel Isolation[1]	At 3.6 GHz				
Between RXOUT-CHA AND RXOUT-CHB	Receive operation		45		dB
Between TERM-CHA AND TERM-CHB	Transmit operation		60		dB
SWITCH ISOLATION					
ANT-CHA to TERM-CHA and ANT-CHB to TERM-CHB[1]	Transmit operation, PD-CHAB = 0 V		18.5		dB
SWITCHING CHARACTERISTICS (t_{ON}, t_{OFF})					
	50% control voltage to 90%, 10% of RXOUT-CHA or RXOUT-CHB in receive operation		600		ns
	50% control voltage to 90%, 10% of TERM-CHA or TERM-CHB in transmit operation		595		ns
RECOMMENDED OPERATING CONDITIONS					
Supply Voltage (V_{DD}) Range	VDD1-CHA, VDD1-CHB, VDD2-CHA, VDD2-CHB, SWVDD-CHAB	4.75	5	5.25	V
Control Voltage Range	SWCTRL-CHAB, BP-CHA, BP-CHB, PD-CHAB	0		V_{DD}	V
RF Input Power	SWCTRL-CHAB = 5 V, T_{CASE} = 105°C				
At ANT-CHA, ANT-CHB	PD-CHAB = 5 V, BP-CHA = BP-CHB = 0 V				
	9 dB PAR LTE full lifetime average			43	dBm
	7 dB PAR LTE single event (<10 sec) average[1]			46	dBm
At ANT-CHA, ANT-CHB	PD-CHAB = 0 V, BP-CHA = BP-CHB = 0 V				
	9 dB PAR LTE full lifetime average			31	dBm

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
At ANT-CHA, ANT-CHB	PD-CHAB = 0 V, BP-CHA = BP-CHB = 5 V				
	9 dB PAR LTE full lifetime average, 3.3 GHz to 4.0 GHz			43	dBm
	7 dB PAR LTE single event (<10 sec) average[1]			46	dBm
T_{CASE} Range[2]		−40		+105	°C
Junction Temperature at Maximum T_{CASE}					
	Receive operation[3]			132	°C
	Transmit operation[3]			134	°C
DIGITAL INPUT					
SWCTRL-CHAB, PD-CHAB					
Low (V_{IL})		0		0.7	V
High (V_{IH})		1.4		V_{DD}	V
BP-CHA, BP-CHB					
Low (V_{IL})		0		0.3	V
High (V_{IH})		1.0		V_{DD}	V
SUPPLY CURRENT (I_{DD})	VDD1-CHx and VDD2-CHx = 5 V per channel				
High Gain Mode			86		mA
Low Gain Mode			36		mA
Power-Down Mode			12		mA
Transmitter Current (Switch)	SWVDD-CHAB = 5 V		1.3		mA
DIGITAL INPUT CURRENTS	SWCTRL-CHAB, PD-CHAB, BP-CHA, BP-CHB = 5 V per channel				
SWCTRL-CHAB			0.084		mA
PD-CHAB			0.19		mA
BP-CHA, BP-CHB			0.19		mA

[1] Peak power >53 dBm has not been evaluated.
[2] Measured at the exposed pad.
[3] See Table 5 and Table 6.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (V_{DD})	
VDD1-CHA, VDD1-CHB, VDD2-CHA, and VDD2-CHB	7 V
SWVDD-CHAB	5.4 V
Digital Control Input Voltage	
SWCTRL-CHAB	−0.3 V to V_{DD}+ 0.3 V
BP-CHA, BP-CHB, and PD-CHAB	−0.3 V to V_{DD}+ 0.3 V
Digital Control Input Current	
BP-CHA, BP-CHB, PD-CHAB, and SWCTRL-CHAB	20 mA
RF Input Power	
Transmit Input Power (LTE Peak, 9 dB PAR)	53 dBm
Receive Input Power (LTE Peak, 9 dB PAR)	25 dBm
Temperature	
Storage Range	−65°C to +150°C
Reflow	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operation environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}	Unit
CP-40-15		
High Gain Mode	30	°C/W
Low Gain Mode	36	°C/W
Power-Down Mode	6	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADRF5515

Table 4. ADRF5515, 40-Lead LFCSP

ESD Model	Withstand Threshold	Class
HBM	1 kV	1C
CDM	750 V	

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

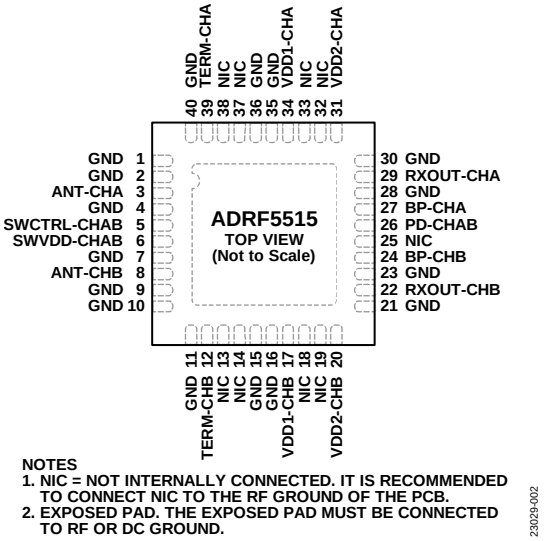


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4, 7, 9 to 11, 15, 16, 21, 23, 28, 30, 35, 36, 40	GND	Ground.
3	ANT-CHA	RF Input to Channel A. The ANT-CHA pin is ac-coupled to 0 V and matched to 50 Ω. Matching and a dc blocking capacitor are not required.
5	SWCTRL-CHAB	Control Voltage for Switches on Channel A and Channel B.
6	SWVDD-CHAB	Supply Voltage for Switches on Channel A and Channel B.
8	ANT-CHB	RF Input to Channel B. The ANT-CHB pin is ac-coupled to 0 V and matched to 50 Ω. Matching and a dc blocking capacitor are not required.
12	TERM-CHB	Termination Output for Channel B. The TERM-CHB pin is the transmitter path for Channel B. The TERM-CHB pin is ac-coupled to 0 V and matched to 50 Ω. No matching and dc blocking capacitor required.
13, 14, 18, 19, 25, 32, 33, 37, 38	NIC	Not Internally Connected. It is recommended to connect NIC to the RF ground of the PCB.
17	VDD1-CHB	Supply Voltage for Stage 1 LNA on Channel B.
20	VDD2-CHB	Supply Voltage for Stage 2 LNA on Channel B.
22	RXOUT-CHB	Receiver Output. The RXOUT-CHB pin is the receiver path for Channel B. The RXOUT-CHB pin is ac matched to 50 Ω. No matching component is required. A dc blocking capacitor is required.
24	BP-CHB	Bypass Second Stage LNA of Channel B.
26	PD-CHAB	Power-Down All Stages of LNA for Channel A and Channel B.
27	BP-CHA	Bypass Second Stage LNA of Channel A.
29	RXOUT-CHA	Receiver Output. The RXOUT-CHA pin is the receiver path for Channel A. The RXOUT-CHA pin is ac matched to 50 Ω. No matching component is required. A dc blocking capacitor is required.
31	VDD2-CHA	Supply Voltage for Stage 2 LNA on Channel A.
34	VDD1-CHA	Supply Voltage for Stage 1 LNA on Channel A.
39	TERM-CHA	Termination Output for Channel A. The TERM-CHA pin is the transmitter path for Channel A. The TERM-CHA pin is ac-coupled to 0 V and matched to 50 Ω. No matching and dc blocking capacitor required.
	EPAD	Exposed Pad. The exposed pad must be connected to RF or dc ground.

INTERFACE SCHEMATICS



Figure 3. GND Interface

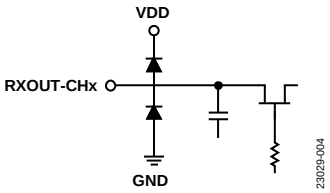


Figure 4. RXOUT-CHx Interface

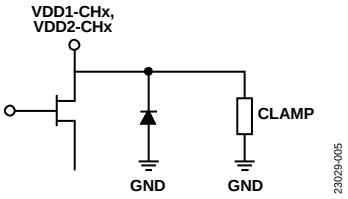


Figure 5. VDD1-CHx, VDD2-CHx Interface

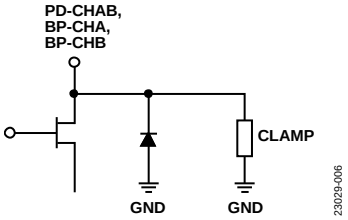


Figure 6. PD-CHAB, BP-CHx Interface

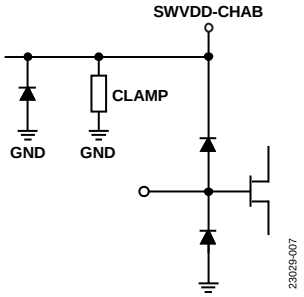


Figure 7. SWCTRL-CHAB, SWVDD-CHAB Interface

TYPICAL PERFORMANCE CHARACTERISTICS

RECEIVE OPERATION, HIGH GAIN MODE

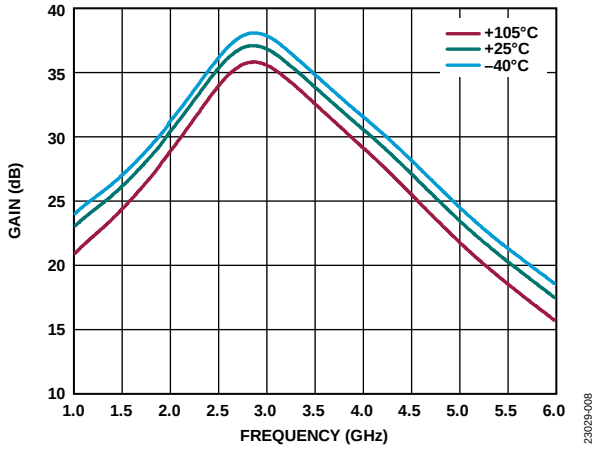


Figure 8. Gain vs. Frequency at Various Temperatures

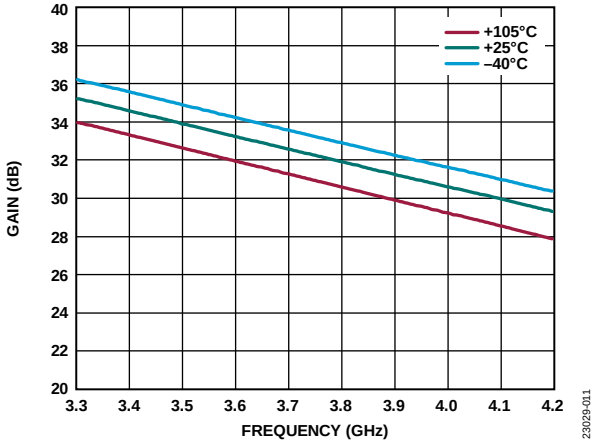


Figure 11. Gain vs. Frequency at Various Temperatures, 3.3 GHz to 4.2 GHz

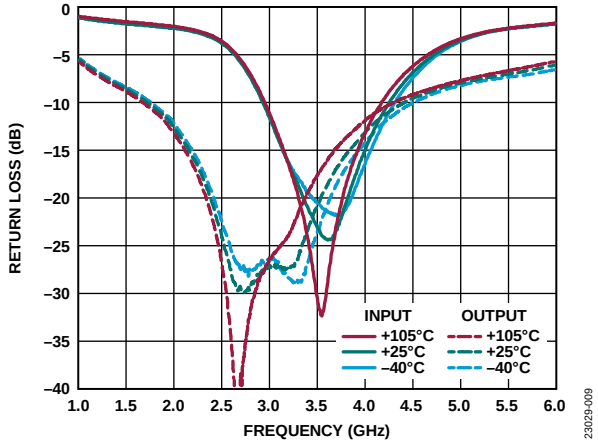


Figure 9. Input/Output Return Loss vs. Frequency at Various Temperatures

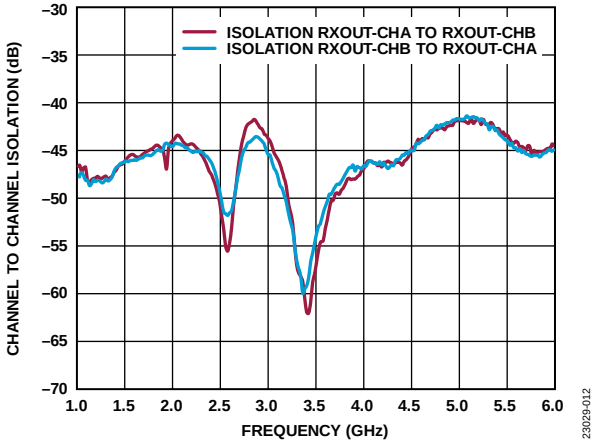


Figure 12. Channel to Channel Isolation vs. Frequency

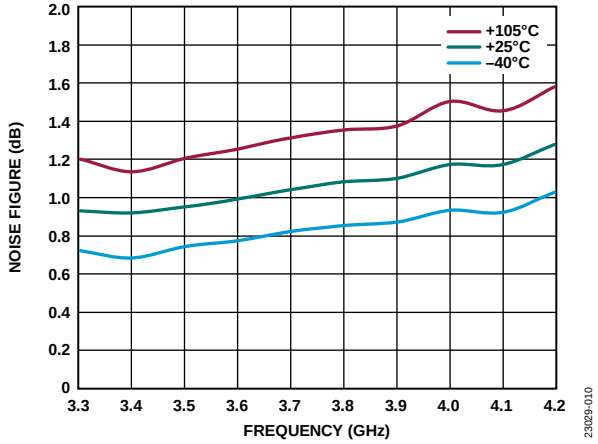


Figure 10. Noise Figure vs. Frequency at Various Temperatures

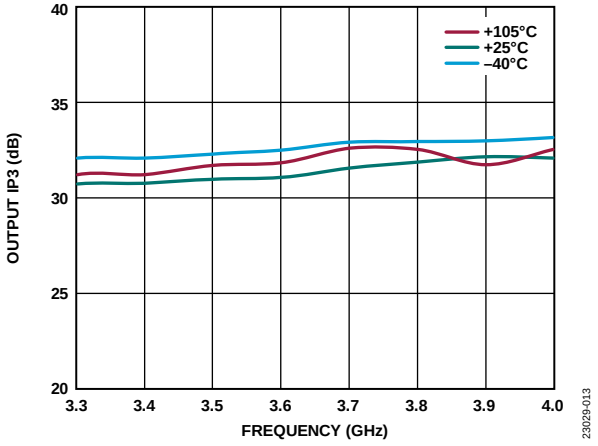


Figure 13. Output IP3 vs. Frequency at Various Temperatures, 8 dBm Output Tone Power

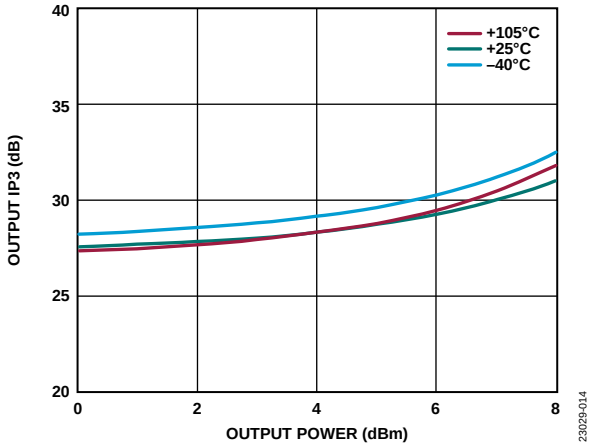


Figure 14. Output IP3 vs. Output Power at Various Temperatures, 3.6 GHz

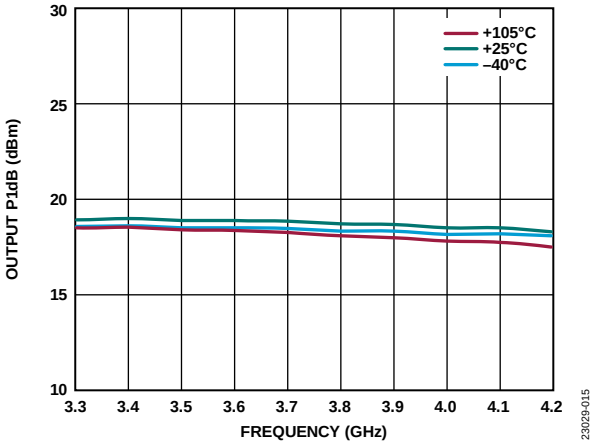


Figure 15. Output P1dB vs. Frequency at Various Temperatures

RECEIVE OPERATION, LOW GAIN MODE

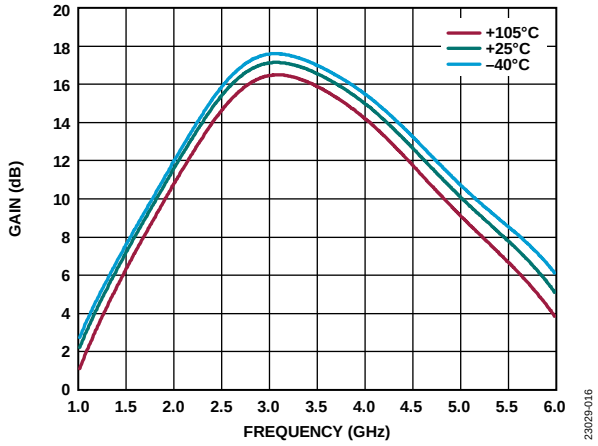


Figure 16. Gain vs. Frequency at Various Temperatures

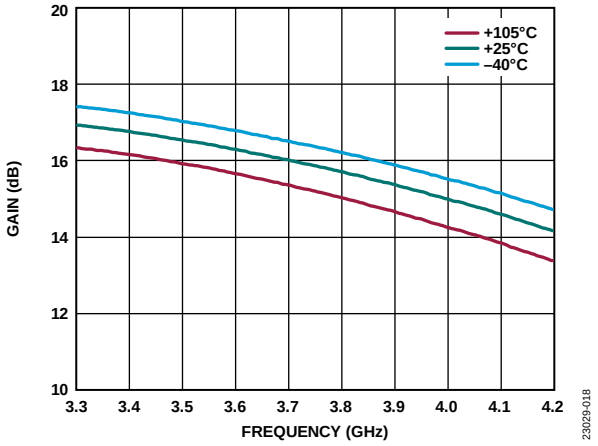


Figure 18. Gain vs. Frequency at Various Temperatures, 3.3 GHz to 4.2 GHz

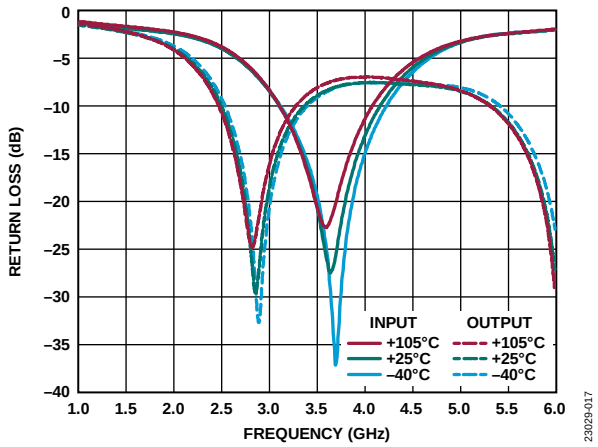


Figure 17. Input/Output Return Loss vs. Frequency at Various Temperatures

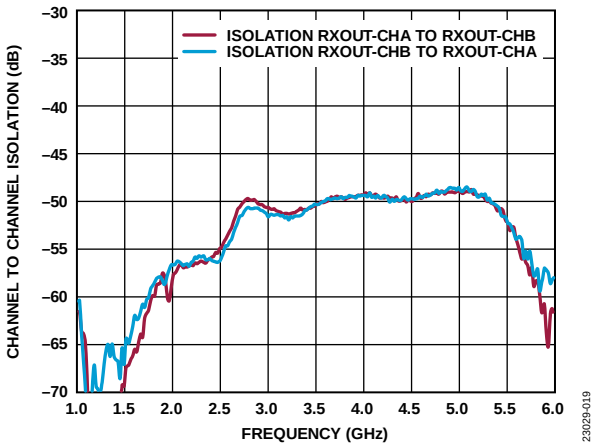


Figure 19. Channel to Channel Isolation vs. Frequency

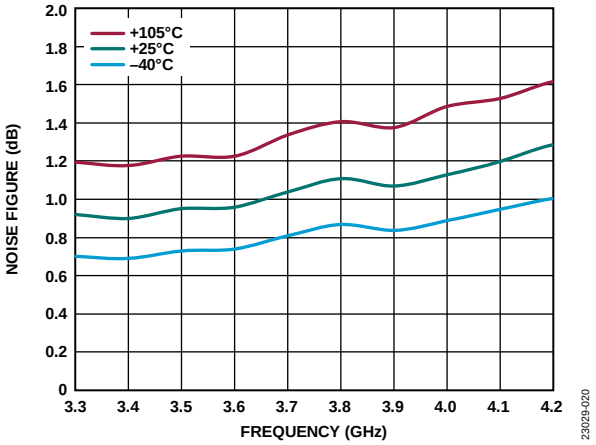


Figure 20. Noise Figure vs. Frequency at Various Temperatures

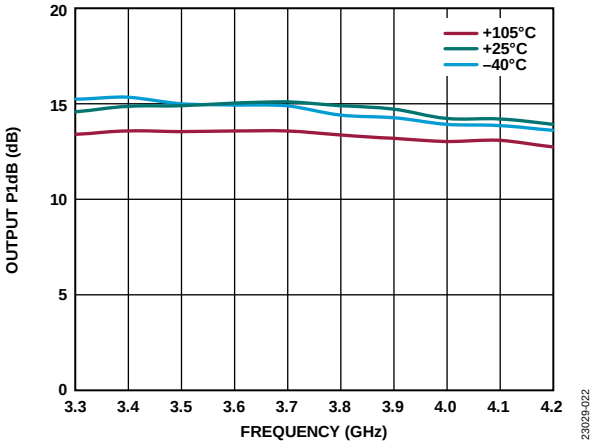


Figure 22. Output P1dB vs. Frequency at Various Temperatures

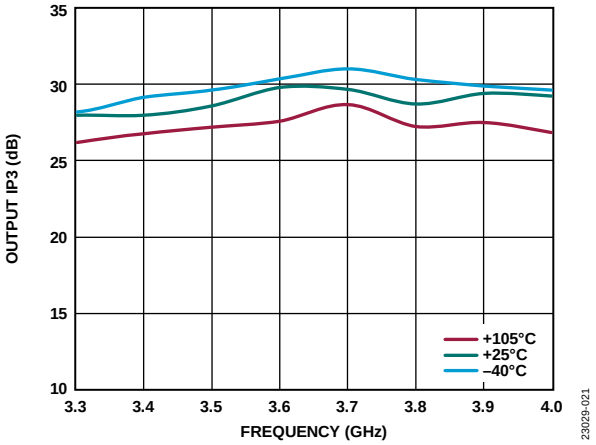


Figure 21. Output IP3 vs. Frequency at Various Temperatures, −10 dBm Output Tone Power

TRANSMIT OPERATION

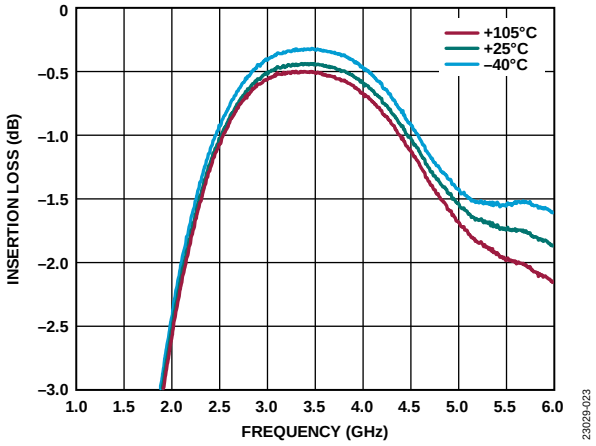


Figure 23. Insertion Loss vs. Frequency at Various Temperatures

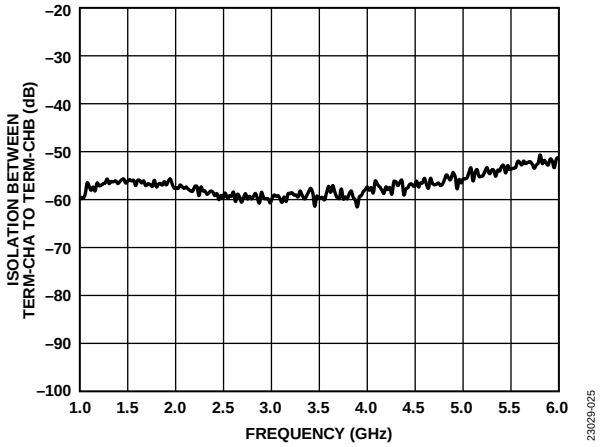


Figure 25. Isolation Between TERM-CHA to TERM-CHB vs. Frequency

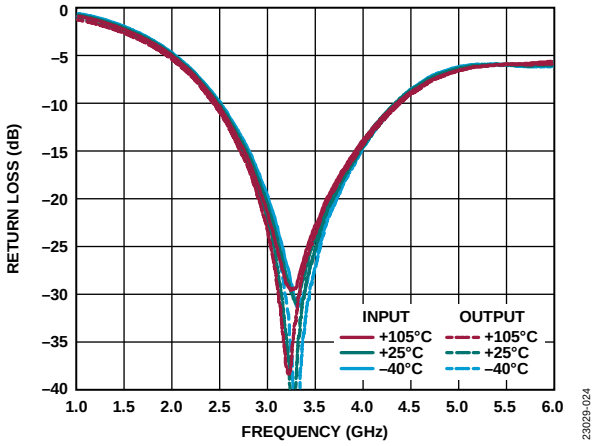


Figure 24. Input/Output Return Loss vs. Frequency at Various Temperatures

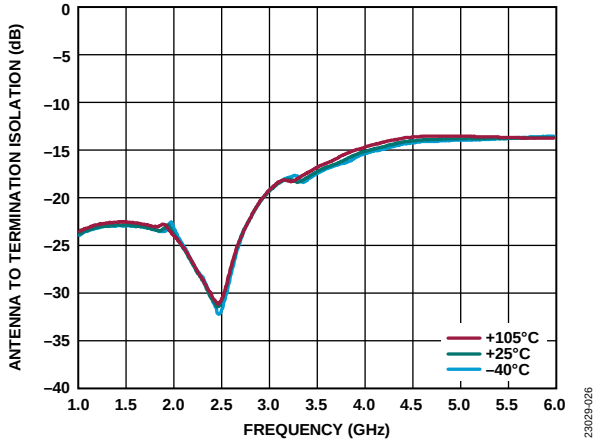


Figure 26. Antenna to Termination Isolation vs. Frequency at Various Temperatures, LNA On

THEORY OF OPERATION

The ADRF5515 requires a positive supply voltage applied to VDD1-CHA, VDD2-CHA, VDD1-CHB, VDD2-CHB, and SWVDD-CHAB. Use bypassing capacitors on the supply lines to filter noise and use 300 Ω series resistors on the BP-CHx and PD-CHAB digital control pins for glitch and overcurrent protection.

SIGNAL PATH SELECT

The ADRF5515 supports transmit operations when 5 V is applied to SWCTRL-CHAB. In transmit operation, when an RF input is applied to ANT-CHA and ANT-CHB, the signal paths are connected from ANT-CHA to TERM-CHA and from ANT-CHB to TERM-CHB.

The ADRF5515 supports receive operations when 0 V is applied to SWCTRL-CHAB. In receive operation, an RF input applied at ANT-CHA and ANT-CHB connects ANT-CHA to RXOUT-CHA and ANT-CHB to RXOUT-CHB.

Transmit Operation

The ADRF5515 supports insertion loss mode and isolation mode when in transmit operation, that is, when SWCTRL-CHAB = 5 V. As detailed in Table 7, with PD-CHAB set to 5 V and BP-CHA or BP-CHB set to 0 V, insertion loss mode is selected. Under the same circumstances, isolation mode is selected by applying 0 V to PD-CHAB.

Receive Operation

The ADRF5515 supports high gain mode, low gain mode, power-down high isolation mode, and power-down low isolation mode in receive operation, as detailed in Table 7.

When 0 V is applied to PD-CHAB, the LNA is powered up and the user can select high gain mode or low gain mode. To select high gain mode, apply 0 V to BP-CHA or BP-CHB. To select low gain mode, apply 5 V to BP-CHA or BP-CHB.

When 5 V is applied to PD-CHAB, the ADRF5515 enters power-down mode. To select power-down high isolation mode, apply 0 V to BP-CHA or BP-CHB. To select power-down low isolation mode, apply 5 V to BP-CHA or BP-CHB.

BIASING SEQUENCE

To bias up the ADRF5515, perform the following steps:

1. Connect GND to ground.
2. Bias up VDD1-CHA, VDD2-CHA, VDD1-CHB, VDD2 CHB, and SWVDD-CHAB.
3. Bias up SWCTRL-CHAB.
4. Bias up PD-CHAB.
5. Bias up BP-CHA and BP-CHB.
6. Apply an RF input signal.

To bias down, perform these steps in the reverse order.

Table 6. Truth Table: Signal Path

	Signal Path Select	
SWCTRL-CHAB	**Transmit Operation[1]**	**Receive Operation**
Low	Off	On
High	On	Off

[1] See the signal path descriptions in Table 6.

Table 7. Truth Table: Operation, SWCTRL-CHAB = Low

Operation	PD-CHAB	BP-CHA, BP-CHB	Signal Path
Receive Operation			ANT-CHA to RXOUT-CHA, ANT-CHB to RXOUT-CHB
High Gain Mode	Low	Low	
Low Gain Mode	Low	High	
Power-Down High Isolation Mode	High	Low	
Power-Down Low Isolation Mode	High	High	

APPLICATIONS INFORMATION

To generate the evaluation PCB used in a typical application circuit (see the ADRF5515-EVALZ user guide for more information), use proper RF circuit design techniques. Signal lines at the RF port must have a 50 Ω impedance, and the package ground leads and the backside ground slug must connect directly to the ground plane. Use 300 Ω series resistors on the BP-CHx and PD-CHAB digital control pins for glitch and overcurrent protection. The evaluation board shown in Figure 27 is available from Analog Devices, Inc., on request. See the ADRF5515-EVALZ user guide for additional information on the evaluation board.

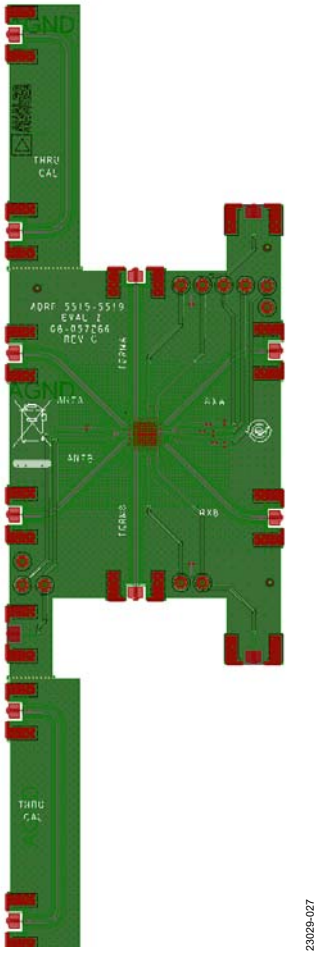
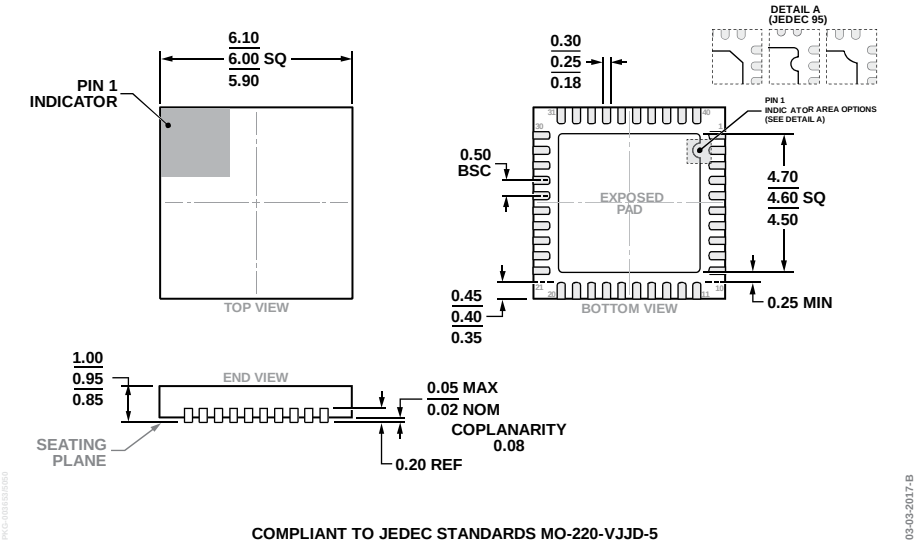


Figure 27. ADRF5515-EVALZ Evaluation Board

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VJJD-5

Figure 28. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.95 mm Package Height
(CP-40-15)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADRF5515BCPZN	−40°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-15
ADRF5515BCPZN-R7	−40°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-15
ADRF5515BCPZN-RL	−40°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-15
ADRF5515-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

©2020 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D23029-11/20(0)