Dual-Channel, 2.3 GHz to 2.8 GHz, 20 W Receiver Front End

FEATURES

- Integrated dual-channel RF front end
  - 2-stage LNA and high power silicon SPDT switch
  - On-chip bias and matching
  - Single-supply operation
- High power handling at T_{CASE} = 105°C
  - LTE average power (9 dB PAR) full lifetime: 43 dBm
- Gain
  - High gain mode: 35 dB typical at 2.6 GHz
  - Low gain mode: 14 dB typical at 2.6 GHz
- Low noise figure
  - High gain mode: 1.0 dB typical at 2.6 GHz
  - Low gain mode: 1.0 dB typical at 2.6 GHz
- High isolation
  - RXOUT-CHA and RXOUT-CHB: 45 dB typical
  - TERM-CHA and TERM-CHB: 60 dB typical
- Low insertion loss: 0.5 dB typical at 2.6 GHz
- High OIP3: 32 dBm typical
- Power-down mode and low gain mode
- Low supply current
  - High gain mode: 110 mA typical at 5 V
  - Low gain mode: 36 mA typical at 5 V
  - Power-down mode: 12 mA typical at 5 V
- Positive logic control
- 6 mm × 6 mm, 40-lead LFCSP package
- Pin compatible with the ADRF5545A and ADRF5549 10 W versions

APPLICATIONS

- Wireless infrastructure
- TDD massive multiple input and multiple output and active antenna systems
- TDD-based communication systems

FUNCTIONAL BLOCK DIAGRAM

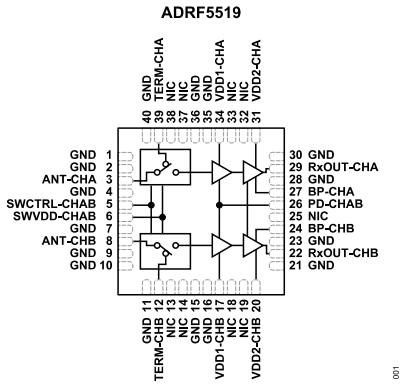


Figure 1.

GENERAL DESCRIPTION

The ADRF5519 is a dual-channel, integrated RF, front-end multichip module designed for time division duplexing (TDD) applications that operates from 2.3 GHz to 2.8 GHz. The ADRF5519 is configured in dual channels with a cascading two-stage low noise amplifier (LNA) and a high power silicon single-pole, double-throw (SPDT) switch.

In high gain mode, the cascaded two-stage LNA and switch offer a low noise figure (NF) of 1.0 dB and a high gain of 35 dB at 2.6 GHz with an output third-order intercept point (OIP3) of 32 dBm (typical). In low gain mode, one stage of the two-stage LNA is in bypass, providing 14 dB of gain at a lower current of 36 mA. In power-down mode, the LNAs are turned off and the device draws 12 mA.

In transmit operation, RF inputs are connected to a termination pin (ANT-CHA or ANT-CHB connected to TERM-CHA or TERM-CHB, respectively). The switch provides a low insertion loss of 0.5 dB and handles a long-term evolution (LTE) average power (9 dB peak to average ratio (PAR)) of 43 dBm for full lifetime operation.

The device comes in a RoHS-compliant, compact, 6 mm × 6 mm, 40-lead LFCSP package.

DOCUMENT FEEDBACK
TECHNICAL SUPPORT

Information furnished by Analog Devices is believed to be accurate and reliable "as is". However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

TABLE OF CONTENTS

Features 1
Applications 1
Functional Block Diagram 1
General Description 1
Specifications 3
  Electrical Specifications 3
Absolute Maximum Ratings 5
  Thermal Resistance 5
  Electrostatic Discharge (ESD) Ratings 5
  ESD Caution 5
Pin Configuration and Function Descriptions 6
Typical Performance Characteristics 8
  Receive Operation, High Gain Mode 8
  Receive Operation, Low Gain Mode 10
  Transmit Operation 12
Theory of Operation 13
  Signal Path Select 13
  Biasing Sequence 13
Applications Information 14
  1.9 GHz Operation 14
Outline Dimensions 16
  Ordering Guide 16
  Evaluation Boards 16

REVISION HISTORY

4/2021—Revision 0: Initial Version:

Updated Features Section 1

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

VDD1-CHA, VDD1-CHB, VDD2-CHA, VDD2-CHB, and SWVDD-CHAB = 5 V, SWCTRL-CHAB = 0 V or SWVDD-CHAB, BP-CHA = VDD1-CHA or 0 V, BP-CHB = VDD1-CHB or 0 V, PD-CHAB = 0 V or VDD1-CHA, case temperature (T_{CASE}) = 25°C, and a 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		2.3		2.8	GHz
GAIN[1]	Receive operation at 2.6 GHz				
High Gain Mode			35		dB
Low Gain Mode			14		dB
GAIN FLATNESS[1]	Receive operation in any 100 MHz bandwidth				
High Gain Mode			0.6		dB
Low Gain Mode			0.2		dB
NOISE FIGURE (NF)[1]	Receive operation at 2.6 GHz				
High Gain Mode			1.0		dB
Low Gain Mode			1.0		dB
OUTPUT THIRD-ORDER INTERCEPT POINT (OIP3)[1]	Receive operation, two-tone output power = 8 dBm per tone at 1 MHz tone spacing				
High Gain Mode			32		dBm
Low Gain Mode			27		dBm
OUTPUT 1 dB COMPRESSION (OP1dB)					
High Gain Mode			18		dBm
Low Gain Mode			13		dBm
INSERTION LOSS[1]	Transmit operation at 2.6 GHz		0.5		dB
CHANNEL TO CHANNEL ISOLATION[1]	At 2.6 GHz				
Between RXOUT-CHA and RXOUT-CHB	Receive operation		45		dB
Between TERM-CHA and TERM-CHB	Transmit operation		65		dB
SWITCH ISOLATION					
ANT-CHA to TERM-CHA and ANT-CHB to TERM-CHB[1]	Receive operation		20		dB
SWITCHING CHARACTERISTICS (t_{ON}, t_{OFF})					
	50% control voltage to 90%, 10% of RXOUT-CHA or RXOUT-CHB in receive operation		900		ns
	50% control voltage to 90%, 10% of TERM-CHA or TERM-CHB in transmit operation		900		ns
DIGITAL INPUT					
SWCTRL-CHAB, PD-CHAB, BP-CHA, BP-CHB					
Low (V_{IL})		0		0.63	V
High (V_{IH})		1.17		V_{DD}	V
SUPPLY CURRENT (I_{DD})	VDD1-CHx and VDD2-CHx = 5 V per channel				
High Gain			110		mA
Low Gain			36		mA
Power-Down Mode			12		mA
Transmit Current (Switch)	SWVDD-CHAB = 5 V		1.55		mA
DIGITAL INPUT CURRENTS	SWCTRL-CHAB, PD-CHAB, BP-CHA, BP-CHB = 5 V per channel				
SWCTRL-CHAB			0.084		mA
PD-CHAB			0.3		mA
BP-CHA, BP-CHB			0.15		mA

SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RECOMMENDED OPERATING CONDITIONS					
Supply Voltage (VDD) Range	VDD1-CHA, VDD1-CHB, VDD2-CHA, VDD2-CHB, SWVDD-CHAB	4.75	5	5.25	V
Control Voltage Range	SWCTRL-CHAB, BP-CHA, BP-CHB, PD-CHAB	0		V_{DD}	V
RF Input Power at ANT-CHA, ANT-CHB	SWCTRL-CHAB = 5 V, PD-CHAB = 5 V, BP-CHA = BP-CHB = 0 V, T_{CASE}[2] = 105°C				
	Continuous wave			43	dBm
	9 dB PAR LTE full lifetime average			43	dBm
	7 dB PAR LTE single event (<10 sec) average[3]			46	dBm
Case Temperature Range (T_{CASE}) [2]		−40		+105	°C
Junction Temperature at Maximum T_{CASE}[2]					
	Receive operation[1]			132	°C
	Transmit operation[1]			134	°C

[1] See Table 6 and Table 7.

[2] Measured at EPAD.

[3] PAR > 7 dB has not been validated due to measurement setup limited to a maximum RF power of 53 dBm.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Positive Supply Voltage	
VDD1-CHA, VDD1-CHB, VDD2-CHA, VDD2-CHB	7 V
SWVDD-CHAB	5.4 V
Digital Control Input Voltage	
SWCTRL-CHAB	−0.3 V to V_{DD}[1] + 0.3 V
BP-CHA, BP-CHB, PD-CHAB	−0.3 V to V_{DD}[2] + 0.3 V
Digital Control Input Current	
SWCTRL-CHAB, BP-CHA, BP-CHB, PD-CHAB	20 mA
RF Input Power	
Transmit Input Power (LTE Peak, 9 dB PAR)	53 dBm
Receive Input Power (LTE Peak, 9 dB PAR)	25 dBm
Temperature	
Storage	−65°C to +150°C
Reflow (Moisture Sensitivity Level 3 (MSL3) Rating)	260°C

[1] V_{DD} is the voltage of the SWVDD-CHAB pin.

[2] V_{DD} is the voltage of the VDD1-CHA, VDD1-CHB, VDD2-CHA, and VDD2-CHB pins.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operation environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}	Unit
CP-40-15		
High Gain Mode, Receive Operation	25	°C/W
Low Gain Mode, Receive Operation	36	°C/W
Power-Down Mode, Transmit Operation	6	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

Table 4. ADRF5519, 40-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	1000	1C
CDM	750	C2

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

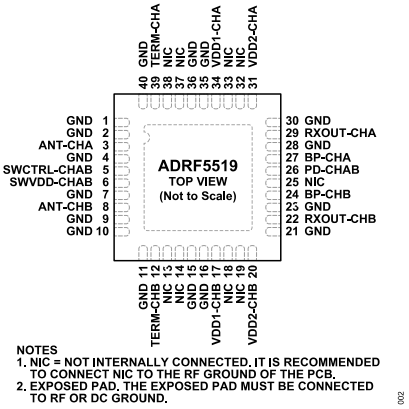


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4, 7, 9 to 11, 15, 16, 21, 23, 28, 30, 35, 36, 40	GND	Ground.
3	ANT-CHA	RF Input to Channel A.
5	SWCTRL-CHAB	Control Voltage for Switches on Channel A and Channel B.
6	SWVDD-CHAB	Supply Voltage for Switches on Channel A and Channel B.
8	ANT-CHB	RF Input to Channel B.
12	TERM-CHB	Termination Output. This pin is the transmitter path for Channel B.
13, 14, 18, 19, 25, 32, 33, 37, 38	NIC	Not Internally Connected. It is recommended to connect NIC to the RF ground of the PCB.
17	VDD1-CHB	Supply Voltage for Stage 1 LNA on Channel B.
20	VDD2-CHB	Supply Voltage for Stage 2 LNA on Channel B.
22	RXOUT-CHB	RF Output. This pin is the receiver path for Channel B. The RXOUT-CHB pin is ac matched to 50 Ω. No matching component is required. A dc blocking capacitor is required.
24	BP-CHB	Bypass Second Stage LNA of Channel B.
26	PD-CHAB	Power-Down All Stages of LNA for Channel A and Channel B.
27	BP-CHA	Bypass Second Stage LNA of Channel A.
29	RXOUT-CHA	RF Output. This pin is the receiver path for Channel A. The RXOUT-CHA pin is ac matched to 50 Ω. No matching component is required. A dc blocking capacitor is required.
31	VDD2-CHA	Supply Voltage for Stage 2 LNA on Channel A.
34	VDD1-CHA	Supply Voltage for Stage 1 LNA on Channel A.
39	TERM-CHA	Termination Output. This pin is the transmitter path for Channel A.
	EPAD	Exposed Pad. The exposed pad must be connected to RF or dc ground.

Interface Schematics



Figure 3. GND Interface

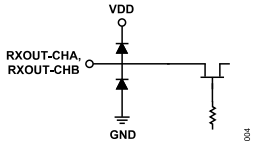


Figure 4. RXOUT-CHx Interface

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

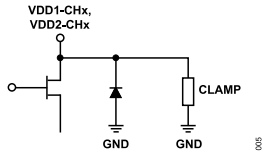


Figure 5. VDD1-CHx, VDD2-CHx Interface

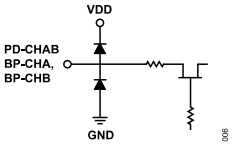


Figure 6. PD-CHAB, BP-CHx Interface

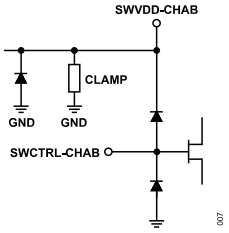


Figure 7. SWCTRL-CHAB, SWVDD-CHAB Interface

TYPICAL PERFORMANCE CHARACTERISTICS

RECEIVE OPERATION, HIGH GAIN MODE

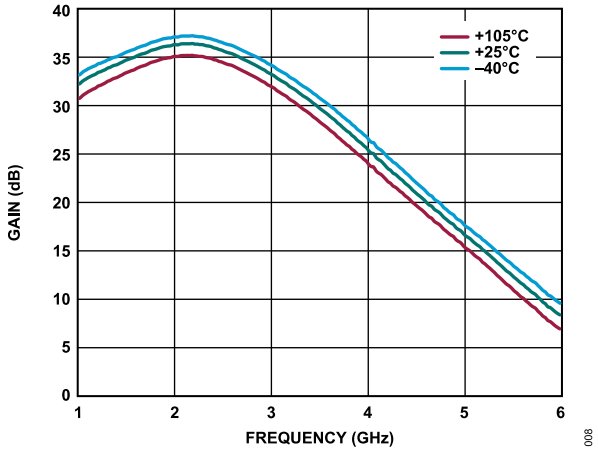


Figure 8. Gain vs. Frequency at Various Temperatures

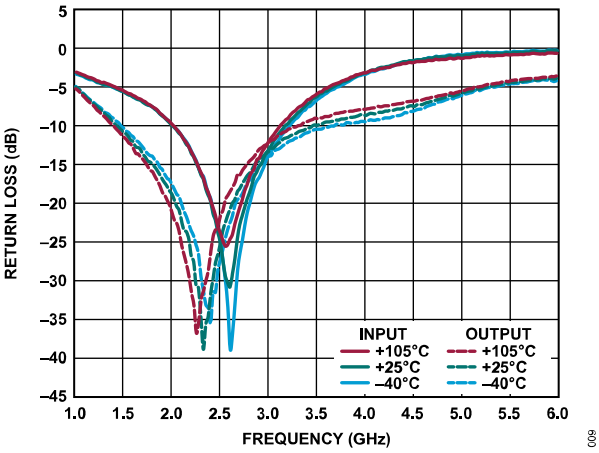


Figure 9. Return Loss vs. Frequency

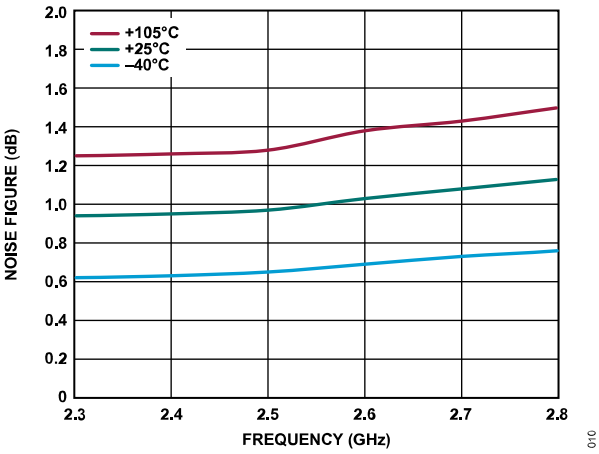


Figure 10. Noise Figure vs. Frequency

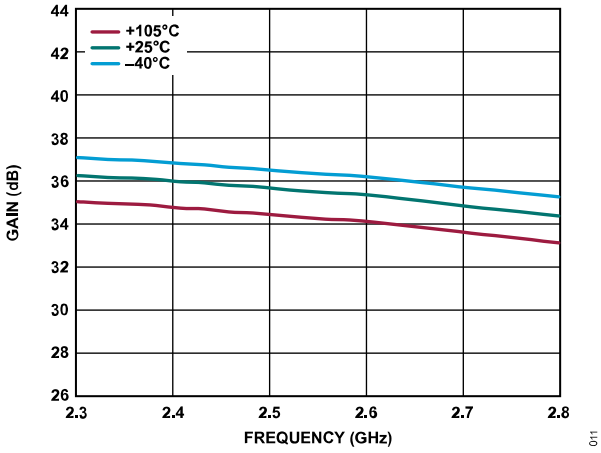


Figure 11. Gain vs. Frequency at Various Temperatures, 2.3 GHz to 2.8 GHz

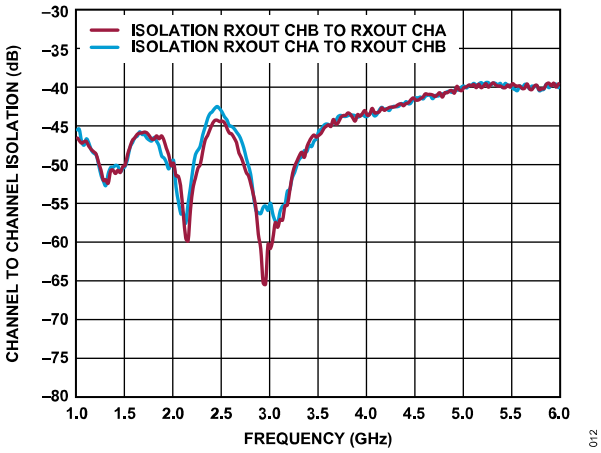


Figure 12. Channel to Channel Isolation vs. Frequency

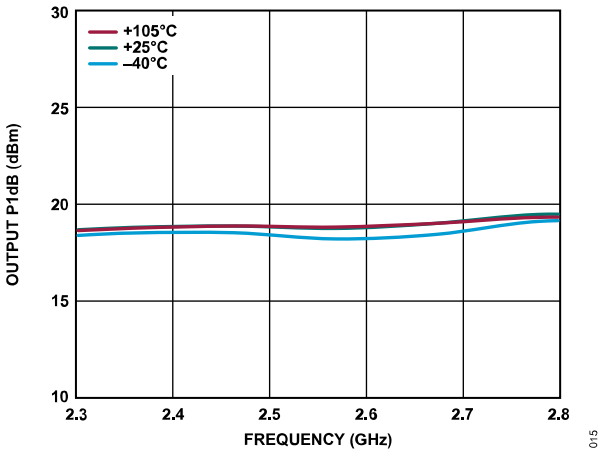


Figure 13. Output P1dB vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

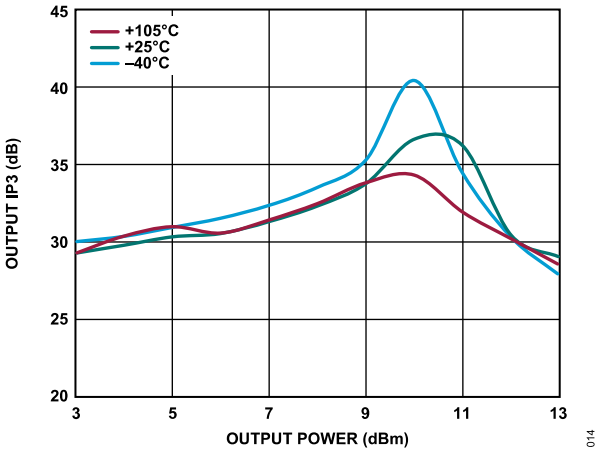


Figure 14. Output IP3 vs. Output Power, 2.6 GHz

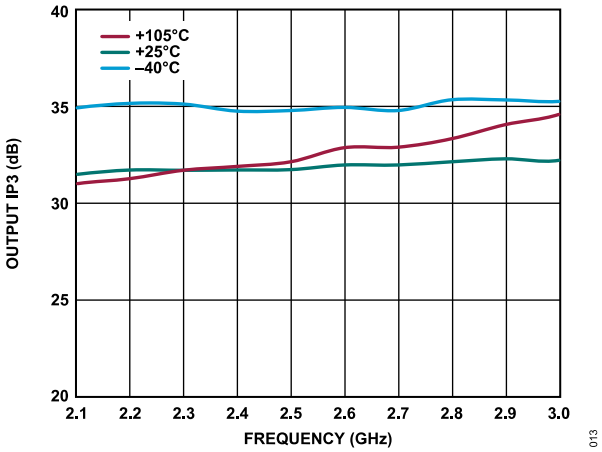


Figure 15. Output IP3 vs. Frequency, 8 dBm Output Tone Power

TYPICAL PERFORMANCE CHARACTERISTICS

RECEIVE OPERATION, LOW GAIN MODE

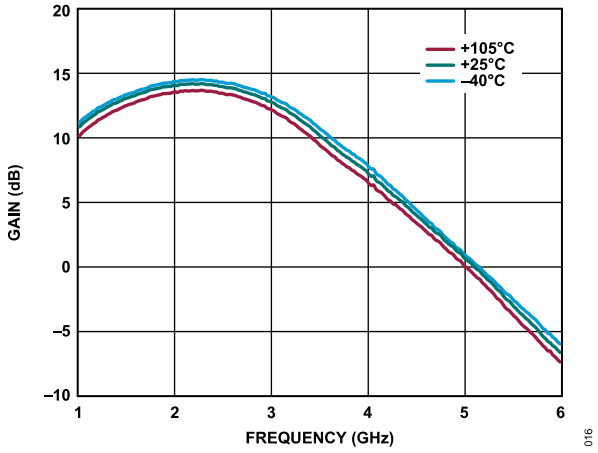


Figure 16. Gain vs. Frequency at Various Temperatures

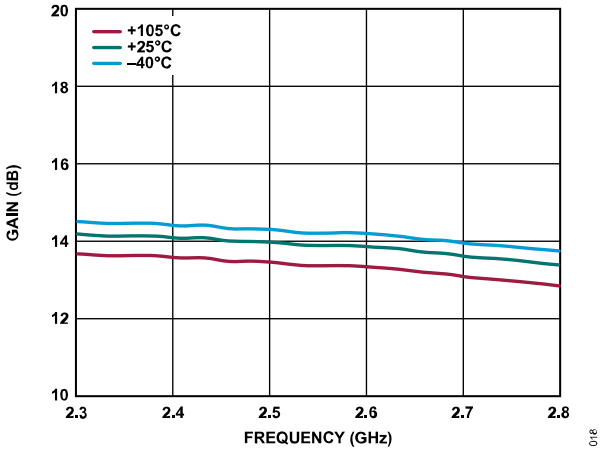


Figure 18. Gain vs. Frequency at Various Temperatures, 2.3 GHz to 2.8 GHz

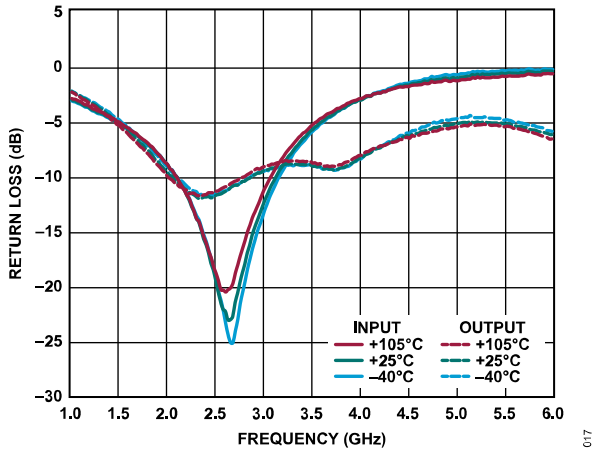


Figure 17. Return Loss vs. Frequency

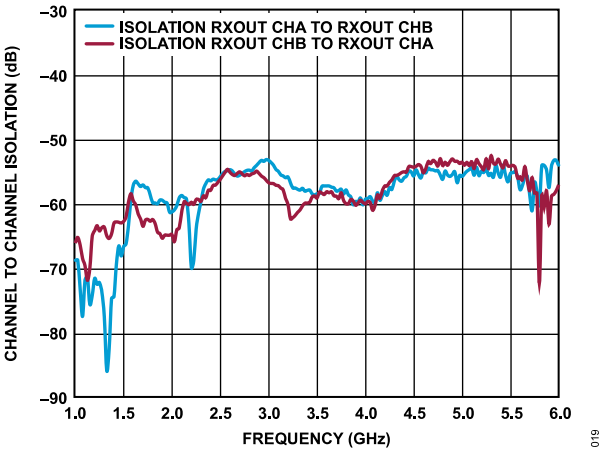


Figure 19. Channel to Channel Isolation vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

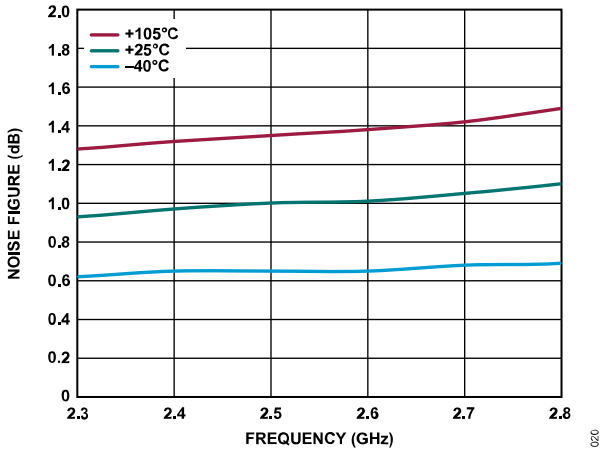


Figure 20. Noise Figure vs. Frequency at Various Temperatures

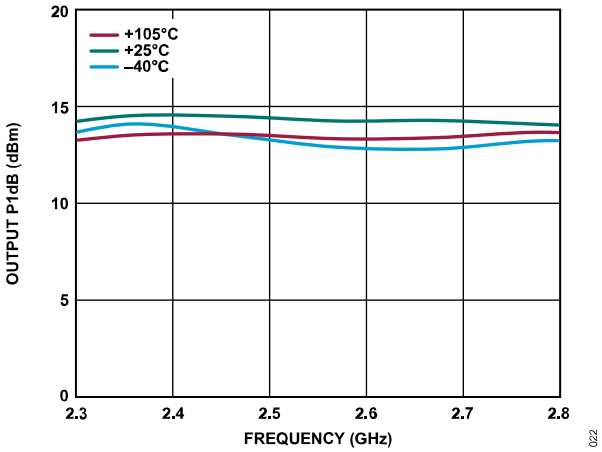


Figure 22. Output P1dB vs. Frequency

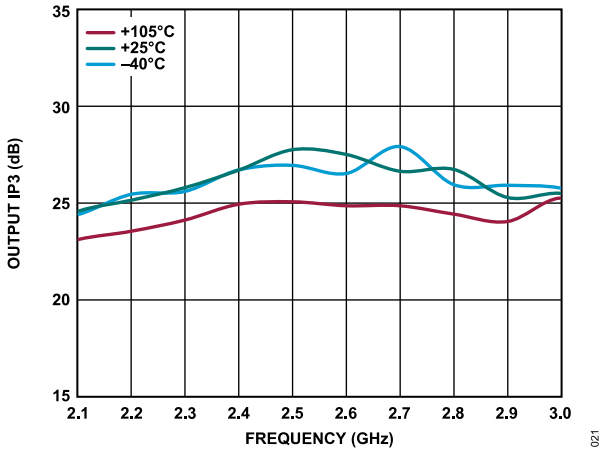


Figure 21. Output IP3 vs. Frequency at −10 dBm Output Tone Power

TYPICAL PERFORMANCE CHARACTERISTICS

TRANSMIT OPERATION

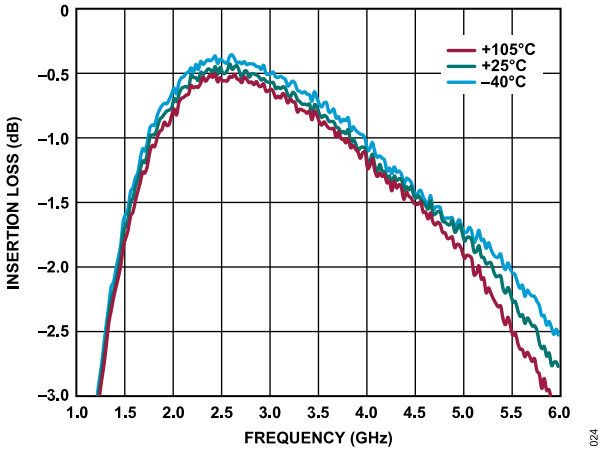


Figure 23. Insertion Loss vs. Frequency at Various Temperatures

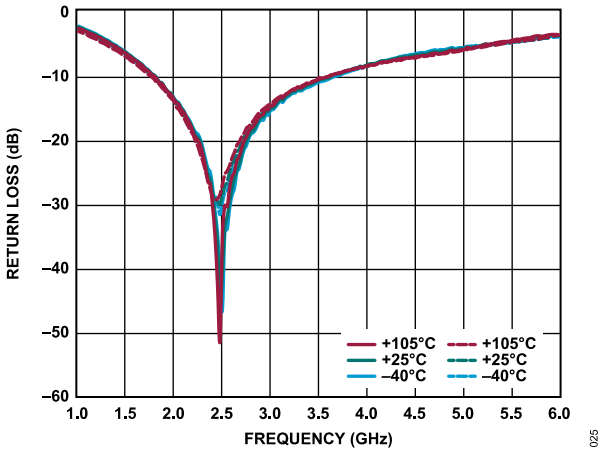


Figure 24. Return Loss vs. Frequency

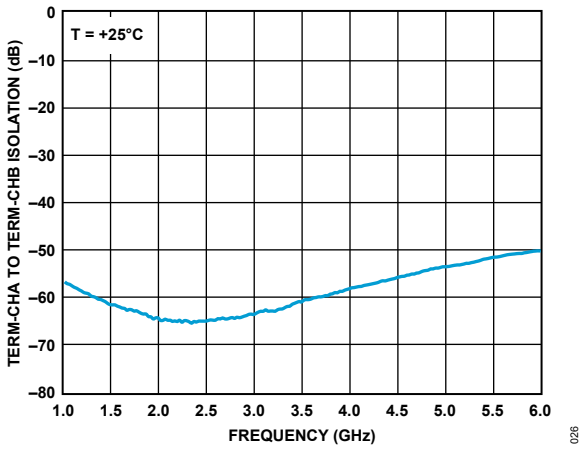


Figure 25. TERM-CHA to TERM-CHB Isolation vs. Frequency

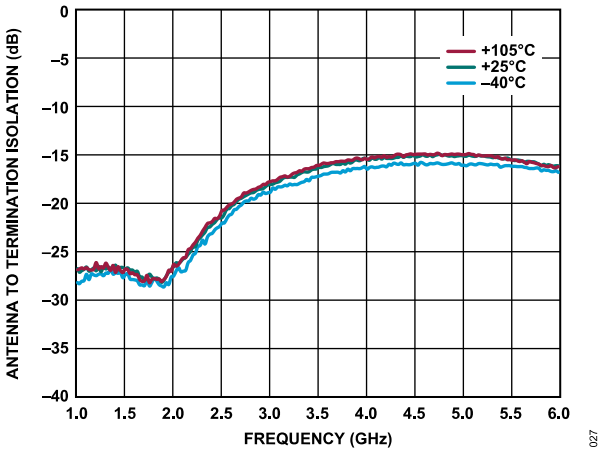


Figure 26. Antenna to Termination Isolation vs. Frequency, LNA On

THEORY OF OPERATION

The ADRF5519 requires a positive supply voltage applied to the VDD1-CHA pin, VDD2-CHA pin, VDD1-CHB pin, VDD2-CHB pin, and SWVDD-CHAB pin. Use bypassing capacitors on the supply lines to filter noise.

SIGNAL PATH SELECT

The ADRF5519 supports transmit operations when 5 V is applied to SWCTRL-CHAB. In transmit operation, when an RF input is applied to ANT-CHA and ANT-CHB, the signal paths are connected from ANT-CHA to TERM-CHA and from ANT-CHB to TERM-CHB.

The ADRF5519 supports receive operations when 0 V is applied to SWCTRL-CHAB. In receive operation, an RF input applied at ANT-CHA and ANT-CHB connects ANT-CHA to RXOUT-CHA and ANT-CHB to RXOUT-CHB.

Receive Operation

The ADRF5519 supports high gain mode, low gain mode, power-down high isolation mode, and power-down low isolation mode in receive operation, as detailed in Table 7.

When 0 V is applied to PD-CHAB, the LNA is powered up and the user can select high gain mode or low gain mode. To select high gain mode, apply 0 V to BP-CHA or BP-CHB. To select low gain mode, apply 5 V to BP-CHA or BP-CHB.

When 5 V is applied to PD-CHAB, the ADRF5519 enters power-down mode. To select power-down high isolation mode, apply 0 V to BP-CHA or BP-CHB. To select power-down low isolation mode, apply 5 V to BP-CHA or BP-CHB.

BIASING SEQUENCE

To bias up the ADRF5519, perform the following steps:

1. Connect any GND pin to ground.
2. Bias up VDD1-CHA, VDD2-CHA, VDD1-CHB, VDD2-CHB, and SWVDD-CHAB.
3. Bias up SWCTRL-CHAB.
4. Bias up PD-CHAB.
5. Bias up BP-CHA and BP-CHB.
6. Apply an RF input signal.

To bias down, perform these steps in the reverse order.

Table 6. Truth Table: Signal Path

	Signal Path Select	
SWCTRL-CHAB	**Transmit Operation[1]**	**Receive Operation**
Low	Off	On
High	On	Off

[1] See the signal path descriptions in Table 7.

Table 7. Truth Table: Receive Operation, SWCTRL-CHAB = 0 V

Operation	PD-CHAB	BP-CHA, BP-CHB	Signal Path
Receive Operation			ANT-CHA to RXOUT-CHA, ANT-CHB to RXOUT-CHB
High Gain Mode	Low	Low	
Low Gain Mode	Low	High	
Power-Down High Isolation Mode	High	Low	
Power-Down Low Isolation Mode	High	High	

APPLICATIONS INFORMATION

To generate the evaluation PCB used in a typical application circuit, use proper RF circuit design techniques. Signal lines at the RF port must have a 50 Ω impedance, and the package ground leads and the backside ground slug must connect directly to the ground plane. Use 300 Ω series resistors on the BP-CHx and PD-CHAB digital control pins for glitch and overcurrent protection. The ADRF5519-EVALZ is available from Analog Devices, Inc., upon request.

1.9 GHZ OPERATION

The ADRF5519 can be used for applications at 1.9 GHz, tuned from 1.7 GHz to 2.1 GHz, and 3 dB derated from Table 1 power rating. Table 9 shows the typical specifications of the ADRF5519-EVALZ tuned at 1.9 GHz.

Table 8 lists the required matching components. The ADRF5519-EVALZ is assembled and shipped without any matching components by default. The ADRF5519-EVALZ can be tuned for a 1.9 GHz application with a series RF trace and a parallel capacitor, as shown in Table 8.

Table 8. Matching Components

Matching Components	Series RF Trace	Parallel Capacitor
ANT_x Pin	Z_0 = 50 Ω $\lambda/8 \ at \ 1.9 \ GHz$ 11.7 mm for ADRF5519-EVALZ	1 pF[1]
TERM_x Pin	<1.5 mm	1.2 pF[1]

[1] ATC 600S 0603 Series

The simulated tuning performance at receive mode and transmit mode is shown in Figure 27 and Figure 28.

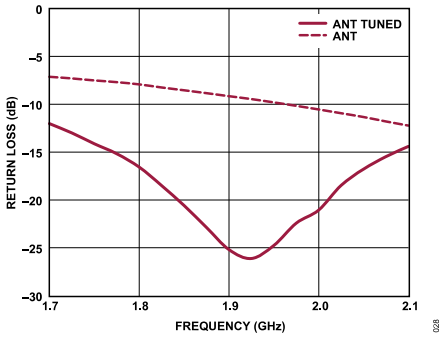


Figure 27. ANT-CHx Return Loss with and Without Tuning at Receive Mode

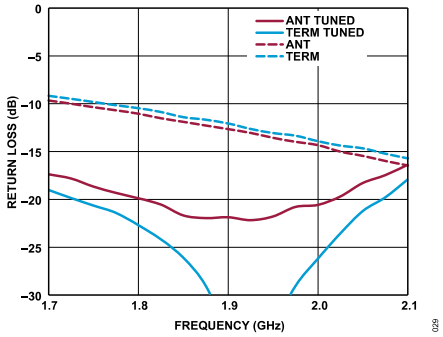


Figure 28. ANT-CHx and TERM-CHx Return Loss with and Without Tuning at Transmit Mode

Table 9. Typical Specifications at 1.9 GHz with Recommended Matching

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GAIN[1]	Receive operation at 1.9 GHz				
High Gain Mode			35		dB
Low Gain Mode			13		dB
GAIN FLATNESS	Receive operation from 1.7 GHz to 2.1 GHz				
High Gain Mode			0.5		dB
Low Gain Mode			0.5		dB
NOISE FIGURE (NF)[1]	Receive operation at 1.9 GHz				
High Gain Mode			0.9		dB
Low Gain Mode			0.9		dB
OUTPUT THIRD ORDER INTERCEPT POINT (OIP3)[1]	Receive operation, per tone at 1 MHz tone spacing at 1.9 GHz				
High Gain Mode	Output power = 8 dBm per tone		30		dBm
Low Gain Mode	Output power = −10 dBm per tone		22		dBm
OUTPUT 1 dB COMPRESSION (OP1dB)	Receive operation at 1.9 GHz				
High Gain Mode			17		dBm
Low Gain Mode			12		dBm
INSERTION LOSS[1]	Transmit operation at 1.9 GHz		0.55		dB

APPLICATIONS INFORMATION

Table 9. Typical Specifications at 1.9 GHz with Recommended Matching

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RETURN LOSS	At 1.9 GHz				
ANT-CHA and ANT-CHB	Receive operation		>20		dB
RXOUT-CHA and RXOUT-CHB			>20		dB
ANT-CHA and ANT-CHB	Transmit operation		>20		dB
TERM-CHA and TERM-CHB			>20		dB
RF INPUT POWER at ANT-CHA, ANT-CHB	SWCTRL-CHAB = 5 V, PD-CHAB = 5 V, BP-CHA = BP-CHB = 0 V, T_{CASE} = 105°C				
	Continuous wave at 1.9 GHz			40	dBm
	9 dB PAR LTE full lifetime average at 1.9 GHz			40	dBm

[1] See Table 6 and Table 7.

OUTLINE DIMENSIONS

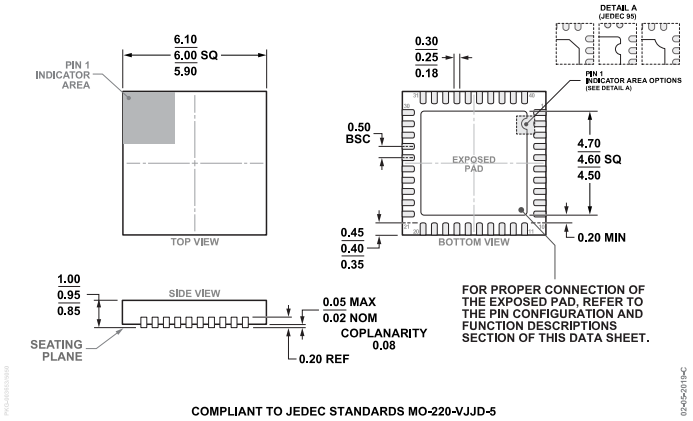


Figure 29. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.95 mm Package Height
(CP-40-15)
Dimensions shown in millimeters

Updated: April 09, 2021

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADRF5519BCPZN	−40°C to +105°C	40-Lead LFCSP (6mm × 6mm w/ EP)	Reel, 0	CP-40-15
ADRF5519BCPZN-R7	−40°C to +105°C	40-Lead LFCSP (6mm × 6mm w/ EP)	Reel, 750	CP-40-15
ADRF5519BCPZN-RL	−40°C to +105°C	40-Lead LFCSP (6mm × 6mm w/ EP)	Reel, 2500	CP-40-15

[1] Z = RoHS Compliant Part

EVALUATION BOARDS

ADRF5519-EVALZ	ADRF5519 Evaluation Board

©2021 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.