SLWS160A − FEBRUARY 2005 − REVIISED JANUARY 2010

14 Bit, 80 MSPS Analog-to-Digital Converter

FEATURES

- 14 Bit Resolution
- 80 MSPS Maximum Sample Rate
- SNR = 74 dBc at 80 MSPS and 50 MHz IF
- SFDR = 94 dBc at 80 MSPS and 50 MHz IF
- 2.2 V_{pp} Differential Input Range
- 5 V Supply Operation
- 3.3 V CMOS Compatible Outputs
- 1.85 W Total Power Dissipation
- 2s Complement Output Format
- On-Chip Input Analog Buffer, Track and Hold, and Reference Circuit
- 52 Pin HTQFP Package With Exposed Heatsink
- Pin Compatible to the AD6644/45
- Industrial Temperature Range = −40°C to 85°C

APPLICATIONS

- Single and Multichannel Digital Receivers
- Base Station Infrastructure
- Instrumentation
- Video and Imaging

RELATED DEVICES

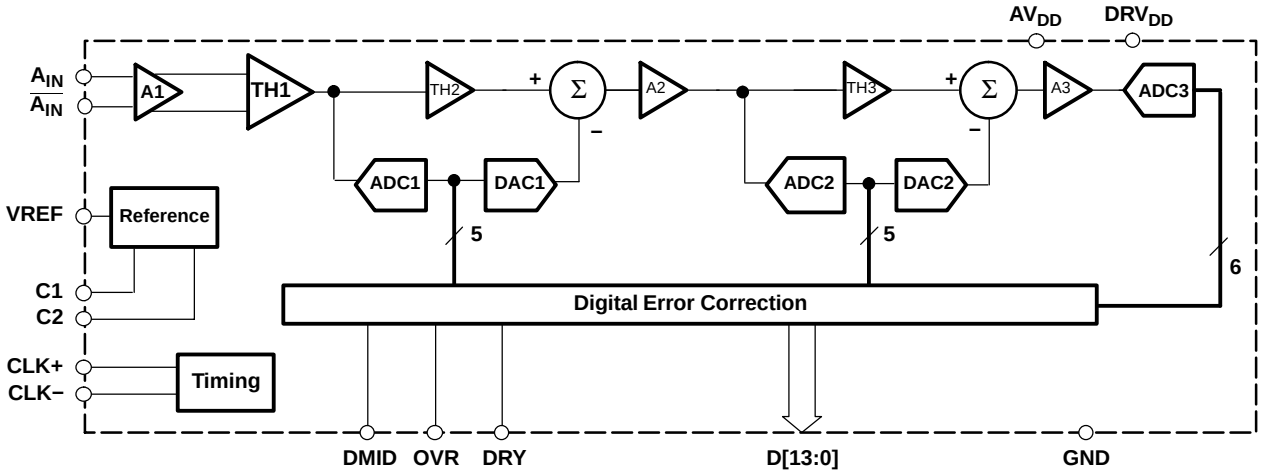
- Clocking: CDC7005
- Amplifiers: OPA695, THS4509

DESCRIPTION

The ADS5423 is a 14 bit 80 MSPS analog-to-digital converter (ADC) that operates from a 5 V supply, while providing 3.3 V CMOS compatible digital outputs. The ADS5423 input buffer isolates the internal switching of the on-chip Track and Hold (T&H) from disturbing the signal source. An internal reference generator is also provided to further simplify the system design. The ADS5423 has outstanding low noise and linearity, over input frequency. With only a 2.2 V_{PP} input range, simplifies the design of multicarrier applications, where the carriers are selected on the digital domain.

The ADS5423 is available in a 52 pin HTQFP with heatsink package and is pin compatible to the AD6645. The ADS5423 is built on state of the art Texas Instruments complementary bipolar process (BiCom3) and is specified over full industrial temperature range (−40°C to 85°C).

FUNCTIONAL BLOCK DIAGRAM



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NOTE:

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted[1]

		ADS5423	UNIT
Supply voltage	AV_{DD} to GND	6	V
	DRV_{DD} to GND	5	
Analog input to GND		−0.3 to AV_{DD} + 0.3	V
Clock input to GND		−0.3 to AV_{DD} + 0.3	V
CLK to $\overline{CLK}$		±2.5	V
Digital data output to GND		−0.3 to DRV_{DD} + 0.3	V
Operating temperature range		−40 to 85	°C
Maximum junction temperature		150	°C
Storage temperature range		−65 to 150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

THERMAL CHARACTERISTICS[1]

PARAMETER	TEST CONDITIONS	TYP	UNIT
θ_{JA}	Soldered slug, no airflow	22.5	°C/W
θ_{JA}	Soldered slug, 200-LPFM airflow	15.8	°C/W
θ_{JA}	Unsoldered slug, no airflow	33.3	°C/W
θ_{JA}	Unsoldered slug, 200-LPFM airflow	25.9	°C/W
θ_{JC}	Bottom of package (heatslug)	2	°C/W

(1) Using 25 thermal vias (5 x 5 array). See the Application Section.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because small parametric changes could cause the device not to meet its published specifications.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
Supplies				
Analog supply voltage, AV_{DD}	4.75	5	5.25	V
Output driver supply voltage, DRV_{DD}	3	3.3	3.6	V
Analog Input				
Differential input range		2.2		V_{PP}
Input common-mode voltage, V_{CM}		2.4		V
Digital Output				
Maximum output load		10		pF
Clock Input				
ADCLK input sample rate (sine wave) $1/t_C$	30		80	MSPS
Clock amplitude, sine wave, differential[1]		3		V_{PP}
Clock duty cycle[2]		50%		
Open free-air temperature range	−40		85	°C

(1) See Figure 17 and Figure 18 for more information.
(2) See Figure 16 for more information.

ELECTRICAL CHARACTERISTICS

Over full temperature range (T_{MIN} = −40°C to T_{MAX} = 85°C), sampling rate = 80 MSPS, 50% clock duty cycle, AV_{DD} = 5 V, DRV_{DD} = 3.3 V, −1 dBFS differential input, and 3 V_{PP} differential sinusoidal clock, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			14		Bits
Analog Inputs					
Differential input range			2.2		V_{PP}
Differential input resistance	See Figure 30		1		kΩ
Differential input capacitance	See Figure 30		1.5		pF
Analog input bandwidth			570		MHz
Internal Reference Voltages					
Reference voltage, V_{REF}			2.4		V
Dynamic Accuracy					
No missing codes			Tested		
Differential linearity error, DNL	f_{IN} = 5 MHz	−0.95	±0.5	1.5	LSB
Integral linearity error, INL	f_{IN} = 5 MHz		±1.5		LSB
Offset error		−5	0	5	mV
Offset temperature coefficient			1.7		ppm/°C
Gain error		−5	0.9	5	%FS
PSRR			1		mV/V
Gain temperature coefficient			77		ppm/°C
Power Supply					
Analog supply current, I_{AVDD}	V_{IN} = full scale, f_{IN} = 70 MHz		355	410	mA
Output buffer supply current, I_{DRVDD}	V_{IN} = full scale, f_{IN} = 70 MHz		35	42	mA
Power dissipation	Total power with 10-pF load on each digital output to ground, f_{IN} = 70 MHz		1.85	2.2	W
Power-up time			20	100	ms
Dynamic AC Characteristics					
Signal-to-noise ratio, SNR	f_{IN} = 10 MHz		74.6		dBc
	f_{IN} = 30 MHz	73	74.3		
	f_{IN} = 50 MHz		74.2		
	f_{IN} = 70 MHz	73	74.1		
	f_{IN} = 100 MHz		73.5		
	f_{IN} = 170 MHz		72		
	f_{IN} = 230 MHz		71.5		
Spurious-free dynamic range, SFDR	f_{IN} = 10 MHz		94		dBc
	f_{IN} = 30 MHz	85	93		
	f_{IN} = 50 MHz		94		
	f_{IN} = 70 MHz		90		
	f_{IN} = 100 MHz		86		
	f_{IN} = 170 MHz		73		
	f_{IN} = 230 MHz		64		

ELECTRICAL CHARACTERISTICS

Over full temperature range (T_{MIN} = −40°C to T_{MAX} = 85°C), sampling rate = 80 MSPS, 50% clock duty cycle, AV_{DD} = 5 V, DRV_{DD} = 3.3 V, −1 dBFS differential input, and 3 V_{PP} differential sinusoidal clock, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-noise + distortion, SINAD	f_{IN} = 10 MHz		74.6		dBc
	f_{IN} = 30 MHz	72.8	74.2		
	f_{IN} = 50 MHz		74.1		
	f_{IN} = 70 MHz		73.9		
	f_{IN} = 100 MHz		72.7		
	f_{IN} = 170 MHz		69.1		
	f_{IN} = 230 MHz		62.8		
Second harmonic, HD2	f_{IN} = 10 MHz		105		dBc
	f_{IN} = 30 MHz		100		
	f_{IN} = 50 MHz		99		
	f_{IN} = 70 MHz		92		
	f_{IN} = 100 MHz		90		
	f_{IN} = 170 MHz		94		
	f_{IN} = 230 MHz		88		
Third harmonic, HD3	f_{IN} = 10 MHz		94		dBc
	f_{IN} = 30 MHz		93		
	f_{IN} = 50 MHz		94		
	f_{IN} = 70 MHz		90		
	f_{IN} = 100 MHz		86		
	f_{IN} = 170 MHz		73		
	f_{IN} = 230 MHz		64		
Worst-harmonic / spur (other than HD2 and HD3)	f_{IN} = 10 MHz		94		dBc
	f_{IN} = 30 MHz		95		
	f_{IN} = 50 MHz		95		
	f_{IN} = 70 MHz		90		
	f_{IN} = 100 MHz		88		
	f_{IN} = 170 MHz		88		
	f_{IN} = 230 MHz		88		
RMS idle channel noise	Input pins tied together		0.9		LSB

DIGITAL CHARACTERISTICS

Over full temperature range (T_{MIN} = −40°C to T_{MAX} = 85°C), AV_{DD} = 5 V, DRV_{DD} = 3.3 V, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Outputs					
Low-level output voltage	C_{LOAD} = 10 pF(1)		0.1	0.6	V
High-level output voltage	C_{LOAD} = 10 pF(1)	2.6	3.2		V
Output capacitance			3		pF
DMID			$DRV_{DD}/2$		V

(1) Equivalent capacitance to ground of (load + parasitics of transmission lines).

TIMING CHARACTERISTICS[3]

Over full temperature range, AV_{DD} = 5 V, DRV_{DD} = 3.3 V, sampling rate = 80 MSPS

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
Aperture Time					
t_A	Aperture delay		500		ps
t_J	Clock slope independent aperture uncertainity (jitter)		150		fs
k_J	Clock slope dependent jitter factor		50		µV
Clock Input					
t_{CLK}	Clock period		12.5		ns
t_{CLKH}[1]	Clock pulsewidth high		6.25		ns
t_{CLKL}[1]	Clock pulsewidth low		6.25		ns
Clock to DataReady (DRY)					
t_{DR}	Clock rising 50% to DRY falling 50%	2.8	3.9	4.7	ns
t_{C_DR}	Clock rising 50% to DRY rising 50%		t_{DR} + t_{CLKH}		ns
$t_{C_DR_50\%}$	Clock rising 50% to DRY rising 50% with 50% duty cycle clock	9	10.1	11	ns
Clock to DATA, OVR[4]					
t_r	Data V_{OL} to data V_{OH} (rise time)		2		ns
t_f	Data V_{OH} to data V_{OL} (fall time)		2		ns
L	Latency		3		Cycles
$t_{su(C)}$	Valid DATA[2] to clock 50% with 50% duty cycle clock (setup time)	4.8	6.3		ns
$t_{H(C)}$	Clock 50% to invalid DATA[2] (hold time)	2.6	3.6		ns
DataReady (DRY) to DATA, OVR[4]					
$t_{su(DR)_50\%}$	Valid DATA[2] to DRY 50% with 50% duty cycle clock (setup time)	3.3	4		ns
$t_{h(DR)_50\%}$	DRY 50% to invalid DATA[2] with 50% duty cycle clock (hold time)	5.4	5.9		ns

(1) See Figure 1 for more information.
(2) See V_{OH} and V_{OL} levels.
(3) All values obtained from design and characterization.
(4) Data is updated with clock rising edge or DRY falling edge.

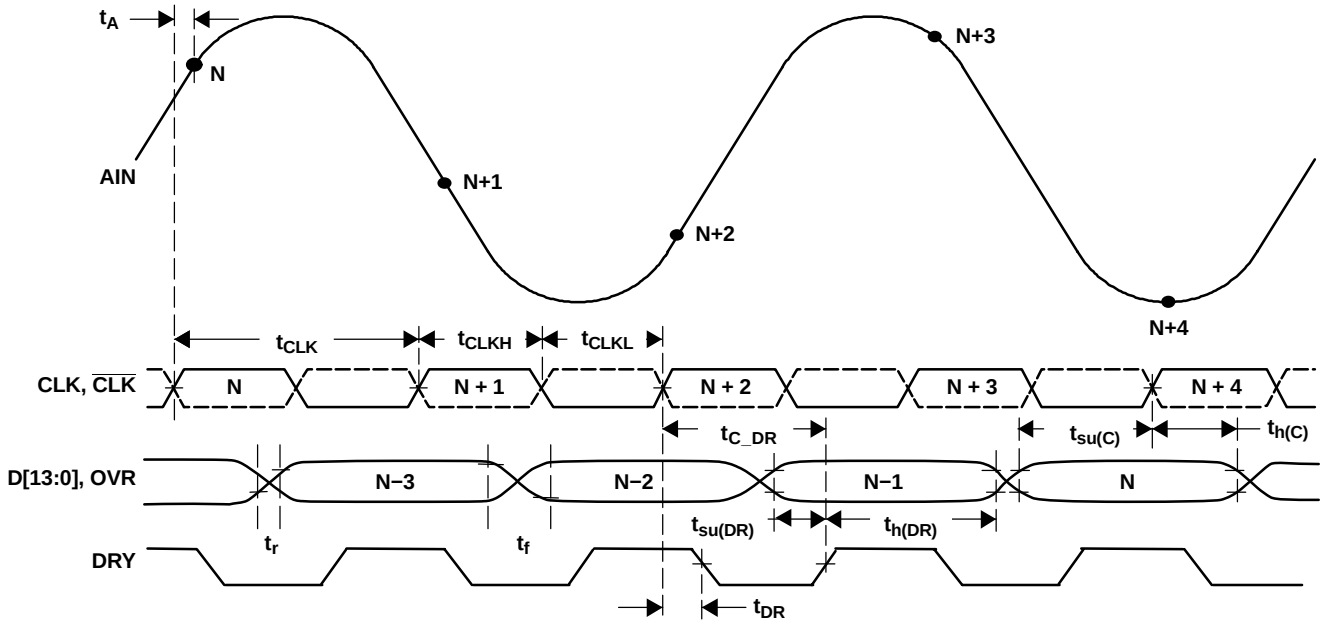
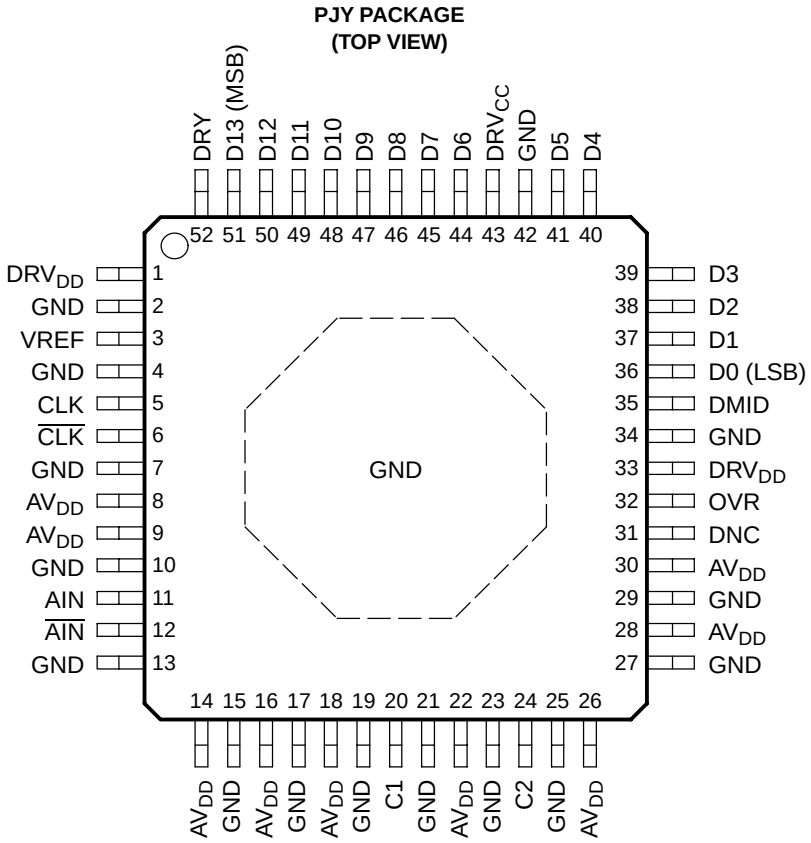


Figure 1. Timing Diagram

PIN CONFIGURATION



PIN ASSIGNMENTS

TERMINAL		DESCRIPTION
NAME	NO.	
DRV_{DD}	1, 33, 43	3.3 V power supply, digital output stage only
GND	2, 4, 7, 10, 13, 15, 17, 19, 21, 23, 25, 27, 29, 34, 42	Ground
VREF	3	2.4 V reference. Bypass to ground with a 0.1-µF microwave chip capacitor.
CLK	5	Clock input. Conversion initiated on rising edge.
$\overline{CLK}$	6	Complement of CLK, differential input
AV_{DD}	8, 9, 14, 16, 18, 22, 26, 28, 30	5 V analog power supply
AIN	11	Analog input
$\overline{AIN}$	12	Complement of AIN, differential analog input
C1	20	Internal voltage reference. Bypass to ground with a 0.1-µF chip capacitor.
C2	24	Internal voltage reference. Bypass to ground with a 0.1-µF chip capacitor.
DNC	31	Do not connect
OVR	32	Overrange bit. A logic level high indicates the analog input exceeds full scale.
DMID	35	Output data voltage midpoint. Approximately equal to $(DV_{CC})/2$
D0 (LSB)	36	Digital output bit (least significant bit); two's complement
D1−D5, D6−D12	37−41, 44−50	Digital output bits in two's complement
D13 (MSB)	51	Digital output bit (most significant bit); two's complement
DRY	52	Data ready output

DEFINITION OF SPECIFICATIONS

Analog Bandwidth

The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

Aperture Delay

The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle

The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine wave clock results in a 50% duty cycle.

Maximum Conversion Rate

The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate

The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSB.

Integral Nonlinearity (INL)

The INL is the deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSB.

Gain Error

The gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range.

Offset Error

The offset error is the difference, given in number of LSBs, between the ADC's actual value average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into mV.

PSRR

The maximum change in offset voltage divided by the total change in supply voltage, in units of mV/V.

Temperature Drift

The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree celcius of the paramter from T_{MIN} or T_{MAX}. It is computed as the maximum variation of that parameter over the whole temperature range divided by $T_{MAX} - T_{MIN}$.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and the first five harmonics.

$$SNR = 10Log_{10}\frac{P_S}{P_N}$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10Log_{10}\frac{P_S}{P_N + P_D}$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Total Harmonic Distortion (THD)

THD is the ratio of the fundamental power (P_S) to the power of the first five harmonics (P_D).

$$THD = 10Log_{10}\frac{P_S}{P_D}$$

THD is typically given in units of dBc (dB to carrier).

Power Up Time

The difference in time from the point where the supplies are stable at ±5% of the final value, to the time the ac test is past.

Spurious-Free Dynamic Range (SFDR)

The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion

IMD3 is the ratio of the power of the fundamental (at frequiencies f_1, f_2) to the power of the worst spectral component at either frequency $2f_1 - f_2$ or $2f_2 - f_1$). IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference or dBFS (dB to full scale) when it is referred to the full-scale range.

TYPICAL CHARACTERISTICS

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = −1 dBFS, sampling rate = 80 MSPS, 3.3 Vpp sinusoidal clock, 50% duty cycle, 16k FFT points, unless otherwise noted

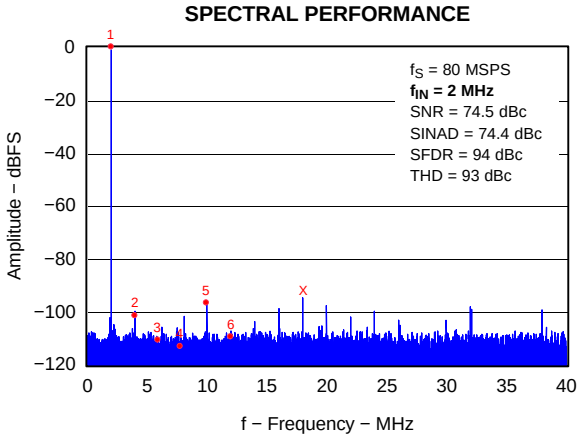


Figure 2

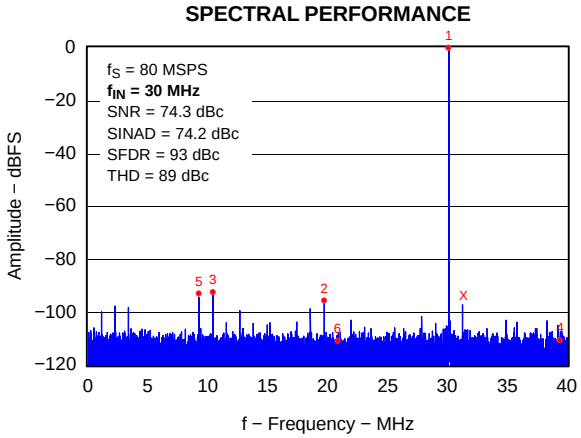


Figure 3

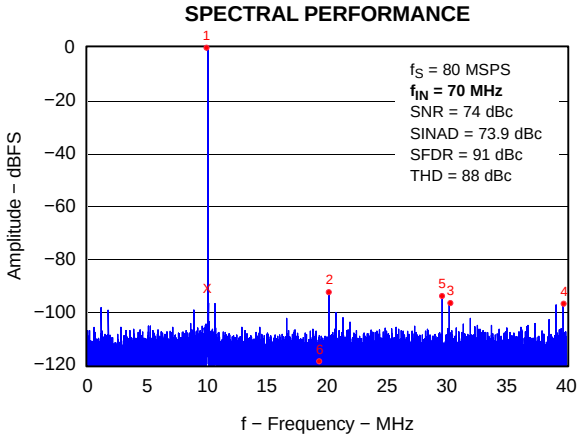


Figure 4

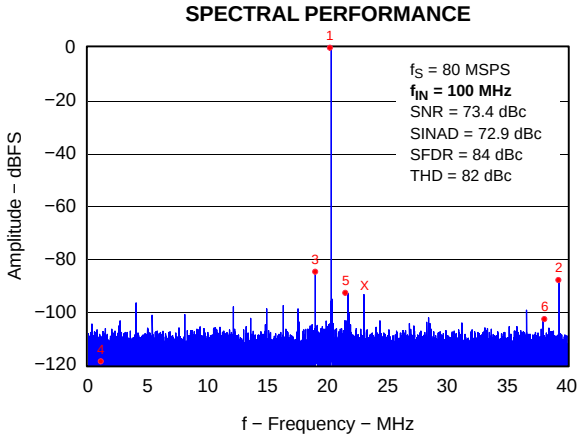


Figure 5

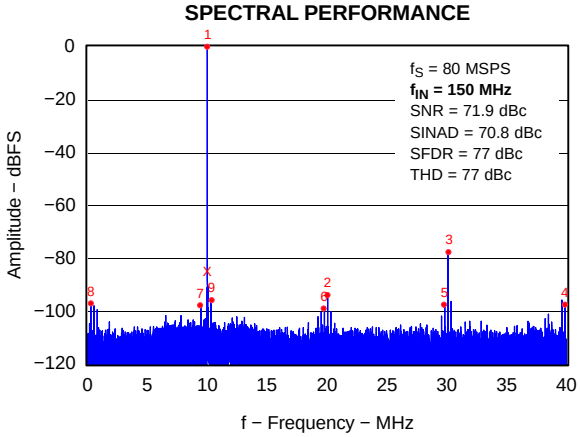


Figure 6

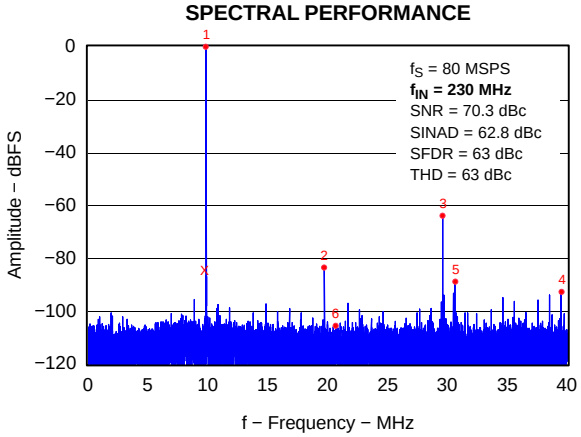


Figure 7

TYPICAL CHARACTERISTICS

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = −1 dBFS, sampling rate = 80 MSPS, 3.3 Vpp sinusoidal clock, 50% duty cycle, 16k FFT points, unless otherwise noted

SPECTRAL PERFORMANCE

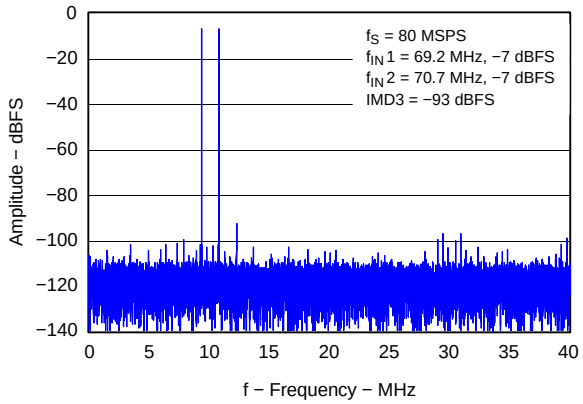


Figure 8

SPECTRAL PERFORMANCE

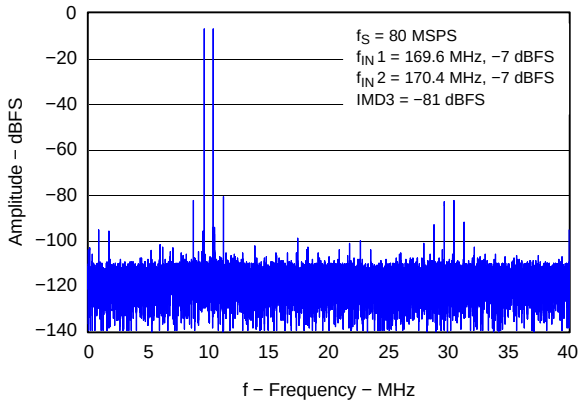


Figure 9

WCDMA CARRIER

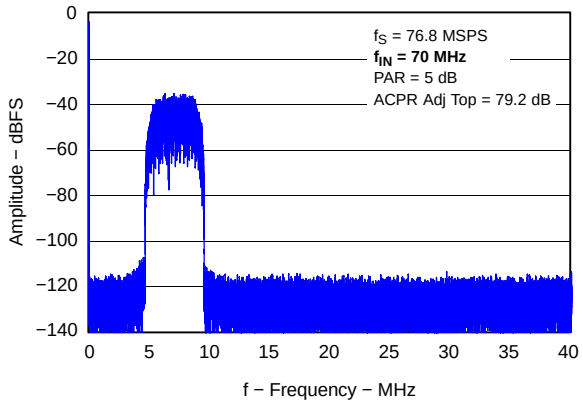


Figure 10

WCDMA CARRIER

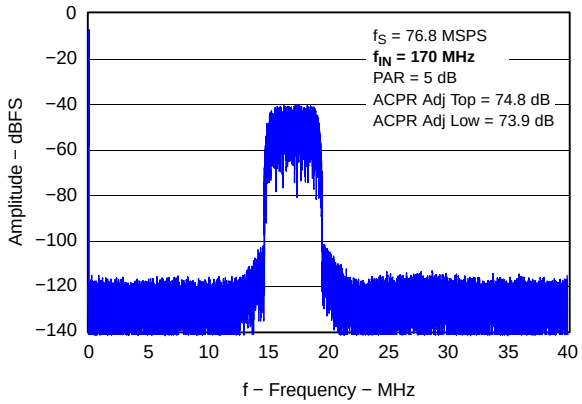


Figure 11

AC PERFORMANCE vs INPUT AMPLITUDE

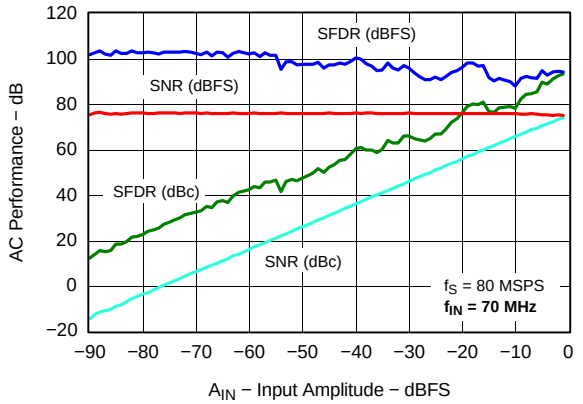


Figure 12

AC PERFORMANCE vs INPUT AMPLITUDE

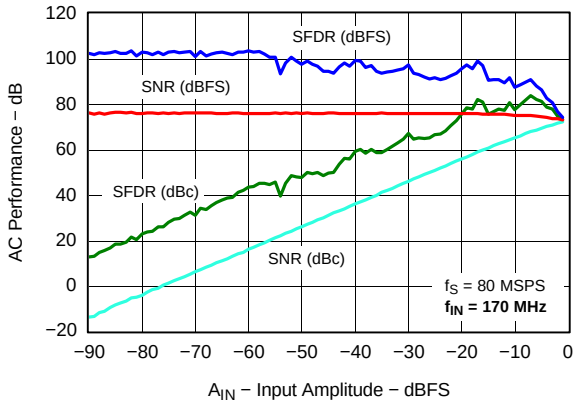


Figure 13

TYPICAL CHARACTERISTICS

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = −1 dBFS, sampling rate = 80 MSPS, 3.3 Vpp sinusoidal clock, 50% duty cycle, 16k FFT points, unless otherwise noted

TWO-TONE SPURIOUS-FREE DYNAMIC RANGE vs INPUT AMPLITUDE

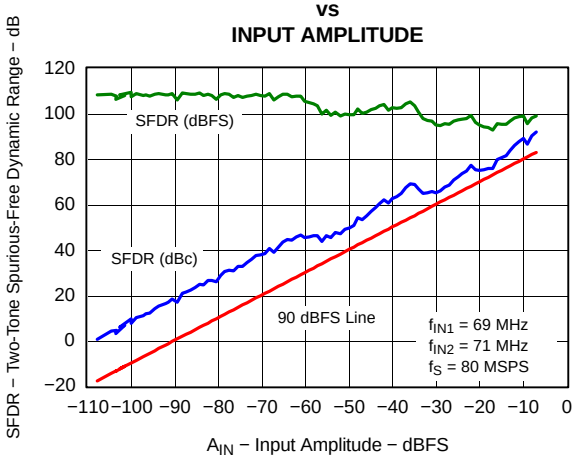


Figure 14

NOISE HISTOGRAM WITH INPUTS SHORTED

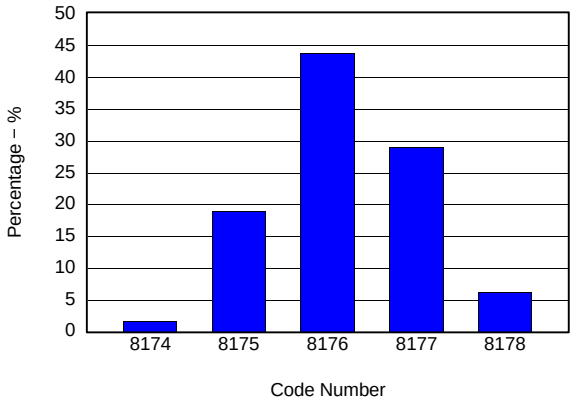


Figure 15

SPURIOUS-FREE DYNAMIC RANGE vs DUTY CYCLE

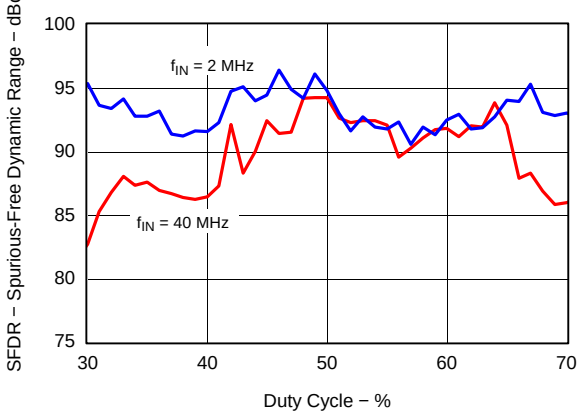


Figure 16

AC PERFORMANCE vs CLOCK LEVEL

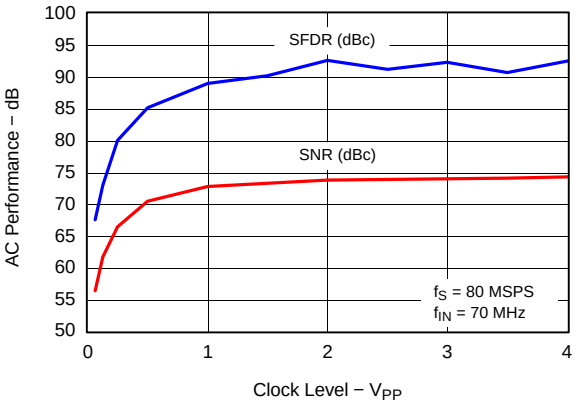


Figure 17

AC PERFORMANCE vs CLOCK LEVEL

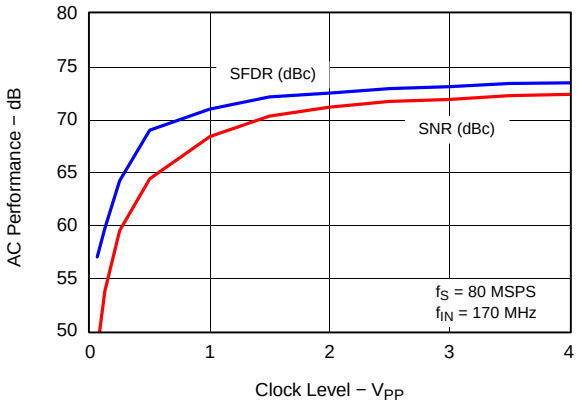


Figure 18

AC PERFORMANCE vs CLOCK COMMON MODE

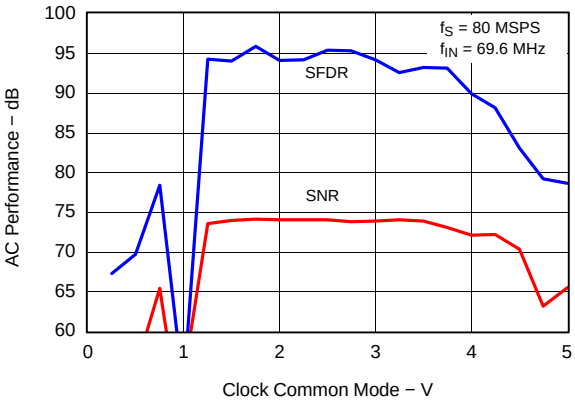


Figure 19

TYPICAL CHARACTERISTICS

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = −1 dBFS, sampling rate = 80 MSPS, 3.3 Vpp sinusoidal clock, 50% duty cycle, 16k FFT points, unless otherwise noted

SPURIOUS-FREE DYNAMIC RANGE vs SUPPLY VOLTAGE

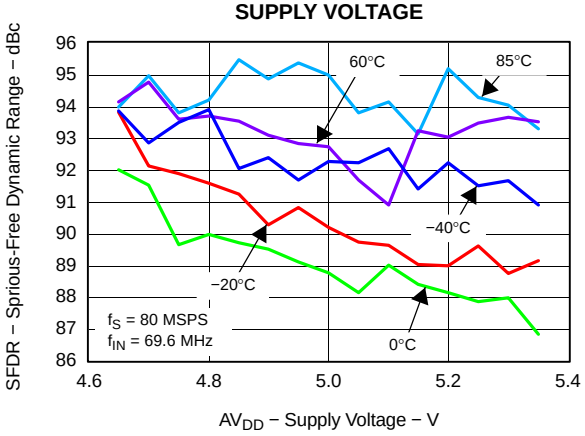


Figure 20

SIGNAL-TO−NOISE RATIO vs SUPPLY VOLTAGE

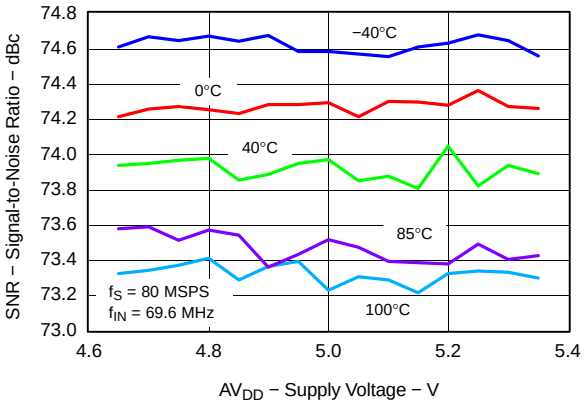


Figure 21

SPURIOUS-FREE DYNAMIC RANGE vs SUPPLY VOLTAGE

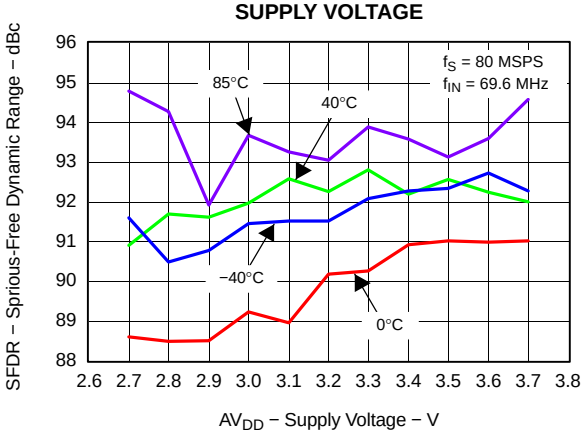


Figure 22

SIGNAL-TO-NOISE RATIO vs SUPPLY VOLTAGE

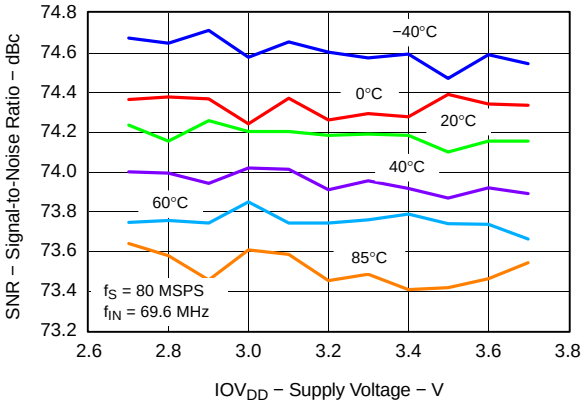


Figure 23

DIFFERENTIAL NONLINEARITY

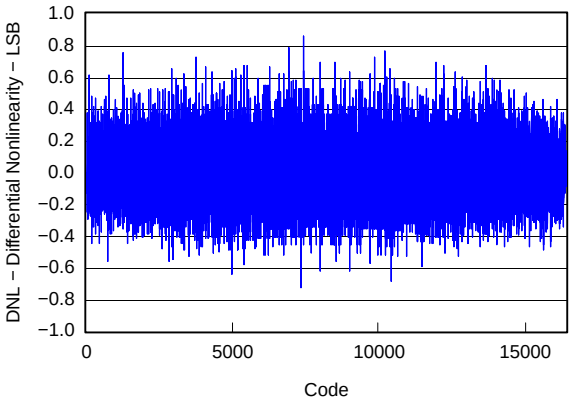


Figure 24

INTEGRAL NONLINEARITY

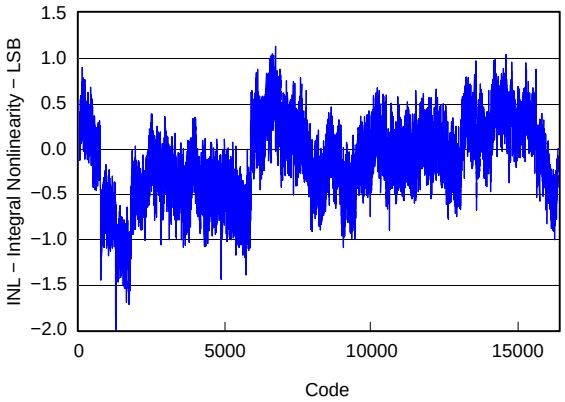


Figure 25

TYPICAL CHARACTERISTICS

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = −1 dBFS, sampling rate = 80 MSPS, 3.3 Vpp sinusoidal clock, 50% duty cycle, 16k FFT points, unless otherwise noted

INPUT BANDWIDTH

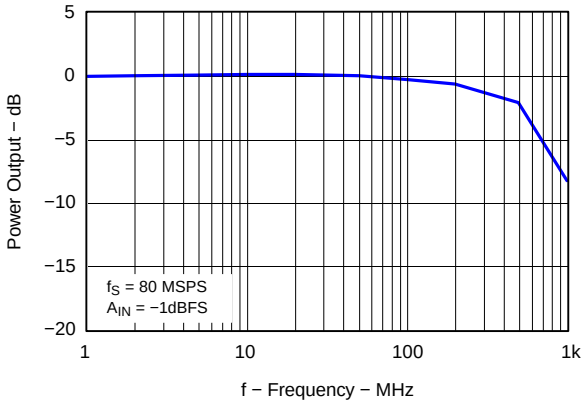


Figure 26

TOTAL POWER vs SAMPLING FREQUENCY

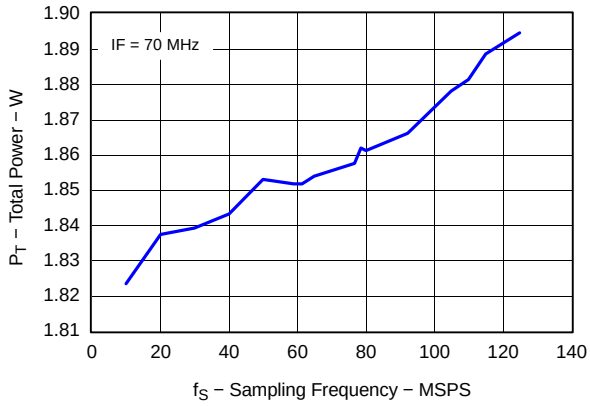


Figure 27

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = −1 dBFS, sampling rate = 80 MSPS, 3.3 Vpp sinusoidal clock, 50% duty cycle, 16k FFT points, unless otherwise noted

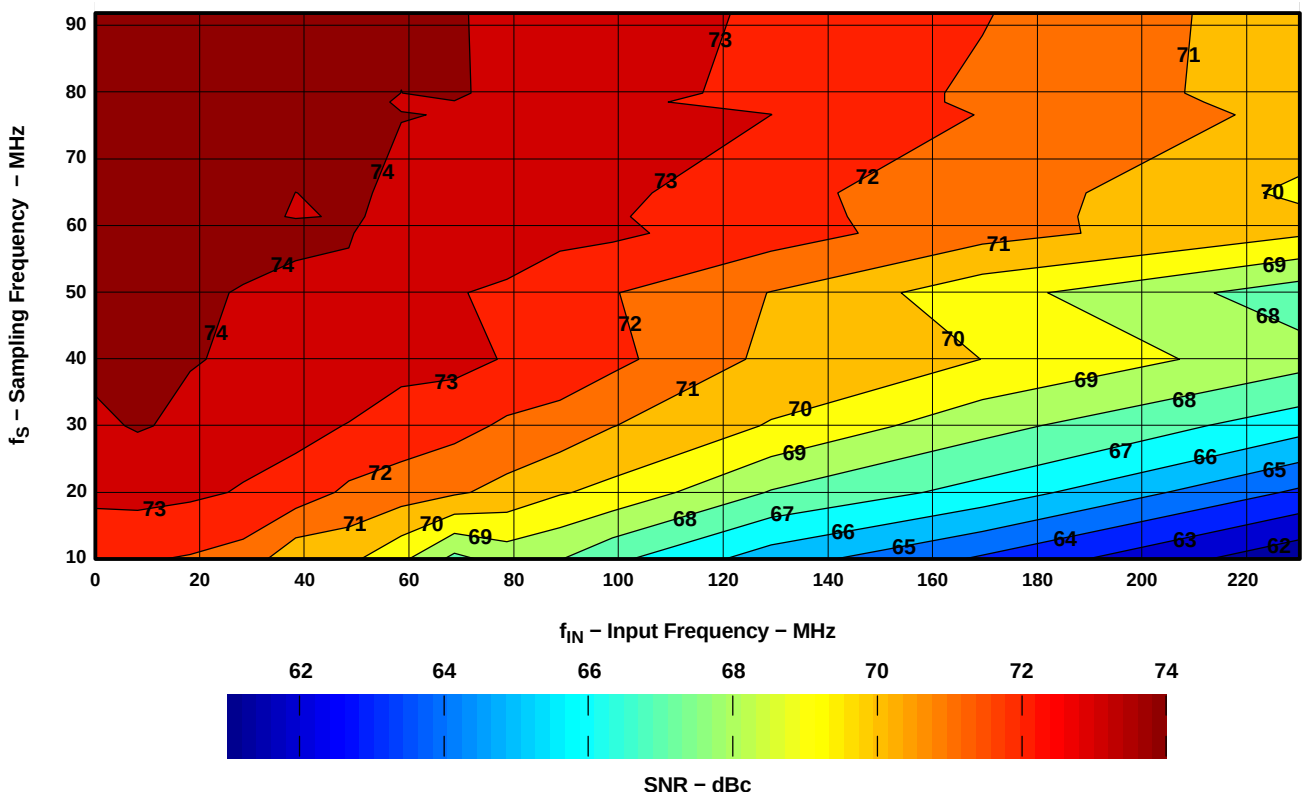


Figure 28.

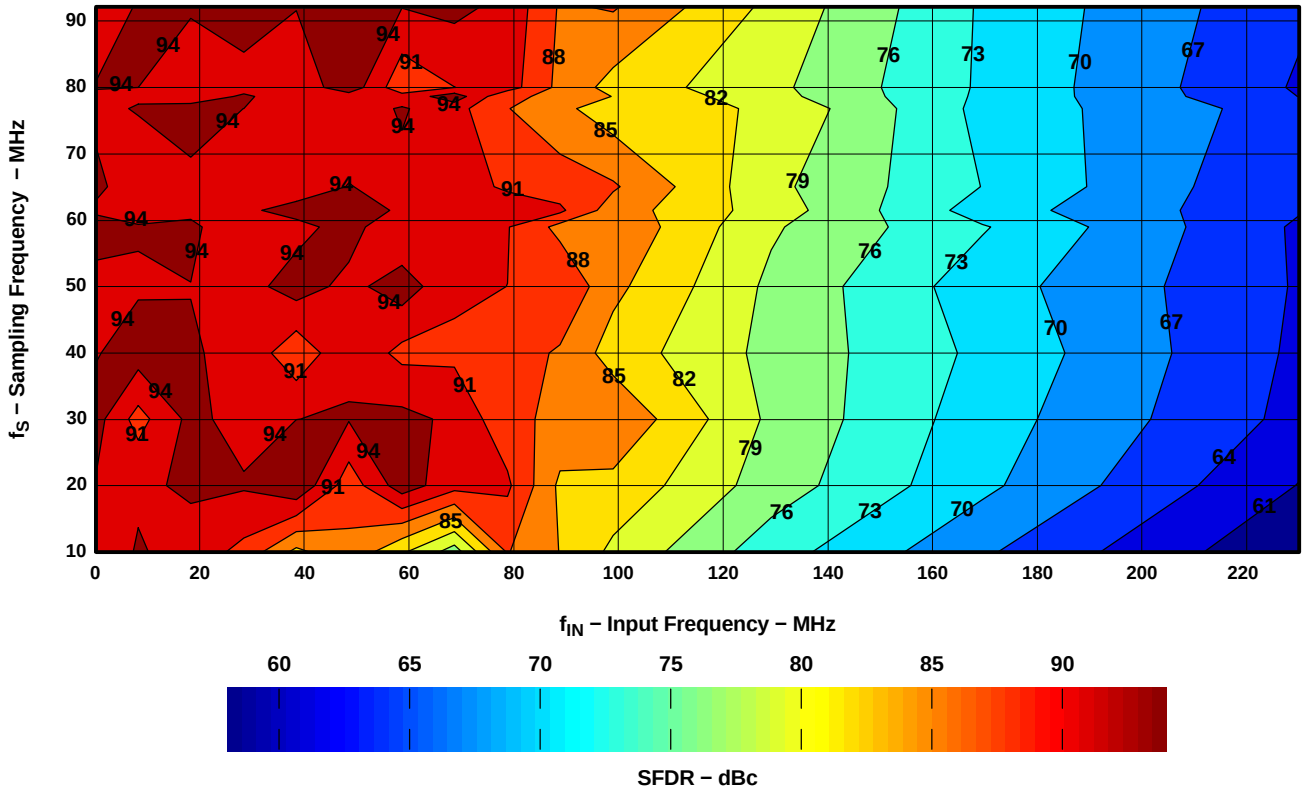


Figure 29.

EQUIVALENT CIRCUITS

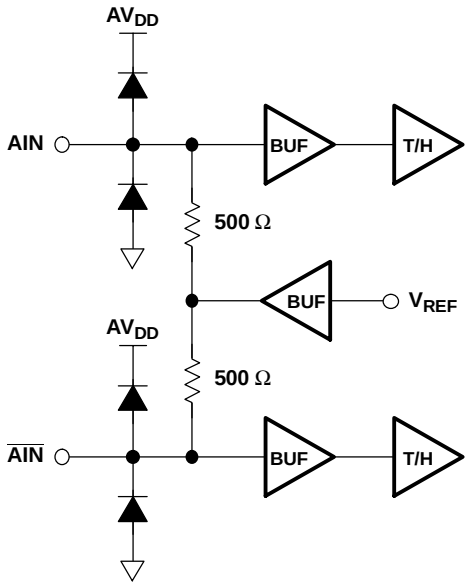


Figure 30. Analog Input

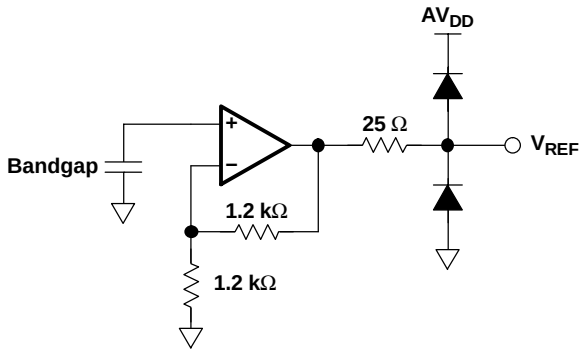


Figure 33. Reference

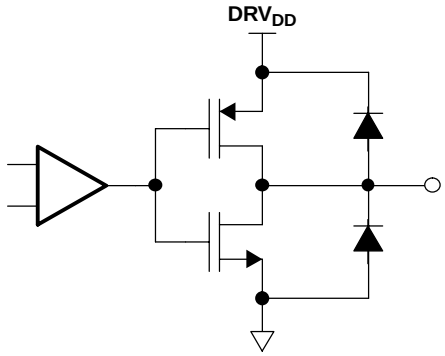


Figure 31. Digital Output

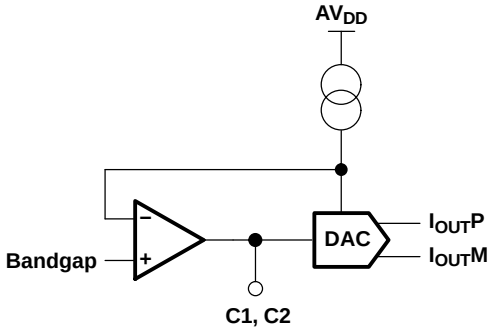


Figure 34. Decoupling Pin

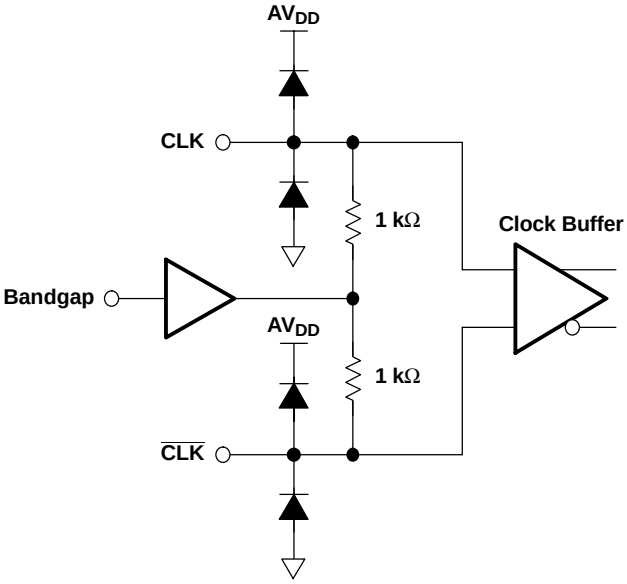


Figure 32. Clock Input

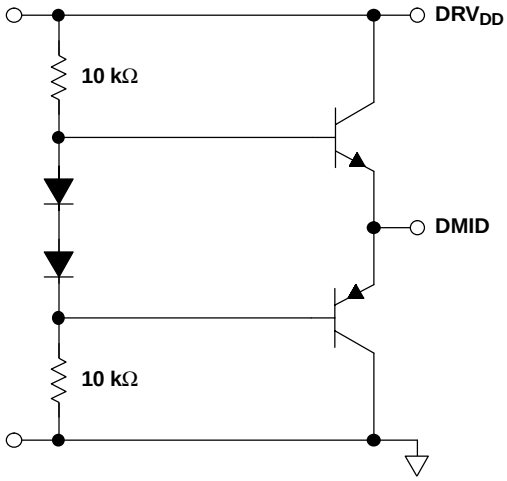


Figure 35. DMID Generation

APPLICATION INFORMATION

THEORY OF OPERATION

The ADS5423 is a 14 bit, 80 MSPS, monolithic pipeline analog to digital converter. Its bipolar analog core operates from a 5 V supply, while the output uses 3.3 V supply for compatibility with the CMOS family. The conversion process is initiated by the rising edge of the external input clock. At that instant, the differential input signal is captured by the input track and hold (T&H) and the input sample is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. Both the rising and the falling clock edges are used to propagate the sample through the pipeline every half clock cycle. This process results in a data latency of three clock cycles, after which the output data is available as a 14 bit parallel word, coded in binary two's complement format.

INPUT CONFIGURATION

The analog input for the ADS5423 (see Figure 30) consists of an analog differential buffer followed by a bipolar track-and-hold. The analog buffer isolates the source driving the input of the ADC from any internal switching. The input common mode is set internally through a 500 Ω resistor connected from 2.4 V to each of the inputs. This results in a differential input impedance of 1 kΩ.

For a full-scale differential input, each of the differential lines of the input signal (pins 11 and 12) swings symmetrically between 2.4 +0.55 V and 2.4 –0.55 V. This means that each input is driven with a signal of up to 2.4 ±0.55 V, so that each input has a maximum signal swing of 1.1 V_{PP} for a total differential input signal swing of 2.2 V_{PP}. The maximum swing is determined by the internal reference voltage generator eliminating any external circuitry for this purpose.

The ADS5423 obtains optimum performance when the analog inputs are driven differentially. The circuit in Figure 36 shows one possible configuration using an RF transformer with termination either on the primary or on the secondary of the transformer. If voltage gain is required a step up transformer can be used. For higher gains that would require impractical higher turn ratios on the transformer, a single-ended amplifier driving the transformer can be used (see Figure 37). Another circuit optimized for performance would be the one on Figure 38, using the THS4304 or the OPA695. Texas Instruments has shown excellent performance on this configuration up to 10 dB gain with the THS4304 and at 14 dB gain with the OPA695. For the best performance, they need to be configured differentially after the transformer (as shown) or in inverting mode for the OPA695 (see SBAA113); otherwise, HD2 from the op amps limits the useful frequency.

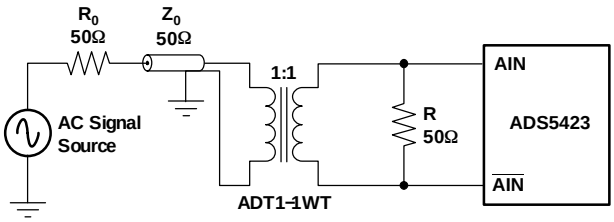


Figure 36. Converting a Single-Ended Input to a Differential Signal Using RF Transformers

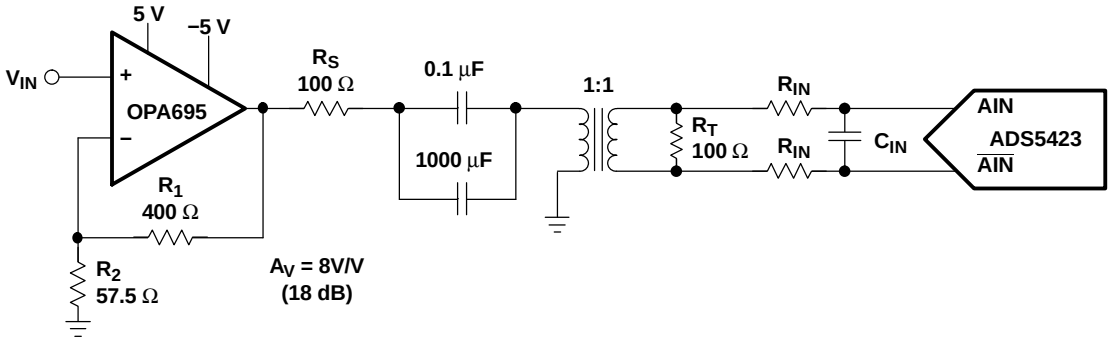


Figure 37. Using the OPA695 With the ADS5423

APPLICATION INFORMATION

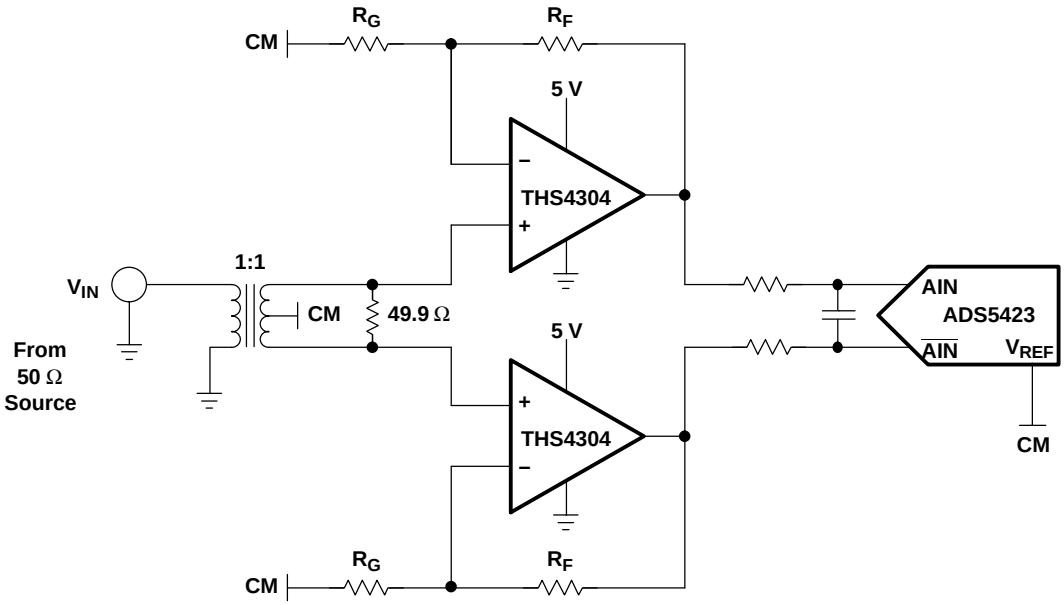


Figure 38. Using the THS4304 With the ADS5423

Besides these, Texas Instruments offers a wide selection of single-ended operational amplifiers (including the THS3201, THS3202, and OPA847) that can be selected depending on the application. An RF gain block amplifier, such as Texas Instrument's THS9001, can also be used with an RF transformer for high input frequency applications. For applications requiring dc-coupling with the signal source, instead of using a topology with three single ended amplifiers, a differential input/differential output amplifier like the THS4509 (see Figure 39) can be used, which minimizes board space and reduce number of components.

Figure 41 shows their combined SNR and SFDR performance versus frequency with −1 dBFS input signal level and sampling at 80 MSPS.

On this configuration, the THS4509 amplifier circuit provides 10 dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5423.

The 225 Ω resistors and 2.7 pF capacitor between the THS4509 outputs and ADS5423 inputs (along with the input capacitance of the ADC) limit the bandwidth of the signal to about 100 MHz (−3 dB).

For this test, an Agilent signal generator is used for the signal source. The generator is an ac-coupled 50 Ω source. A band-pass filter is inserted in series with the input to reduce harmonics and noise from the signal source.

APPLICATION INFORMATION

Input termination is accomplished via the 69.8 Ω resistor and 0.22 µF capacitor to ground in conjunction with the input impedance of the amplifier circuit. A 0.22 µF capacitor and 49.9 Ω resistor is inserted to ground across the 69.8 Ω resistor and 0.22 µF capacitor on the alternate input to balance the circuit.

Gain is a function of the source impedance, termination, and 348 Ω feedback resistor. See the THS4509 data sheet for further component values to set proper 50 Ω termination for other common gains.

Since the ADS5423 recommended input common-mode voltage is +2.4 V, the THS4509 is operated from a single power supply input with V_{S+} = +5 V and V_{S-} = 0 V (ground). This maintains maximum headroom on the internal transistors of the THS4509.

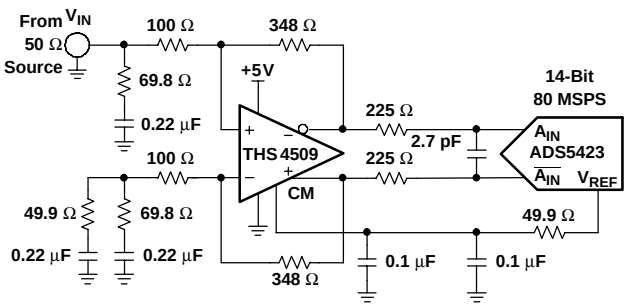


Figure 39. Using the THS4509 With the ADS5423

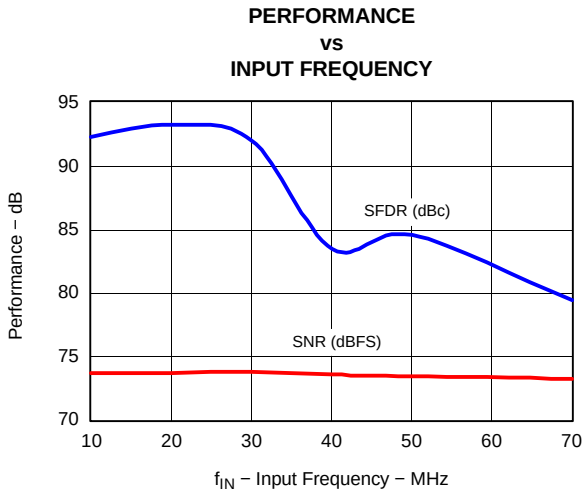


Figure 40. Performance vs Input Frequency for the THS4509 + ADS5423 Configuration

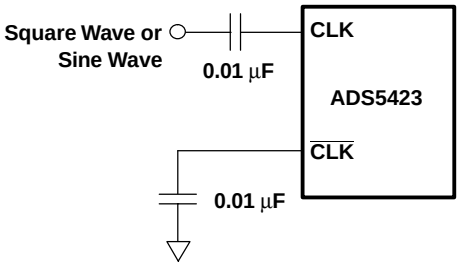


Figure 41. Single-Ended Clock

CLOCK INPUTS

The ADS5423 clock input can be driven with either a differential clock signal or a single-ended clock input, with little or no difference in performance between both configurations. In low input frequency applications, where jitter may not be a big concern, the use of single ended clock (see Figure 41) could save some cost and board space without any trade-off in performance. When driven on this configuration, it is best to connect CLKM (pin 11) to ground with a 0.01 µF capacitor, while CLKP is ac-coupled with a 0.01 µF capacitor to the clock source, as shown in Figure 38.

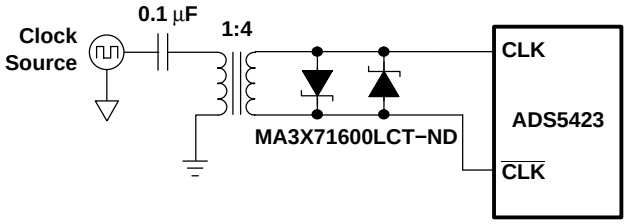


Figure 42. Differential Clock

Nevertheless, for jitter sensitive applications, the use of a differential clock will have some advantages (as with any other ADCs) at the system level. The first advantage is that it allows for common-mode noise rejection at the PCB level. A further analysis (see Clocking High Speed Data Converters, SLYT075) reveals one more advantage. The following formula describes the different contributions to clock jitter:

$$(\text{Jittertotal})^2 = (\text{EXT_jitter})^2 + (\text{ADC_jitter})^2 = (\text{EXT_jitter})^2 + (\text{ADC_int})^2 + (\text{K/clock_slope})^2$$

APPLICATION INFORMATION

The first term would represent the external jitter, coming from the clock source, plus noise added by the system on the clock distribution, up to the ADC. The second term is the ADC contribution, which can be divided in two portions. The first does not depend directly on any external factor. That is the best we can get out of our ADC. The second contribution is a term inversely proportional to the clock slope. The faster the slope, the smaller this term will be. As an example, we could compute the ADC jitter contribution from a sinusoidal input clock of 3 Vpp amplitude and Fs = 80 MSPS:

ADC_jitter = sqrt $((150fs)^2 + (5 \times 10^{-5}/(1.5 \times 2 \times PI \times 80 \times 10^6))^2) = 164fs$

The use of differential clock allows for the use of bigger clock amplitudes without exceeding the absolute maximum ratings. This, on the case of sinusoidal clock, results on higher slew rates which minimizes the impact of the jitter factor inversely proportional to the clock slope.

Figure 42 shows this approach. The back-to-back Schottky can be added to limit the clock amplitude in cases where this would exceed the absolute maximum ratings, even when using a differential clock. Figure 17 and Figure 18 show the performance versus input clock amplitude for a sinusoidal clock.

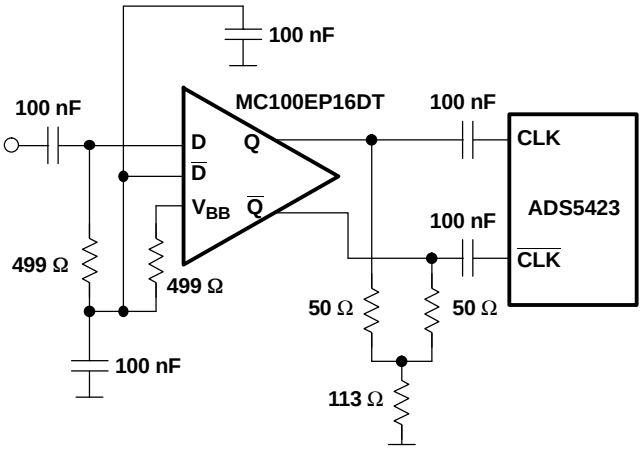


Figure 43. Differential Clock Using PECL Logic

Another possibility is the use of a logic based clock, as PECL. In this case, the slew rate of the edges will most likely be much higher than the one obtained for the same clock amplitude based on a sinusoidal clock. This solution would minimize the effect of the slope dependent ADC jitter. Nevertheless, observe that for the ADS5423, this term is small and has been optimized. Using logic gates to square a sinusoidal clock may not produce the best results as logic gates may not have been optimized to act as comparators, adding too much jitter while squaring the inputs.

The common-mode voltage of the clock inputs is set internally to 2.4 V using internal 1 kΩ resistors. It is recommended using an ac coupling, but if for any reason, this scheme is not possible, due to, for instance, asynchronous clocking, the ADS5423 presents a good tolerance to clock common-mode variation (see Figure 19).

Additionally, the internal ADC core uses both edges of the clock for the conversion process. This means that, ideally, a 50% duty cycle should be provided. Figure 16 shows the performance variation of the ADC versus clock duty cycle.

DIGITAL OUTPUTS

The ADC provides 14 data outputs (D13 to D0, with D13 being the MSB and D0 the LSB), a data-ready signal (DRY, pin 52), and an out-of-range indicator (OVR, pin 32) that equals 1 when the output reaches the full-scale limits.

The output format is two's complement. When the input voltage is at negative full scale (around −1.1 V differential), the output will be, from MSB to LSB, 10 0000 0000 0000. Then, as the input voltage is increased, the output switches to 10 0000 0000 0001, 10 0000 0000 0010 and so on until 11 1111 1111 1111 right before mid-scale (when both inputs are tight together if we neglect offset errors). Further increase on input voltages, outputs the word 00 0000 0000 0000, to be followed by 00 0000 0000 0001, 00 0000 0000 0010 and so on until reaching 01 1111 1111 1111 at full-scale input (1.1 V differential).

APPLICATION INFORMATION

Although the output circuitry of the ADS5423 has been designed to minimize the noise produced by the transients of the data switching, care must be taken when designing the circuitry reading the ADS5423 outputs. Output load capacitance should be minimized by minimizing the load on the output traces, reducing their length and the number of gates connected to them, and by the use of a series resistor with each pin. Typical numbers on the data sheet tables and graphs are obtained with 100 Ω series resistor on each digital output pin, followed by a 74AVC16244 digital buffer as the one used in the evaluation board.

POWER SUPPLIES

The use of low noise power supplies with adequate decoupling is recommended, being the linear supplies the first choice vs switched ones, which tend to generate more noise components that can be coupled to the ADS5423.

The ADS5423 uses two power supplies. For the analog portion of the design, a 5 V AV_{DD} is used, while for the digital outputs supply (DRV_{DD}), we recommend the use of 3.3 V. All the ground pins are marked as GND, although AGND pins and DRGND pins are not tied together inside the package. Customers willing to experiment with different grounding schemes should know that AGND pins are 4, 7, 10, 13, 15, 17, 19, 21, 23, 25, 27, and 29, while DRGND pins are 2, 34, and 42. Nevertheless, we recommend that both grounds are tied together externally, using a common ground plane. That is the case on the production test boards and modules provided to customer for evaluation. In order to obtain the best performance, the user should layout the board to assure that the digital return currents do not flow under the analog portion of the board. This can be achieved without the need to split the board and just with careful component placing and increasing the number of vias and ground planes.

Finally, notice that the metallic heat sink under the package is also connected to analog ground.

LAYOUT INFORMATION

The evaluation board represents a good guideline of how to layout the board to obtain the maximum performance out of the ADS5423. General design rules as the use of multilayer boards, single ground plane for both, analog and digital ADC ground connections and local decoupling ceramic chip capacitors should be applied. The input traces should be isolated from any external source of interference or noise, including the digital outputs as well as the clock traces. The clock should also be isolated from other signals, especially on applications where low jitter is required, as high IF sampling.

Besides performance oriented rules, special care has to be taken when considering the heat dissipation out of the device. The thermal heat sink (octagonal, with 2,5 mm on each side) should be soldered to the board, and provision for more than 16 ground vias should be made. The thermal package information describes the T_{JA} values obtained on the different configurations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS5423IPGP	Active	Production	HTQFP (PGP) | 52	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS5423IPGP
ADS5423IPGP.B	Active	Production	HTQFP (PGP) | 52	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS5423IPGP
ADS5423IPGPR	Active	Production	HTQFP (PGP) | 52	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS5423IPGP
ADS5423IPGPR.B	Active	Production	HTQFP (PGP) | 52	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS5423IPGP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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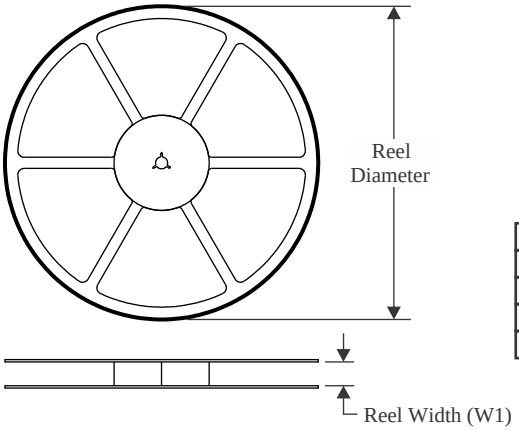
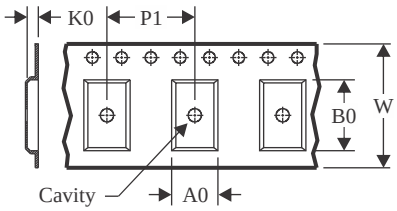
TAPE AND REEL INFORMATION

REEL DIMENSIONS

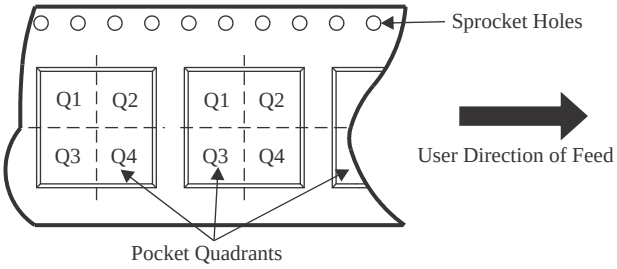


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

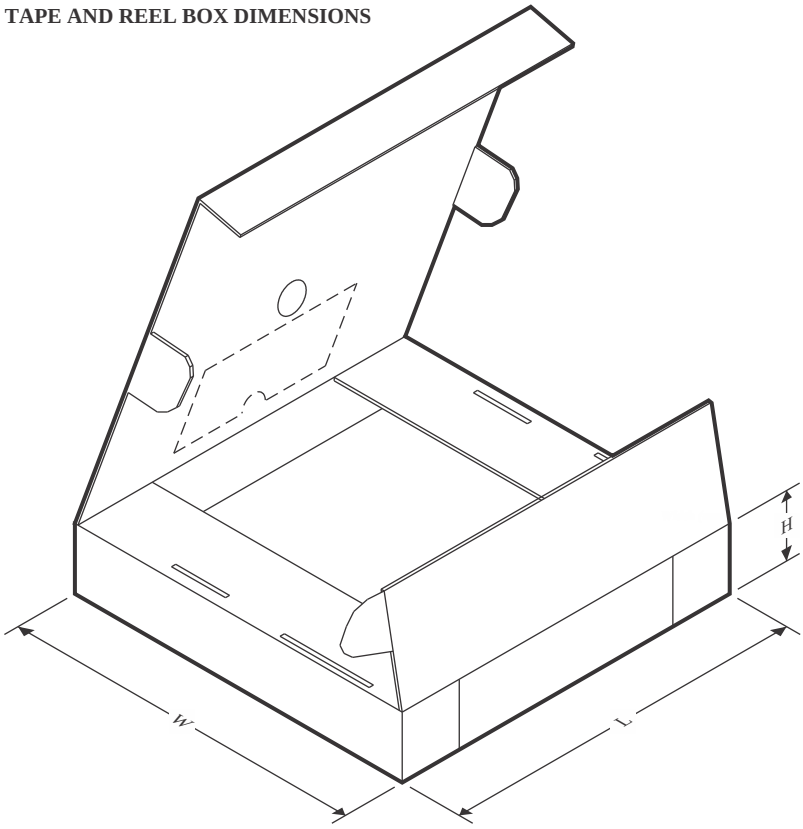
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS5423IPGPR	HTQFP	PGP	52	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

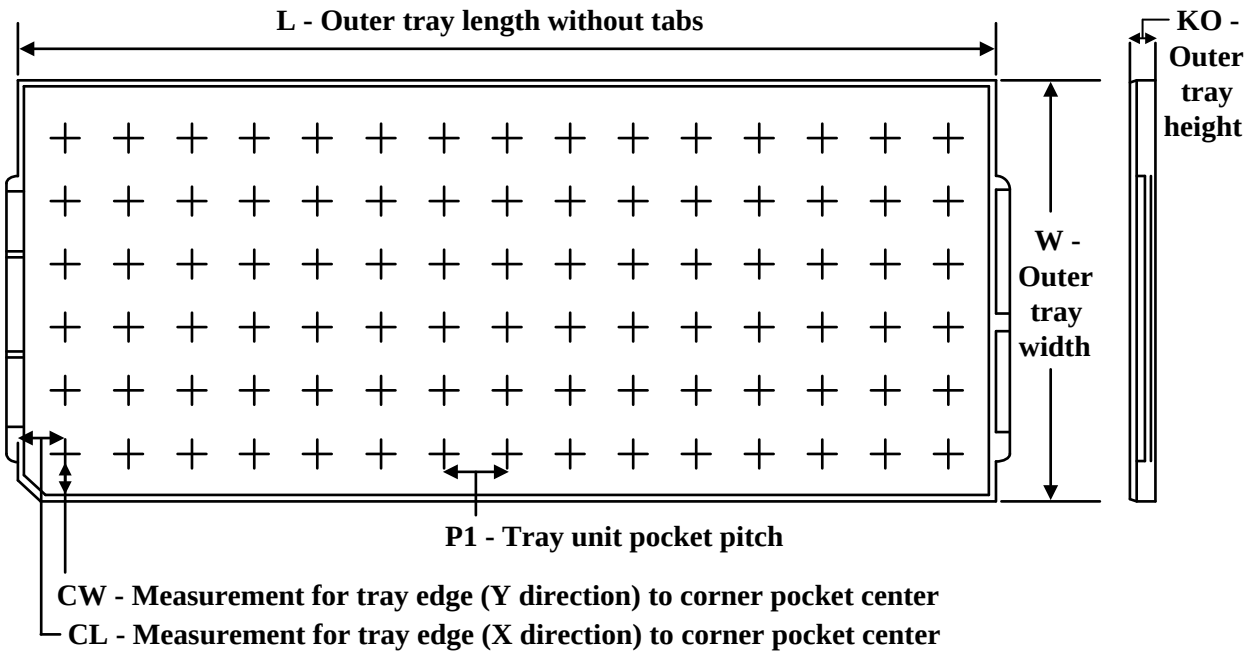
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS5423IPGPR	HTQFP	PGP	52	1000	350.0	350.0	43.0

TRAY

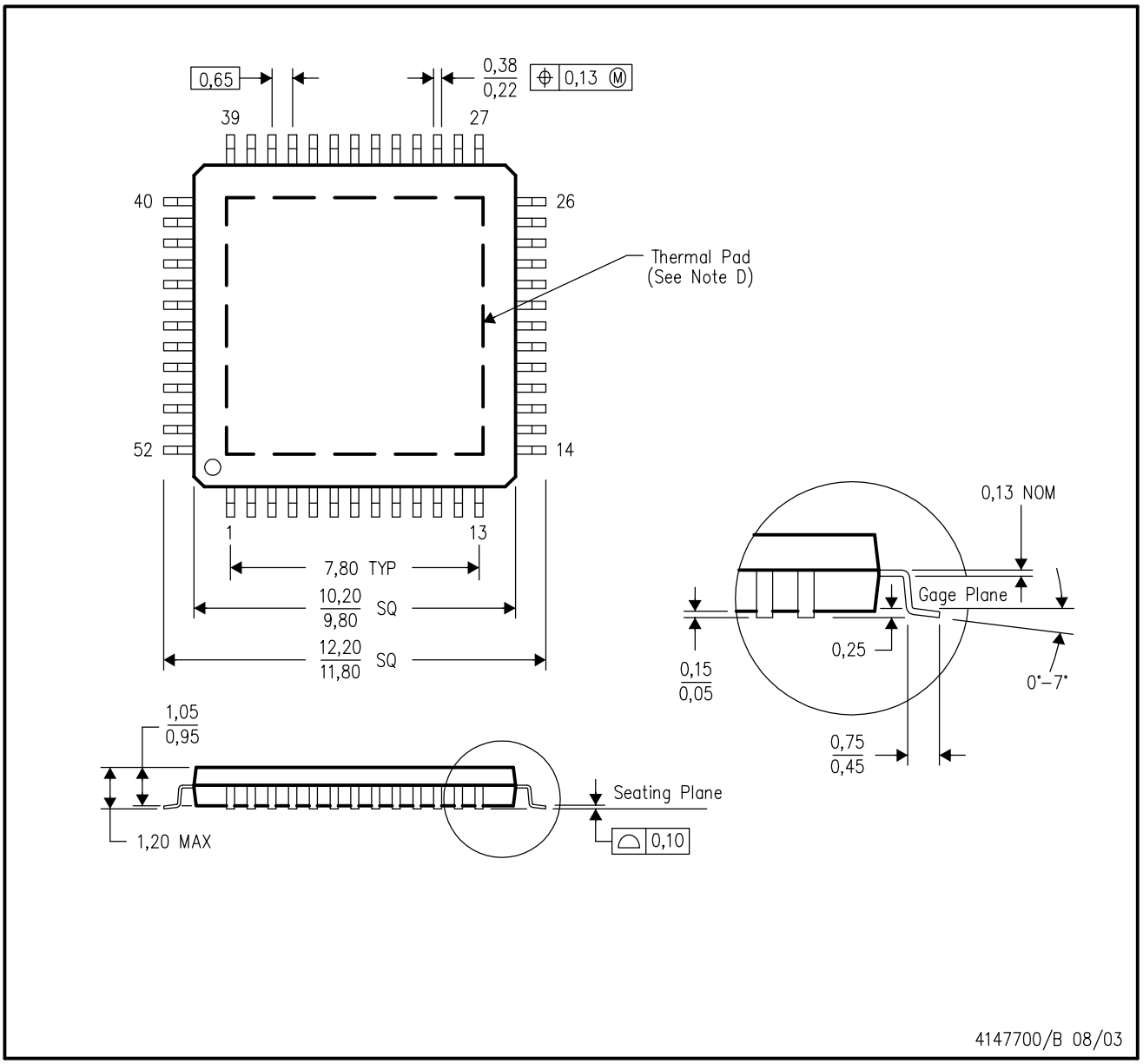


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADS5423IPGP	PGP	HTQFP	52	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
ADS5423IPGP.B	PGP	HTQFP	52	160	8 x 20	150	315	135.9	7620	15.2	13.1	13

PGP (S–PQFP–G52) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

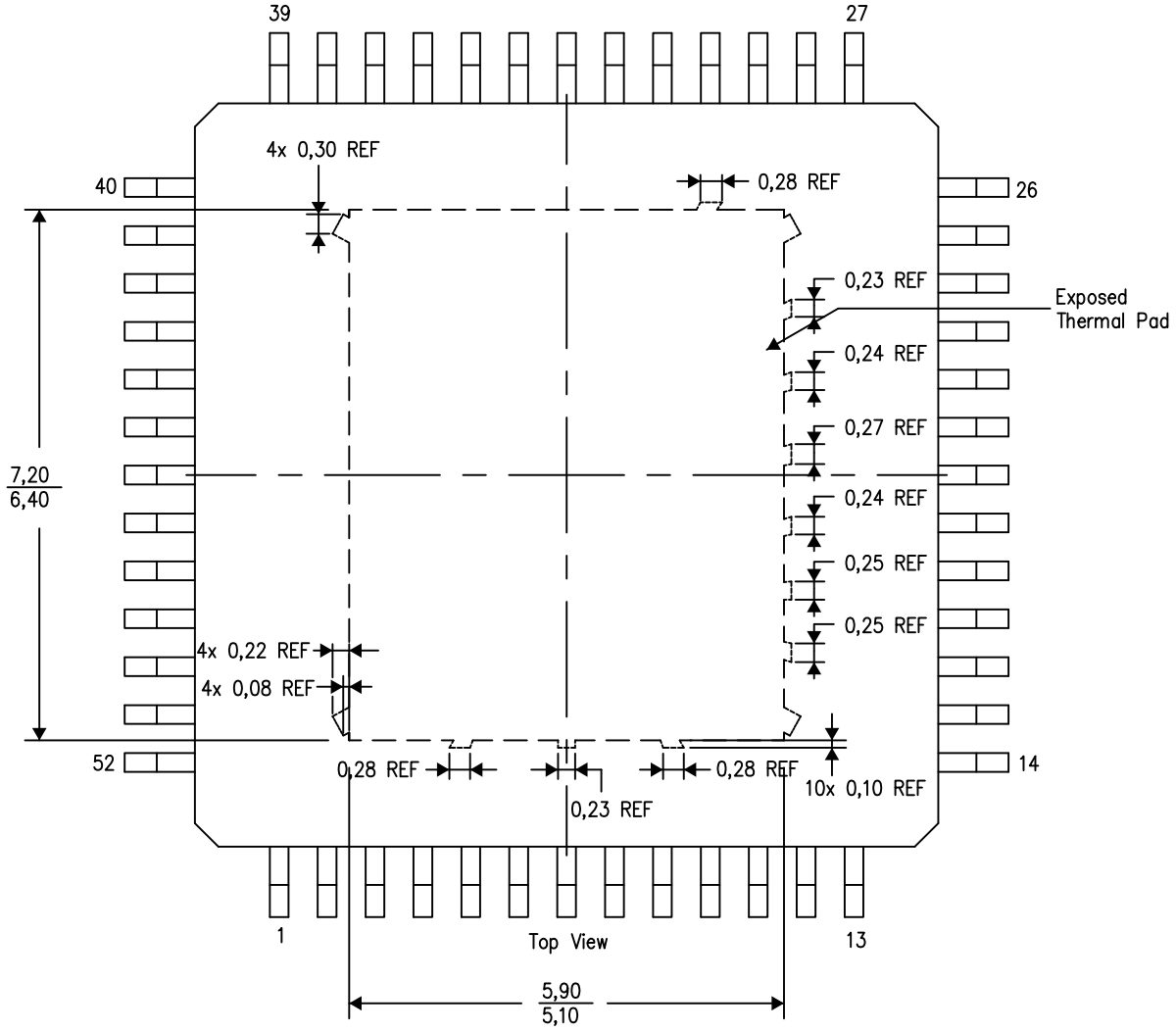
PGP (S-PQFP-G52) PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4210154-4/B 11/13

NOTE: All linear dimensions are in millimeters

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