ADS7886 12-Bit, 1-MSPS, Micro-Power, Miniature SAR Analog-to-Digital Converters

1 Features

- 1-MHz Sample Rate Serial Device
- 12-Bit Resolution
- Zero Latency
- 20-MHz Serial Interface
- Supply Range: 2.35 V to 5.25 V
- Typical Power Dissipation at 1 MSPS:
  - 3.9 mW at 3-V V_{DD}
  - 7.5 mW at 5-V V_{DD}
- INL ±1.25 LSB Maximum, ±0.65 LSB (Typical)
- DNL ±1 LSB Maximum, +0.4 / –0.65 LSB (Typical)
- Typical AC Performance: 72.25-dB SINAD, –84-dB THD
- Unipolar Input Range: 0 V to V_{DD}
- Power Down Current: 1 µA
- Wide Input Bandwidth: 15 MHz at 3 dB
- 6-Pin SOT-23 and SC70 Packages

2 Applications

- Base Band Converters in Radio Communication
- Motor Current and Bus Voltage Sensors in Digital Drives
- Optical Networking (DWDM, MEMS Based Switching)
- Optical Sensors
- Battery-Powered Systems
- Medical Instrumentations
- High-Speed Data Acquisition Systems
- High-Speed Closed-Loop Systems

3 Description

The ADS7886 is a 12-bit, 1-MSPS analog-to-digital converter (ADC). The device includes a capacitor based SAR A/D converter with inherent sample and hold. The serial interface in each device is controlled by the $\overline{CS}$ and SCLK signals for glueless connections with microprocessors and DSPs. The input signal is sampled with the falling edge of $\overline{CS}$, and SCLK is used for conversion and serial data output.

The device operates from a wide supply range from 2.35 V to 5.25 V. The low power consumption of the device makes it suitable for battery-powered applications. The device also includes a power down feature for power saving at lower conversion speeds.

The high level of the digital input to the device is not limited to device V_{DD}. This means the digital input can go as high as 5.25 V when device supply is 2.35 V. This feature is useful when digital signals are coming from other circuit with different supply levels. Also this relaxes restriction on power-up sequencing.

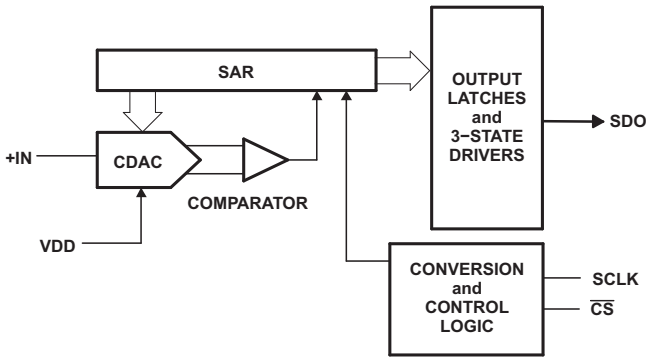
The ADS7886 is available in 6-pin SOT-23 and SC70 packages and is specified for operation from –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS7886	SOT-23 (6)	2.90 mm × 1.60 mm
	SC70 (6)	2.00 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Device Comparison Table ... 3
6 Pin Configuration and Functions ... 3
7 Specifications ... 4
7.1 Absolute Maximum Ratings ... 4
7.2 ESD Ratings ... 4
7.3 Recommended Operating Conditions ... 4
7.4 Thermal Information ... 4
7.5 Electrical Characteristics ... 5
7.6 Timing Requirements ... 7
7.7 Typical Characteristics ... 9
8 Detailed Description ... 14
8.1 Overview ... 14
8.2 Functional Block Diagram ... 14
8.3 Feature Description ... 14
8.4 Device Functional Modes ... 15
9 Application and Implementation ... 16
9.1 Application Information ... 16
9.2 Typical Application ... 16
10 Power Supply Recommendations ... 18
11 Layout ... 18
11.1 Layout Guidelines ... 18
11.2 Layout Example ... 19
12 Device and Documentation Support ... 20
12.1 Documentation Support ... 20
12.2 Receiving Notification of Documentation Updates 20
12.3 Community Resource ... 20
12.4 Trademarks ... 20
12.5 Electrostatic Discharge Caution ... 20
12.6 Glossary ... 20
13 Mechanical, Packaging, and Orderable Information ... 20

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2009) to Revision B **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Package/Ordering Information* table, see POA at the end of the datasheet. ... 1
- Changed $R_{\theta JA}$ values from: 295.2 °C/W to: 113.4 °C/W for DBV package ... 4
- Changed $R_{\theta JA}$ values from: 351.3 °C/W to: 149.6 °C/W for DCK package ... 4

Changes from Original (September 2005) to Revision A **Page**

- Added V_{IH} information ... 5
- Changed V_{IH} information ... 5

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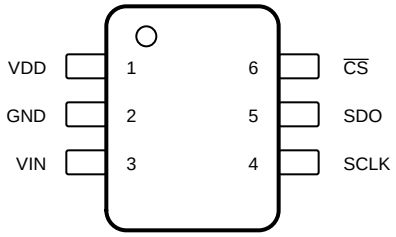
5 Device Comparison Table

Table 1. Micro-Power Miniature SAR Converter Family

BIT	< 300 KSPS	300 KSPS – 1.25 MSPS
12-Bit	ADS7866 (1.2 V_{DD} to 3.6 V_{DD})	ADS7886 (2.35 V_{DD} to 5.25 V_{DD})
10-Bit	ADS7867 (1.2 V_{DD} to 3.6 V_{DD})	ADS7887 (2.35 V_{DD} to 5.25 V_{DD})
8-Bit	ADS7868 (1.2 V_{DD} to 3.6 V_{DD})	ADS7888 (2.35 V_{DD} to 5.25 V_{DD})

6 Pin Configuration and Functions

DBV and DCK Packages
6-Pin SOT-23 and SC70
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{DD}	—	Power supply input also acts like a reference voltage to ADC.
2	GND	—	Ground for power supply, all analog and digital signals are referred with respect to this pin.
3	VIN	I	Analog signal input
4	SCLK	I	Serial clock
5	SDO	O	Serial data out
6	$\overline{CS}$	I	Chip select signal, active low

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
+IN to AGND		–0.3	V_{DD} +0.3	V
$+V_{DD}$ to AGND		–0.3	7	V
Digital input voltage to GND		–0.3	7	V
Digital output to GND		–0.3	(V_{DD} + 0.3)	V
Power dissipation, SOT-23 and SC70 packages			(T_J Max–T_A)/$R_{\theta JA}$	
Lead temperature, soldering	Vapor phase (60 s)		215	°C
	Infrared (15 s)		220	
Junction temperature (T_J Max)			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T_A	Operating temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		ADS7886		UNIT
		DBV (SOT-23)	DCK (SC70)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	113.4	149.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.3	58.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.3	41.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.6	1.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	35	41.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

+V_{DD} = 2.35 V to 5.25 V, T_A = –40°C to 125°C, $f_{(sample)}$ = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
	Full-scale input voltage span(1)		0		V_{DD}	V
	Absolute input voltage range	+IN	–0.2		V_{DD}+0.2	V
C_I	Input capacitance(2)			21		pF
I_{lkg}	Input leakage current	T_A = 125°C		40		nA
SYSTEM PERFORMANCE						
	Resolution			12		Bits
	No missing codes	ADS7886SB	12			Bits
		ADS7886S	11			
INL	Integral nonlinearity	ADS7886SB	–1.25	±0.65	1.25	LSB(3)
		ADS7886S	2		2	
DNL	Differential nonlinearity	ADS7886SB	–1	+0.4/-0.65	1	LSB
		ADS7886S	–2		2	
E_O	Offset error(4)	V_{DD} = 2.35 V to 3.6 V	–2.5	±0.5	2.5	LSB
		V_{DD} = 4.75 V to 5.25 V	–2	±0.5	2	
E_G	Gain error		–1.75	±0.5	1.75	LSB
SAMPLING DYNAMICS						
	Conversion time	20-MHz SCLK	760	800		ns
	Acquisition time		325			ns
	Maximum throughput rate	20-MHz SCLK			1	MHz
	Aperture delay			5		ns
	Step Response			160		ns
	Overvoltage recovery			160		ns
DYNAMIC CHARACTERISTICS						
SNR	Signal-to-noise ratio	V_{DD} = 2.35 V to 3.6 V, f_I = 100 kHz	69	71.25		dB
		V_{DD} = 4.75 V to 5.25 V, f_I = 100 kHz	70	72.25		
SINAD	Signal-to-noise and distortion	V_{DD} = 2.35 V to 3.6 V, f_I = 100 kHz	69	71.25		dB
		V_{DD} = 4.75 V to 5.25 V, f_I = 100 kHz	70	72.25		
THD	Total harmonic distortion(5)	f_I = 100 kHz		–84		dB
SFDR	Spurious free dynamic range	f_I = 100 kHz		85.5		dB
	Full power bandwidth	At –3 dB		15		MHz
DIGITAL INPUT/OUTPUT						
Logic family — CMOS						
V_{IH}	High-level input voltage	V_{DD} = 2.35 V to 3.6 V	1.8		5.25	V
		V_{DD} = 3.6 V to 5.25 V	2.4		5.25	
V_{IL}	Low-level input voltage	V_{DD} = 5 V			0.8	V
		V_{DD} = 3 V			0.4	
V_{OH}	High-level output voltage	$I_{(source)}$ = 200 µA	V_{DD} – 0.2			V
V_{OL}	Low-level output voltage	$I_{(sink)}$ = 200 µA			0.4	

(1) Ideal input span; does not include gain or offset error.
(2) See Figure 27 for details on the sampling circuit.
(3) LSB means least significant bit.
(4) Measured relative to an ideal full-scale input.
(5) Calculated on the first nine harmonics of the input frequency.

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Electrical Characteristics (continued)

$+V_{DD}$ = 2.35 V to 5.25 V, T_A = –40°C to 125°C, $f_{(sample)}$ = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY REQUIREMENTS						
$+V_{DD}$	Supply voltage		2.35	3.3	5.25	V
	Supply current (normal mode)	V_{DD} = 2.35 V to 3.6 V, 1-MHz throughput		1.3	1.5	mA
		V_{DD} = 4.75 V to 5.25 V, 1-MHz throughput		1.5	2	
		V_{DD} = 2.35 V to 3.6 V, static state			1.1	
		V_{DD} = 4.75 V to 5.25 V, static state			1.5	
	Power down state supply current	SCLK off			1	µA
		SCLK on (20 MHz)			200	
	Power dissipation at 1-MHz throughput	V_{DD} = 3 V		3.9	4.5	mW
		V_{DD} = 5 V		7.5	10	
	Power dissipation in static state	V_{DD} = 3 V			3.3	mW
		V_{DD} = 5 V			7.5	
	Power-up time				0.1	µs
	Invalid conversions after power up or reset				1	

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7.6 Timing Requirements

All specifications typical at T_A = –40°C to 125°C, V_{DD} = 2.35 V to 5.25 V (see Figure 1 and Figure 2) (unless otherwise specified)(1).

PARAMETER			TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{conv}	Conversion time	ADS7866	V_{DD} = 3 V			16 × t_{SCLK}	ns
			V_{DD} = 5 V			16 × t_{SCLK}	
t_q	Minimum quiet time needed from bus 3-state to start of next conversion		V_{DD} = 3 V	40			ns
			V_{DD} = 5 V	40			
t_{d1}	Delay time, $\overline{CS}$ low to first data (0) out		V_{DD} = 3 V		15	25	ns
			V_{DD} = 5 V		13	25	
t_{su1}	Setup time, $\overline{CS}$ low to SCLK low		V_{DD} = 3 V	10			ns
			V_{DD} = 5 V	10			
t_{d2}	Delay time, SCLK falling to SDO		V_{DD} = 3 V		15	25	ns
			V_{DD} = 5 V		13	25	
t_{h1}	Hold time, SCLK falling to data valid(2)		V_{DD} < 3 V	7			ns
			V_{DD} > 5 V	5.5			
t_{d3}	Delay time, 16th SCLK falling edge to SDO 3-state		V_{DD} = 3 V		10	25	ns
			V_{DD} = 5 V		8	20	
t_{w1}	Pulse duration, $\overline{CS}$		V_{DD} = 3 V	25	40		ns
			V_{DD} = 5 V	25	40		
t_{d4}	Delay time, $\overline{CS}$ high to SDO 3-state		V_{DD} = 3 V		17	30	ns
			V_{DD} = 5 V		15	25	
t_{wH}	Pulse duration, SCLK high		V_{DD} = 3 V	0.4 × t_{SCLK}			ns
			V_{DD} = 5 V	0.4 × t_{SCLK}			
t_{wL}	Pulse duration, SCLK low		V_{DD} = 3 V	0.4 × t_{SCLK}			ns
			V_{DD} = 5 V	0.4 × t_{SCLK}			
	Frequency, SCLK		V_{DD} = 3 V			20	MHz
			V_{DD} = 5 V			20	
t_{d5}	Delay time, second falling edge of clock and $\overline{CS}$ to enter in power down (use min spec not to accidently enter in power down) Figure 2		V_{DD} = 3 V	–2		5	ns
			V_{DD} = 5 V	–2		5	
t_{d6}	Delay time, $\overline{CS}$ and 10th falling edge of clock to enter in power down (use max spec not to accidently enter in power down) Figure 2		V_{DD} = 3 V	2		–5	ns
			V_{DD} = 5 V	2		–5	

(1) 3-V Specifications apply from 2.35 V to 3.6 V, and 5-V specifications apply from 4.75 V to 5.25 V.
(2) With 50-pf load.

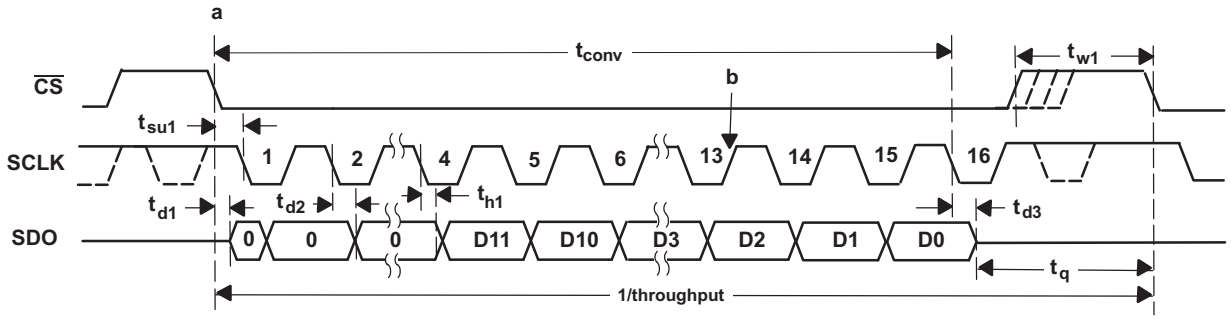


Figure 1. Interface Timing Diagram

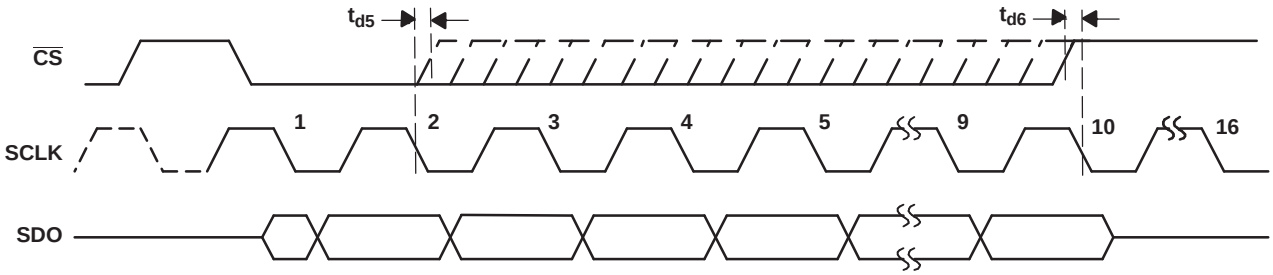


Figure 2. Entering Power Down Mode

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7.7 Typical Characteristics

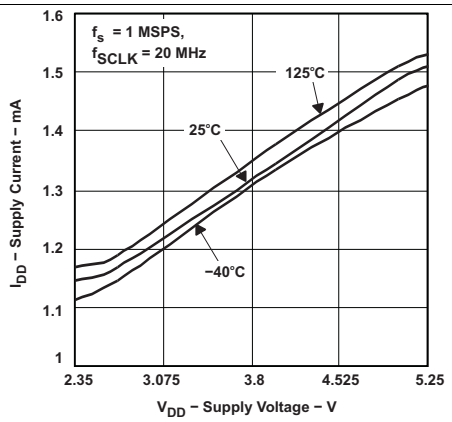


Figure 3. Supply Current vs Supply Voltage

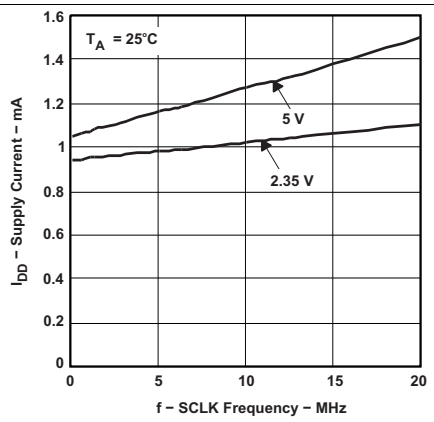


Figure 4. Supply Current vs SCLK Frequency

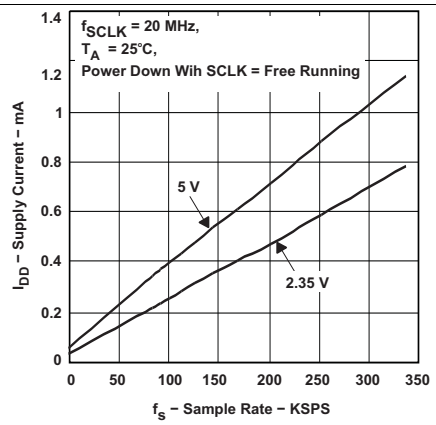


Figure 5. Supply Current vs Sample Rate

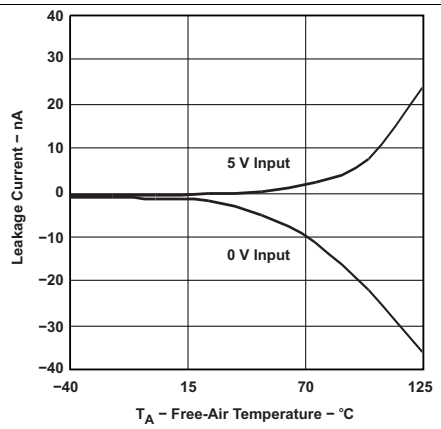


Figure 6. Analog Input Leakage Current vs Free-Air Temperature

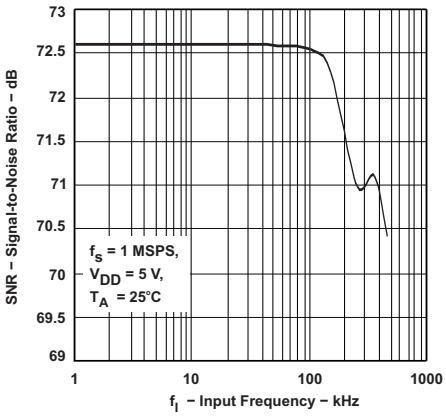


Figure 7. Signal-to-Noise Ratio vs Input Frequency

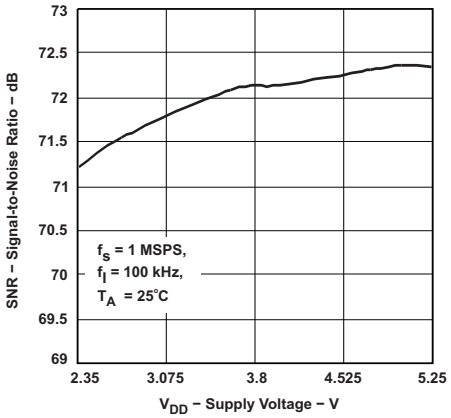


Figure 8. Signal-to-Noise Ratio vs Supply Voltage

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Typical Characteristics (continued)

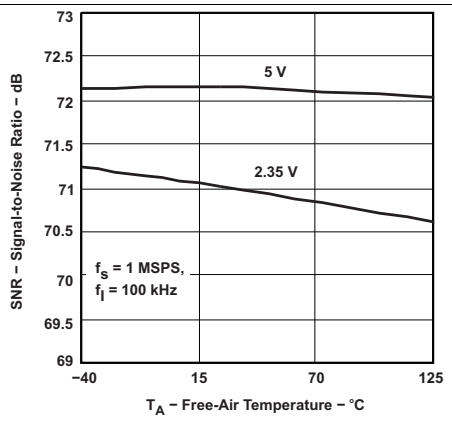


Figure 9. Signal-to-Noise Ratio vs Free-Air Temperature

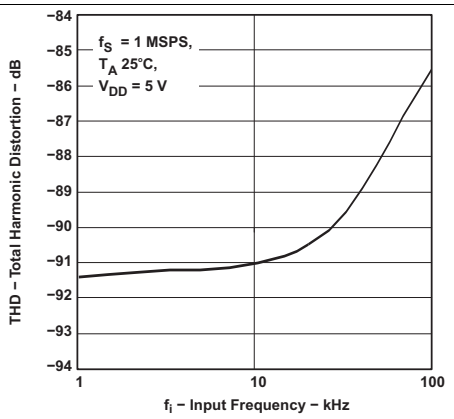


Figure 10. Total Harmonic Distortion vs Input Frequency

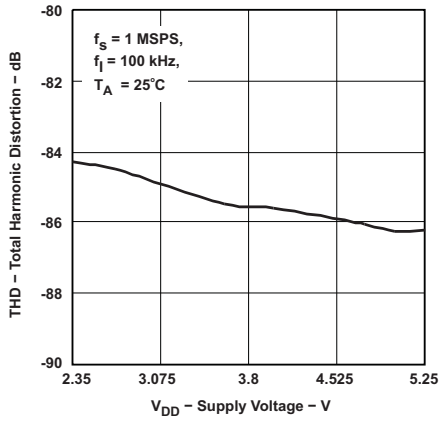


Figure 11. Total Harmonic Distortion vs Supply Voltage

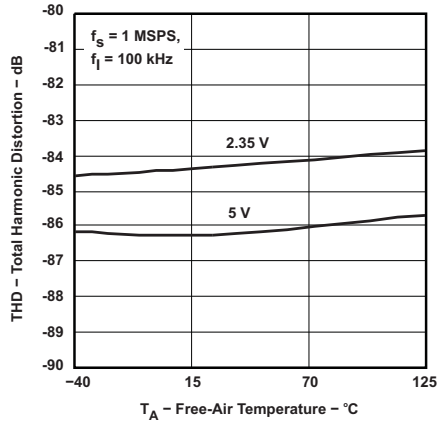


Figure 12. Total Harmonic Distortion vs Free-Air Temperature

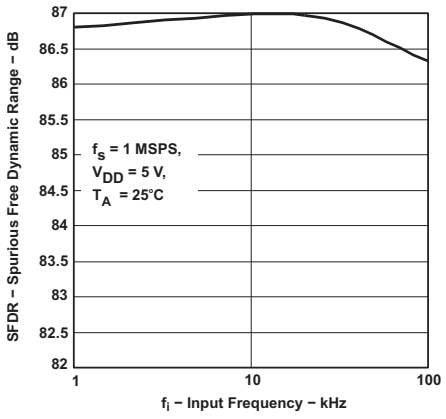


Figure 13. Spurious Free Dynamic Range vs Input Frequency

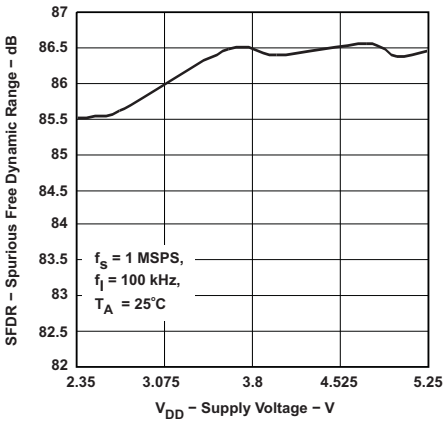


Figure 14. Spurious Free Dynamic Range vs Supply Voltage

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Typical Characteristics (continued)

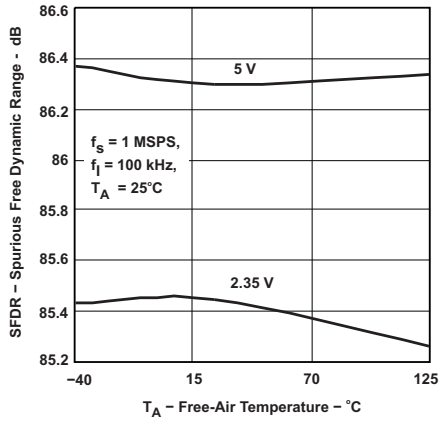


Figure 15. Spurious Free Dynamic Range vs Supply Voltage

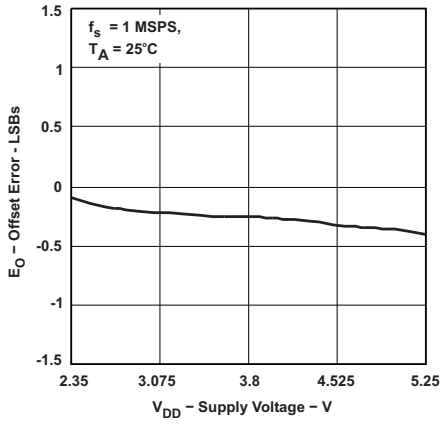


Figure 16. Offset Error vs Supply Voltage

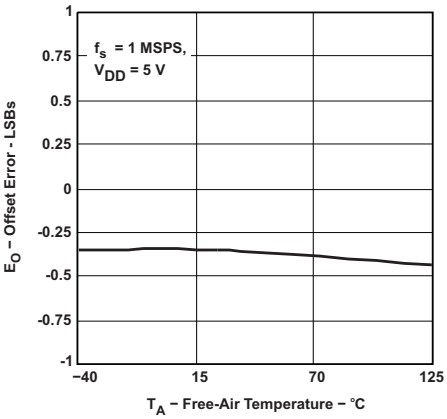


Figure 17. Offset Error vs Free-Air Temperature

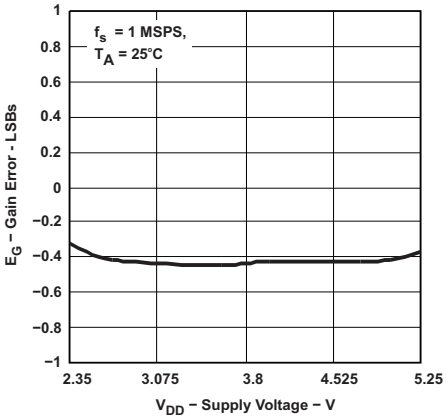


Figure 18. Gain Error vs Supply Voltage

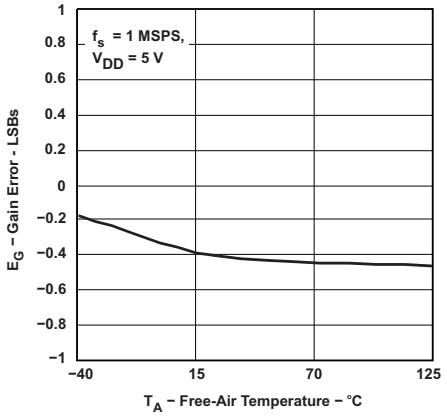


Figure 19. Gain Error vs Free-Air Temperature

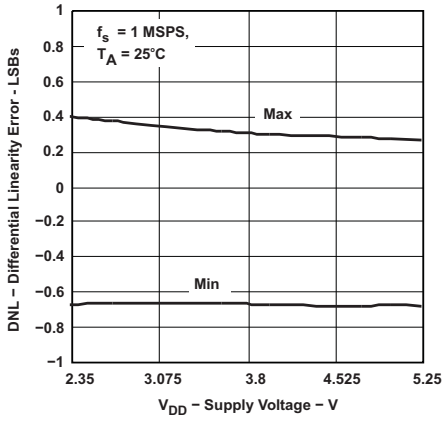


Figure 20. Differential Linearity Error vs Supply Voltage

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Typical Characteristics (continued)

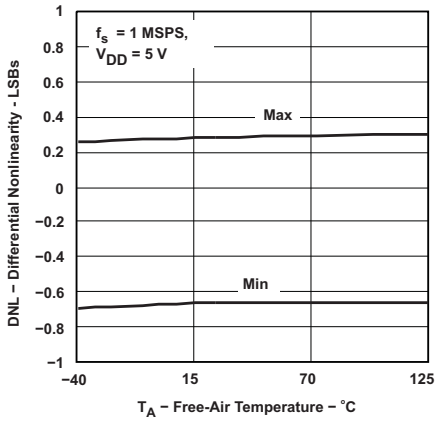


Figure 21. Differential Nonlinearity vs Free-Air Temperature

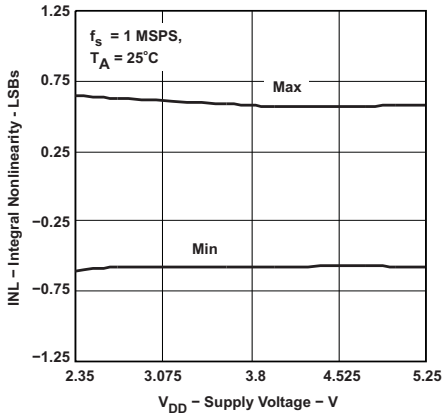


Figure 22. Integral Nonlinearity vs Supply Voltage

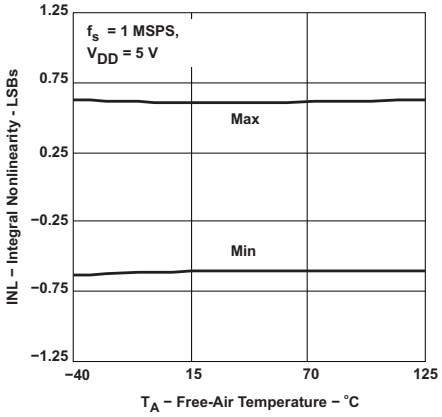


Figure 23. Integral Nonlinearity vs Free-Air Temperature

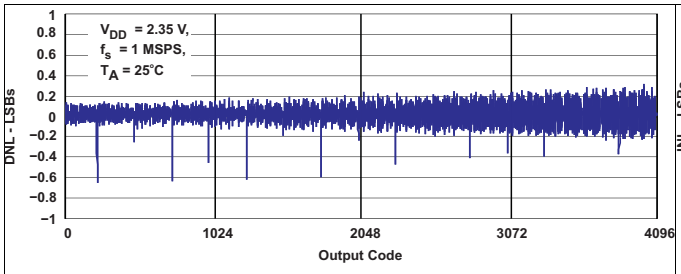


Figure 24. DNL

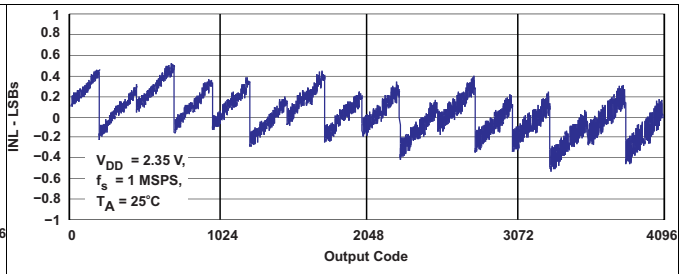


Figure 25. INL

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Typical Characteristics (continued)

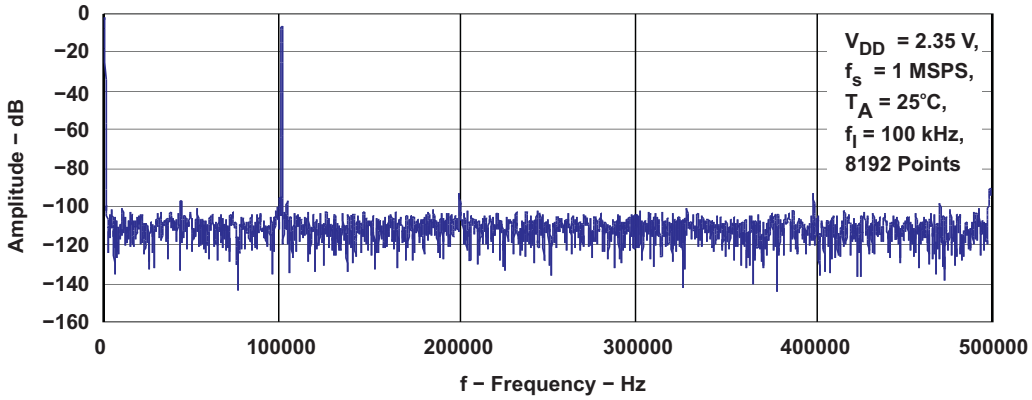


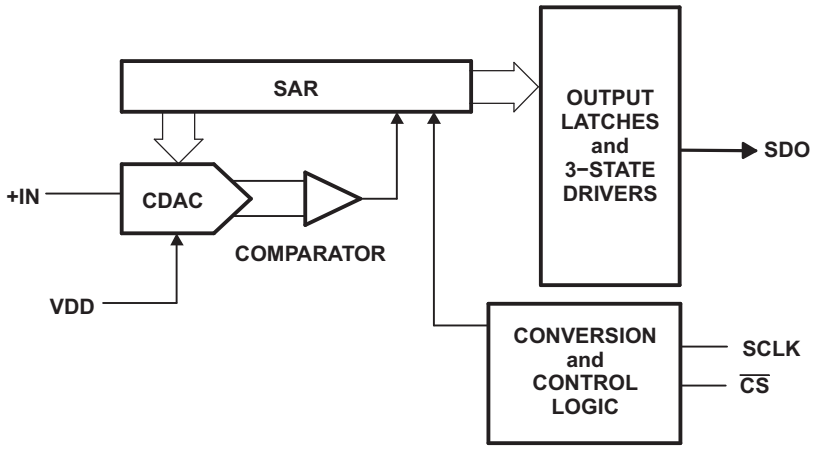
Figure 26. FFT

8 Detailed Description

8.1 Overview

The ADS7886 is 12-bit, 1-MSPS analog-to-digital converter (ADC). The device includes a capacitor-based SAR A/D converter with inherent sample and hold circuitry. The serial interface in device is controlled by the CS and SCLK signals for easy interface with microprocessors and DSPs. The input signal is sampled with the falling edge of CS, and SCLK is used for conversion and serial data output. The device operates from a wide supply range from 2.35 V to 5.25 V. The low power consumption of the device makes it suitable for battery-powered applications. The device also includes a power-saving, power-down feature which is useful when the device is operated at lower conversion speeds. The high level of the digital input to the device is not limited to device VDD. This means the digital input can go as high as 5.25 V when device supply is 2.35 V. This feature is useful when digital signals are coming from other circuit with different supply levels. This also relaxes the restrictions on power-up sequencing.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Driving the VIN and V_{DD} Pins

The VIN input should be driven with a low impedance source. In most cases additional buffers are not required. In cases where the source impedance exceeds 200 Ω, using a buffer would help achieve the rated performance of the converter. The THS4031 is a good choice for the driver amplifier buffer.

The reference voltage for the A/D converter is derived from the supply voltage internally. The devices offer limited low-pass filtering functionality on-chip. The supply to these converters should be driven with a low impedance source and should be decoupled to the ground. A 1-µF storage capacitor and a 10-nF decoupling capacitor should be placed close to the device. Wide, low impedance traces should be used to connect the capacitor to the pins of the device. The ADS7886 draws very little current from the supply lines. The supply line can be driven by either:

- Directly from the system supply.
- A reference output from a low drift and low drop out reference voltage generator like REF3030 or REF3130. The ADS7886 operates from a wide range of supply voltages. The actual choice of the reference voltage generator would depend upon the system. Figure 33 shows one possible application circuit.
- A low-pass filtered system supply followed by a buffer, like the zero-drift OPA735, can also be used in cases where the system power supply is noisy. Care must be taken to ensure that the voltage at the V_{DD} input does not exceed 7 V to avoid damage to the converter. This can be done easily using single supply CMOS amplifiers like the OPA735. Figure 34 shows one possible application circuit.

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Feature Description (continued)

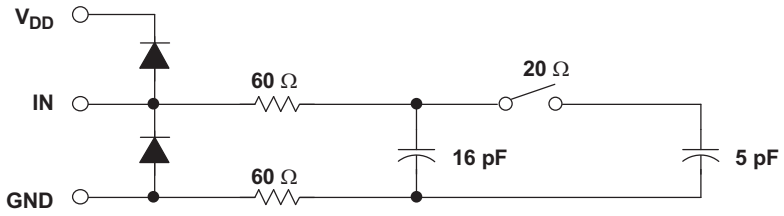


Figure 27. Typical Equivalent Sampling Circuit

8.4 Device Functional Modes

8.4.1 Normal Operation

The cycle begins with the falling edge of $\overline{CS}$. This point is indicated as **a** in Figure 1. With the falling edge of $\overline{CS}$, the input signal is sampled and the conversion process is initiated. The device outputs data while the conversion is in progress. The data word contains 4 leading zeros, followed by 12-bit data in MSB first format.

The falling edge of $\overline{CS}$ clocks out the first zero, and a zero is clocked out on every falling edge of the clock until the third edge. Data is in MSB first format with the MSB being clocked out on the 4th falling edge. On the 16th falling edge of SCLK, SDO goes to the 3-state condition. The conversion ends on the 16th falling edge of SCLK. The device enters the acquisition phase on the first rising edge of SCLK after the 13th falling edge. This point is indicated by **b** in Figure 1.

$\overline{CS}$ can be asserted (pulled high) after 16 clocks have elapsed. It is necessary not to start the next conversion by pulling $\overline{CS}$ low until the end of the quiet time (t_q) after SDO goes to 3-state. To continue normal operation, it is necessary that $\overline{CS}$ is not pulled high until point **b**. Without this, the device does not enter the acquisition phase and no valid data is available in the next cycle. (Also refer to power down mode for more details.) $\overline{CS}$ going high any time after the conversion start aborts the ongoing conversion and SDO goes to 3-state.

The high level of the digital input to the device is not limited to device V_{DD}. This means the digital input can go as high as 5.25 V when the device supply is 2.35 V. This feature is useful when digital signals are coming from another circuit with different supply levels. Also, this relaxes the restriction on power up sequencing. However, the digital output levels (V_{OH} and V_{OL}) are governed by V_{DD} as listed in the *Electrical Characteristics* table.

8.4.2 Power Down Mode

The device enters power down mode if $\overline{CS}$ goes high anytime after the 2nd SCLK falling edge to before the 10th SCLK falling edge. Ongoing conversion stops and SDO goes to 3-state under this power down condition as shown in Figure 2.

A dummy cycle with $\overline{CS}$ low for more than 10 SCLK falling edges brings the device out of power down mode. For the device to come to the fully powered up condition it takes 1 µs. $\overline{CS}$ can be pulled high any time after the 10th falling edge as shown in Figure 28. It is not necessary to continue until the 16th clock if the next conversion starts 1 µs after $\overline{CS}$ going low of the dummy cycle and the quiet time (t_q) condition is met.

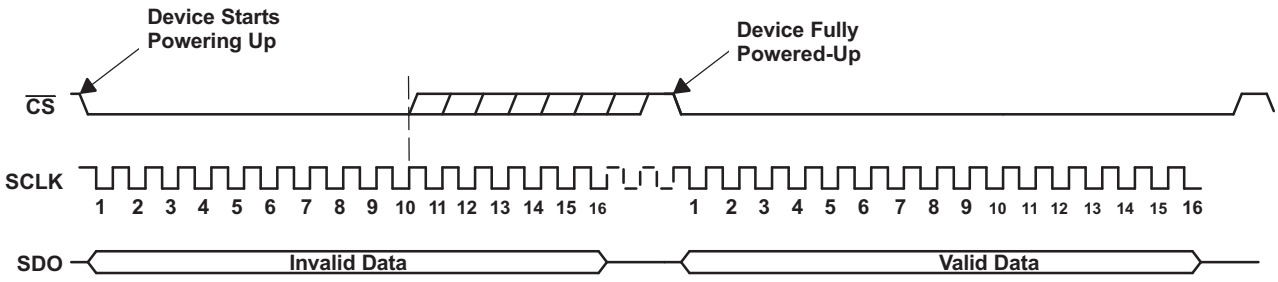


Figure 28. Exiting Power Down Mode

9 Application and Implementation

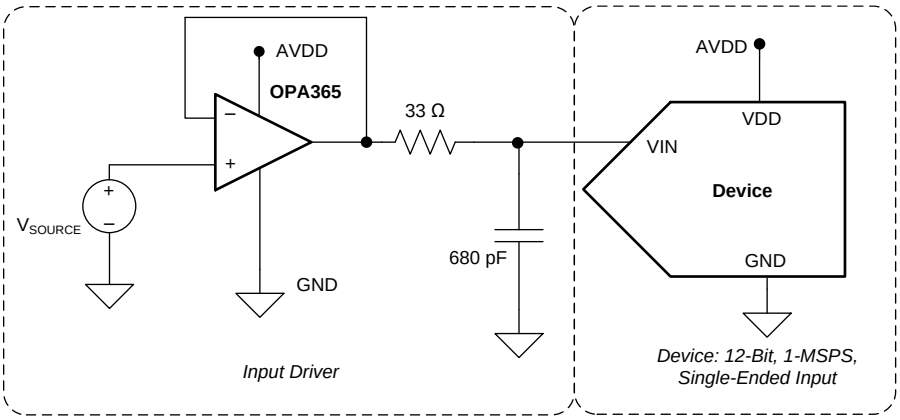
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR), analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section details some general principles for designing the input driver circuit, reference driver circuit, and provides some application circuits designed for the ADS7886.

9.2 Typical Application



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Figure 29. Typical Data Acquisition (DAQ) Circuit: Single-Supply DAQ

9.2.1 Design Requirements

The goal of this application is to design a single-supply digital acquisition (DAQ) circuit based on the ADS7886 with SNR greater than 72.5 dB and THD less than –84 dB for input frequencies of 2 kHz to 100 kHz at a throughput of 1 MSPS.

9.2.2 Detailed Design Procedure

To achieve a SINAD of 61 dB, the operational amplifier must have high bandwidth to settle the input signal within the acquisition time of the ADC. The operational amplifier must have low noise to keep the total system noise below 20% of the input-referred noise of the ADC. For the application circuit shown in Figure 29, OPA365 is selected for its high bandwidth (50 MHz) and low noise (4.5 nV$\sqrt{Hz}$).

The reference voltage for the ADS7887 and ADS7888 A/D converters are derived from the supply voltage internally. The supply to these converters must be driven with a low impedance source and must be decoupled to the ground. To drive supply pin of ADS7887 ultra-low noise fast transient response low dropout voltage regulator TPS73201 is selected. Alternatively one can drive supply pin with low impedance voltage reference similar to REF3030.

For a step-by-step design procedure for low power, small form factor digital acquisition (DAQ) circuit based on similar SAR ADCs, see TI Precision Design, *Three 12-Bit Data Acquisition Reference Designs Optimized for Low Power and Ultra-Small Form Factor* (TIDU390).

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Typical Application (continued)

9.2.3 Application Curves

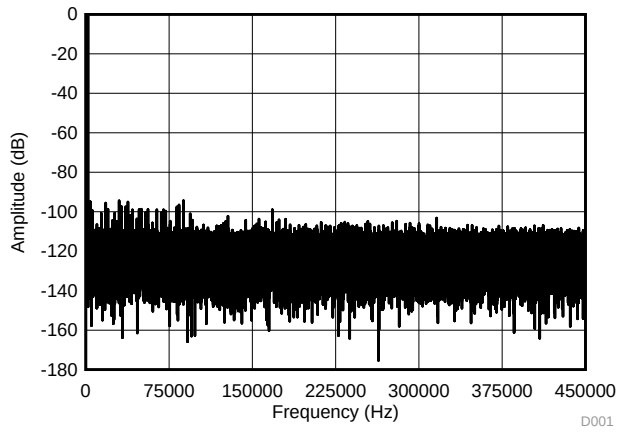


Figure 30. Test Results for the ADS7886 and OPA365 for a 2-kHz Input

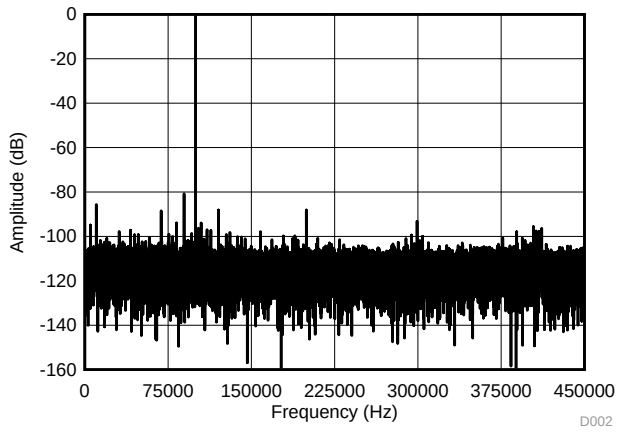


Figure 31. Test Results for the ADS7886 and OPA365 for a 100-kHz Input

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10 Power Supply Recommendations

The reference voltage for the ADS7886 A/D converter is derived from the supply voltage internally. The supply to ADS7886 should be driven with a low impedance source and should be decoupled to the ground. Decouple the VDD with 1-µF ceramic decoupling capacitors, as shown in Figure 32. Always set the VDD supply to be greater than or equal to the maximum input signal to avoid saturation of codes.

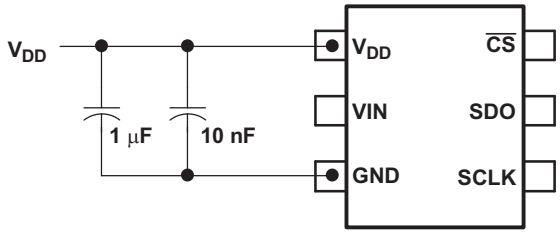


Figure 32. Supply/Reference Decoupling Capacitors

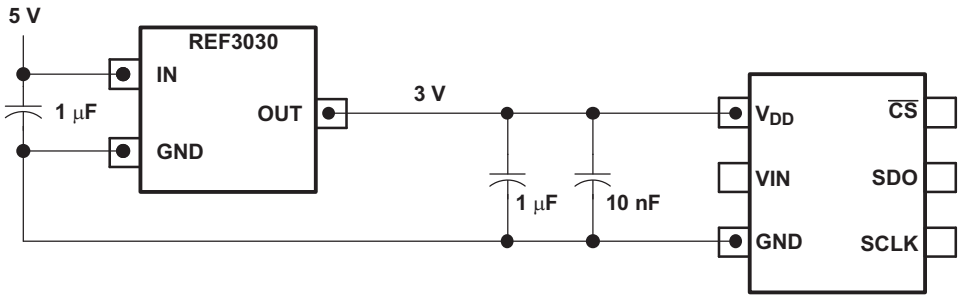


Figure 33. Using the REF3030 Reference

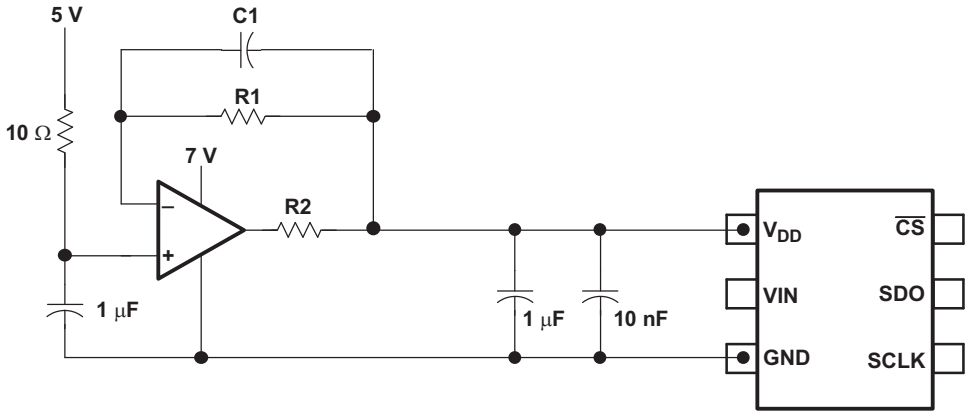


Figure 34. Buffering With the OPA735

11 Layout

11.1 Layout Guidelines

Figure 35 shows a board layout example for the ADS7886. Some of the key considerations are

1. Use a ground plane underneath the device and partition the PCB into analog and digital sections.
2. Avoid crossing digital lines with the analog signal path.
3. The power sources to the device must be clean and well-bypassed. Use 1-µF ceramic bypass capacitors in close proximity to the supply pin (VDD).

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Layout Guidelines (continued)

4. Avoid placing vias between the VDD and bypass capacitors.
5. Connect ground pin to the ground plane using short, low-impedance path.
6. The fly-wheel RC filters are placed close to the device.

Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance precision. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.

11.2 Layout Example

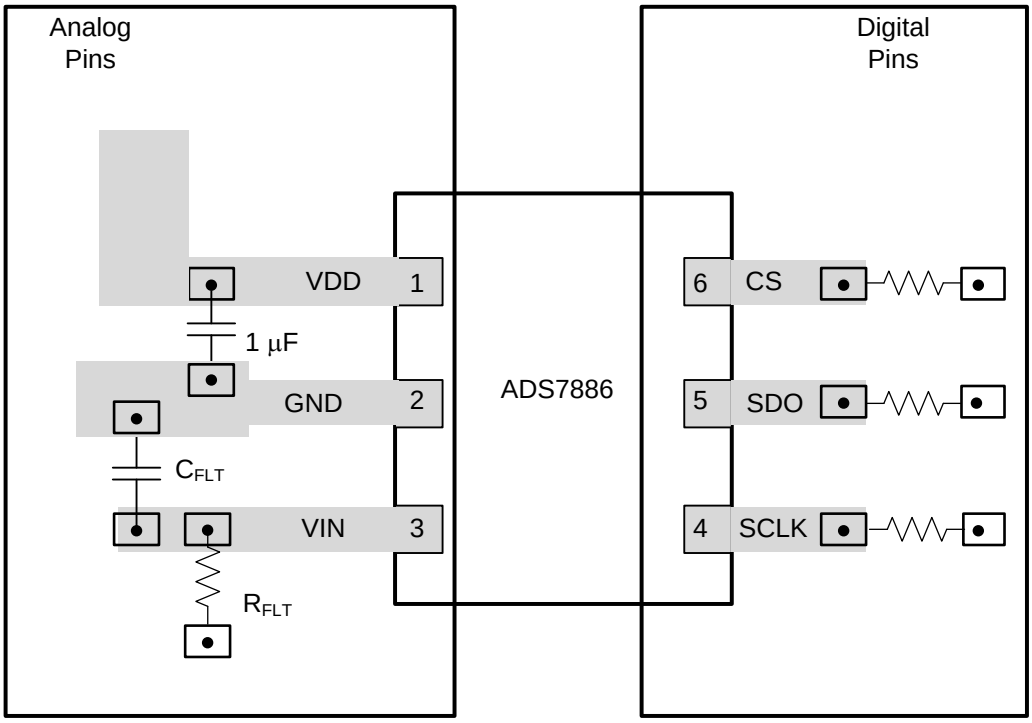


Figure 35. ADS7886 Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *OPAx365 50-MHz, Zerø-Crossover, Low-Distortion, High CMRR, RRI/O, Single-Supply Operational Amplifier* (SBOS365)
- *Cap-Free NMOS 250-mA Low Dropout Regulator With Reverse Current Protection* (SGLS346)
- *Three 12-Bit Data Acquisition Reference Designs Optimized for Low Power and Ultra-Small Form Factor* (TIDU390)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS7886SBDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BBAQ
ADS7886SBDBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BBAQ
ADS7886SBDBVT	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BBAQ
ADS7886SBDBVT.A	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BBAQ
ADS7886SBDCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BNL
ADS7886SBDCKR.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BNL
ADS7886SBDCKT	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BNL
ADS7886SBDCKT.A	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BNL
ADS7886SDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BBAQ
ADS7886SDBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BBAQ
ADS7886SDBVT	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BBAQ
ADS7886SDBVT.A	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BBAQ
ADS7886SDCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BNL
ADS7886SDCKR.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BNL
ADS7886SDCKT	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BNL
ADS7886SDCKT.A	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BNL

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

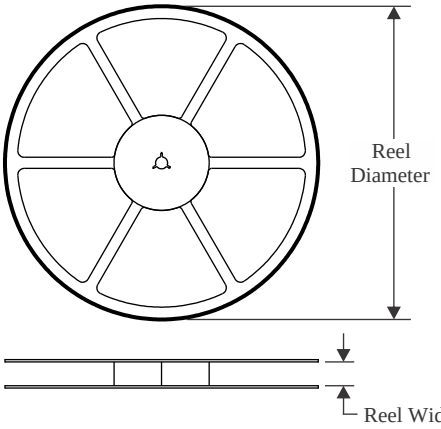
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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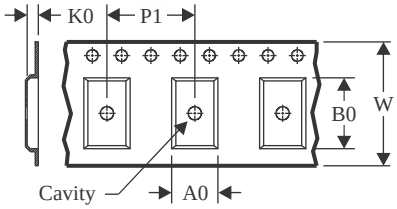
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

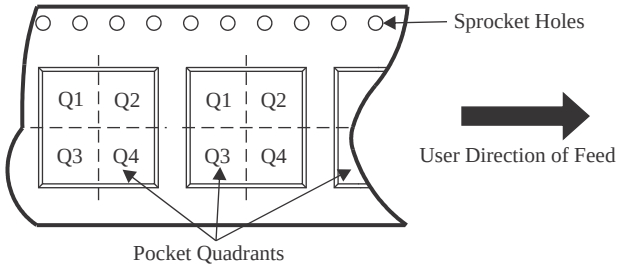


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

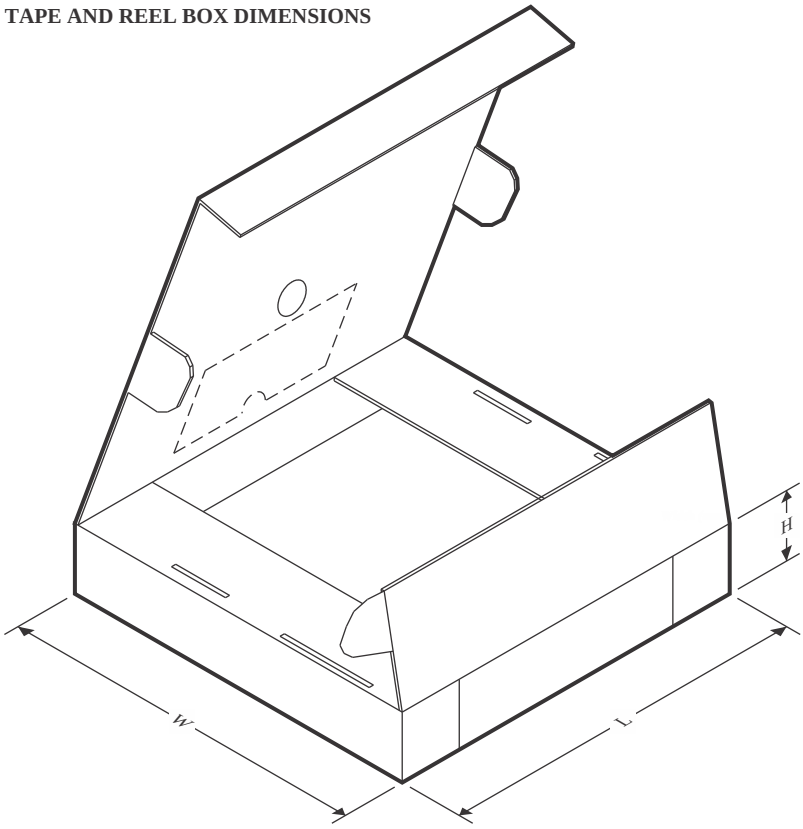
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7886SBDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADS7886SBDBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADS7886SBDCKR	SC70	DCK	6	3000	180.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
ADS7886SBDCKT	SC70	DCK	6	250	180.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
ADS7886SDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADS7886SDBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADS7886SDCKR	SC70	DCK	6	3000	180.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
ADS7886SDCKT	SC70	DCK	6	250	180.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

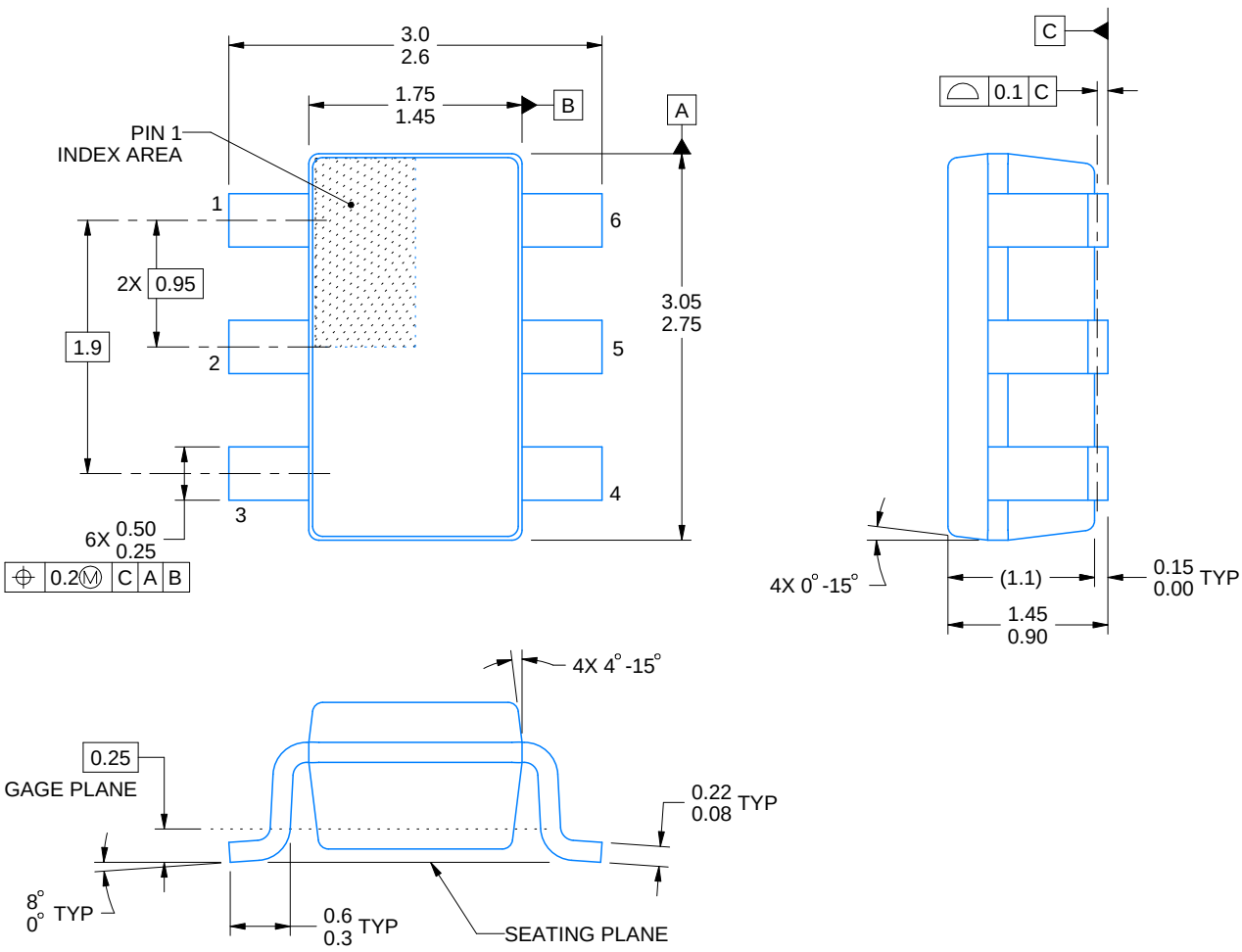
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7886SBDBVR	SOT-23	DBV	6	3000	213.0	191.0	35.0
ADS7886SBDBVT	SOT-23	DBV	6	250	213.0	191.0	35.0
ADS7886SBDCKR	SC70	DCK	6	3000	213.0	191.0	35.0
ADS7886SBDCKT	SC70	DCK	6	250	213.0	191.0	35.0
ADS7886SDBVR	SOT-23	DBV	6	3000	213.0	191.0	35.0
ADS7886SDBVT	SOT-23	DBV	6	250	213.0	191.0	35.0
ADS7886SDCKR	SC70	DCK	6	3000	213.0	191.0	35.0
ADS7886SDCKT	SC70	DCK	6	250	213.0	191.0	35.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

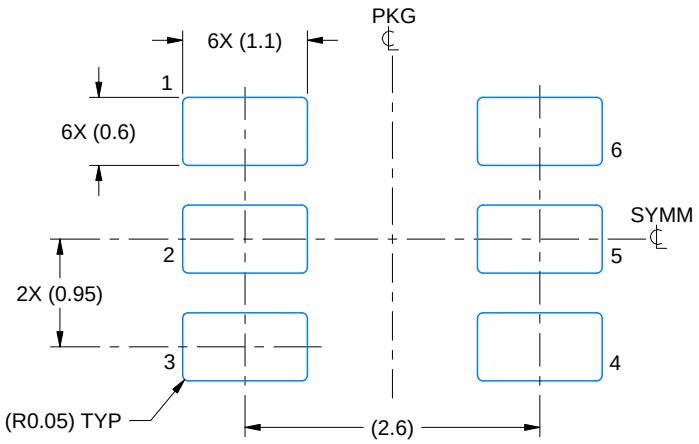
SMALL OUTLINE TRANSISTOR



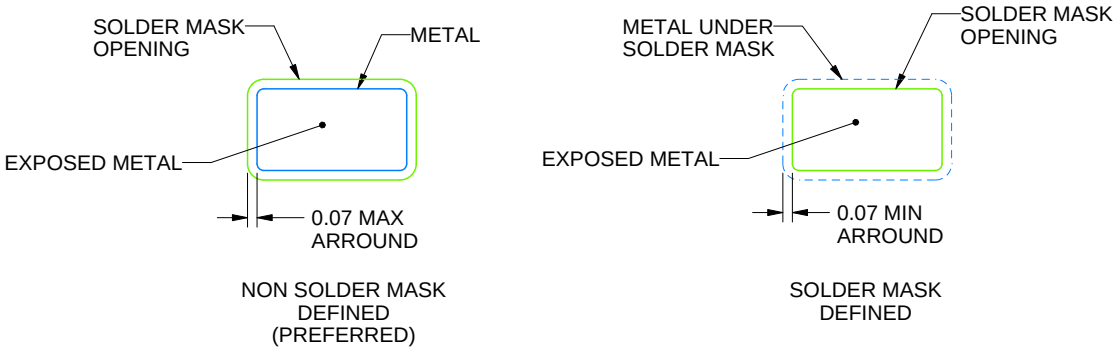
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

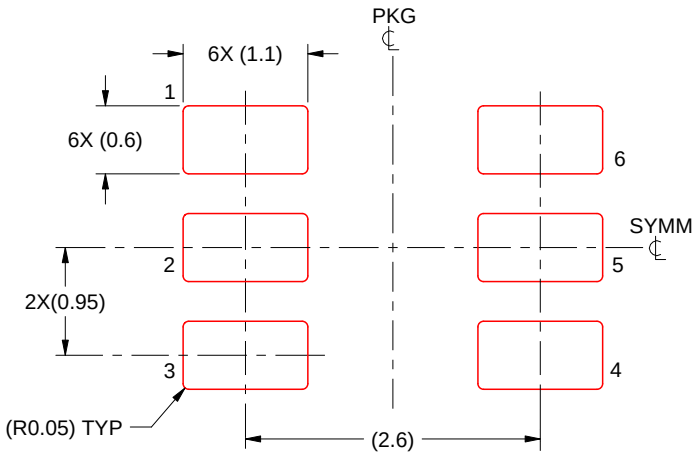


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

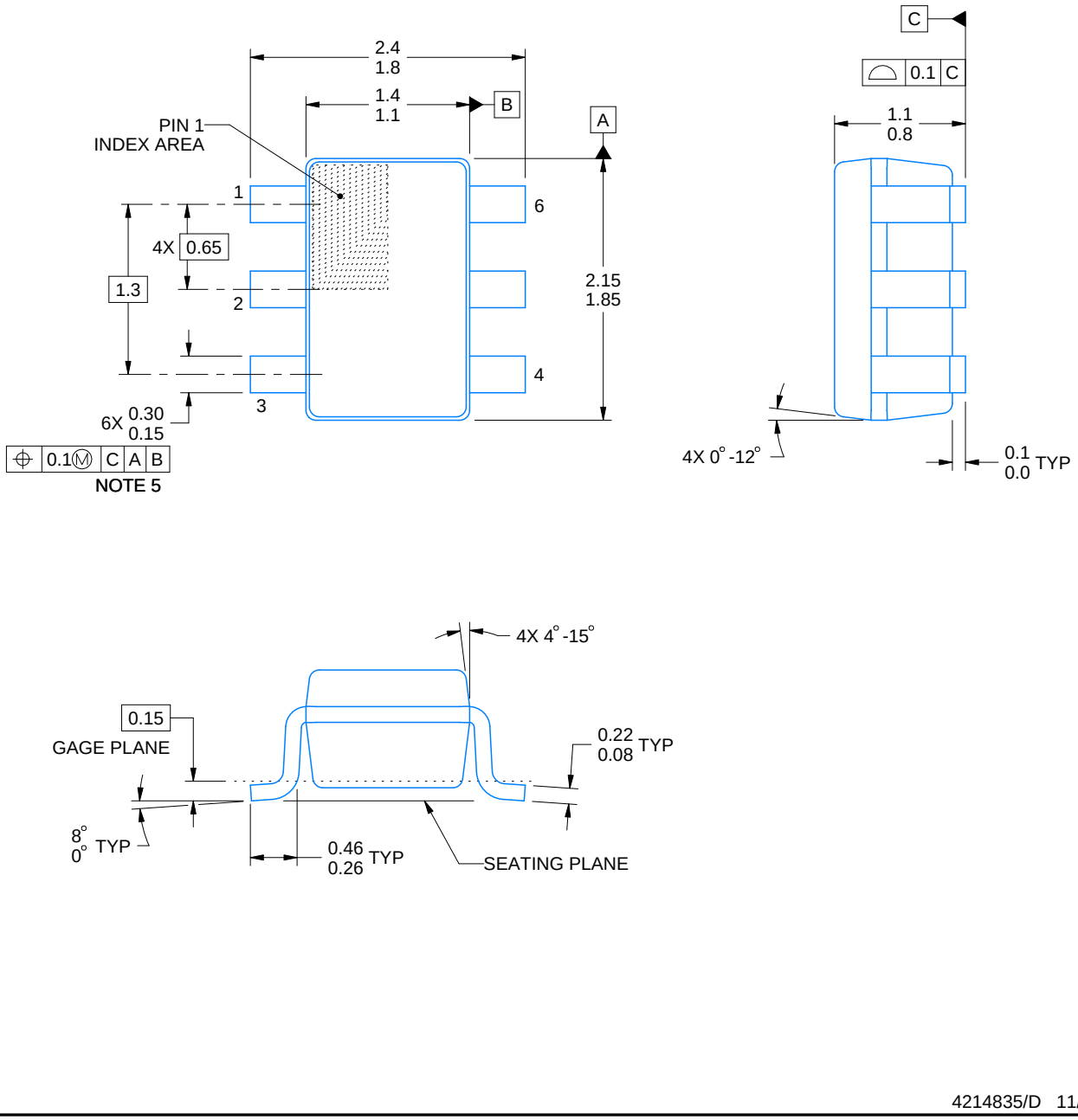
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

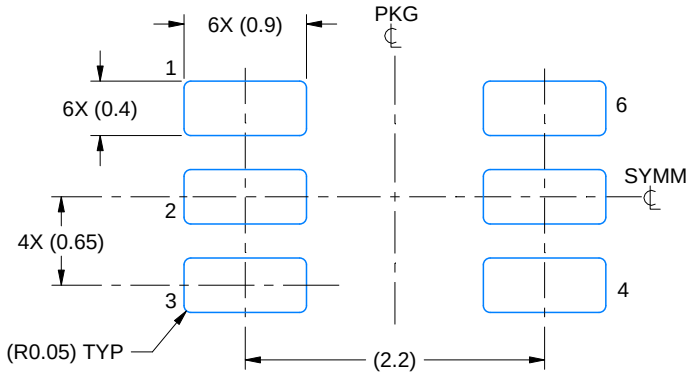
SMALL OUTLINE TRANSISTOR



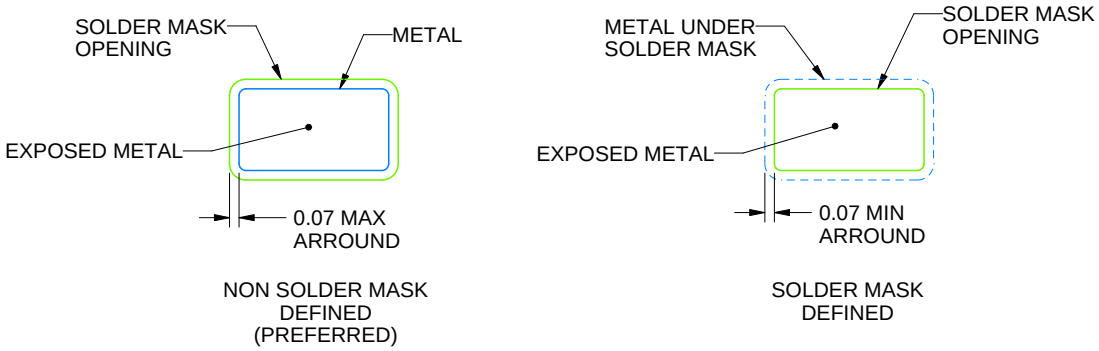
4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

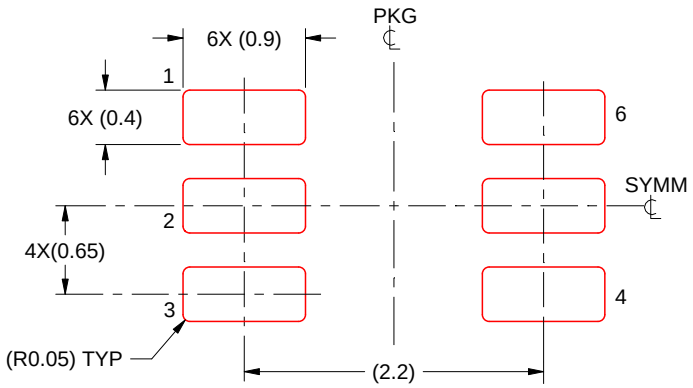


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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