ADS788x 10-Bit, 8-Bit, 1.25-MSPS, Micro-Power, Miniature SAR Analog-to-Digital Converters

1 Features

- 1.25-MHz Sample Rate Serial Device
- 10-Bit Resolution (ADS7887)
- 8-Bit Resolution (ADS7888)
- Zero Latency
- 25-MHz Serial Interface
- Supply Range: 2.35 V to 5.25 V
- Typical Power Dissipation at 1.25 MSPS:
  - 3.8 mW at 3-V V_{DD}
  - 8 mw at 5-V V_{DD}
- ±0.35 LSB INL, DNL (ADS7887)
- ±0.15 LSB INL, ±0.1 LSB DNL (ADS7888)
- 61 dB SINAD, –84 dB THD (ADS7887)
- 49.5 dB SINAD, –67.5 dB THD (ADS7888)
- Unipolar Input Range: 0 V to V_{DD}
- Power-Down Current: 1 µA
- Wide Input Bandwidth: 15 MHz at 3 dB
- 6-Pin SOT23 and SC70 Packages

2 Applications

- Base Band Converters in Radio Communication
- Motor Current and Bus Voltage Sensors in Digital Drives
- Optical Networking (DWDM, MEMS-Based Switching)
- Optical Sensors
- Battery-Powered Systems
- Medical Instrumentations
- High-Speed Data Acquisition Systems
- High-Speed Closed-Loop Systems

3 Description

The ADS7887 device is a 10-bit, 1.25-MSPS, analog-to-digital converter (ADC), and the ADS7888 device is a 8-bit, 1.25-MSPS ADC. These devices include a capacitor-based SAR A/D converter with inherent sample and hold. The serial interface in each device is controlled by the $\overline{CS}$ and SCLK signals for glueless connections with microprocessors and DSPs. The input signal is sampled with the falling edge of $\overline{CS}$, and SCLK is used for conversion and serial data output.

The devices operate from a wide supply range from 2.35 V to 5.25 V. The low power consumption of the devices make them suitable for battery-powered applications. The devices also include a power-saving, power-down feature for when the devices are operated at lower conversion speeds.

The high level of the digital input to the device is not limited to device V_{DD}. This means the digital input can go as high as 5.25 V when device supply is 2.35 V. This feature is useful when digital signals are coming from other circuit with different supply levels. Also this relaxes restriction on power-up sequencing.

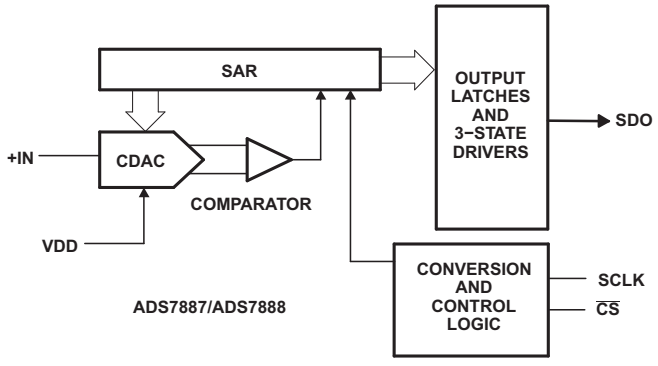
The ADS7887 and ADS7888 are available in 6-pin SOT-23 and SC70 packages and are specified for operation from –40°C to 125°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS7887 ADS7888	SOT-23 (6)	2.90 mm × 1.60 mm
	SC70 (6)	2.00 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2005) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Changed *Thermal Information* table	6

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5 Companion Products

PART NUMBER	NAME
SN74LVTH245A	3.3-V ABT Octal Bus Transceivers With 3-State Outputs
LMV761	Low Voltage, Precision Comparator with Push-Pull Output
TPS54418	2.95V to 6V Input, 4A Synchronous Step-Down SWIFT™ Converter
LMV339	Quad General Purpose Low-Voltage Comparators
TPS730	Low-Noise, High PSRR, RF 200-mA Low-Dropout Linear Regulators

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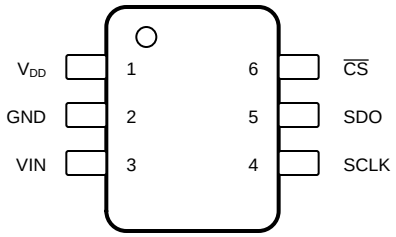
6 Device Comparison

BIT	< 300 KSPS	300 KSPS – 1.25 MSPS
12-Bit	ADS7866 (1.2 V_{DD} to 3.6 V_{DD})	ADS7886 (2.35 V_{DD} to 5.25 V_{DD})
10-Bit	ADS7867 (1.2 V_{DD} to 3.6 V_{DD})	ADS7887 (2.35 V_{DD} to 5.25 V_{DD})
8-Bit	ADS7868 (1.2 V_{DD} to 3.6 V_{DD})	ADS7888 (2.35 V_{DD} to 5.25 V_{DD})

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7 Pin Configuration and Functions

DBV or DCK Package
6-Pin SOT-23 or SC70
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{DD}	—	Power supply input also acts like a reference voltage to ADC.
2	GND	—	Ground for power supply, all analog and digital signals are referred with respect to this pin.
3	VIN	I	Analog signal input
4	SCLK	I	Serial clock
5	SDO	O	Serial data out
6	$\overline{CS}$	I	Chip select signal, active low

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8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
+IN to AGND		–0.3	V_{DD} + 0.3	V
$+V_{DD}$ to AGND		–0.3	7	V
Digital input voltage to GND		–0.3	7	V
Digital output to GND		–0.3	V_{DD} + 0.3	V
Power dissipation, both packages		$(T_{J(MAX)} – T_A) / R_{\theta JA}$		
Lead temperature, soldering	Vapor phase (60 s)		215	°C
	Infrared (15 s)		220	
Junction temperature, $T_{J(MAX)}$			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T_A	Operating temperature	–40	125	°C

8.4 Thermal Information

THERMAL METRIC(1)		ADS7887, ADS7888		UNIT
		DBV (SOT-23)	DCK (SC70)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.9	150.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.6	62.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.5	43	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.8	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36.2	42.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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8.5 Electrical Characteristics – ADS7887

$+V_{DD}$ = 2.35 V to 5.25 V, T_A = –40°C to 125°C, and f_{sample} = 1.25 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
	Full-scale input voltage span(1)		0		V_{DD}	V
	Absolute input voltage range	+IN	–0.2		V_{DD} + 0.2	V
C_i	Input capacitance(2)			21		pF
I_{llkg}	Input leakage current	T_A = 125°C		40		nA
SYSTEM PERFORMANCE						
	Resolution			10		Bits
	No missing codes		10			Bits
INL	Integral nonlinearity		–0.75	±0.35	0.75	LSB(3)
DNL	Differential nonlinearity		–0.5	±0.35	0.5	LSB
E_O	Offset error(4)(5)(6)		–1.5	±0.5	1.5	LSB
E_G	Gain error(5)		–1	±0.5	1	LSB
SAMPLING DYNAMICS						
	Conversion time	25-MHz SCLK	530	560		ns
	Acquisition time		260			ns
	Maximum throughput rate	25-MHz SCLK			1.25	MHz
	Aperture delay			5		ns
	Step Response			160		ns
	Overvoltage recovery			160		ns
DYNAMIC CHARACTERISTICS						
THD	Total harmonic distortion(7)	100 kHz		–84	–72	dB
SINAD	Signal-to-noise and distortion	100 kHz	60.5	61		dB
SFDR	Spurious free dynamic range	100 kHz	73	81		dB
	Full power bandwidth	At –3 dB		15		MHz
DIGITAL INPUT/OUTPUT						
V_{IH}	High-level input voltage	VDD = 2.35 V to 5.25 V	V_{DD} – 0.4		5.25	V
V_{IL}	Low-level input voltage	V_{DD} = 5 V			0.8	V
		V_{DD} = 3 V			0.4	
V_{OH}	High-level output voltage	At I_{source} = 200 µA	V_{DD} – 0.2			V
V_{OL}	Low-level output voltage	At I_{sink} = 200 µA			0.4	
POWER SUPPLY REQUIREMENTS						
$+V_{DD}$	Supply voltage		2.35	3.3	5.25	V
	Supply current (normal mode)	At V_{DD} = 2.35 V to 5.25 V, 1.25-MHz throughput			2	mA
		At V_{DD} = 2.35 V to 5.25 V, static state			1.5	
	Power-down state supply current	SCLK off			1	µA
		SCLK on (25 MHz)			200	
	Power dissipation at 1.25-MHz throughput	V_{DD} = 5 V		8	10	mW
		V_{DD} = 3 V		3.8	6	
	Power dissipation in static state	V_{DD} = 5 V		5.5	7.5	mW
		V_{DD} = 3 V		3	4.5	
	Power-down time				0.1	µs

(1) Ideal input span; does not include gain or offset error.
(2) Refer Figure 31 for details on sampling circuit
(3) LSB means least significant bit
(4) Measured relative to an ideal full-scale input
(5) Offset error and gain error ensured by characterization.
(6) First transition of 000H to 001H at 0.5 × ($V_{ref}/2^{10}$)
(7) Calculated on the first nine harmonics of the input frequency

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Electrical Characteristics – ADS7887 (continued)

$+V_{DD}$ = 2.35 V to 5.25 V, T_A = –40°C to 125°C, and f_{sample} = 1.25 MHz (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power-up time				0.8	µs
Invalid conversions after power up				1	

8.6 Electrical Characteristics – ADS7888

$+V_{DD}$ = 2.35 V to 5.25 V, T_A = –40°C to 125°C, and f_{sample} = 1.25 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
	Full-scale input voltage span(1)		0		V_{DD}	V
	Absolute input voltage range	+IN	–0.2		V_{DD} + 0.2	V
C_i	Input capacitance(2)			21		pF
I_{lkg}	Input leakage current	T_A = 125°C		40		nA
SYSTEM PERFORMANCE						
	Resolution			8		Bits
	No missing codes		8			Bits
INL	Integral nonlinearity		–0.3	±0.15	0.3	LSB(3)
DNL	Differential nonlinearity		–0.3	±0.1	0.3	LSB
E_O	Offset error(4) (5) (6)		–0.5	±0.15	0.5	LSB
E_G	Gain error(5)		–0.5	±0.15	0.5	LSB
SAMPLING DYNAMICS						
	Conversion time	25-MHz SCLK	450	480		ns
	Acquisition time	1.5 MSPS mode, see Figure 34	206			ns
	Maximum throughput rate	25-MHz SCLK			1.25	MHz
	Aperture delay			5		ns
	Step Response			160		ns
	Overvoltage recovery			160		ns
DYNAMIC CHARACTERISTICS						
THD	Total harmonic distortion(7)	100 kHz		–67.5	–65	dB
SINAD	Signal-to-noise and distortion	100 kHz	49	49.5		dB
SFDR	Spurious free dynamic range	100 kHz	65	77		dB
	Full power bandwidth	At –3 dB		15		MHz
DIGITAL INPUT/OUTPUT						
V_{IH}	High-level input voltage	V_{DD} = 2.35 V to 5.25 V	V_{DD} – 0.4		5.25	V
V_{IL}	Low-level input voltage	V_{DD} = 5 V			0.8	V
		V_{DD} = 3 V			0.4	
V_{OH}	High-level output voltage	At I_{source} = 200 µA	V_{DD} – 0.2			V
V_{OL}	Low-level output voltage	At I_{sink} = 200 µA			0.4	
POWER SUPPLY REQUIREMENTS						
$+V_{DD}$	Supply voltage		2.35	3.3	5.25	V
	Supply current (normal mode)	At V_{DD} = 2.35 V to 5.25 V, 1.25-MHz throughput			2	mA
		At V_{DD} = 2.35 V to 5.25 V, static state			1.5	

(1) Ideal input span; does not include gain or offset error.
(2) Refer Figure 31 for details on sampling circuit
(3) LSB means least significant bit
(4) Measured relative to an ideal full-scale input
(5) Offset error and gain error ensured by characterization.
(6) First transition of 000H to 001H at ($V_{ref}/2^8$)
(7) Calculated on the first nine harmonics of the input frequency

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Electrical Characteristics – ADS7888 (continued)

$+V_{DD}$ = 2.35 V to 5.25 V, T_A = –40°C to 125°C, and f_{sample} = 1.25 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Power-down state supply current	SCLK off			1	µA
		SCLK on (25 MHz)			200	
	Power dissipation at 1.25 MHz throughput	V_{DD} = 5 V		8	10	mW
		V_{DD} = 3 V		3.8	6	
	Power dissipation in static state	V_{DD} = 5 V		5.5	7.5	mW
		V_{DD} = 3 V		3	4.5	
	Power-down time				0.1	µs
	Power-up time				0.8	µs
	Invalid conversions after power up				1	

8.7 Timing Requirements

All specifications typical at T_A = –40°C to 125°C and V_{DD} = 2.35 V to 5.25 V (unless otherwise noted; see Figure 32)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
t_{conv}	Conversion time	ADS7887	V_{DD} = 3 V			14 × t_{SCLK}	ns
			V_{DD} = 5 V			14 × t_{SCLK}	
		ADS7888	V_{DD} = 3 V			12 × t_{SCLK}	
			V_{DD} = 5V			12 × t_{SCLK}	
t_q	Quiet time	Minimum time required from bus 3-state to start of next conversion	V_{DD} = 3 V	40			ns
			V_{DD} = 5 V	40			
t_{d1}	Delay time	$\overline{CS}$ low to first data (0) out	V_{DD} = 3 V		15	25	ns
			V_{DD} = 5 V		13	25	
t_{su1}	Setup time	$\overline{CS}$ low to SCLK low	V_{DD} = 3 V	10			ns
			V_{DD} = 5 V	10			
t_{d2}	Delay time	SCLK falling to SDO	V_{DD} = 3 V		15	25	ns
			V_{DD} = 5 V		13	25	
t_{h1}	Hold time	SCLK falling to data valid (with 50-pF load)	V_{DD} < 3 V	7			ns
			V_{DD} > 5 V	5.5			
t_{d3}	Delay time	16th SCLK falling edge to SDO 3-state	V_{DD} = 3 V		10	25	ns
			V_{DD} = 5 V		8	20	
t_{w1}	Pulse duration	$\overline{CS}$	V_{DD} = 3 V	25	40		ns
			V_{DD} = 5 V	25	40		
t_{d4}	Delay time	$\overline{CS}$ high to SDO 3-state, see Figure 34	V_{DD} = 3 V		17	30	ns
			V_{DD} = 5 V		15	25	
t_{wH}	Pulse duration	SCLK high	V_{DD} = 3 V	0.4 × t_{SCLK}			ns
			V_{DD} = 5 V	0.4 × t_{SCLK}			
t_{wL}	Pulse duration	SCLK low	V_{DD} = 3 V	0.4 × t_{SCLK}			ns
			V_{DD} = 5 V	0.4 × t_{SCLK}			
	Frequency	SCLK	V_{DD} = 3 V			25	MHz
			V_{DD} = 5 V			25	
t_{d5}	Delay time	Second falling edge of clock and $\overline{CS}$ to enter in power down (use min spec not to accidently enter in power down, see Figure 35)	V_{DD} = 3 V	–2		5	ns
			V_{DD} = 5 V	–2		5	
t_{d6}	Delay time	$\overline{CS}$ and 10th falling edge of clock to enter in power down (use max spec not to accidently enter in power down, see Figure 35)	V_{DD} = 3 V	2		–5	ns
			V_{DD} = 5 V	2		–5	

(1) 3-V Specifications apply from 2.35 V to 3.6 V, and 5-V specifications apply from 4.75 V to 5.25 V.

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8.8 Typical Characteristics

8.8.1 ADS7887 and ADS7888

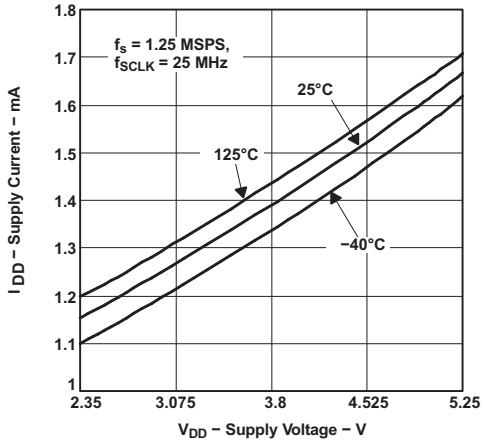


Figure 1. Supply Current vs Supply Voltage

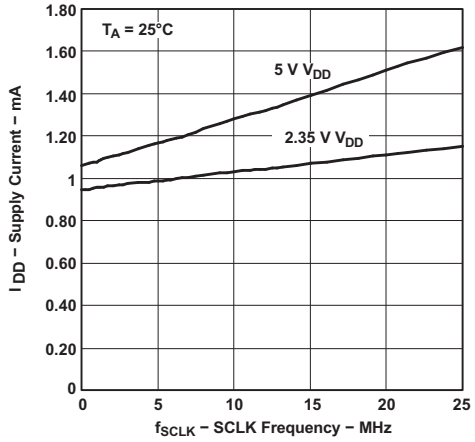


Figure 2. Supply Current vs SCLK Frequency

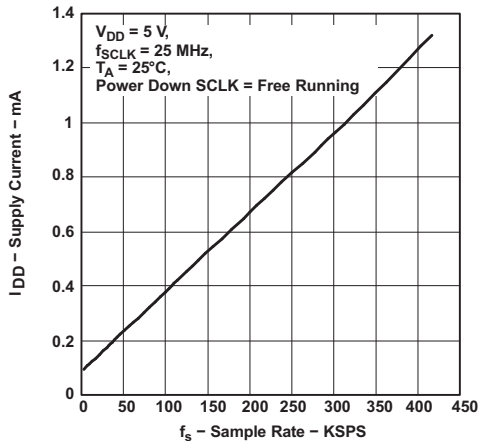


Figure 3. Supply Current vs Sample Rate

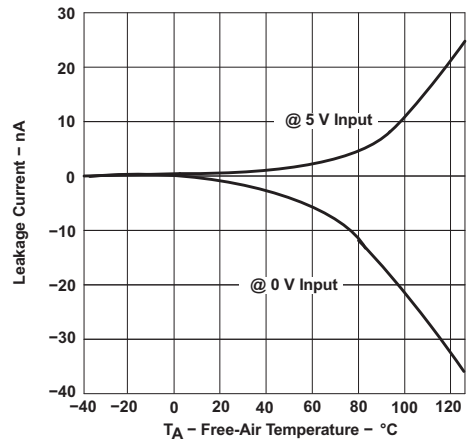


Figure 4. Analog Input Leakage Current vs Free-Air Temperature

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8.8.2 ADS7887 Only

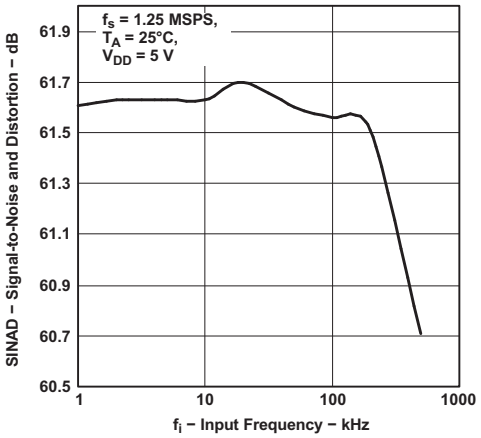


Figure 5. Signal-to-Noise and Distortion vs Input Frequency

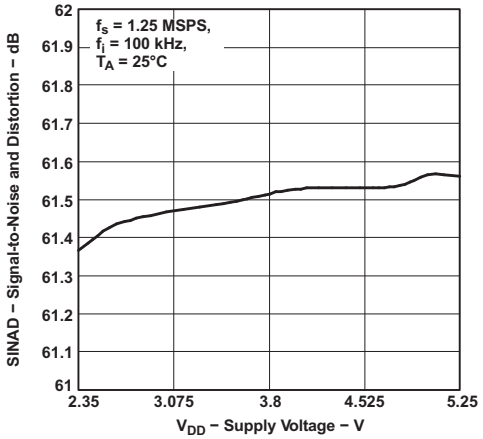


Figure 6. Signal-to-Noise and Distortion vs Supply Voltage

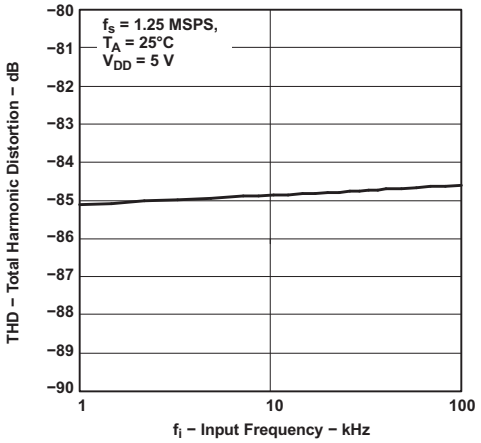


Figure 7. Total Harmonic Distortion vs Input Frequency

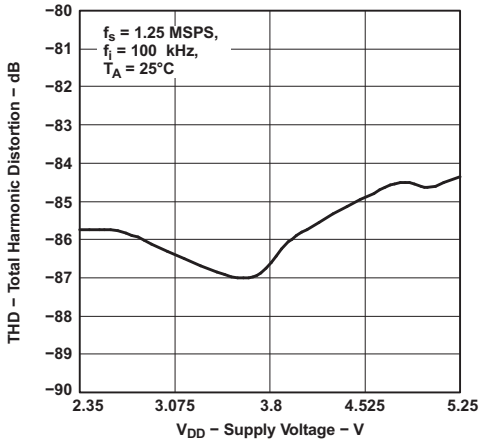


Figure 8. Total Harmonic Distortion vs Supply Voltage

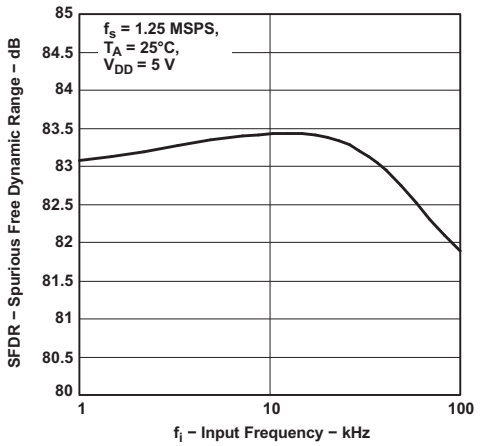


Figure 9. Spurious Free Dynamic Range vs Input Frequency

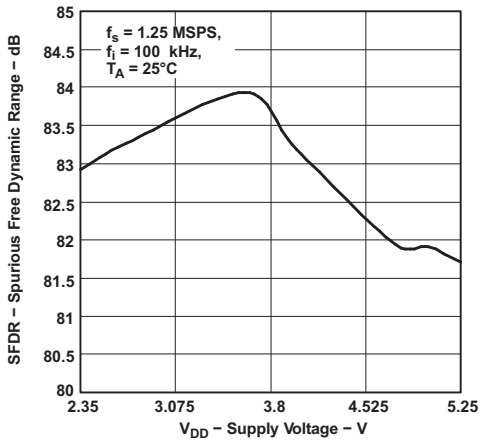


Figure 10. Spurious Free Dynamic Range vs Supply Voltage

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ADS7887 Only (continued)

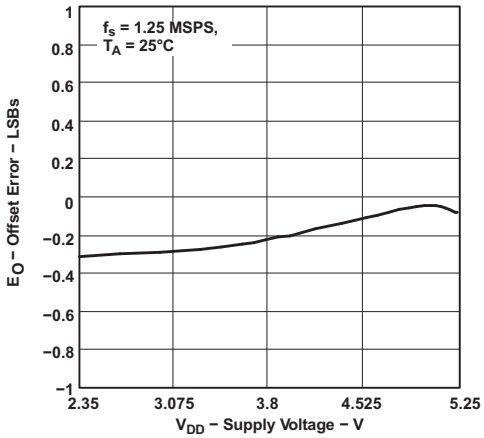


Figure 11. Offset Error vs Supply Voltage

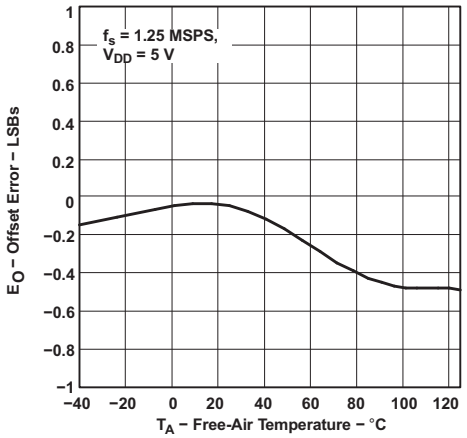


Figure 12. Offset Error vs Free-Air Temperature

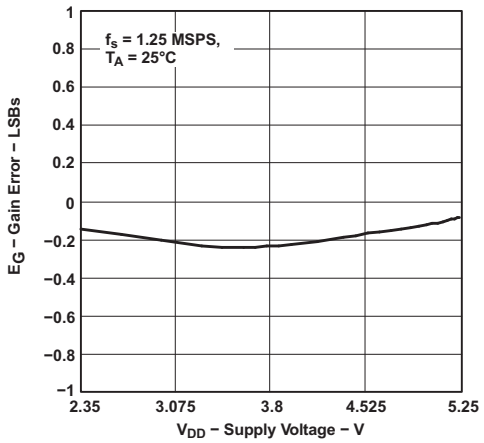


Figure 13. Gain Error vs Supply Voltage

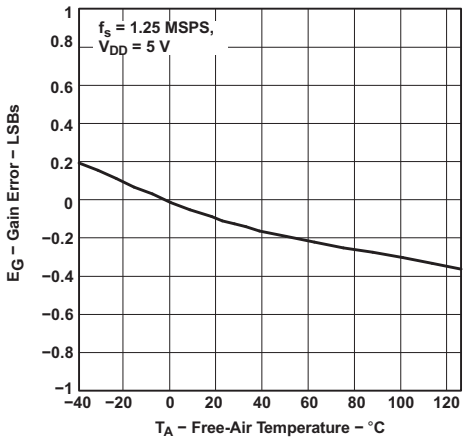


Figure 14. Gain Error vs Free-Air Temperature

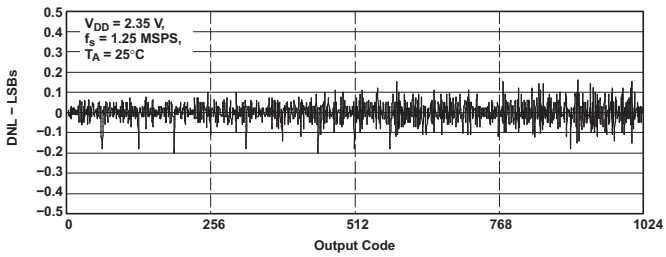


Figure 15. DNL

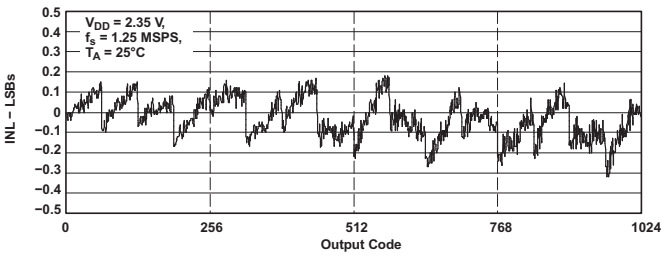


Figure 16. INL

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ADS7887 Only (continued)

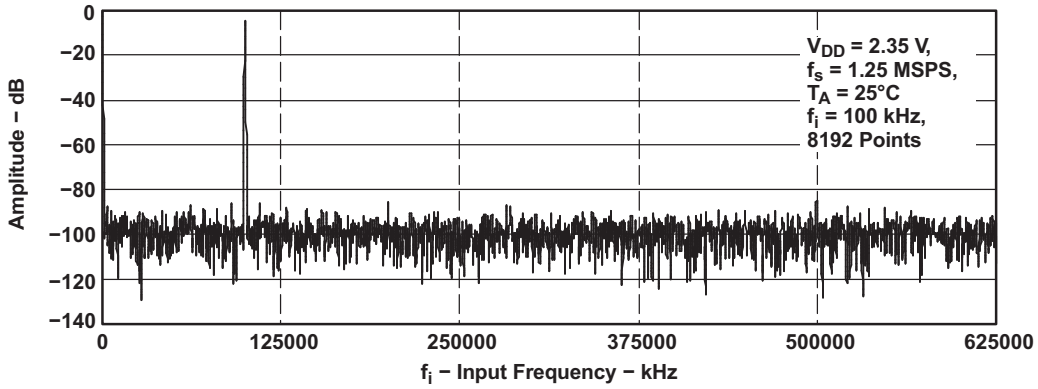


Figure 17. FFT

8.8.3 ADS7888 Only

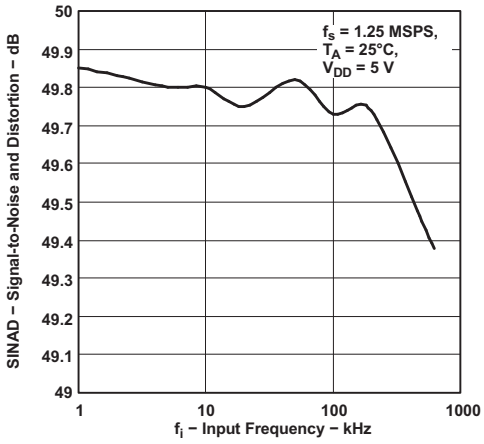


Figure 18. Signal-to-Noise and Distortion vs Input Frequency

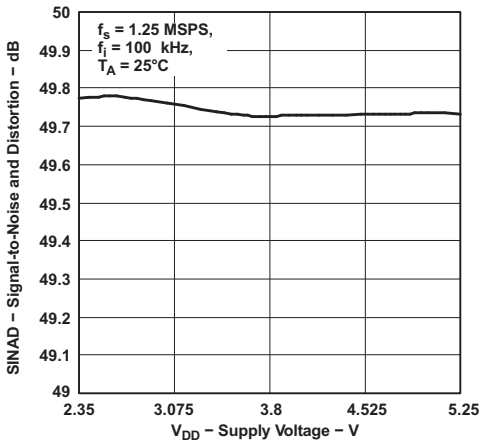


Figure 19. Signal-to-Noise and Distortion vs Supply Voltage

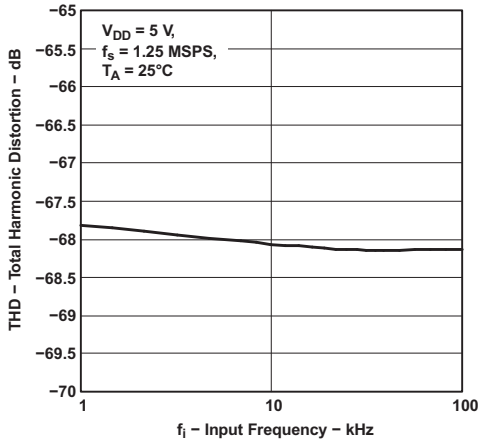


Figure 20. Total Harmonic Distortion vs Input Frequency

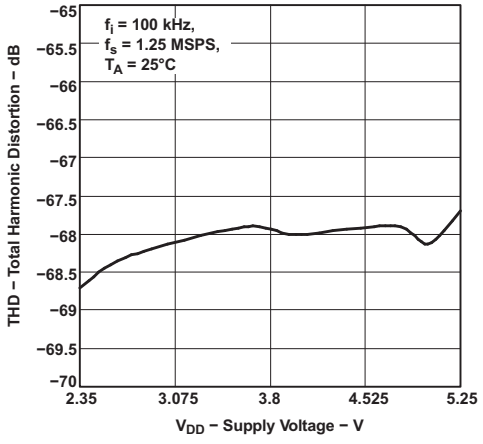


Figure 21. Total Harmonic Distortion vs Supply Voltage

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ADS7888 Only (continued)

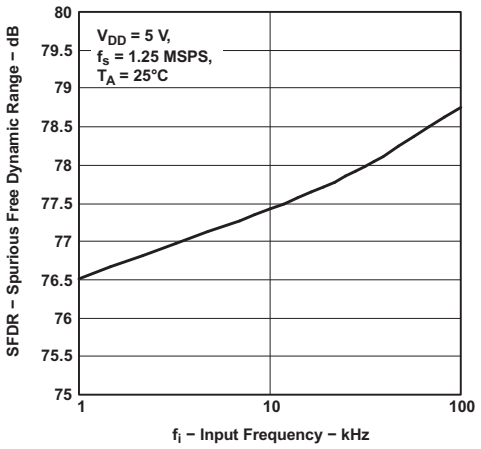


Figure 22. Spurious Free Dynamic Range vs Input Frequency

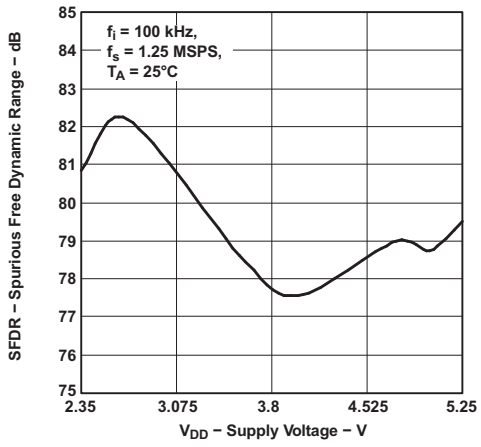


Figure 23. Spurious Free Dynamic Range vs Supply Voltage

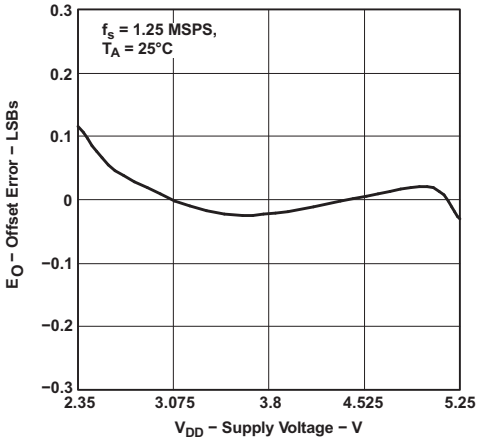


Figure 24. Offset Error vs Supply Voltage

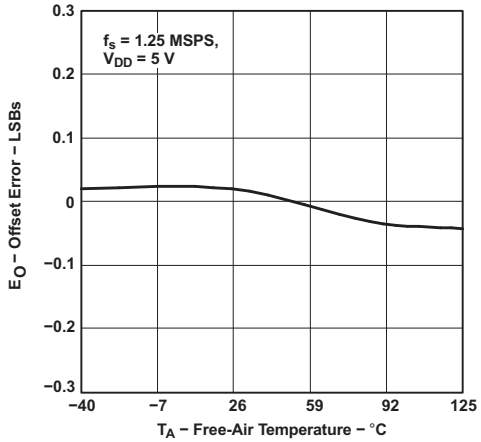


Figure 25. Offset Error vs Free-Air Temperature

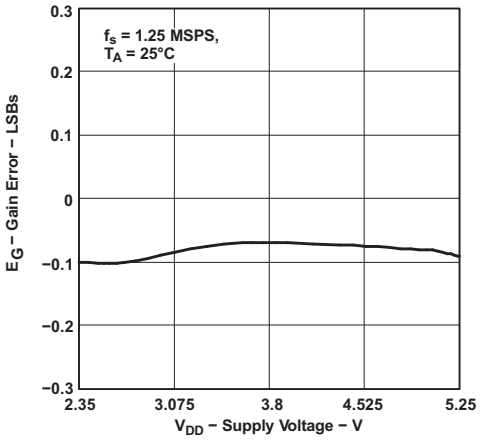


Figure 26. Gain Error vs Supply Voltage

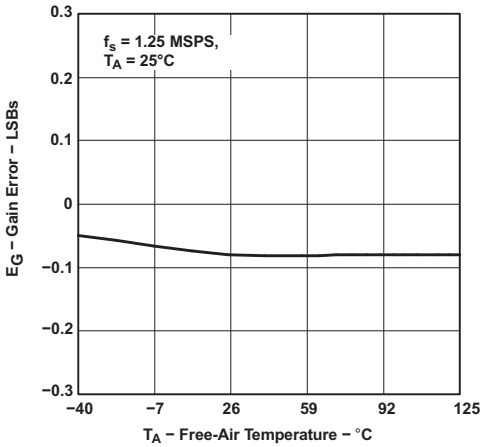


Figure 27. Gain Error vs Free-Air Temperature

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ADS7888 Only (continued)

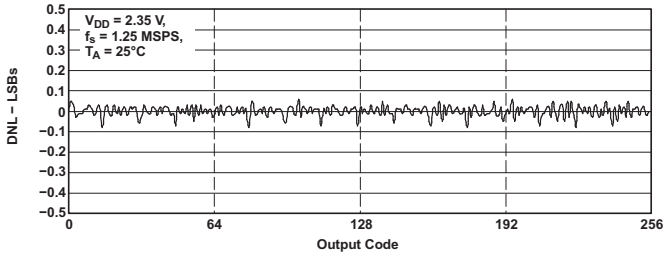


Figure 28. DNL

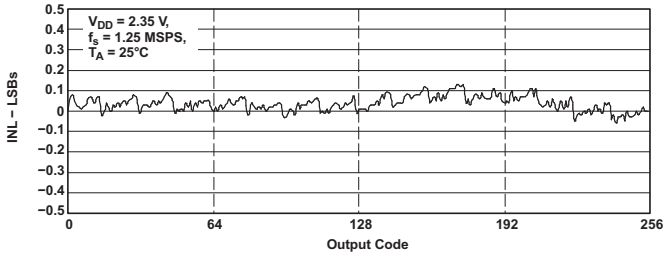


Figure 29. INL

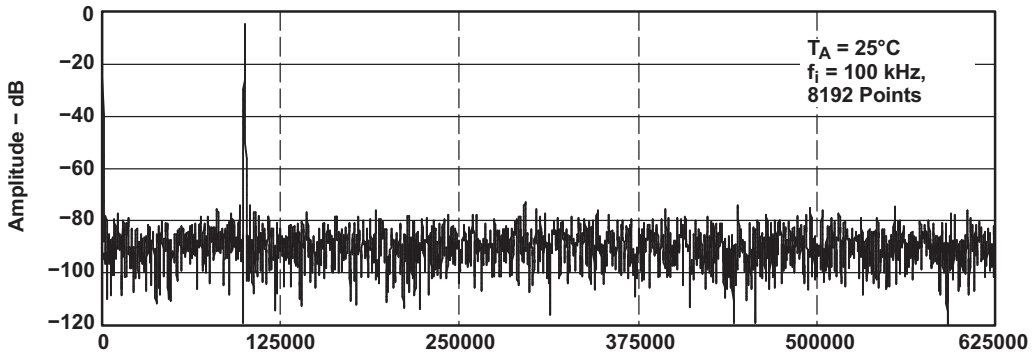


Figure 30. FFT

9 Detailed Description

9.1 Overview

The ADS788x devices are ADC converters. The serial interface in each device is controlled by the $\overline{CS}$ and SCLK signals for easy interface with microprocessors and DSPs. The input signal is sampled with the falling edge of $\overline{CS}$, and SCLK is used for conversion and serial data output. They both operate in a wide supply range from 2.35 V to 5.25 V and low power consumption makes them suitable for battery-powered applications.

9.1.1 Driving the VIN and V_{DD} Pins of the ADS7887 and ADS7888

The VIN input to the ADS7887 and ADS7888 must be driven with a low impedance source. In most cases additional buffers are not required. In cases where the source impedance exceeds 200 Ω, using a buffer would help achieve the rated performance of the converter. The THS4031 is a good choice for the driver amplifier buffer.

The reference voltage for the ADS7887 and ADS7888 A/D converters are derived from the supply voltage internally. The devices offer limited low-pass filtering functionality on-chip. The supply to these converters must be driven with a low impedance source and must be decoupled to the ground. A 1-µF storage capacitor and a 10-nF decoupling capacitor must be placed close to the device. Wide, low impedance traces must be used to connect the capacitor to the pins of the device. The ADS7887 and ADS7888 draw very little current from the supply lines. The supply line can be driven by either:

- Directly from the system supply.
- A reference output from a low drift and low dropout reference voltage generator like REF3030 or REF3130. The ADS7887 and ADS7888 can operate off a wide range of supply voltages. The actual choice of the reference voltage generator would depend upon the system. Figure 41 shows one possible application circuit.
- A low-pass filtered version of the system supply followed by a buffer like the zero-drift OPA735 can also be used in cases where the system power supply is noisy. Take care to ensure that the voltage at the V_{DD} input does not exceed 7 V (especially during power up) to avoid damage to the converter. This can be done easily using single-supply CMOS amplifiers like the OPA735. Figure 42 shows one possible application circuit.

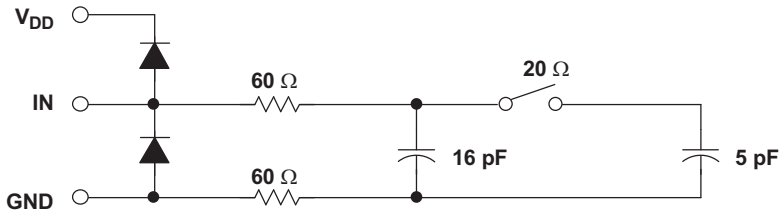
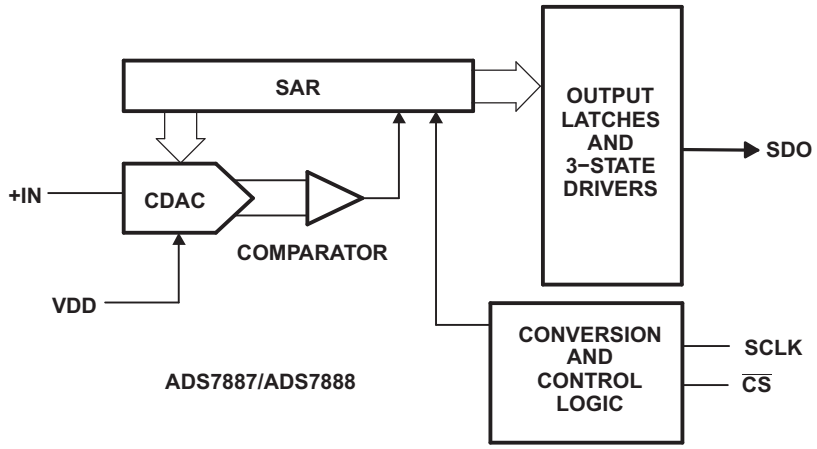


Figure 31. Typical Equivalent Sampling Circuit

9.2 Functional Block Diagram



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9.3 Feature Description

9.3.1 ADS7887 Operation

The cycle begins with the falling edge of $\overline{CS}$. This point is indicated as *a* in Figure 32. With the falling edge of $\overline{CS}$, the input signal is sampled and the conversion process is initiated. The device outputs data while the conversion is in progress. The data word contains 4 leading zeros, followed by 10-bit data in MSB first format and padded by 2 lagging zeros.

The falling edge of $\overline{CS}$ clocks out the first zero, and a zero is clocked out on every falling edge of the clock until the third edge. Data is in MSB first format with the MSB being clocked out on the 4th falling edge. Data is padded with two lagging zeros as shown in Figure 32. On the 16th falling edge of SCLK, SDO goes to the 3-state condition. The conversion ends on the 14th falling edge of SCLK. The device enters the acquisition phase on the first rising edge of SCLK after the 13th falling edge. This point is indicated by *b* in Figure 32.

$\overline{CS}$ can be asserted (pulled high) after 16 clocks have elapsed. It is necessary not to start the next conversion by pulling $\overline{CS}$ low until the end of the quiet time (t_q) after SDO goes to 3-state. To continue normal operation, it is necessary that $\overline{CS}$ is not pulled high until point *b*. Without this, the device does not enter the acquisition phase and no valid data is available in the next cycle (refer to *Power-Down Mode* for more details). $\overline{CS}$ going high any time after the conversion start aborts the ongoing conversion and SDO goes to 3-state.

The high level of the digital input to the device is not limited to device V_{DD}. This means the digital input can go as high as 5.25 V when the device supply is 2.35 V. This feature is useful when digital signals are coming from another circuit with different supply levels. Also, this relaxes the restriction on power-up sequencing. However, the digital output levels (V_{OH} and V_{OL}) are governed by V_{DD} as listed in *Specifications*.

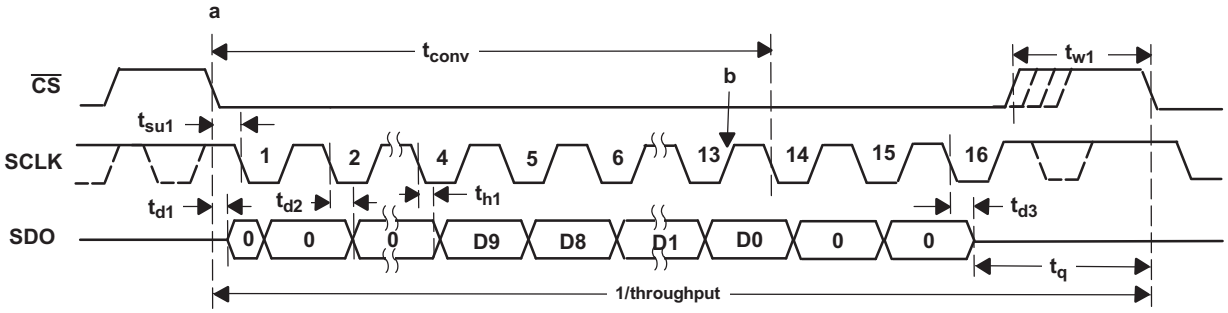


Figure 32. ADS7887 Interface Timing Diagram

9.3.2 ADS7888 Operation

The cycle begins with the falling edge of $\overline{CS}$. This point is indicated as *a* in Figure 33. With the falling edge of $\overline{CS}$, the input signal is sampled and the conversion process is initiated. The device outputs data while the conversion is in progress. The data word contains 4 leading zeros, followed by 8-bit data in MSB first format and padded by 4 lagging zeros.

The falling edge of $\overline{CS}$ clocks out the first zero, and a zero is clocked out on every falling edge of the clock until the third edge. Data is in MSB first format with the MSB being clocked out on the 4th falling edge. Data is padded with four lagging zeros as shown in Figure 33. On the 16th falling edge of SCLK, SDO goes to the 3-state condition. The conversion ends on the 12th falling edge of SCLK. The device enters the acquisition phase on the first rising edge of SCLK after the 11th falling edge. This point is indicated by *b* in Figure 33.

$\overline{CS}$ can be asserted (pulled high) after 16 clocks have elapsed. It is necessary not to start the next conversion by pulling $\overline{CS}$ low until the end of the quiet time (t_q) after SDO goes to 3-state. To continue normal operation, it is necessary that $\overline{CS}$ is not pulled high until point *b*. Without this, the device does not enter the acquisition phase and no valid data is available in the next cycle (refer to *Power-Down Mode* for more details). $\overline{CS}$ going high any time after the conversion start aborts the ongoing conversion and SDO goes to 3-state.

The high level of the digital input to the device is not limited to device V_{DD}. This means the digital input can go as high as 5.25 V when the device supply is 2.35 V. This feature is useful when digital signals are coming from another circuit with different supply levels. Also, this relaxes the restriction on power-up sequencing. However, the digital output levels (V_{OH} and V_{OL}) are governed by V_{DD} as listed in *Specifications*.

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Feature Description (continued)

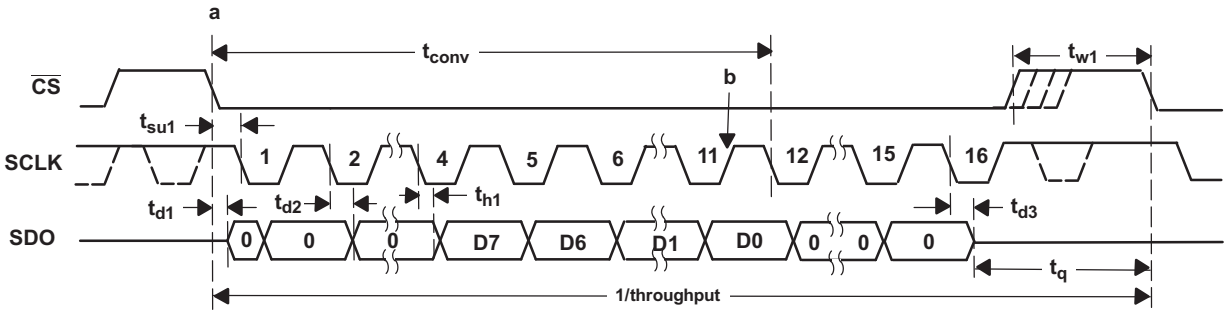


Figure 33. ADS7888 Interface Timing Diagram

As shown in Figure 34, the ADS7888 can achieve 1.5-MSPS throughput. $\overline{CS}$ can be pulled high after the 12th falling edge (with a 25-MHz SCLK). SDO goes to 3-state after the LSB (as $\overline{CS}$ is high). $\overline{CS}$ can be pulled low at the end of the quiet time (t_q) after SDO goes to 3-state.

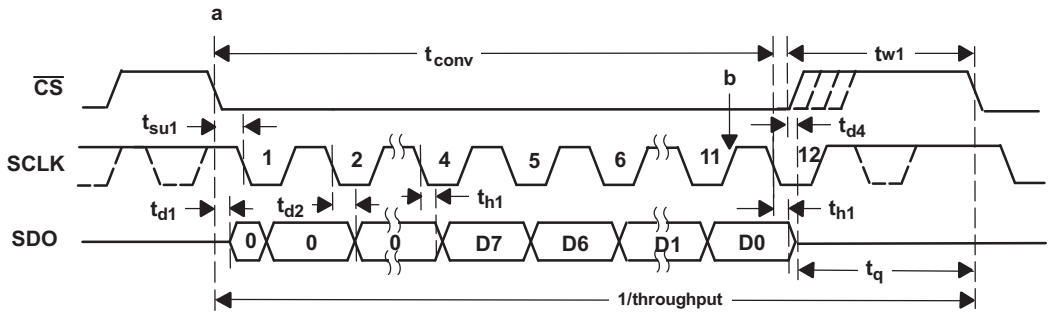


Figure 34. ADS7888 Interface Timing Diagram, Data Transfer With 12-Clock Frame

9.4 Device Functional Modes

9.4.1 Power-Down Mode

The device enters power-down mode if $\overline{CS}$ goes high anytime after the 2nd SCLK falling edge to before the 10th SCLK falling edge. Ongoing conversion stops and SDO goes to 3-state under this power-down condition as shown in Figure 35.

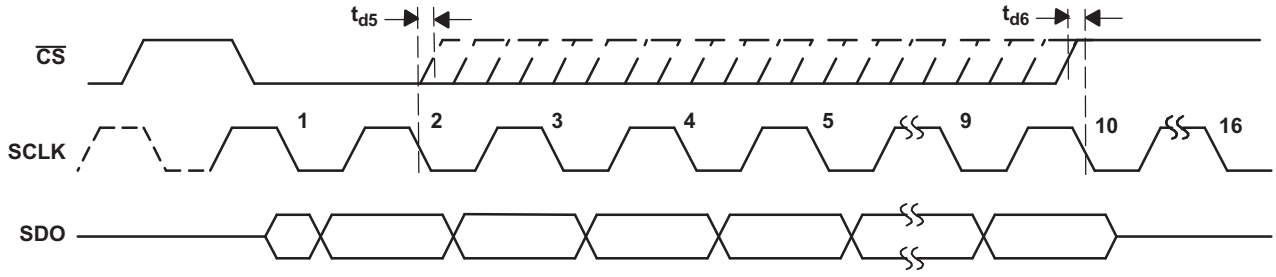


Figure 35. Entering Power-Down Mode

A dummy cycle with $\overline{CS}$ low for more than 10 SCLK falling edges brings the device out of power-down mode. For the device to come to the fully powered-up condition it takes 0.8 µs. $\overline{CS}$ can be pulled high any time after the 10th falling edge as shown in Figure 36. It is not necessary to continue until the 16th clock if the next conversion starts 0.8 µs after $\overline{CS}$ going low of the dummy cycle and the quiet time (t_q) condition is met.

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Device Functional Modes (continued)

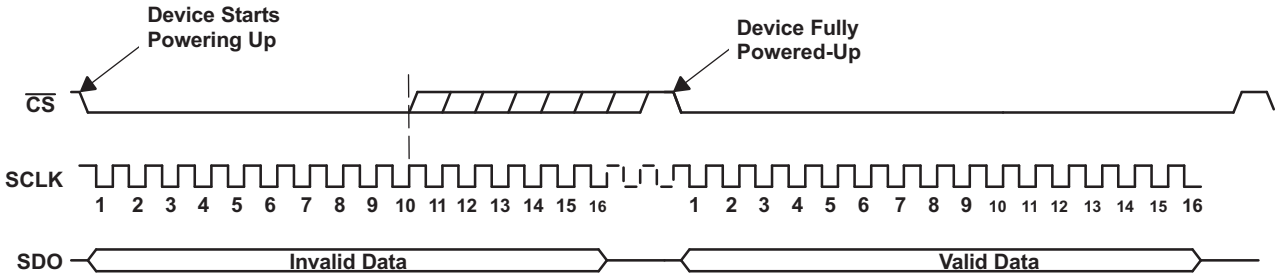


Figure 36. Exiting Power-Down Mode

10 Application and Implementation

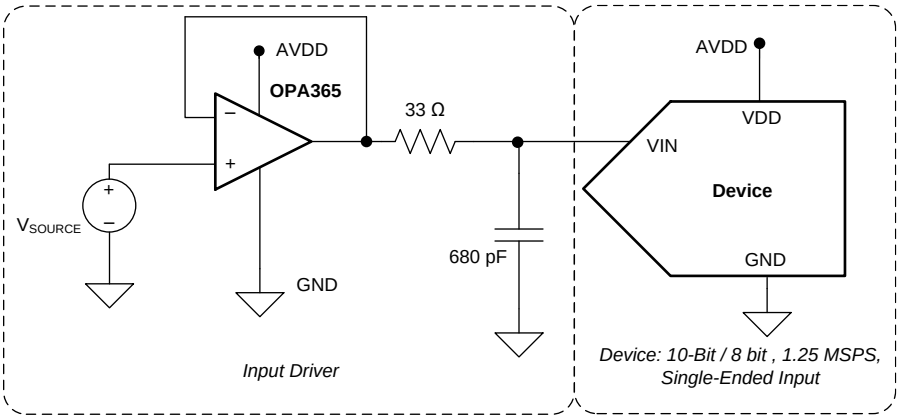
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The primary circuits required to maximize the performance of a high-precision, the successive approximation register (SAR) and analog-to-digital converter (ADC), are the input driver and the reference driver circuits. This section details some general principles for designing the input driver circuit, references the driver circuit, and provides some application circuits designed for the ADS7887 and ADS7888.

10.2 Typical Application



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Figure 37. Typical Data Acquisition (DAQ) Circuit: Single-Supply DAQ

10.2.1 Design Requirements

The goal of this application is to design a single-supply digital acquisition (DAQ) circuit based on the ADS7887 with SNR greater than 61 dB and THD less than –84 dB for input frequencies of 2 kHz to 100 kHz at a throughput of 1.25 MSPS.

10.2.2 Detailed Design Procedure

To achieve a SINAD of 61 dB, the operational amplifier must have high bandwidth to settle the input signal within the acquisition time of the ADC. The operational amplifier must have low noise to keep the total system noise below 20% of the input-referred noise of the ADC. For the application circuit shown in Figure 37, OPA365 is selected for its high bandwidth (50 MHz) and low noise (4.5 nV/√Hz).

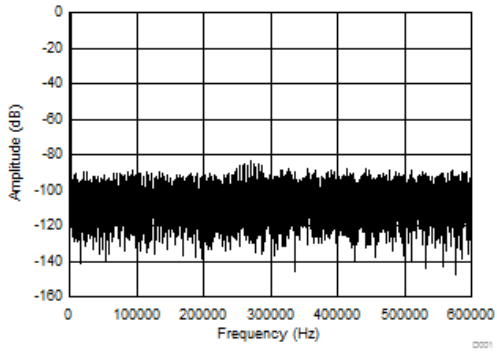
The reference voltage for the ADS7887 and ADS7888 A/D converters are derived from the supply voltage internally. The supply to these converters must be driven with a low impedance source and must be decoupled to the ground. To drive supply pin of ADS7887 ultra low noise fast transient response low dropout voltage regulator TPS73201 is selected. Alternatively one can drive supply pin with low impedance voltage reference similar to REF3030.

For a step-by-step design procedure for low power, small form factor digital acquisition (DAQ) circuit based on similar SAR ADCs refer to TI Precision Design, *Three 12-Bit Data Acquisition Reference Designs Optimized for Low Power and Ultra-Small Form Factor*.

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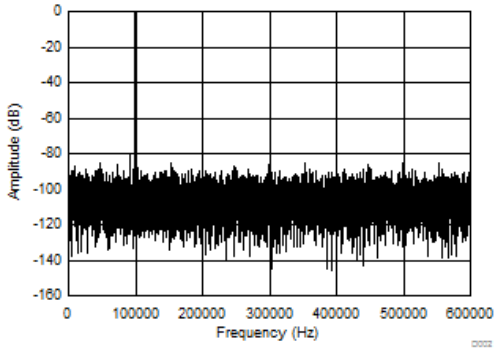
Typical Application (continued)

10.2.3 Application Curves



SNR: 61.9 dB THD: –86.8 dB SINAD: 61.3 dB

Figure 38. Test Results for the ADS7887 and OPA365 for a 2-kHz Input



SNR: 61.8 dB THD: –85.1 dB SINAD: 61.5 dB

Figure 39. Test Results for the ADS7887 and OPA365 for a 100-kHz Input

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11 Power Supply Recommendations

The reference voltage for the ADS7887 and ADS7888 A/D converters are derived from the supply voltage internally. The supply to these converters must be driven with a low impedance source and must be decoupled to the ground Decouple the V_{DD} with 1-µF ceramic decoupling capacitors, as shown in Figure 40. Always set the V_{DD} supply to be greater than or equal to the maximum input signal to avoid saturation of codes.

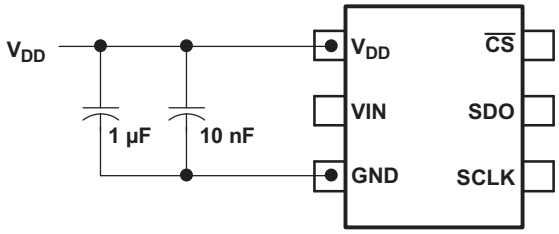


Figure 40. Supply and Reference Decoupling Capacitors

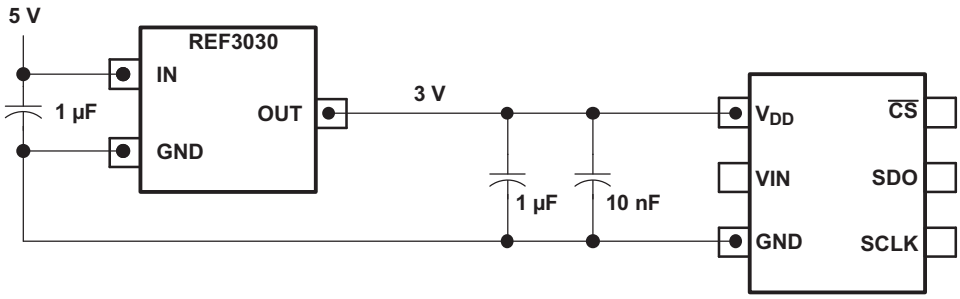


Figure 41. Using the REF3030 Reference

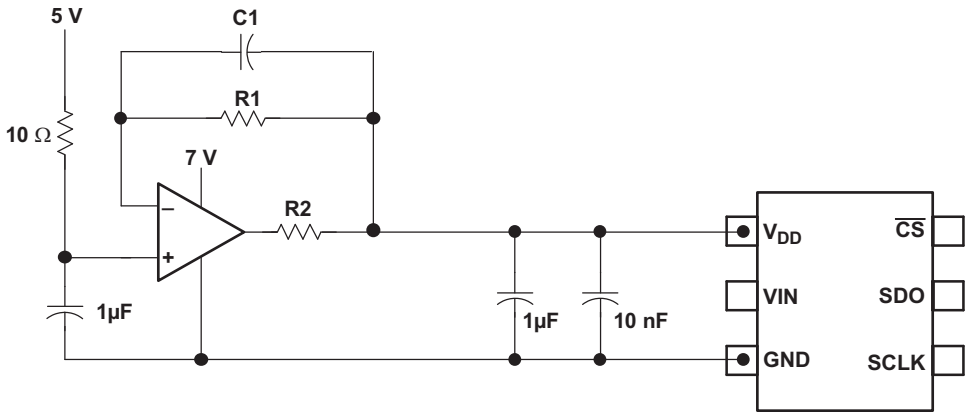


Figure 42. Buffering With the OPA735

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12 Layout

12.1 Layout Guidelines

Figure 43 shows a board layout example for the ADS7887 and ADS7888. Some of the key considerations are:

1. Use a ground plane underneath the device and partition the PCB into analog and digital sections.
2. Avoid crossing digital lines with the analog signal path.
3. The power sources to the device must be clean and well-bypassed. Use 1-µF ceramic bypass capacitors in close proximity to the supply pin (VDD).
4. Avoid placing vias between the VDD and bypass capacitors.
5. Connect ground pin to the ground plane using short, low-impedance path.
6. The fly-wheel RC filters are placed close to the device.

Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance precision. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.

12.2 Layout Example

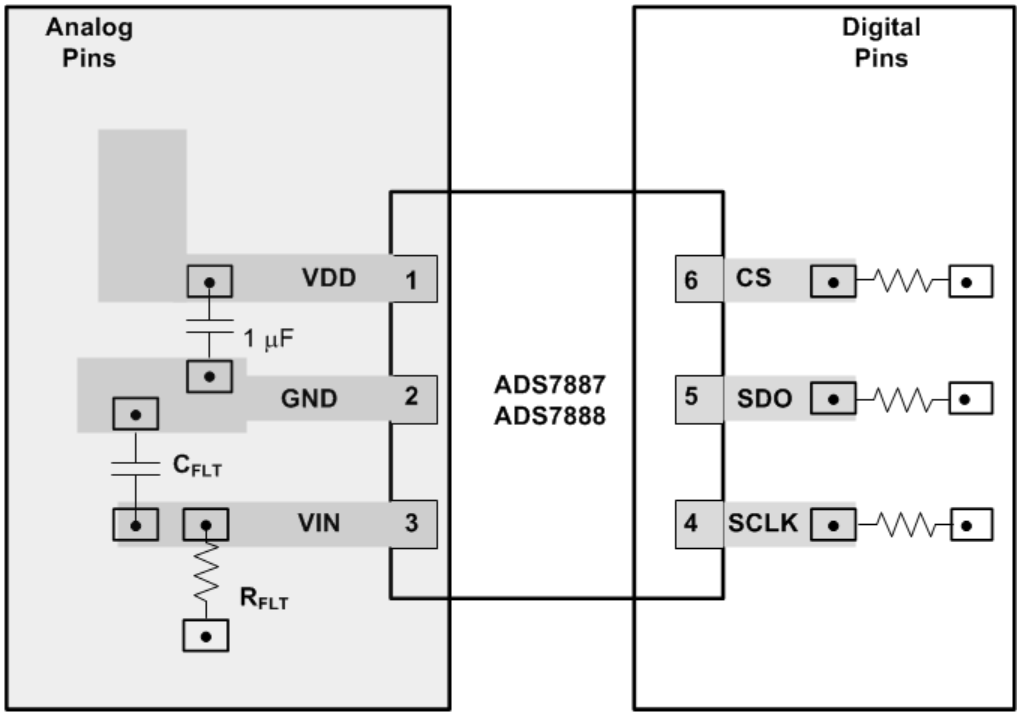


Figure 43. ADS7887 and ADS7888 Example Layout

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- *50MHz, Low-Distortion, High CMRR, RRI/O, Single-Supply Operational Amplifier* (SBOS365)
- *Cap-Free NMOS 250-mA Low Dropout Regulator With Reverse Current Protection* (SGLS346)
- *Three 12-Bit Data Acquisition Reference Designs Optimized for Low Power and Ultra-Small Form Factor* (TIDU390)

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ADS7887	Click here	Click here	Click here	Click here	Click here
ADS7888	Click here	Click here	Click here	Click here	Click here

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS7887SDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BAWQ
ADS7887SDBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BAWQ
ADS7887SDBVT	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BAWQ
ADS7887SDBVT.A	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BAWQ
ADS7887SDCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BNI
ADS7887SDCKR.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BNI
ADS7887SDCKT	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BNI
ADS7887SDCKT.A	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BNI
ADS7888SDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BAZQ
ADS7888SDBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BAZQ
ADS7888SDBVT	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BAZQ
ADS7888SDBVT.A	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BAZQ
ADS7888SDCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BNH
ADS7888SDCKR.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BNH
ADS7888SDCKT	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BNH
ADS7888SDCKT.A	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	BNH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

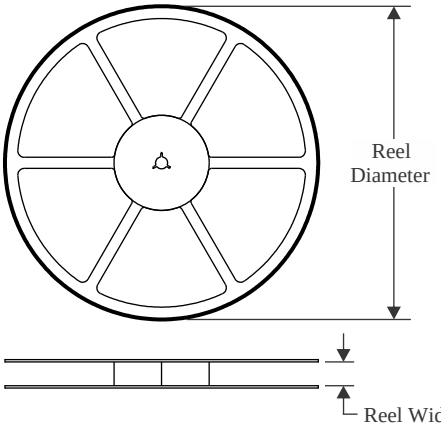
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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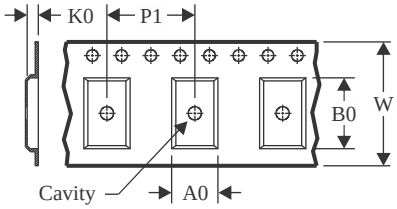
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

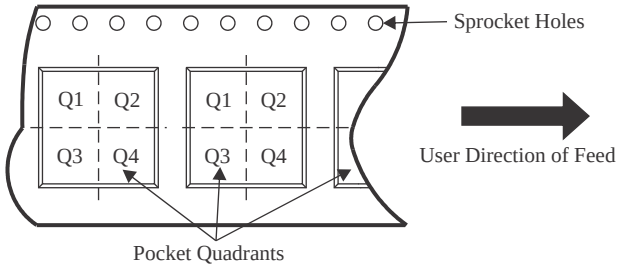


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

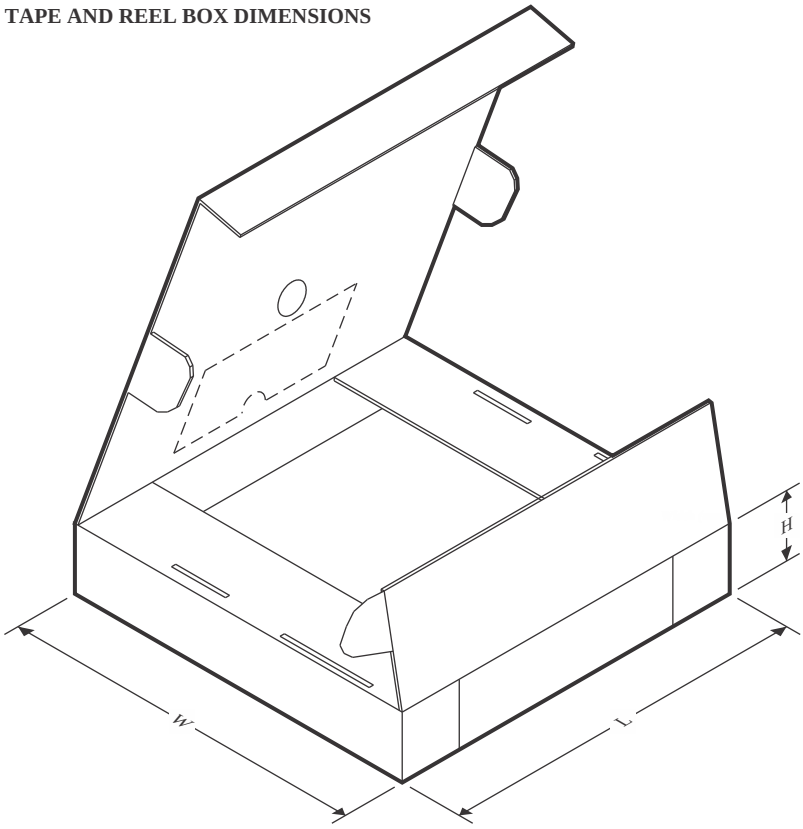
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7887SDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADS7887SDBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADS7887SDCKR	SC70	DCK	6	3000	180.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
ADS7887SDCKT	SC70	DCK	6	250	180.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
ADS7888SDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADS7888SDBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADS7888SDCKR	SC70	DCK	6	3000	180.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
ADS7888SDCKT	SC70	DCK	6	250	180.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

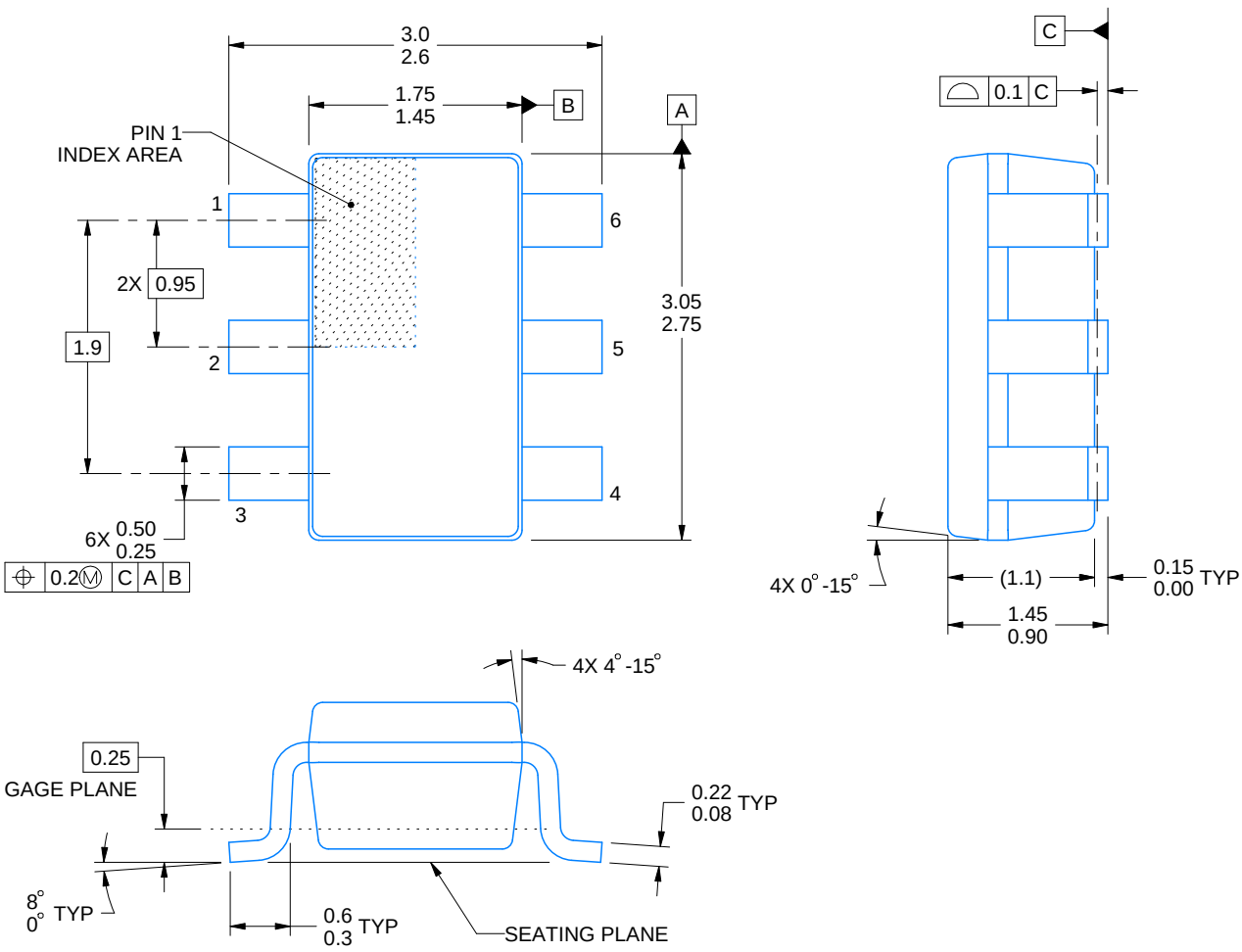
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7887SDBVR	SOT-23	DBV	6	3000	213.0	191.0	35.0
ADS7887SDBVT	SOT-23	DBV	6	250	213.0	191.0	35.0
ADS7887SDCKR	SC70	DCK	6	3000	213.0	191.0	35.0
ADS7887SDCKT	SC70	DCK	6	250	213.0	191.0	35.0
ADS7888SDBVR	SOT-23	DBV	6	3000	213.0	191.0	35.0
ADS7888SDBVT	SOT-23	DBV	6	250	213.0	191.0	35.0
ADS7888SDCKR	SC70	DCK	6	3000	213.0	191.0	35.0
ADS7888SDCKT	SC70	DCK	6	250	213.0	191.0	35.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

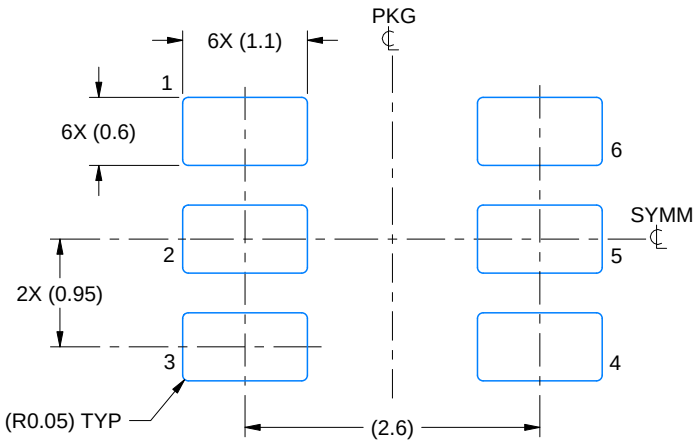
SMALL OUTLINE TRANSISTOR



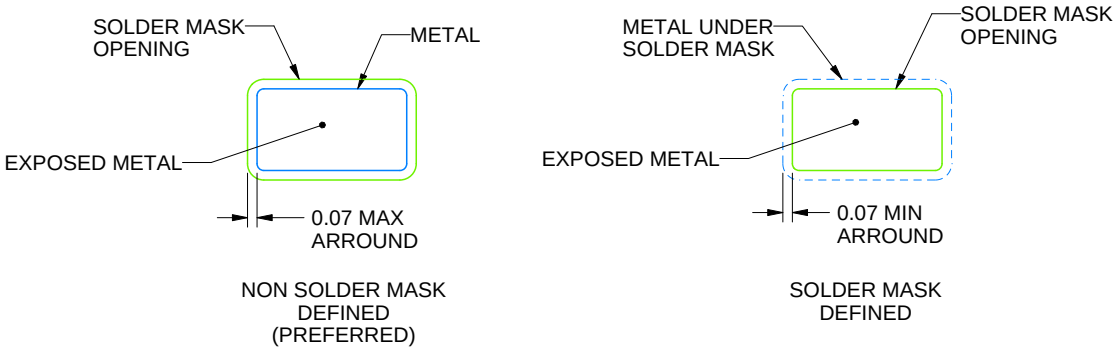
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

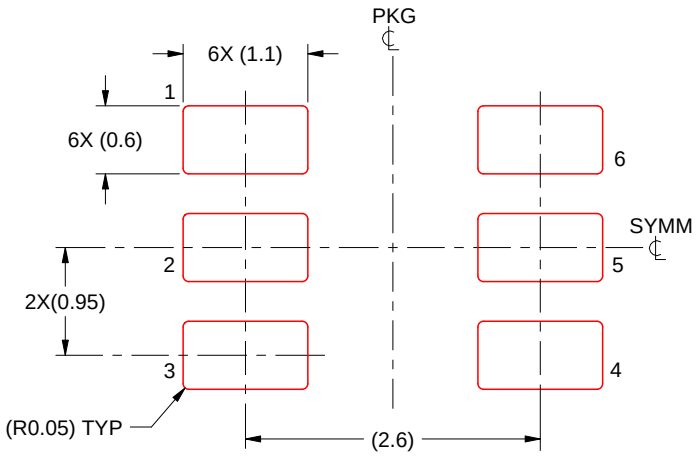


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

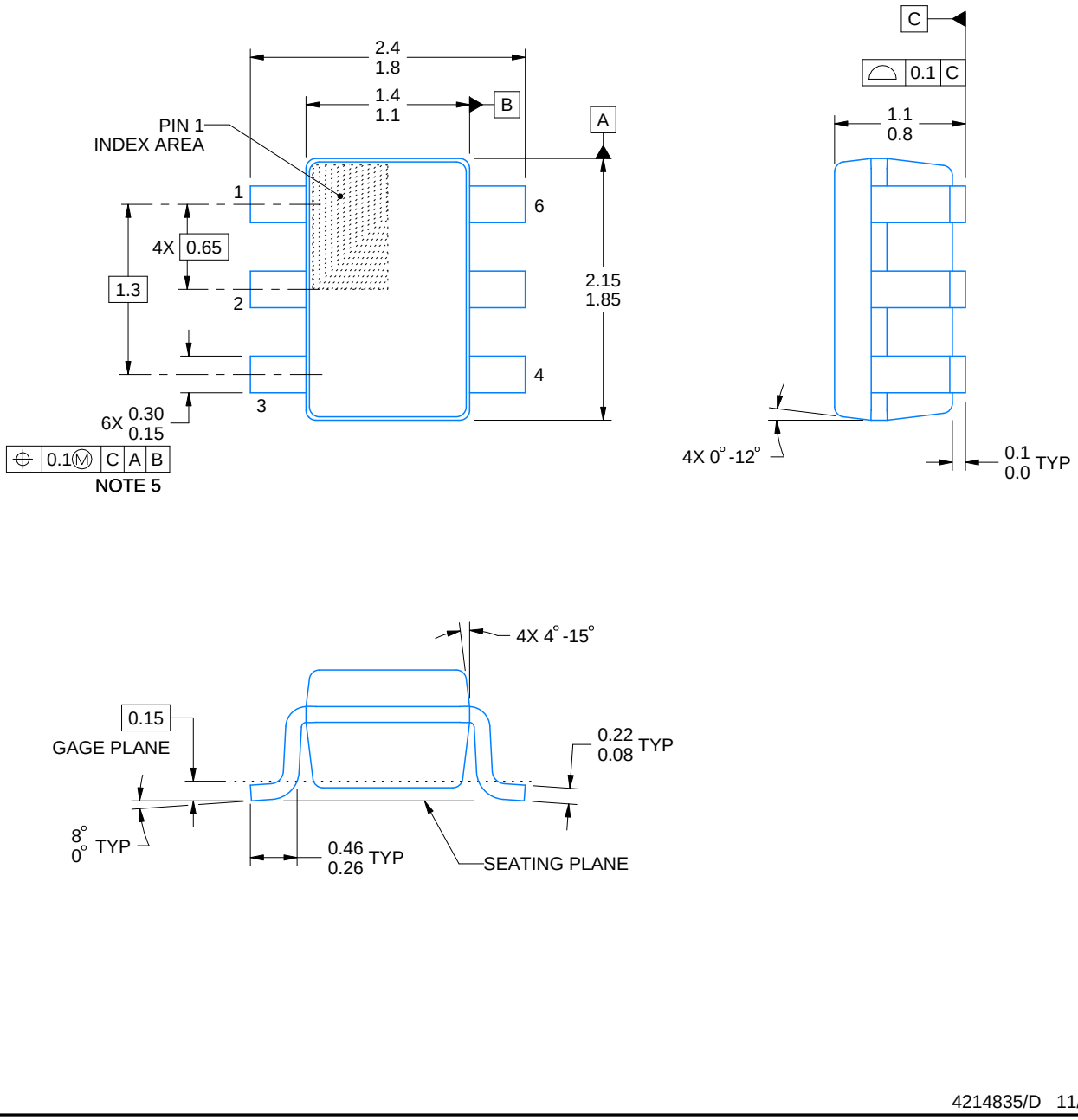
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

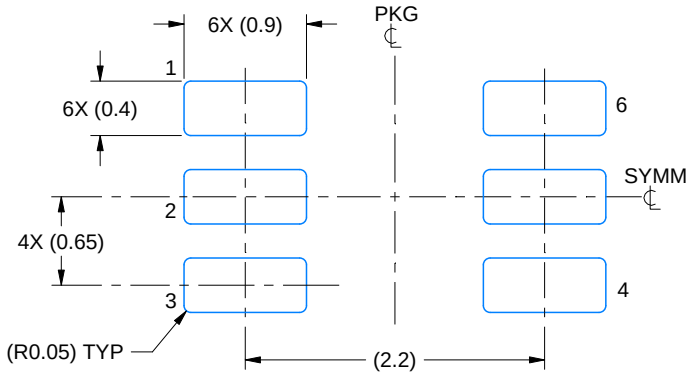
SMALL OUTLINE TRANSISTOR



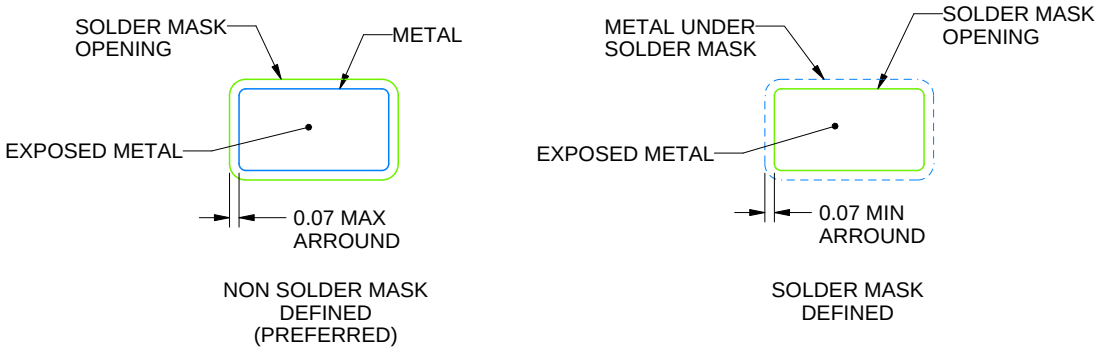
4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

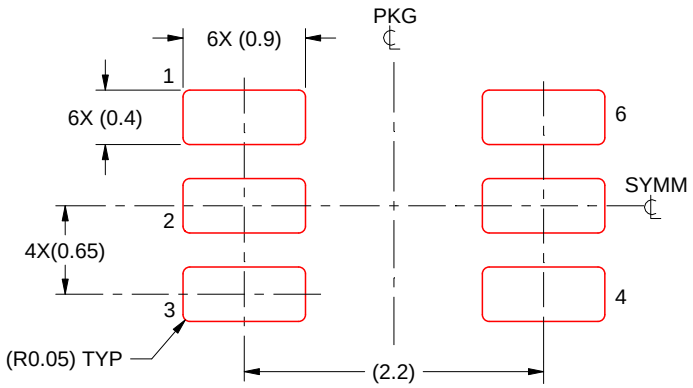


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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