ADS892xB 16-Bit, High-Speed SAR ADCs With Integrated Reference Buffer, and Enhanced Performance Features

1 Features

- Resolution: 16-Bits
- High Sample Rate With No Latency Output:
  - ADS8920B: 1MSPS
  - ADS8922B: 500kSPS
  - ADS8924B: 250kSPS
- Integrated LDO Enables Low-Power, Single-Supply Operation
- Low-Power Reference Buffer With No Droop
- Excellent AC and DC Performance:
  - SNR: 96.8dB, THD: –125dB
  - INL: ±0.25LSB
  - DNL: ±0.2LSB, 16-Bit No-Missing-Codes
- Wide Input Range:
  - Unipolar DifferentialInput Range: $\pm V_{REF}$
  - V_{REF} Input Range: 2.5V to 5V
- Enhanced-SPI Digital Interface
  - Interface SCLK: 18MHz at 1MSPS
  - Configurable Data Parity Output
- Extended Temperature Range: –40°C to +125°C
- Small Footprint: 4mm × 4mm VQFN

2 Applications

- Precision multifunction input & output DAQ
- Parametric measurement unit (PMU)
- AC analog input module

3 Description

The ADS8920B, ADS8922B, and ADS8924B (ADS892xB) belong to a family of pin-to-pin compatible, high-speed, single-channel, high-precision, 16-bit successive approximation register (SAR) based analog-to-digital convertors (ADCs) with an integrated reference buffer and integrated low-dropout regulator (LDO). The device family includes the ADS890xB (20-bit) and ADS891xB (18-bit) resolution variants.

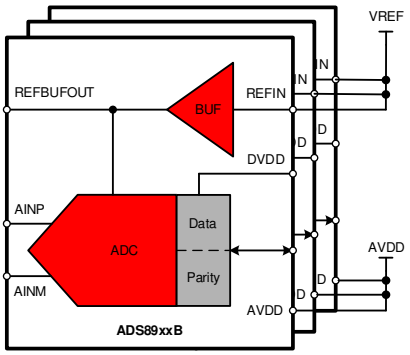
The ADS892xB boost analog performance while maintaining high-resolution data transfer by using TI's enhanced-SPI feature. Enhanced-SPI enables the ADS89xxB to achieve high throughput at lower clock speeds, thereby simplifying the board layout and lowering system cost. Enhanced-SPI also simplifies clocking-in of data, thereby making this device an excellent choice for applications involving FPGAs, DSPs. The ADS89xxB is compatible with a standard SPI.

Table 3-1. Package Information

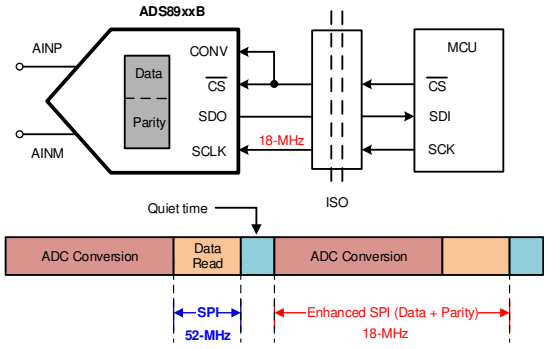
DEVICE	PACKAGE(1)	PACKAGE SIZE(2)
ADS8920B ADS8922B ADS8924B	RGE (VQFN, 24)	4mm × 4mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Multi-ADC System with Single Supply and Reference



Lowest Clock Speeds at 1-MSPS using 3-Wire Enhanced-SPI



Ease of System Design With ADS89xxB Integrated Features

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

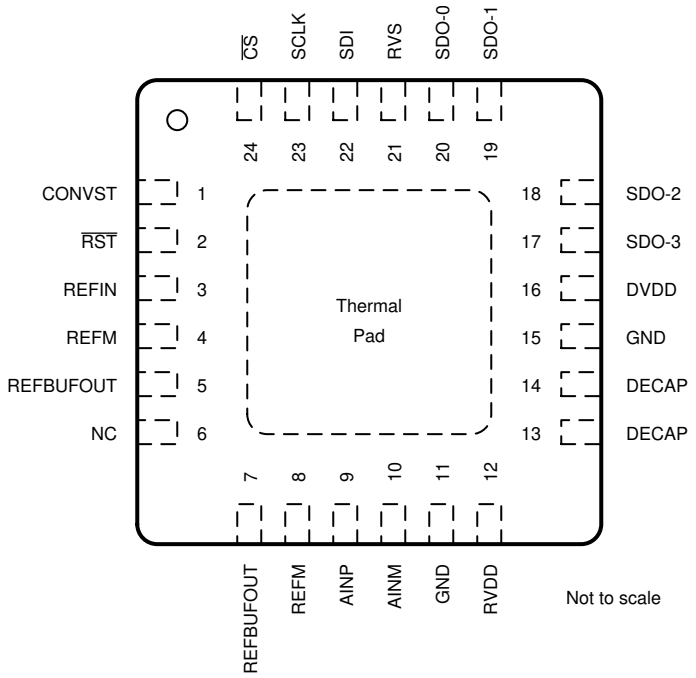


Figure 4-1. RGE Package 24-Pin VQFN Top View

Table 4-1. Pin Functions

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
AINM	10	Analog input	Negative analog input
AINP	9	Analog input	Positive analog input
$\overline{CS}$	24	Digital input	Chip-select input pin; active low The device takes control of the data bus when $\overline{CS}$ is low. The SDO-x pins go to Hi-Z when $\overline{CS}$ is high.
CONVST	1	Digital input	Conversion start input pin. A CONVST rising edge brings the device from ACQ state to CNV state.
DECAP	13, 14	Power supply	Place decoupling capacitor here for internal power supply. Short pin 13 and 14 together.
DVDD	16	Power supply	Interface power supply pin
GND	11, 15	Power supply	Ground
NC	6	No connection	Float these pins; no external connection.
REFBUFOUT	5, 7	Analog input/output	Internal reference buffer output, external reference input. Short pin 5 and 7 together.
REFIN	3	Analog input	Reference voltage input
REFM	4, 8	Analog input	Reference ground potential
$\overline{RST}$	2	Digital input	Asynchronous reset input pin. A low pulse on the $\overline{RST}$ pin resets the device. All register bits return to the default state.
RVDD	12	Power supply	Analog power supply pin.
RVS	21	Digital output	Multifunction output pin. With $\overline{CS}$ held high, RVS reflects the status of the internal ADCST signal. With $\overline{CS}$ low, the status of RVS depends on the output protocol selection.
SCLK	23	Digital input	Clock input pin for the serial interface. All system-synchronous data transfer protocols are timed with respect to the SCLK signal.
SDI	22	Digital input	Serial data input pin. This pin is used to feed data or commands into the device.
SDO-0	20	Digital output	Serial communication pin: data output 0

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Table 4-1. Pin Functions (continued)

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
SDO-1	19	Digital output	Serial communication pin: data output 1
SDO-2	18	Digital output	Serial communication pin: data output 2
SDO-3	17	Digital output	Serial communication pin: data output 3
Thermal pad		Supply	Exposed thermal pad; connect to GND.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
RVDD to GND	–0.3	7	V
DVDD to GND	–0.3	7	V
REFIN to REFM	–0.3	RV_{DD} + 0.3	V
REFM to GND	–0.1	0.1	V
Analog Input (AINP, AINM) to GND	–0.3	V_{REF} + 0.3	V
Digital input ($\overline{RST}$, CONVST, $\overline{CS}$, SCLK, SDI) to GND	–0.3	DV_{DD} + 0.3	V
Digital output (RVS, SDO-0, SDO-1, SDO-2, SDO-3) to GND	–0.3	DV_{DD} + 0.3	V
Analog Input (AINP, AINM) to RVDD and GND	–130	130	mA
Operating free-air temperature, T_A	–40	125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22C101(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
RV_{DD}	Analog supply voltage (RVDD to AGND)		3	5	5.5	V
DV_{DD}	Digital supply voltage (DVDD to AGND)	Operating	1.65	3	5.5	V
		Specified throughput	2.35	3	5.5	
V_{REF}	Reference input voltage on REFIN		2.5		RV_{DD} – 0.3	V
C_{REFBUF}	External ceramic decoupling capacitor		10			µF
R_{ESR}	External series resistor		0		1.3	Ω
T_A	Specified free-air operating temperature		–40	25	125	°C

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5.4 Thermal Information

THERMAL METRIC[1]		ADS892xB RGE (VQFN) 24 PINS	UNITS
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

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5.5 Electrical Characteristics

At RV_{DD} = 5.5V, DV_{DD} = 1.65V to 5.5V, V_{REF} = 5V, and maximum throughput (unless otherwise noted). Minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
FSR	Full-scale input range (AINP – AINM)		$-V_{REF}$		V_{REF}	V
V_{IN}	Absolute input voltage (AINP and AINM to REFM)		0		V_{REF}	V
V_{CM}	Common-mode voltage (AINP + AINM) / 2		(V_{REF} / 2) – 0.1	V_{REF} / 2	(V_{REF} / 2) + 0.1	V
C_{IN}	Input capacitance	Sample mode		60		pF
		Hold mode		4		pF
VOLTAGE REFERENCE INPUT (REFIN)						
I_{REF}	Reference input current	V_{REF} = 5V		0.1	1	µA
C_{REF}	Internal capacitance			10		pF
REFERENCE BUFFER OUTPUT (REFBUFOUT)						
$V_{(RO)}$	Reference buffer offset voltage ($V_{REFBUFOUT} – V_{REF}$)	With EN_MARG = 0b(1), T_A = 25°C(5)	–250		250	µV
C_{REFBUF}	External ceramic decoupling capacitor		10			µF
R_{ESR}	External series resistor		0		1.3	Ω
I_{SHRT}	Short-circuit current			30		mA
	Margining range	With EN_MARG = 1b(1)		±4.5		mV
	Margining resolution	With EN_MARG = 1b(1)		280		µV
DC ACCURACY(2) (C_{REFBUF} = 10µF, R_{ESR} = 0Ω)						
	Resolution			16		Bits
NMC	No missing codes		16			Bits
INL	Integral nonlinearity(3)		-0.5	±0.3	0.5	LSB(4)
DNL	Differential nonlinearity(3)		-0.5	±0.2	0.5	LSB (4)
$E_{(IO)}$	Input offset error(3)	T_A = 25°C(5)	-3	±0.5	3	LSB (4)
		T_A = –40°C to +125°C(5)	-5	±3	5	
dV_{OS}/dT	Input offset thermal drift(5)			1		µV/°C
G_E	Gain error(3)	EN_MARG = 0b(1) (6)	-0.03	±0.005	0.03	%FSR
dG_E/dT	Gain error thermal drift	EN_MARG = 0b(1) (6)		3.6		ppm/°C
TNS	Transition noise			0.5		LSB (4)
	First output code deviation for burst-mode data acquisition	See *Section 6.3.2*	–3		3	TNS
CMRR	Common-mode rejection ratio	dc to 20kHz		80		dB
SAMPLING DYNAMICS						
	Aperture delay			4		ns
$t_{j\text{-rms}}$	Aperture jitter			2		ps RMS
$f_{3\text{-DB(small)}}$	Small-signal bandwidth			23		MHz

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5.5 Electrical Characteristics (continued)

At RV_{DD} = 5.5V, DV_{DD} = 1.65V to 5.5V, V_{REF} = 5V, and maximum throughput (unless otherwise noted). Minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC ACCURACY(2) (7) (C_{REFBUF} = 10µF, R_{ESR} = 0Ω)						
SINAD	Signal-to-noise + distortion	f_{IN} = 2kHz	95.7	95.9		dB
SNR	Signal-to-noise ratio	f_{IN} = 2kHz	96	96.8		dB
		f_{IN} = 100kHz		95		
THD	Total harmonic distortion	f_{IN} = 2kHz		–125		dB
		f_{IN} = 100kHz		–110		
SFDR	Spurious-free dynamic range	f_{IN} = 2kHz		25		dB
LDO OUTPUT (DECAP)						
V_{LDO}	LDO output voltage (DECAP pins)			2.85		V
C_{LDO}	External ceramic capacitor on DECAP pins		1			µF
t_{PU_LDO}	LDO power-up time	C_{LDO} = 1µF, RV_{DD} > V_{LDO}		1		ms
$I_{SHRT-LDO}$	Short-circuit current			100		mA
DIGITAL INPUTS						
V_{IH}	High-level input voltage	1.65V < DV_{DD} < 2.3V	0.8 DV_{DD}		DV_{DD} + 0.3	V
		2.3V < DV_{DD} < 5.5V	0.7 DV_{DD}		DV_{DD} + 0.3	
V_{IL}	Low-level input voltage	1.65V < DV_{DD} < 2.3V	–0.3		0.2 DV_{DD}	V
		2.3V < DV_{DD} < 5.5V	–0.3		0.3 DV_{DD}	
	Input current			±0.01	0.1	µA
DIGITAL OUTPUTS						
V_{OH}	High-level output voltage	I_{OH} = 500µA source	0.8 DV_{DD}		DV_{DD}	V
V_{OL}	Low-level output voltage	I_{OH} = 500µA sink	0		0.2 DV_{DD}	V
POWER SUPPLY						
I_{RVDD}	Analog supply current	ADS8920B at RV_{DD} = 5V, 1MSPS		4.2	5.3	mA
		ADS8922B at RV_{DD} = 5V, 500-KSPS		3.2	4	mA
		ADS8924B at RV_{DD} = 5V, 250-KSPS		2.8	3.5	mA
		Static, no conversion		970		µA
		Static, PD_ADC = 1b(8)		900		µA
		Static, PD_REFBUF = 1b(8)		120		µA
		Static, PD_ADC = 1b and PD_REFBUF = 1b(8)		40		µA
I_{DVDD}	Digital supply current	DV_{DD} = 3V, C_{LOAD} = 10pF, no conversion		1		µA
P_{RVDD}	Power dissipation	ADS8920B at RV_{DD} = 5V, 1MSPS		21	26.5	mW
		ADS8922B at RV_{DD} = 5V, 500-KSPS		16	20	
		ADS8924B at RV_{DD} = 5V, 250-KSPS		14	17.5	

(1) See the REF_MRG Register.
(2) While operating with internal reference buffer and LDO.
(3) See Figure 5-8, Figure 5-9, Figure 5-14, and Figure 5-15 for statistical distribution data for DNL, INL, offset, and gain error parameters.
(4) LSB = least-significant bit. 1LSB at 16-bit resolution is approximately 15ppm .
(5) For selected V_{REF}, see the OFST_CAL Register.
(6) Includes internal reference buffer errors and drifts.
(7) For V_{IN} = –0.1dBFS.
(8) See the PD_CNTL Register.

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5.6 Timing Requirements

			MIN	TYP	MAX	UNIT	TIMING DIAGRAM
CONVERSION CYCLE							
f_{cycle}	Sampling frequency	ADS8920B			1000	kHz	Figure 5-1
		ADS8922B			500		
		ADS8924B			250		
t_{cycle}	ADC cycle-time period	ADS8920B	1			µs	
		ADS8922B	2				
		ADS8924B	4				
t_{wh_CONVST}	Pulse duration: CONVST high		30			ns	
t_{wl_CONVST}	Pulse duration: CONVST low		30			ns	
t_{acq}	Acquisition time		300			ns	
t_{qt_acq}	Quiet acquisition time		30			ns	Figure 6-15, see Section 6.5.4
t_{d_cnvcap}	Quiet aperture time		20			ns	
ASYNCHRONOUS RESET, AND LOW POWER MODES							
t_{wl_RST}	Pulse duration: $\overline{RST}$ low		100			ns	Figure 5-2
SPI-COMPATIBLE SERIAL INTERFACE							
f_{CLK}	Serial clock frequency	2.35V ≤ D_{VDD} ≤ 5.5V, T_A = –40°C to +125°C, V_{IH} > 0.7 D_{VDD}, V_{IL} < 0.3D_{VDD}			70	MHz	Figure 5-3
		1.65V ≤ D_{VDD} < 2.35V, T_A = –40°C to +125°C, V_{IH} > 0.8 D_{VDD}, V_{IL} < 0.2D_{VDD}			20		
		1.65V ≤ D_{VDD} < 2.35V, T_A = 0°C to +60°C, V_{IH} > 0.8 D_{VDD}, V_{IL} < 0.2D_{VDD}			57		
		1.65V ≤ D_{VDD} < 2.35V, T_A = –40°C to +125°C, V_{IH} > 0.9 D_{VDD}, V_{IL} < 0.1D_{VDD}			68		
		1.71V ≤ DV_{DD} < 1.89V, T_A = +20°C to +90°C, V_{IH} > 0.75 DV_{DD}, V_{IL} < 0.25 DV_{DD}			52		
t_{CLK}	Serial clock time period		$1/f_{CLK}$			ns	Figure 5-3
t_{ph_CK}	SCLK high time		0.45		0.55	t_{CLK}	Figure 5-3
t_{pl_CK}	SCLK low time		0.45		0.55	t_{CLK}	
t_{su_CSCK}	Setup time: $\overline{CS}$ falling to the first SCLK capture edge		12			ns	
t_{su_CKDI}	Setup time: SDI data valid to the SCLK capture edge		1.5			ns	
t_{ht_CKDI}	Hold time: SCLK capture edge to (previous) data valid on SDI		1			ns	
t_{ht_CKCS}	Delay time: last SCLK falling to $\overline{CS}$ rising		7			ns	
SOURCE-SYNCHRONOUS SERIAL INTERFACE (External Clock)(1)							
f_{CLK}	Serial clock frequency	SDR (DATA_RATE = 0b), 2.35V ≤ DV_{DD} ≤ 5.5V			70	MHz	Figure 5-4, see Section 6.5.4
		DDR (DATA_RATE = 1b), 2.35V ≤ DV_{DD} ≤ 5.5V			35		
t_{CLK}	Serial clock time period		$1/f_{CLK}$			ns	

(1) The external clock option is not recommended when operating with DV_{DD} < 2.35V. See Table 6-9.

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5.7 Switching Characteristics

At RV_{DD} = 5.5V, DV_{DD} = 1.65V to 5.5V, V_{REF} = 5V, and maximum throughput (unless otherwise noted). Minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C.

PARAMETER[1]			MIN	TYP	MAX	UNIT	TIMING DIAGRAM
CONVERSION CYCLE							
t_{conv}	Conversion time	ADS8920B	580		640	ns	Figure 5-1
		ADS8922B	1100		1200		
		ADS8924B	2400		2500		
ASYNCHRONOUS RESET, AND LOW POWER MODES							
t_{d_rst}	Delay time: $\overline{RST}$ rising to RVS rising				3	ms	Figure 5-2
t_{PU_ADC}	Power-up time for converter module		1			ms	See PD_CNTL Register
t_{PU_REFBUF}	Power-up time for internal reference buffer, C_{REFBUF} = 10µF		10			ms	
t_{PU_Device}	Power-up time for device	C_{LDO} = 1µF, C_{REFBUF} = 10µF	10			ms	
SPI-COMPATIBLE SERIAL INTERFACE							
t_{den_CSDO}	Delay time: $\overline{CS}$ falling to data enable				9	ns	Figure 5-3
t_{dz_CSDO}	Delay time: $\overline{CS}$ rising to SDO going to Hi-Z				10	ns	
t_{d_CKDO}	Delay time: SCLK launch edge to (next) data valid on SDO				13	ns	
$t_{d_CSRDY_f}$	Delay time: $\overline{CS}$ falling to RVS falling				12	ns	Figure 5-4
$t_{d_CSRDY_r}$	Delay time: $\overline{CS}$ rising to RVS rising	After NOP operation			30	ns	Figure 5-4
		After WR or RD operation			120		
SOURCE-SYNCHRONOUS SERIAL INTERFACE (External Clock)[1]							
$t_{d_CKSTR_r}$	Delay time: SCLK launch edge to RVS rising				13	ns	Figure 5-4
$t_{d_CKSTR_f}$	Delay time: SCLK launch edge to RVS falling				13	ns	
$t_{off_STRDO_f}$	Time offset: RVS falling to (next) data valid on SDO		-2		2	ns	
$t_{off_STRDO_r}$	Time offset: RVS rising to (next) data valid on SDO		-2		2	ns	
t_{ph_STR}	Strobe output high time, 2.35V ≤ DV_{DD} ≤ 5.5V		0.45		0.55	t_{STR}	
t_{pl_STR}	Strobe output low time, 2.35V ≤ DV_{DD} ≤ 5.5V		0.45		0.55	t_{STR}	
SOURCE-SYNCHRONOUS SERIAL INTERFACE (Internal Clock)							
t_{d_CSSTR}	Delay time: $\overline{CS}$ falling to RVS rising		15		50	ns	Figure 5-5
t_{STR}	Strobe output time period	INTCLK option		15		ns	
		INTCLK / 2 option		30			
		INTCLK / 4 option		60			
t_{ph_STR}	Strobe output high time		0.45		0.55	t_{STR}	
t_{pl_STR}	Strobe output low time		0.45		0.55	t_{STR}	

(1) The external clock option is not recommended when operating with DVDD < 2.35V. See Table 6-9.

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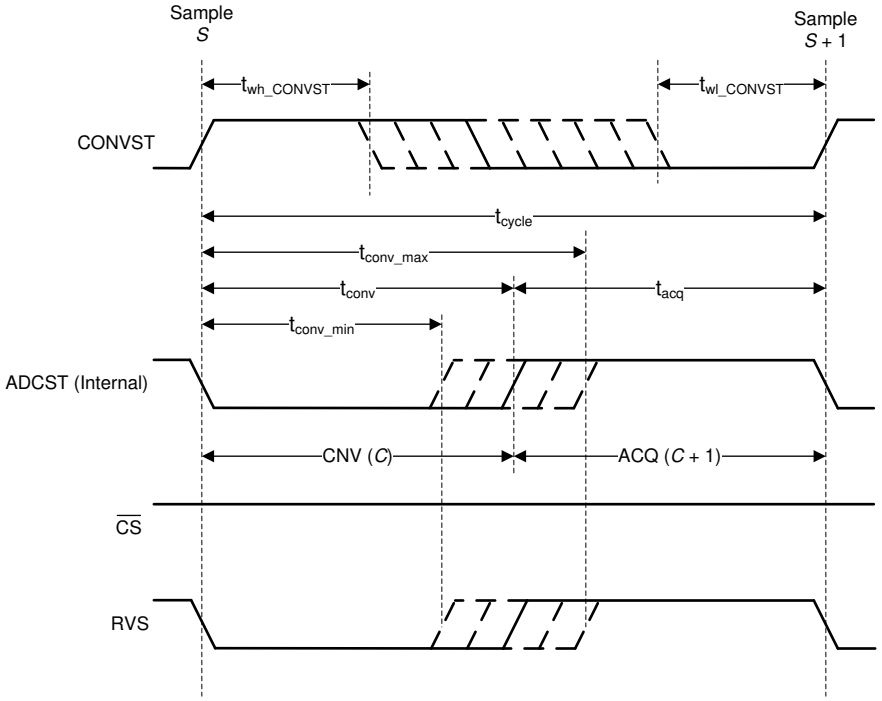


Figure 5-1. Conversion Cycle Timing

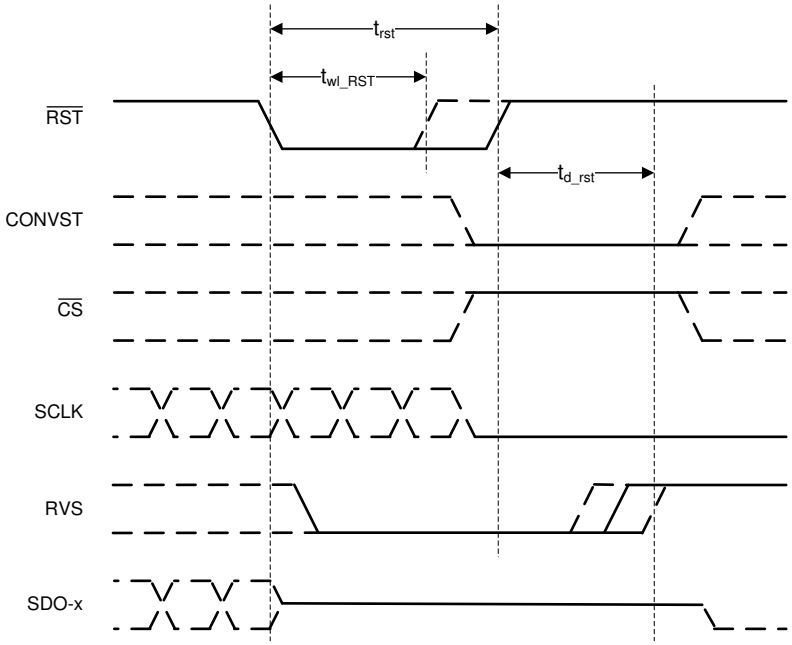
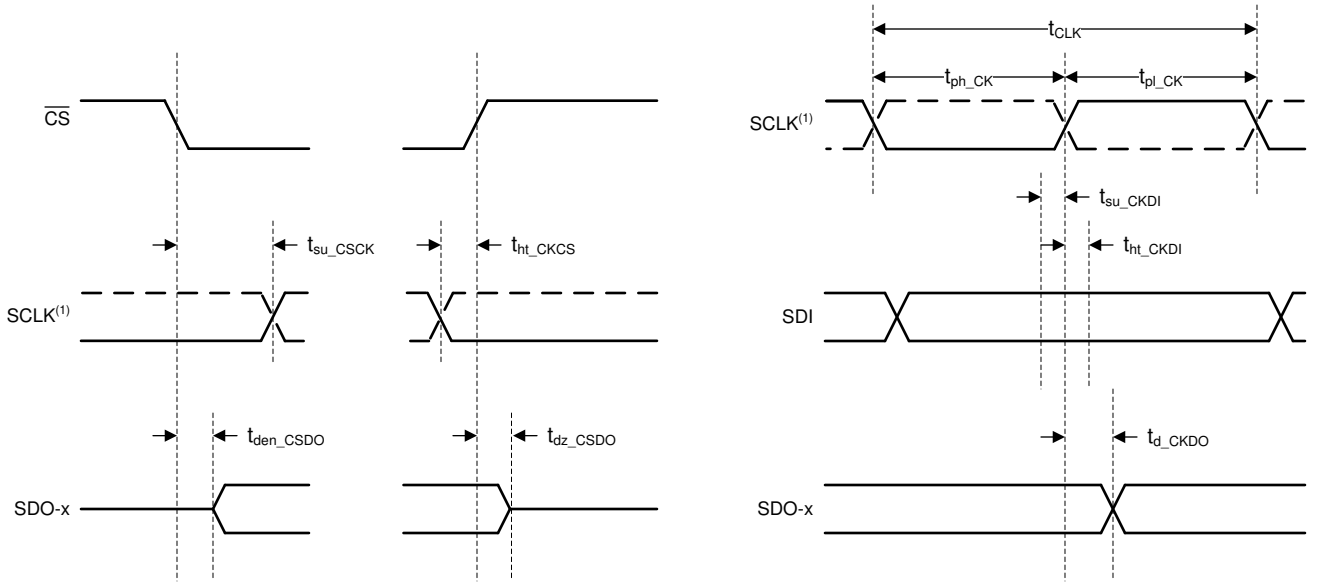


Figure 5-2. Asynchronous Reset Timing



1. The SCLK polarity, launch edge, and capture edge depend on the SPI protocol selected.

Figure 5-3. SPI-Compatible Serial Interface Timing

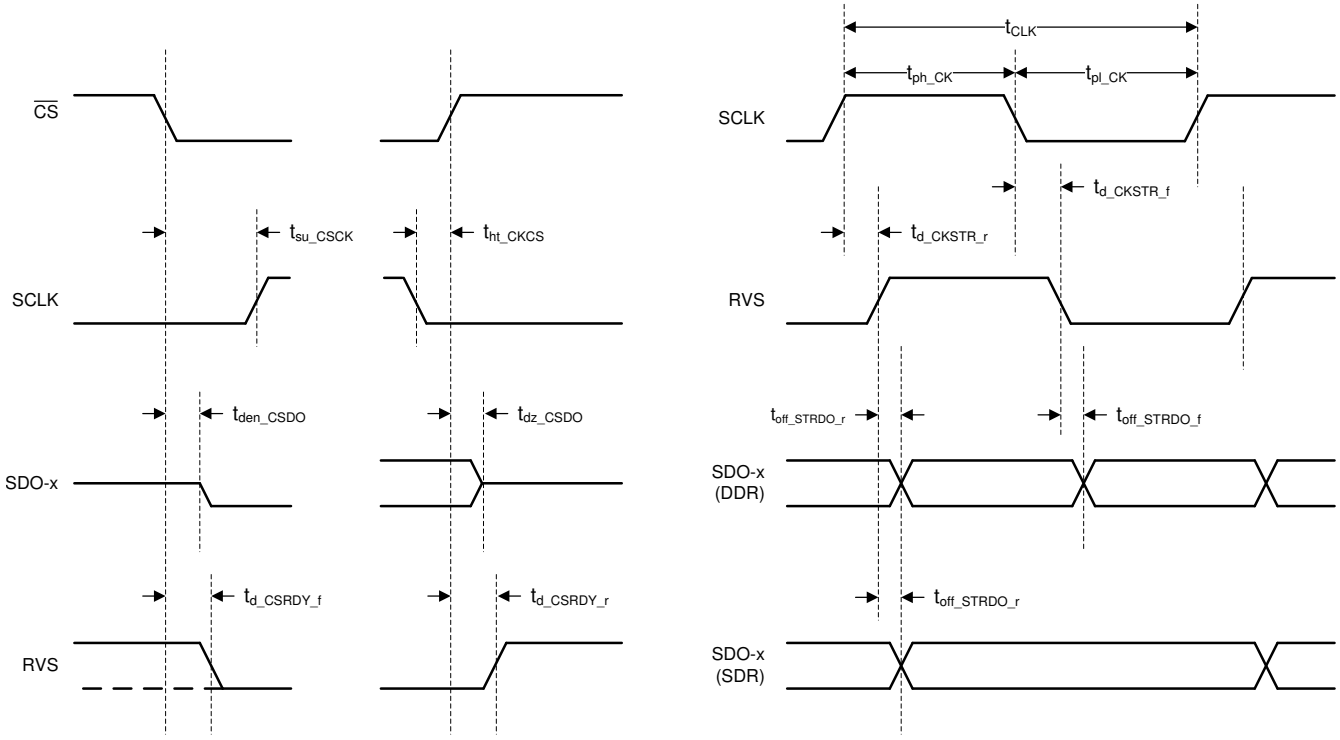


Figure 5-4. Source-Synchronous Serial Interface Timing (External Clock)

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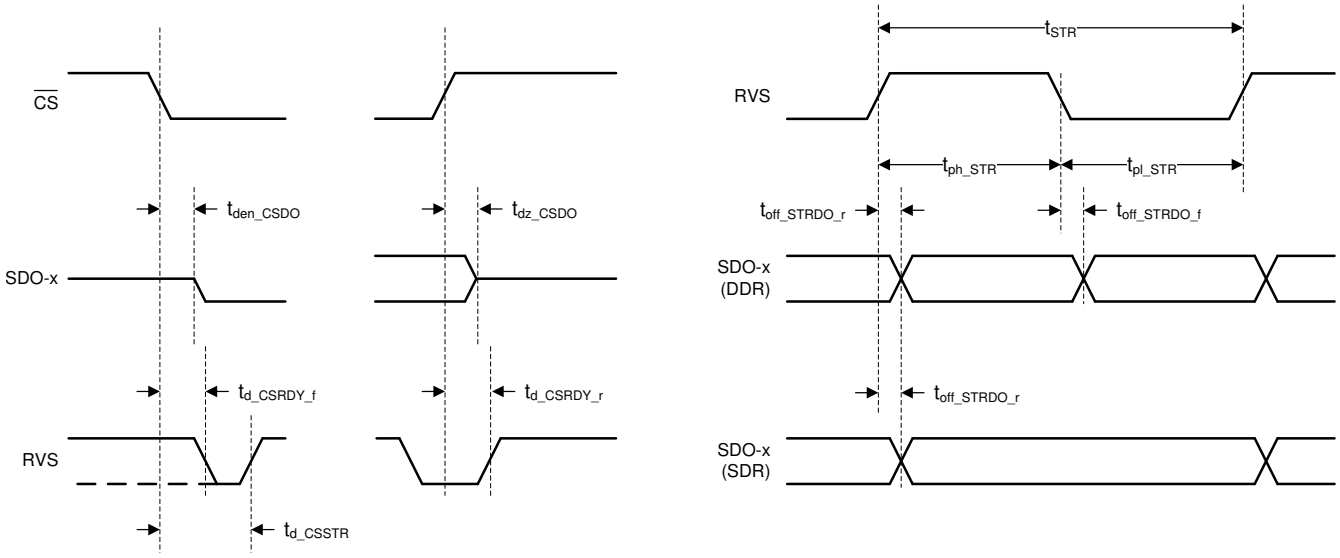
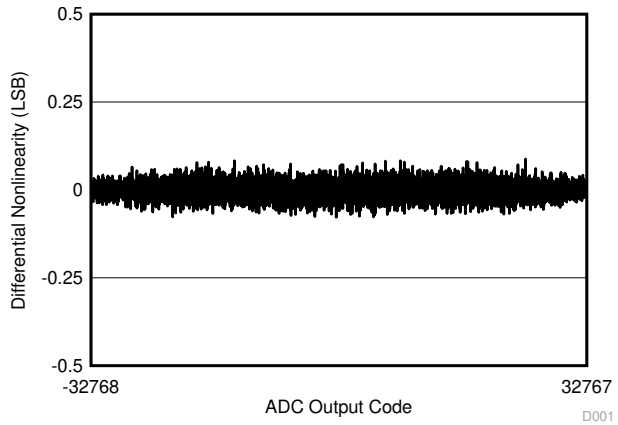


Figure 5-5. Source-Synchronous Serial Interface Timing (Internal Clock)

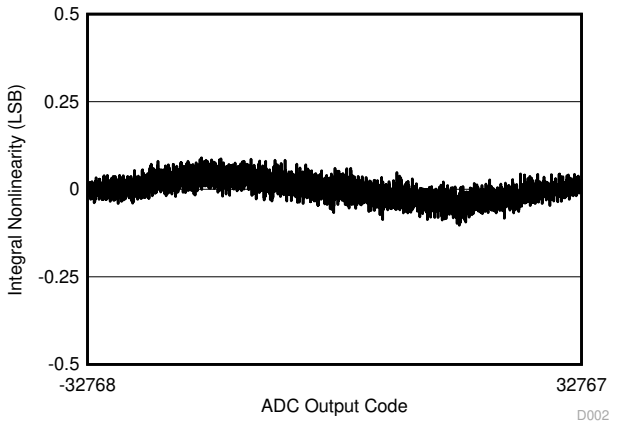
5.8 Typical Characteristics

at T_A = 25°C, RV_{DD} = 5.5V, DV_{DD} = 3V, V_{REF} = 5V, and maximum-rated throughput (unless otherwise noted)



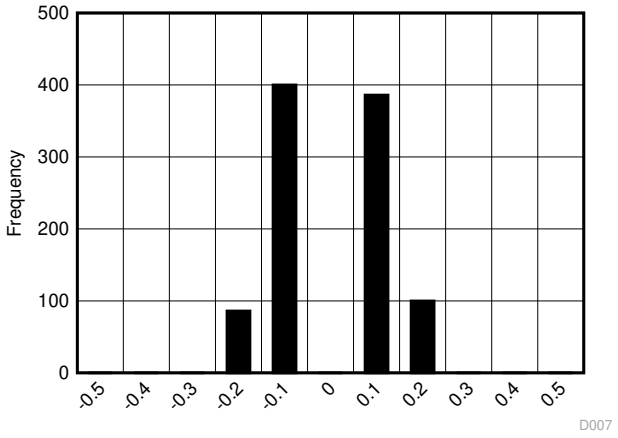
Typical DNL = ±0.2LSB

Figure 5-6. Typical DNL



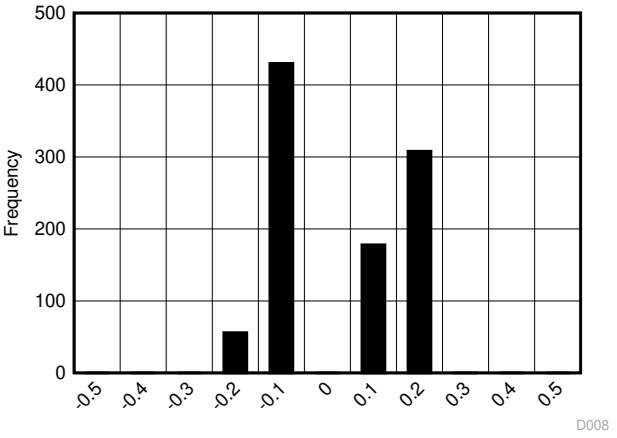
Typical INL = ±0.3LSB

Figure 5-7. Typical INL



1000 devices

Figure 5-8. Typical DNL Distribution



1000 devices

Figure 5-9. Typical INL Distribution

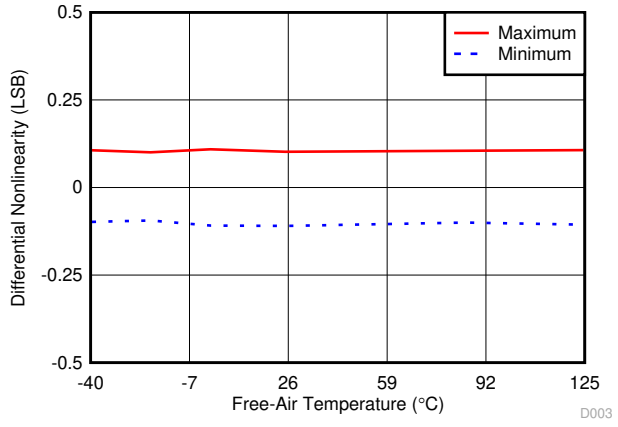


Figure 5-10. DNL vs Temperature

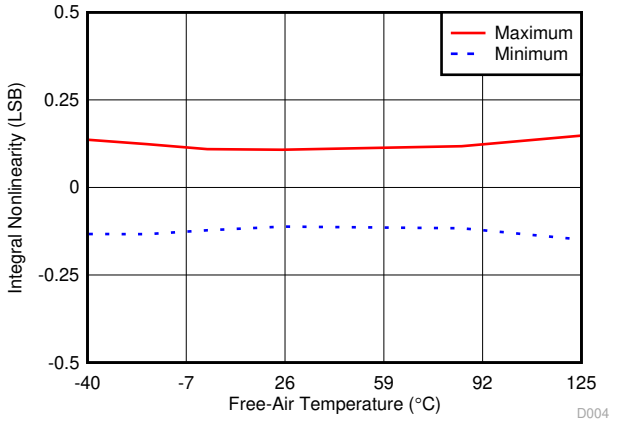


Figure 5-11. INL vs Temperature

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5.8 Typical Characteristics (continued)

at T_A = 25°C, RV_{DD} = 5.5V, DV_{DD} = 3V, V_{REF} = 5V, and maximum-rated throughput (unless otherwise noted)

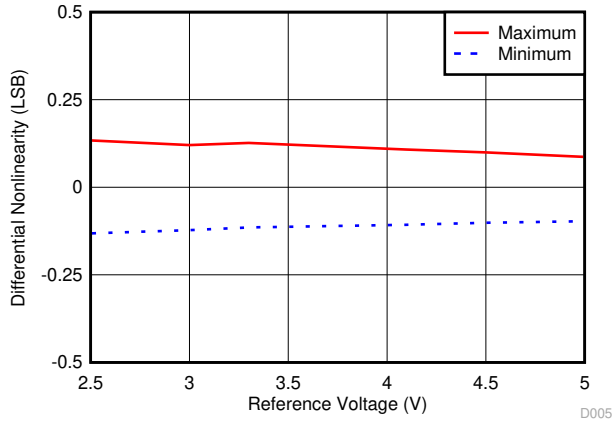


Figure 5-12. DNL vs Reference Voltage

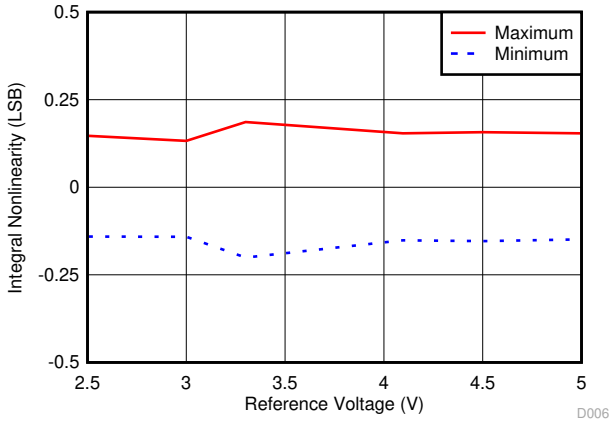


Figure 5-13. INL vs Reference Voltage

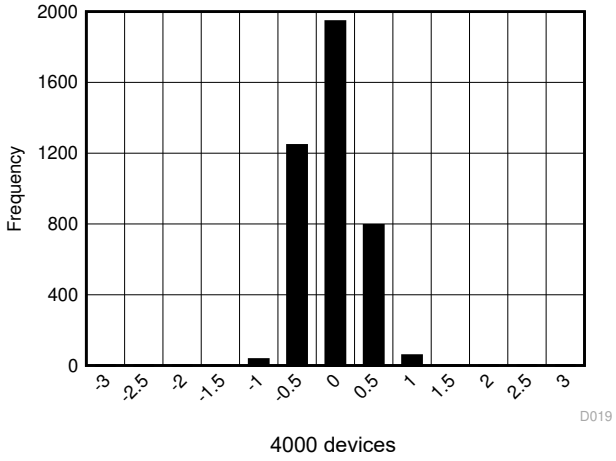


Figure 5-14. Typical Offset Distribution

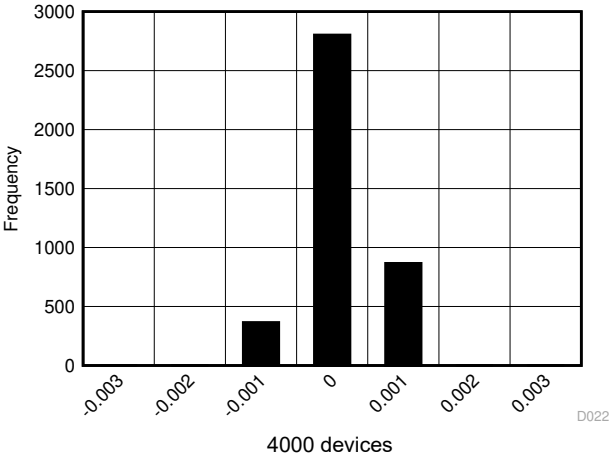


Figure 5-15. Typical Gain Error Distribution

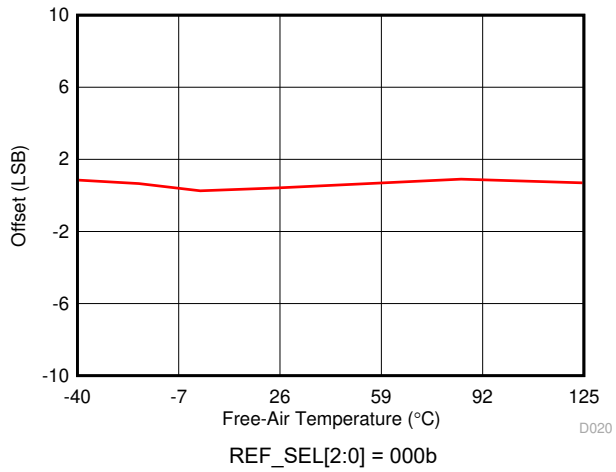


Figure 5-16. Offset vs Temperature

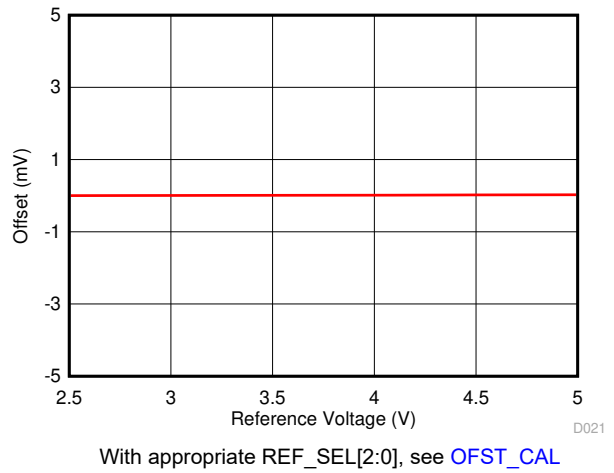
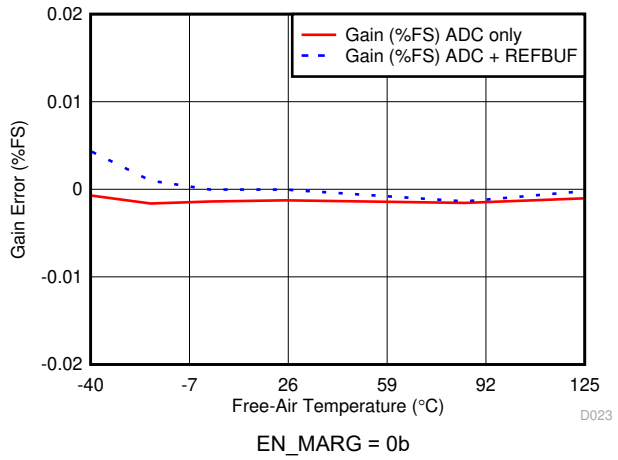


Figure 5-17. Offset vs Reference Voltage

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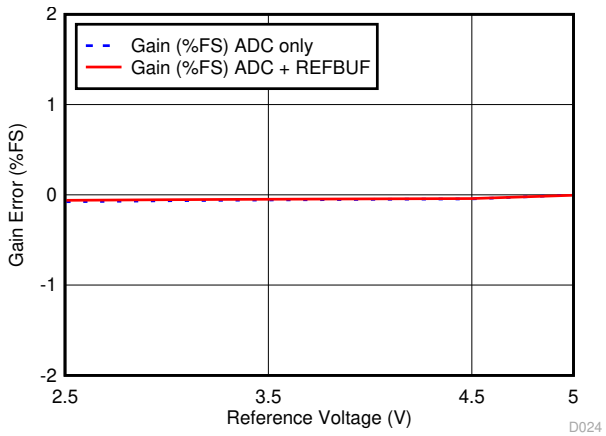
5.8 Typical Characteristics (continued)

at T_A = 25°C, RV_{DD} = 5.5V, DV_{DD} = 3V, V_{REF} = 5V, and maximum-rated throughput (unless otherwise noted)



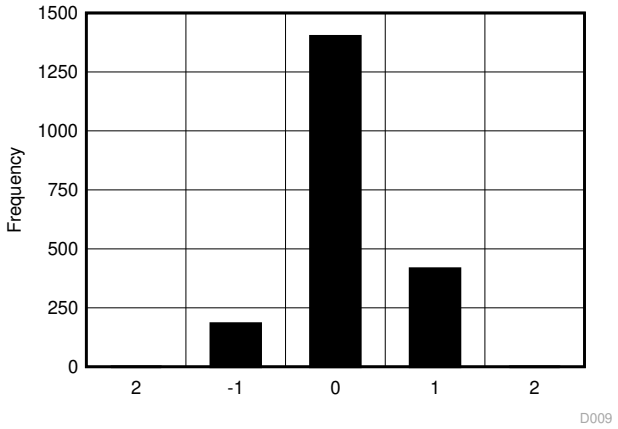
EN_MARG = 0b

Figure 5-18. Gain Error vs Temperature



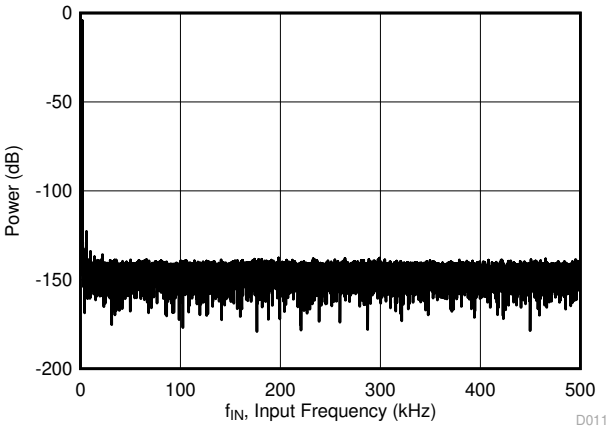
EN_MARG = 0b

Figure 5-19. Gain Error vs Reference Voltage



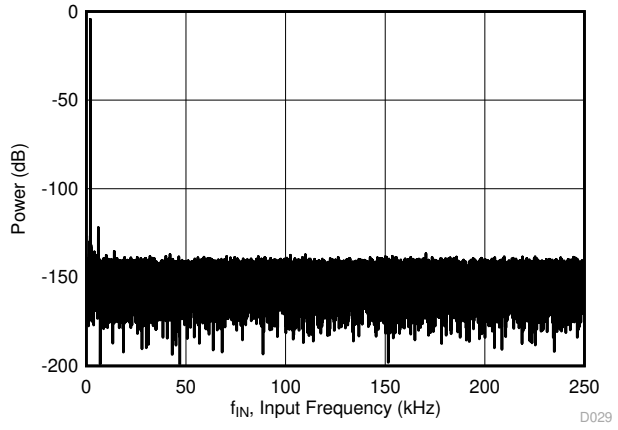
Standard Deviation = 0.47LSB

Figure 5-20. DC Input Histogram



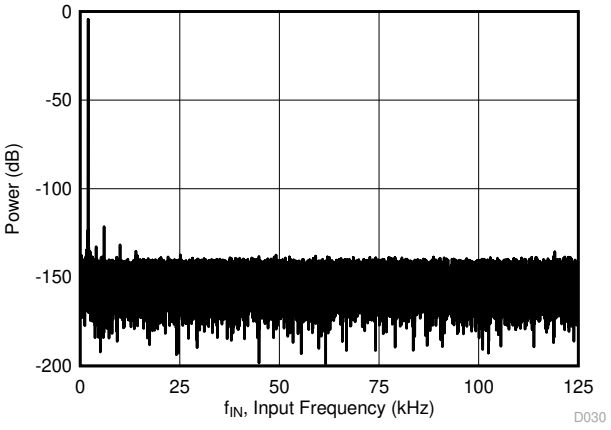
f_{IN} = 2kHz SNR = 96.8dB THD = –125dB

Figure 5-21. Typical FFT - ADS8920B



f_{IN} = 2kHz SNR = 96.8dB THD = –125dB

Figure 5-22. Typical FFT - ADS8922B



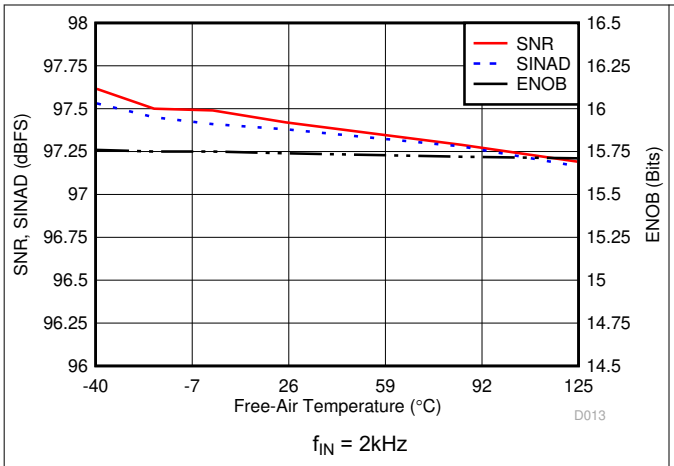
f_{IN} = 2kHz SNR = 96.8dB THD = –125dB

Figure 5-23. Typical FFT - ADS8924B

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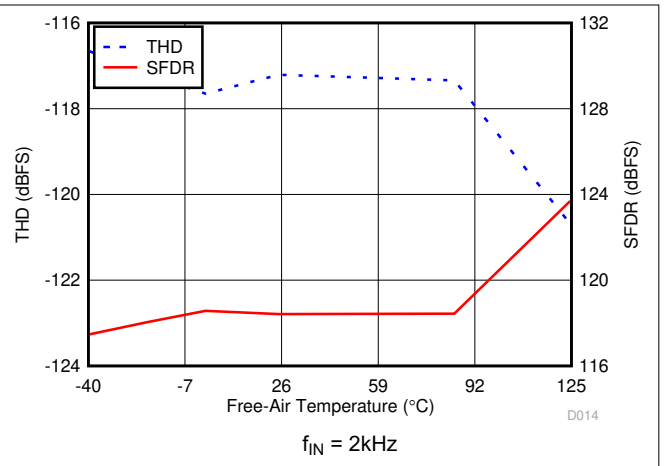
5.8 Typical Characteristics (continued)

at T_A = 25°C, RV_{DD} = 5.5V, DV_{DD} = 3V, V_{REF} = 5V, and maximum-rated throughput (unless otherwise noted)



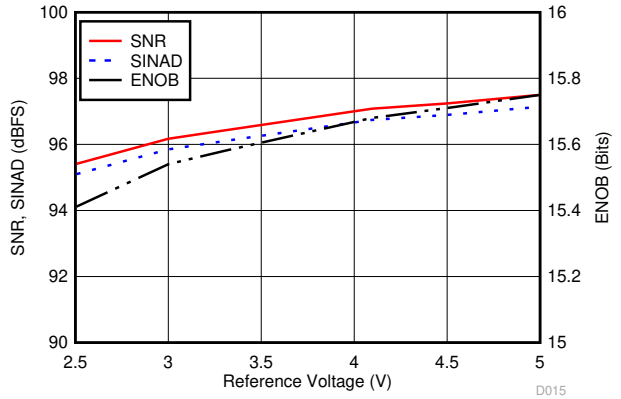
f_{IN} = 2kHz

Figure 5-24. Noise Performance vs Temperature



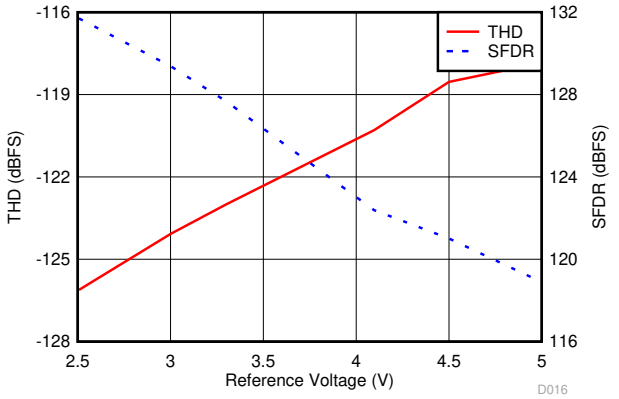
f_{IN} = 2kHz

Figure 5-25. Distortion Performance vs Temperature



f_{IN} = 2kHz

Figure 5-26. Noise Performance vs Reference Voltage



f_{IN} = 2kHz

Figure 5-27. Distortion Performance vs Reference Voltage

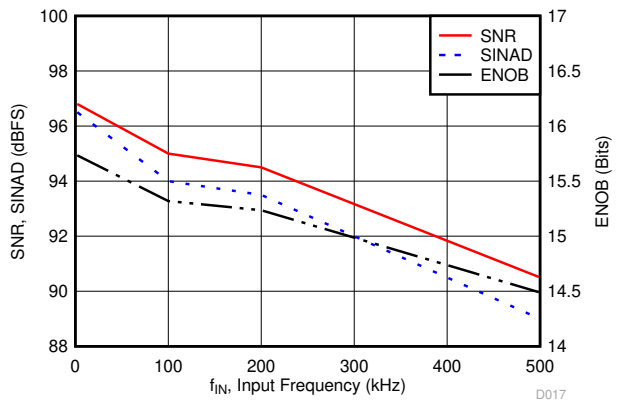


Figure 5-28. Noise Performance vs Input Frequency

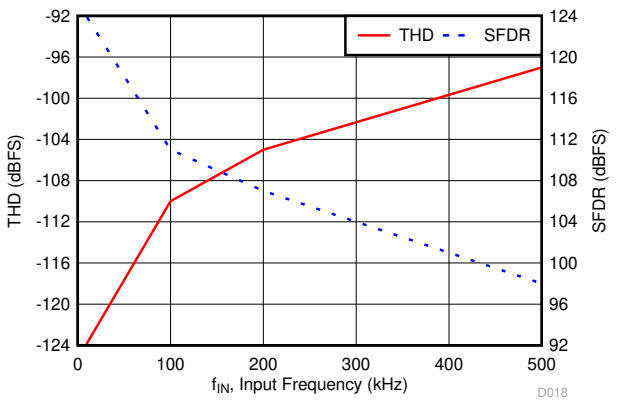


Figure 5-29. Distortion Performance vs Input Frequency

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5.8 Typical Characteristics (continued)

at T_A = 25°C, RV_{DD} = 5.5V, DV_{DD} = 3V, V_{REF} = 5V, and maximum-rated throughput (unless otherwise noted)

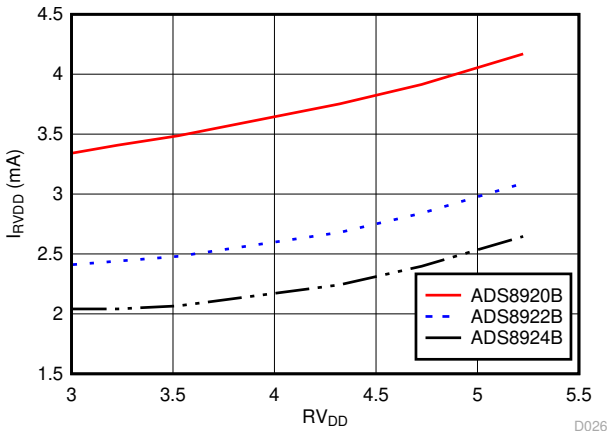
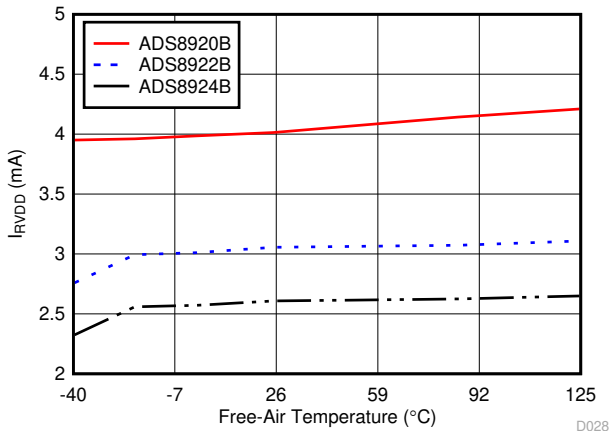


Figure 5-30. Analog Supply Current vs Supply Voltage



RV_{DD} = 5V

Figure 5-31. Analog Supply Current vs Temperature

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6 Detailed Description

6.1 Overview

The ADS892xB is a family of high-speed, successive approximation register (SAR), analog-to-digital converters (ADC) based on a charge redistribution architecture. These compact devices integrate a reference buffer and LDO, and feature high performance at a high throughput rate with low power consumption.

This device family supports unipolar, fully differential, analog input signals. The integrated reference buffer supports the burst mode of data acquisition for external reference voltages in the range 2.5V to 5V, and offers a wide selection of input ranges without additional input scaling.

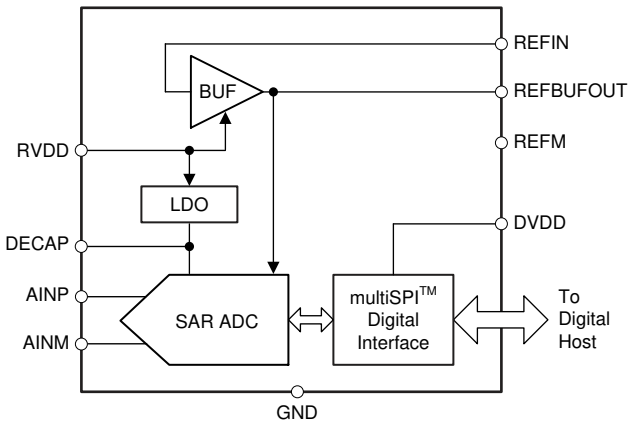
When a conversion is initiated, the differential input between the AINP and AINM pins is sampled on the internal capacitor array. The device uses an internal clock to perform conversions. During the conversion process, both analog inputs are disconnected from the internal circuit. At the end of conversion process, the device reconnects the sampling capacitors to the AINP and AINM pins and enters an acquisition phase.

The integrated LDO allows the device to operate on a single supply, RV_{DD}. The device consumes only 21 mW, 16 mW, or 14 mW of power when operating at the rated maximum throughput of 1MSPS, 500 kSPS, or 250 kSPS, respectively, with the internal reference buffer and LDO enabled.

The enhanced multiSPI™ digital interface is backward-compatible with traditional SPI protocol. Configurable features simplify board layout, timing, and firmware, and support high throughput at lower clock speeds, thus allowing an easy interface with a variety of microcontrollers, DSPs, and FPGAs.

The ADS892xB enables test and measurement, medical, and industrial applications to achieve fast, low-noise, low-distortion, low-power data acquisition in small form factors.

6.2 Functional Block Diagram



6.3 Feature Description

From a functional perspective, the device comprises four modules: the low-dropout regulator (LDO), the reference buffer (BUF), the converter (SAR ADC), and the interface (multiSPI digital interface), as shown in the *Functional Block Diagram* section.

The LDO module is powered by the RV_{DD} supply, and generates the bias voltage for internal circuit blocks of the device. The reference buffer module buffers the external reference voltage source from the dynamic, capacitive switching load present on the reference pins during the conversion process. The converter module samples and converts the analog input into an equivalent digital output code. The interface module facilitates communication and data transfer between the device and the host controller.

6.3.1 LDO Module

To enable single-supply operation, the device features an internal low-dropout regulator (LDO). The LDO is powered by the RV_{DD} supply, and the output is available on the two DECAP pins. This LDO output powers the critical analog blocks within the device, and must not be used for any other external purposes.

Short the two DECAP pins together, and decouple with the GND pin by placing a 1µF, X7R-grade, ceramic capacitor with a 10V rating, as shown in Figure 6-1. There is no upper limit on the value of the decoupling capacitor; however, a larger decoupling capacitor results in a longer power-up time for the device. See the *Layout* section for layout recommendations.

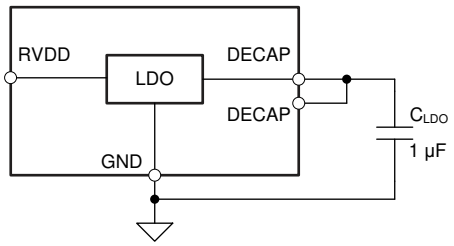


Figure 6-1. Internal LDO Connections

6.3.2 Reference Buffer Module

On the CONVST rising edge, the device moves from ACQ state to CONV state, and the internal capacitors are switched to the REFBUFOUT pins as per the successive approximation algorithm. Most of the switching charge required during the conversion process is provided by external decoupling capacitor C_{REFBUF}. If the charge lost from the C_{REFBUF} is not replenished before the next CONVST rising edge, the voltage on REFBUFOUT pins is less than $V_{REFBUFOUT}$. The subsequent conversion occurs with this different reference voltage, and causes a proportional error in the output code. The internal reference buffer of the device maintains the voltage on REFBUFOUT pins within 0.5LSB of $V_{REFBUFOUT}$. All the performance characteristics of the device are specified with the internal reference buffer and specified values of C_{REFBUF} and R_{ESR}.

In burst-mode of operation, the device stays in ACQ state for a long duration of time and then performs a burst of conversions. During the acquisition state (ACQ), the sampling capacitor (C_S) is connected to the differential input pins and no charge is drawn from the REFBUFOUT pins. However, during the very first conversion cycle, there is a step change in the current drawn from the REFBUFOUT pins. This sudden change in load triggers a transient settling response in the reference buffer. For a fixed input voltage, any transient settling error at the end of the conversion cycle results in a change in output codes over the subsequent conversions, as shown in Figure 6-2. The internal reference buffer of the ADS89xxB, when used with the recommended values of C_{REFBUF} and R_{ESR}, keeps the transient settling error at the end of each conversion cycle within 0.5LSB. Therefore, the device supports burst-mode of operation with every conversion result being as per the datasheet specifications.

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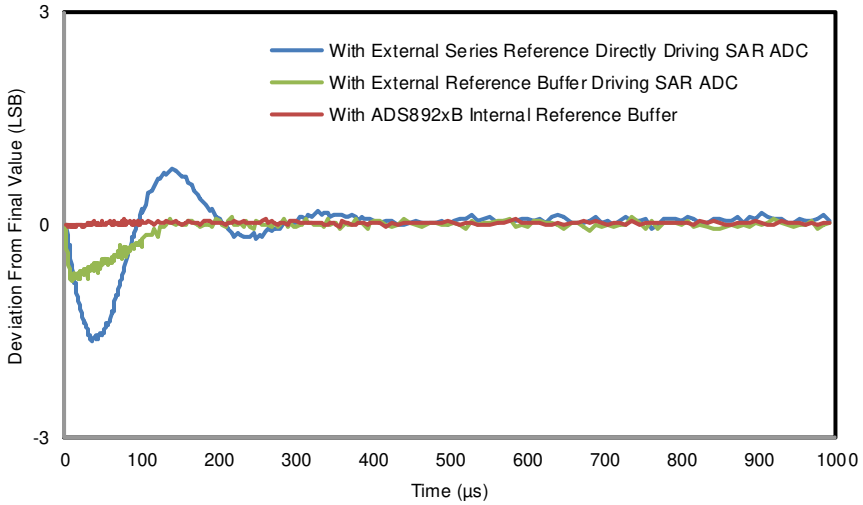


Figure 6-2. ADC Output Codes in Burst-Mode Operation With Various ADC Reference Buffers

Figure 6-3 shows the block diagram of the internal reference buffer.

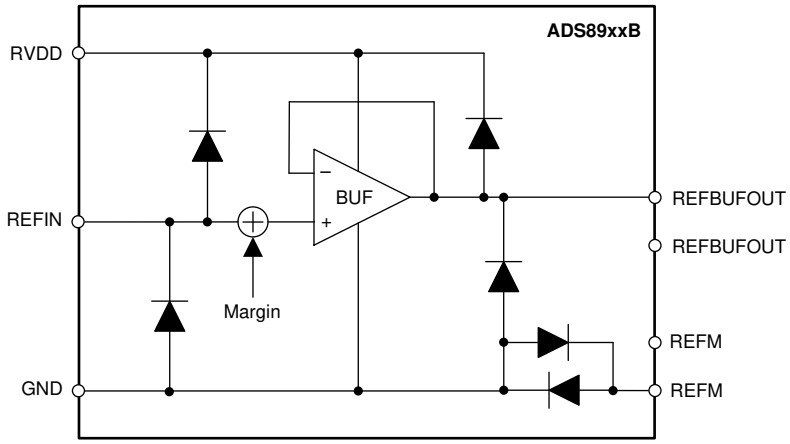


Figure 6-3. Internal Reference Buffer Block Diagram

The input range for the device is set by the external voltage applied at the REFIN pin (V_{REF}). The REFIN pin has electrostatic discharge (ESD) protection diodes to the RVDD and GND pins. For minimum input offset error (see $E_{(IO)}$ specified in the *Electrical Characteristics*), set the REF_SEL[2:0] bits to the value closest to V_{REF} (see the OFST_CAL register).

The internal reference buffer has a typical gain of 1V/V with minimal offset error (see $V_{(RO)}$ specified in the *Electrical Characteristics*), and the output of the buffer is available between the REFBUFOUT pins and the REFM pins. Set the REF_OFST[4:0] bits to add or subtract an intentional offset voltage (see the REF_MRG register).

Figure 6-4 shows the external connections required for the internal reference buffer.

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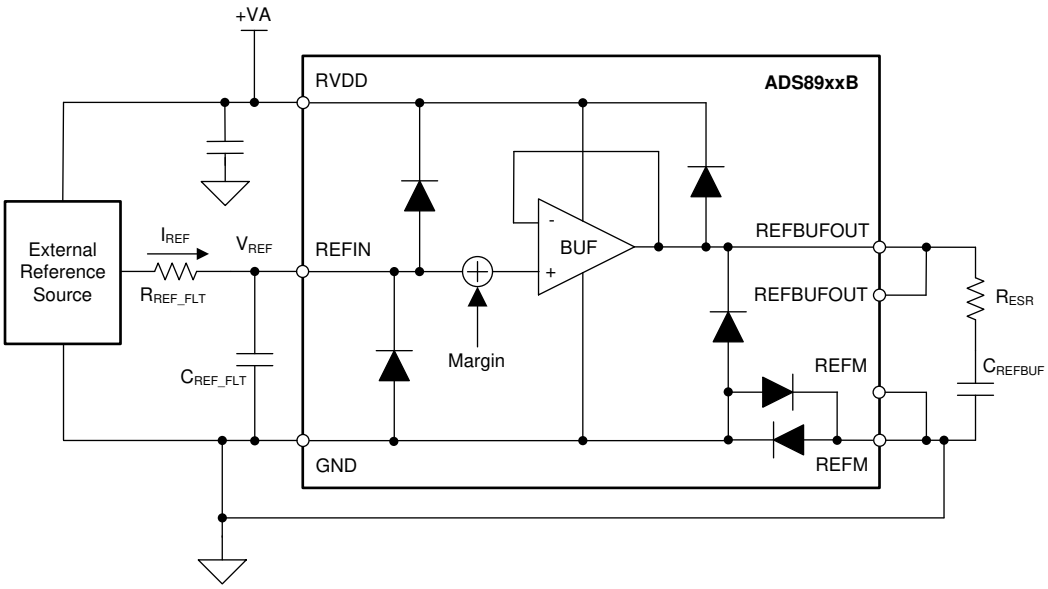


Figure 6-4. External Connections for the Internal Reference Buffer

Select R_{REF_FLT} and C_{REF_FLT} to limit the broadband noise contribution from the external reference source. The device takes very little current, I_{REF}, from the REFIN pin (typically, 0.1µA). However, this current flows through R_{REF_FLT} and can result in additional gain error.

Short the two REFBUFOUT pins externally. Short the two REFM pins to GND externally. As shown in Figure 6-4, place a combination of R_{ESR} and C_{REFBUF} (see the *Electrical Characteristics*) between the REFBUFOUT pins and the REFM pins as close to the device as possible. See the *Layout* section for layout recommendations.

6.3.3 Converter Module

As shown in Figure 6-5, the converter module samples the analog input signal (provided between the AINP and AINM pins), compares this signal with the reference voltage (between the pair of REFBUFOUT and REFM pins), and generates an equivalent digital output code.

The converter module receives $\overline{RST}$ and CONVST inputs from the interface module, and outputs the ADCST signal and the conversion result back to the interface module.

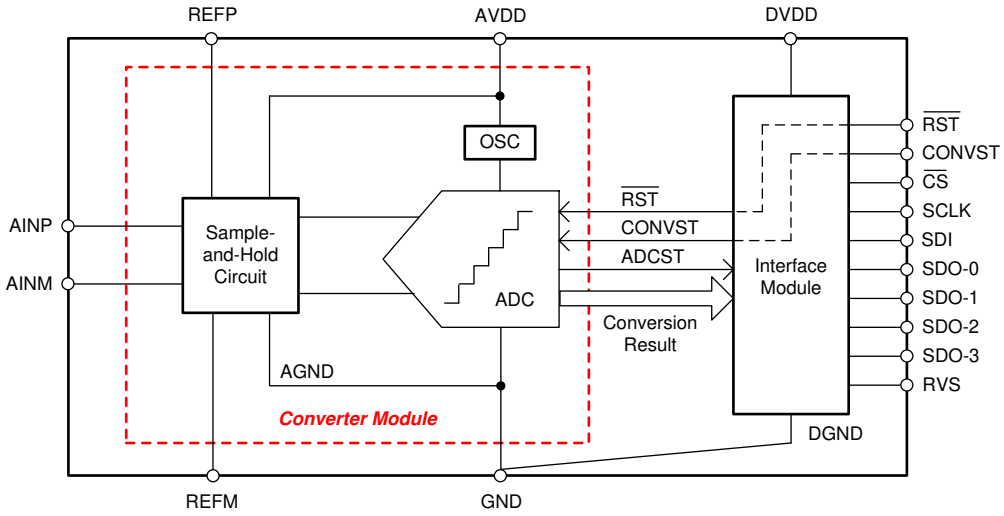


Figure 6-5. Converter Module

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6.3.3.1 Sample-and-Hold Circuit

These devices support unipolar, fully differential, analog input signals. Figure 6-6 shows a small-signal equivalent circuit of the sample-and-hold circuit. Each sampling switch is represented by a resistance (R_{S1} and R_{S2}, typically 50Ω) in series with an ideal switch (SW_1 and SW_2). The sampling capacitors, C_{S1} and C_{S2}, are typically 60 pF.

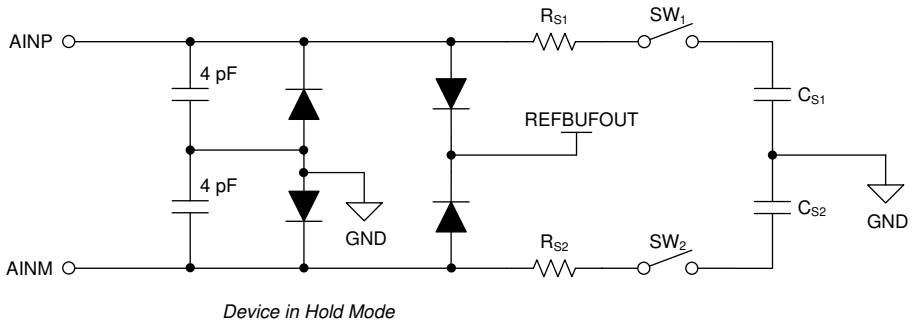


Figure 6-6. Input Sampling Stage Equivalent Circuit

During the acquisition process (ACQ state), both positive and negative inputs are individually sampled on C_{S1} and C_{S2}, respectively. During the conversion process (CNV state), the device converts for the voltage difference between the two sampled values: $V_{AINP} – V_{AINM}$.

Each analog input pin has electrostatic discharge (ESD) protection diodes to REFBUFOUT and GND. Keep the analog inputs within the specified range to avoid turning the diodes on.

Equation 2 and Equation 3 show the full-scale input range (FSR) and common-mode voltage (V_{CM}), respectively, supported at the analog inputs for any external reference voltage provided on the REFIN pin (V_{REF}).

$$\text{FSR} = \pm V_{REF} \quad (1)$$

$$\text{FSR} = V_{REF} \quad (2)$$

$$V_{CM} = \left(\frac{V_{REF}}{2} \right) \pm 0.1\text{V} \quad (3)$$

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6.3.3.2 Internal Oscillator

The device family features an internal oscillator (OSC) that provides the conversion clock; see Figure 6-5. The conversion duration is bound by the minimum and maximum value of t_{conv}, as specified in the *Switching Characteristics* table.

The interface module uses this internal clock (OSC), an external clock (provided by the host controller on the SCLK pin), or a combination of both the internal and external clocks, to execute the data transfer operations between the device and host controller; see the *Interface Module* section for more details.

6.3.3.3 ADC Transfer Function

The device family supports unipolar, fully differential analog inputs. The device output is in two's compliment format. Figure 6-7 and Table 6-1 show the ideal transfer characteristics for the device.

The least significant bit (LSB) for the ADC is given by Equation 4:

$$1\ \text{LSB} = \frac{\text{FSR}}{2^{16}} = 2 \times \frac{V_{REF}}{2^{16}} \tag{4}$$

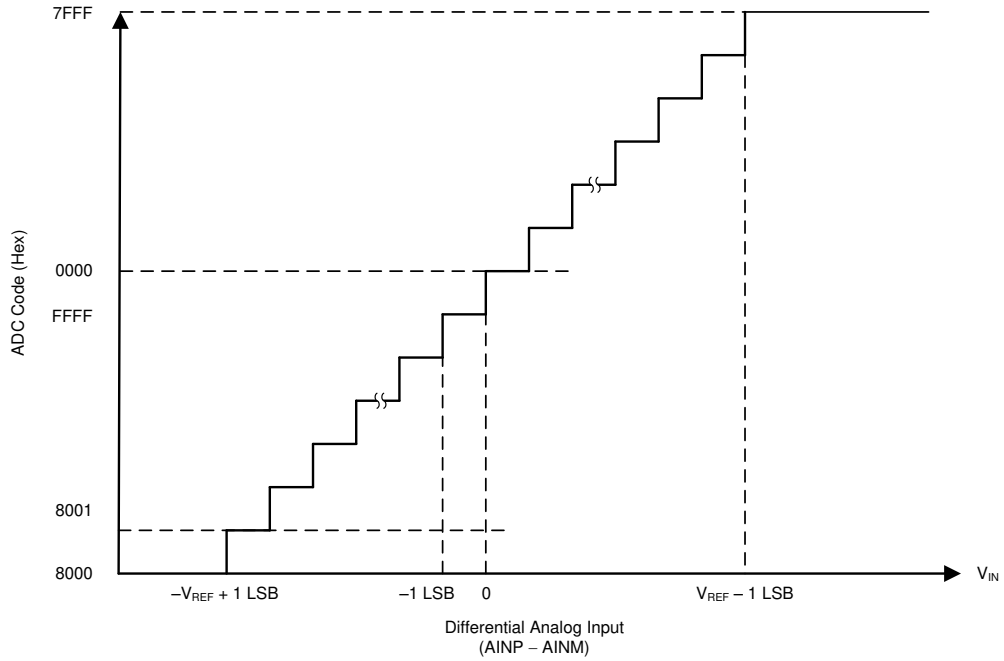


Figure 6-7. Transfer Characteristics

Table 6-1. Transfer Characteristics

DIFFERENTIAL ANALOG INPUT VOLTAGE (AINP – AINM)	OUTPUT CODE (HEX)
< $-V_{REF}$	8000
$-V_{REF}$ + 1LSB	8001
–1LSB	FFFF
0	0000
1LSB	0001
> V_{REF} – 1LSB	7FFF

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6.3.4 Interface Module

The interface module facilitates the communication and data transfer between the device and the host controller. As shown in Figure 6-8, the module consists of shift registers (both input and output), configuration registers, and a protocol unit.

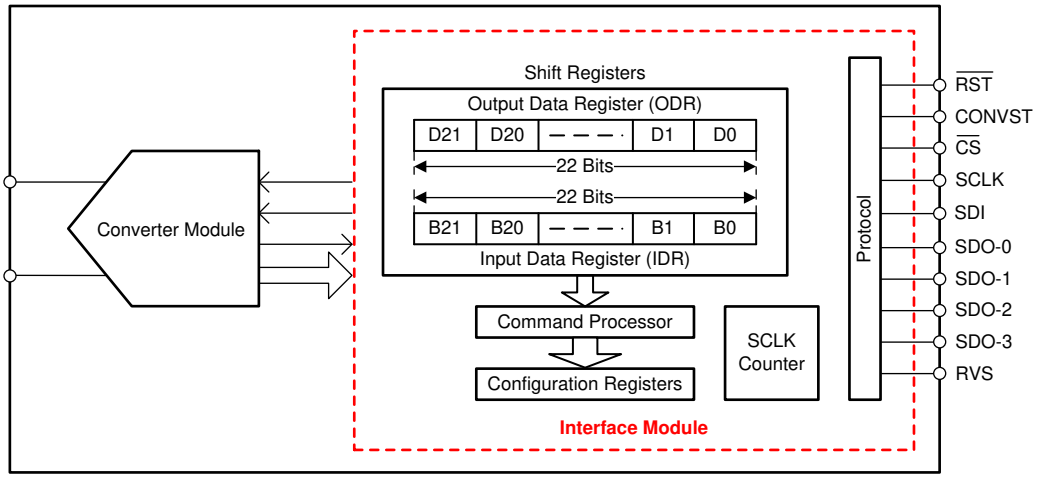


Figure 6-8. Interface Module

The *Pin Configuration and Functions* section provides descriptions of the interface pins. The *Data Transfer Frame* section details the functions of shift registers, the SCLK counter, and the command processor. The *Data Transfer Protocols* section details supported protocols. The *Register Maps* section explains the configuration registers and bit settings.

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6.4 Device Functional Modes

As shown in Figure 6-9, this device family supports three functional states: RST, ACQ, and CNV. The device state is determined by the status of the CONVST and $\overline{\text{RST}}$ control signals provided by the host controller.

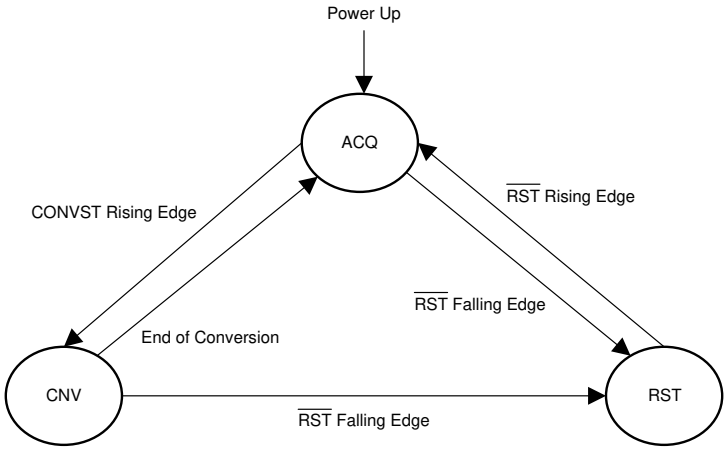


Figure 6-9. Device Functional States

6.4.1 RST State

The $\overline{\text{RST}}$ pin is an asynchronous digital input for the device. To enter RST state, the host controller pulls the $\overline{\text{RST}}$ pin low and keeps the pin low for the t_{wl_RST} duration (as specified in the *Timing Requirements* table).

In RST state, all configuration registers (see the *Register Maps* section) are reset to the default values, the RVS pin remains low, and the SDO-x pins are Hi-Z.

To exit RST state, the host controller pulls the $\overline{\text{RST}}$ pin high, with CONVST and SCLK held low and $\overline{\text{CS}}$ held high, as shown in Figure 6-10. After a delay of t_{d_rst}, the device enters ACQ state and the RVS pin goes high.

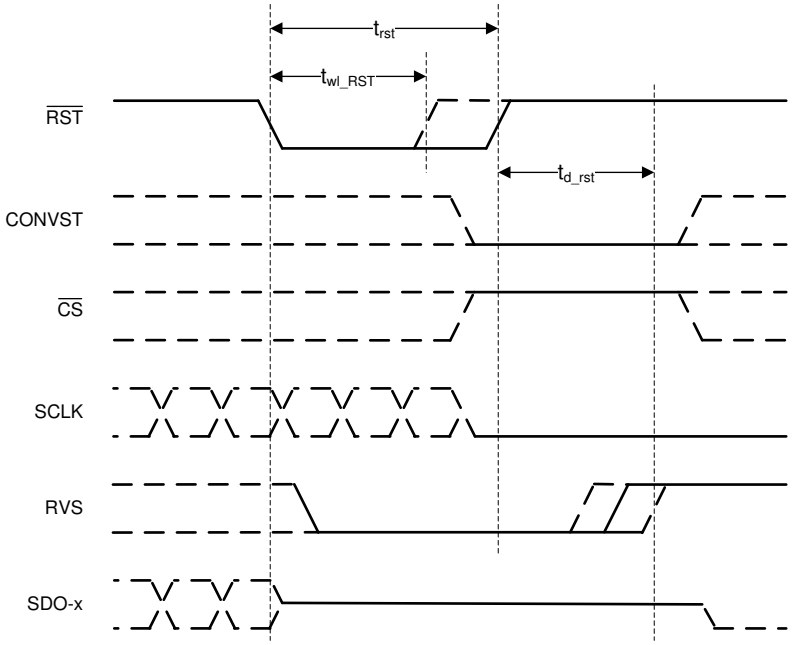


Figure 6-10. Asynchronous Reset

To operate the device in either ACQ or CNV state, $\overline{\text{RST}}$ must be held high. With $\overline{\text{RST}}$ held high, transitions on the CONVST pin determine the functional state of the device.

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Figure 6-11 shows a typical conversion process. The internal ADCST signal goes low during conversion and goes high at the end of conversion. With $\overline{CS}$ held high, RVS reflects the status of ADCST.

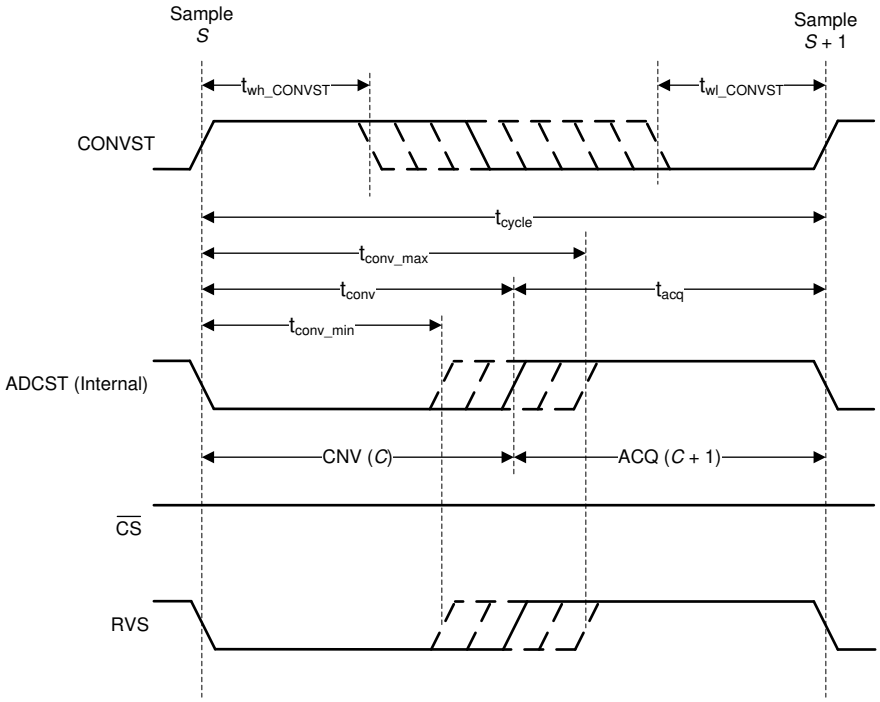


Figure 6-11. Typical Conversion Process

6.4.2 ACQ State

In ACQ state, the device acquires the analog input signal. The device enters ACQ state at power-up, when coming out of power down (See the PD Control section), after any asynchronous reset, and at the end of every conversion.

An $\overline{RST}$ falling edge takes the device from ACQ state to RST state. A CONVST rising edge takes the device from ACQ state to CNV state.

6.4.3 CNV State

The device moves from ACQ state to CNV state on a rising edge of the CONVST pin. The conversion process uses an internal clock. The device ignores any further transitions on the CONVST signal until the ongoing conversion is complete (that is, during the time interval of t_{conv}).

At the end of conversion, the device enters ACQ state. The cycle time for the device is given by Equation 5:

$$t_{cycle\text{-}min} = t_{conv} + t_{acq\text{-}min} \quad (5)$$

Note

The conversion time, t_{conv}, varies within the specified limits of t_{conv_min} and t_{conv_max} (as specified in the *Switching Characteristics* table). After initiating a conversion, the host controller must monitor for a low-to-high transition on the RVS pin or wait for the t_{conv_max} duration to elapse before initiating a new operation (data transfer or conversion). If RVS is not monitored, substitute t_{conv} in Equation 5 with t_{conv_max}.

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6.5 Programming

This device family features nine configuration registers (as described in the *Register Maps* section). To access the internal configuration registers, these devices support the commands listed in Table 6-2.

Table 6-2. Supported Commands

B[21:17]	B[16:8]	B[7:0]	COMMAND ACRONYM	COMMAND DESCRIPTION
00000	000000000	00000000	NOP	No operation
10000	<9-bit address>	<8-bit unmasked bits>	CLR_BITS	Clear <8-bit unmasked bits> from <9-bit address>
10001	<9-bit address>	00000000	RD_REG	Read contents from the <9-bit address>
10010	<9-bit address>	<8-bit data>	WR_REG	Write <8-bit data> to the <9-bit address>
10011	<9-bit address>	<8-bit unmasked bits>	SET_BITS	Set <8-bit unmasked bits> from <9-bit address>
11111	111111111	11111111	NOP	No operation
Remaining combinations	xxxxxxxxx	xxxxxxxx	Reserved	These commands are reserved and treated by the device as no operation

These devices support two types of data transfer operations: *data write* (the host controller configures the device), and *data read* (the host controller reads data from the device).

Any data write to the device is always synchronous to the external clock provided on the SCLK pin. The WR_REG command writes the 8-bit data into the 9-bit address specified in the command string. The CLR_BITS command clears the specified bits (identified by 1) at the 9-bit address (without affecting the other bits), and the SET_BITS command sets the specified bits (identified by 1) at the 9-bit address (without affecting the other bits).

The data read from the device can be synchronized to the same external clock or to an internal clock of the device by programming the configuration registers (see the *Data Transfer Protocols* section for details).

6.5.1 Output Data Word

In any data transfer frame, the contents of an internal, 22-bit, output data word are shifted out on the SDO pins. The D[21:6] bits of the 22-bit output data word for any frame *F* + 1, are determined by:

- Value of the DATA_VAL bit applicable to frame *F* + 1 (see the DATA_CNTL register)
- The command issued in frame *F*

If a valid RD_REG command is executed in frame *F*, then the D[21:14] bits in frame *F* + 1 reflect the contents of the selected register, and the D[13:0] bits are zeros.

If the DATA_VAL bit for frame *F* + 1 is set to 1, then the D[21:6] bits in frame *F* + 1 are replaced by the DATA_PATN[15:0] bits.

For all other combinations, the D[21:6] bits for frame *F* + 1 are the latest conversion result.

Figure 6-12 shows the output data word. Figure 6-13 shows further details of the parity computation unit illustrated in Figure 6-12.

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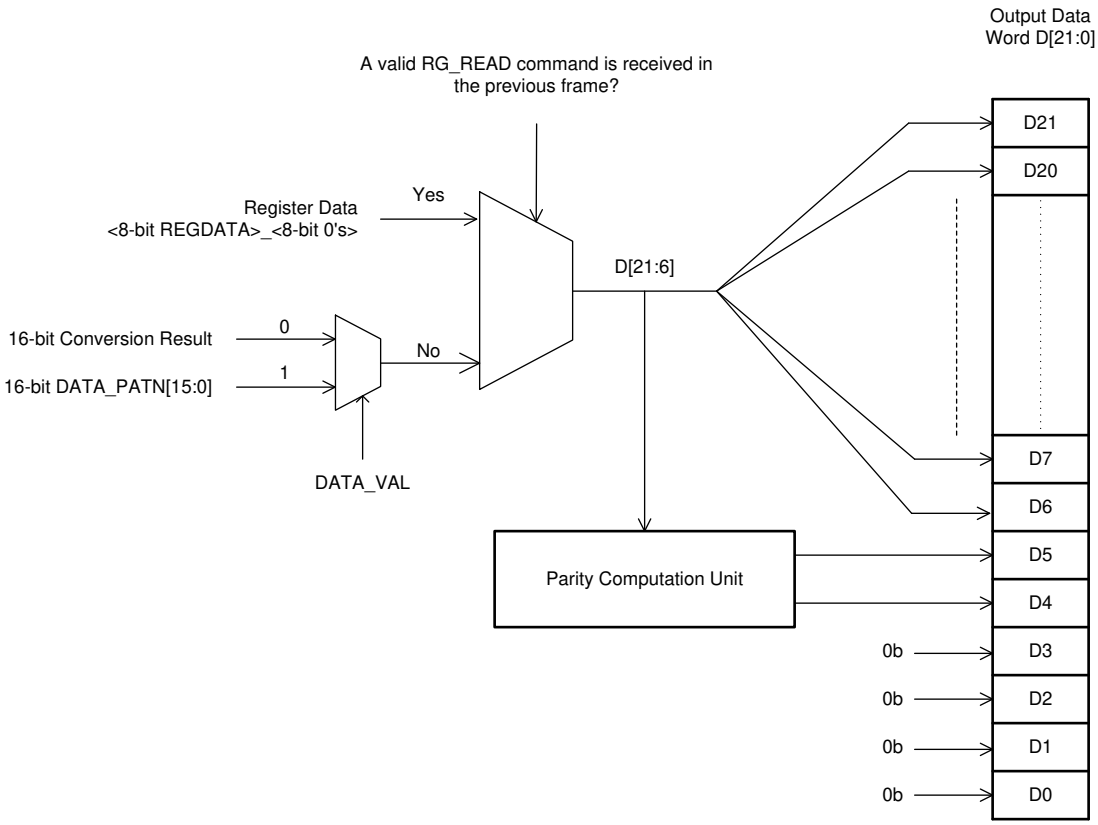


Figure 6-12. Output Data Word (D[21:0])

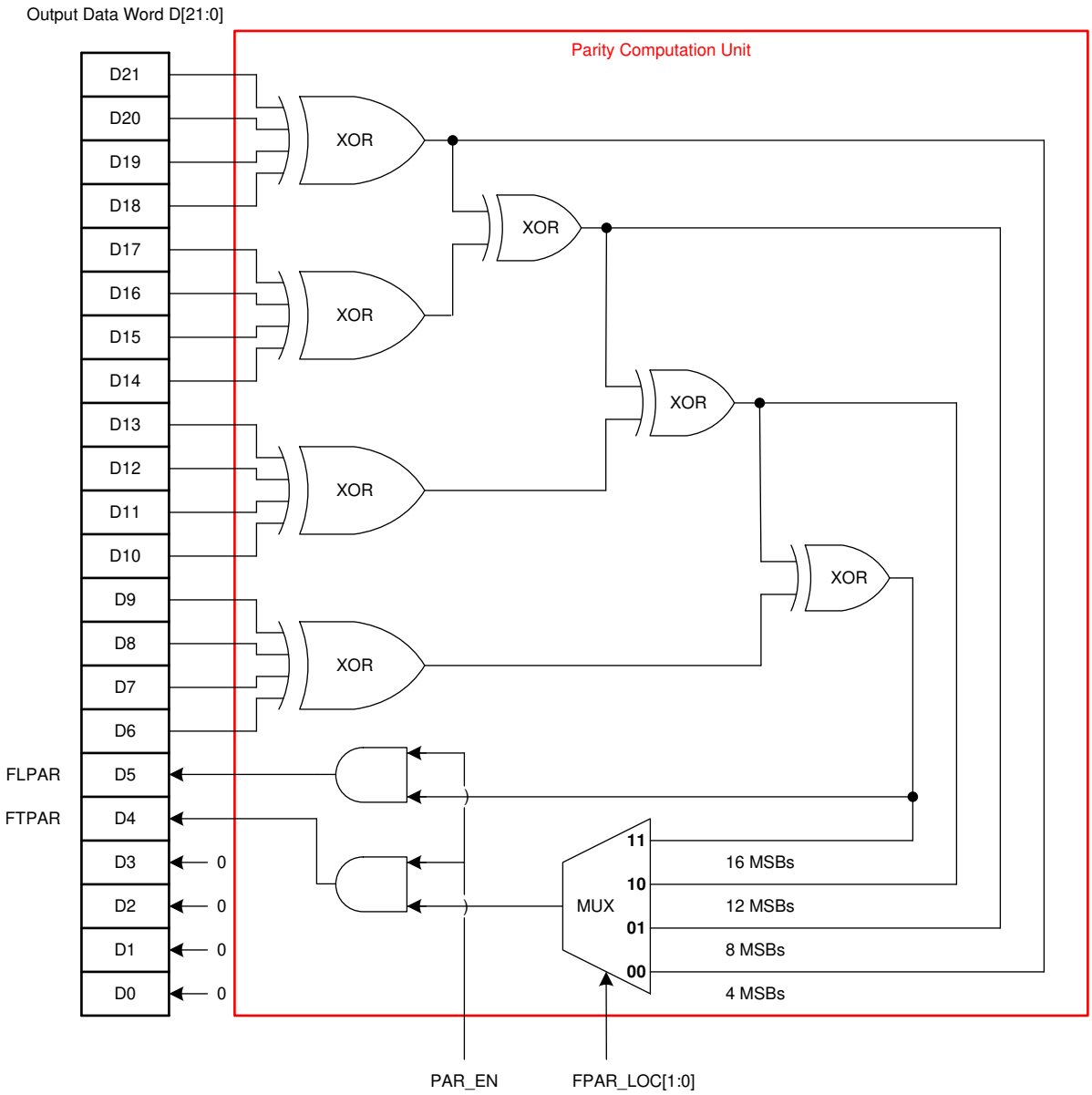


Figure 6-13. Parity Bits Computation

With the PAR_EN bit set to 0, the D[5] and D[4] bits of the output data word are set to 0 (default configuration).

When the PAR_EN bit is set to 1, the device calculates the parity bits (FLPAR and FTPAR) and appends them as bits D[5] and D[4].

- FLPAR is the even parity calculated on bits D[21:6].
- FTPAR is the even parity calculated on the bits defined by FPAR_LOC[1:0].

See the DATA_CNTL register for more details on the FPAR_LOC[1:0] bit settings. Bits D[3:0] are set to 0000b.

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6.5.2 Data Transfer Frame

A data transfer frame between the device and the host controller is bounded between a $\overline{CS}$ falling edge and the subsequent $\overline{CS}$ rising edge. The host controller can initiate a data transfer frame (as shown in Figure 6-14) at any time irrespective of the status of the CONVST signal; however, the data read during such a data transfer frame is a function of relative timing between the CONVST and $\overline{CS}$ signals.

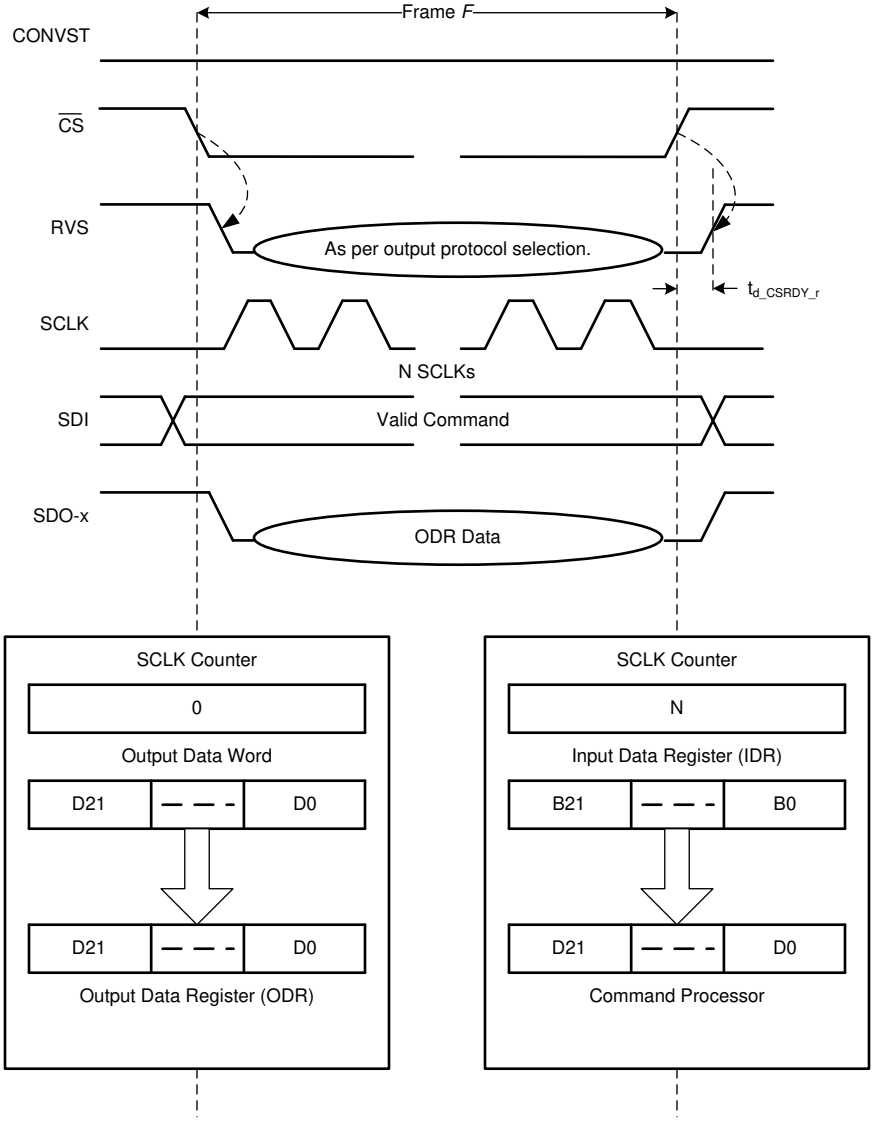


Figure 6-14. Data Transfer Frame

For this discussion, assume that the CONVST signal remains low.

A typical data transfer frame *F* follows this order:

1. The host controller pulls $\overline{CS}$ low to initiate a data transfer frame. On the $\overline{CS}$ falling edge:
   - RVS goes low, indicating the beginning of the data transfer frame.
   - The SCLK counter is reset to 0.
   - The device takes control of the data bus. As shown in Figure 6-14, the 22-bit contents of the output data word (see Figure 6-12) are loaded in to the 22-bit output data register (ODR; see Figure 6-8).
   - The 22-bit input data register (IDR; see Figure 6-8) is reset to 000000h, corresponding to a NOP command.

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2. During the frame, the host controller provides clocks on the SCLK pin. Inside the device:
   - For each SCLK capture edge, the SCLK counter is incremented and the data bit received on the SDI pin is shifted in to the IDR.
   - For each launch edge of the output clock (SCLK in this case), ODR data are shifted out on the selected SDO-x pins.
   - The status of the RVS pin depends on the output protocol selection (see the *Protocols for Reading From the Device* section).
3. The host controller pulls $\overline{CS}$ high to end the data transfer frame. On the $\overline{CS}$ rising edge:
   - The SDO-x pins go to Hi-Z.
   - RVS goes high (after a delay of $t_{d_CSRDY_r}$).
   - As illustrated in Figure 6-14, the 22-bit contents of the IDR are transferred to the command processor (see Figure 6-8) for decoding and further action.

After pulling $\overline{CS}$ high, the host controller monitors for a low-to-high transition on the RVS pin, or waits for the $t_{d_CSRDY_r}$ time (see the *Switching Characteristics* table) to elapse before initiating a new operation (data transfer or conversion). The delay, $t_{d_CSRDY_r}$, for any data transfer frame *F* varies based on the data transfer operation executed in frame *F*.

At the end of data transfer frame *F*:

- If the SCLK counter is < 22, then the IDR captured less than 22 bits from the SDI. In this case, the device treats frame *F* as a *short command frame*. At the end of a short command frame, the IDR is not updated and the device treats the frame as a no operation (NOP) command.
- If the SCLK counter = 22, then the IDR captured exactly 22 bits from SDI. In this case, the device treats the frame *F* as a *optimal command frame*. At the end of an optimal command frame, the command processor decodes the 22-bit contents of the IDR as a valid command word.
- If the SCLK counter > 22, then the IDR captured more than 22 bits from the SDI; however, only the *last 22 bits* are retained. In this case, the device treats frame F as a *long command frame*. At the end of a long command frame, the command processor treats the 22-bit contents of the IDR as a valid command word. There is no restriction on the maximum number of clocks that can be provided within any data transfer frame *F*. However, as explained above, make sure that the last 22 bits shifted into the device before the $\overline{CS}$ rising edge constitute the desired command.

In a short command frame, the write operation to the device is invalidated; however, the output data bits transferred during the short command frame are still valid output data. Therefore, the host controller can use such shorter data transfer frames to read only the required number of MSB bits from the 22-bit output data word. As shown in Figure 6-12, an *optimal read frame* for the ADS892xB devices must read only the 16 MSB bits of the output data word. The length of an optimal read frame depends on the output protocol selection; see the *Protocols for Reading From the Device* section for more details.

Note

The previous example shows data-read and data-write operations synchronous to the external clock provided on the SCLK pin.

However, the device also supports data read operation synchronous to the internal clock; see the *Protocols for Reading From the Device* section for more details. In this case, while the ODR contents are shifted on the SDO (or SDOs) on the launch edge of the internal clock, the device continues to capture the SDI data into the IDR (and increment the SCLK counter) on SCLK capture edges.

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6.5.3 Interleaving Conversion Cycles and Data Transfer Frames

The host controller operates the device at the desired throughput by interleaving the conversion cycles and the data transfer frames.

The cycle time of the device, t_{cycle}, is the time difference between two consecutive CONVST rising edges provided by the host controller. The response time of the device, t_{resp}, is the time difference between the host controller initiating conversion *C*, and the host controller receiving the complete result for conversion *C*.

Figure 6-15 shows three conversion cycles: *C*, *C* + 1, and *C* + 2. Conversion *C* is initiated by a CONVST rising edge at time t = 0, and the conversion result becomes available for data transfer at t_{conv}. However, this result is loaded into the ODR only on the subsequent $\overline{CS}$ falling edge. This $\overline{CS}$ falling edge must be provided before the completion of conversion *C* + 1 (that is, before t_{cycle} + t_{conv}).

To achieve the rated performance specifications, the host controller must make sure that no digital signals toggle during the quiet acquisition time (t_{qt_acq}) and quiet aperture time (t_{d_cnvcap}). Any noise during t_{d_cnvcap} can negatively affect the result of the ongoing conversion, whereas any noise during t_{qt_acq} can negatively affect the result of the subsequent conversion.

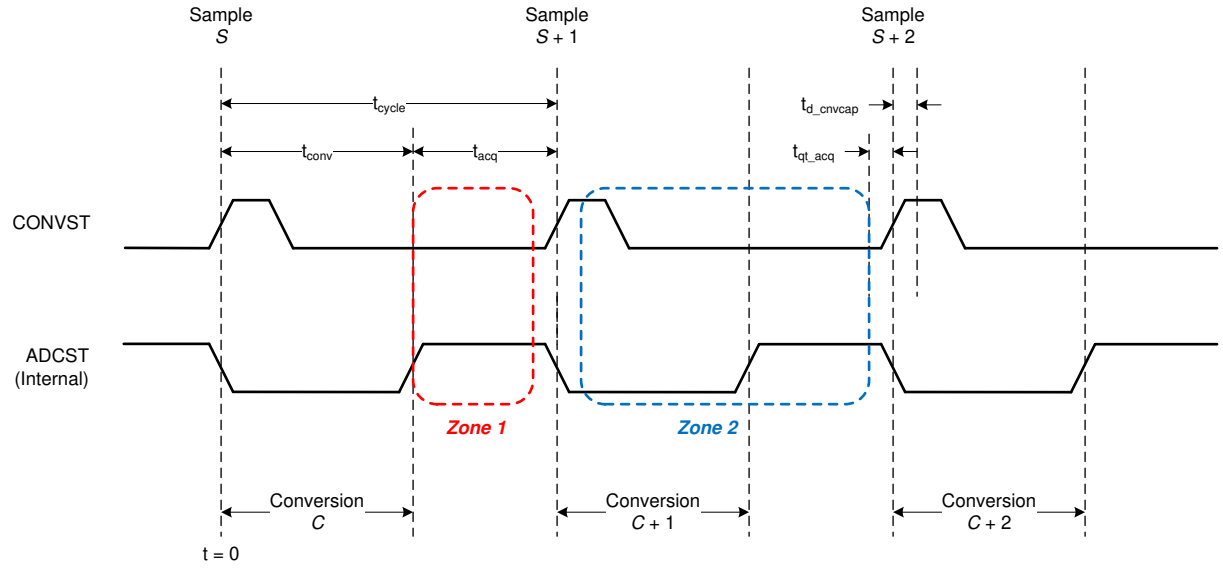


Figure 6-15. Data Transfer Zones

This architecture allows for two distinct time zones (zone 1 and zone 2) to transfer data for each conversion. Zone 1 and zone 2 for conversion *C* are defined in Table 6-3.

Table 6-3. Data Transfer Zones Timing

ZONE	STARTING TIME	ENDING TIME
Zone 1 for conversion *C*	t_{conv}	$t_{cycle} - t_{qt_aq}$
Zone 2 for conversion *C*	$t_{cycle} + t_{d_cn\ vcap}$	$t_{cycle} + t_{cycle} - t_{qt_acq}$

The response time includes the conversion time and the data transfer time, and thus is a function of the selected data transfer zone.

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Figure 6-16 and Figure 6-17 illustrate interleaving of three conversion cycles (*C*, *C* + 1, and *C* + 2) with three data transfer frames (*F*, *F* + 1, and *F* + 2) in zone 1 and in zone 2, respectively.

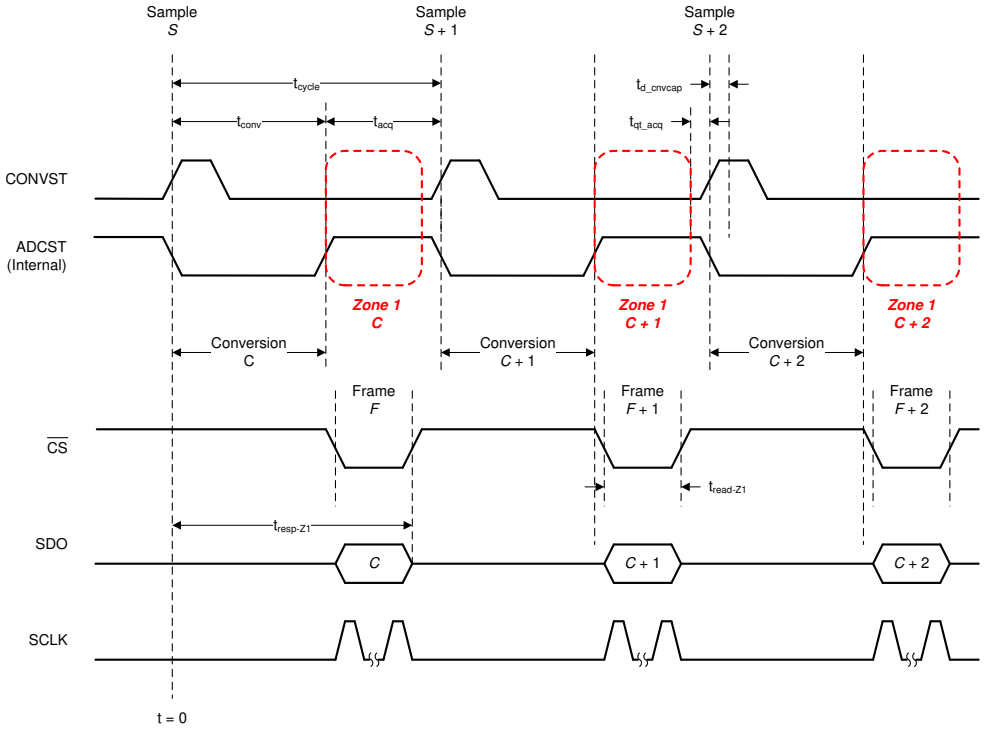


Figure 6-16. Zone 1 Data Transfer

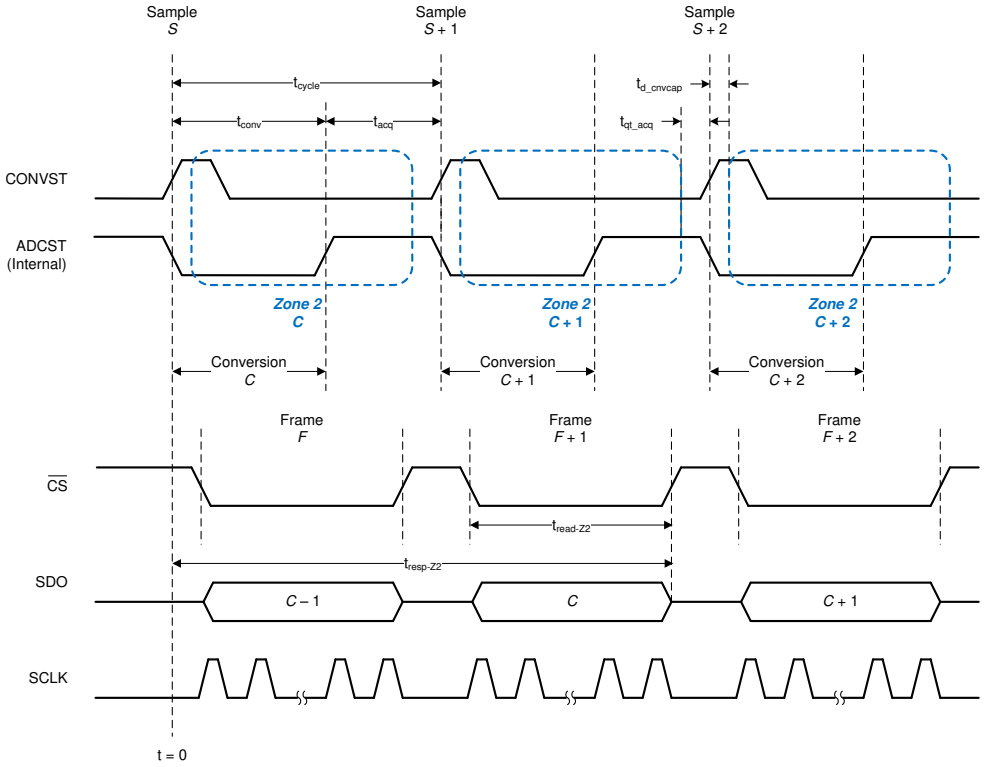


Figure 6-17. Zone 2 Data Transfer

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To achieve cycle time t_{cycle}, the read time in zone 1 is given by Equation 6:

$$t_{read\text{-}Z1} \leq t_{cycle} - t_{conv} - t_{qt_acq} \quad (6)$$

For an optimal data transfer frame, Equation 6 results in an SCLK frequency given by Equation 7:

$$f_{SCLK} \geq \frac{16}{t_{read\text{-}Z1}} \quad (7)$$

Then, the zone 1 data transfer achieves a response time defined by Equation 8:

$$t_{resp\text{-}Z1\text{-}min} = t_{conv} + t_{read\text{-}Z1} \quad (8)$$

At lower SCLK speeds, $t_{read\text{-}Z1}$ increases, resulting in slower response times and higher cycle times.

To achieve the same cycle time, t_{cycle}, the read time in zone 2 is given by Equation 9:

$$t_{read\text{-}Z2} \leq t_{cycle} - t_{d_cnvcap} - t_{qt_acq} \quad (9)$$

For an optimal data transfer frame, Equation 9 results in an SCLK frequency given by Equation 10:

$$f_{SCLK} \geq \frac{16}{t_{read\text{-}Z2}} \quad (10)$$

Then, the zone 2 data transfer achieves a response time defined by Equation 11:

$$t_{resp\text{-}Z2\text{-}min} = t_{cycle} + t_{d_cn\ vcap} + t_{read\text{-}Z2} \quad (11)$$

Any increase in $t_{read\text{-}Z2}$ increases response time and can increase cycle time.

For a given cycle time, the zone 1 data transfer clearly achieves faster response time, but also requires a higher SCLK speed (as evident from Equation 6, Equation 7, and Equation 8); whereas, the zone 2 data transfer clearly requires a lower SCLK speed but has a slower response time (as evident from Equation 9, Equation 10, and Equation 11).

Note

A data transfer frame can begin in zone 1, and then extend into zone 2; however, the host controller must make sure that no digital transitions occur during the t_{qt_acq} and t_{d_cnvcap} time intervals.

Note

For data transfer operations in zone 2 using the ADC-Clock-Master protocol (SDO_MODE[1:0] = 11b), the device supports only the external-clock-echo option (SSYNC_CLK_SEL[1:0] = 00b); see Table 6-9.

6.5.4 Data Transfer Protocols

This device family features a multiSPI digital interface that allows the host controller to operate at slower SCLK speeds and still achieve the required throughput and response time. The multiSPI digital interface module offers three options to reduce the SCLK speed required for data transfer:

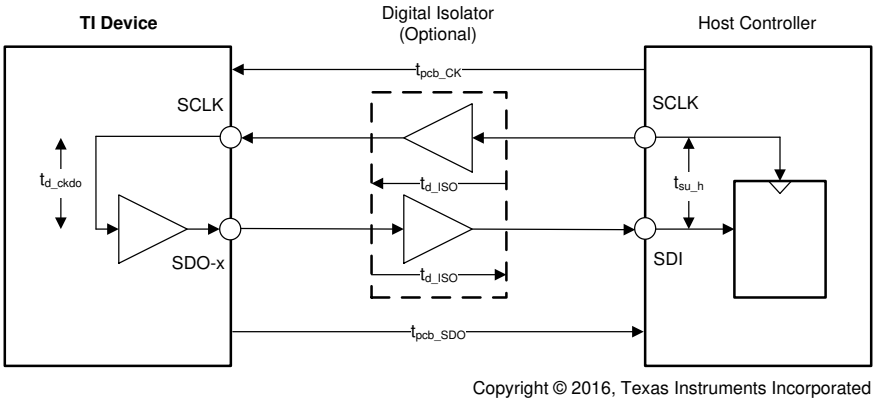
- Increase the width of the output data bus.
- Enable double data rate (DDR) transfer.
- Extended data transfer window, as shown in Figure 6-17.

These three options can be combined to achieve further reduction in SCLK speed.

There are various factors that limit the maximum SCLK frequency in a system.

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Figure 6-18 shows the delays in the communication channel between the host controller and the device in a typical serial communication.



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Figure 6-18. Delays in Serial Communication

For example, if t_{pcb_CK} and t_{pcb_SDO} are the delays introduced by the printed circuit board (PCB) traces for the serial clock and SDO signals, t_{d_CKDO} is the clock-to-data delay of the device, t_{d_ISO} is the propagation delay introduced by the digital isolator, and t_{su_h} is the setup time specification of the host controller, then the total delay in the path is given by Equation 12:

$$t_{d_total_serial} = t_{pcb_CK} + t_{d_iso} + t_{d_ckdo} + t_{d_iso} + t_{pcb_SDO} + t_{su_h} \quad (12)$$

In a standard SPI protocol, the host controller and the device launch and capture data bits on alternate SCLK edges. Therefore, the $t_{d_total_serial}$ delay must be kept to less than half of the SCLK duration. Equation 13 shows the fastest clock allowed by the SPI protocol:

$$f_{clk\text{-}SPI} \leq \frac{1}{2 \times t_{d_total\text{-}serial}} \quad (13)$$

Larger values of the $t_{d_total_serial}$ delay restricts the maximum SCLK speed for the SPI protocol, resulting in higher read and response times, and can possibly limit the throughput.

Figure 6-19 shows a delay (t_{d_delcap}) introduced in the capture path (inside the host controller).

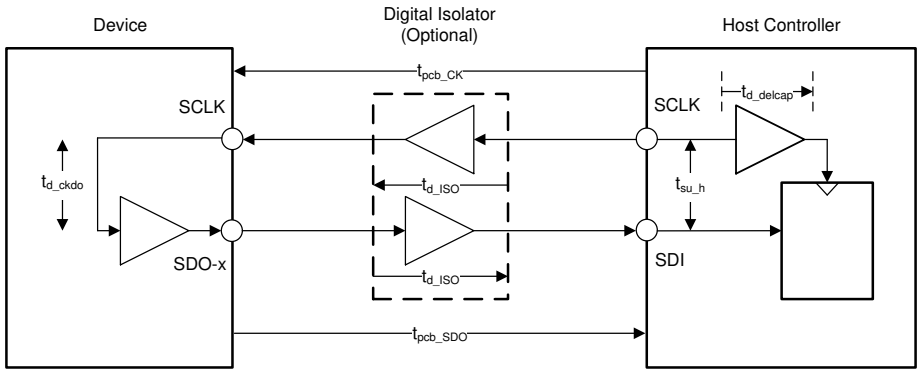


Figure 6-19. Delayed Capture

The total delay in the path modifies to Equation 14:

$$t_{d_total_serial} = t_{pcb_CK} + t_{d_iso} + t_{d_ckdo} + t_{d_iso} + t_{pcb_SDO} + t_{su_h} - t_{d_delcap} \quad (14)$$

This reduction in total delay allows the SPI protocol to operate at higher clock speeds.

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The multiSPI digital interface module offers two additional options to remove the restriction on the SCLK speed:

- Early data launch (EDL) mode of operation

  In EDL mode, the device launches the output data on SDO-x pin (or pins) half a clock earlier compared to the standard SPI protocol. Therefore, Equation 13 modifies to Equation 15:

$$f_{ck\text{-}SPI} \leq \frac{1}{t_{d_total\text{-}serial}} \quad (15)$$

  The reduction in total delay allows the serial interface to operate at higher clock speeds.
- ADC-Clock-Master (*source-synchronous*) mode of operation

  As illustrated in Figure 6-20, in ADC-Clock-Master mode, the device provides a synchronous output clock (on the RVS pin) along with the output data (on the SDO-x pins).

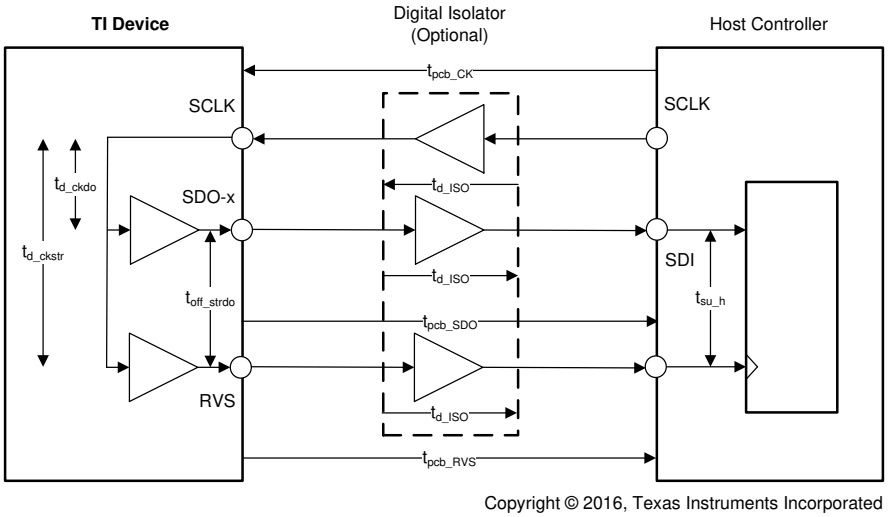


Figure 6-20. Delays in ADC-Clock-Master (Source-Synchronous) Mode

For negligible values of t_{off_STRDO}, the total delay in the path for a source-synchronous data transfer, is given by Equation 16:

$$t_{d_total_srcsync} = t_{pcb_RVS} - t_{pcb_SDO} + t_{su_h} \quad (16)$$

As shown by the difference between Equation 12 and Equation 16, using ADC-Clock-Master mode completely eliminates the effect of isolator delays (t_{d_ISO}) and clock-to-data delays (t_{d_CKDO}); typically, the largest contributors in the overall delay computation.

Furthermore, the actual values of t_{pcb_RVS} and t_{pcb_SDO} do not matter. In most cases, the $t_{d_total_srcsync}$ delay can be kept at a minimum by routing the RVS and SDO lines together on the PCB. Therefore, the ADC-Clock-Master mode allows the data transfer between the host controller and the device to operate at much higher SCLK speeds.

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6.5.4.1 Protocols for Configuring the Device

As shown in Table 6-4, the host controller can use any of the four legacy, SPI-compatible protocols (SPI-00S, SPI-01S, SPI-10S, or SPI-11S) to write data to the device.

Table 6-4. SPI Protocols for Configuring the Device

PROTOCOL	SCLK POLARITY (At $\overline{CS}$ Falling Edge)	SCLK PHASE (Capture Edge)	SDI_CNTL	SDO_CNTL	NO. OF SCLK (Optimal Command Frame)	TIMING DIAGRAM
SPI-00S	Low	Rising	00h	00h	22	Figure 6-21
SPI-01S	Low	Falling	01h	00h	22	Figure 6-22
SPI-10S	High	Falling	02h	00h	22	Figure 6-23
SPI-11S	High	Rising	03h	00h	22	Figure 6-24

At power-up or after coming out of any asynchronous reset, the device supports the SPI-00S protocol for data-read and data-write operations.

To select a different SPI-compatible protocol, program the SDI_MODE[1:0] bits in the SDI_CNTL register. This first write operation must adhere to the SPI-00S protocol. Any subsequent data transfer frames must adhere to the newly selected protocol.

Figure 6-21 to Figure 6-24 detail the four protocols using an optimal command frame; see the *Timing of Requirements* and Switching Characteristics tables for associated timing parameters.

Note

As explained in the *Data Transfer Frame* section, a valid write operation to the device requires a minimum of 22 SCLKs to be provided within a data transfer frame.

Any data write operation to the device must continue to follow the SPI-compatible protocol selected in the SDI_CNTL register, irrespective of the protocol selected for the data-read operation.

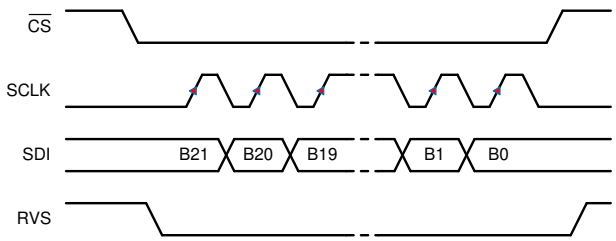


Figure 6-21. SPI-00S Protocol, Optimal Command Frame

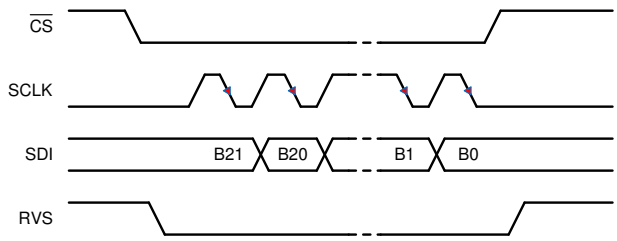


Figure 6-22. SPI-01S Protocol, Optimal Command Frame

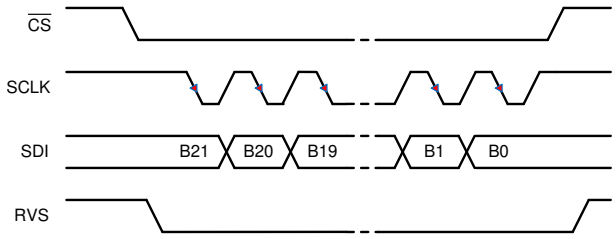


Figure 6-23. SPI-10S Protocol, Optimal Command Frame

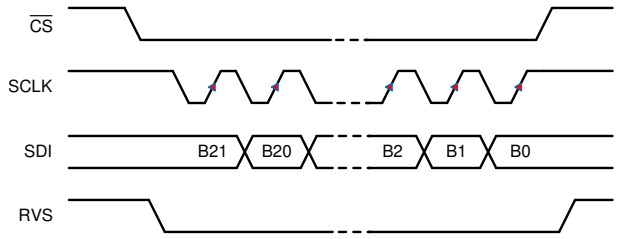


Figure 6-24. SPI-11S Protocol, Optimal Command Frame

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6.5.4.2 Protocols for Reading From the Device

The protocols for the data-read operation can be broadly classified into three categories:

1. Legacy, SPI-compatible (SPI-xy-S) protocol
2. SPI-compatible protocols with bus width options (SPI-xy-D and SPI-xy-Q)
3. Source-synchronous (SRC) protocols

6.5.4.2.1 Legacy, SPI-Compatible (SYS-xy-S) Protocols

As shown in Table 6-5, the host controller can use any of the four legacy, SPI-compatible protocols (SPI-00S, SPI-01S, SPI-10S, or SPI-11S) to read data from the device.

Table 6-5. SPI Protocols for Reading From the Device

PROTOCOL	SCLK POLARITY (At $\overline{CS}$ Falling Edge)	SCLK PHASE (Capture Edge)	MSB BIT LAUNCH EDGE	SDI_CNTL	SDO_CNTL	NO. OF SCLK (Optimal Read Frame)	TIMING DIAGRAM
SPI-00S	Low	Rising	$\overline{CS}$ falling	00h	00h	16	Figure 6-25
SPI-01S	Low	Falling	1st SCLK rising	01h	00h	16	Figure 6-26
SPI-10S	High	Falling	$\overline{CS}$ falling	02h	00h	16	Figure 6-27
SPI-11S	High	Rising	1st SCLK falling	03h	00h	16	Figure 6-28

At power-up or after coming out of any asynchronous reset, the device supports the SPI-00S protocol for data-read and data-write operations. To select a different SPI-compatible protocol for both the data transfer operations:

1. Program the SDI_MODE[1:0] bits in the SDI_CNTL register. This first write operation must adhere to the SPI-00S protocol. Any subsequent data transfer frames must adhere to the newly selected protocol.
2. Set the SDO_MODE[1:0] bits = 00b in the SDO_CNTL register.

Figure 6-25 to Figure 6-28 explain the details of the four protocols using an optimal command frame to read all 22 bits of the output data word. Table 6-5 shows the number of SCLK required in an optimal read frame for the different output protocol selections.

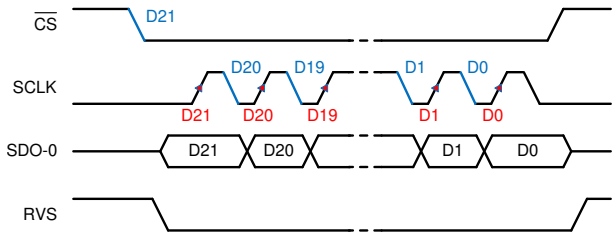


Figure 6-25. SPI-00S Protocol, 22 SCLKs

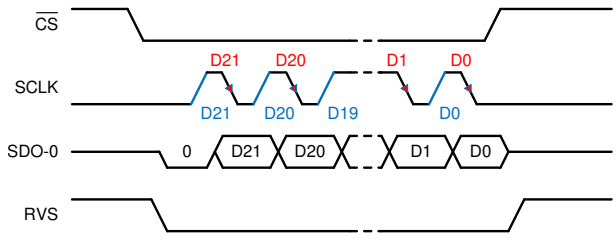


Figure 6-26. SPI-01S Protocol, 22 SCLKs

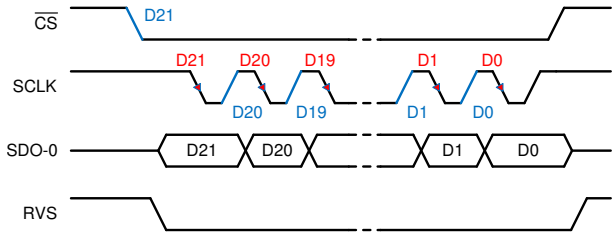


Figure 6-27. SPI-10S Protocol, 22 SCLKs

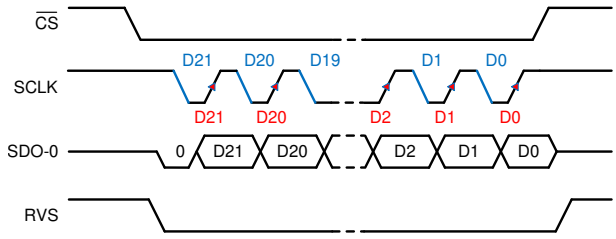


Figure 6-28. SPI-11S Protocol, 22 SCLKs

For SDI_MODE[1:0] = 00b or 10b, the device supports an *Early Data Launch* (EDL) option. Set SDO_MODE[1:0] = 01b in the SDO_CNTL register to enable the feature (see Table 6-6). Setting SDO_MODE[1:0] = 01b has no effect if SDI_MODE[1:0] = 01b or 11b.

Table 6-6. SPI Protocols with Early Data Launch

PROTOCOL	SCLK POLARITY (At $\overline{CS}$ Falling Edge)	SCLK PHASE (Capture Edge)	MSB BIT LAUNCH EDGE	SDI_CNTL	SDO_CNTL	NO. OF SCLK (Optimal Read Frame)	TIMING DIAGRAM
SPI-00S-EDL	Low	Rising	$\overline{CS}$ falling	00h	01h	16	Figure 6-25
SPI-10S-EDL	High	Falling	$\overline{CS}$ falling	02h	01h	16	Figure 6-27

As shown in Figure 6-29, and Figure 6-30, the device launches the output data bit on the SDO-0 pin half clock earlier compared to the standard SPI protocol.

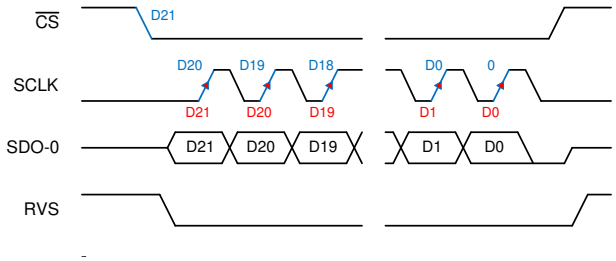


Figure 6-29. SPI-00S-EDL Protocol, 22 SCLKs

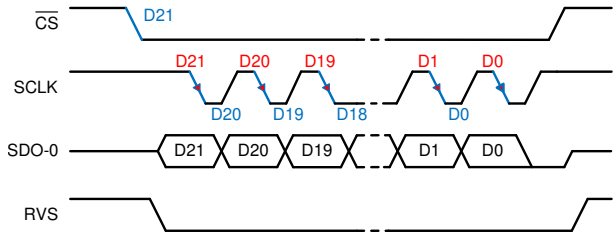


Figure 6-30. SPI-10S-EDL Protocol, 22 SCLKs

When using these SPI-compatible protocols, the RVS output remains low throughout the data transfer frame; see the *Timing Requirements* and Switching Characteristics tables for associated timing parameters.

With SDO_CNTL[7:0] = 00h or 01h, if the host controller uses a long data transfer frame, the device exhibits daisy-chain operation (see the *Multiple Devices: Daisy-Chain Topology* section).

Note

Use SPI-compatible protocols to execute the RD_REG, WR_REG, CLR_BITS, and SET_BITS commands specified in Table 6-2.

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6.5.4.2.2 SPI-Compatible Protocols with Bus Width Options

The device provides an option to increase the SDO bus width from one bit (default, single SDO) to two bits (dual SDO) or four bits (quad SDO) when operating with any of the four legacy, SPI-compatible protocols.

Set the SDO_WIDTH[1:0] bits in the SDO_CNTL register to select the SDO bus width. The SCLK launch edge depends on the SPI protocol selection (as shown in Table 6-7).

Table 6-7. SPI-Compatible Protocols with Bus Width Options

PROTOCOL	SCLK POLARITY (At $\overline{CS}$ Falling Edge)	SCLK PHASE (Capture Edge)	MSB BIT LAUNCH EDGE	SDI_CNTL	SDO_CNTL	#SCLK (Optimal Read Frame)	TIMING DIAGRAM
SPI-00D	Low	Rising	$\overline{CS}$ falling	00h	08h	8	Figure 6-31
SPI-01D	Low	Falling	First SCLK rising	01h	08h	8	Figure 6-32
SPI-10D	High	Falling	$\overline{CS}$ falling	02h	08h	8	Figure 6-33
SPI-11D	High	Rising	First SCLK falling	03h	08h	8	Figure 6-34
SPI-00-Q	Low	Rising	$\overline{CS}$ falling	00h	0Ch	4	Figure 6-35
SPI-01-Q	Low	Falling	First SCLK rising	01h	0Ch	4	Figure 6-36
SPI-10-Q	High	Falling	$\overline{CS}$ falling	02h	0Ch	4	Figure 6-37
SPI-11-Q	High	Rising	First SCLK falling	03h	0Ch	4	Figure 6-38

In dual-SDO mode (SDO_WIDTH[1:0] = 10b), two bits of data are launched on the two SDO pins (SDO-0 and SDO-1) on every SCLK launch edge.

In quad-SDO mode (SDO_WIDTH[1:0] = 11b), four bits of data are launched on the four SDO pins (SDO-0, SDO-1, SDO-2, and SDO-3) on every SCLK launch edge.

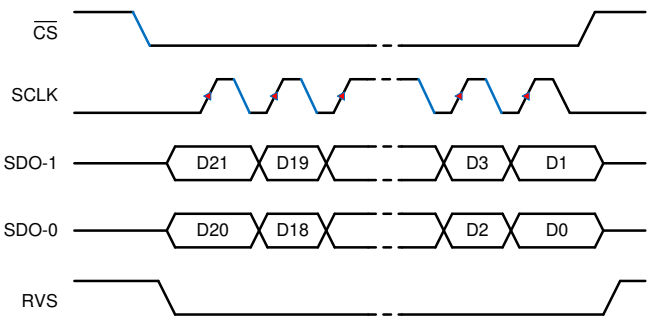


Figure 6-31. SPI-00D Protocol

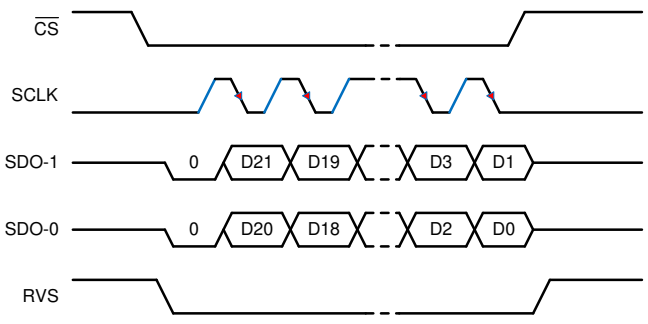


Figure 6-32. SPI-01D Protocol

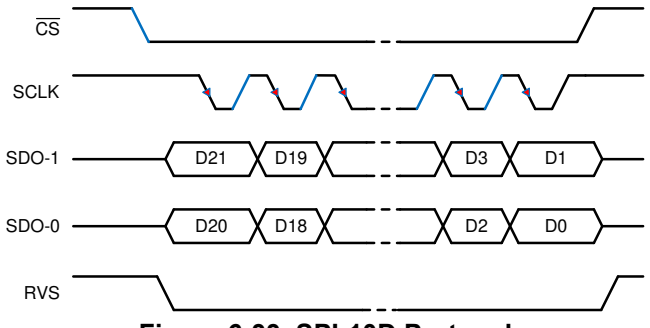


Figure 6-33. SPI-10D Protocol

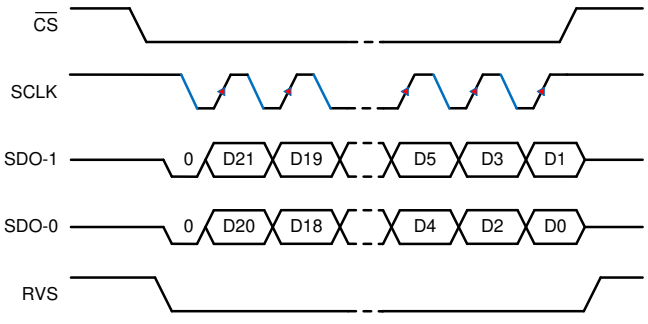


Figure 6-34. SPI-11D Protocol

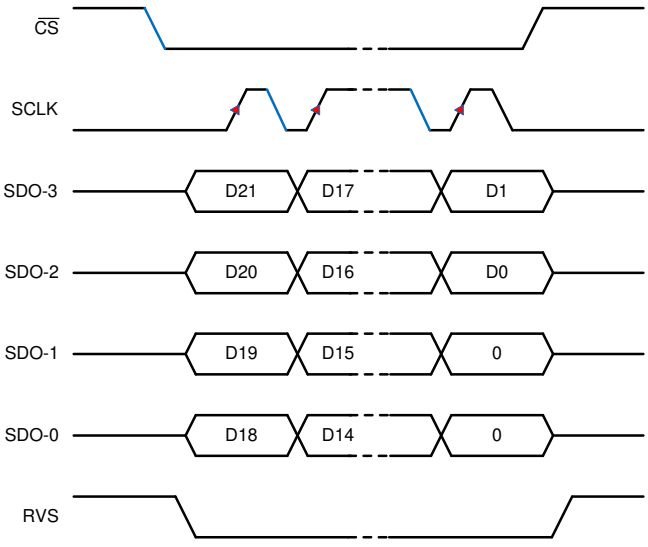


Figure 6-35. SPI-00-Q Protocol

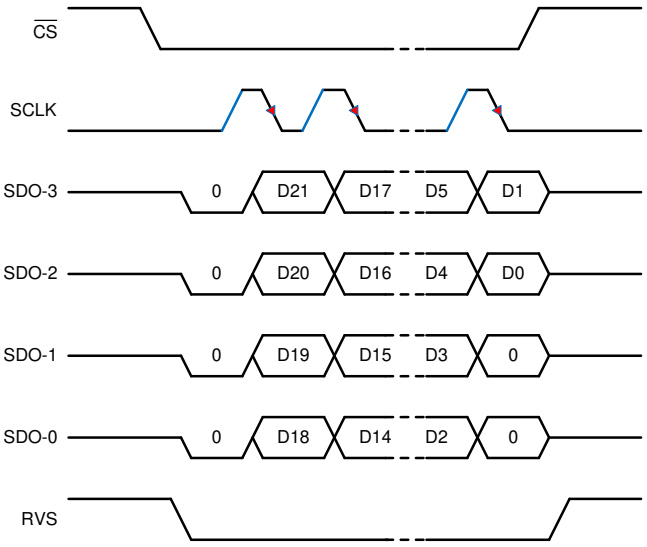


Figure 6-36. SPI-01-Q Protocol

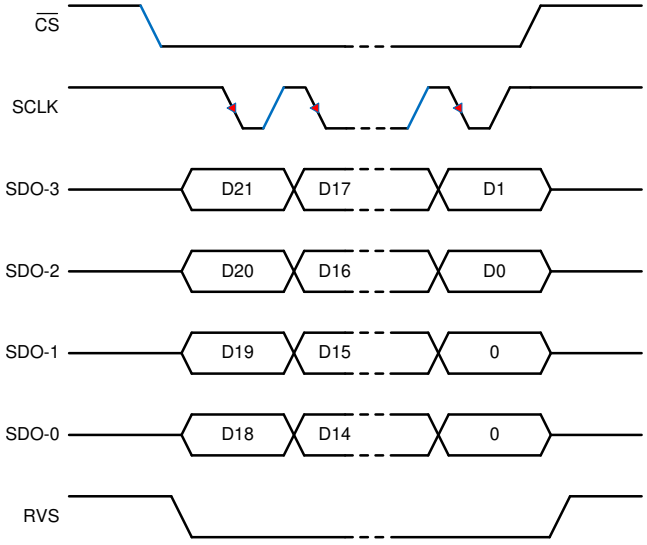


Figure 6-37. SPI-10-Q Protocol

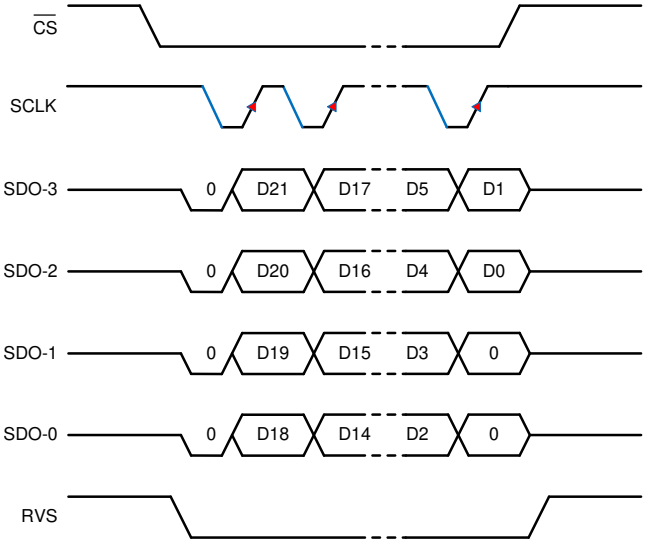


Figure 6-38. SPI-11-Q Protocol

For SDI_MODE[1:0] = 00b or 10b, the device supports an early data launch (EDL) option. Set SDO_MODE[1:0] = 01b in the SDO_CNTL register to enable the feature (see Table 6-8). Setting SDO_MODE[1:0] = 01b has no effect if SDI_MODE[1:0] = 01b or 11b.

Table 6-8. SPI Protocols with Early Data Launch

PROTOCOL	SCLK POLARITY (At $\overline{CS}$ Falling Edge)	SCLK PHASE (Capture Edge)	MSB BIT LAUNCH EDGE	SDI_CNTL	SDO_CNTL	NO. OF SCLK (Optimal Read Frame)	TIMING DIAGRAM
SPI-00D-EDL	Low	Rising	$\overline{CS}$ falling	00h	09h	8	Figure 6-31
SPI-10D-EDL	High	Falling	$\overline{CS}$ falling	02h	09h	8	Figure 6-33
SPI-00-Q-EDL	Low	Rising	$\overline{CS}$ falling	00h	0Dh	4	Figure 6-35
SPI-10-Q-EDL	High	Falling	$\overline{CS}$ falling	02h	0Dh	4	Figure 6-37

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As shown in Figure 6-29, and Figure 6-30, the device launches the output data bits on the SDO-x pins half clock earlier compared to the standard SPI protocol.

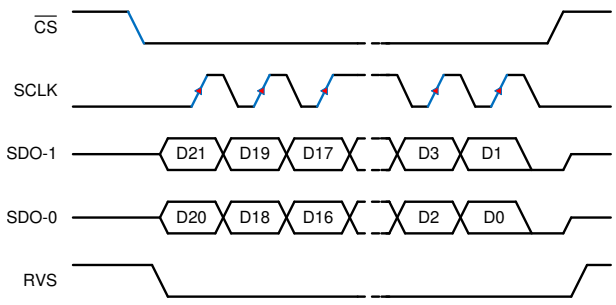


Figure 6-39. SPI-00D-EDL Protocol

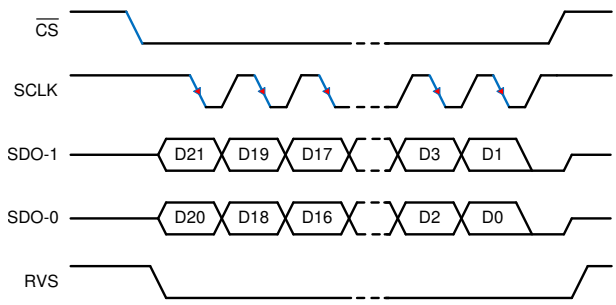


Figure 6-40. SPI-10D-EDL Protocol

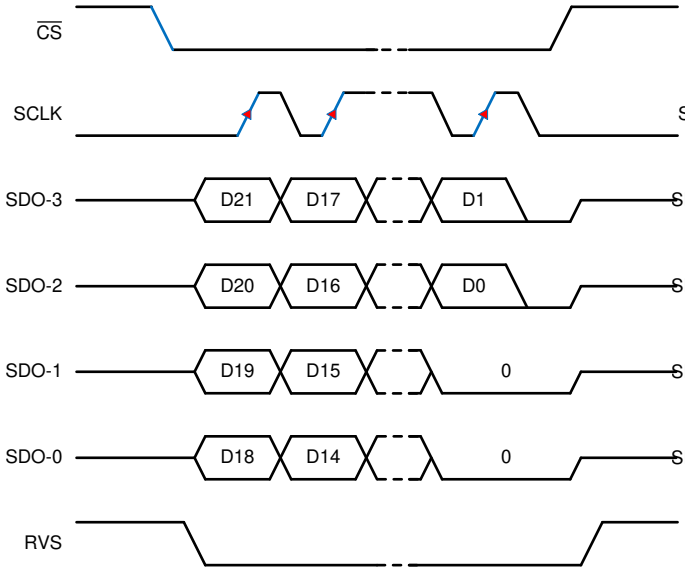


Figure 6-41. SPI-00-Q-EDL Protocol

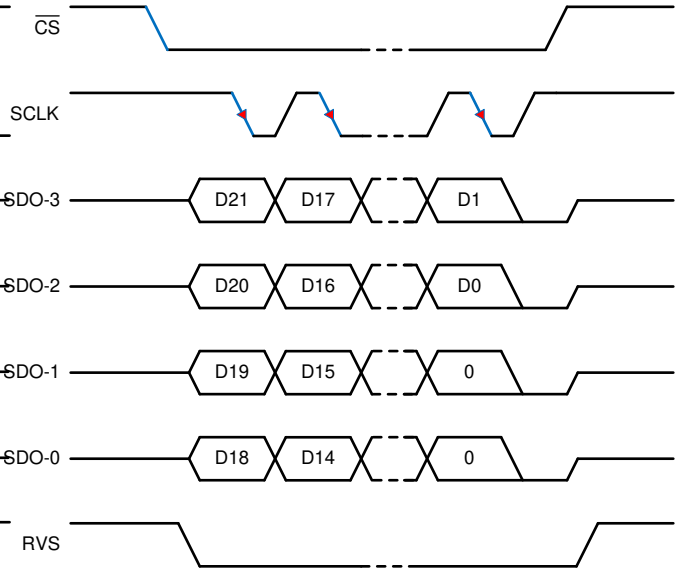


Figure 6-42. SPI-10-Q-EDL Protocol

When using any of the SPI-compatible protocols, the RVS output remains low throughout the data transfer frame; see the *Timing Requirements* and Switching Characteristics tables for associated timing parameters.

Figure 6-31 to Figure 6-42 illustrate how the wider data bus allows the host controller to read all 22 bits of the output data word using shorter data transfer frames. Table 6-7 and Table 6-8 show the number of SCLK required in an optimal read frame for the different output protocol selections.

Note

With SDO_CNTL[7:0] ≠ 00h or 01h, a long data transfer frame does not result in daisy-chain operation. On SDO pin (or pins), the 22 bits of output data word are followed by zeros.

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6.5.4.2.3 Source-Synchronous (SRC) Protocols

As described in the *Data Transfer Protocols* section, the multiSPI digital interface supports an ADC-Clock-Master or a *source-synchronous* mode of data transfer between the device and host controller. In this mode, the device provides an output clock that is synchronous with the output data. Furthermore, the host controller can also select the output clock source, data bus width, and data transfer rate.

6.5.4.2.3.1 Output Clock Source Options with SRC Protocols

In all SRC protocols, the RVS pin provides the output clock. The device allows this output clock to be synchronous to either the external clock provided on the SCLK pin or to the internal clock of the device. Furthermore, this internal clock can be divided by a factor of two or four to lower the data rates.

As shown in Figure 6-43, set the SSYNC_CLK_SEL[1:0] bits in the SDO_CNTL register to select the output clock source.

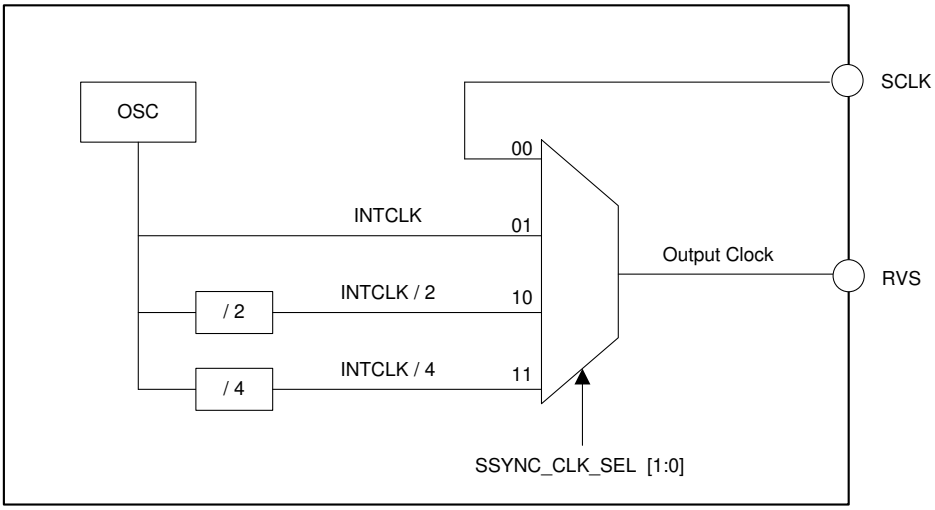


Figure 6-43. Output Clock Source Options With SRC Protocols

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6.5.4.2.3.2 Bus Width Options With SRC Protocols

The device provides an option to increase the SDO bus width from one bit (default, single SDO) to two bits (dual SDO) or to four bits (quad SDO) when operating with any of the SRC protocols. Set the SDO_WIDTH[1:0] bits in the SDO_CNTL register to select the SDO bus width.

In dual-SDO mode (SDO_WIDTH[1:0] = 10b), two bits of data are launched on the two SDO pins (SDO-0 and SDO-1) on every SCLK rising edge.

In quad-SDO mode (SDO_WIDTH[1:0] = 11b), four bits of data are launched on the four SDO pins (SDO-0, SDO-1, SDO-2, and SDO-3) on every SCLK rising edge.

6.5.4.2.3.3 Output Data Rate Options With SRC Protocols

The device provides an option to transfer the data to the host controller at a single data rate (default, SDR) or at a double data rate (DDR). Set the DATA_RATE bit in the SDO_CNTL register to select the data transfer rate.

In SDR mode (DATA_RATE = 0b), the RVS pin toggles from low to high, and the output data bits are launched on the SDO pins on the output clock rising edge.

In DDR mode (DTA_RATE = 1b), the RVS pin toggles (from low-to-high or high-to-low), and the output data bits are launched on the SDO pins on every output clock edge, starting with the first rising edge.

The device supports all 24 combinations of output clock source, bus width, and output data rate, as shown in Table 6-9.

Table 6-9. SRC Protocol Combinations

PROTOCOL	OUTPUT CLOCK SOURCE	BUS WIDTH	OUTPUT DATA RATE	SDI_CNTL	SDO_CNTL	#OUTPUT CLOCK (Optimal Read Frame)	TIMING DIAGRAM
SRC-EXT-SS	SCLK(1)	Single	SDR	00h, 01h, 02h, or 03h(1)	03h	8	Figure 6-44
SRC-INT-SS	INTCLK(2)	Single	SDR		43h	8	Figure 6-45
SRC-IB2-SS	INTCLK / 2(2)	Single	SDR		83h	8	
SRC-IB4-SS	INTCLK / 4(2)	Single	SDR		C3h	8	
SRC-EXT-DS	SCLK(1)	Dual	SDR		0Bh	8	Figure 6-48
SRC-INT-DS	INTCLK(2)	Dual	SDR		4Bh	8	Figure 6-49
SRC-IB2-DS	INTCLK / 2(2)	Dual	SDR		8Bh	8	
SRC-IB4-DS	INTCLK / 4(2)	Dual	SDR		CBh	8	
SRC-EXT-QS	SCLK(1)	Quad	SDR		0Fh	4	Figure 6-52
SRC-INT-QS	INTCLK(2)	Quad	SDR		4Fh	4	Figure 6-53
SRC-IB2-QS	INTCLK / 2(2)	Quad	SDR		8Fh	4	
SRC-IB4-QS	INTCLK / 4(2)	Quad	SDR		CFh	4	
SRC-EXT-SD	SCLK(1)	Single	DDR		13h	8	Figure 6-46
SRC-INT-SD	INTCLK(1)	Single	DDR		53h	8	Figure 6-47
SRC-IB2-SD	INTCLK / 2(2)	Single	DDR		93h	8	
SRC-IB4-SD	INTCLK / 4(2)	Single	DDR		D3h	8	
SRC-EXT-DD	SCLK(1)	Dual	DDR		1Bh	4	Figure 6-50
SRC-INT-DD	INTCLK(2)	Dual	DDR		5Bh	4	Figure 6-51
SRC-IB2-DD	INTCLK / 2(2)	Dual	DDR		9Bh	4	
SRC-IB4-DD	INTCLK / 4(2)	Dual	DDR		DBh	4	
SRC-EXT-QD	SCLK(1)	Quad	DDR		1Fh	2	Figure 6-54
SRC-INT-QD	INTCLK(2)	Quad	DDR		5Fh	2	Figure 6-51
SRC-IB2-QD	INTCLK / 2(2)	Quad	DDR		9Fh	2	
SRC-IB4-QD	INTCLK / 4(2)	Quad	DDR		DFh	2	

(1) The EXTCLK option is not recommended when operating with DV_{DD} < 2.35V.
(2) The device supports INTCLK, INTCLK / 2, and INTCLK / 4 options only for data transfer operations in zone 1. The EXTCLK option is supported in zone 1 and zone 2; see Figure 6-15.

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Figure 6-44 to Figure 6-55 show the details of various source synchronous protocols. Table 6-9 shows the number of output clocks required in an optimal read frame for the different output protocol selections.

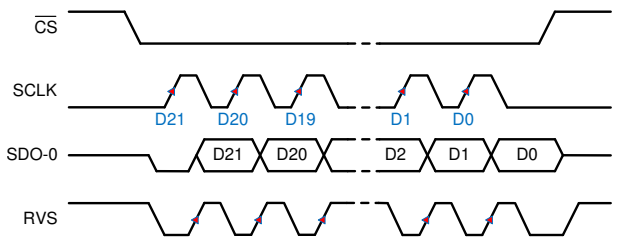


Figure 6-44. SRC-EXT-SS: SRC, SCLK, Single SDO, SDR

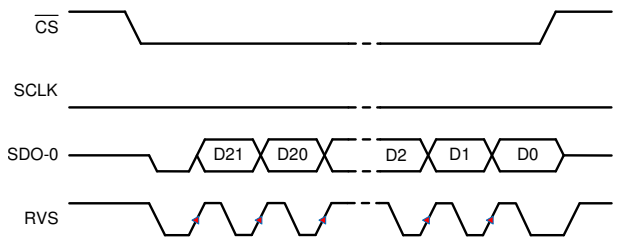


Figure 6-45. SRC-INT-SS: SRC, INTCLK, Single SDO, SDR

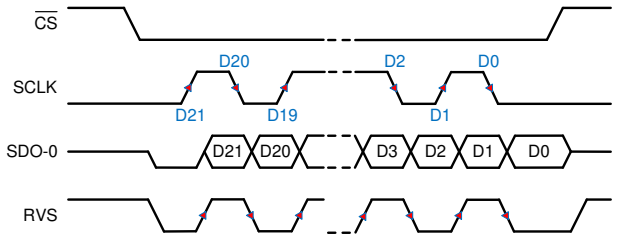


Figure 6-46. SRC-EXT-SD: SRC, SCLK, Single SDO, DDR

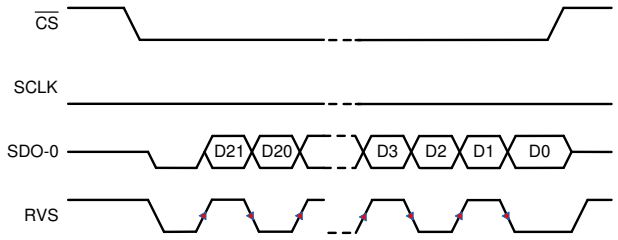


Figure 6-47. SRC-INT-SD: SRC, INTCLK, Single SDO, DDR

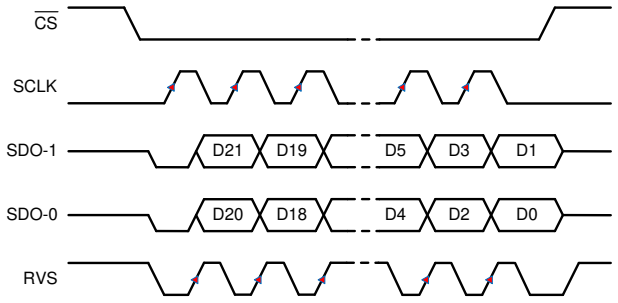


Figure 6-48. SRC-EXT-DS: SRC, SCLK, Dual SDO, SDR

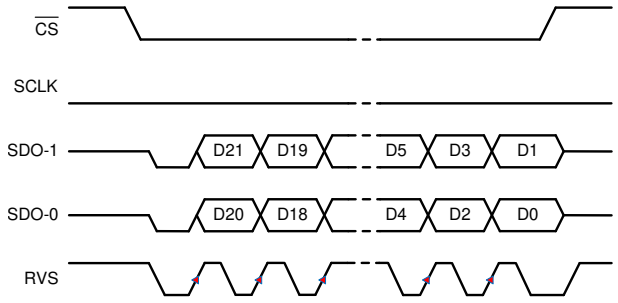


Figure 6-49. SRC-INT-DS: SRC, INTCLK, Dual SDO, SDR

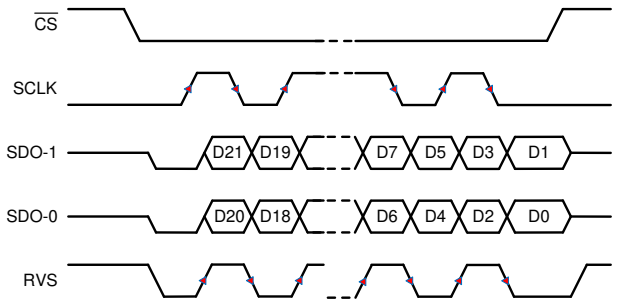


Figure 6-50. SRC-EXT-DD: SRC, SCLK, Dual SDO, DDR

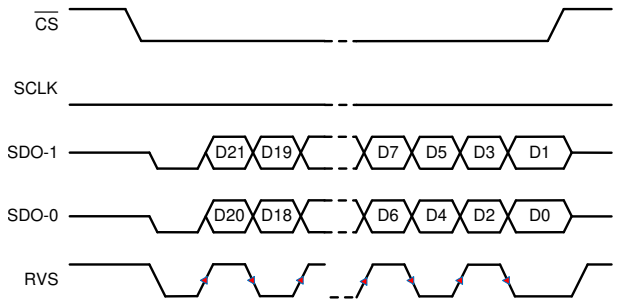


Figure 6-51. SRC-INT-DD: SRC, INTCLK, Dual SDO, DDR

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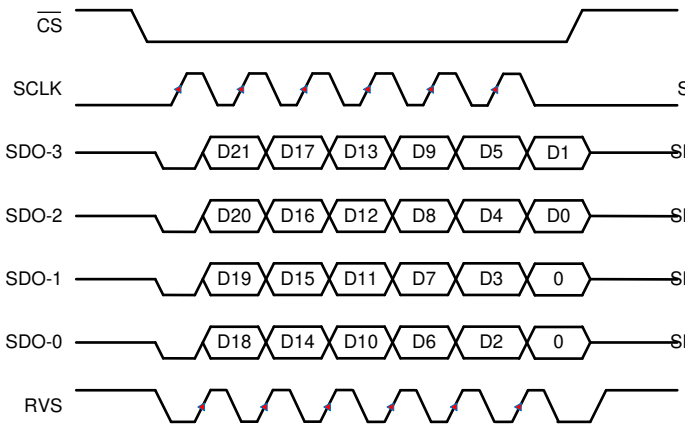


Figure 6-52. SRC-EXT-QS: SRC, SCLK, Quad SDO, SDR

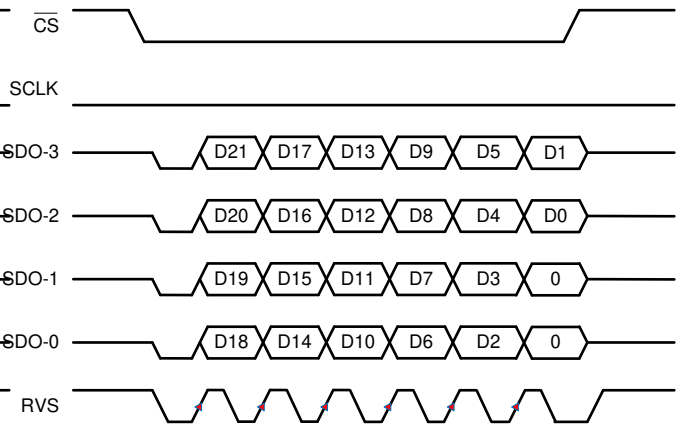


Figure 6-53. SRC-INT-QS: SRC, INTCLK, Quad SDO, SDR

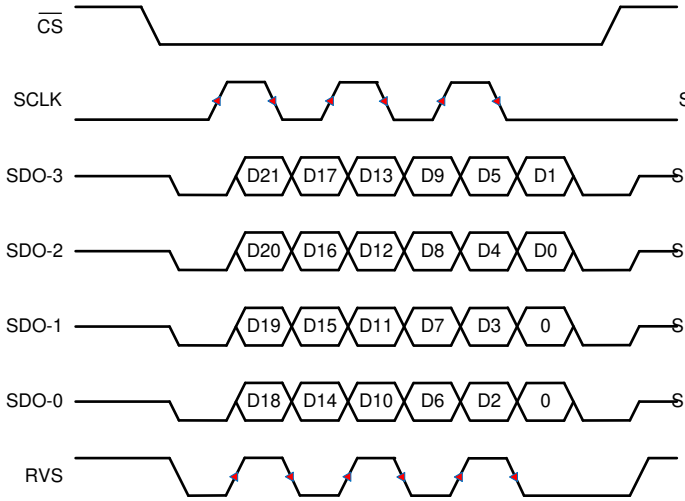


Figure 6-54. SRC-EXT-QD: SRC, SCLK, Quad SDO, DDR

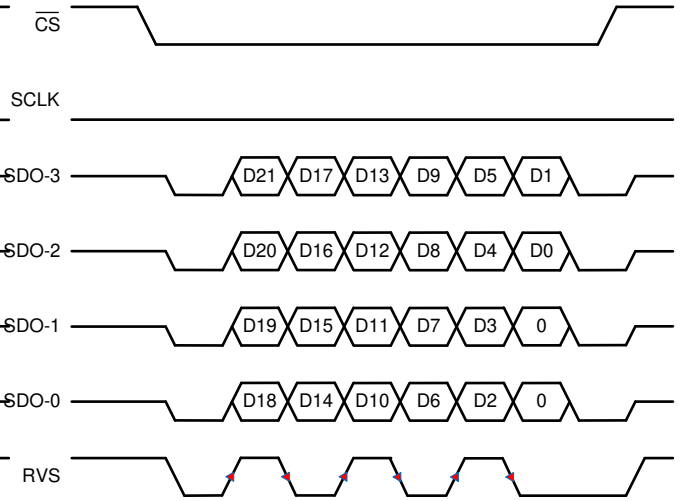


Figure 6-55. SRC-INT-QD: SRC, INTCLK, Quad SDO, DDR

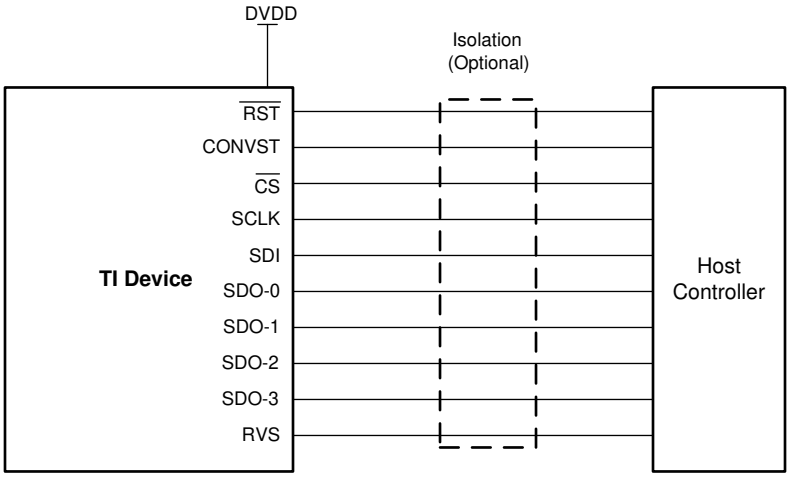
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6.5.5 Device Setup

The multiSPI digital interface and the device configuration registers offer multiple operation modes. This section describes how to select the hardware connection topology to meet different system requirements.

6.5.5.1 Single Device: All multiSPI Options

Figure 6-56 shows the connections between a host controller and a single device to exercise all options provided by the multiSPI digital interface.

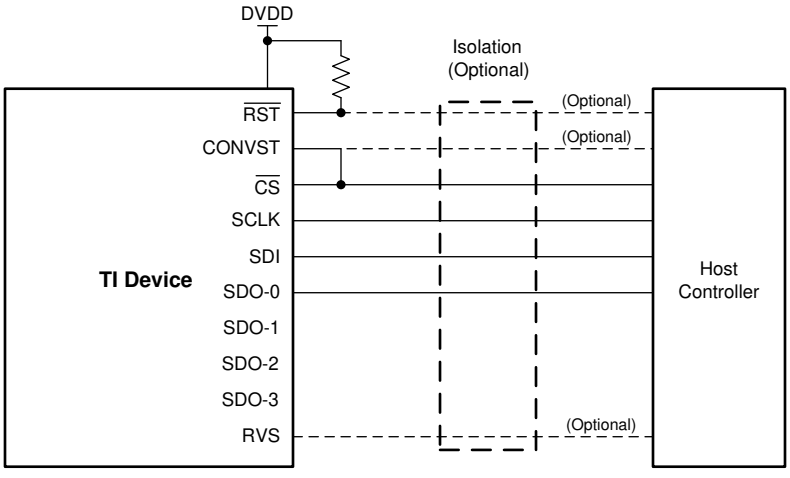


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Figure 6-56. MultiSPI Digital Interface, All Pins

6.5.5.2 Single Device: Minimum Pins for a Standard SPI

Figure 6-57 shows the minimum-pin interface for applications using a standard SPI protocol.



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Figure 6-57. SPI, Minimum Pins

The $\overline{CS}$, SCLK, SDI, and SDO-0 pins constitute a standard SPI port of the host controller. The CONVST pin is tied to $\overline{CS}$, and the $\overline{RST}$ pin is tied to DVDD. The SDO-1, SDO-2, and SDO-3 pins have no external connections. The following features are also available:

- Control the CONVST pin independently to get additional timing flexibility.
- Control $\overline{RST}$ pin independently to add asynchronous reset functionality.
- Monitor the RVS pin for additional timing benefits.

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6.5.5.3 Multiple Devices: Daisy-Chain Topology

A typical connection diagram showing multiple devices in a daisy-chain topology is shown in Figure 6-58.

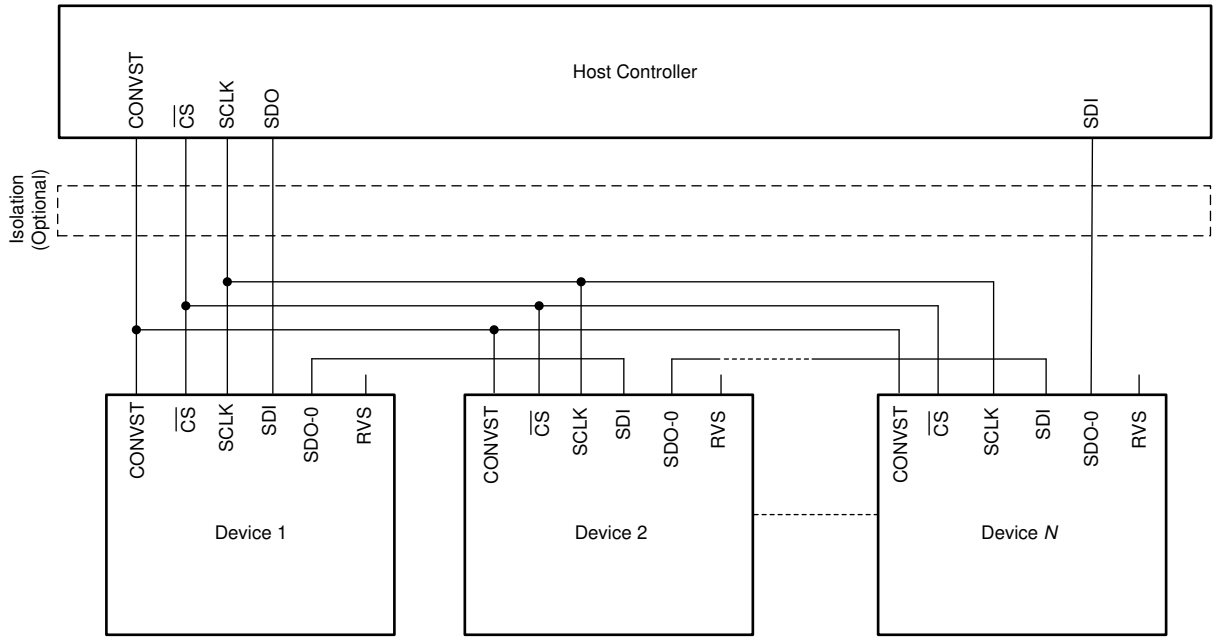


Figure 6-58. Daisy-Chain Connections

The CONVST, $\overline{CS}$, and SCLK inputs of all devices are connected together and controlled by a single CONVST, $\overline{CS}$, and SCLK pin of the host controller, respectively. The SDI input pin of the first device in the chain (Device 1) is connected to the SDO pin of the host controller, the SDO-0 output pin of Device 1 is connected to the SDI input pin of Device 2, and so on. The SDO-0 output pin of the last device in the chain (Device *N*) is connected to the SDI pin of the host controller.

To operate multiple devices in a daisy-chain topology, the host controller sets the configuration registers in each device with identical values and operates with any of the legacy, SPI-compatible protocols for data-read and data-write operations (SDO_CNT[7:0] = 00h or 01h). With these configurations settings, the 22-bit ODR and 22-bit IDR registers in each device collapse to form a single, 22-bit unified shift register (USR) per device, as shown in Figure 6-59.

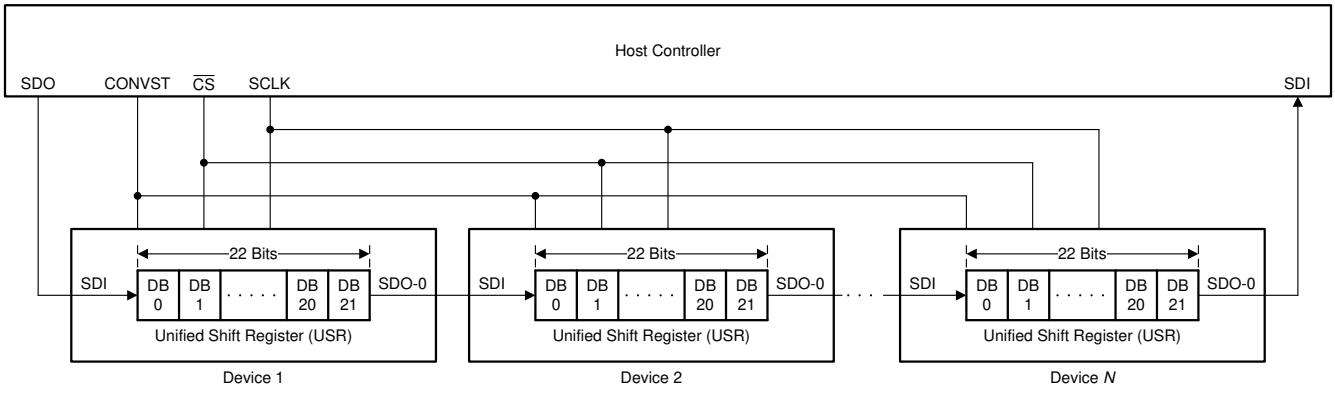


Figure 6-59. Unified Shift Register

All devices in the daisy-chain topology sample the respective device analog input signals on the CONVST rising edge. The data transfer frame starts with a $\overline{CS}$ falling edge. On each SCLK launch edge, every device in the chain shifts out the MSB of the respective USR on to the respective SDO-0 pin. On every SCLK capture edge, each device in the chain shifts in data received on the respective SDI pin as the LSB bit of the respective USR. Therefore, in a daisy-chain configuration, the host controller receives the data of Device *N*, followed by the data of Device *N* – 1, and so on (MSB-first). On the $\overline{CS}$ rising edge, each device decodes the contents in the respective USR, and takes appropriate action.

A typical timing diagram for three devices connected in daisy-chain topology using the SPI-00S protocol is shown in Figure 6-60.

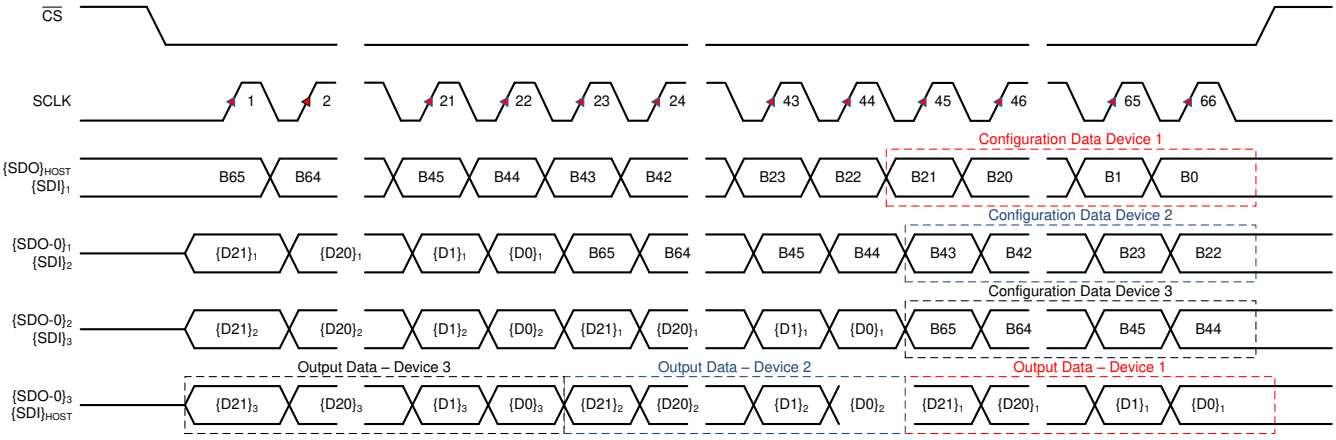


Figure 6-60. Three-Device, Daisy-Chain Timing

In daisy-chain topology, the overall throughput of the system is proportionally reduced as more devices are connected in the daisy-chain.

Note

For *N* devices connected in daisy-chain topology, an optimal data transfer frame must contain 22 × *N* SCLK capture edges. For a longer data transfer frame (number of SCLK in the frame > 22 × *N*), the host controller must appropriately align the configuration data for each device before bringing $\overline{CS}$ high. A shorter data transfer frame (number of SCLK in the frame < 22 × *N*) can result in an erroneous device configuration, and *must be avoided*.

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6.5.5.4 Multiple Devices: Star Topology

A typical connection diagram showing multiple devices in a star topology is shown in Figure 6-61. The CONVST, SDI, and SCLK inputs of all devices are connected together, and are controlled by a single CONVST, SDO, and SCLK pin of the host controller, respectively. Similarly, the SDO output pin of all devices are tied together and connected to the a single SDI input pin of the host controller. The $\overline{CS}$ input pin of each device is individually controlled by separate $\overline{CS}$ control lines from the host controller.

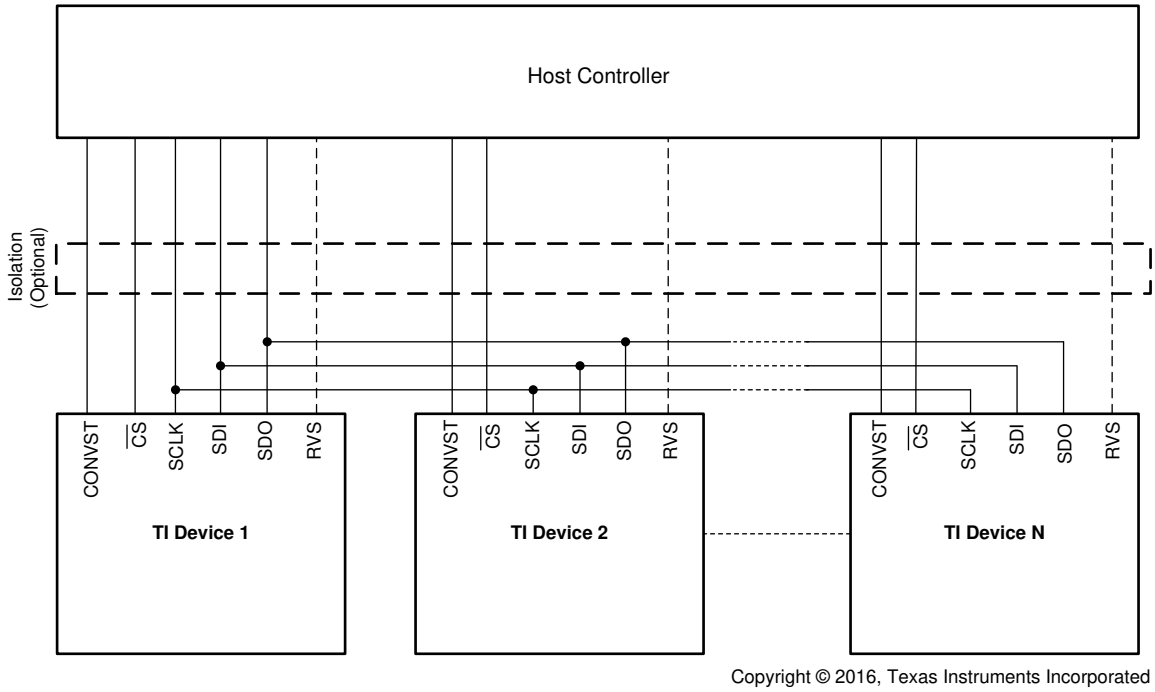


Figure 6-61. Star-Topology Connection

The timing diagram for three devices connected in the star topology is shown in Figure 6-62. To avoid any conflict related to multiple devices driving the SDO line at the same time, make sure that the host controller pulls down the $\overline{CS}$ signal for *only one device at any particular time*.

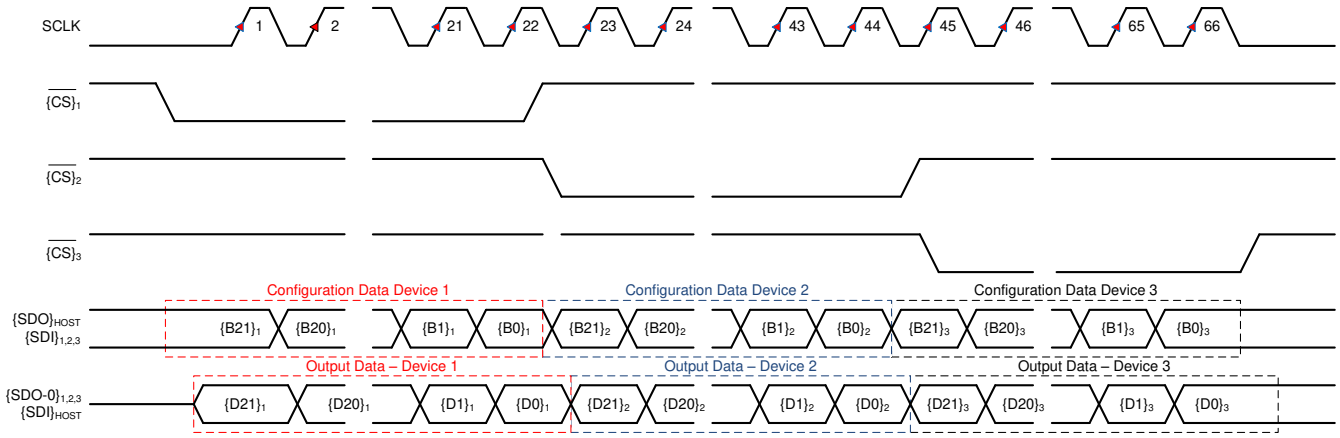


Figure 6-62. Three-Device, Star Connection Timing

7 Register Maps

7.1 Device Configuration and Register Maps

The device features nine configuration registers, mapped as described in Table 7-1.

Table 7-1. Configuration Registers Mapping

ADDRESS	REGISTER NAME	REGISTER DESCRIPTION
004h	PD_CNTL	Low-power modes control
008h	SDI_CNTL	SDI input protocol selection
00Ch	SDO_CNTL	SDO output protocol selection
010h	DATA_CNTL	Output data word configuration
014h	PATN_LSB	Eight least significant bits (LSB) of the output pattern
015h	PATN_MID	Eight middle bits of the output pattern
016h	PATN_MSB	Four most significant bits (MSB) of the output pattern
020h	OFST_CAL	Offset calibration
030h	REF_MRG	Reference margin

7.1.1 PD_CNTL Register (address = 04h) [reset = 08h]

This register controls the low-power modes offered by the device.

Figure 7-1. PD_CNTL Register

7	6	5	4	3	2	1	0
0	0	0	0	1	PD_REFBUF	PD_ADC	0
R-0b	R-0b	R-0b	R-0b	R-1b	R/W-0b	R/W-0b	R-0b

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-2. PD_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	R	00001b	Reserved bits. Reads return 00001b.
2	PD_REFBUF	R/W	0b	This bit powers down the internal reference buffer. 0b = Internal reference buffer is powered up 1b = Internal reference buffer is powered down
1	PD_ADC	R/W	0b	This bit powers down the converter module. 0b = converter module is powered up 1b = converter module is powered down
0	0	R	0b	Reserved bits. Do not write. Reads return 0b.

To power-down the converter module, set the PD_ADC bit in the PD_CNTL register. The converter module powers down on the rising edge of $\overline{CS}$. To power-up the converter module, reset the PD_ADC bit in the PD_CNTL register. The converter module starts to power-up on the rising edge of $\overline{CS}$. Wait for t_{PU_ADC} before initiating any conversion or data transfer operation.

To power-down the internal reference buffer, set the PD_REFBUF bit in the PD_CNTL register. The internal reference buffer powers down on the rising edge of $\overline{CS}$. To power-up the internal reference buffer, reset the PD_REFBUF bit in the PD_CNTL register. The internal reference buffer starts to power-up on the rising edge of $\overline{CS}$. Wait for t_{PU_REFBUF} before initiating any conversion.

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7.1.2 SDI_CNTL Register (address = 008h) [reset = 00h]

This register selects the SPI protocol for writing data to the device.

Figure 7-2. SDI_CNTL Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SDI_MODE[1:0]	
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R/W-00b	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-3. SDI_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	R	000000b	Reserved bits. Do not write. Reads return 000000b.
1-0	SDI_MODE[1:0]	R/W	00b	These bits select the protocol for writing data into the device. 00b = Standard SPI with CPOL = 0 and CPHASE = 0 01b = Standard SPI with CPOL = 0 and CPHASE = 1 10b = Standard SPI with CPOL = 1 and CPHASE = 0 11b = Standard SPI with CPOL = 1 and CPHASE = 1

7.1.3 SDO_CNTL Register (address = 0Ch) [reset = 00h]

This register configures the protocol for reading data from the device.

Figure 7-3. SDO_CNTL Register

7	6	5	4	3	2	1	0
SSYNC_CLK_SEL[1:0]		0	DATA_RATE	SDO_WIDTH[1:0]		SDO_MODE[1:0]	
R/W-00b		R-0b	R/W-0b	R/W-00b		R/W-00b	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-4. SDO_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	SSYNC_CLK_SEL[1:0]	R/W	00b	These bits select the source and frequency of the clock for the ADC-Clock-Master mode, and are valid only if SDO_MODE[1:0] = 11b. 00b = External SCLK echo 01b = Internal clock (INTCLK) 10b = Internal clock / 2 (INTCLK / 2) 11b = Internal clock / 4 (INTCLK / 4)
5	0	R	0b	Reserved bit. Do not write. Reads return 0b.
4	DATA_RATE	R/W	0b	This bit is ignored if SDO_MODE[1:0] = 00b. When SDO_MODE[1:0] = 11b: 0b = SDOs are updated at single data rate (SDR) with respect to the output clock 1b = SDOs are updated at double data rate (DDR) with respect to the output clock
3-2	SDO_WIDTH[1:0]	R/W	00b	These bits set the width of the output bus. 0xb = Data are output only on SDO-0 10b = Data are output only on SDO-0 and SDO-1 11b = Data are output on SDO-0, SDO-1, SDO-2, and SDO-3
1-0	SDO_MODE[1:0]	R/W	00b	These bits select the protocol for reading data from the device. 00b = SDO follows the SPI protocol selected in the SDI_CNTL register 01b = SDO follows the SPI protocol selected in the SDI_CNTL register but with *Early Data Launch* feature enabled. See Table 6-6. 10b = Invalid configuration, not supported by the device 11b = SDO follows the source-synchronous protocol

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7.1.4 DATA_CNTL Register (address = 010h) [reset = 00h]

This register configures the contents of the 22-bit output data word (D[21:0]).

Figure 7-4. DATA_CNTL Register

7	6	5	4	3	2	1	0
0	0	0	0	FPAR_LOC[1:0]		PAR_EN	DATA_VAL
R-0b	R-0b	R-0b	R-0b	R/W-00b		R/W-0b	R/W-0b

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-5. DATA_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R	0000b	Reserved bits. Reads return 0000b.
3-2	FPAR_LOC[1:0]	R/W	00b	These bits control the data span for calculating the FTPAR bit (bit D[4] in the output data word). 00b = D[4] reflects even parity calculated for 4MSB 01b = D[4] reflects even parity calculated for 8MSB 10b = D[4] reflects even parity calculated for 12MSB 11b = D[4] reflects even parity calculated for all 16 bits (that is, the same as FLPAR)
1	PAR_EN	R/W	0b	0b = Output data does not contain any parity information D[5] = 0 D[4] = 0 1b = Parity information is appended to the LSB of the output data D[5] = Even parity calculated on bits D[21:6] D[4] = Even parity computed on selected number of MSB of D[21:6] as per FPAR_LOC[1:0] setting See Figure 6-13 for further details of parity computation.
0	DATA_VAL	R/W	0b	These bits control bits D[21:6] of the output data word. 0b = 16-bit conversion output 1b = 16-bit contents of the fixed-pattern registers See PATN CNTL for more details.

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7.1.5 PATN_LSB Register (address = 014h) [reset = 00h]

This register controls the eight LSB of the output pattern when DATA_VAL = 1b; see Figure 7-8.

Figure 7-5. PATN_LSB Register

7	6	5	4	3	2	1	0
PATN_LSB_BITS							
R/W-00000000b							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-6. PATN_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PATN_LSB_BITS	R/W	00000000b	8LSB of the output pattern

7.1.6 PATN_MID Register (address = 015h) [reset = 00h]

This register controls the middle eight bits of the output pattern when DATA_VAL = 1b; see Figure 7-8.

Figure 7-6. PATN_MID Register

7	6	5	4	3	2	1	0
PATN_MID_BITS							
R/W-00000000b							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-7. PATN_MID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PATN_MID_BITS	R/W	00000000b	8 middle bits of the output pattern

7.1.7 PATN_MSB Register (address = 016h) [reset = 00h]

This register controls the four MSB of the output pattern when DATA_VAL = 1b; see Figure 7-8.

Figure 7-7. PATN_MSB Register

7	6	5	4	3	2	1	0
0	0	0	0	PATN_MSB_BITS			
R-0b	R-0b	R-0b	R-0b	R/W-0000b			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-8. PATN_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R	0000b	Reserved bits. Reads return 0000b.
3-0	PATN_MSB_BITS	R/W	0000b	4MSB of the output pattern

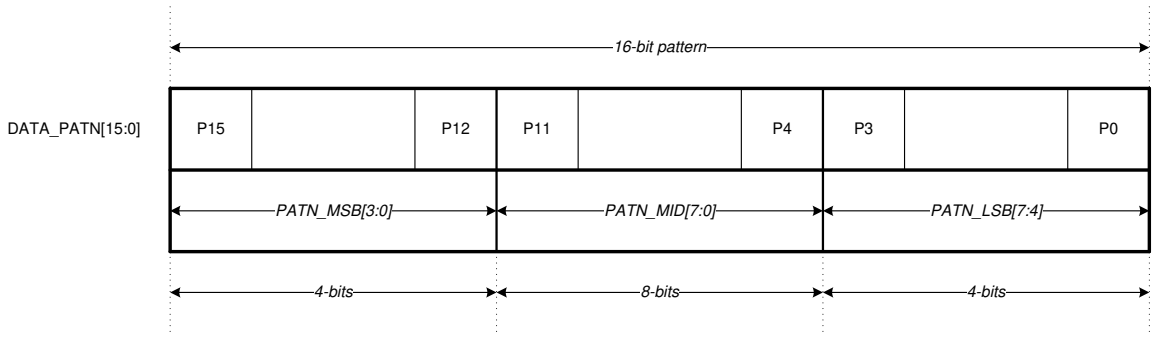


Figure 7-8. DATA_PATN[15:0]

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7.1.8 OFST_CAL Register (address = 020h) [reset = 00h]

This register selects the external reference range for optimal offset calibration.

Figure 7-9. OFST_CAL Register

7	6	5	4	3	2	1	0
0	0	0	0	0	REF_SEL[2:0]		
R-0b	R-0b	R-0b	R-0b	R-0b	R/W-000b		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-9. OFST_CAL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	R	00000b	Reserved bits. Reads return 00000b.
2-0	REF_SEL[2:0]	R/W	000b	These bits select the external reference range for optimal offset. 000b = Optimum offset calibration for V_{REF} = 5.0V 001b = Optimum offset calibration for V_{REF} = 4.5V 010b = Optimum offset calibration for V_{REF} = 4.096V 011b = Optimum offset calibration for V_{REF} = 3.3V 100b = Optimum offset calibration for V_{REF} = 3.0V 101b = Optimum offset calibration for V_{REF} = 2.5V 110b = Optimum offset calibration for V_{REF} = 5.0V 111b = Optimum offset calibration for V_{REF} = 5.0V

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7.1.9 REF_MRG Register (address = 030h) [reset = 00h]

This register selects the margining to be added to or subtracted from the reference buffer output; see the *Reference Buffer Module* section.

Figure 7-10. REF_MRG Register

7	6	5	4	3	2	1	0
0	0	EN_MARG	REF_OFST[4:0]				
R-0b	R-0b	R/W-0b	R/W-00000b				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-10. REF_MRG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	R	00b	Reserved bits. Reads return 00b.
5	EN_MARG	R/W	0b	This bit enables margining feature. 0b = Margining is disabled 1b = Margining is enabled
4-0	REF_OFST[4:0]	R/W	00000b	These bits select the reference offset value as per Table 7-11.

Table 7-11. REF_OFST[4:0] settings

REF_OFST[4:0]	$\Delta V_{REFBUFOUT}$ (typical(1))
00000b	0mV
00001b	280µV
00010b	580µV
00011b	840µV
00100b	1.12mV
00101b	1.4mV
00110b	1.68mV
00111b	1.96mV
01000b	2.24mV
01001b	2.52mV
01010b	2.8mV
01011b	3.08mV
01100b	3.36mV
01101b	3.64mV
01110b	3.92mV
01111b	4.2mV
10000b	–4.5mV
10001b	–4.22mV
10010b	–3.94mV
10011b	–3.66mV
10100b	–3.38mV
10101b	–3.1mV
10110b	–2.82mV
10111b	–2.54mV
11000b	–2.26mV
11001b	–1.98mV
11010b	–1.7mV
11011b	–1.42mV
11100b	–1.14mV
11101b	–860 µV
11110b	–580 µV
11111b	–280 µV

(1) The actual $V_{REFBUFOUT}$ value can vary by ±10% from Table 7-11

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The two primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR), analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section presents general principles for designing these circuits, followed by an application circuit designed using the ADS892xB.

8.1.1 ADC Reference Driver

The external reference source must provide low-drift and very accurate voltage at the REFIN pin of the ADS892xB. The output broadband noise of most references can be in the order of a few hundred μV_{RMS}. Therefore, to prevent any degradation in the noise performance of the ADC, appropriately filter the output of the voltage reference by using a low-pass filter with a cutoff frequency of a few hundred hertz.

The internal reference buffer of the ADS892xB provides the dynamic load posed on the REFBUFOUT pin during the conversion process. Decouple the REFBUFOUT pin with the REFM pin using the recommended C_{REFBUF} and R_{ESR}. See the Layout section for layout recommendations.

8.1.2 ADC Input Driver

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and a charge kickback filter. The amplifier is used for signal conditioning of the input signal and the low output impedance of the amplifier provides a buffer between the signal source and the switched capacitor inputs of the ADC. The charge kickback filter helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC, and band-limits the wideband noise contributed by the front-end circuit. Careful design of the front-end circuit is critical to meet the linearity and noise performance of the ADS892xB.

8.1.2.1 Charge-Kickback Filter

The charge-kickback filter is an RC filter at the input pins of the ADC that filters the broadband noise from the front-end drive circuitry, and attenuates the sampling charge injection from the switched-capacitor input stage of the ADC. A filter capacitor, C_{FLT}, is connected from each input pin of the ADC to the ground (as shown in Figure 8-1). This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. Generally, the value of this capacitor must be at least 20 times the specified value of the ADC sampling capacitance. For the ADS892xB, the input sampling capacitance is equal to 60pF; therefore, for optimal performance, keep C_{FLT} greater than 1.2nF. This capacitor must be a COG- or NPO-type. The type of dielectric used in COG or NPO ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.

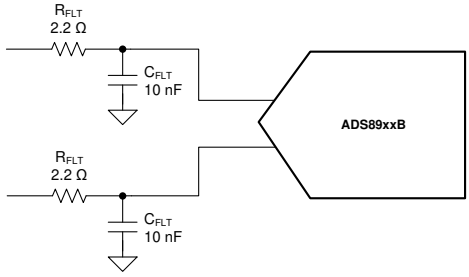


Figure 8-1. Charge Kickback Filter Configuration

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Driving capacitive loads can degrade the phase margin of the input amplifier, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors (R_{FLT}) are used at the output of the amplifiers. A higher value of R_{FLT} helps with amplifier stability, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FLT} requires balancing the stability of the driver amplifier and distortion performance of the design. Always verify the stability and settling behavior of the driving amplifier and charge-kickback filter by TINA-TI™ SPICE simulation. Keep the tolerance of the selected resistors less than 1% to keep the inputs balanced.

8.1.2.2 Input Amplifier Selection

Selection criteria for the input amplifiers is highly dependent on the input signal type, as well as the performance goals, of the data acquisition system. Some key amplifier specifications to consider when selecting an appropriate amplifier to drive the inputs of the ADC are:

- *Small-signal bandwidth.* Select the small-signal bandwidth of the input amplifiers to be as high as possible after meeting the power budget of the system. Higher bandwidth reduces the closed-loop output impedance of the amplifier, thus allowing the amplifier to more easily drive the ADC sample-and-hold capacitor and the RC filter (Charge-Kickback Filter) at the inputs of the ADC. Higher bandwidth amplifiers offer faster settling times while driving the capacitive load of the charge-kickback filter, thus reducing harmonic distortion at higher input frequencies. To maintain the overall stability of the input driver circuit, select the amplifier with a unity gain bandwidth (UGB) as described in Equation 17:

$$\text{UGB} \geq 4 \times \left(\frac{1}{2\,\pi\, \times R_{FLT} \times C_{FLT}} \right) \tag{17}$$

- *Distortion.* Both the ADC and the input driver introduce distortion in a data acquisition block. To make sure that the distortion performance of the data acquisition system is not limited by the front-end circuit, the distortion of the input driver must be at least 10dB less than the distortion of the ADC, as shown in Equation 18.

$$\text{THD}_{AMP} \leq \text{THD}_{ADC} - 10\ (\text{dB}) \tag{18}$$

- *Noise.* Noise contribution of the front-end amplifiers must be as low as possible to prevent any degradation in SNR performance of the system. Generally, to make sure that the noise performance of the data acquisition system is not limited by the front-end circuit, the total noise contribution from the front-end circuit must be kept below 20% of the input-referred noise of the ADC. Noise from the input driver circuit is band-limited by designing a low cutoff frequency, charge-kickback filter, as explained in Equation 19.

$$N_G \times \sqrt{2} \times \sqrt{\left(\frac{V_{1/f_AMP_PP}}{6.6} \right)^2 + e_{n_RMS}^2 \times \frac{\pi}{2} \times f_{-3dB}} \leq \frac{1}{5} \times \frac{V_{REF}}{\sqrt{2}} \times 10^{-\left(\frac{\text{SNR(dB)}}{20} \right)} \tag{19}$$

  where:

  - V_{1/f_AMP_PP} is the peak-to-peak flicker noise in µV
  - e_{n_RMS} is the amplifier broadband noise density in nV/$\sqrt{\text{Hz}}$
  - f_{-3dB} is the 3dB bandwidth of the charge-kickback filter
  - N_G is the noise gain of the front-end circuit that is equal to 1 in a buffer configuration

- *Settling Time.* For dc signals with fast transients that are common in a multiplexed application, the input signal must settle within an 16-bit accuracy at the device inputs during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Typically, amplifier datasheets specify the output settling performance only up to 0.1% to 0.001%, which is not always sufficient for the desired 16-bit accuracy. Therefore, always verify the settling behavior of the input driver by TINA-TI SPICE simulations before selecting the amplifier.

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8.2 Typical Application

8.2.1 Data Acquisition (DAQ) Circuit for Lowest Distortion and Noise Performance With Differential Input

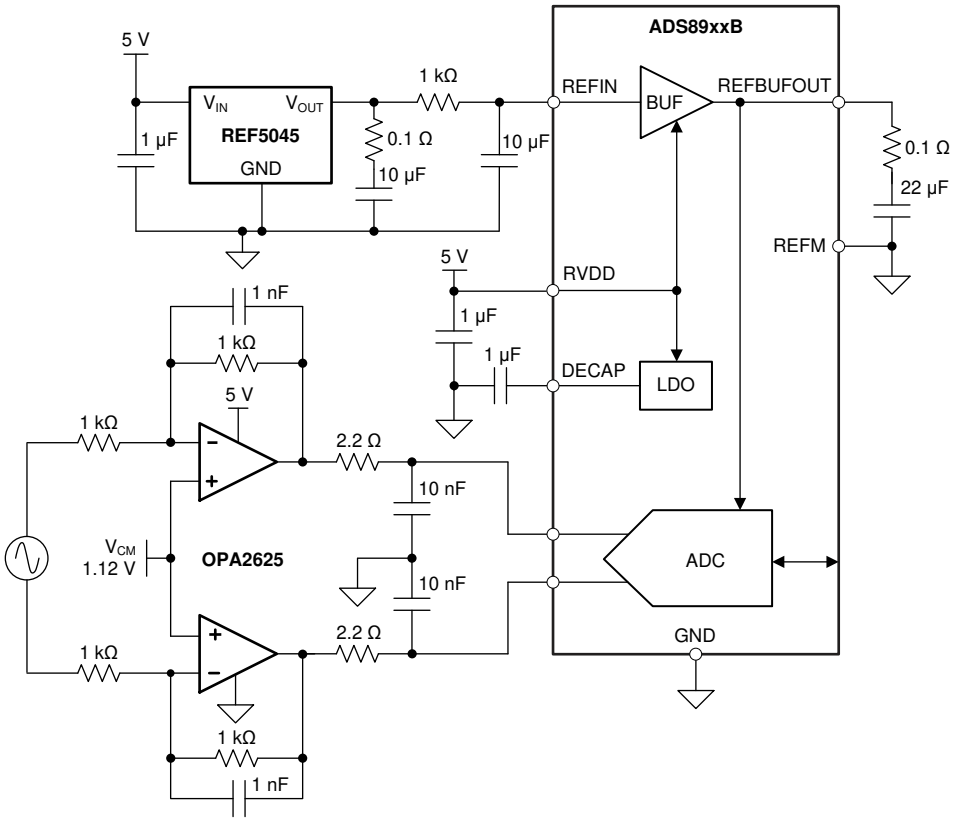


Figure 8-2. Differential-Input DAQ Circuit for Lowest Distortion and Noise Using the ADS892xB

8.2.1.1 Design Requirements

For this example, the design parameters are listed in Table 8-1.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
ADC sample rate	Maximum-specified throughput
Input signal	2kHz input, 4.5V_{PP} fully differential
Noise performance, SNR	> 96dB
Distortion, THD	< –120dB
Linearity, INL	< ±0.5LSB
Reference	4.5V
Power supply	< 5.5V analog, 3.3V I/O

8.2.1.2 Detailed Design Procedure

The application circuit is illustrated in Figure 8-2. For simplicity, power-supply decoupling capacitors are not shown in these circuit diagrams; see the *Power-Supply Recommendations* section for suggested guidelines.

The reference voltage of 4.5V is generated by the high-precision, low-noise REF5045 circuit. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3dB cutoff frequency of 16Hz.

Generally, the distortion from the input driver must be at least 10dB less than the ADC distortion. The low-power OPA2625 (a high-bandwidth, low-distortion, high-precision amplifier in an inverting gain configuration) as an input driver provides exceptional ac performance because of extremely low-distortion and high-bandwidth

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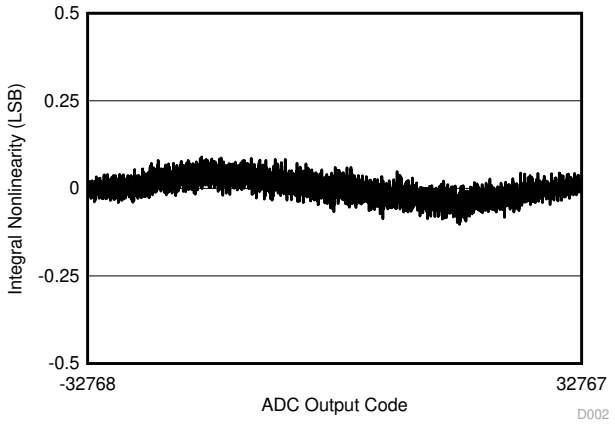
specifications. The distortion resulting from variation in the common-mode signal is eliminated by using the OPA2625 in an inverting gain configuration. To exercise the complete dynamic range of the device, the common-mode voltage at the ADS892xB inputs is established at a value of 2.25V (4.5V / 2) by using the noninverting pins of the OPA2625 amplifiers. In addition, the components of the charge kickback filter keep the noise from the front-end circuit low without adding distortion to the input signal.

For a complete schematic, see the *ADS8920BEVM-PDK user's guide* located in the *ADS8920B SAR Analog to Digital Converter Evaluation Module* web folder at www.ti.com.

A similar circuit is used in reference design TIPD211, a step-by-step process to design a *20-Bit, 1MSPS, 4-Ch Small Form Factor Design for Test and Measurement Applications* using four ADS8900B SAR ADCs, four OPA2625 precision amplifiers and one REF5050 precision reference.

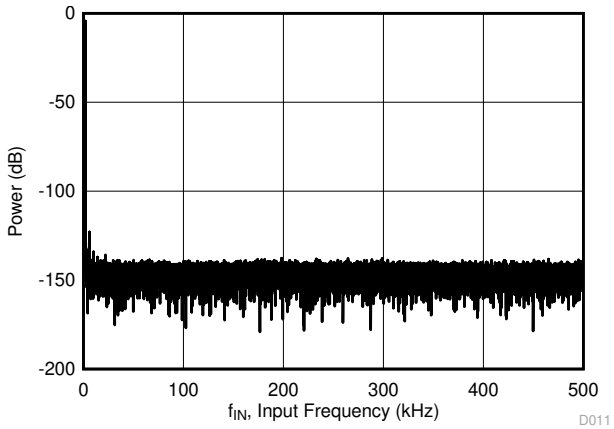
For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, see also TI Precision Design TIPD211, *18-Bit, 1MSPS, 4-Ch Small Form Factor Design for Test and Measurement Applications* (TIDUBW7).

8.2.1.3 Application Curves



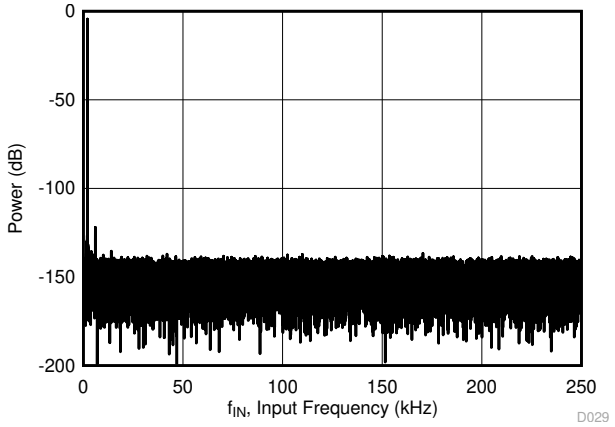
16-bit NMC DNL, ±0.2LSB INL

Figure 8-3. Typical Linearity



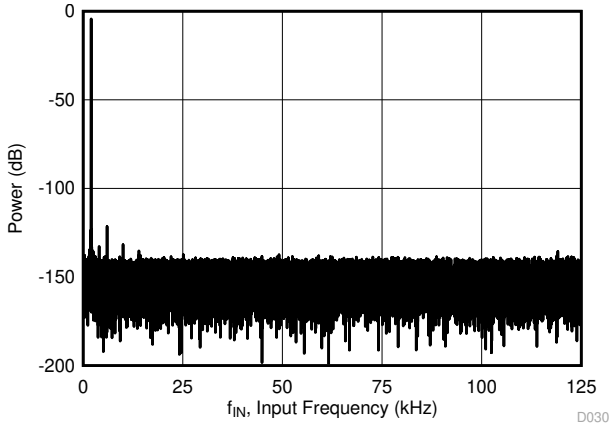
96.2dB SNR, –124dB THD

Figure 8-4. Noise-Performance FFT Plot - ADS8920B



96.2dB SNR, –124dB THD

Figure 8-5. Noise-Performance FFT Plot - ADS8922B



96.2dB SNR, –124dB THD

Figure 8-6. Noise-Performance FFT Plot - ADS8924B

8.2.2 DAQ Circuit With FDA Input Driver and Single-Ended or Differential Input

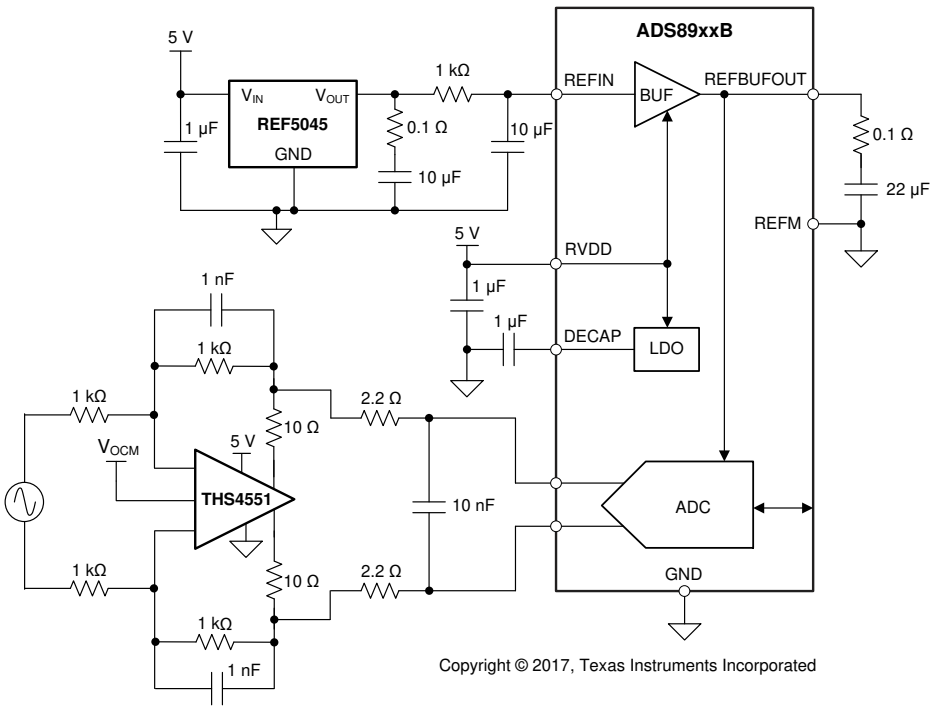


Figure 8-7. DAQ Circuit With FDA Input Driver and Differential Input

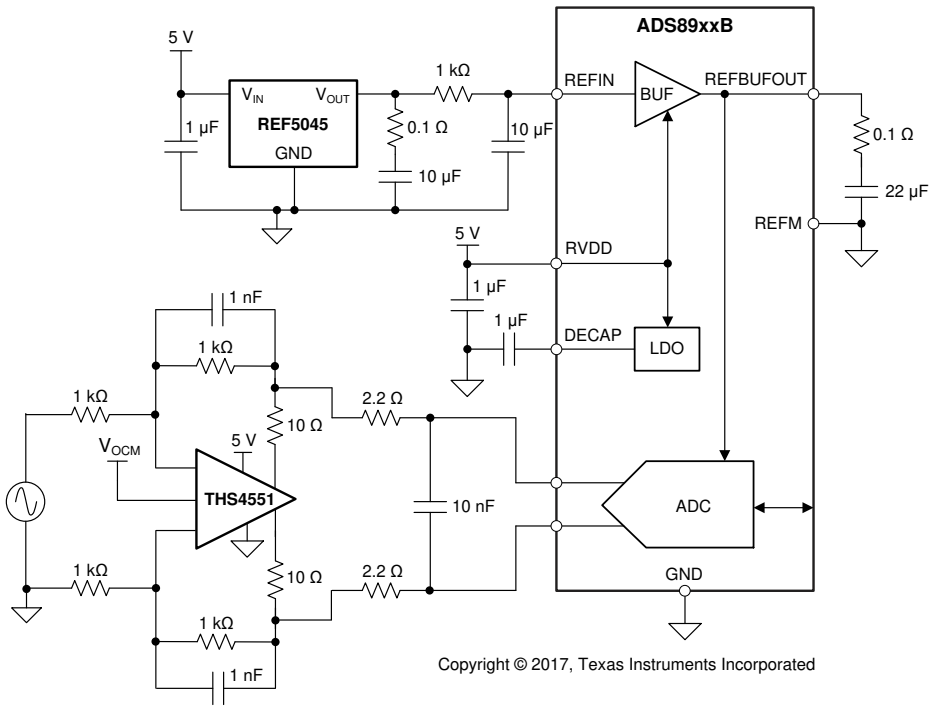


Figure 8-8. DAQ Circuit With FDA Input Driver and Single-Ended Input

8.2.3 Design Requirements

For this example, the design parameters are listed in Table 8-2.

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Table 8-2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
ADC sample rate	Maximum-specified throughput
Input signal	2kHz input, ±4.5V_{PP} fully differential and ±4.5V_{PP} single-ended bipolar signal
Noise performance, SNR	> 96dB
Distortion, THD	< –120dB
Linearity, INL	< ±0.5LSB
Reference	4.5V
Power supply	< 5.4V analog, 3.3V I/O

8.2.4 Detailed Design Procedure

The application circuits are shown in Figure 8-7 and Figure 8-8. In both applications, the input signal is processed through a high-bandwidth, low-distortion, fully-differential amplifier (FDA) designed in a gain of 1V/V and a low-pass RC filter before going to the ADC.

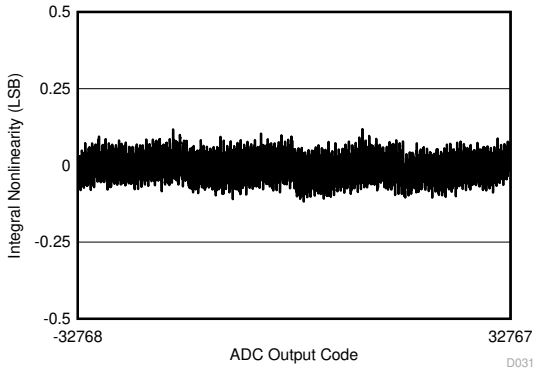
The reference voltage of 4.5V generated by the high-precision, low-noise REF5045 circuit. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3dB cutoff frequency of 16Hz.

Generally, the distortion from the input driver must be at least 10dB less than the ADC distortion. The distortion resulting from variation in the common-mode signal is eliminated by using the FDA in an inverting gain configuration that establishes a fixed common-mode level for the circuit. This configuration also eliminates the requirement of a rail-to-rail swing at the amplifier input. Therefore, these circuits use the low-power THS4551 as an input driver that provides exceptional ac performance because of the extremely low-distortion and high bandwidth specifications. In addition, the components of the charge kickback filter keep the noise from the front-end circuit low without adding distortion to the input signal.

The circuit in Figure 8-7 shows a fully-differential data acquisition (DAQ) block optimized for low distortion and noise using the THS4551 and ADS892xB. This front-end circuit configuration requires a differential signal at the input of the FDA and provides a differential output to drive the ADC inputs. The common-mode voltage of the input signal provided to the ADC is set by the V_{OCM} pin of the THS4551 (not shown in Figure 8-7). To use the complete dynamic range of the ADC, V_{OCM} can be set to V_{REF} / 2 by using a simple resistive divider.

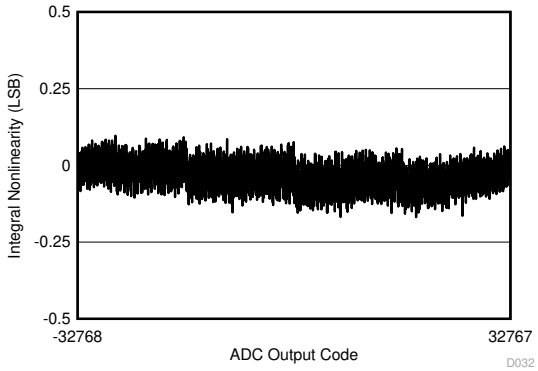
The circuit in Figure 8-8 shows a single-ended to differential DAQ block optimized for low distortion and noise using the THS4551 and the ADS892xB. This front-end circuit configuration requires a single-ended bipolar signal at the input of the FDA and provides a fully-differential output to drive the ADC inputs. The common-mode voltage of the input signal provided to the ADC is set by the V_{OCM} pin of the THS4551 (not shown in Figure 8-8). To use the complete dynamic range of the ADC, V_{OCM} can be set to V_{REF} / 2 by using a simple resistive divider.

8.2.5 Application Curves



±0.15LSB INL

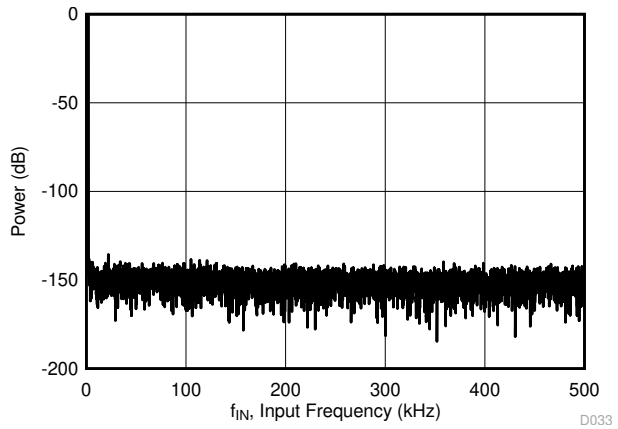
Figure 8-9. Typical Linearity, Differential Input



±0.15LSB INL

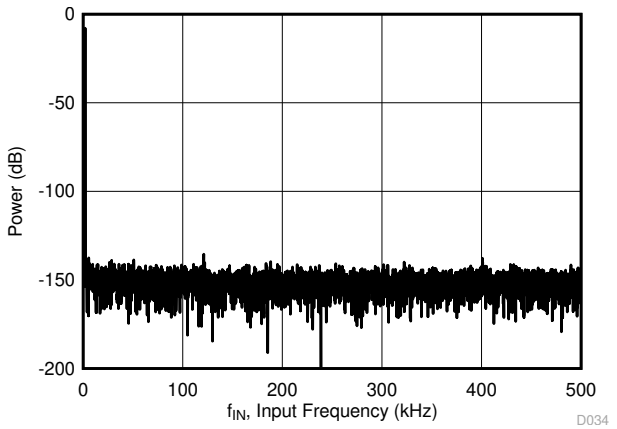
Figure 8-10. Typical Linearity, Single-Ended Input

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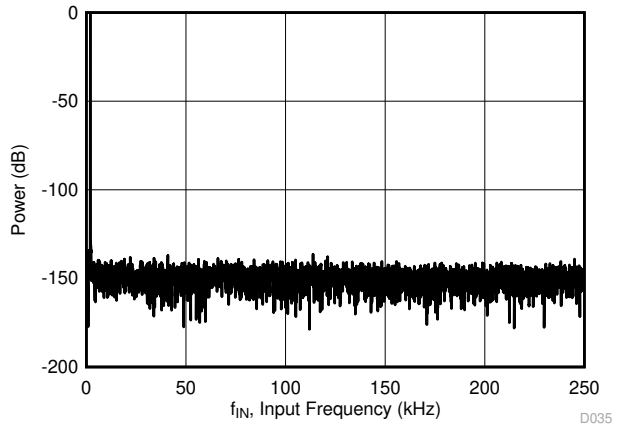
SNR = 96.1dB, THD = –131.7dB

Figure 8-11. Noise-Performance FFT Plot: ADS8920B, Differential Input



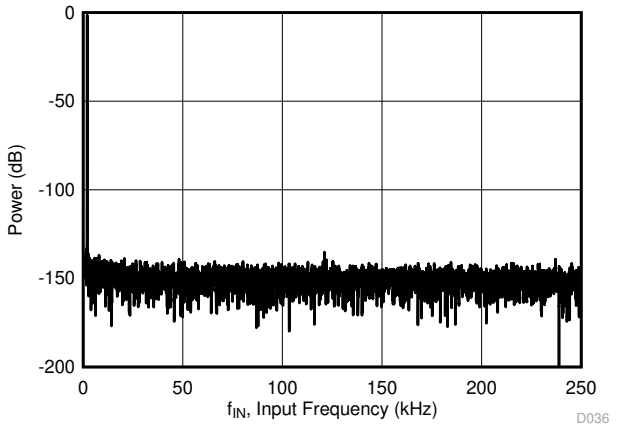
SNR = 95.9dB, THD = –125.9dB

Figure 8-12. Noise-Performance FFT Plot: ADS8920B, Single-Ended Input



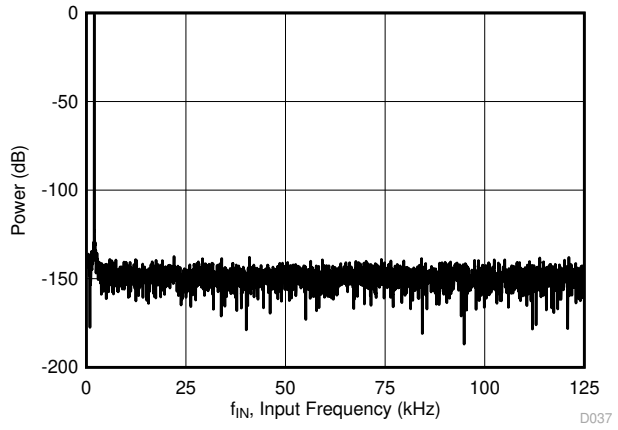
SNR = 96.2dB, THD = –132dB

Figure 8-13. Noise-Performance FFT Plot: ADS8922B, Differential Input



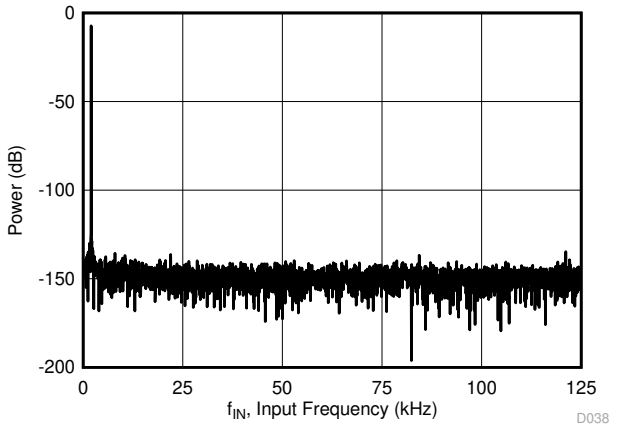
SNR = 96dB, THD = –126dB

Figure 8-14. Noise-Performance FFT Plot: ADS8922B, Single-Ended Input



SNR = 96.1dB, THD = –131.5dB

Figure 8-15. Noise-Performance FFT Plot: ADS8924B, Differential Input



SNR = 95.9dB, THD = –125.6dB

Figure 8-16. Noise-Performance FFT Plot: ADS8924B, Single-Ended Input

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8.3 Power-Supply Recommendations

The devices have two separate power supplies: RV_{DD} and DV_{DD}. The internal reference buffer and the internal LDO operate on RV_{DD}. The ADC core operates on the LDO output (available on the DECAP pins). DV_{DD} is used for the interface circuits. RV_{DD} and DV_{DD} can be independently set to any value within the permissible ranges.

The RV_{DD} supply voltage value defines the permissible range for the external reference voltage V_{REF} on REFIN pin as:

$$2.5V \le V_{REF} \le (RV_{DD} - 0.3)V \quad (20)$$

In other words, to use the external reference voltage of V_{REF}, set RV_{DD} so that:

$$3V \le RV_{DD} \le (V_{REF} + 0.3)V \quad (21)$$

Place a 10µF decoupling capacitor between the RVDD and GND pins, and between the DVDD and GND pins, as shown in Figure 8-17. Use a minimum 1µF decoupling capacitor between the DECAP pins and the GND pin.

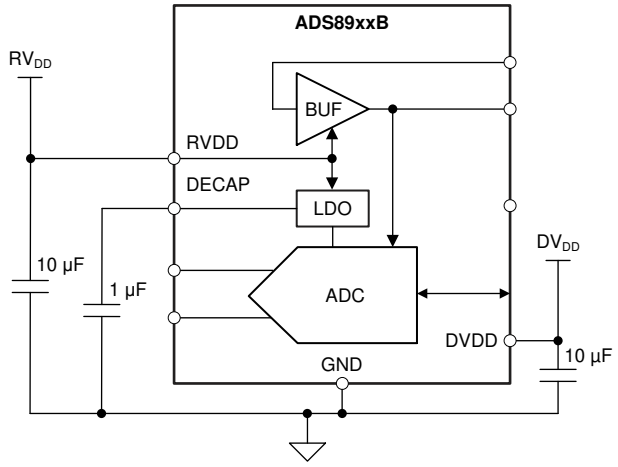


Figure 8-17. Power-Supply Decoupling

8.4 Layout

8.4.1 Layout Guidelines

This section provides some layout guidelines for achieving optimum performance with the ADS892xB ADS892xB device family.

8.4.1.1 Signal Path

As illustrated in Figure 8-18, the analog input signals are routed in opposite directions to the digital connections. The reference decoupling components are kept away from the switching digital signals. This arrangement prevents noise generated by digital switching activity from coupling to sensitive analog signals.

8.4.1.2 Grounding and PCB Stack-Up

Low inductance grounding is critical for achieving optimum performance. Grounding inductance is kept below 1nH with 15-mil grounding vias and a printed circuit board (PCB) layout design that has at least four layers. Place all critical components of the signal chain on the top layer with a solid analog ground from subsequent inner layers to minimize via length to ground.

For lowest inductance grounding, connect the GND pins of the ADS892xB ADS892xB (pin 11 and pin 15) directly to the device thermal pad and place at least four 8-mil grounding vias on the device thermal pad.

8.4.1.3 Decoupling of Power Supplies

Place the decoupling capacitors on RV_{DD}, the LDO output, and DV_{DD} within 20 mil from the respective pins, and use a 15-mil via to ground from each capacitor. Avoid placing vias between any supply pin and the respective decoupling capacitor.

8.4.1.4 Reference Decoupling

Dynamic currents are also present at the REFBUFOUT and REFM pins during the conversion phase, and excellent decoupling is required to achieve optimum performance. Place a 10µF, X7R-grade, ceramic capacitor with at least 10V rating and an ESR of 1Ω between the REFBUFOUT and the REFM pins, as illustrated in Figure 8-18. Select 0603- or 0805-size capacitors to keep equivalent series inductance (ESL) low. Connect the REFM pins to the decoupling capacitor before a ground via.

8.4.1.5 Differential Input Decoupling

Dynamic currents are also present at the differential analog inputs of the ADS892xB. Use C0G- or NPO-type capacitors to decouple these inputs because with these type of capacitors, capacitance stays almost constant over the full input voltage range. Lower-quality capacitors (such as X5R and X7R) have large capacitance changes over the full input-voltage range that can cause degradation in the performance of the device.

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8.4.2 Layout Example

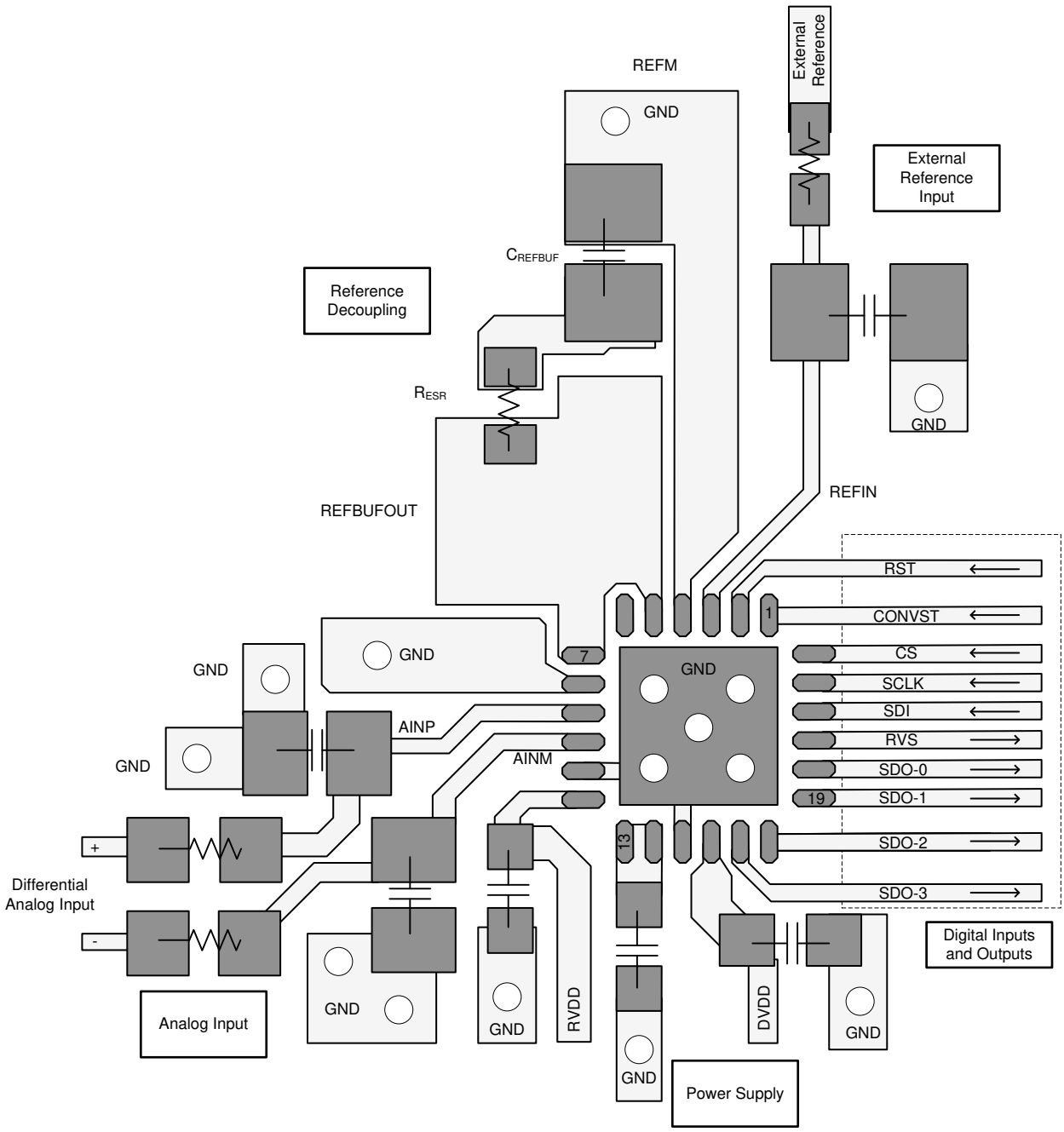


Figure 8-18. Recommended Layout

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- *ADS8920BEVM-PDK User's Guide*
- *Enabling Faster, Smarter, and More Robust System Solutions for SAR ADCs With TI's multiSPI™ Digital Interface*
- *Ultrasound CW Doppler Summing and 20-bit True Raw Data Conversion Reference Design*
- *20-Bit, 1MSPS, 4-Ch Small Form Factor Design for Test and Measurement Applications Reference Design*
- *20-Bit, 1MSPS Isolator Optimized Data Acquisition Reference Design Maximizing SNR and Sample Rate*
- *A 20-bit,1MSPS Isolated Data Acquisition (DAQ) Reference Design Optimizing Jitter for Maximum SNR and Sample Rate*
- *OPAx625 High-Bandwidth, High-Precision, Low THD+N, 16-Bit and 18-Bit Analog-to-Digital Converter (ADC) Drivers Datasheet*
- *REF5050 Low-Noise, Very Low Drift, Precision Voltage Reference Datasheet*
- *THS4551 Low Noise, Precision, 150MHz, Fully Differential Amplifier*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2017) to Revision C (August 2026)	Page
• Deleted first page table and added *Package Information* table	1
• Added serial clock frequency condition in *Timing Characteristics* table	9
• Changed reset value of PD_CNTL to 08h	52

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Changes from Revision A (July 2016) to Revision B (August 2017) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document 1
- Changed *Device Information* table into *SPI Clock at 1MSPS* table 1
- Changed front-page diagram..... 1
- Changed REFBUFOUT pin description from "Reference buffer output, ADC reference input" to "Internal reference buffer output, external reference input"..... 3
- Changed DV_{DD} range in condition line of Electrical Characteristics from 2.35V to 3.6V to 1.65V to 5.5V..... 7
- Changed maximum value for DV_{DD} range in *Electrical Characteristics*, *Timing Requirements*, and *Switching Characteristics* from 3.6V to 5.5V..... 7
- Added T_A = 25°C to reference buffer offset voltage test condition in *Electrical Characteristics* table..... 7
- Changed input offset thermal drift typ value from 10 to 1..... 7
- Added f_{IN} = 2kHz test condition to SFDR in *Electrical Characteristics* table 7
- Added new conditions to serial clock frequency in the *Timing Requirements* table..... 9
- Changed serial clock time period in *Timing Characteristics* table 9
- Added serial clock frequency conditions in *Timing Characteristics* table 9
- Changed serial clock time period in *Timing Characteristics* table 9
- Added strobe output time to *Switching Characteristics* table..... 10
- Added descriptive text and one figure to the *Reference Buffer Module* section..... 20
- Deleted text from first note element regarding data transfer activity in zone 2..... 33
- Added new option bullet for multiSPI digital interface module in *Data Transfer Protocols* section 35
- Added new note (1) for SCLK in Table 9 45
- Deleted "For the ADS892xB, limit the value of R_{FLT} to a maximum of 2.5Ω to avoid any significant degradation in linearity performance. " from the last paragraph of the *Charge Kickback Filter* section..... 58
- Changed *Data Acquisition (DAQ) Circuit for Lowest Distortion and Noise Performance...* section for clarity.. 60
- Added more design parameters to *Design Parameters* table..... 60
- Changed *Detailed Design Procedure* section for clarity..... 60
- Added two new application curves..... 61
- Added new typical application subsection 62

Changes from Revision * (June 2016) to Revision A (July 2016) **Page**

- Changed from product preview to production data 1
- Changed DV_{DD} specified throughput value in the *Recommended Operating Conditions* from 3.6V to 5.5V..... 5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS8920BRGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8920B
ADS8920BRGER.B	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8920B
ADS8920BRGET	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8920B
ADS8920BRGET.B	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8920B
ADS8920BRGETG4	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8920B
ADS8920BRGETG4.B	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8920B
ADS8922BRGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8922B
ADS8922BRGER.B	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8922B
ADS8922BRGET	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8922B
ADS8922BRGET.B	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8922B
ADS8924BRGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8924B
ADS8924BRGER.B	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8924B
ADS8924BRGET	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8924B
ADS8924BRGET.B	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8924B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

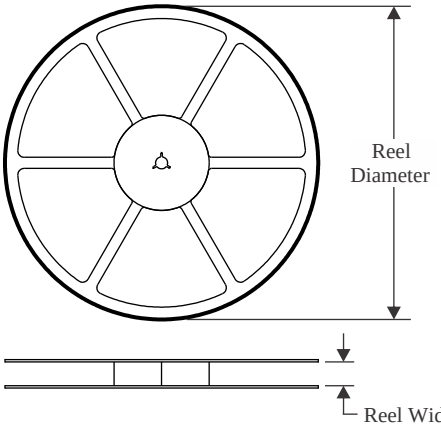
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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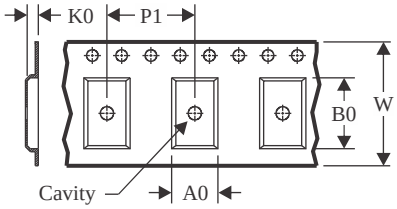
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

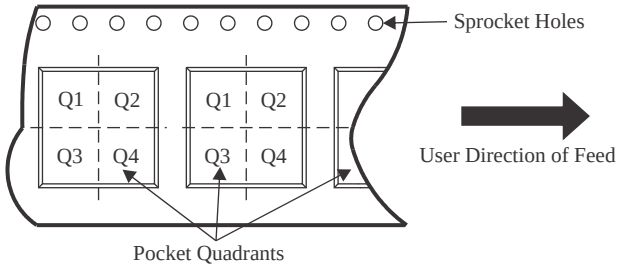


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

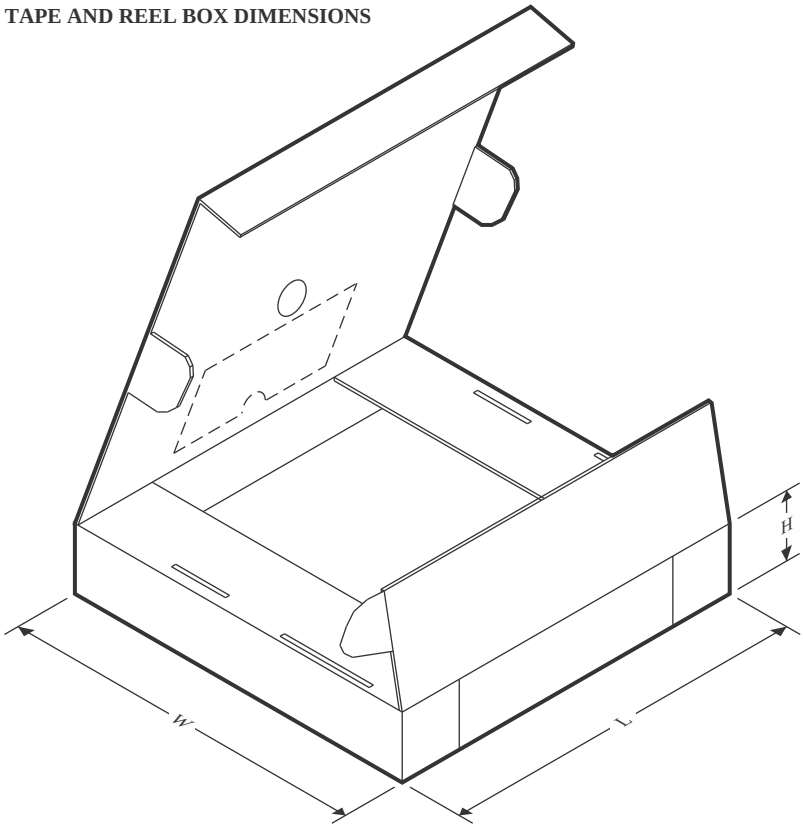
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8920BRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8920BRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8920BRGETG4	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8922BRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8922BRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8924BRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8924BRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

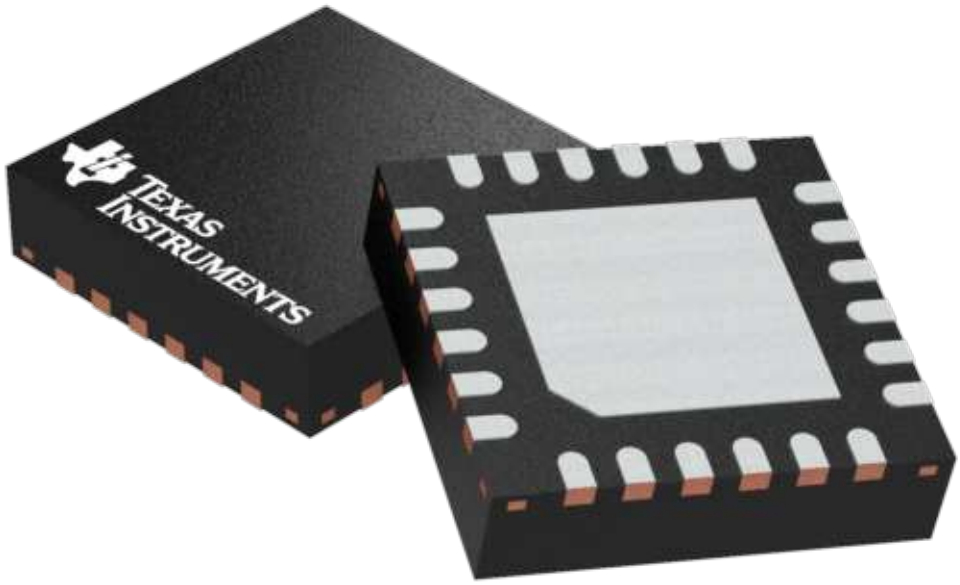


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8920BRGER	VQFN	RGE	24	3000	346.0	346.0	33.0
ADS8920BRGET	VQFN	RGE	24	250	210.0	185.0	35.0
ADS8920BRGETG4	VQFN	RGE	24	250	210.0	185.0	35.0
ADS8922BRGER	VQFN	RGE	24	3000	346.0	346.0	33.0
ADS8922BRGET	VQFN	RGE	24	250	210.0	185.0	35.0
ADS8924BRGER	VQFN	RGE	24	3000	346.0	346.0	33.0
ADS8924BRGET	VQFN	RGE	24	250	210.0	185.0	35.0

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



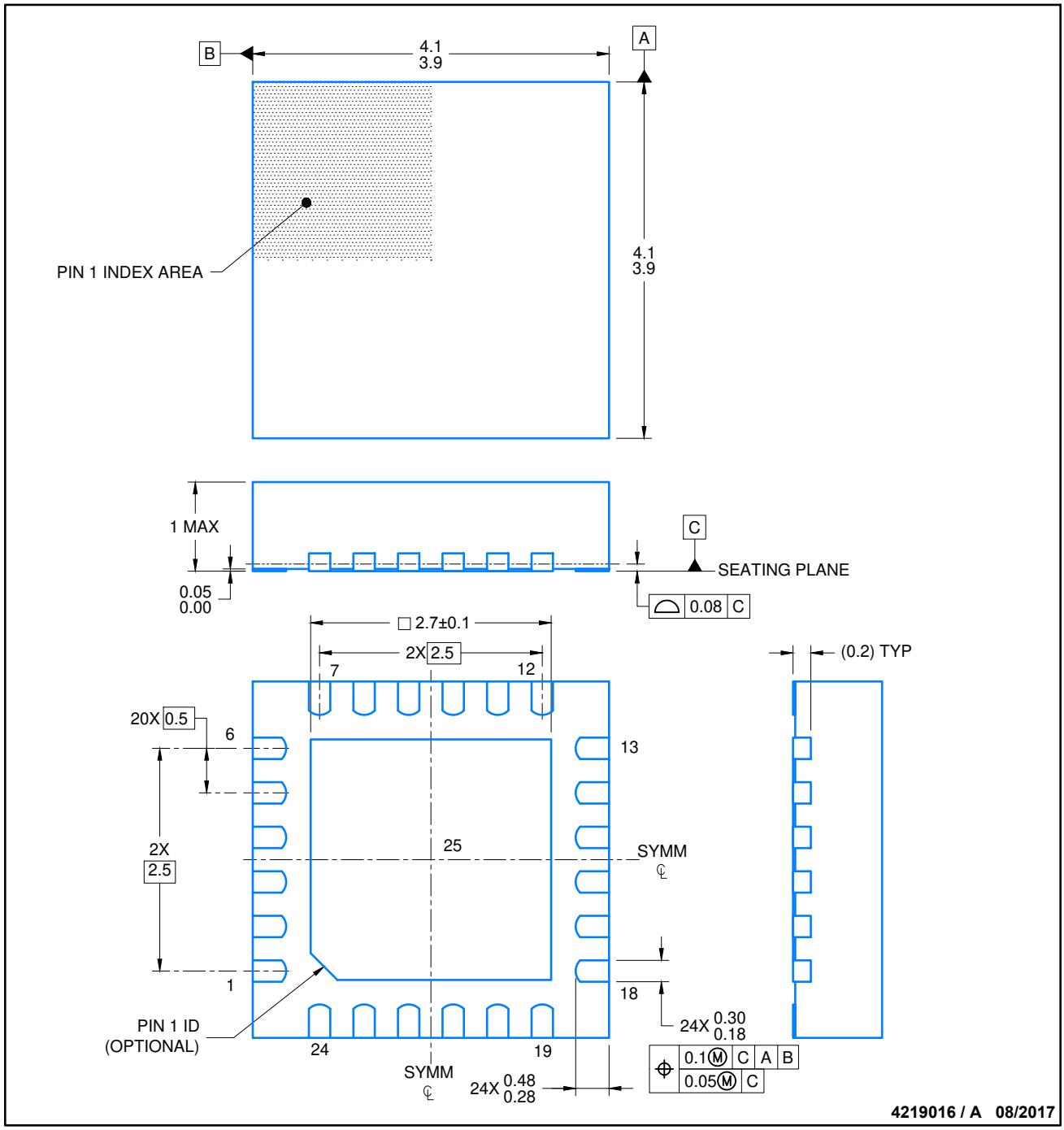
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGE0024H

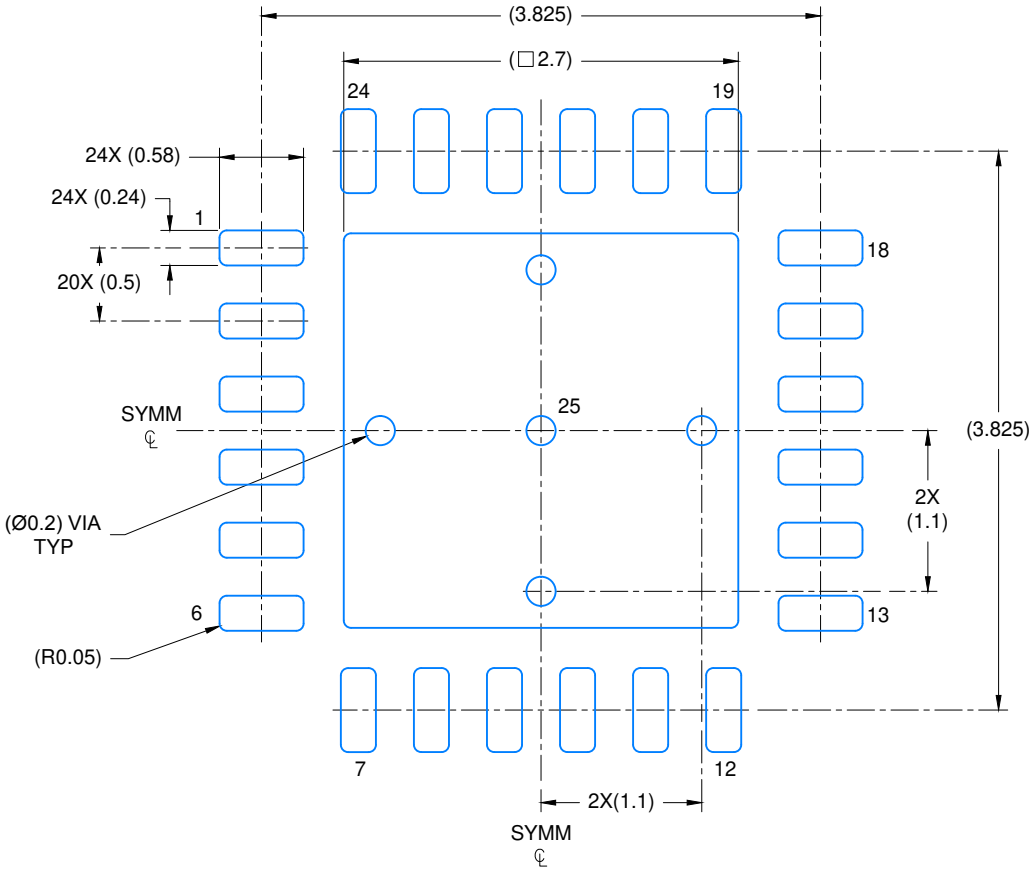
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



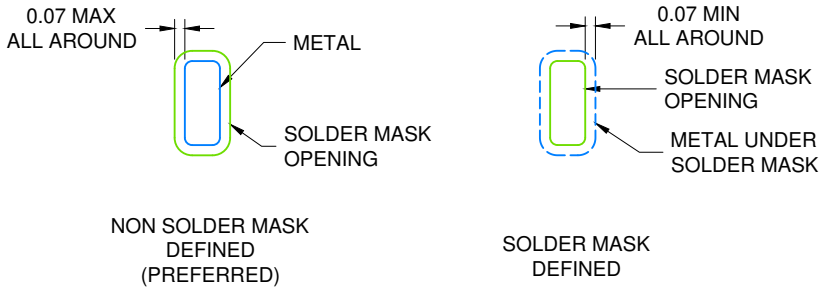
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X

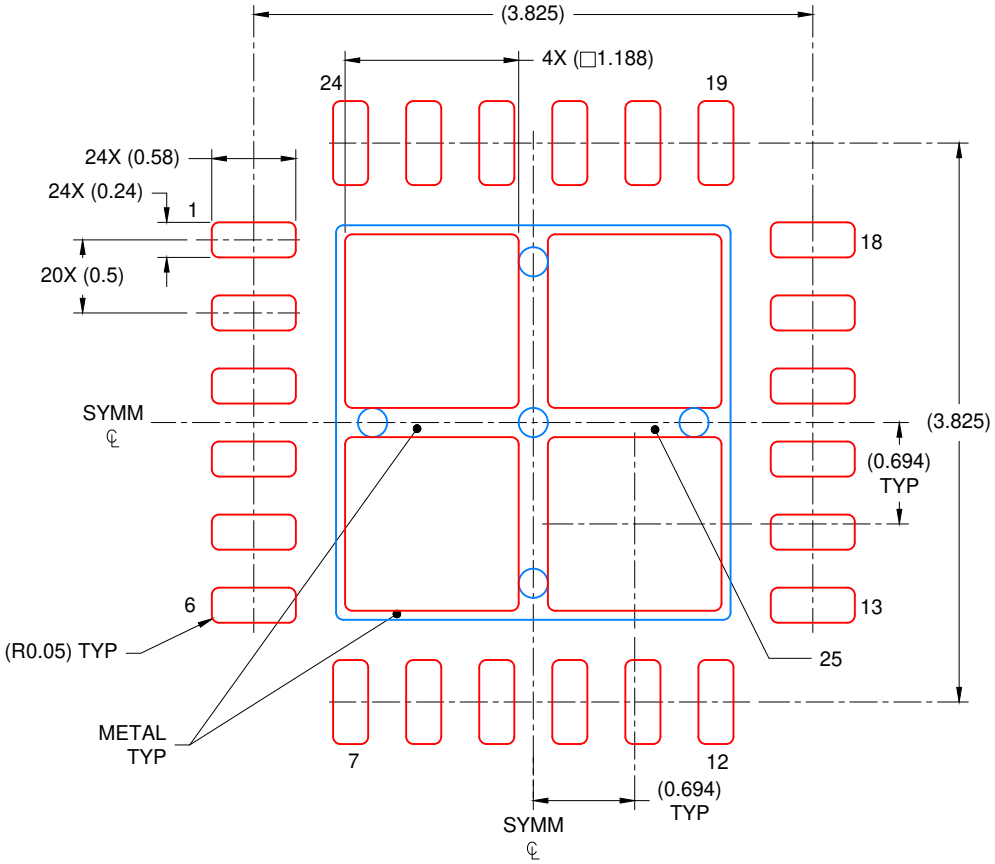


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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Last updated 10/2025