AFE4403 Ultra-Small, Integrated Analog Front-End for Heart Rate Monitors and Low-Cost Pulse Oximeters

1 Features

- Fully-Integrated AFE for Pulse Oximeter and Heart Rate Monitoring Applications:
- Transmit:
  - Integrated Dual LED Driver (H-Bridge or Common Anode)
  - Option for a Third LED Support for Optimized SPO2, HRM, or Multi-Wavelength HRM
  - Up to 110-dB Dynamic Range
  - LED Current:
    - Programmable to 100 mA with 8-Bit Current Resolution
  - 30 µA + Average LED Current
  - Programmable LED On-Time
  - Independent LED2 and LED1 Current Reference
- Receive Channel with High Dynamic Range:
  - 22-Bit Output in Twos Complement Format
  - Up to 105-dB Dynamic Range
  - Low Power: < 650 µA
  - Dynamic Power-Down Mode to Reduce Current to 300 µA
  - Adaptable to a Very Wide Range of Signal Amplitudes:
    - Total Programmable Gain: 10 kΩ to 4 MΩ
  - Integrated Digital Ambient Estimation and Subtraction
- Flexible Clocking by External Clock or Crystal:
  - Pulse Frequency: 62.5 SPS to 2000 SPS
  - Flexible Pulse sequencing and Timing Control
  - Input Clock Range: 4 MHz (Min) to 60 MHz (Max)
- Integrated Fault Diagnostics:
  - Photodiode and LED Open and Short Detection
- Supplies:
  - Rx = 2.0 V to 3.6 V
  - Tx = 3.0 V to 5.25 V
- Package: Compact DSBGA-36 (3.07 mm × 3.07 mm × 0.5 mm)
- Specified Temperature Range: 0°C–20°C to 70°C

2 Applications

- Medical Pulse Oximeter Applications
- Optical HRM
- Industrial Photometry Applications

3 Description

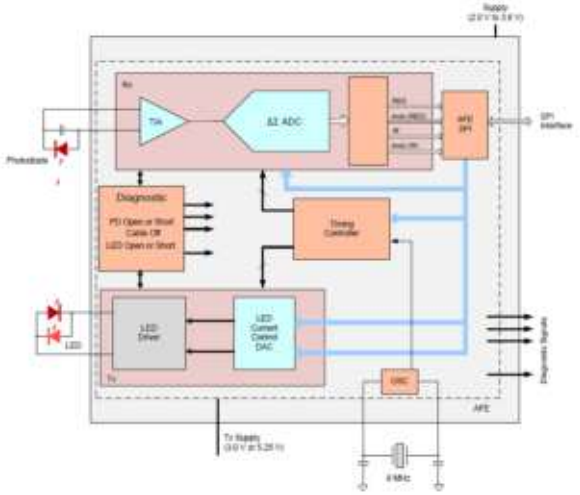
The AFE4403 is a fully-integrated analog front-end (AFE) ideally suited for pulse oximeter applications. The device consists of a low-noise receiver channel with an integrated analog-to-digital converter (ADC), an LED transmit section, and diagnostics for sensor and LED fault detection. The device is a very configurable timing controller. This flexibility enables the user to have complete control of the device timing characteristics. To ease clocking requirements and provide a low-jitter clock to the AFE4403, an oscillator is also integrated that functions from an external crystal. The device communicates to an external microcontroller or host processor using an SPI™ interface.

The device is a complete AFE solution packaged in a single, compact DSBGA-36 (3.07 mm × 3.07 mm × 0.5 mm) and is specified over the operating temperature range of –20°C to 70°C.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
AFE4403	DSBGA (36)	3.07 mm × 3.07 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



Block Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Revision History....3
5 Device Family Options....4
6 Pin Configuration and Functions....5
7 Specifications....7
7.1 Absolute Maximum Ratings....7
7.2 ESD Ratings....7
7.3 Recommended Operating Conditions....8
7.4 Thermal Information....8
7.5 Electrical Characteristics....9
7.6 Timing Requirements....13
7.7 Timing Requirements: Supply Ramp and Power-Down....14
7.8 Typical Characteristics....16
8 Detailed Description....22
8.1 Overview....22
8.2 Functional Block Diagram....22
8.3 Feature Description....23
8.4 Device Functional Modes....47
8.5 Programming....57
8.6 Register Maps....60
9 Application Information Disclaimer....84
9.1 Application Information....84
9.2 Typical Application....84
10 Power Supply Recommendations....88
10.1 Power Consumption Considerations....89
11 Layout....91
11.1 Layout Guidelines....91
11.2 Layout Example....91
12 Device and Documentation Support....92
12.1 Trademarks....92
12.2 Electrostatic Discharge Caution....92
12.3 Glossary....92
13 Mechanical, Packaging, and Orderable Information....92

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4 Revision History

Changes from Revision B (July 2014) to Revision C (February 2021) **Page**

- Moved the Storage temperature range from the *ESD* table to the *Absolute Maximum Ratings* table....7
- Added paragraph starting *"ADC_RDY is an interrupt issued by the AFE ...."* in the *ADC Operation and Averaging Module* section....47
- Changed figure *Averaging Module* in the *ADC Operation and Averaging Module* section....47
- Changed Section *Operation Without Averaging* 48
- Changed the introduction paragraph in Section *Operation With Averaging* 48
- Changed all the bullet points in Section *Operation With Averaging* 48
- Deleted the paragraph starting with "When the number of averages is 0..." in Section *Operation With Averaging* 48
- Changed *Figure - "ADC Data Without Averaging (When Number of Averages = 0)"* in Section *Operation With Averaging* 48
- Added Note after *Figure - "ADC Data Without Averaging (When Number of Averages = 0)"* in Section *Operation With Averaging* 48
- Changed *Figure - "ADC Data with Averaging Enabled"* in Section *Operation With Averaging* 48
- Added Note after *Figure - "ADC Data with Averaging Enabled"* in Section *Operation With Averaging* 48
- Changed the paragraph startng with "The sequence of the..." in Section *Dynamic Power-Down Mode* 52
- Added paragraph starting *"The time window between the ADC_RDY ...."* in Section *Dynamic Power-Down Mode* 52
- Changed LED2VAL[23:0] bit description in Section *AFE Register Description* 63
- Changed ALED2VAL[23:0] bit description in Section *AFE Register Description* 63
- Changed LED1VAL[23:0] bit description in Section *AFE Register Description* 63
- Changed ALED1VAL[23:0] bit description in Section *AFE Register Description* 63
- Changed LED2-ALED2VAL[23:0] bit description in Section *AFE Register Description* 63
- Changed LED1-ALED1VAL[23:0] bit description in Section *AFE Register Description* 63

Changes from Revision A (June 2014) to Revision B (July 2014) **Page**

- Changed Pin Configuration diagram: changed *Top View* to *Bottom View* 5
- Added footnote to Figure 8-6 28

Changes from Revision * (May 2014) to Revision A (June 2014) **Page**

- Changed document status to Production Data 1
- Changed first and third sub-bullets of *Flexible Clocking* Features bullet 1
- Changed MIN to NOM in Body Size column of Device Information table 1
- Added Device Family Options table and Pin Configuration and Functions section....4
- Added Specifications section....7
- Added *Application and Implementation* section....84
- Added *Power Supply Recommendations* section 88
- Added Layout section....91

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5 Device Family Options

PRODUCT	PACKAGE-LEAD	LED DRIVE CONFIGURATION	LED DRIVE CURRENT (mA, max)	Tx POWER SUPPLY (V)
AFE4400	VQFN-40	Bridge, push-pull	50	3 to 5.25
AFE4490	VQFN-40	Bridge, push-pull	50, 75, 100, 150, and 200	3 to 5.25
AFE4403	DSBGA-36	Bridge, push-pull	25, 50, 75, and 100	3 to 5.25

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6 Pin Configuration and Functions

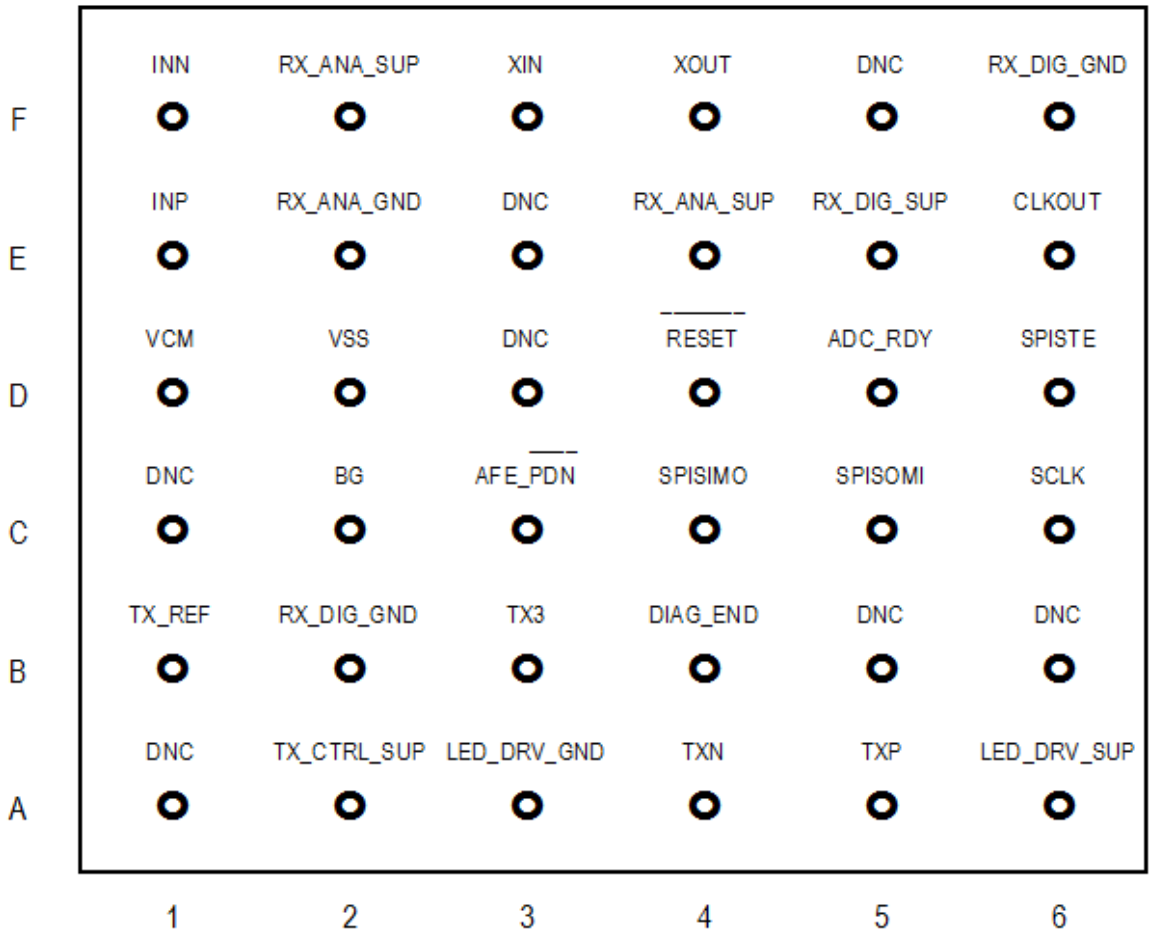


Figure 6-1. YZP Package, DSBGA-36, (Bottom View)

Table 6-1. Pin Functions

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
ADC_RDY	D5	Digital	Output signal that indicates ADC conversion completion. Can be connected to the interrupt input pin of an external microcontroller.
AFE_ $\overline{\text{PDN}}$	C3	Digital	AFE-only power-down input; active low. Can be connected to the port pin of an external microcontroller.
BG	C2	Reference	Decoupling capacitor for internal band-gap voltage to ground. Connect a decoupling capacitor to ground. To achieve the lowest transmitter noise, use a capacitor value of 2.2 µF. To reduce the recovery time from power-down (from 1 s to 0.1 s), use a capacitor value of 0.1 µF instead—but with slightly degraded transmitter noise.
CLKOUT	E6	Digital	Buffered 4-MHz output clock output. Can be connected to the clock input pin of an external microcontroller.
DIAG_END	B4	Digital	Output signal that indicates completion of diagnostics. Can be connected to the port pin of an external microcontroller.
DNC(1)	C1, A1, E3, D3, F5, B5, B6	—	Do not connect these pins. Leave as open circuit.
INN	F1	Analog	Receiver input pin. Connect to photodiode anode.
INP	E1	Analog	Receiver input pin. Connect to photodiode cathode.
LED_DRV_GND	A3	Supply	LED driver ground pin, H-bridge. Connect to common board ground.

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Table 6-1. Pin Functions (continued)

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
LED_DRV_SUP	A6	Supply	LED driver supply pin, H-bridge. Connect to an external power supply capable of supplying the large LED current, which is drawn by this supply pin.
$\overline{\text{RESET}}$	D4	Digital	AFE-only reset input, active low. Can be connected to the port pin of an external microcontroller
RX_ANA_GND	E2	Supply	Rx analog ground pin. Connect to common board ground.
RX_ANA_SUP	F2, E4	Supply	Rx analog supply pin; 0.1-µF decoupling capacitor to ground
RX_DIG_GND	B2, F6	Supply	Rx digital ground pin. Connect to common board ground.
RX_DIG_SUP	E5	Supply	Rx digital supply pin; 0.1-µF decoupling capacitor to ground
SCLK	C6	SPI	SPI clock pin
SPISIMO	C4	SPI	SPI serial in master out
SPISOMI	C5	SPI	SPI serial out master in
SPISTE	D6	SPI	SPI serial interface enable
TX_CTRL_SUP	A2	Supply	Transmit control supply pin (0.1-µF decoupling capacitor to ground)
TX_REF	B1	Reference	Transmitter reference voltage, 0.25 V default after reset. Connect a decoupling capacitor to ground. To achieve the lowest transmitter noise, use a capacitor value of 2.2 µF. To reduce the recovery time from power-down (from 1 s to 0.1 s), use a capacitor value of 0.1 µF instead—but with slightly degraded transmitter noise.
TXN	A4	Analog	LED driver out. Connect to LED in common anode or H-bridge configuration.
TXP	A5	Analog	LED driver out. Connect to LED in common anode or H-bridge configuration.
TX3	B3	Analog	LED driver out for third LED. Connect to optional third LED supported in common anode configuration.
VCM	D1	Reference	Input common-mode voltage output. This signal can be used to shield (guard) the INP, INN traces. If used as a shield, then connect a series resistor (1 kΩ) and a decoupling capacitor (10 nF) to ground. If VCM is not used externally, then these external components are not required.
VSS	D2	Supply	Substrate ground. Connect to common board ground.
XOUT	F4	Digital	Crystal oscillator pins. Connect an external crystal between these pins with the correct load capacitor (as specified by vendor) to ground.
XIN	F3	Digital	Crystal oscillator pins. Connect an external crystal between these pins with the correct load capacitor (as specified by vendor) to ground.

(1) Leave pins as open circuit. Do not connect.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
RX_ANA_SUP, RX_DIG_SUP to RX_ANA_GND, RX_DIG_GND		–0.3	4	V
TX_CTRL_SUP, LED_DRV_SUP to LED_DRV_GND		–0.3	6	V
RX_ANA_GND, RX_DIG_GND to LED_DRV_GND		–0.3	0.3	V
Analog inputs		RX_ANA_GND – 0.3	RX_ANA_SUP + 0.3	V
Digital inputs		RX_DIG_GND – 0.3	RX_DIG_SUP + 0.3	V
Input current to any pin except supply pins(2)			±7	mA
Input current	Momentary		±50	mA
	Continuous		±7	mA
Operating temperature range		0 –20	70	°C
Maximum junction temperature, T_J			125	°C
Storage temperature range, T_{stg}		–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing beyond the supply rails must be current-limited to 10 mA or less.

7.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–1000	1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–250	250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	MAX	UNIT
SUPPLIES					
RX_ANA_SUP	AFE analog supply		2.0	3.6	V
RX_DIG_SUP	AFE digital supply		2.0	3.6	V
TX_CTRL_SUP	Transmit controller supply		3.0	5.25	V
LED_DRV_SUP	Transmit LED driver supply	H-bridge	[3.0 or (0.75 + V_{LED} + V_{CABLE})(1) (2), whichever is greater]	5.25	V
		Common anode configuration	[3.0 or (0.5 + V_{LED} + V_{CABLE})(1) (2), whichever is greater]	5.25	V
	Difference between LED_DRV_SUP and TX_CTRL_SUP		–0.3	0.3	V
TEMPERATURE					
	Specified temperature range		–20	70	°C
	Storage temperature range		–60	150	°C

(1) V_{LED} refers to the maximum voltage drop across the external LED (at maximum LED current) connected between the TXP and TXN pins (in H-bridge mode) and from the TXP and TXN pins to LED_DRV_SUP (in the common anode configuration).

(2) V_{CABLE} refers to voltage drop across any cable, connector, or any other component in series with the LED.

7.4 Thermal Information

THERMAL METRIC(1)		AFE4403 YZP (WCSP) 36 BALLS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	8.5	
ψ_{JT}	Junction-to-top characterization parameter	0.8	
ψ_{JB}	Junction-to-board characterization parameter	8.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

Minimum and maximum specifications are at T_A = –20°C to 70°C, typical specifications are at 25°C. Crystal mode enabled, detector capacitor = 50 pF differential, ADC averaging set to maximum allowed for each PRF, TX_REF voltage set to 0.5 V, and CLKOUT tri-stated, at RX_ANA_SUP = RX_DIG_SUP = 3 V, TX_CTRL_SUP = LED_DRV_SUP = 3.3 V, stage 2 amplifier disabled, and f_{CLK} = 8 MHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PERFORMANCE (Full-Signal Chain)						
I_{IN_FS}	Full-scale input current	R_F = 10 kΩ		50		µA
		R_F = 25 kΩ		20		µA
		R_F = 50 kΩ		10		µA
		R_F = 100 kΩ		5		µA
		R_F = 250 kΩ		2		µA
		R_F = 500 kΩ		1		µA
		R_F = 1 MΩ		0.5		µA
PRF	Pulse repetition frequency		62.5		2000	SPS
DC_{PRF}	PRF duty cycle				25%	
CMRR	Common-mode rejection ratio	f_{CM} = 50 Hz and 60 Hz, LED1 and LED2 with R_{SERIES} = 500 kΩ, R_F = 500 kΩ		75		dB
		f_{CM} = 50 Hz and 60 Hz, LED1-AMB and LED2-AMB with R_{SERIES} = 500 kΩ, R_F = 500 kΩ		95		dB
$PSRR_{LED}$	PSRR, transmit LED driver	With respect to ripple on LED_DRV_SUP		75		dB
$PSRR_{Tx}$	PSRR, transmit control	With respect to ripple on TX_CTRL_SUP		60		dB
$PSRR_{Rx}$	PSRR, receiver	With respect to ripple on RX_ANA_SUP and RX_DIG_SUP		60		dB
	Total integrated noise current, input-referred (receiver with transmitter loop back, 0.1-Hz to 20-Hz bandwidth)	R_F = 100 kΩ, PRF = 600 Hz, duty cycle = 5%		25		pA_{RMS}
		R_F = 500 kΩ, PRF = 600 Hz, duty cycle = 5%		6		pA_{RMS}
RECEIVER FUNCTIONAL BLOCK LEVEL SPECIFICATION						
	Total integrated noise current, input referred (receiver alone) over 0.1-Hz to 20-Hz bandwidth	R_F = 500 kΩ, ambient cancellation enabled, stage 2 gain = 4, PRF = 1200 Hz, LED duty cycle = 25%		3.2		pA_{RMS}
		R_F = 500 kΩ, ambient cancellation enabled, stage 2 gain = 4, PRF = 1200 Hz, LED duty cycle = 5%		5.3		pA_{RMS}
I-V TRANSIMPEDANCE AMPLIFIER						
G	Gain	R_F = 10 kΩ to 1 MΩ	See the *Receiver Channel* section for details			V/µA
	Gain accuracy			±7%		
	Feedback resistance	R_F	10k, 25k, 50k, 100k, 250k, 500k, and 1M			Ω
	Feedback resistor tolerance	R_F		±20%		
	Feedback capacitance	C_F	5, 10, 25, 50, 100, and 250			pF
	Feedback capacitor tolerance	C_F		±20%		
	Full-scale differential output voltage			1		V
	Common-mode voltage on input pins	Set internally		0.9		V
	External differential input capacitance	Includes equivalent capacitance of photodiode, cables, EMI filter, and so forth	10		1000	pF
	Shield output voltage, V_{CM}	With a 1-kΩ series resistor and a 10-nF decoupling capacitor to ground	0.8	0.9	1	V

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7.5 Electrical Characteristics (continued)

Minimum and maximum specifications are at T_A = –20°C to 70°C, typical specifications are at 25°C. Crystal mode enabled, detector capacitor = 50 pF differential, ADC averaging set to maximum allowed for each PRF, TX_REF voltage set to 0.5 V, and CLKOUT tri-stated, at RX_ANA_SUP = RX_DIG_SUP = 3 V, TX_CTRL_SUP = LED_DRV_SUP = 3.3 V, stage 2 amplifier disabled, and f_{CLK} = 8 MHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AMBIENT CANCELLATION STAGE						
	Gain			0, 3.5, 6, 9.5, and 12		dB
	Current DAC range		0		10	µA
	Current DAC step size			1		µA
LOW-PASS FILTER						
	Low-pass corner frequency	3-dB attenuation		500		Hz
	Pass-band attenuation, 2 Hz to 10 Hz	Duty cycle = 25%		0.004		dB
		Duty cycle = 10%		0.041		dB
	Filter settling time	After diagnostics mode		28		ms
ANALOG-TO-DIGITAL CONVERTER						
	Resolution				22	Bits
	Sample rate	See the *ADC Operation and Averaging Module* section		4 × PRF		SPS
	ADC full-scale voltage			±1.2		V
	ADC conversion time	See the *ADC Operation and Averaging Module* section			PRF / 4	µs
	ADC reset time[2]		2			t_{CLK}
TRANSMITTER						
	Output current range			Selectable, 0 to 100 (see the LEDCNTRL: LED Control Register for details)		mA
	LED current DAC error			±10%		
	Output current resolution			8		Bits
	Transmitter noise dynamic range, over 0.1-Hz to 20-Hz bandwidth, TX_REF set to 0.5 V	At 25-mA output current		110		dB
		At 50-mA output current		110		dB
	Minimum sample time of LED1 and LED2 pulses			50		µs
	LED current DAC leakage current	LED_ON = 0		1		µA
		LED_ON = 1		50		µA
	LED current DAC linearity	Percent of full-scale current		0.50		%
	Output current settling time (with resistive load)	From zero current to 50 mA		7		µs
		From 50 mA to zero current		7		µs
DIAGNOSTICS						
	Duration of diagnostics state machine	Start of diagnostics after the DIAG_EN register bit is set. End of diagnostic is indicated by DIAG_END going high.		16		ms
	Open fault resistance			> 100		kΩ
	Short fault resistance			< 10		kΩ
INTERNAL OSCILLATOR						
f_{CLKOUT}	CLKOUT frequency	With an 8-MHz crystal connected to the XIN, XOUT pins		4		MHz
	CLKOUT duty cycle			50%		
	Crystal oscillator start-up time	With an 8-MHz crystal connected to the XIN, XOUT pins		200		µs

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7.5 Electrical Characteristics (continued)

Minimum and maximum specifications are at T_A = –20°C to 70°C, typical specifications are at 25°C. Crystal mode enabled, detector capacitor = 50 pF differential, ADC averaging set to maximum allowed for each PRF, TX_REF voltage set to 0.5 V, and CLKOUT tri-stated, at RX_ANA_SUP = RX_DIG_SUP = 3 V, TX_CTRL_SUP = LED_DRV_SUP = 3.3 V, stage 2 amplifier disabled, and f_{CLK} = 8 MHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL CLOCK						
	Maximum allowable external clock jitter	For SPO2 applications		50		ps
		For optical heart rate only			1000	ps
	External clock input frequency (1)	±2%	4	8	60	MHz
	External clock input voltage	Voltage input high (V_{IH})	0.75 × RX_DIG_SUP			V
		Voltage input low (V_{IL})	0.25 × RX_DIG_SUP			V
TIMING						
	Wake-up time from complete power-down			1000		ms
	Wake-up time from Rx power-down			100		µs
	Wake-up time from Tx power-down			1000		ms
$t_{\overline{RESET}}$	Active low $\overline{RESET}$ pulse duration			1		ms
$t_{DIAGEND}$	DIAG_END pulse duration at the completion of diagnostics			4		CLKOUT cycles
t_{ADCRDY}	ADC_RDY pulse duration			1		CLKOUT cycle
DIGITAL SIGNAL CHARACTERISTICS						
V_{IH}	Logic high input voltage	AFE_ $\overline{PDN}$, SCLK, SPISIMO, SPISTE, $\overline{RESET}$	0.8 DVDD	> 1.3	DVDD + 0.1	V
V_{IL}	Logic low input voltage	AFE_ $\overline{PDN}$, SCLK, SPISIMO, SPISTE, $\overline{RESET}$	–0.1	< 0.4	0.2 DVDD	V
I_{IN}	Logic input current	0 V < $V_{DigitalInput}$ < DVDD	–10		10	µA
V_{OH}	Logic high output voltage	DIAG_END, SPISOMI, ADC_RDY, CLKOUT	0.9 DVDD	> (RX_DIG_SUP – 0.2 V)		V
V_{OL}	Logic low output voltage	DIAG_END, SPISOMI, ADC_RDY, CLKOUT		< 0.4	0.1 DVDD	V
SUPPLY CURRENT						
	Receiver analog supply current	RX_ANA_SUP = 3.0 V, with 8-MHz clock running, Rx stage 2 disabled		0.6		mA
		RX_ANA_SUP = 3.0 V, with 8-MHz clock running, Rx stage 2 enabled		0.7		mA
		RX_ANA_SUP = 3.0 V, with 8-MHz clock running, Rx stage 2 disabled, external clock mode		0.49		mA
	Receiver digital supply current	RX_DIG_SUP = 3.0 V		0.15		mA
	LED driver supply current	With zero LED current setting		30		µA
	Transmitter control supply current			15		µA
	Complete power-down (using the AFE_ $\overline{PDN}$ pin)	Receiver current only (RX_ANA_SUP)		3		µA
		Receiver current only (RX_DIG_SUP)		3		µA
		Transmitter current only (LED_DRV_SUP)		1		µA
		Transmitter current only (TX_CTRL_SUP)		1		µA
	Power-down Rx alone	Receiver current only (RX_ANA_SUP)		200		µA
		Receiver current only (RX_DIG_SUP)		150		µA
	Power-down Tx alone	Transmitter current only (LED_DRV_SUP)		2		µA
		Transmitter current only (TX_CTRL_SUP)		2		µA

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7.5 Electrical Characteristics (continued)

Minimum and maximum specifications are at T_A = –20°C to 70°C, typical specifications are at 25°C. Crystal mode enabled, detector capacitor = 50 pF differential, ADC averaging set to maximum allowed for each PRF, TX_REF voltage set to 0.5 V, and CLKOUT tri-stated, at RX_ANA_SUP = RX_DIG_SUP = 3 V, TX_CTRL_SUP = LED_DRV_SUP = 3.3 V, stage 2 amplifier disabled, and f_{CLK} = 8 MHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER DISSIPATION							
Power-down with the AFE_PDN pin	LED_DRV_SUP	Does not include LED current.			1		µA
	TX_CTRL_SUP				1		µA
	RX_ANA_SUP				5		µA
	RX_DIG_SUP				0.1		µA
Power-down with the PDNAFE register bit	LED_DRV_SUP	Does not include LED current.			1		µA
	TX_CTRL_SUP				1		µA
	RX_ANA_SUP				15		µA
	RX_DIG_SUP				20		µA
Power-down Rx	LED_DRV_SUP	Does not include LED current.			30		µA
	TX_CTRL_SUP				15		µA
	RX_ANA_SUP				200		µA
	RX_DIG_SUP				150		µA
Power-down Tx	LED_DRV_SUP	Does not include LED current.			2		µA
	TX_CTRL_SUP				2		µA
	RX_ANA_SUP				600		µA
	RX_DIG_SUP				150		µA
After reset, with 8-MHz clock running	LED_DRV_SUP	Does not include LED current.			30		µA
	TX_CTRL_SUP				15		µA
	RX_ANA_SUP				600		µA
	RX_DIG_SUP				150		µA
With stage 2 mode enabled and 8-MHz clock running	LED_DRV_SUP	Does not include LED current.			30		µA
	TX_CTRL_SUP				15		µA
	RX_ANA_SUP				700		µA
	RX_DIG_SUP				150		µA
Dynamic power-down mode enabled	LED_DRV_SUP	Does not include LED current.	PRF = 100 Hz, PDN_CYCLE duration = 8 ms		7		µA
	TX_CTRL_SUP				5		µA
	RX_ANA_SUP				205		µA
	RX_DIG_SUP				150		µA

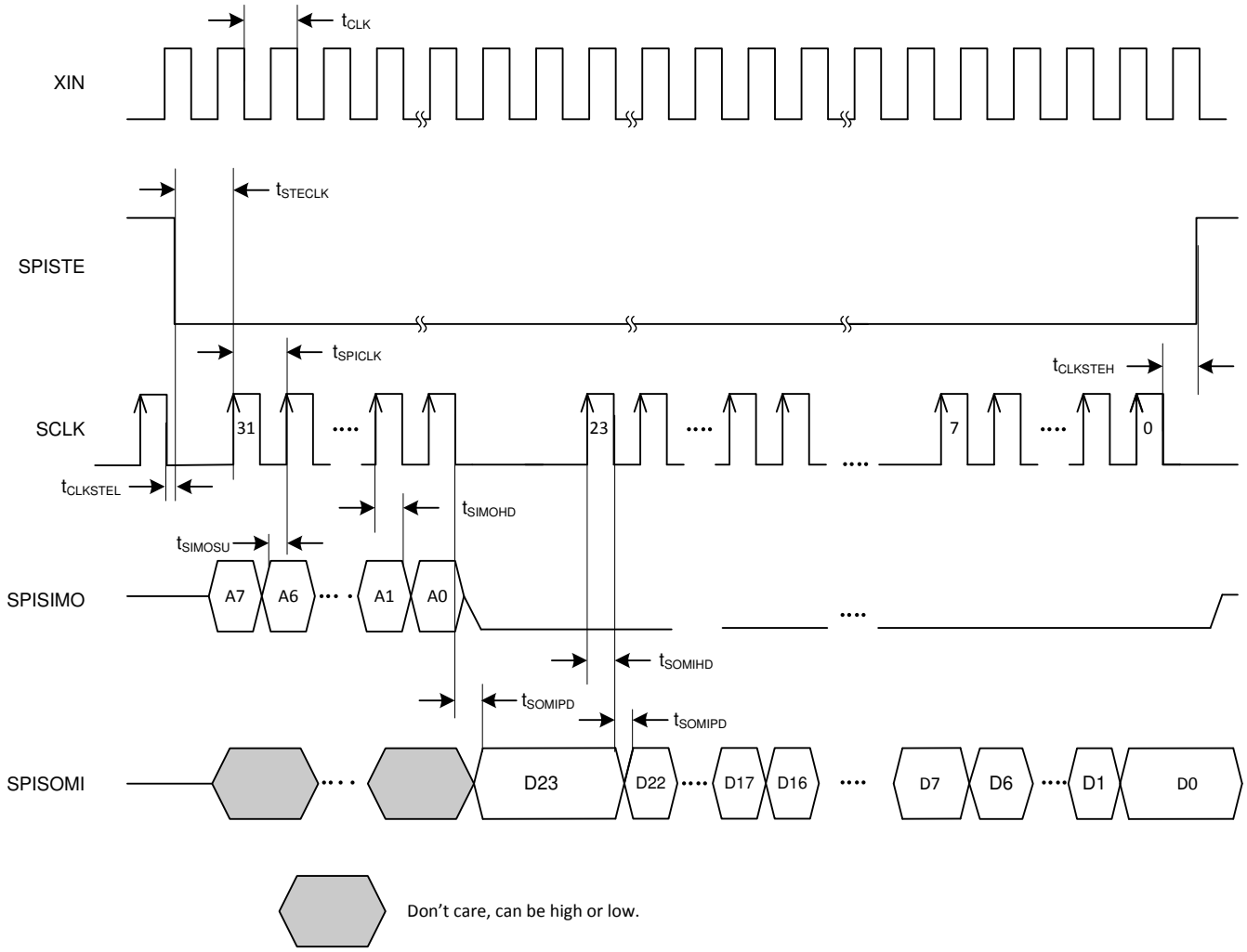
(1) Refer to the CLKDIV[2:0] register bits for a detailed list of input clock frequencies that are supported.

(2) A low ADC reset time can result in a small component of the LED signal leaking into the ambient phase. With an ADC reset of two clock cycles, a –60-dB leakage is expected. In many cases, this leakage does not affect system performance. However, if this crosstalk must be completely eliminated, a longer ADC reset time of approximately six clock cycles is recommended for t_{22}, t_{24}, t_{26}, and t_{28} in Figure 8-13.

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7.6 Timing Requirements

PARAMETER		MIN	TYP	MAX	UNIT
t_{CLK}	Clock frequency on the XIN pin		8		MHz
t_{SCLK}	Serial shift clock period	62.5			ns
t_{STECLK}	STE low to SCLK rising edge, setup time	10			ns
$t_{CLKSTEH,L}$	SCLK transition to SPI STE high or low	10			ns
t_{SIMOSU}	SIMO data to SCLK rising edge, setup time	10			ns
t_{SIMOHD}	Valid SIMO data after SCLK rising edge, hold time	10			ns
t_{SOMIPD}	SCLK falling edge to valid SOMI, setup time	17			ns
t_{SOMIHD}	SCLK rising edge to invalid data, hold time	0.5			t_{SCLK}



A. The SPI_READ register bit must be enabled before attempting a register read.
B. Specify the register address whose contents must be read back on A[7:0].
C. The AFE outputs the contents of the specified register on the SPISOMI pin.

Figure 7-1. Serial Interface Timing Diagram, Read Operation

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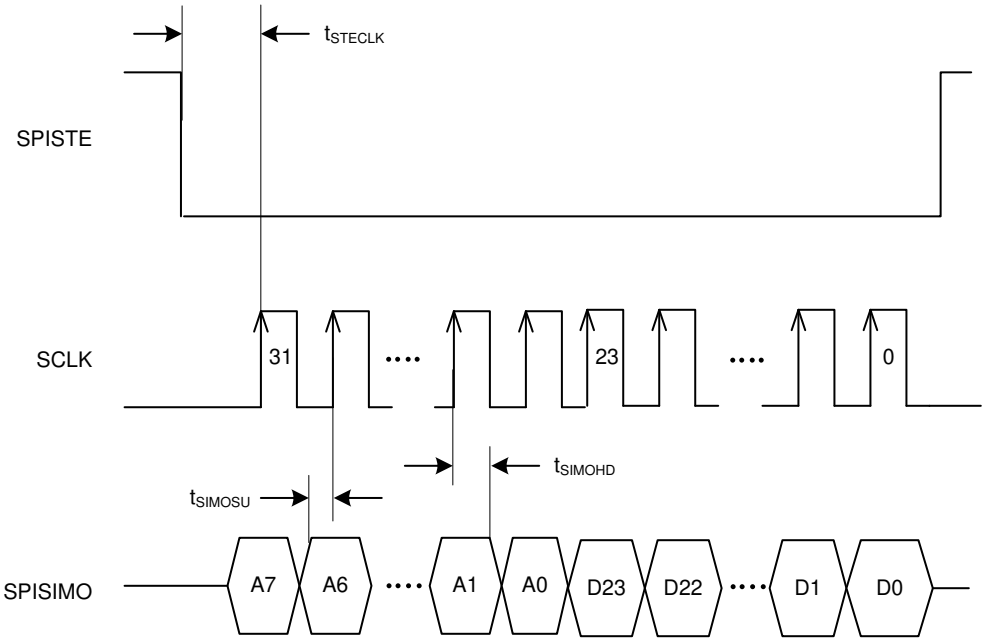


Figure 7-2. Serial Interface Timing Diagram, Write Operation

7.7 Timing Requirements: Supply Ramp and Power-Down

PARAMETER		VALUE
t_1	Time between Rx and Tx supplies ramping up	Keep as small as possible (for example, ±10 ms)
t_2	Time between both supplies stabilizing and high-going $\overline{\text{RESET}}$ edge	> 100 ms
t_3	$\overline{\text{RESET}}$ pulse duration	> 0.5 ms
t_4	Time between $\overline{\text{RESET}}$ and SPI commands	> 1 µs
t_5	Time between SPI commands and the ADC_ $\overline{\text{RESET}}$ which corresponds to valid data	> 3 ms of cumulative sampling time in each phase(1) (2) (3)
t_6	Time between $\overline{\text{RESET}}$ pulse and high-accuracy data coming out of the signal chain	> 1 s(3)
t_7	Time from AFE_ $\overline{\text{PDN}}$ high-going edge and $\overline{\text{RESET}}$ pulse(4)	> 100 ms
t_8	Time from AFE_ $\overline{\text{PDN}}$ high-going edge (or PDN_AFE bit reset) to high-accuracy data coming out of the signal chain	> 1 s(3)

(1) This time is required for each of the four switched RC filters to fully settle to the new settings. The same time is applicable whenever there is a change to any of the signal chain controls (for example, LED current setting, TIA gain, and so forth).

(2) If the SPI commands involve a change in the TX_REF value from its default, then there is additional wait time of approximately 1 s (for a 2.2-µF decoupling capacitor on the TX_REF pin).

(3) Dependent on the value of the capacitors on the BG and TX_REF pins. The 1-s wait time is necessary when the capacitors are 2.2 µF and scale down proportionate to the capacitor value. A very low capacitor (for example, 0.1 µF) on these pins causes the transmitter dynamic range to reduce to approximately 100 dB.

(4) After an active power-down from AFE_ $\overline{\text{PDN}}$, the device should be reset using a low-going $\overline{\text{RESET}}$ pulse.

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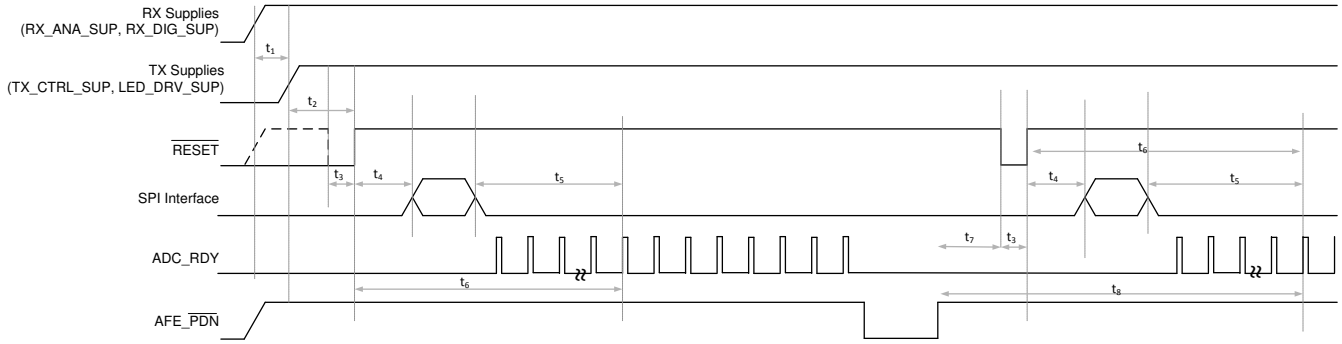


Figure 7-3. Supply Ramp and Hardware Power-Down Timing

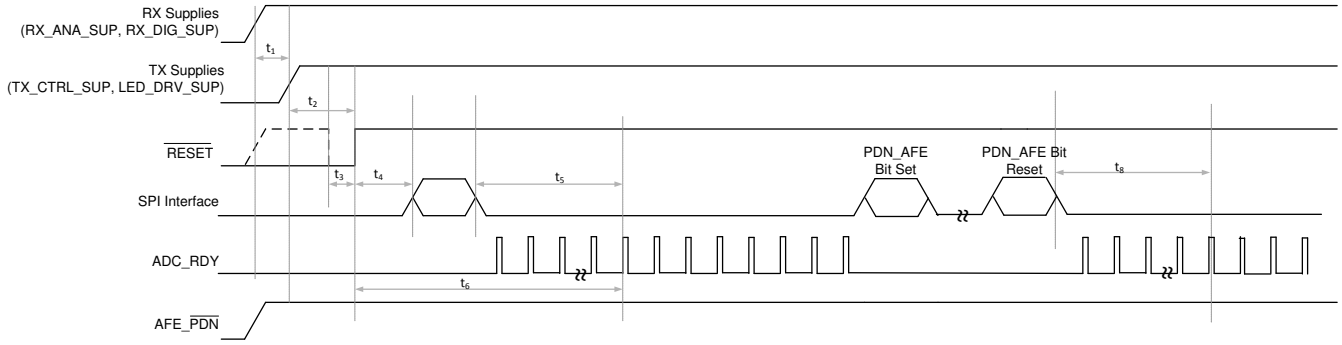


Figure 7-4. Supply Ramp and Software Power-Down Timing

7.8 Typical Characteristics

At PRF = 100 Hz, 25% duty cycle, R_F = 500 kΩ, C_F is adjusted to keep TIA time constant at 1/10th of sampling duration, All supplies at 3.3 V, 8-MHz external clock, CLKOUT tri-state, 1-µF capacitor on TX_REF and BG pins, detector C_{IN} = 50 pF, TX_REF = 0.5 V, ADC averaging = max allowed, and SNR in dBFS is noise referred to full-scale range of 2 V, unless otherwise noted.

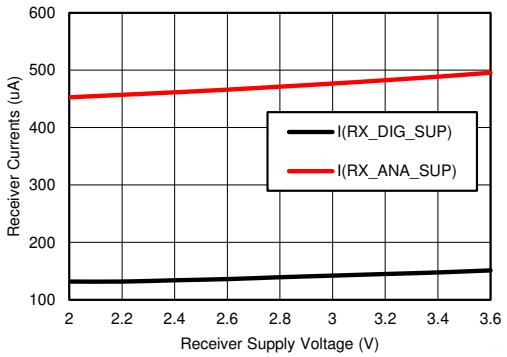
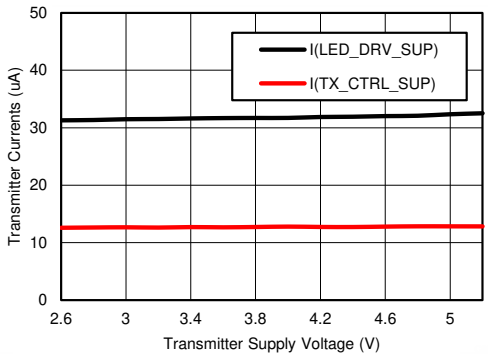
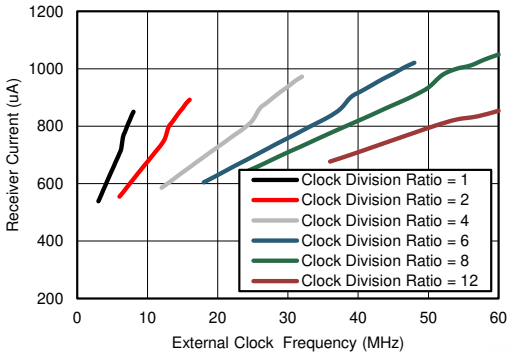


Figure 7-5. Receiver Currents vs Receiver Supply Voltage



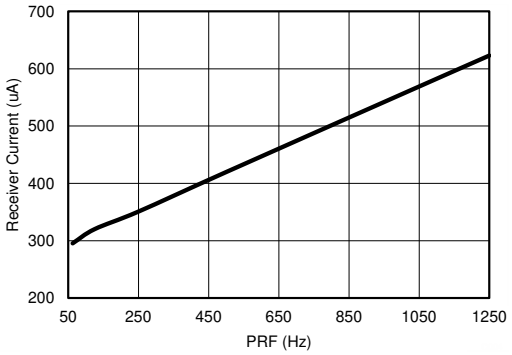
LED current = 0 mA

Figure 7-6. Transmitter Currents vs Transmitter Supply Voltage



PRF = 150 Hz

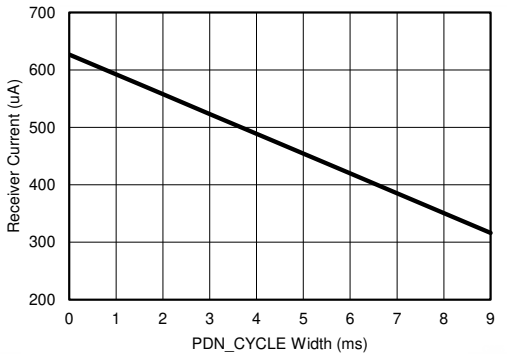
Figure 7-7. Receiver Currents (Analog and Digital) vs Clock Divider Ratio



Active window = 500 µs LED pulse = 100 µs

All four DYNAMIC bits set to 1

Figure 7-8. Receiver Current vs PRF in Dynamic Power-Down Mode



PRF = 100 Hz LED pulse = 100 µs

All four DYNAMIC bits set to 1

Figure 7-9. Receiver Current (Analog and Digital) vs Dynamic Power-Down Duty Cycle

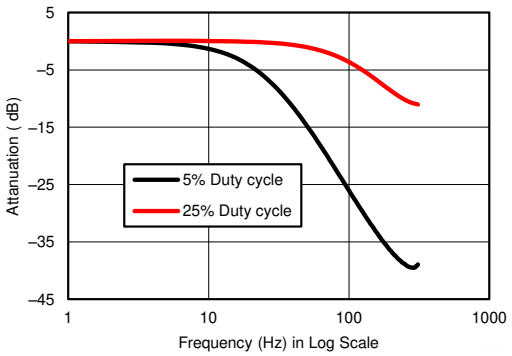


Figure 7-10. Filter Response vs Duty cycle

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7.8 Typical Characteristics (continued)

At PRF = 100 Hz, 25% duty cycle, R_F = 500 kΩ, C_F is adjusted to keep TIA time constant at 1/10th of sampling duration, All supplies at 3.3 V, 8-MHz external clock, CLKOUT tri-state, 1-µF capacitor on TX_REF and BG pins, detector C_{IN} = 50 pF, TX_REF = 0.5 V, ADC averaging = max allowed, and SNR in dBFS is noise referred to full-scale range of 2 V, unless otherwise noted.

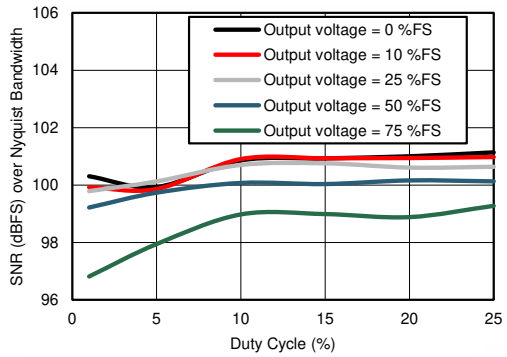


Figure 7-11. SNR over Nyquist Bandwidth vs Duty Cycle (Input Current with Tx-Rx Loopback)

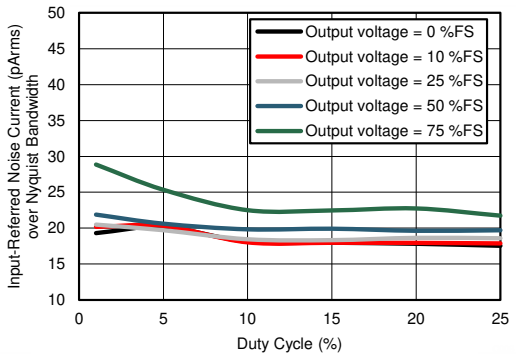


Figure 7-12. Input-Referred Noise Current over Nyquist Bandwidth vs Duty Cycle (Input Current with Tx-Rx Loopback)

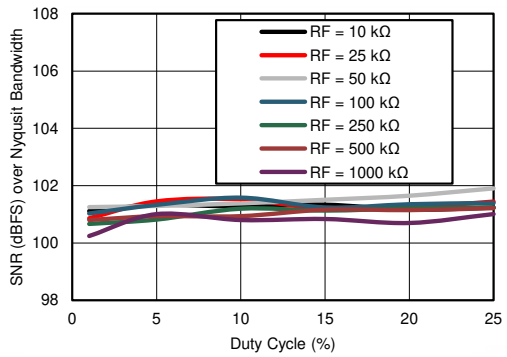


Figure 7-13. Receiver SNR over Nyquist Bandwidth vs Duty Cycle (Different Gain Settings)

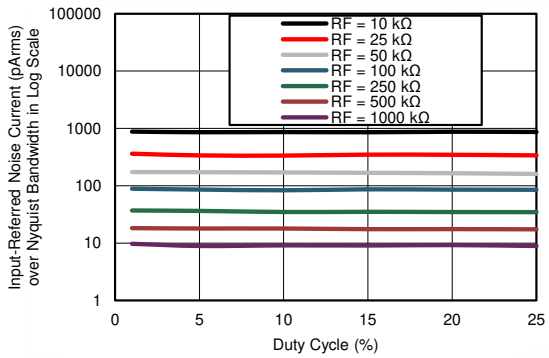


Figure 7-14. Receiver Input-Referred Noise Current over Nyquist Bandwidth vs Duty Cycle (Different Gain Settings)

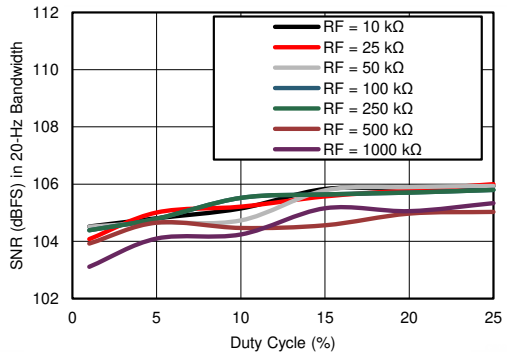


Figure 7-15. Receiver SNR in 20-Hz BW vs Duty Cycle (Different Gain Settings)

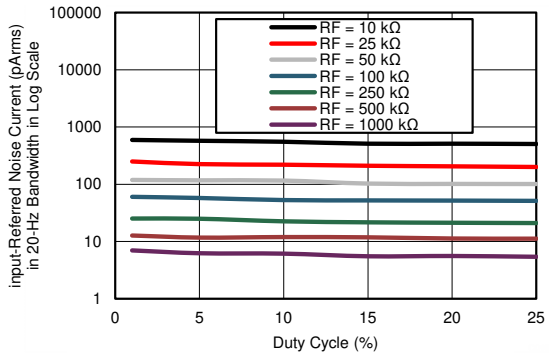


Figure 7-16. Receiver Input-Referred Noise Current in 20-Hz BW vs Duty Cycle (Different Gain Settings)

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7.8 Typical Characteristics (continued)

At PRF = 100 Hz, 25% duty cycle, R_F = 500 kΩ, C_F is adjusted to keep TIA time constant at 1/10th of sampling duration, All supplies at 3.3 V, 8-MHz external clock, CLKOUT tri-state, 1-µF capacitor on TX_REF and BG pins, detector C_{IN} = 50 pF, TX_REF = 0.5 V, ADC averaging = max allowed, and SNR in dBFS is noise referred to full-scale range of 2 V, unless otherwise noted.

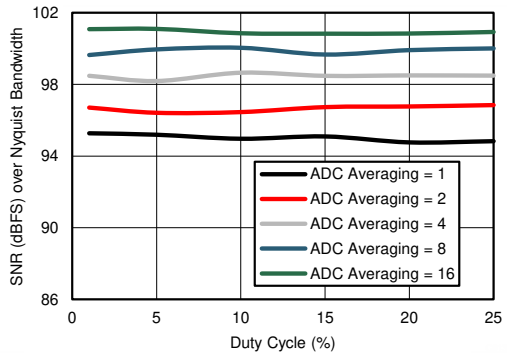


Figure 7-17. Receiver SNR over Nyquist Bandwidth vs Duty Cycle (Different ADC Averaging)

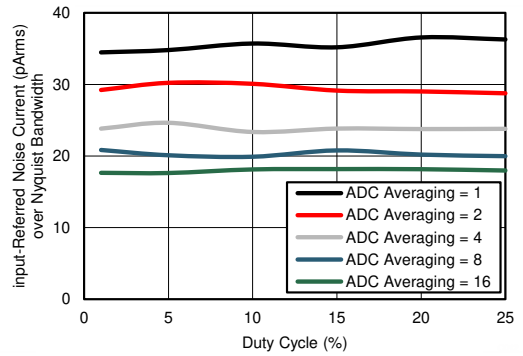


Figure 7-18. Receiver Input-Referred Noise Current over Nyquist Bandwidth vs Duty Cycle (Different ADC Averaging)

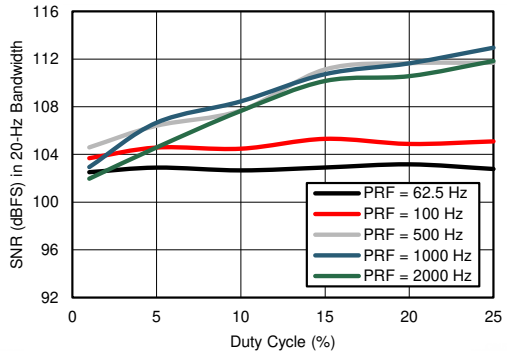


Figure 7-19. Receiver SNR in 20-Hz BW vs Duty Cycle (Different PRFs)

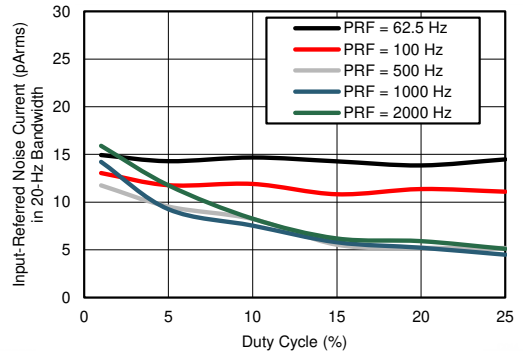
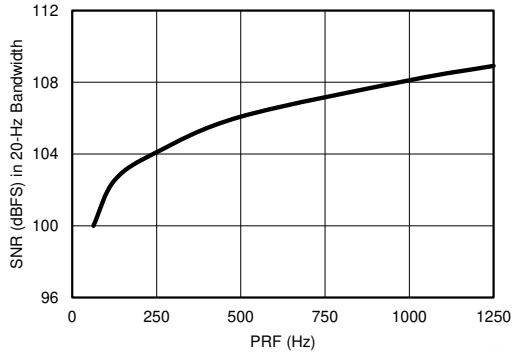


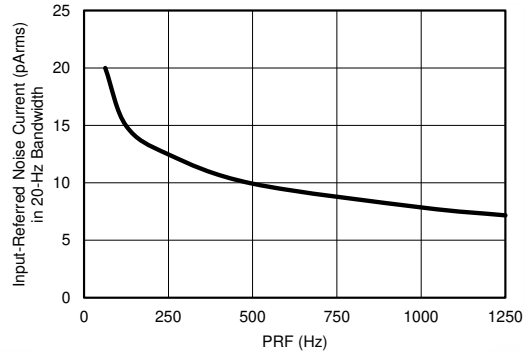
Figure 7-20. Receiver Input Referred Noise in 20-Hz BW vs Duty Cycle (Different PRFs)



Active window = 500 µs LED pulse = 100 µs

All four DYNAMIC bits set to 1

Figure 7-21. Receiver SNR in 20-Hz BW in Dynamic Power-Down Mode vs PRF



Active window = 500 µs LED pulse = 100 µs

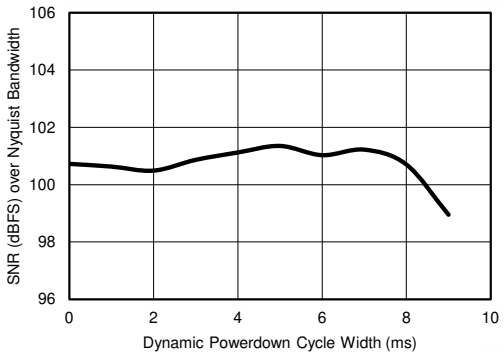
All four DYNAMIC bits set to 1

Figure 7-22. Receiver Input-Referred Noise in 20-Hz BW in Dynamic Power-Down Mode vs PRF

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7.8 Typical Characteristics (continued)

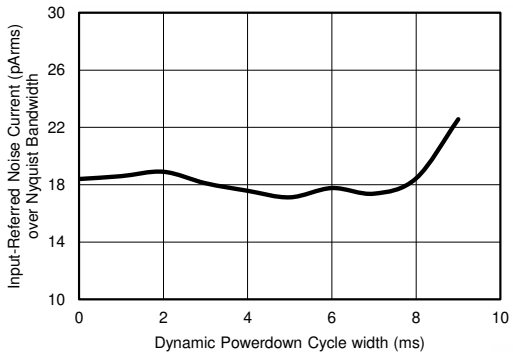
At PRF = 100 Hz, 25% duty cycle, R_F = 500 kΩ, C_F is adjusted to keep TIA time constant at 1/10th of sampling duration, All supplies at 3.3 V, 8-MHz external clock, CLKOUT tri-state, 1-µF capacitor on TX_REF and BG pins, detector C_{IN} = 50 pF, TX_REF = 0.5 V, ADC averaging = max allowed, and SNR in dBFS is noise referred to full-scale range of 2 V, unless otherwise noted.



PRF = 100 Hz LED pulse = 100 µs

All four DYNAMIC bits set to 1

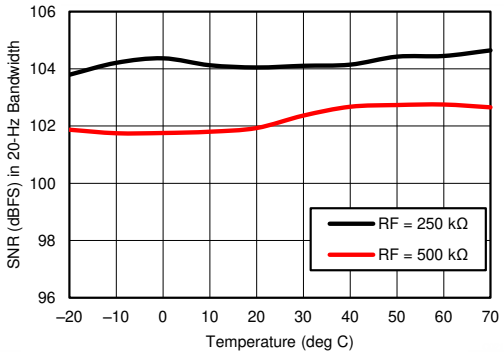
Figure 7-23. Receiver SNR over Nyquist Bandwidth vs Dynamic Power-Down Duty Cycle



PRF = 100 Hz LED pulse = 100 µs

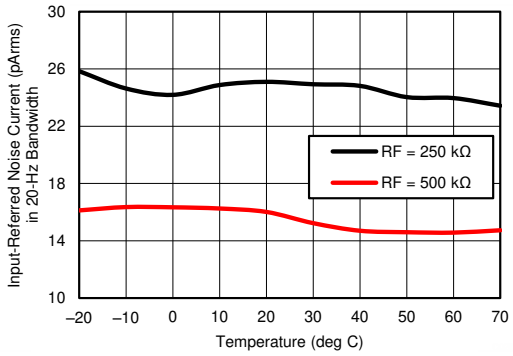
All four DYNAMIC bits set to 1

Figure 7-24. Receiver Input-Referred Noise over Nyquist Bandwidth vs Dynamic Power-Down Duty Cycle



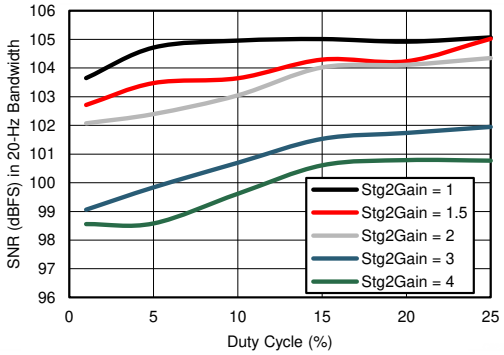
LED pulse = 100 µs Pleth current = 1 µA

Figure 7-25. SNR in 20-Hz Bandwidth vs Temperature (Tx-Rx Loopback)



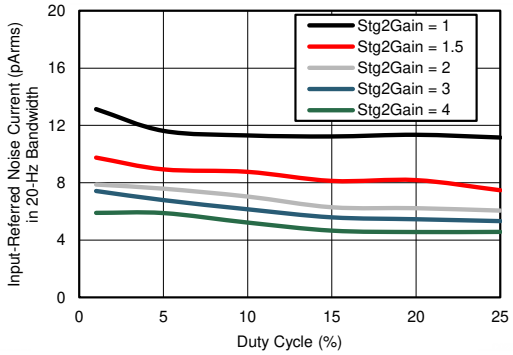
LED pulse = 100 µs Pleth current = 1 µA

Figure 7-26. Input-Referred Noise Current in 20-Hz BW vs Temperature (TX-Rx Loopback)



Stage 2 enabled

Figure 7-27. Receiver SNR over Nyquist Bandwidth vs Duty Cycle (Different Stage 2 Gain Settings)



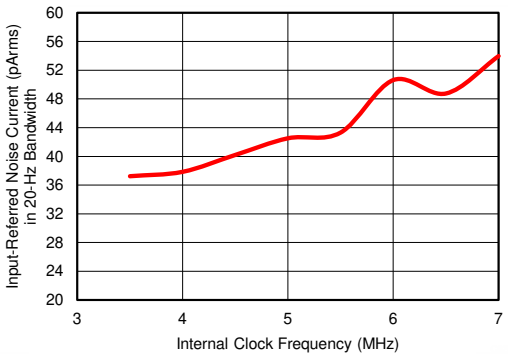
Stage 2 enabled

Figure 7-28. Receiver Input-Referred Noise Current over Nyquist Bandwidth vs Duty Cycle (Different Stage 2 Gain Settings)

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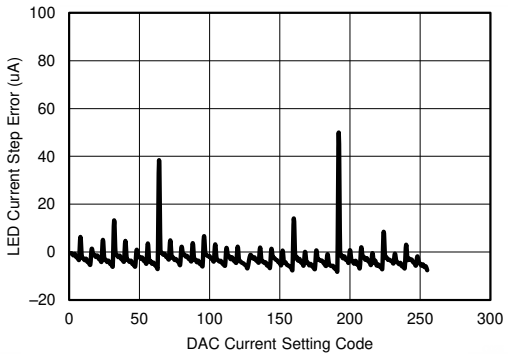
7.8 Typical Characteristics (continued)

At PRF = 100 Hz, 25% duty cycle, R_F = 500 kΩ, C_F is adjusted to keep TIA time constant at 1/10th of sampling duration, All supplies at 3.3 V, 8-MHz external clock, CLKOUT tri-state, 1-µF capacitor on TX_REF and BG pins, detector C_{IN} = 50 pF, TX_REF = 0.5 V, ADC averaging = max allowed, and SNR in dBFS is noise referred to full-scale range of 2 V, unless otherwise noted.



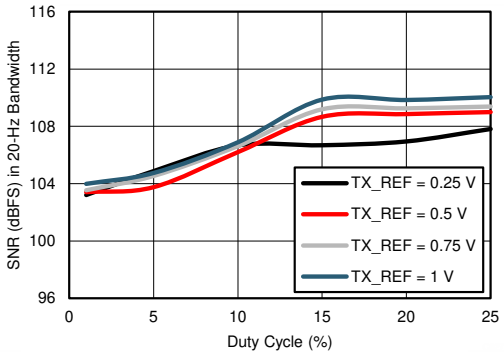
R_F = 250 kΩ PRF = 100 Hz ADC averaging = 1

Figure 7-29. Receiver Input-Referred Noise Current vs Internal Clock Frequency



TX_REF = 0.25 V

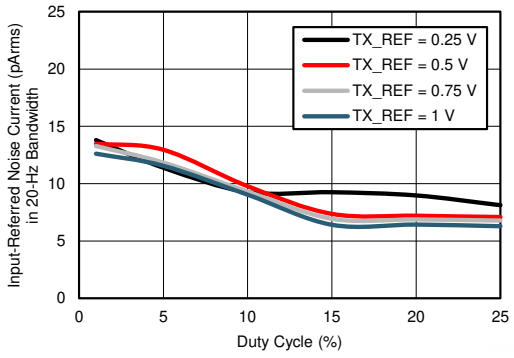
Figure 7-30. Transmitter DAC Current Step Error



PRF = 500 Hz

DAC current is set such that ADC output is 50 %FS

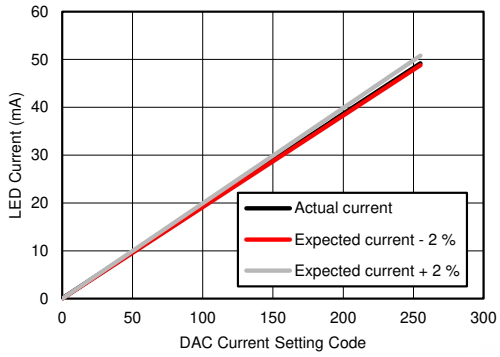
Figure 7-31. SNR in 20-Hz BW vs Duty Cycle (TX_REF Voltage with Tx-Rx Loopback)



PRF = 500 Hz

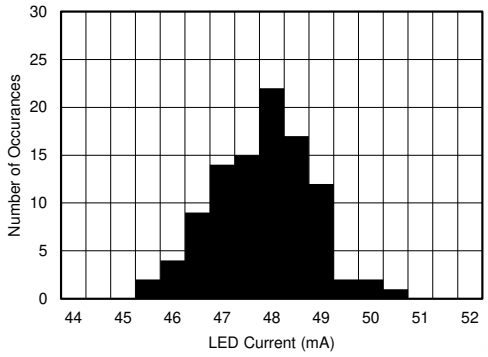
DAC current is set such that ADC output is 50 %FS

Figure 7-32. Input Referred Noise Current in 20-Hz BW vs Duty Cycle (TX_REF Voltage with Tx-Rx Loopback)



TX_REF = 0.25 V

Figure 7-33. Transmitter Current linearity



LED current = 48 mA 100 devices on tester

Figure 7-34. Transmitter Current Across Devices

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7.8 Typical Characteristics (continued)

At PRF = 100 Hz, 25% duty cycle, R_F = 500 kΩ, C_F is adjusted to keep TIA time constant at 1/10th of sampling duration, All supplies at 3.3 V, 8-MHz external clock, CLKOUT tri-state, 1-µF capacitor on TX_REF and BG pins, detector C_{IN} = 50 pF, TX_REF = 0.5 V, ADC averaging = max allowed, and SNR in dBFS is noise referred to full-scale range of 2 V, unless otherwise noted.

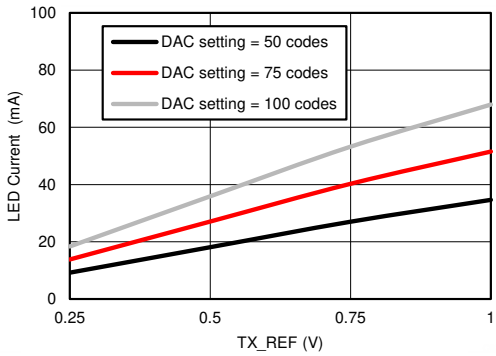


Figure 7-35. Transmitter Current vs TX_REF Voltage (Multiple DAC Settings)

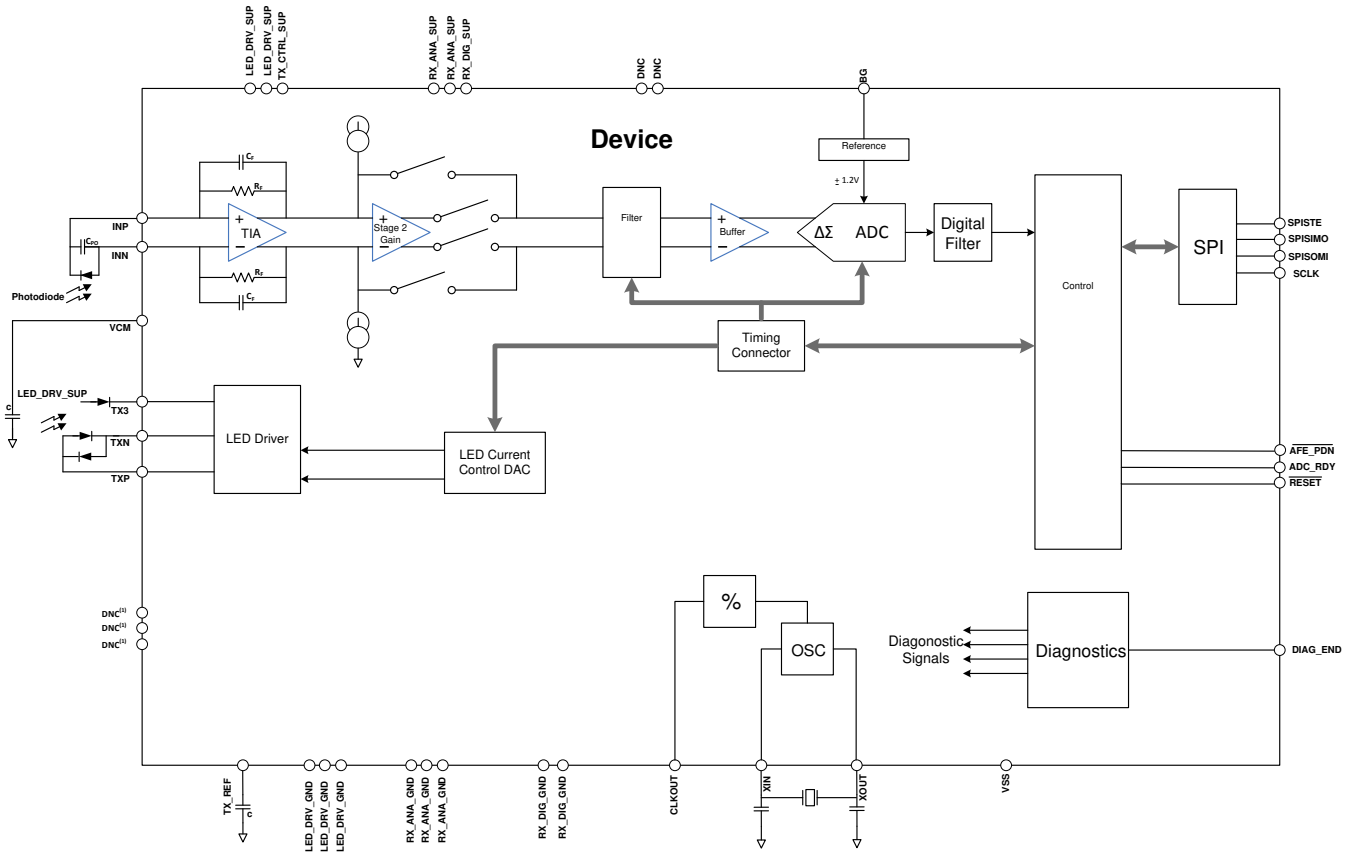
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8 Detailed Description

8.1 Overview

The AFE4403 is a complete analog front-end (AFE) solution targeted for pulse oximeter applications. The device consists of a low-noise receiver channel, an LED transmit section, and diagnostics for sensor and LED fault detection. To ease clocking requirements and provide the low-jitter clock to the AFE, an oscillator is also integrated that functions from an external crystal. The device communicates to an external microcontroller or host processor using an SPI interface. The *Functional Block Diagram* section provides a detailed block diagram for the AFE4403. The blocks are described in more detail in the following sections.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Receiver Channel

This section describes the functionality of the receiver channel.

8.3.1.1 Receiver Front-End

The receiver consists of a differential current-to-voltage (I-V) transimpedance amplifier (TIA) that converts the input photodiode current into an appropriate voltage, as shown in Figure 8-1. The feedback resistor of the amplifier (R_F) is programmable to support a wide range of photodiode currents. Available R_F values include: 1 MΩ, 500 kΩ, 250 kΩ, 100 kΩ, 50 kΩ, 25 kΩ, and 10 kΩ.

The device is ideally suited as a front-end for a PPG (photoplethysmography) application. In such an application, the light from the LED is reflected (or transmitted) from (or through) the various components inside the body (such as blood, tissue, and so forth) and are received by the photodiode. The signal received by the photodiode has three distinct components:

1. A pulsatile or ac component that arises as a result of the changes in blood volume through the arteries.
2. A constant dc signal that is reflected or transmitted from the time invariant components in the path of light. This constant dc component is referred to as the pleth signal.
3. Ambient light entering the photodiode.

The ac component is usually a small fraction of the pleth component, with the ratio referred to as the perfusion index (PI). Thus, the allowed signal chain gain is usually determined by the amplitude of the dc component.

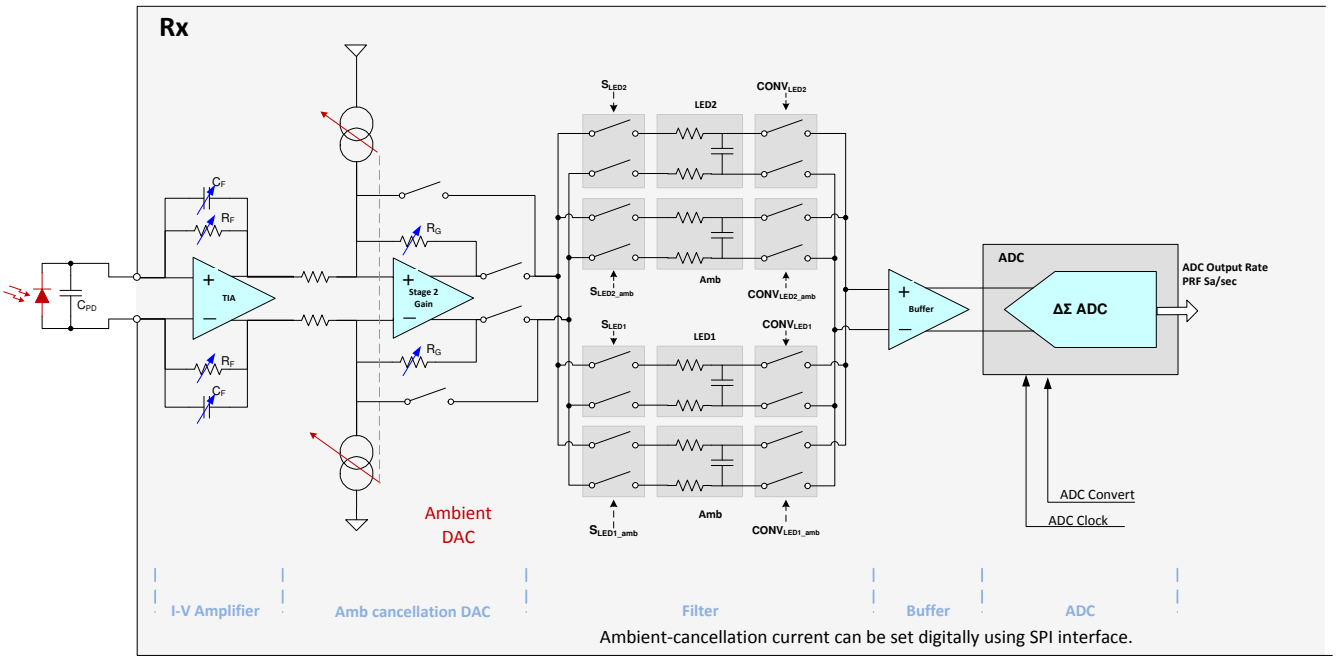


Figure 8-1. Receiver Front-End

The R_F amplifier and the feedback capacitor (C_F) form a low-pass filter for the input signal current. Always ensure that the low-pass filter RC time constant has sufficiently high bandwidth (as shown by Equation 1) because the input current consists of pulses. For this reason, the feedback capacitor is also programmable. Available C_F values include: 5 pF, 10 pF, 25 pF, 50 pF, 100 pF, and 250 pF. Any combination of these capacitors can also be used.

$$R_F \times C_F \leq \frac{\text{Rx Sample Time}}{10} \quad (1)$$

The output voltage of the I-V amplifier includes the pleth component (the desired signal) and a component resulting from the ambient light leakage. The I-V amplifier is followed by the second stage, which consists of a current digital-to-analog converter (DAC) that sources the cancellation current and an amplifier that gains up the pleth component alone. The amplifier has five programmable gain settings: 0 dB, 3.5 dB, 6 dB, 9.5 dB, and 12 dB. The gained-up pleth signal is then low-pass filtered (500-Hz bandwidth) and buffered before driving a 22-bit ADC. The current DAC has a cancellation current range of 10 µA with 10 steps (1 µA each). The DAC value can be digitally specified with the SPI interface. Using ambient compensation with the ambient DAC allows the dc-biased signal to be centered to near mid-point of the amplifier (±0.9 V). Using the gain of the second stage allows for more of the available ADC dynamic range to be used.

The output of the ambient cancellation amplifier is separated into LED2 and LED1 channels. When LED2 is on, the amplifier output is filtered and sampled on capacitor C_{LED2}. Similarly, the LED1 signal is sampled on the C_{LED1} capacitor when LED1 is on. In between the LED2 and LED1 pulses, the idle amplifier output is sampled to estimate the ambient signal on capacitors C_{LED2_amb} and C_{LED1_amb}.

The sampling duration is termed the *Rx sample time* and is programmable for each signal, independently. The sampling can start after the I-V amplifier output is stable (to account for LED and cable settling times). The Rx sample time is used for all dynamic range calculations; the minimum time recommended is 50 µs. While the AFE4403 can support pulse widths lower than 50 us, having too low a pulse width could result in a degraded signal and noise from the photodiode.

A single, 22-bit ADC converts the sampled LED2, LED1, and ambient signals sequentially. Each conversion provides a single digital code at the ADC output. As discussed in the *Receiver Timing* section, the conversions are meant to be staggered so that the LED2 conversion starts after the end of the LED2 sample phase, and so on.

Note that four data streams are available at the ADC output (LED2, LED1, ambient LED2, and ambient LED1) at the same rate as the pulse repetition frequency. The ADC is followed by a digital ambient subtraction block that additionally outputs the (LED2 – ambient LED2) and (LED1 – ambient LED1) data values.

The model of the photodiode and the connection to the TIA is shown in Figure 8-2.

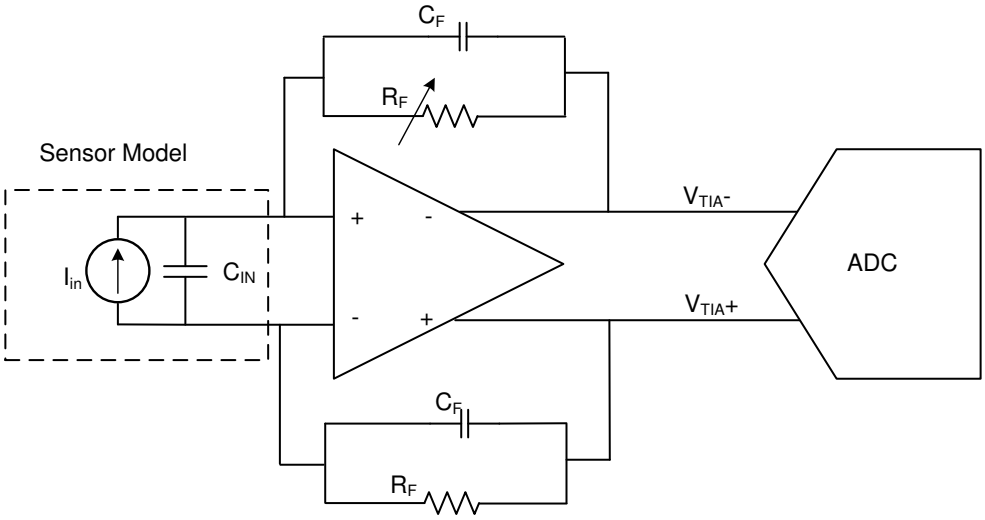


Figure 8-2. TIA Block Diagram

I_{in} is the signal current generated by the photodiode in response to the incident light. C_{in} is the zero-bias capacitance of the photodiode. The current-to-voltage gain in the TIA is given by Equation 2:

$$V_{TIA}\,(\text{diff}) = V_{TIA}{}^{+} - V_{TIA}{}^{-} = 2 \times I_{in} \times R_F \quad (2)$$

For example, for a photodiode current of I_{in} = 1 µA and a TIA gain setting of R_F = 100 kΩ, the differential output of the TIA is equal to 200 mV. The TIA has an operating range of ±1 V, and the ADC has an input full-scale range of ±1.2 V (the extra margin is to prevent the ADC from saturating while operating the TIA at the fullest

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output range). Furthermore, because the PPG signal is one-sided, only one half of the full-scale is used. TI recommends operating the device at a dc level that is not more than 50% to 60% of the ADC full-scale. The margin allows for sudden changes in the signal level that might saturate the signal chain if operating too close to full-scale. Signal levels are shown in Figure 8-3:

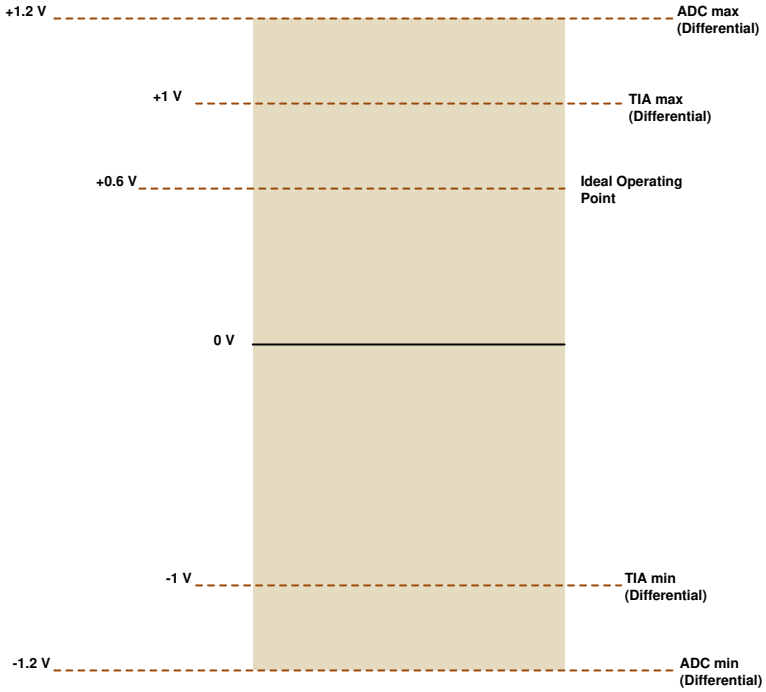


Figure 8-3. Signal Levels in TIA and ADC

On startup, a gain calibration algorithm running on the microcontroller unit (MCU) can be used to monitor the dc level and adjusts the LED current and TIA gain to get close to the target dc level. In addition to a target dc level, a high and low threshold (for example 80% and 20% of full-scale) can be determined that can cause the algorithm to switch to a different TIA gain or LED current setting when the signal amplitude changes beyond these thresholds.

In heart rate monitoring (HRM) applications demanding small-form factors, the sensor size can be so small (and the signal currents so low) that they do not occupy even 50% of full-scale even with the highest TIA gain setting of 1 MΩ, which is the case for signal currents that are less than 300 nA. As such, experimentation with various use cases is essential in order to determine the optimal target value, as well as high and low thresholds. Also, by enabling the stage 2 and introducing additional gain (up to 12 dB), a few extra decibels of SNR can be achieved.

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8.3.1.2 Ambient Cancellation Scheme and Second Stage Gain Block

The receiver provides digital samples corresponding to ambient duration. The host processor (external to the AFE) can use these ambient values to estimate the amount of ambient light leakage. The processor must then set the value of the ambient cancellation DAC using the SPI, as shown in Figure 8-4.

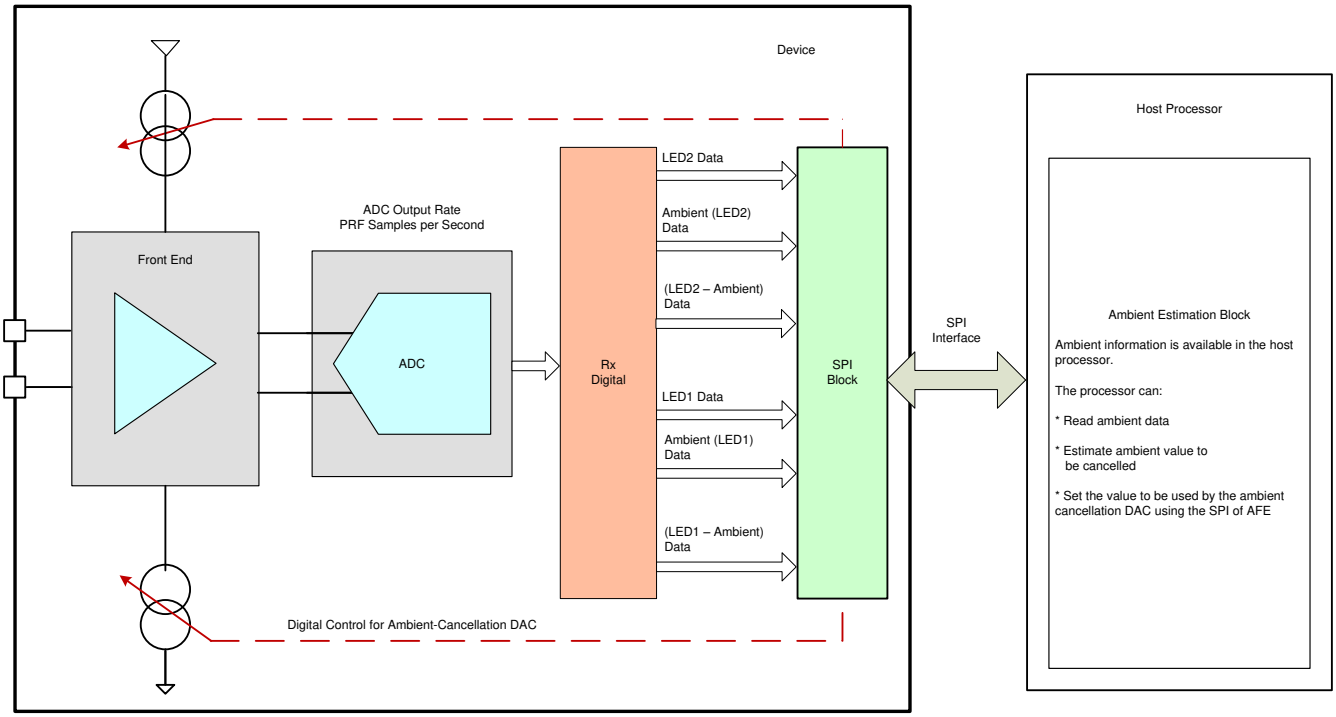


Figure 8-4. Ambient Cancellation Loop (Closed by the Host Processor)

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Using the set value, the ambient cancellation stage subtracts the ambient component and gains up only the pleth component of the received signal; see Figure 8-5. The amplifier gain is programmable to 0 dB, 3.5 dB, 6 dB, 9.5 dB, and 12 dB.

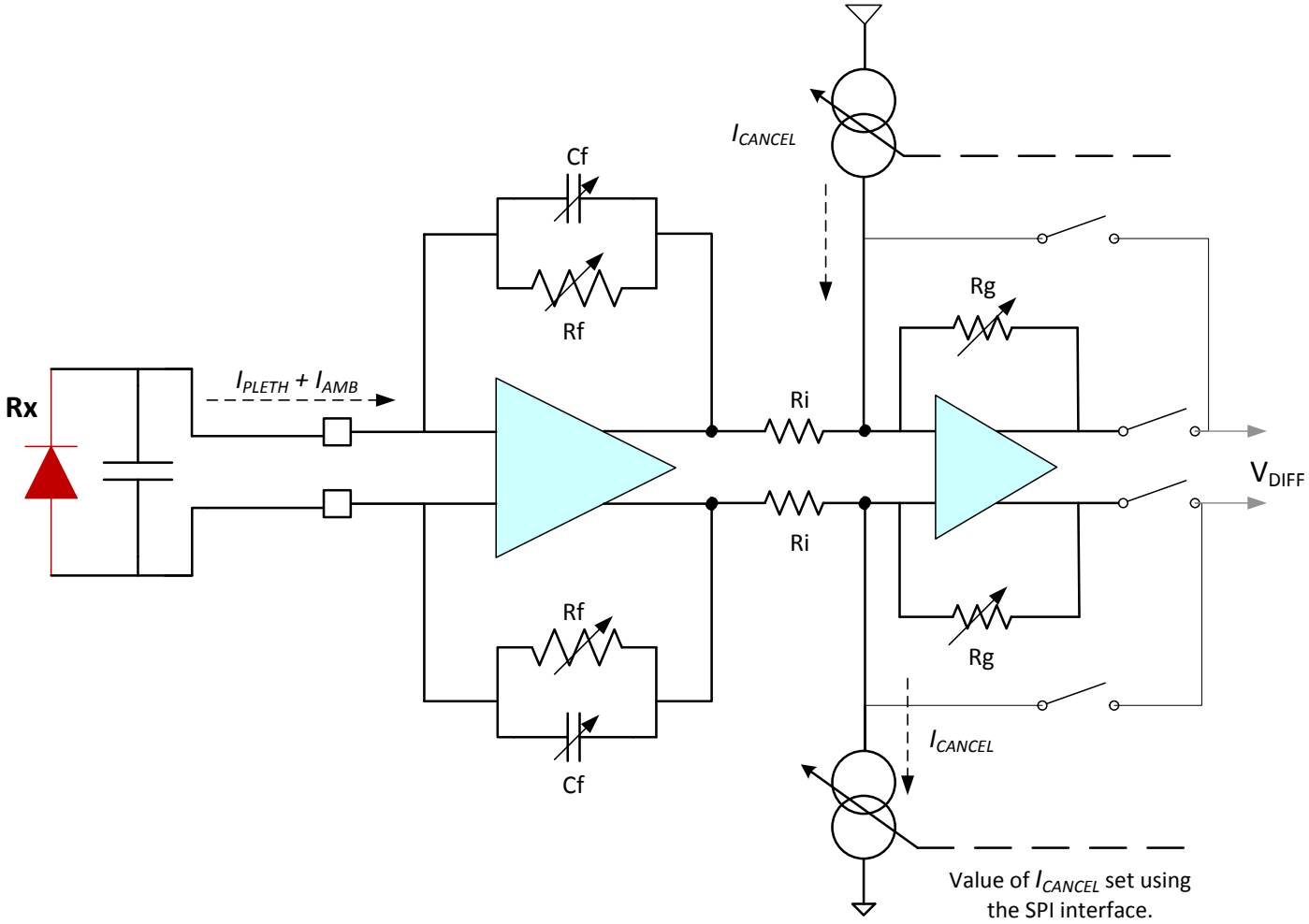


Figure 8-5. Front-End (I-V Amplifier and Cancellation Stage)

The differential output of the second stage is V_{DIFF}, as given by Equation 3:

$$V_{DIFF} = 2 \times \left(I_{PLETH} \times \frac{R_F}{R_I} + I_{AMB} \times \frac{R_F}{R_I} - I_{CANCEL} \right) \times R_G \quad (3)$$

where:

- R_I = 100 kΩ,
- I_{PLETH} = photodiode current pleth component,
- I_{AMB} = photodiode current ambient component, and
- I_{CANCEL} = the cancellation current DAC value (as estimated by the host processor).

R_G values with various gain settings are listed in Table 8-1.

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Table 8-1. R_G Values

GAIN	R_G(kΩ)
0 (x1)	100
3.5 (x1.5)	150
6 (x2)	200
9.5 (x3)	300
12 (x4)	400

8.3.1.3 Receiver Control Signals

LED2 sample phase (S_{LED2} or S_R): When this signal is high, the amplifier output corresponds to the LED2 on-time. The amplifier output is filtered and sampled into capacitor C_{LED2}. To avoid settling effects resulting from the LED or cable, program S_{LED2} to start after the LED turns on. This settling delay is programmable.

Ambient sample phase (S_{LED2_amb} or S_{R_amb}): When this signal is high, the amplifier output corresponds to the LED2 off-time and can be used to estimate the ambient signal (for the LED2 phase). The amplifier output is filtered and sampled into capacitor C_{LED2_amb}.

LED1 sample phase (S_{LED1} or S_{IR}): When this signal is high, the amplifier output corresponds to the LED1 on-time. The amplifier output is filtered and sampled into capacitor C_{LED1}. To avoid settling effects resulting from the LED or cable, program S_{LED1} to start after the LED turns on. This settling delay is programmable.

Ambient sample phase (S_{LED1_amb} or S_{IR_amb}): When this signal is high, the amplifier output corresponds to the LED1 off-time and can be used to estimate the ambient signal (for the LED1 phase). The amplifier output is filtered and sampled into capacitor C_{LED1_amb}.

LED2 convert phase ($CONV_{LED2}$ or $CONV_R$): When this signal is high, the voltage sampled on C_{LED2} is buffered and applied to the ADC for conversion. At the end of the conversion, the ADC provides a single digital code corresponding to the LED2 sample.

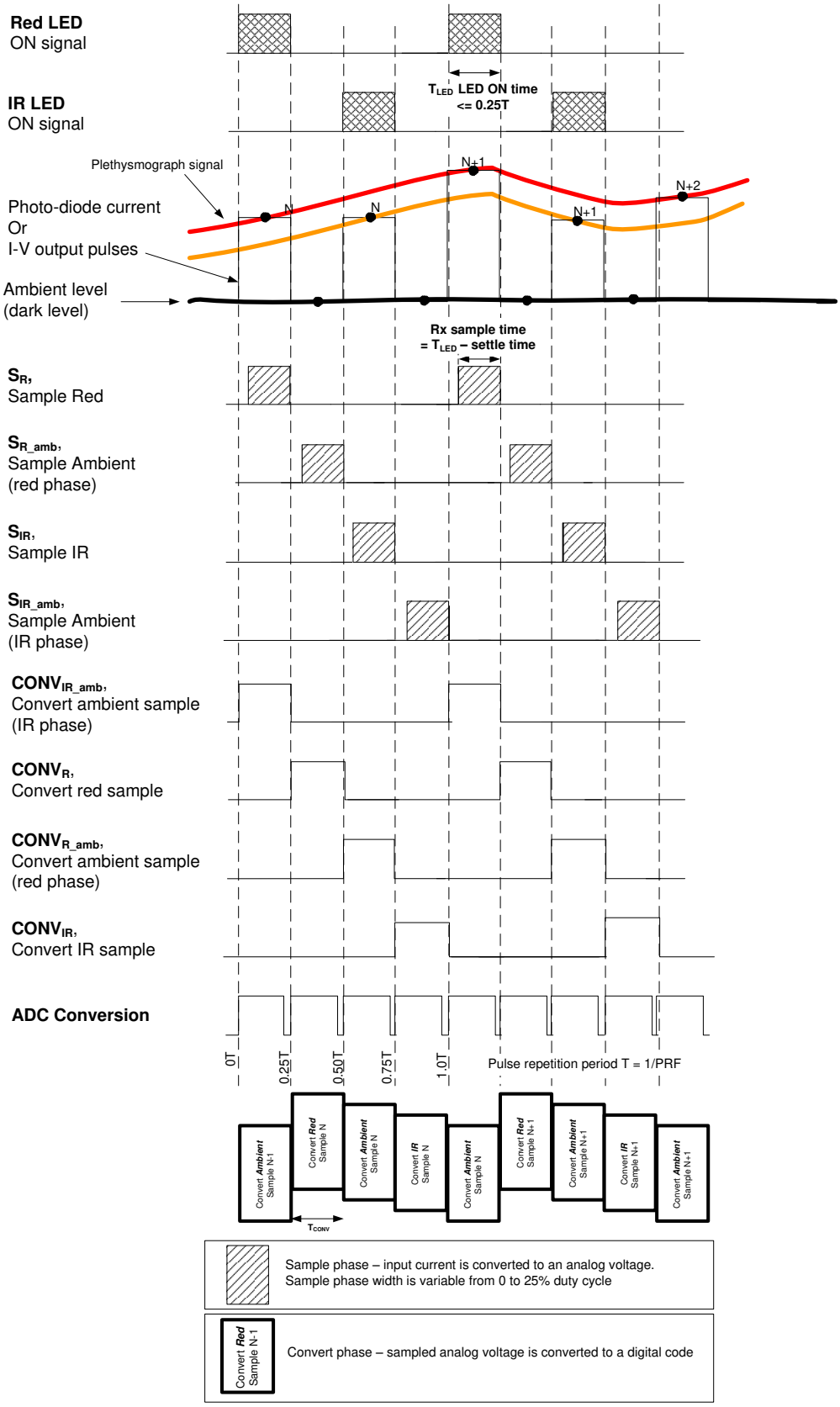
Ambient convert phases ($CONV_{LED2_amb}$ or $CONV_{R_amb}$, $CONV_{LED1_amb}$or $CONV_{IR_amb}$): When this signal is high, the voltage sampled on C_{LED2_amb} (or C_{LED1_amb}) is buffered and applied to the ADC for conversion. At the end of the conversion, the ADC provides a single digital code corresponding to the ambient sample.

LED1 convert phase ($CONV_{LED1}$ or $CONV_{IR}$): When this signal is high, the voltage sampled on C_{LED1} is buffered and applied to the ADC for conversion. At the end of the conversion, the ADC provides a single digital code corresponding to the LED1 sample.

8.3.1.4 Receiver Timing

See Figure 8-6 for a timing diagram detailing the control signals related to the LED on-time, Rx sample time, and the ADC conversion times for each channel. Figure 8-6 shows the timing for a case where each phase occupies 25% of the pulse repetition period. However, this percentage is not a requirement. In cases where the device is operated with low pulse repetition frequency (PRF) or low LED pulse durations, the active portion of the pulse repetition period can be reduced. Using the dynamic power-down feature, the overall power consumption can be significantly reduced.

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NOTE: Relationship to the AFE4403 EVM is: LED1 = IR and LED2 = RED.

Figure 8-6. Rx Timing Diagram

8.3.2 Clocking and Timing Signal Generation

The crystal oscillator generates a master clock signal using an external crystal. In the default mode, a divide-by-2 block converts the 8-MHz clock to 4 MHz, which is used by the AFE to operate the timer modules, ADC, and diagnostics. The 4-MHz clock is buffered and output from the AFE in order to clock an external microcontroller. The clocking functionality is shown in Figure 8-7.

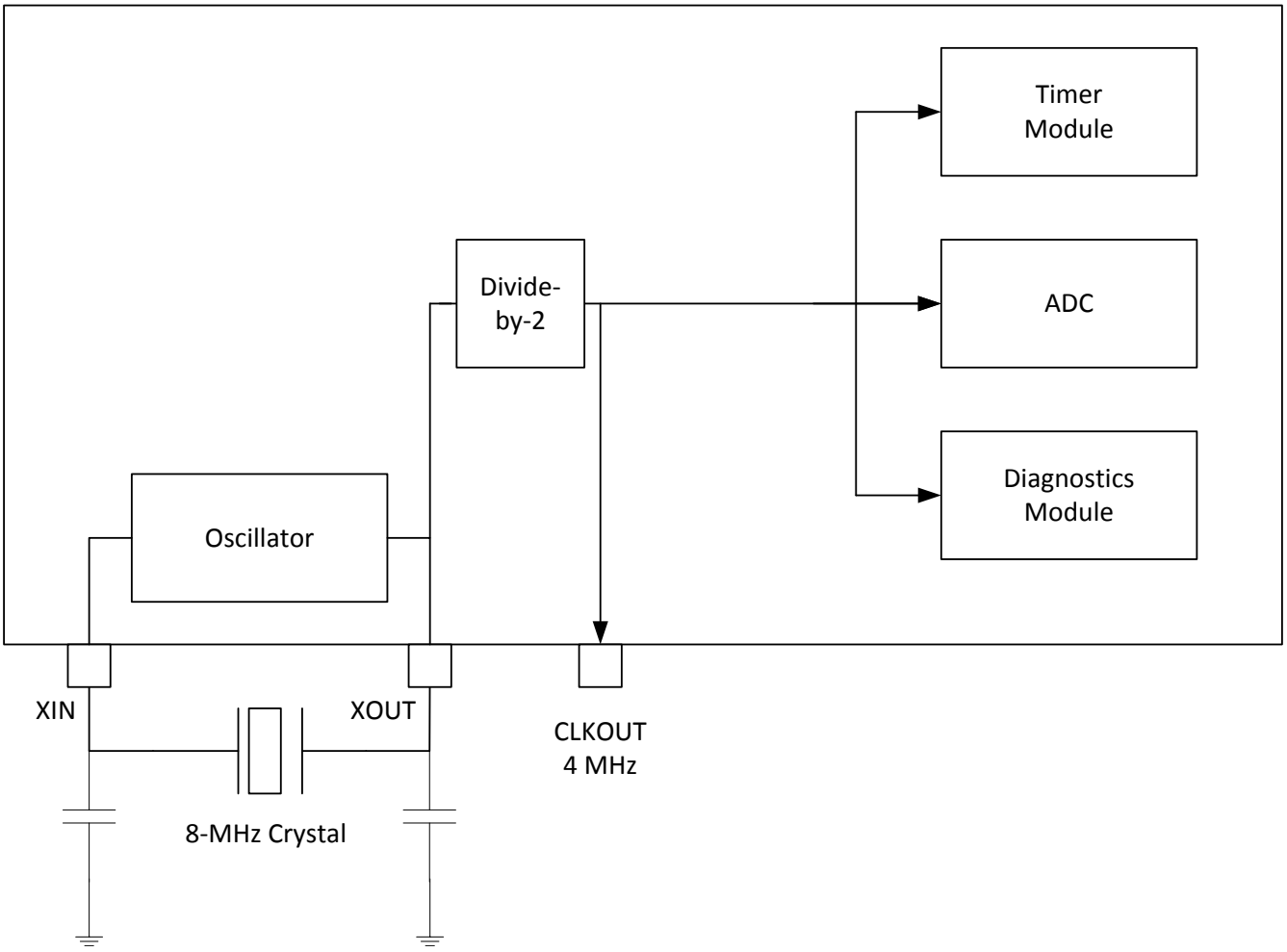


Figure 8-7. AFE Clocking

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To enable flexible clocking, the AFE4403 has a clock divider with programmable division ratios. While the default division ratio is divide-by-2, the clock divider can be programmed to select between ratios of 1, 2, 4, 6, 8, or 12. The division ratio should be selected based on the external clock input frequency such that the divided clock has a frequency close to 4 MHz. For this reason, CLKOUT is referred as a 4-MHz clock in this document. When operating with an external clock input, the divider is reset based on the $\overline{\text{RESET}}$ rising edge. Figure 8-8 shows the case where the divider ratio is set to divide-by-2.

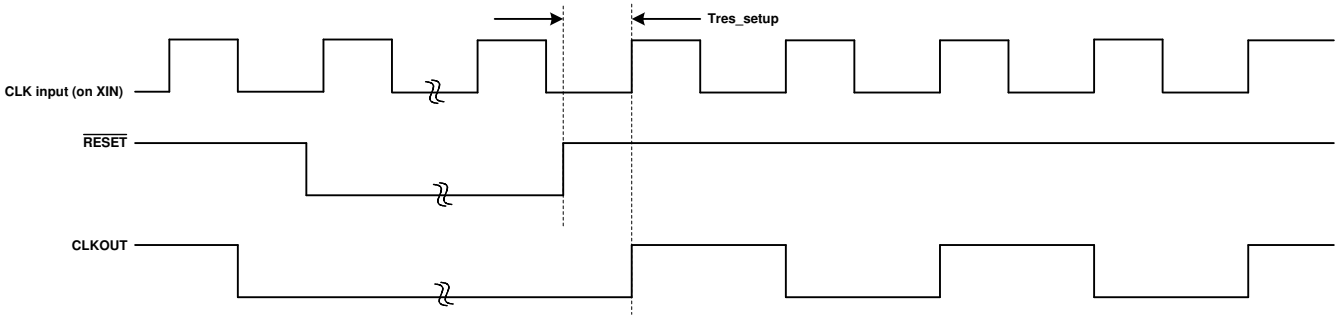


Figure 8-8. Clock Divider Reset

The device supports both external clock mode as well as an internal clock mode with external crystal.

In the external clock mode, an external clock is input on the XIN pin and the device internally generates the internal clock (used by the timing engine and the ADC) by a programmable division ratio. After division, the internal clock should be within a range of 4 MHz to 6 MHz. The exact frequency of this divided clock is one of the pieces of information required to establish the heart rate being measured from the pulse data.

In internal clock mode, an external crystal (connected between XIN and XOUT) is used to generate the clock. To generate sustained oscillations, the oscillator within the AFE provides negative resistance to cancel out the ESR of the crystal. A good rule of thumb is to limit the ESR of the crystal to less than a third of the negative resistance achievable by the oscillator. Figure 8-9 shows the connection of Crystal to AFE4403.

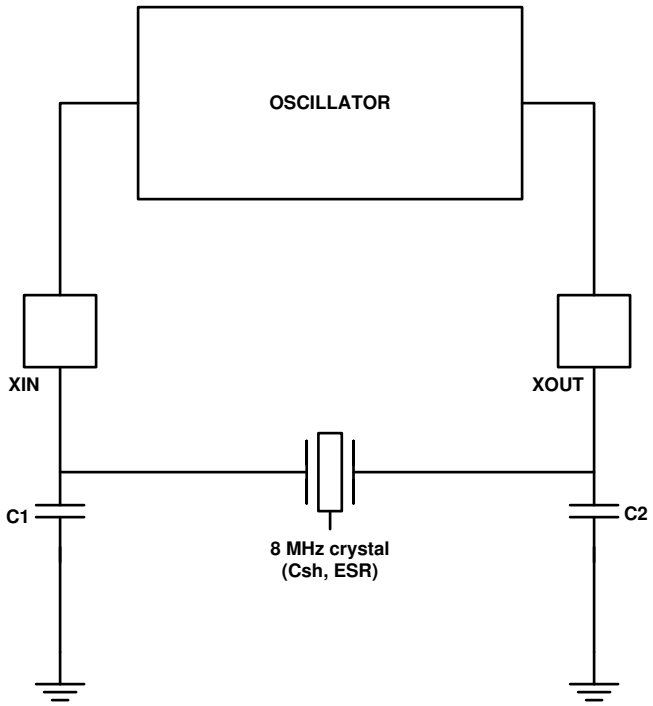


Figure 8-9. Connection of Crystal to AFE4403

In Figure 8-9 the crystal is characterized by a capacitance, C_{sh} (shunt capacitance of the crystal) and an equivalent series resistance (ESR). C1 and C2 are external capacitors added at the XIN and XOUT pins.

The negative resistance achievable from the internal oscillator is given by Equation 4:

$$R = –1 / (2 \times \omega \times C_{sh} \times [1 + C_{sh} / C_L]) \quad (4)$$

where

- C_L = (C1 × C2) / (C1 + C2),
- ω is the frequency of oscillation in rads,
- C_{sh} is the shunt capacitor of the crystal, and
- C1, C2 are the capacitors to ground from the XIN, XOUT pins. A value of approximately 15 pF is recommended for C1, C2.

For example, with C_{sh} = 8 pF, C1 = C2 = 15 pF, and a frequency of 8 MHz, the result is Equation 5:

$$R = –600\ \Omega \quad (5)$$

Thus, the crystal ESR is limited to less than approximately 200 Ω.

TI highly recommends that a single clock source be used to generate the clock required by the AFE as well as the clock needed by the microcontroller (MCU). If an independent clock source is used by the MCU, then any energy coupling into the AFE supply or ground or input pins can cause aliased spurious tones close to the heart rate being measured. To enable operation with the single clock source between the AFE and the MCU, two options are possible:

1. **AFE clock as master:** The AFE uses a crystal to generate its clock. CLKOUT from the AFE is used as the input clock for the MCU.
2. **MCU clock as master:** The AFE operates with an external clock provided by the MCU.

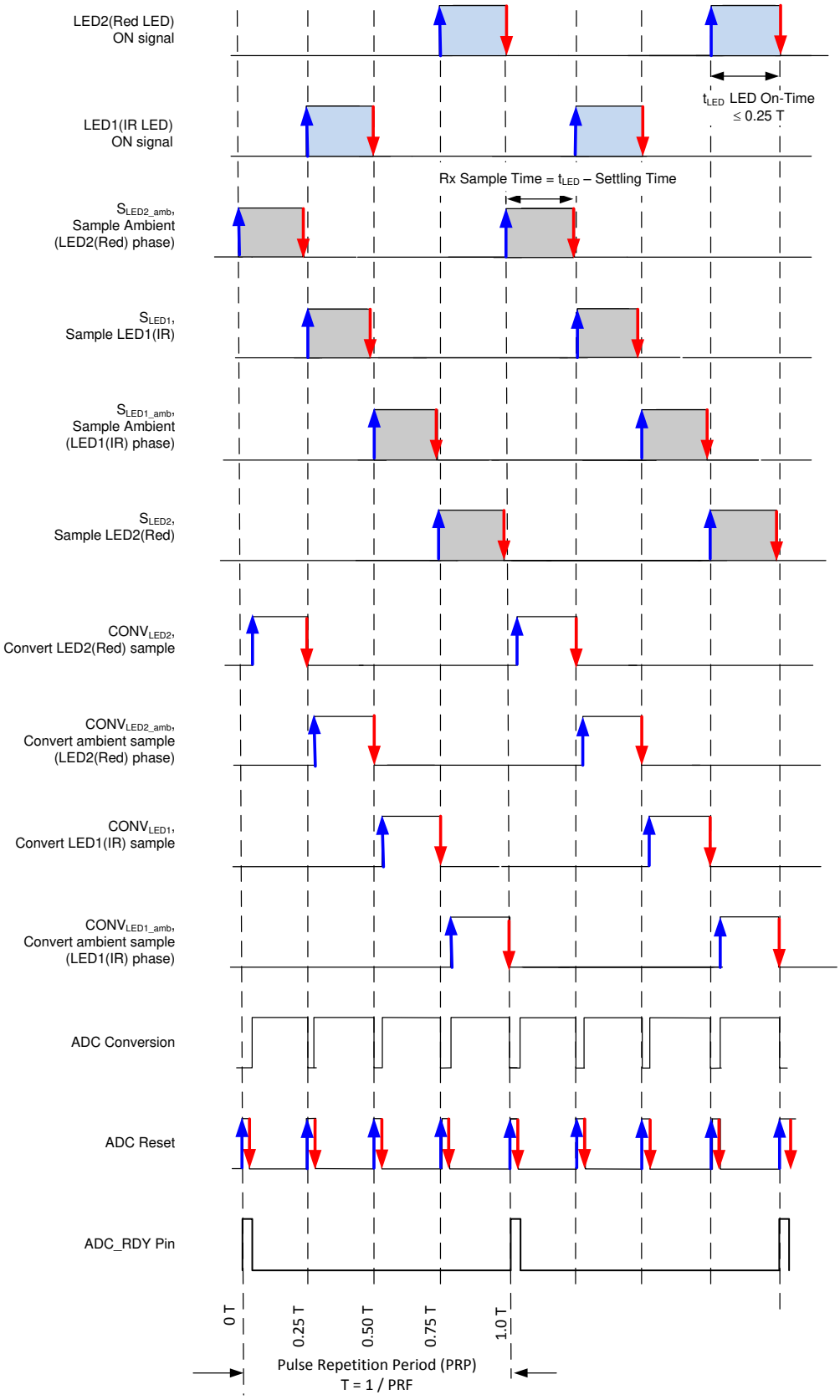
Note that the switching of CLKOUT consumes power. Thus, if CLKOUT is not used, it can be shut off using the CLKOUT_TRI bit.

8.3.3 Timer Module

See Figure 8-10 for a timing diagram detailing the various timing edges that are programmable using the timer module. The rising and falling edge positions of 11 signals can be controlled. The module uses a single 16-bit counter (running off of the 4-MHz clock) to set the time-base.

All timing signals are set with reference to the pulse repetition period (PRP). Therefore, a dedicated compare register compares the 16-bit counter value with the reference value specified in the PRF register. Every time that the 16-bit counter value is equal to the reference value in the PRF register, the counter is reset to 0.

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NOTE: Programmable edges are shown in blue and red.

Figure 8-10. AFE Control Signals

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For the timing signals in Figure 8-6, the start and stop edge positions are programmable with respect to the PRF period. Each signal uses a separate timer compare module that compares the counter value with preprogrammed reference values for the start and stop edges. All reference values can be set using the SPI interface.

After the counter value has exceeded the stop reference value, the output signal is set. When the counter value equals the stop reference value, the output signal is reset. Figure 8-11 shows a diagram of the timer compare register. With a 4-MHz clock, the edge placement resolution is 0.25 µs.

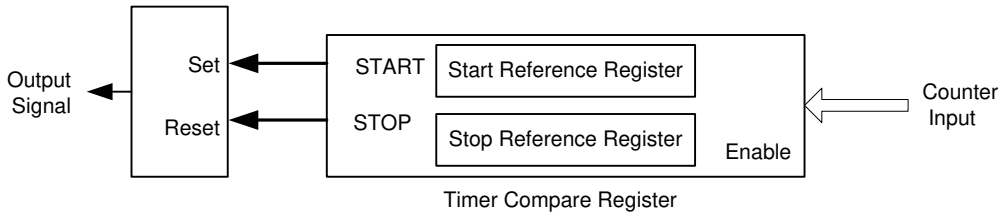


Figure 8-11. Compare Register

The ADC conversion signal requires four pulses in each PRF clock period. Timer compare register 11 uses four sets of start and stop registers to control the ADC conversion signal, as shown in Figure 8-12.

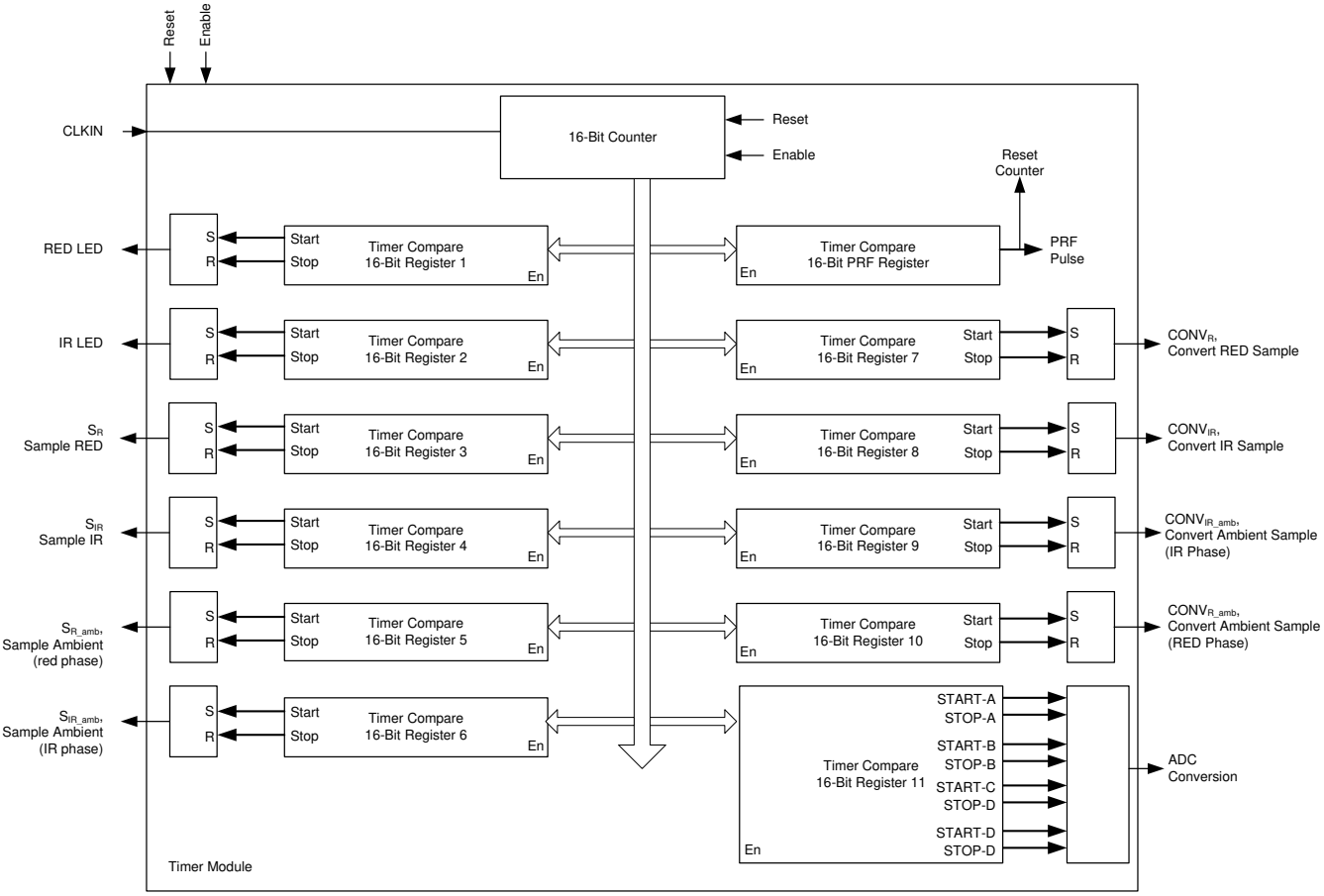


Figure 8-12. Timer Module

8.3.3.1 Using the Timer Module

The timer module registers can be used to program the start and end instants in units of 4-MHz clock cycles. These timing instants and the corresponding registers are listed in Table 8-2.

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Note that the device does not restrict the values in these registers; thus, the start and end edges can be positioned anywhere within the pulse repetition period. Care must be taken by the user to program suitable values in these registers to avoid overlapping the signals and to make sure none of the edges exceed the value programmed in the PRP register. Writing the same value in the start and end registers results in a pulse duration of one clock cycle. The following steps describe the timer sequencing configuration:

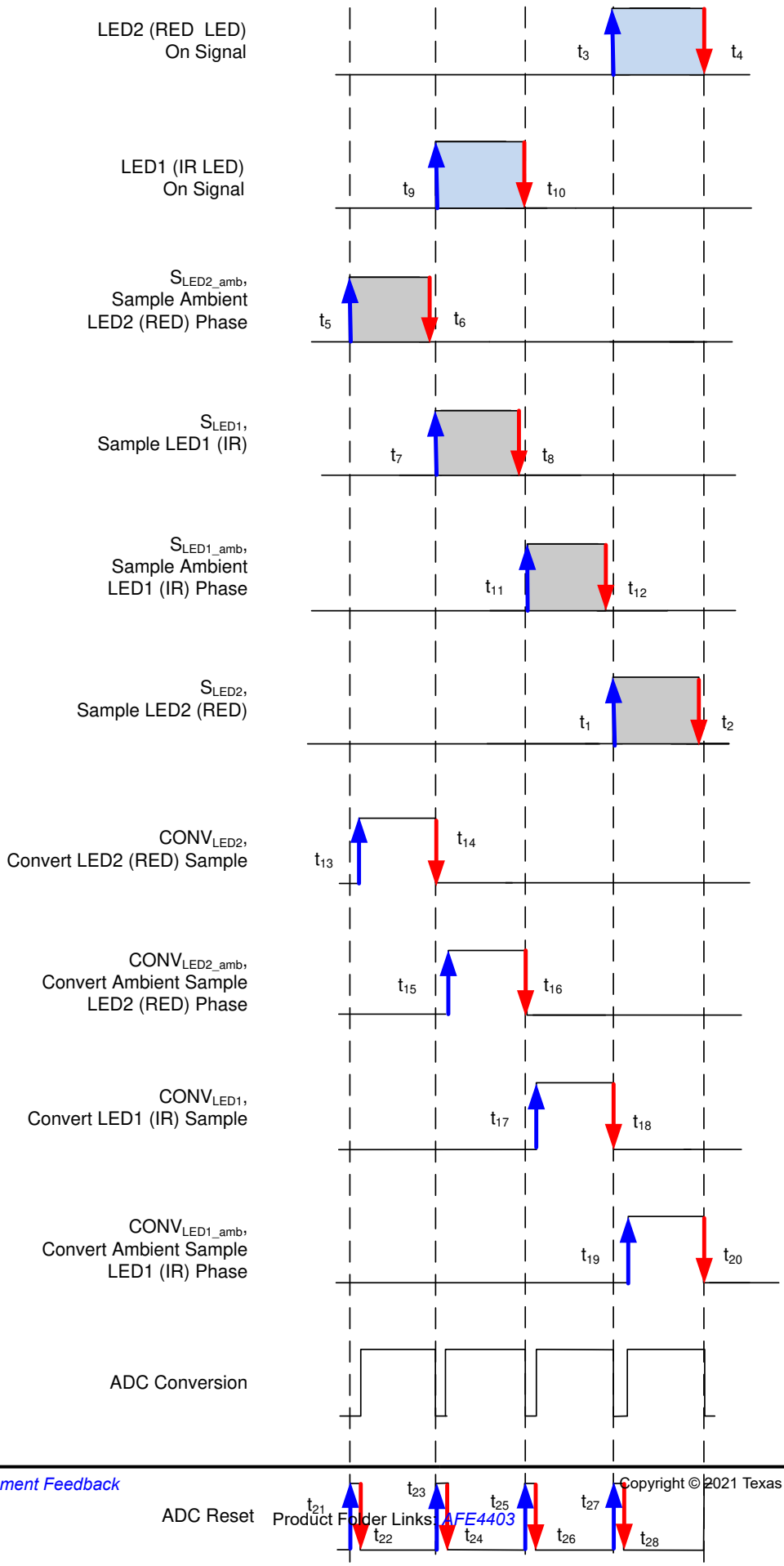
1. With respect to the start of the PRP period (indicated by timing instant t_0 in Figure 8-13), the following sequence of conversions must be followed in order: convert LED2 → LED2 ambient → LED1 → LED1 ambient.
2. Also, starting from t_0, the sequence of sampling instants must be staggered with respect to the respective conversions as follows: sample LED2 ambient → LED1 → LED1 ambient → LED2.
3. Finally, align the edges for the two LED pulses with the respective sampling instants.

Table 8-2. Clock Edge Mapping to SPI Registers

TIME INSTANT (See Figure 8-13 and Figure 8-14)(3)	DESCRIPTION	CORRESPONDING REGISTER ADDRESS AND REGISTER BITS	EXAMPLE(1) (Decimal)
t_0	Start of pulse repetition period	No register control	—
t_1	Start of sample LED2 pulse	LED2STC[15:0], register 01h	6050
t_2	End of sample LED2 pulse	LED2ENDC[15:0], register 02h	7998
t_3	Start of LED2 pulse	LED2LEDSTC[15:0], register 03h	6000
t_4	End of LED2 pulse	LED2LEDENDC[15:0], register 04h	7999
t_5	Start of sample LED2 ambient pulse	ALED2STC[15:0], register 05h	50
t_6	End of sample LED2 ambient pulse	ALED2ENDC[15:0], register 06h	1998
t_7	Start of sample LED1 pulse	LED1STC[15:0], register 07h	2050
t_8	End of sample LED1 pulse	LED1ENDC[15:0], register 08h	3998
t_9	Start of LED1 pulse	LED1LEDSTC[15:0], register 09h	2000
t_{10}	End of LED1 pulse	LED1LEDENDC[15:0], register 0Ah	3999
t_{11}	Start of sample LED1 ambient pulse	ALED1STC[15:0], register 0Bh	4050
t_{12}	End of sample LED1 ambient pulse	ALED1ENDC[15:0], register 0Ch	5998
t_{13}	Start of convert LED2 pulse	LED2CONVST[15:0], register 0Dh Must start one AFE clock cycle after the ADC reset pulse ends.	4
t_{14}	End of convert LED2 pulse	LED2CONVEND[15:0], register 0Eh	1999
t_{15}	Start of convert LED2 ambient pulse	ALED2CONVST[15:0], register 0Fh Must start one AFE clock cycle after the ADC reset pulse ends.	2004
t_{16}	End of convert LED2 ambient pulse	ALED2CONVEND[15:0], register 10h	3999
t_{17}	Start of convert LED1 pulse	LED1CONVST[15:0], register 11h Must start one AFE clock cycle after the ADC reset pulse ends.	4004
t_{18}	End of convert LED1 pulse	LED1CONVEND[15:0], register 12h	5999
t_{19}	Start of convert LED1 ambient pulse	ALED1CONVST[15:0], register 13h Must start one AFE clock cycle after the ADC reset pulse ends.	6004
t_{20}	End of convert LED1 ambient pulse	ALED1CONVEND[15:0], register 14h	7999
t_{21}	Start of first ADC conversion reset pulse	ADCRSTSTCT0[15:0], register 15h	0
t_{22}	End of first ADC conversion reset pulse(2)	ADCRSTENDCT0[15:0], register 16h	3
t_{23}	Start of second ADC conversion reset pulse	ADCRSTSTCT1[15:0], register 17h	2000
t_{24}	End of second ADC conversion reset pulse(2)	ADCRSTENDCT1[15:0], register 18h	2003
t_{25}	Start of third ADC conversion reset pulse	ADCRSTSTCT2[15:0], register 19h	4000
t_{26}	End of third ADC conversion reset pulse(2)	ADCRSTENDCT2[15:0], register 1Ah	4003
t_{27}	Start of fourth ADC conversion reset pulse	ADCRSTSTCT3[15:0], register 1Bh	6000
t_{28}	End of fourth ADC conversion reset pulse(2)	ADCRSTENDCT3[15:0], register 1Ch	6003
t_{29}	End of pulse repetition period	PRPCOUNT[15:0], register 1Dh	7999

(1) Values are based off of a pulse repetition frequency (PRF) = 500 Hz and duty cycle = 25%.
(2) See Figure 8-14, note 2 for the effect of the ADC reset time crosstalk.
(3) Any pulse can be set to zero width by making its start value higher than the end value.

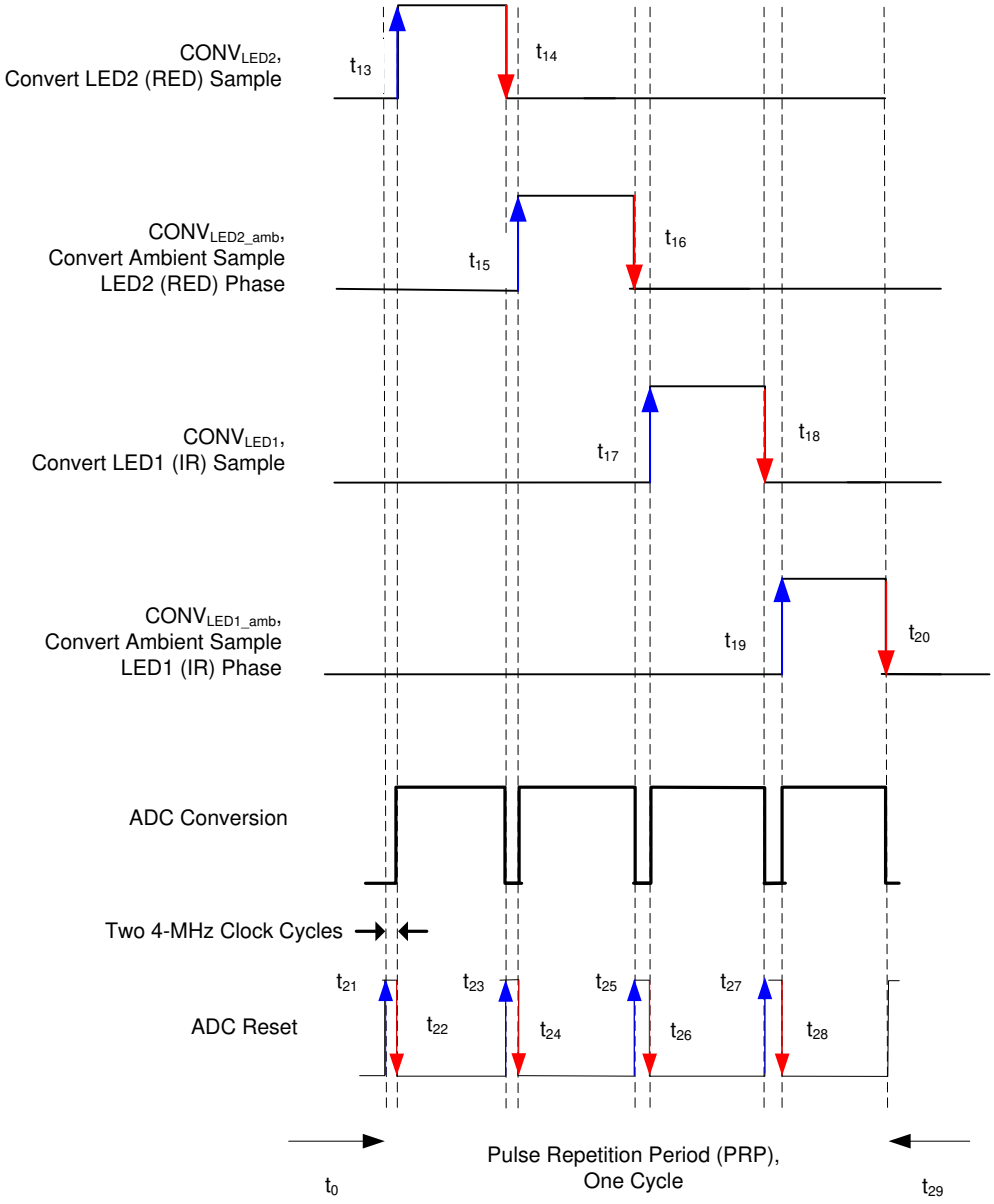
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B. A low ADC reset time can result in a small component of the LED signal leaking into the ambient phase. With an ADC reset of two clock cycles, a –60-dB leakage is expected. In many cases, this leakage does not affect system performance. However, if this crosstalk must be completely eliminated, a longer ADC reset time of approximately six clock cycles is recommended for t_{22}, t_{24}, t_{26}, and t_{28}.

Figure 8-13. Programmable Clock Edges(1)(2)



A. RED = LED2, IR = LED1.

B. A low ADC reset time can result in a small component of the LED signal leaking into the ambient phase. With an ADC reset of two clock cycles, a –60-dB leakage is expected. In many cases, this leakage does not affect system performance. However, if this crosstalk must be completely eliminated, a longer ADC reset time of approximately six clock cycles is recommended for t_{22}, t_{24}, t_{26}, and t_{28}.

Figure 8-14. Relationship Between the ADC Reset and ADC Conversion Signals(1)(2)

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8.3.4 Receiver Subsystem Power Path

The block diagram in Figure 8-15 shows the AFE4403 Rx subsystem power routing. Internal LDOs running off RX_ANA_SUP and RX_DIG_SUP generate the 1.8-V supplies required to drive the internal blocks. The two receive supplies could be shorted to a single supply on the board.

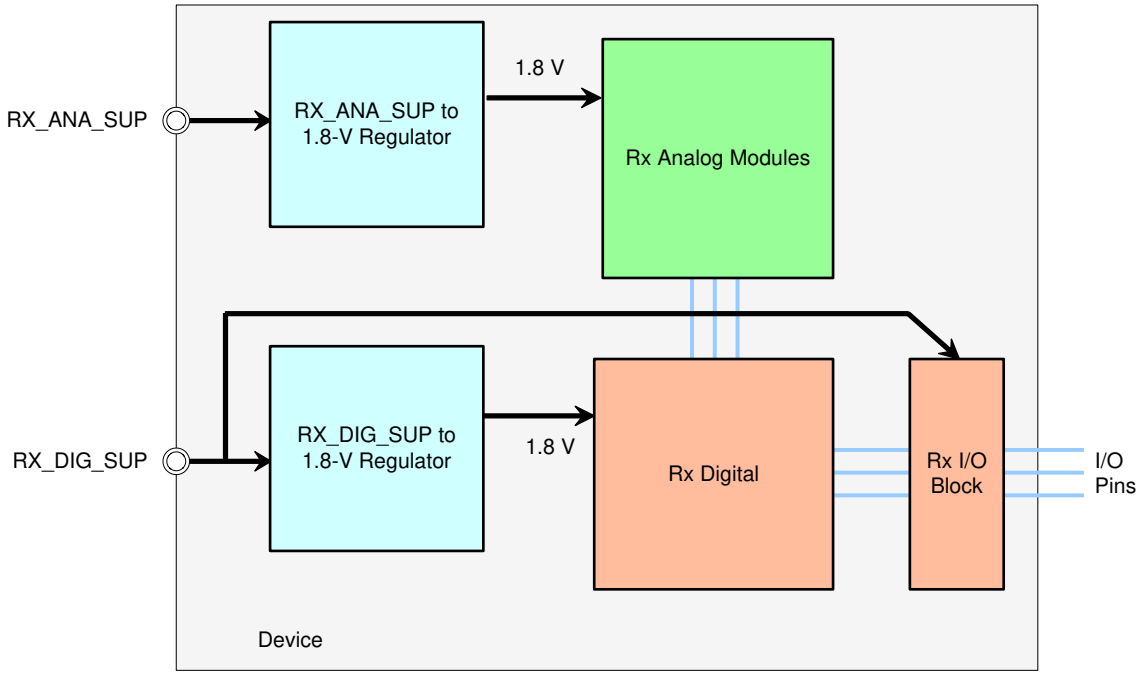


Figure 8-15. Receive Subsystem Power Routing

8.3.5 Transmit Section

The transmit section integrates the LED driver and the LED current control section with 8-bit resolution.

The RED and IR LED reference currents can be independently set. The current source (I_{LED}) locally regulates and ensures that the actual LED current tracks the specified reference. The transmitter section uses an internal 0.25-V reference voltage for operation. This reference voltage is available on the TX_REF pin and must be decoupled to ground with a 2.2-µF capacitor. The TX_REF voltage is derived from the TX_CTRL_SUP. The TX_REF voltage can be programmed from 0.25 V to 1 V. A lower TX_REF voltage allows a lower voltage to be supported on LED_DRV_SUP. However, the transmitter dynamic range falls in proportion to the voltage on TX_REF. Thus, a TX_REF setting of 0.5 V gives a 6-dB lower transmitter dynamic range as compared to a 1-V setting on TX_REF, and a 6-dB higher transmitter dynamic range as compared to a 0.25-V setting on TX_REF.

Note that reducing the value of the band-gap reference capacitor on the BG pin reduces the time required for the device to wake-up and settle. However, this reduction in time is a trade-off between wake-up time and noise performance.For example, reducing the value of the capacitors on the BG and TX_REF pins from 2.2 uF to 0.1 uF reduces the wake-up time (from complete power-down) from 1000 ms to 100 ms, but results in a few decibels of degradation in the transmitter dynamic range.

The minimum LED_DRV_SUP voltage required for operation depends on:

- Voltage drop across the LED (V_{LED}),
- Voltage drop across the external cable, connector, and any other component in series with the LED (V_{CABLE}), and
- Transmitter reference voltage.

See the Recommended Operating Conditions table for further details.

Two LED driver schemes are supported:

- An H-bridge drive for a two-terminal back-to-back LED package; see Figure 8-16.

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- A push-pull drive for a three-terminal LED package; see Figure 8-17.

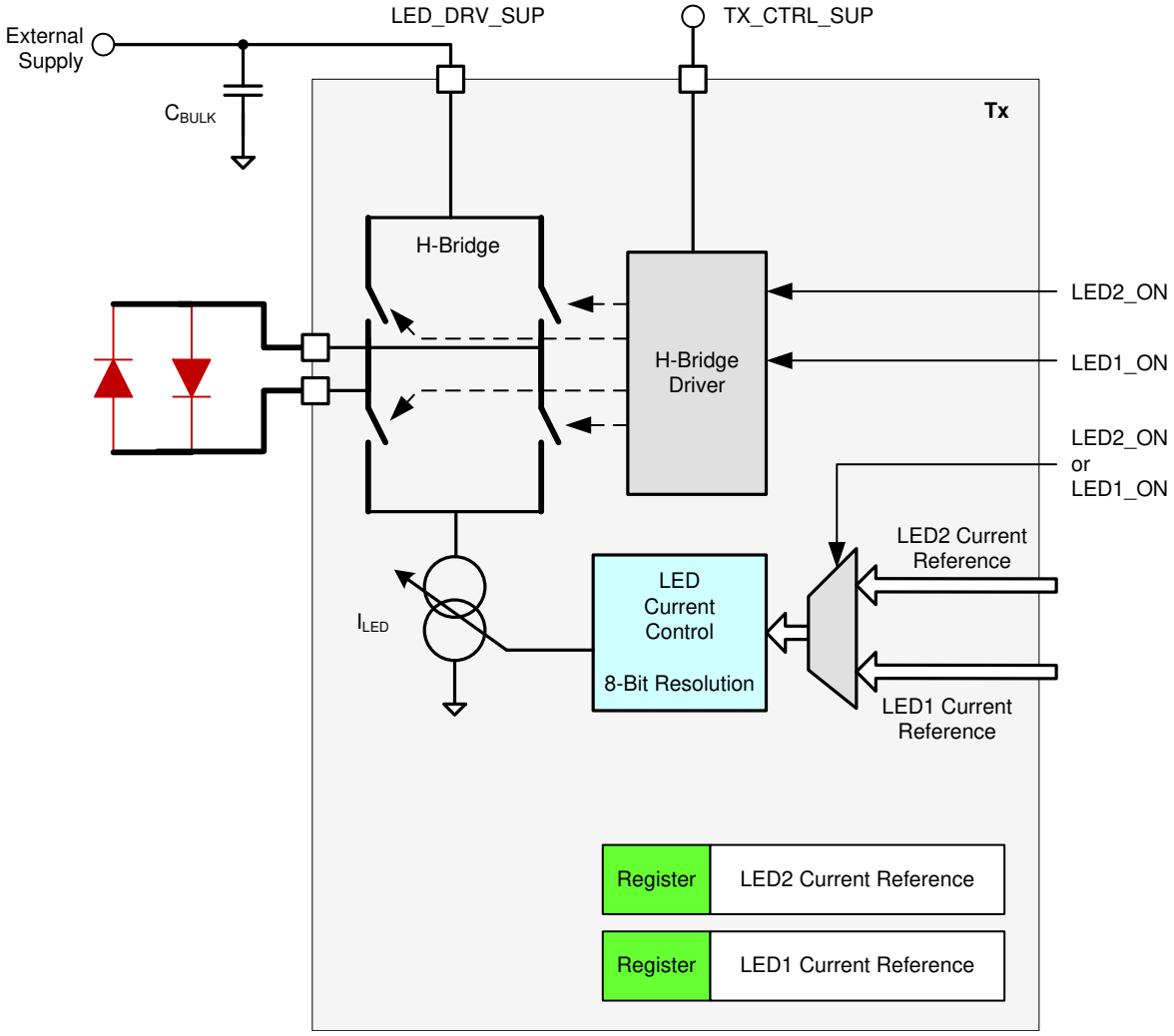


Figure 8-16. Transmit: H-Bridge Drive

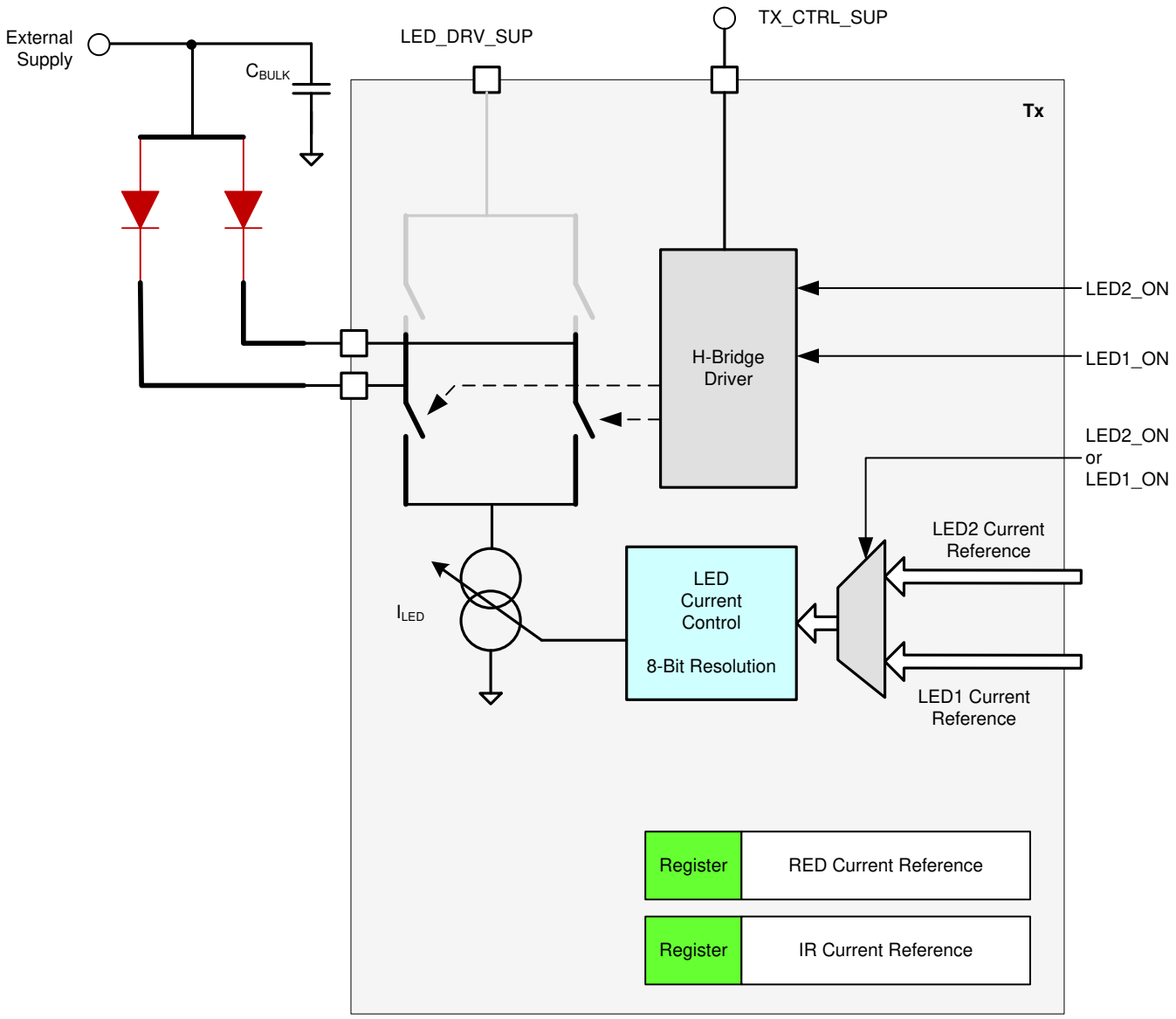


Figure 8-17. Transmit: Push-Pull LED Drive for Common Anode LED Configuration

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8.3.5.1 Third LED Support

A third LED can be optionally connected on the TX3 pin, as shown in Figure 8-18. An example application involving a third LED is where the Red and IR LEDs are connected on the TXP, TXN pins for pulse oximeter applications and a third LED (for example a Green LED) is connected on the TX3 pin for a heart rate monitoring application. The third LED can be connected only in common anode configuration. By programming the TX3_MODE register bit, the timing engine controls on TXP can be transferred to the TX3 pin. In this mode, the register bits that indicate the diagnostic results on the TXP pin now indicate the diagnostic results on the TX3 pin. The selection between using TX3 versus using TXP, TXN is intended as a static mode selection as opposed to a dynamic switching selection. A typical time delay of approximately 20 ms is required for the receive channel to settle after a change to the TX3_MODE setting. During this transition time, the receive signal chain should be active so that the filters are able to settle to the new signal level from the third LED.

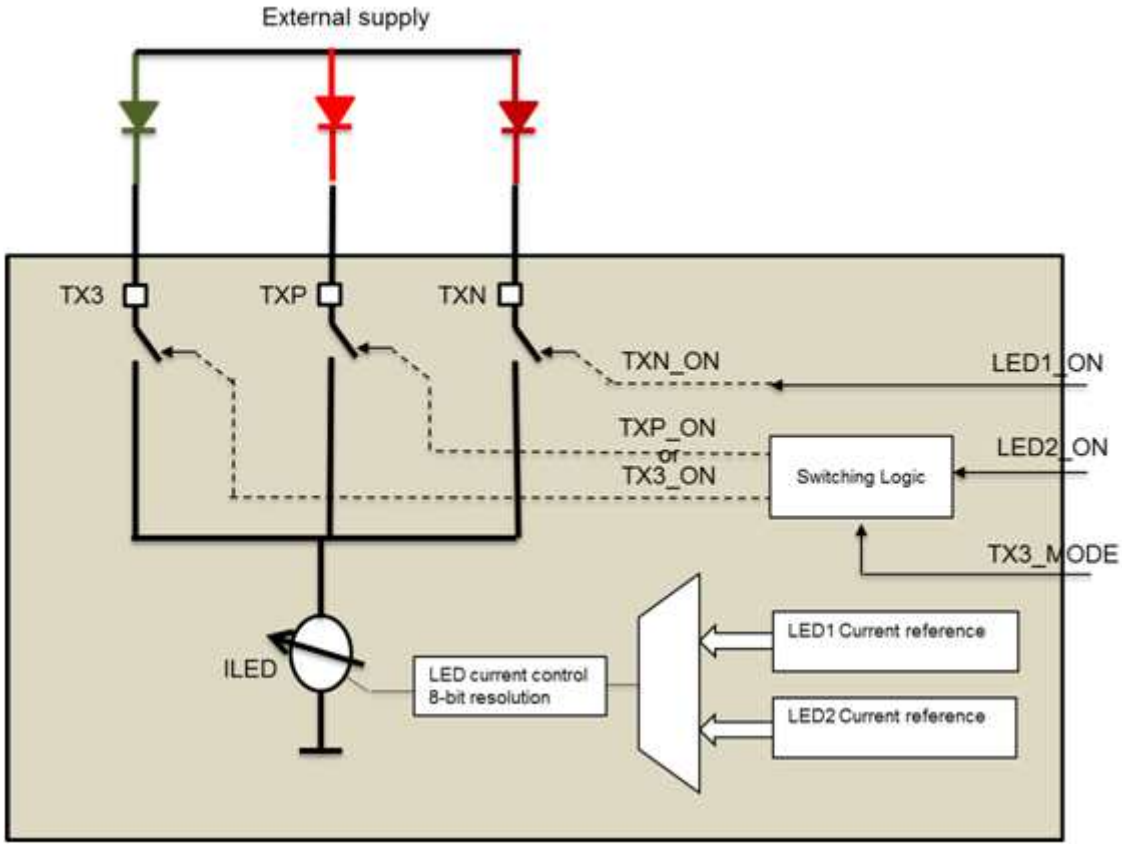


Figure 8-18. Multiplexing Third LED

8.3.5.2 Transmitter Power Path

The block diagram in Figure 8-19 shows the AFE4403 Tx subsystem power routing.

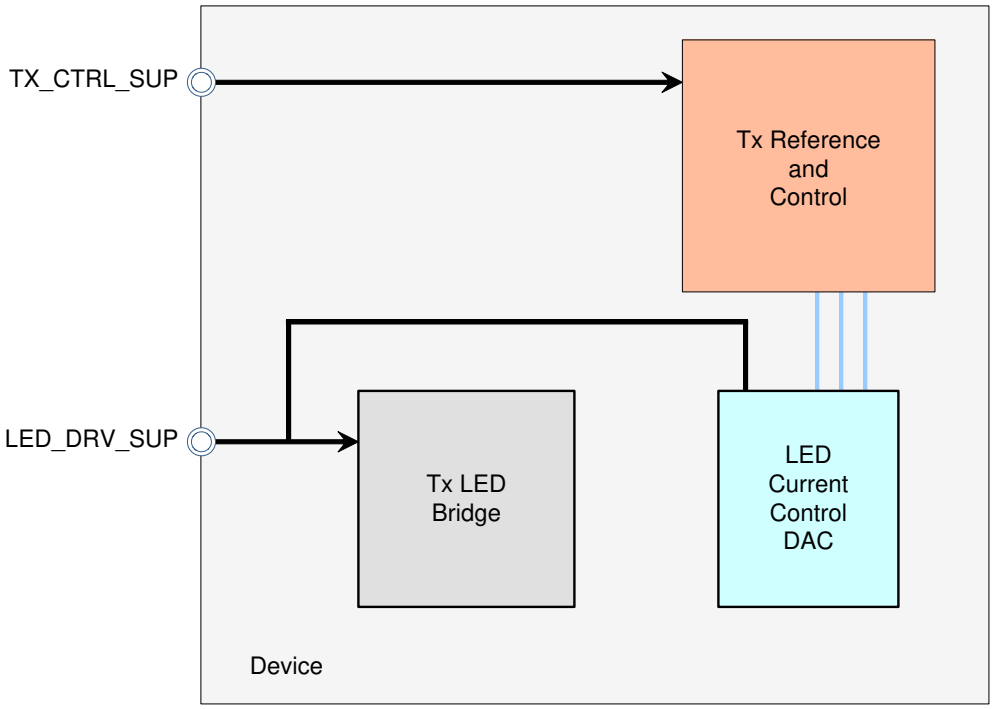


Figure 8-19. Transmit Subsystem Power Routing

8.3.5.3 LED Power Reduction During Periods of Inactivity

The diagram in Figure 8-20 shows how LED bias current passes 50 µA whenever LED_ON occurs. In order to minimize power consumption in periods of inactivity, the LED_ON control must be turned off. Furthermore, the TIMEREN bit in the CONTROL1 register should be disabled by setting the value to 0.

Note that depending on the LEDs used, the LED may sometimes appear dimly lit even when the LED current is set to 0 mA. This appearance is because of the switching leakage currents (as shown in Figure 8-20) inherent to the timer function. The dimmed appearance does not effect the ambient light level measurement because during the ambient cycle, LED_ON is turned off for the duration of the ambient measurement.

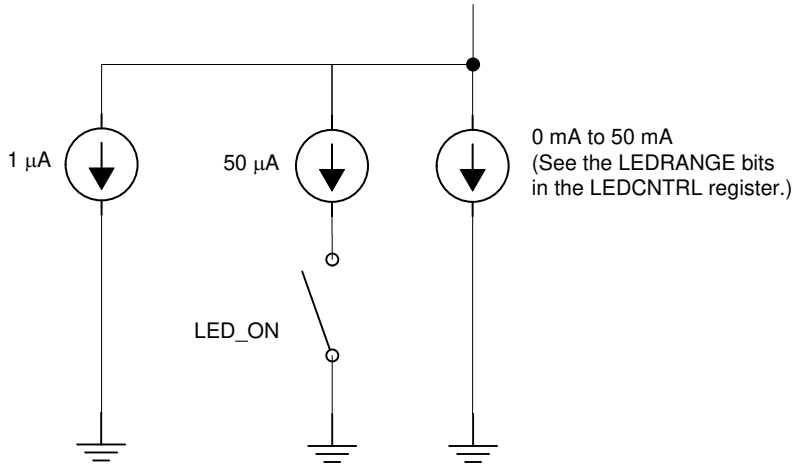


Figure 8-20. LED Bias Current

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8.3.5.4 LED Configurations

Multiple LED configurations are possible with the AFE4403.

Case 1: Red, IR LEDs in the common anode configuration for SPO2 and a Green LED for the HRM. Figure 8-21 shows the common anode configuration for this case. Figure 8-22 shows the configuration for HRM mode.

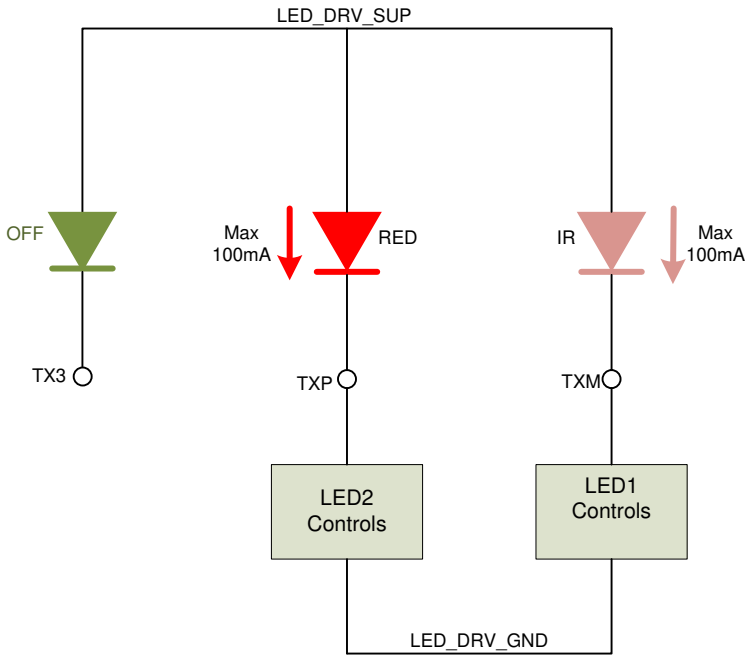


Figure 8-21. SPO2 Application, Common Anode Configuration

HRM mode: Set TX3_MODE = 1.

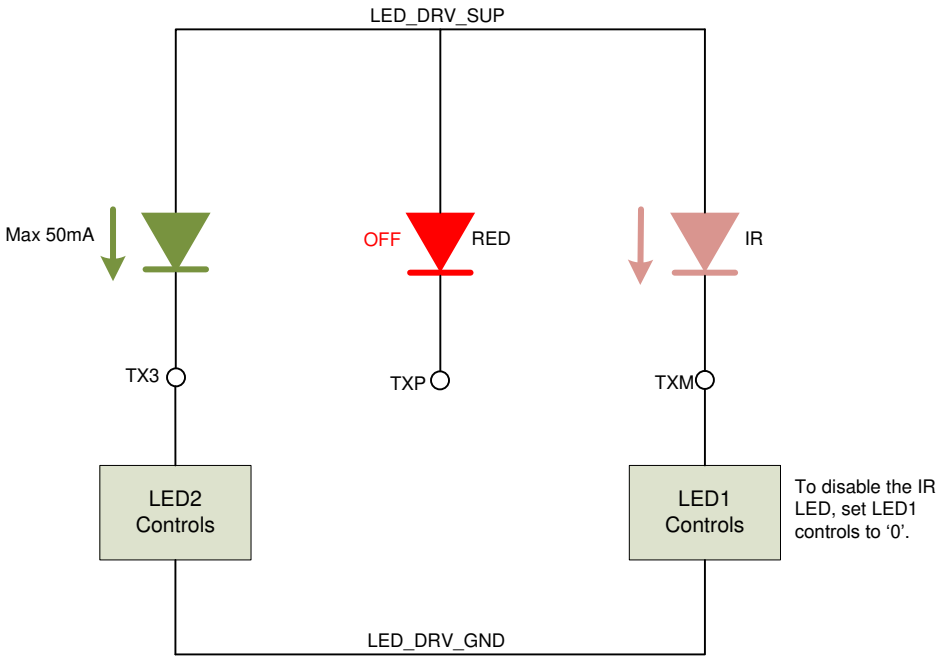


Figure 8-22. HRM Application Using the Third LED (Optional use of the IR LED)

Case 2: Red, IR LEDs in an H-bridge configuration for SPO2 and a Green LED for the HRM. The H-bridge configuration for this case is shown in Figure 8-23. Figure 8-24 shows the configuration for HRM mode.

SPO2 mode: Set TX3_MODE = 0.

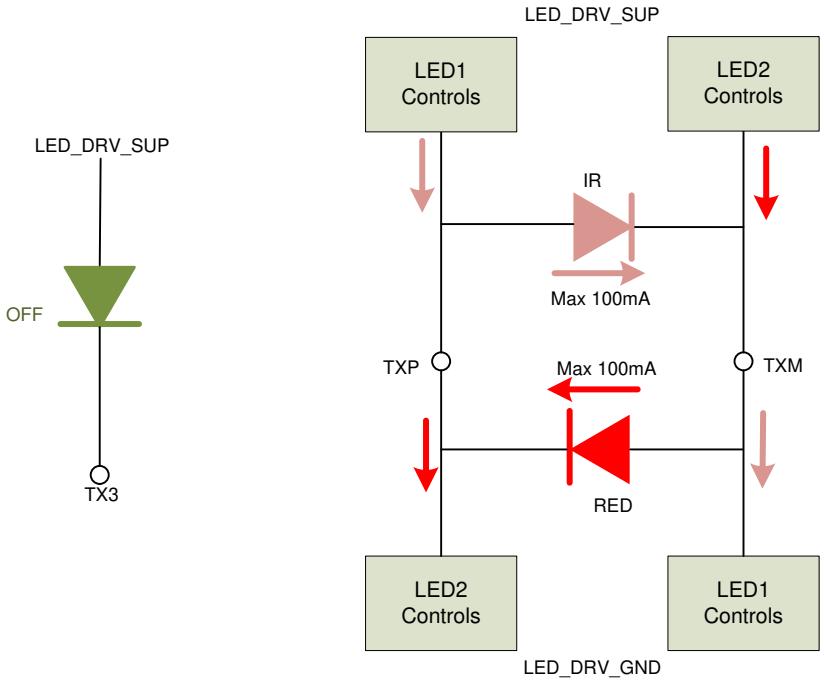


Figure 8-23. SPO2 Application, H-Bridge Configuration

HRM mode: Set TX3_MODE = 1.

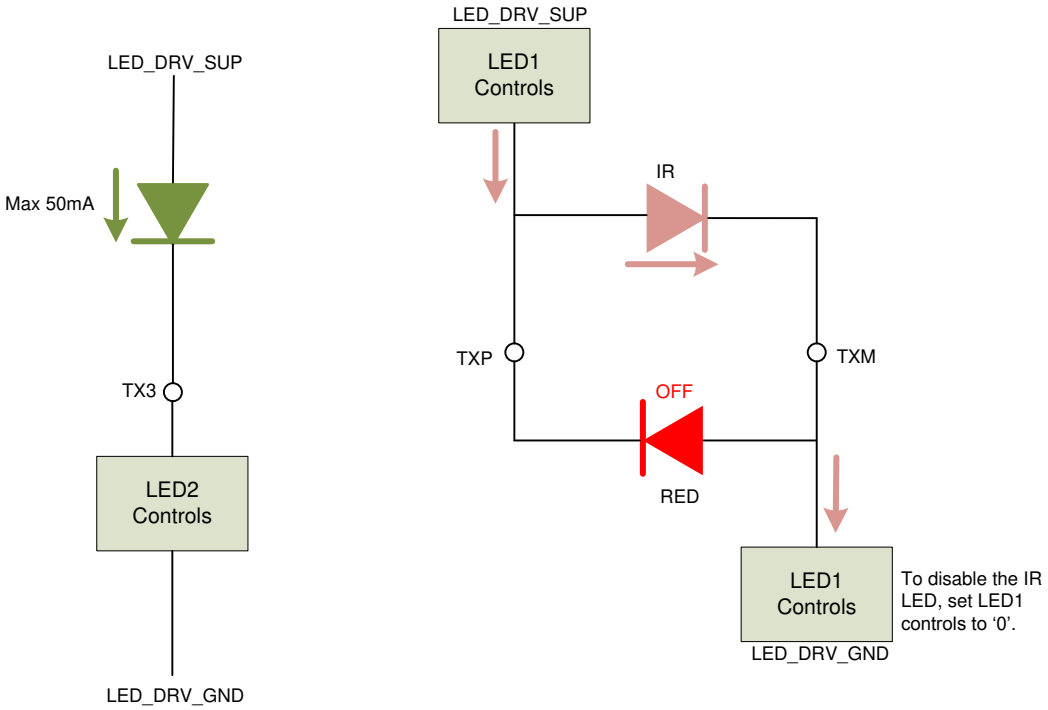


Figure 8-24. HRM Application Using the Third LED

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Case 3: Driving two LEDs simultaneously for HRM.

Some sensor modules have two LEDs on either side of the photodiode to make the illumination more uniform. The two LEDs can be connected in parallel, as shown in Figure 8-25.

The connection shown in Figure 8-25 results in an equal split of the current between the two LEDs if their forward voltages are exactly matched. High mismatch in the forward voltages of the two LEDs can cause one of them to consume the majority of the current.

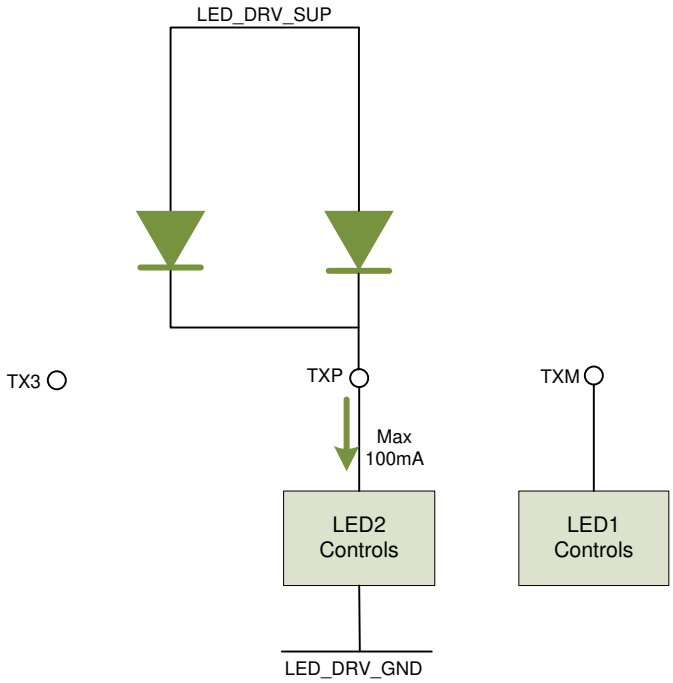


Figure 8-25. Using Two Parallel LEDs for an HRM Application

Case 4: Driving two LEDs separated in time for HRM.

The two LEDs can also be driven as shown in Figure 8-26.

While this mode of driving the two LEDs does not drive them simultaneously, there are two advantages in this case. First, the full current is available for driving each LED. Secondly, the mismatch in the forward voltages between the two LEDs does not play a role.

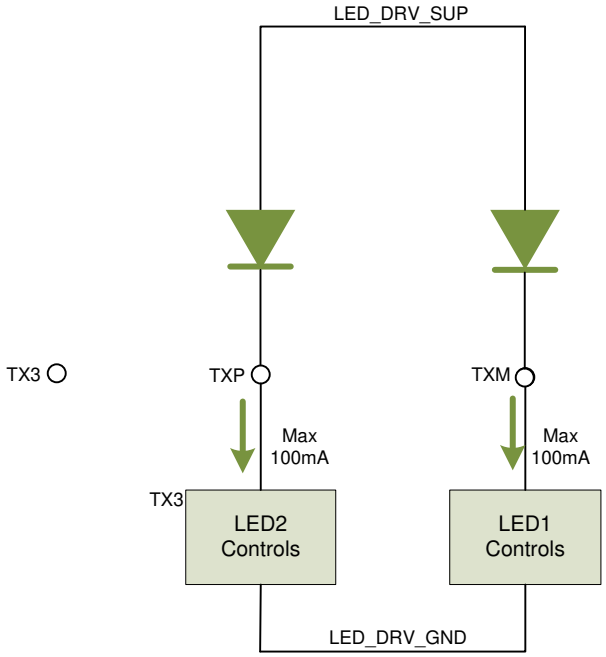


Figure 8-26. Using Two Parallel LEDs for an HRM Application with Separation in Timing

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8.4 Device Functional Modes

8.4.1 ADC Operation and Averaging Module

After the falling edge of the ADC reset signal, the ADC conversion phase starts (refer to Figure 8-14). Each ADC conversion takes 50 µs.

The ADC operates with averaging. The averaging module averages multiple ADC samples and reduces noise to improve dynamic range. Figure 8-27 shows a diagram of the averaging module. The ADC output is a 22-bit code that is obtained by discarding the two MSBs of the 24-bit registers (for example the register with address 2Ah), as shown in Table 8-3.

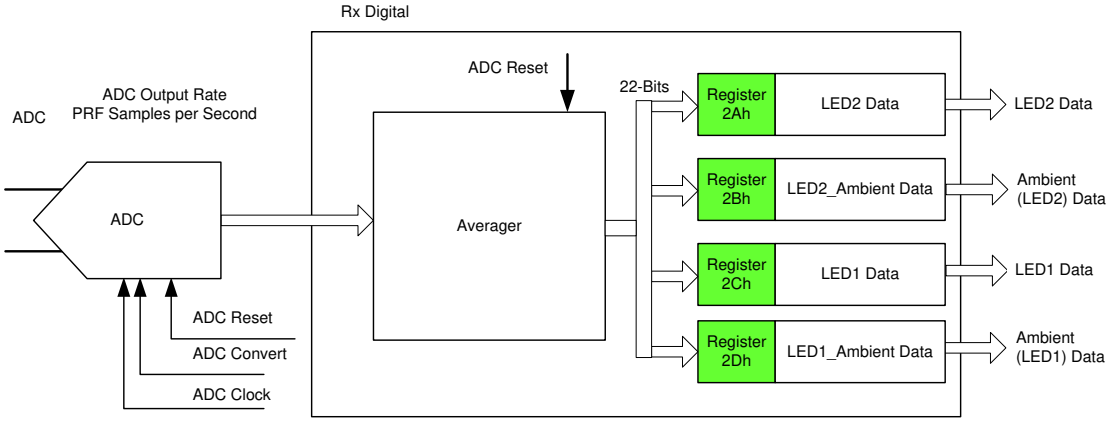


Figure 8-27. Averaging Module

Table 8-3. 22-Bit Word

23	22	21	20	19	18	17	16	15	14	13	12
Ignore				22-Bit ADC Code, MSB to LSB							
11	10	9	8	7	6	5	4	3	2	1	0
22-Bit ADC Code, MSB to LSB											

Table 8-4 shows the mapping of the input voltage to the ADC to its output code.

Table 8-4. ADC Input Voltage Mapping

DIFFERENTIAL INPUT VOLTAGE AT ADC INPUT	22-BIT ADC OUTPUT CODE
–1.2 V	1000000000000000000000
(–1.2 / 2^{21}) V	1111111111111111111111
0	0000000000000000000000
(1.2 / 2^{21}) V	0000000000000000000001
1.2 V	0111111111111111111111

The data format is binary twos complement format, MSB-first. Because the TIA has a full-scale range of ±1 V, TI recommends that the input to the ADC does not exceed ±1 V, which is approximately 80% of its full-scale.

In cases where having the processor read the data as a 24-bit word instead of a 22-bit word is more convenient, the entire register can be mapped to the input level as shown in Table 8-5.

Table 8-5. 24-Bit Word

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
24-Bit ADC Code, MSB to LSB																							

Table 8-6 shows the mapping of the input voltage to the ADC to its output code when the entire 24-bit word is considered.

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Table 8-6. Input Voltage Mapping

DIFFERENTIAL INPUT VOLTAGE AT ADC INPUT	24-BIT ADC OUTPUT CODE
–1.2 V	111000000000000000000000
(–1.2 / 2^{21}) V	111111111111111111111111
0	000000000000000000000000
(1.2 / 2^{21}) V	000000000000000000000001
1.2 V	000111111111111111111111

Now the data can be considered as a 24-bit data in binary twos complement format, MSB-first. The advantage of using the entire 24-bit word is that the ADC output is correct, even when the input is over the normal operating range.

ADC_RDY is an interrupt issued by the AFE which can be used by the MCU to read the registers. To maximize the conversion time available for each phase, the ADC Reset signals should be positioned at 0%, 25%, 50% and 75% of the PRF period. The position of the ADC_RDY corresponds to the position of the 1st ADC Reset signal (0% reset) in the PRF cycle. The contents of all six registers can be read out between the rising edge of ADC_RDY (0%) and the next ADC reset signal (25%).

8.4.1.1 Operation Without Averaging

In this mode, the ADC outputs a digital sample one time for every 50 µs. Consider a case where the ADC Reset signals are positioned at 25%, 50%, 75%, and 100% (or 0%) points in the pulse repetition period. At each rising edge of the ADC reset signal, one ADC conversion value is written into the result registers sequentially as follows (see Figure 8-28):

- At the 25% reset signal, the first ADC conversion sample is written to register 2Ah (Decimal address = 42).
- At the 50% reset signal, the second ADC conversion sample is written to register 2Bh (Decimal address = 43).
- At the 75% reset signal, the third ADC conversion sample is written to register 2Ch (Decimal address = 44).
- At the next 0% reset signal, the fourth ADC conversion sample is written to register 2Dh (Decimal address = 45).
- Every time the registers 2Ah and 2Bh are updated, the contents of the difference register 2Eh is updated. Similarly, every time the registers 2Ch and 2Dh are updated, the contents of the difference register 2Fh is updated.

The time window between the ADC_RDY (first ADC Reset) and the second ADC Reset represents the window where the contents of all the 6 registers correspond to the samples of the four conversion phases from the previous pulse repetition period.

The MCU could either read all of these registers during this time window, or could read each register separately in the time window where its contents are stable.

8.4.1.2 Operation With Averaging

In this mode, all ADC digital samples are accumulated and averaged after every 50 µs. At each rising edge of the ADC reset signal, one averaged ADC conversion value is written into the output registers sequentially, as follows (see Figure 8-29):

- At the 25% reset signal, the first averaged ADC sample is written to register 2Ah (Decimal address = 42).
- At the 50% reset signal, the second averaged ADC sample is written to register 2Bh (Decimal address = 43).
- At the 75% reset signal, the third averaged ADC sample is written to register 2Ch (Decimal address = 44).
- At the next 0% reset signal, the fourth averaged ADC sample is written to register 2Dh (Decimal address = 45).
- Every time the registers 2Ah and 2Bh are updated, the contents of the difference register 2Eh is updated. Similarly, every time the registers 2Ch and 2Dh are updated, the contents of the difference register 2Fh is updated.

The number of samples to be used per conversion phase is specified in the CONTROL1 register (NUMAV[7:0]). The user must specify the correct value for the number of averages, as described in Equation 6:

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$$\text{NUMAV[7:0]} + 1 = \left(\frac{0.25 \times \text{Pulse Repetition Period}}{50\ \mu\text{s}} \right) - 1 \quad (6)$$

Note that the 50-µs factor corresponds to a case where the internal clock of the AFE (after division) is exactly equal to 4 MHz. The factor scales linearly with the clock period being used.

Note that the number of average conversions is limited by 25% of the PRF. For example, eight samples can be averaged with PRF = 625 Hz, and four samples can be averaged with PRF = 1250 Hz.

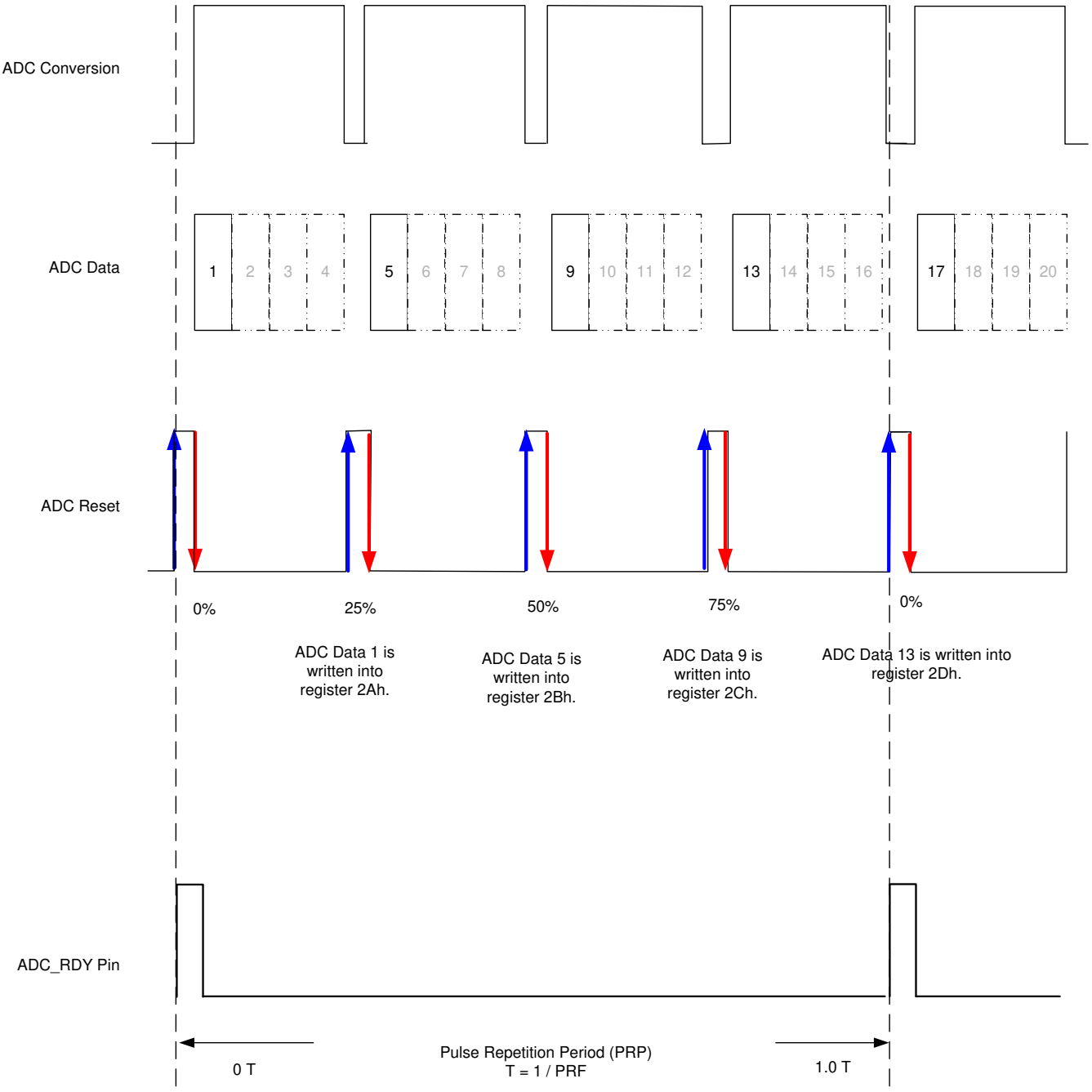
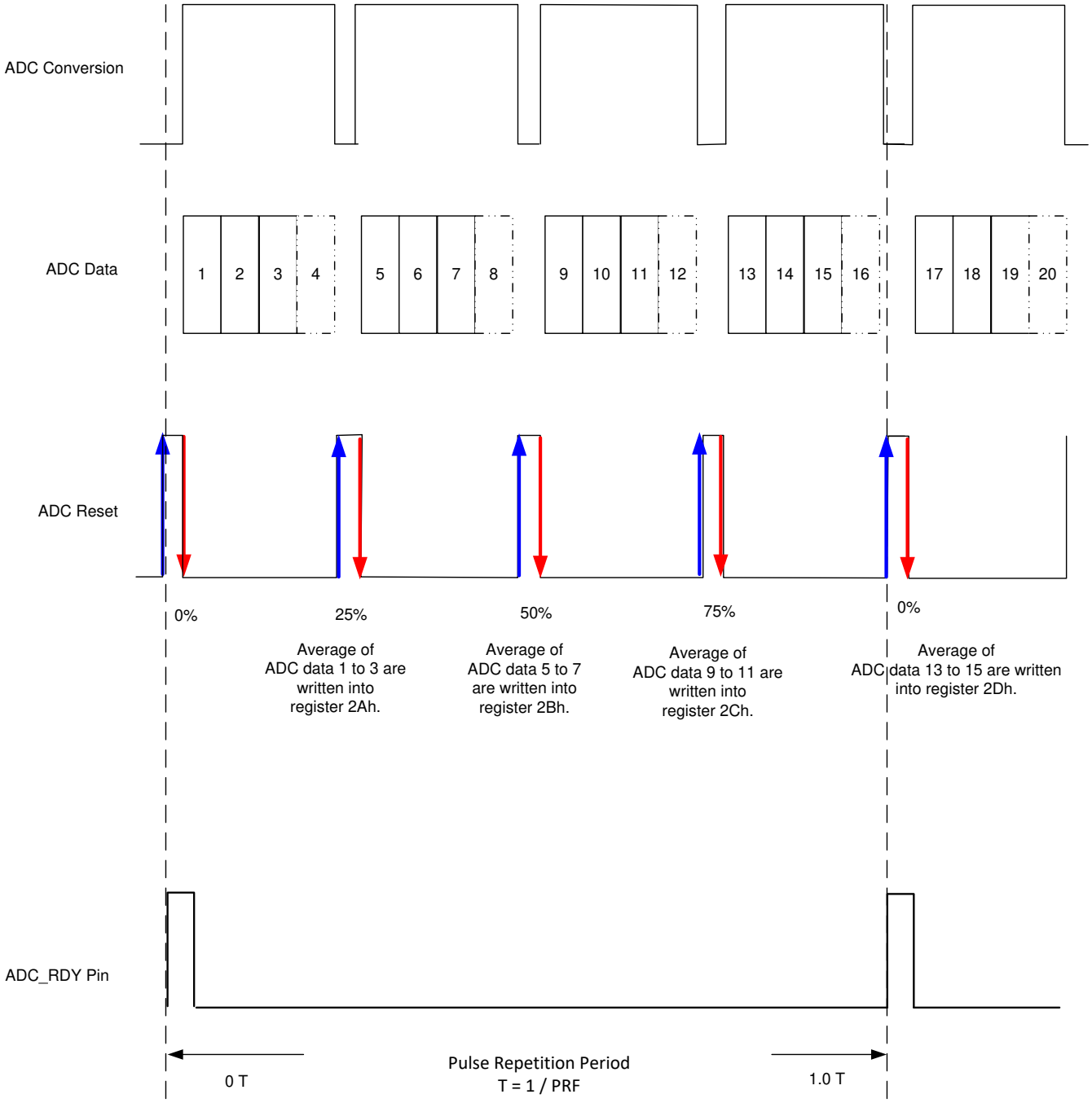


Figure 8-28. ADC Data Without Averaging (When Number of Averages = 0)

Note

Every time Register 2Ah or Register 2Bh are updated, the difference (Register 2Ah - register 2Bh) is written into register 2Eh. Every time Register 2Ch or Register 2Dh are updated, the difference (Register 2Ch - register 2Dh) is written into register 2Fh.



NOTE: Example is with three averages. The value of the NUMAVG[7:0] register bits = 2.

Figure 8-29. ADC Data with Averaging Enabled

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Note

Every time Register 2Ah or Register 2Bh are updated, the difference (Register 2Ah - register 2Bh) is written into register 2Eh. Every time Register 2Ch or Register 2Dh are updated, the difference (Register 2Ch - register 2Dh) is written into register 2Fh.

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8.4.1.3 Dynamic Power-Down Mode

When operated at low PRF, a dynamic power-down mode can be optionally enabled to shut off blocks during a portion of each period. This operation is illustrated in Figure 8-30. The dynamic power-down signal (called PDN_CYCLE) can be internally generated using the timing controller. PDN_CYCLE can be used to shut off power to internal blocks during the unused section within each pulse repetition period.

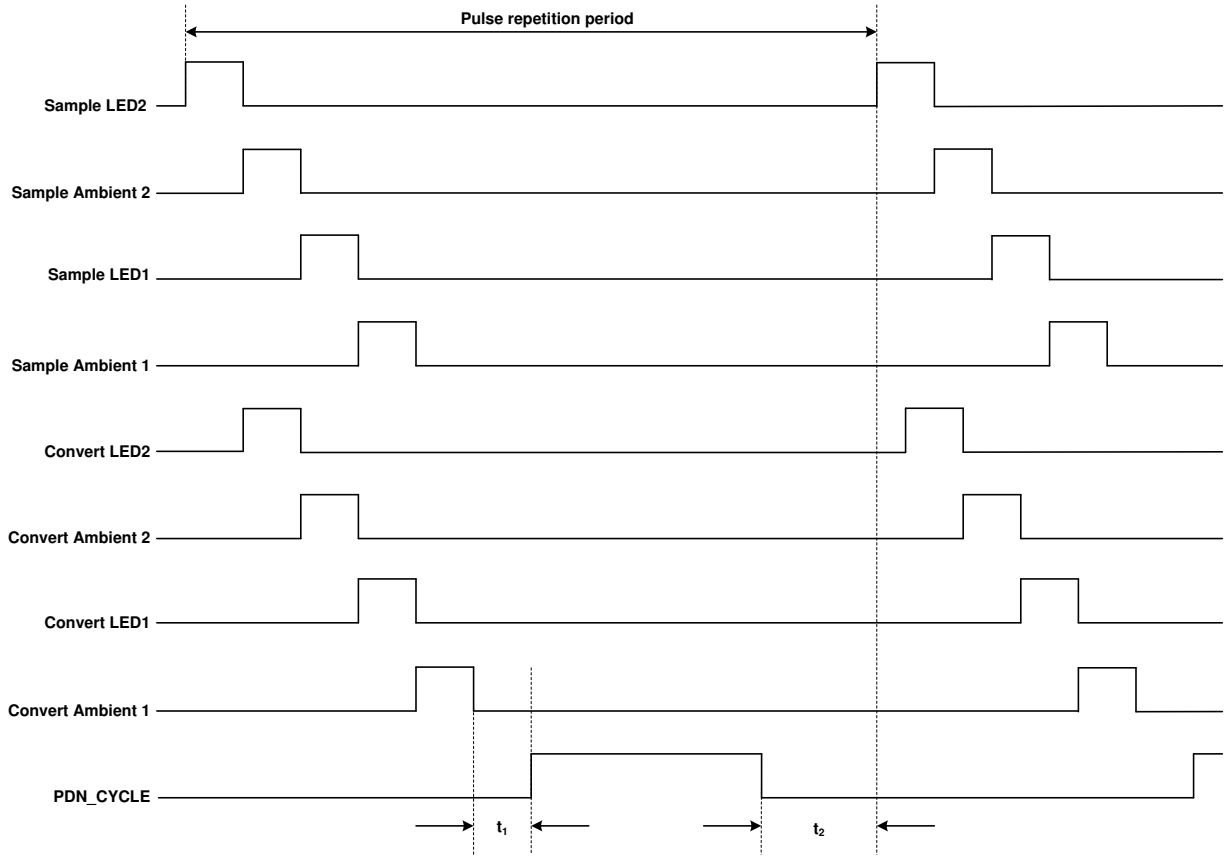


Figure 8-30. Dynamic Power-Down Mode Timing

t_1 and t_2 denote the timing margin between the active portion of the period and the dynamic power-down signal. TI recommends setting t_1 > 50 µs and t_2 > 200 µs in order to ensure sufficient time for the shutdown blocks to recover from power-down. By choosing the blocks that are shut down during dynamic power-down, a power savings of anywhere between 35% to 70% power can be achieved when the PDN_CYCLE phase is active.

The sequence of the convert phases within a pulse repetition period should be as follows: LED2 (Red) → Ambient 2 → LED1 (IR) → Ambient 1. The sample phases must precede the corresponding convert phase. Also note that the ADC_RDY signal coincides with the first ADC Reset signal. The time window between the ADC_RDY (first ADC Reset) and the second ADC Reset represents the window where the contents of all the 6 registers correspond to the samples of the four conversion phases from the previous pulse repetition period.

The MCU could either read all of these registers during this time window, or could read each register separately in the time window where its contents are stable.

The DYNAMIC1, DYNAMIC2, DYNAMIC3, and DYNAMIC4 bits determine which blocks are powered down during the dynamic power-down state (when PDN_CYCLE is high). For maximum power saving, all four bits can be set to 1. TI recommends setting t_1 to greater than 100 µs and t_2 to greater than 200 µs to ensure that the blocks recover from power-down in time for the next cycle.

The bit corresponding to the TIA power-down (DYNAMIC3) needs a bit more consideration. When the TIA is powered down, the TIA no longer maintains the bias across the photodiode output. This loss of bias can cause the photodiode output voltage to drift from the normal value. The recovery time constant associated with the

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photodiode returning to a proper bias condition (when the TIA is powered back on) is approximately equal to 2 × C_{PD} × R_F, where C_{PD} is the effective differential capacitance of the photodiode and R_F is the TIA gain setting. This consideration might result in a different choice for the value of t_2.

8.4.2 Diagnostics

The device includes diagnostics to detect open or short conditions of the LED and photosensor, LED current profile feedback, and cable on or off detection.

8.4.2.1 Photodiode-Side Fault Detection

Figure 8-31 shows the diagnostic for the photodiode-side fault detection.

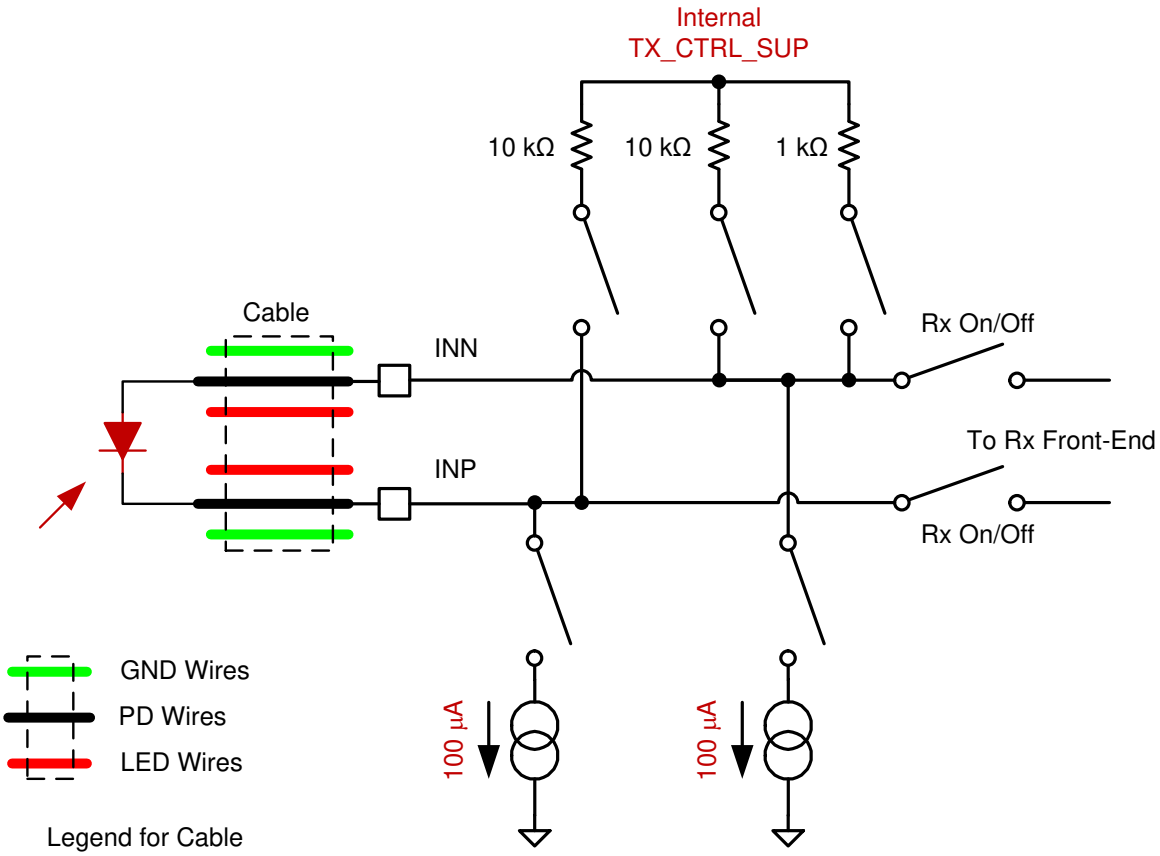


Figure 8-31. Photodiode Diagnostic

8.4.2.2 Transmitter-Side Fault Detection

Figure 8-32 shows the diagnostic for the transmitter-side fault detection.

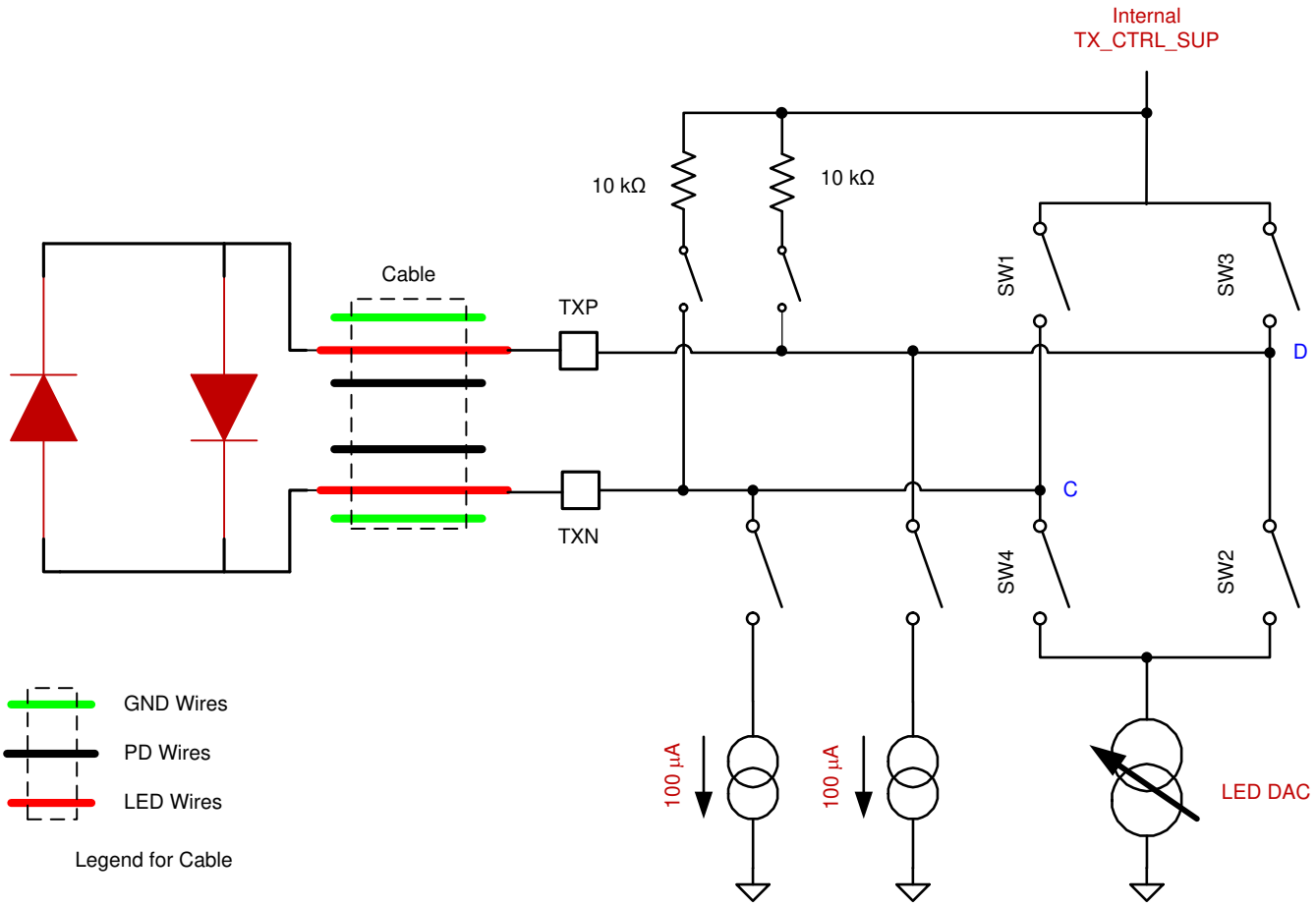


Figure 8-32. Transmitter Diagnostic

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8.4.2.3 Diagnostics Module

The diagnostics module, when enabled, checks for nine types of faults sequentially. The results of all faults are latched in 11 separate flags.

The status of all flags can also be read using the SPI interface. Table 8-7 details each fault and flag used. Note that the diagnostics module requires all AFE blocks to be enabled in order to function reliably.

Table 8-7. Fault and Flag Diagnostics

MODULE(1)	SEQ.	FAULT	FLAG1	FLAG2	FLAG3	FLAG4	FLAG5	FLAG6	FLAG7	FLAG8	FLAG9	FLAG10	FLAG11
—	—	No fault	0	0	0	0	0	0	0	0	0	0	0
PD	1	Rx INP cable shorted to LED cable	1										
	2	Rx INN cable shorted to LED cable		1									
	3	Rx INP cable shorted to GND cable			1								
	4	Rx INN cable shorted to GND cable				1							
	5	PD open or shorted					1	1					
LED	6	Tx OUTM line shorted to GND cable							1				
	7	Tx OUTP line shorted to GND cable								1			
	8	LED open or shorted									1	1	
	9	LED open or shorted											1

(1) Resistances below 10 kΩ are considered to be shorted.

Figure 8-33 shows the timing for the diagnostic function.

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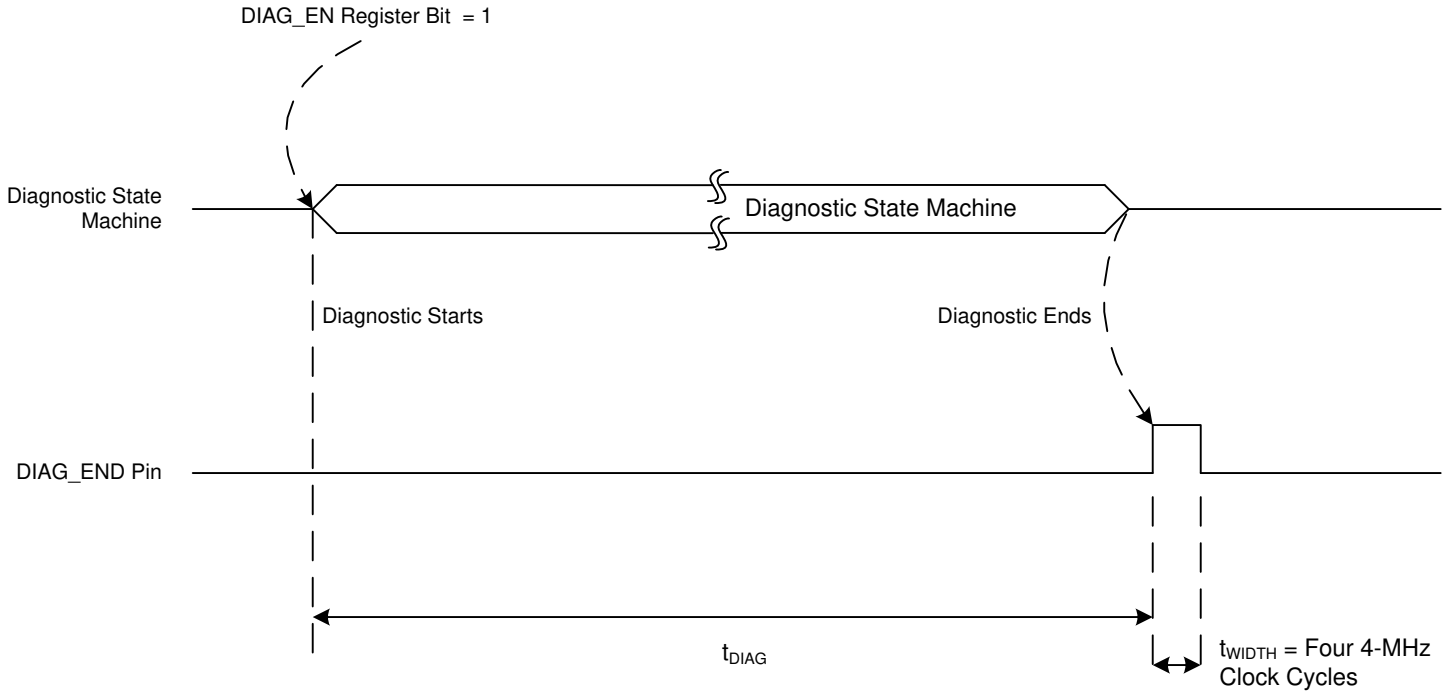


Figure 8-33. Diagnostic Timing Diagram

By default, the diagnostic function takes t_{DIAG} = 16 ms to complete. After the diagnostics function completes, the AFE4403 filter must be allowed time to settle. See the *Electrical Characteristics* for the filter settling time.

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8.5 Programming

8.5.1 Serial Programming Interface

The SPI-compatible serial interface consists of four signals: SCLK (serial clock), SPISOMI (serial interface data output), SPISIMO (serial interface data input), and SPISTE (serial interface enable).

The serial clock (SCLK) is the serial peripheral interface (SPI) serial clock. SCLK shifts in commands and shifts out data from the device. SCLK features a Schmitt-triggered input and clocks data out on the SPISOMI. Data are clocked in on the SPISIMO pin. Even though the input has hysteresis, TI recommends keeping SCLK as clean as possible to prevent glitches from accidentally shifting the data. When the serial interface is idle, hold SCLK low.

The SPI serial out master in (SPISOMI) pin is used with SCLK to clock out the AFE4403 data. The SPI serial in master out (SPISIMO) pin is used with SCLK to clock in data to the AFE4403. The SPI serial interface enable (SPISTE) pin enables the serial interface to clock data on the SPISIMO pin in to the device.

8.5.2 Reading and Writing Data

The device has a set of internal registers that can be accessed by the serial programming interface formed by the SPISTE, SCLK, SPISIMO, and SPISOMI pins.

8.5.2.1 Writing Data

The SPI_READ register bit must be first set to 0 before writing to a register. When SPISTE is low:

- Serially shifting bits into the device is enabled.
- Serial data (on the SPISIMO pin) are latched at every SCLK rising edge.
- The serial data are loaded into the register at every 32nd SCLK rising edge.

In case the word length exceeds a multiple of 32 bits, the excess bits are ignored. Data can be loaded in multiples of 32-bit words within a single active SPISTE pulse. The first eight bits form the register address and the remaining 24 bits form the register data. Figure 8-34 shows an SPI timing diagram for a single write operation. For multiple read and write cycles, refer to the *Multiple Data Reads and Writes* section.

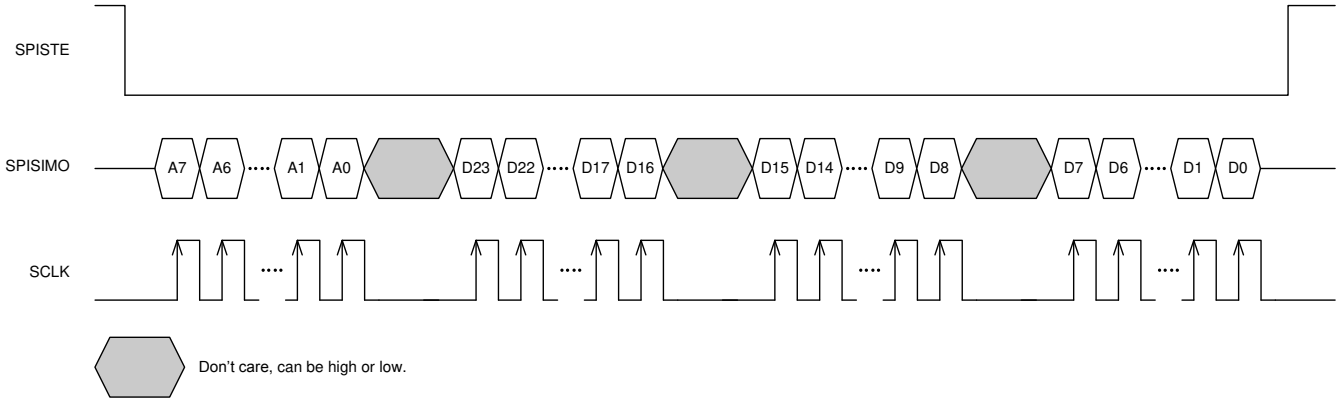
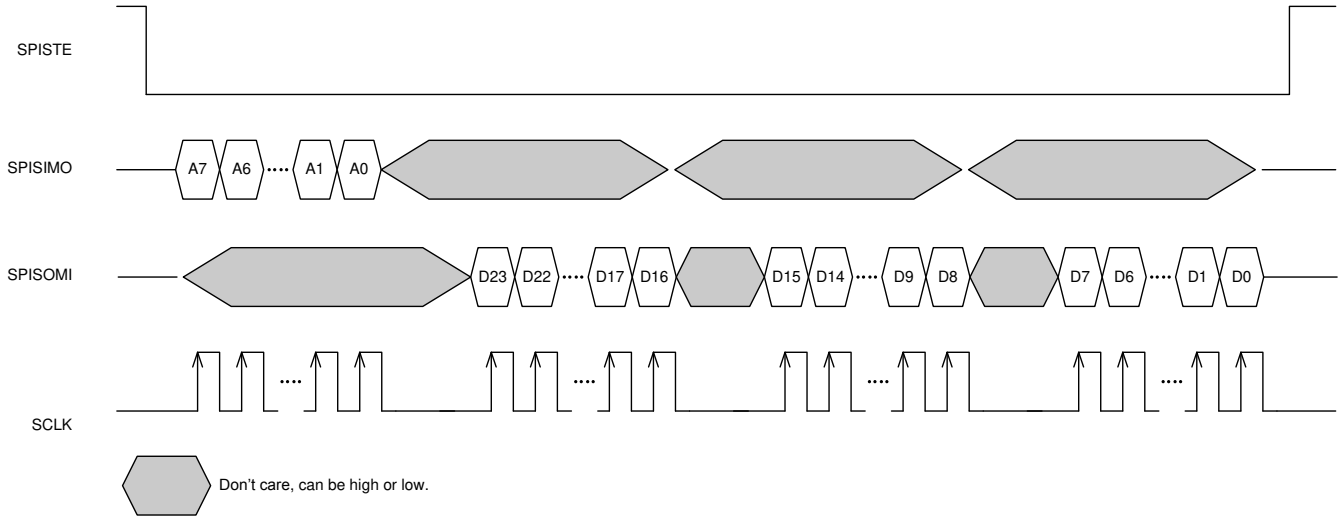


Figure 8-34. AFE SPI Write Timing Diagram

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8.5.2.2 Reading Data

The SPI_READ register bit must be first set to 1 before reading from a register. The AFE4403 includes a mode where the contents of the internal registers can be read back on the SPISOMI pin. This mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the AFE. To enable this mode, first set the SPI_READ register bit using the SPI write command, as described in the *Writing Data* section. In the next command, specify the SPI register address with the desired content to be read. Within the same SPI command sequence, the AFE outputs the contents of the specified register on the SPISOMI pin. Figure 8-35 shows an SPI timing diagram for a single read operation. For multiple read and write cycles, refer to the *Multiple Data Reads and Writes* section.



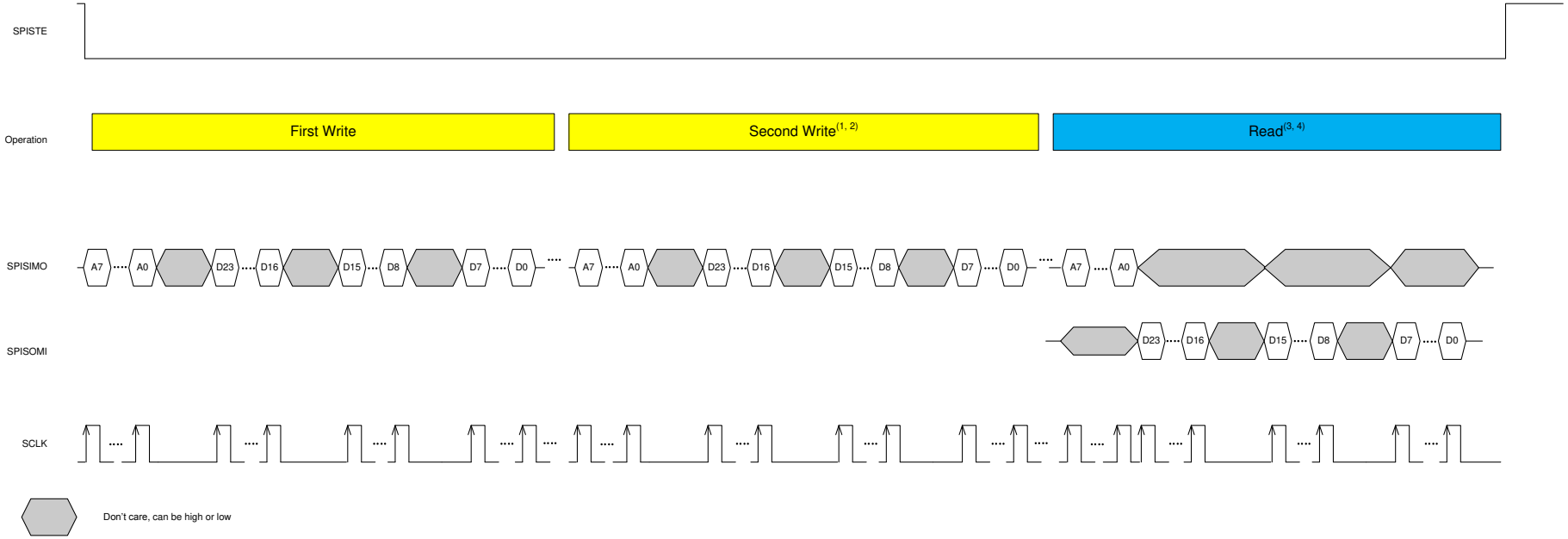
A. The SPI_READ register bit must be enabled before attempting a serial readout from the AFE.
B. Specify the register address of the content that must be readback on bits A[7:0].
C. The AFE outputs the contents of the specified register on the SPISOMI pin.

Figure 8-35. AFE SPI Read Timing Diagram

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8.5.2.3 Multiple Data Reads and Writes

The device includes functionality where multiple read and write operations can be performed during a single SPISTE event. To enable this functionality, the first eight bits determine the register address to be written and the remaining 24 bits determine the register data. Perform two writes with the SPI read bit enabled during the second write operation in order to prepare for the read operation, as described in the *Writing Data* section. In the next command, specify the SPI register address with the desired content to be read. Within the same SPI command sequence, the AFE outputs the contents of the specified register on the SPISOMI pin. This functionality is described in the *Writing Data* and *Reading Data* sections. Figure 8-36 shows a timing diagram for the SPI multiple read and write operations.



A. The SPI read register bit must be enabled before attempting a serial readout from the AFE.
B. The second write operation must be configured for register 0 with data 000001h.
C. Specify the register address whose contents must be read back on A[7:0].
D. The AFE outputs the contents of the specified register on the SPISOMI pin.

Figure 8-36. Serial Multiple Read and Write Operations

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8.5.2.4 Register Initialization

After power-up, the internal registers **must** be initialized to the default values. This initialization can be done in one of two ways:

- Through a hardware reset by applying a low-going pulse on the $\overline{\text{RESET}}$ pin, or
- By applying a software reset. Using the serial interface, set SW_RESET (bit D3 in register 00h) high. This setting initializes the internal registers to the default values and then self-resets to 0. In this case, the $\overline{\text{RESET}}$ pin is kept high (inactive).

8.5.2.5 AFE SPI Interface Design Considerations

Note that when the AFE4403 is deselected, the SPISOMI, CLKOUT, ADC_RDY, and DIAG_END digital output pins do not enter a 3-state mode. This condition, therefore, must be taken into account when connecting multiple devices to the SPI port and for power-management considerations. In order to avoid loading the SPI bus when multiple devices are connected, the SOMI_TRI register bit must be to 1 whenever the AFE SPI is inactive. The DIGOUT_TRISTATE register bit must be set to 1 to tri-state the ADC_RDY and DIAG_END pins. The CLKOUT_TRI register bit must be set to 1 to put the CLKOUT buffer in tri-state mode.

8.6 Register Maps

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8.6.1 AFE Register Map

The AFE consists of a set of registers that can be used to configure it, such as receiver timings, I-V amplifier settings, transmit LED currents, and so forth. The registers and their contents are listed in Table 8-8. These registers can be accessed using the AFE SPI interface.

Table 8-8. AFE Register Map

NAME	REGISTER CONTROL(1)	ADDRESS		REGISTER DATA																						
		Hex	Dec	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONTROL0	W	00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SW_RST	DIAG_EN	TIM_COUNT_RST	SPI_READ
LED2STC	R/W	01	1	0	0	0	0	0	0	0	0	LED2STC[15:0]															
LED2ENDC	R/W	02	2	0	0	0	0	0	0	0	0	LED2ENDC[15:0]															
LED2LEDSTC	R/W	03	3	0	0	0	0	0	0	0	0	LED2LEDSTC[15:0]															
LED2LEDENDC	R/W	04	4	0	0	0	0	0	0	0	0	LED2LEDENDC[15:0]															
ALED2STC	R/W	05	5	0	0	0	0	0	0	0	0	ALED2STC[15:0]															
ALED2ENDC	R/W	06	6	0	0	0	0	0	0	0	0	ALED2ENDC[15:0]															
LED1STC	R/W	07	7	0	0	0	0	0	0	0	0	LED1STC[15:0]															
LED1ENDC	R/W	08	8	0	0	0	0	0	0	0	0	LED1ENDC[15:0]															
LED1LEDSTC	R/W	09	9	0	0	0	0	0	0	0	0	LED1LEDSTC[15:0]															
LED1LEDENDC	R/W	0A	10	0	0	0	0	0	0	0	0	LED1LEDENDC[15:0]															
ALED1STC	R/W	0B	11	0	0	0	0	0	0	0	0	ALED1STC[15:0]															
ALED1ENDC	R/W	0C	12	0	0	0	0	0	0	0	0	ALED1ENDC[15:0]															
LED2CONVST	R/W	0D	13	0	0	0	0	0	0	0	0	LED2CONVST[15:0]															
LED2CONVEND	R/W	0E	14	0	0	0	0	0	0	0	0	LED2CONVEND[15:0]															
ALED2CONVST	R/W	0F	15	0	0	0	0	0	0	0	0	ALED2CONVST[15:0]															
ALED2CONVEND	R/W	10	16	0	0	0	0	0	0	0	0	ALED2CONVEND[15:0]															
LED1CONVST	R/W	11	17	0	0	0	0	0	0	0	0	LED1CONVST[15:0]															
LED1CONVEND	R/W	12	18	0	0	0	0	0	0	0	0	LED1CONVEND[15:0]															
ALED1CONVST	R/W	13	19	0	0	0	0	0	0	0	0	ALED1CONVST[15:0]															
ALED1CONVEND	R/W	14	20	0	0	0	0	0	0	0	0	ALED1CONVEND[15:0]															
ADCRSTSTCT0	R/W	15	21	0	0	0	0	0	0	0	0	ADCRSTCT0[15:0]															
ADCRSTENDCT0	R/W	16	22	0	0	0	0	0	0	0	0	ADCRENDCT0[15:0]															
ADCRSTSTCT1	R/W	17	23	0	0	0	0	0	0	0	0	ADCRSTCT1[15:0]															
ADCRSTENDCT1	R/W	18	24	0	0	0	0	0	0	0	0	ADCRENDCT1[15:0]															
ADCRSTSTCT2	R/W	19	25	0	0	0	0	0	0	0	0	ADCRSTCT2[15:0]															
ADCRSTENDCT2	R/W	1A	26	0	0	0	0	0	0	0	0	ADCRENDCT2[15:0]															
ADCRSTSTCT3	R/W	1B	27	0	0	0	0	0	0	0	0	ADCRSTCT3[15:0]															
ADCRSTENDCT3	R/W	1C	28	0	0	0	0	0	0	0	0	ADCRENDCT3[15:0]															
PRPCOUNT	R/W	1D	29	0	0	0	0	0	0	0	0	PRPCT[15:0]															
CONTROL1	R/W	1E	30	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TIMEREN	NUMAV[7:0]							
SPARE1	N/A	1F	31	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 8-8. AFE Register Map (continued)

NAME	REGISTER CONTROL(1)	ADDRESS		REGISTER DATA																							
		Hex	Dec	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIAGAIN	R/W	20	32	0	0	0	0	0	0	0	0	ENSEPGAN	STAGE2EN1	0	0	0	STG2GAIN1[2:0]			CF_LED1[4:0]					RF_LED1[2:0]		
TIA_AMB_GAIN	R/W	21	33	0	0	0	0	AMBDAC[3:0]				FLTRCNRSEL	STAGE2EN	0	0	0	STG2GAIN2[2:0]			CF_LED[4:0]					RF_LED[2:0]		
LEDCNTRL	R/W	22	34	0	0	0	0	0	0	LED_RANGE[1:0]		LED1[7:0]								LED2[7:0]							
CONTROL2	R/W	23	35	0	0	0	DYNAMIC1	0	TX_REF1	TX_REF0	0	0	DYNAMIC2	0	0	TXBRGMOD	DIGOUT_TRISTATE	XTALDIS	EN_SLOW_DIAG	0	0	0	DYNAMIC3	DYNAMIC4	PDNTX	PDNRX	PDNAFE
SPARE2	N/A	24	36	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPARE3	N/A	25	37	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPARE4	N/A	26	38	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED1	N/A	27	39	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
RESERVED2	N/A	28	40	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
ALARM	R/W	29	41	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LED2VAL	R	2A	42	LED2VAL[23:0]																							
ALED2VAL	R	2B	43	ALED2VAL[23:0]																							
LED1VAL	R	2C	44	LED1VAL[23:0]																							
ALED1VAL	R	2D	45	ALED1VAL[23:0]																							
LED2-ALED2VAL	R	2E	46	LED2-ALED2VAL[23:0]																							
LED1-ALED1VAL	R	2F	47	LED1-ALED1VAL[23:0]																							
DIAG	R	30	48	0	0	0	0	0	0	0	0	0	0	0	PD_ALM	LED_ALM	LED2OPEN	LED1OPEN	LEDSC	OUTNSHGND	OUTPSHGND	PDOC	PDSC	INNSCGND	INPSCGND	INNSCLED	INPSCLED
CONTROL3	R/W	31	49	0	0	0	0	0	0	0	0	TX3_MODE	0	0	0	0	0	0	0	0	0	0	SOMI_TRI	CLKOUT_TRI	CLKDIV[2:0]		
PDNCYCLESTC	R/W	32	50	0	0	0	0	0	0	0	0	PDNCYCLESTC[15:0]															
PDNCYCLEENDC	R/W	33	51	0	0	0	0	0	0	0	0	PDNCYCLEENDC[15:0]															

(1) R = read only, R/W = read or write, N/A = not available, and W = write only.

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8.6.2 AFE Register Description

Figure 8-34. CONTROL0: Control Register 0 (Address = 00h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	0	0	0	0
11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	SW_RST	DIAG_EN	TIM_ COUNT_ RST	SPI_ READ

This register is write-only. CONTROL0 is used for AFE software and count timer reset, diagnostics enable, and SPI read functions.

Bits 23:4 **Must be 0**

Bit 3 **SW_RST: Software reset**

0 = No action (default after reset)
1 = Software reset applied; resets all internal registers to the default values and self-clears to 0

Bit 2 **DIAG_EN: Diagnostic enable**

0 = No action (default after reset)
1 = Diagnostic mode is enabled and the diagnostics sequence starts when this bit is set.
At the end of the sequence, all fault status are stored in the DIAG: Diagnostics Flag Register. Afterwards, the DIAG_EN register bit self-clears to 0.
Note that the diagnostics enable bit is automatically reset after the diagnostics completes (16 ms). During the diagnostics mode, ADC data are invalid because of the toggling diagnostics switches.

Bit 1 **TIM_CNT_RST: Timer counter reset**

0 = Disables timer counter reset, required for normal timer operation (default after reset)
1 = Timer counters are in reset state

Bit 0 **SPI READ: SPI read**

0 = SPI read is disabled (default after reset)
1 = SPI read is enabled

Figure 8-35. LED2STC: Sample LED2 Start Count Register (Address = 01h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	LED2STC[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
LED2STC[15:0]											

This register sets the start timing value for the LED2 signal sample.

Bits 23:16 **Must be 0**

Bits 15:0 **LED2STC[15:0]: Sample LED2 start count**

The contents of this register can be used to position the start of the sample LED2 signal with respect to the pulse repetition period (PRP), as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

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Figure 8-36. LED2ENDC: Sample LED2 End Count Register (Address = 02h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	LED2ENDC[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
LED2ENDC[15:0]											

This register sets the end timing value for the LED2 signal sample.

Bits 23:16 **Must be 0**

Bits 15:0 **LED2ENDC[15:0]: Sample LED2 end count**

The contents of this register can be used to position the end of the sample LED2 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 8-37. LED2LEDSTC: LED2 LED Start Count Register (Address = 03h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	LED2LEDSTC[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
LED2LEDSTC[15:0]											

This register sets the start timing value for when the LED2 signal turns on.

Bits 23:16 **Must be 0**

Bits 15:0 **LED2LEDSTC[15:0]: LED2 start count**

The contents of this register can be used to position the start of the LED2 with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 8-38. LED2LEDENDC: LED2 LED End Count Register (Address = 04h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	LED2LEDENDC[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
LED2LEDENDC[15:0]											

This register sets the end timing value for when the LED2 signal turns off.

Bits 23:16 **Must be 0**

Bits 15:0 **LED2LEDENDC[15:0]: LED2 end count**

The contents of this register can be used to position the end of the LED2 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

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Figure 8-39. ALED2STC: Sample Ambient LED2 Start Count Register (Address = 05h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	ALED2STC[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
ALED2STC[15:0]											

This register sets the start timing value for the ambient LED2 signal sample.

Bits 23:16 **Must be 0**

Bits 15:0 **ALED2STC[15:0]: Sample ambient LED2 start count**

The contents of this register can be used to position the start of the sample ambient LED2 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 8-40. ALED2ENDC: Sample Ambient LED2 End Count Register (Address = 06h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	ALED2ENDC[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
ALED2ENDC[15:0]											

This register sets the end timing value for the ambient LED2 signal sample.

Bits 23:16 **Must be 0**

Bits 15:0 **ALED2ENDC[15:0]: Sample ambient LED2 end count**

The contents of this register can be used to position the end of the sample ambient LED2 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 8-41. LED1STC: Sample LED1 Start Count Register (Address = 07h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	LED1STC[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
LED1STC[15:0]											

This register sets the start timing value for the LED1 signal sample.

Bits 23:17 **Must be 0**

Bits 16:0 **LED1STC[15:0]: Sample LED1 start count**

The contents of this register can be used to position the start of the sample LED1 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

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Figure 8-42. LED1ENDC: Sample LED1 End Count (Address = 08h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	LED1ENDC[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
LED1ENDC[15:0]											

This register sets the end timing value for the LED1 signal sample.

Bits 23:17 **Must be 0**

Bits 16:0 **LED1ENDC[15:0]: Sample LED1 end count**

The contents of this register can be used to position the end of the sample LED1 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 8-43. LED1LEDSTC: LED1 LED Start Count Register (Address = 09h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	LED1LEDSTC[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
LED1LEDSTC[15:0]											

This register sets the start timing value for when the LED1 signal turns on.

Bits 23:16 **Must be 0**

Bits 15:0 **LED1LEDSTC[15:0]: LED1 start count**

The contents of this register can be used to position the start of the LED1 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 8-44. LED1LEDENDC: LED1 LED End Count Register (Address = 0Ah, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	LED1LEDENDC[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
LED1LEDENDC[15:0]											

This register sets the end timing value for when the LED1 signal turns off.

Bits 23:16 **Must be 0**

Bits 15:0 **LED1LEDENDC[15:0]: LED1 end count**

The contents of this register can be used to position the end of the LED1 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

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Figure 8-45. ALED1STC: Sample Ambient LED1 Start Count Register (Address = 0Bh, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	ALED1STC[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
ALED1STC[15:0]											

This register sets the start timing value for the ambient LED1 signal sample.

Bits 23:16 **Must be 0**

Bits 15:0 **ALED1STC[15:0]: Sample ambient LED1 start count**

The contents of this register can be used to position the start of the sample ambient LED1 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 8-46. ALED1ENDC: Sample Ambient LED1 End Count Register (Address = 0Ch, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	ALED1ENDC[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
ALED1ENDC[15:0]											

This register sets the end timing value for the ambient LED1 signal sample.

Bits 23:16 **Must be 0**

Bits 15:0 **ALED1ENDC[15:0]: Sample ambient LED1 end count**

The contents of this register can be used to position the end of the sample ambient LED1 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 8-47. LED2CONVST: LED2 Convert Start Count Register (Address = 0Dh, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	LED2CONVST[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
LED2CONVST[15:0]											

This register sets the start timing value for the LED2 conversion.

Bits 23:16 **Must be 0**

Bits 15:0 **LED2CONVST[15:0]: LED2 convert start count**

The contents of this register can be used to position the start of the LED2 conversion signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

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Figure 8-48. LED2CONVEND: LED2 Convert End Count Register (Address = 0Eh, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	LED2CONVEND[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
LED2CONVEND[15:0]											

This register sets the end timing value for the LED2 conversion.

Bits 23:16 **Must be 0**

Bits 15:0 **LED2CONVEND[15:0]: LED2 convert end count**

The contents of this register can be used to position the end of the LED2 conversion signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 8-49. ALED2CONVST: LED2 Ambient Convert Start Count Register (Address = 0Fh, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	ALED2CONVST[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
ALED2CONVST[15:0]											

This register sets the start timing value for the ambient LED2 conversion.

Bits 23:16 **Must be 0**

Bits 15:0 **ALED2CONVST[15:0]: LED2 ambient convert start count**

The contents of this register can be used to position the start of the LED2 ambient conversion signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 8-50. ALED2CONVEND: LED2 Ambient Convert End Count Register (Address = 10h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	ALED2CONVEND[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
ALED2CONVEND[15:0]											

This register sets the end timing value for the ambient LED2 conversion.

Bits 23:16 **Must be 0**

Bits 15:0 **ALED2CONVEND[15:0]: LED2 ambient convert end count**

The contents of this register can be used to position the end of the LED2 ambient conversion signal with respect to the PRP. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

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Figure 8-51. LED1CONVST: LED1 Convert Start Count Register (Address = 11h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	LED1CONVST[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
LED1CONVST[15:0]											

This register sets the start timing value for the LED1 conversion.

Bits 23:16 **Must be 0**

Bits 15:0 **LED1CONVST[15:0]: LED1 convert start count**

The contents of this register can be used to position the start of the LED1 conversion signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 8-52. LED1CONVEND: LED1 Convert End Count Register (Address = 12h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	LED1CONVEND[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
LED1CONVEND[15:0]											

This register sets the end timing value for the LED1 conversion.

Bits 23:16 **Must be 0**

Bits 15:0 **LED1CONVEND[15:0]: LED1 convert end count**

The contents of this register can be used to position the end of the LED1 conversion signal with respect to the PRP. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 8-53. ALED1CONVST: LED1 Ambient Convert Start Count Register (Address = 13h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	ALED1CONVST[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
ALED1CONVST[15:0]											

This register sets the start timing value for the ambient LED1 conversion.

Bits 23:16 **Must be 0**

Bits 15:0 **ALED1CONVST[15:0]: LED1 ambient convert start count**

The contents of this register can be used to position the start of the LED1 ambient conversion signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

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Figure 8-54. ALED1CONVEND: LED1 Ambient Convert End Count Register (Address = 14h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	ALED1CONVEND[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
ALED1CONVEND[15:0]											

This register sets the end timing value for the ambient LED1 conversion.

Bits 23:16 **Must be 0**

Bits 15:0 **ALED1CONVEND[15:0]: LED1 ambient convert end count**

The contents of this register can be used to position the end of the LED1 ambient conversion signal with respect to the PRP. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

Figure 8-55. ADCRSTSTCT0: ADC Reset 0 Start Count Register (Address = 15h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	ADCRSTSTCT0[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
ADCRSTSTCT0[15:0]											

This register sets the start position of the ADC0 reset conversion signal.

Bits 23:16 **Must be 0**

Bits 15:0 **ADCRSTSTCT0[15:0]: ADC RESET 0 start count**

The contents of this register can be used to position the start of the ADC reset conversion signal (default value after reset is 0000h). Refer to the *Using the Timer Module* section for details.

Figure 8-56. ADCRSTENDCT0: ADC Reset 0 End Count Register (Address = 16h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	ADCRSTENDCT0[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
ADCRSTENDCT0[15:0]											

This register sets the end position of the ADC0 reset conversion signal.

Bits 23:16 **Must be 0**

Bits 15:0 **ADCRSTENDCT0[15:0]: ADC RESET 0 end count**

The contents of this register can be used to position the end of the ADC reset conversion signal (default value after reset is 0000h). Refer to the *Using the Timer Module* section for details.

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Figure 8-57. ADCRSTSTCT1: ADC Reset 1 Start Count Register (Address = 17h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	ADCRSTSTCT1[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
ADCRSTSTCT1[15:0]											

This register sets the start position of the ADC1 reset conversion signal.

Bits 23:16 **Must be 0**

Bits 15:0 **ADCRSTSTCT1[15:0]: ADC RESET 1 start count**

The contents of this register can be used to position the start of the ADC reset conversion. Refer to the *Using the Timer Module* section for details.

Figure 8-58. ADCRSTENDCT1: ADC Reset 1 End Count Register (Address = 18h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	ADCRSTENDCT1[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
ADCRSTENDCT1[15:0]											

This register sets the end position of the ADC1 reset conversion signal.

Bits 23:16 **Must be 0**

Bits 15:0 **ADCRSTENDCT1[15:0]: ADC RESET 1 end count**

The contents of this register can be used to position the end of the ADC reset conversion. Refer to the *Using the Timer Module* section for details.

Figure 8-59. ADCRSTSTCT2: ADC Reset 2 Start Count Register (Address = 19h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	ADCRSTSTCT2[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
ADCRSTSTCT2[15:0]											

This register sets the start position of the ADC2 reset conversion signal.

Bits 23:16 **Must be 0**

Bits 15:0 **ADCRSTSTCT2[15:0]: ADC RESET 2 start count**

The contents of this register can be used to position the start of the ADC reset conversion. Refer to the *Using the Timer Module* section for details.

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Figure 8-60. ADCRSTENDCT2: ADC Reset 2 End Count Register (Address = 1Ah, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	ADCRSTENDCT2[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
ADCRSTENDCT2[15:0]											

This register sets the end position of the ADC2 reset conversion signal.

Bits 23:16 **Must be 0**

Bits 15:0 **ADCRSTENDCT2[15:0]: ADC RESET 2 end count**

The contents of this register can be used to position the end of the ADC reset conversion. Refer to the *Using the Timer Module* section for details.

Figure 8-61. ADCRSTSTCT3: ADC Reset 3 Start Count Register (Address = 1Bh, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	ADCRSTSTCT3[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
ADCRSTSTCT3[15:0]											

This register sets the start position of the ADC3 reset conversion signal.

Bits 23:16 **Must be 0**

Bits 15:0 **ADCRSTSTCT3[15:0]: ADC RESET 3 start count**

The contents of this register can be used to position the start of the ADC reset conversion. Refer to the *Using the Timer Module* section for details.

Figure 8-62. ADCRSTENDCT3: ADC Reset 3 End Count Register (Address = 1Ch, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	ADCRSTENDCT3[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
ADCRSTENDCT3[15:0]											

This register sets the end position of the ADC3 reset conversion signal.

Bits 23:16 **Must be 0**

Bits 15:0 **ADCRSTENDCT3[15:0]: ADC RESET 3 end count**

The contents of this register can be used to position the end of the ADC reset conversion signal (default value after reset is 0000h). Refer to the *Using the Timer Module* section for details.

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Figure 8-63. PRPCOUNT: Pulse Repetition Period Count Register (Address = 1Dh, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	PRPCOUNT[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
PRPCOUNT[15:0]											

This register sets the device pulse repetition period count.

Bits 23:16 **Must be 0**

Bits 15:0 **PRPCOUNT[15:0]: Pulse repetition period count**

The contents of this register can be used to set the pulse repetition period (in number of clock cycles of the 4-MHz clock). The PRPCOUNT value must be set in the range of 800 to 64000. Values below 800 do not allow sufficient sample time for the four samples; see the *Electrical Characteristics* table.

Figure 8-64. CONTROL1: Control Register 1 (Address = 1Eh, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	0	0	0	0
11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	TIMEREN	NUMAV[7:0]							

This register configures the clock alarm pin and timer.

Bits 23:9 **Must be 0**

Bit 8 **TIMEREN: Timer enable**

0 = Timer module is disabled and all internal clocks are off (default after reset)
1 = Timer module is enabled

Bits 7:0 **NUMAV[7:0]: Number of averages**

Specify an 8-bit value corresponding to the number of ADC samples to be averaged – 1.
For example, to average four ADC samples, set NUMAV[7:0] equal to 3.
The maximum number of averages is 16. Any setting of NUMAV[7:0] greater than or equal to a decimal value of 15 results in the number of averages getting set to 16.

Figure 8-65. SPARE1: SPARE1 Register For Future Use (Address = 1Fh, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	0	0	0	0
11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0

This register is a spare register and is reserved for future use.

Bits 23:0 **Must be 0**

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Figure 8-66. TIAGAIN: Transimpedance Amplifier Gain Setting Register (Address = 20h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	ENSEPGAIN	STAGE2EN1	0	0
11	10	9	8	7	6	5	4	3	2	1	0
0	STG2GAIN1[2:0]			CF_LED1[4:0]					RF_LED1[2:0]		

This register sets the device transimpedance amplifier gain mode and feedback resistor and capacitor values.

Bits 23:16 **Must be 0**

Bit 15 **ENSEPGAIN: Enable separate gain mode**

0 = The R_F, C_F values and stage 2 gain settings are the same for both the LED2 and LED1 signals; the values are specified by the bits (RF_LED2, CF_LED2, STAGE2EN2, STG2GAIN2) in the TIA_AMB_GAIN register (default after reset)
1 = The R_F, C_F values and stage 2 gain settings can be independently set for the LED2 and LED1 signals. The values for LED1 are specified using the bits (RF_LED1, CF_LED1, STAGE2EN1, STG2GAIN1) in the TIAGAIN register, whereas the values for LED2 are specified using the corresponding bits in the TIA_AMB_GAIN register.

Bit 14 **STAGE2EN1: Enable stage 2 for LED 1**

0 = Stage 2 is bypassed (default after reset)
1 = Stage 2 is enabled with the gain value specified by the STG2GAIN1[2:0] bits

Bits 13:11 **Must be 0**

Bits 10:8 **STG2GAIN1[2:0]: Program stage 2 gain for LED1**

000 = 0 dB, or linear gain of 1 (default after reset)
001 = 3.5 dB, or linear gain of 1.5
010 = 6 dB, or linear gain of 2
011 = 9.5 dB, or linear gain of 3
100 = 12 dB, or linear gain of 4
101 = Do not use
110 = Do not use
111 = Do not use

Bits 7:3 **CF_LED1[4:0]: Program C_F for LED1**

00000 = 5 pF (default after reset)
00001 = 5 pF + 5 pF
00010 = 15 pF + 5 pF
00100 = 25 pF + 5 pF
01000 = 50 pF + 5 pF
10000 = 150 pF + 5 pF

Note that any combination of these C_F settings is also supported by setting multiple bits to 1. For example, to obtain C_F = 100 pF, set bits 7:3 = 01111.

Bits 2:0 **RF_LED1[2:0]: Program R_F for LED1**

000 = 500 kΩ (default after reset)
001 = 250 kΩ
010 = 100 kΩ
011 = 50 kΩ
100 = 25 kΩ
101 = 10 kΩ
110 = 1 MΩ
111 = None

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Figure 8-67. TIA_AMB_GAIN: Transimpedance Amplifier and Ambient Cancellation Stage Gain Register (Address = 21h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	AMBDAC[3:0]				FLTR CNRSEL	STAGE2EN2	0	0
11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	STG2GAIN[2:0]			CF_LED2[4:0]					RF_LED2[2:0]		

This register configures the ambient light cancellation amplifier gain, cancellation current, and filter corner frequency.

Bits 23:20 **Must be 0**

Bits 19:16 **AMBDAC[3:0]: Ambient DAC value**

These bits set the value of the cancellation current.

0000 = 0 µA (default after reset)
0001 = 1 µA
0010 = 2 µA
0011 = 3 µA
0100 = 4 µA
0101 = 5 µA
0110 = 6 µA
0111 = 7 µA
1000 = 8 µA
1001 = 9 µA
1010 = 10 µA
1011 = Do not use
1100 = Do not use
1101 = Do not use
1110 = Do not use
1111 = Do not use

Bit 15 **Must be 0**

Bit 14 **STAGE2EN2: Stage 2 enable for LED 2**

0 = Stage 2 is bypassed (default after reset)
1 = Stage 2 is enabled with the gain value specified by the STG2GAIN2[2:0] bits

Bits 13:11 **Must be 0**

Bits 10:8 **STG2GAIN2[2:0]: Stage 2 gain setting for LED 2**

000 = 0 dB, or linear gain of 1 (default after reset)
001 = 3.5 dB, or linear gain of 1.5
010 = 6 dB, or linear gain of 2
011 = 9.5 dB, or linear gain of 3
100 = 12 dB, or linear gain of 4
101 = Do not use
110 = Do not use
111 = Do not use

Bits 7:3 **CF_LED[4:0]: Program C_F for LEDs**

00000 = 5 pF (default after reset)
00001 = 5 pF + 5 pF
00010 = 15 pF + 5 pF
00100 = 25 pF + 5 pF
01000 = 50 pF + 5 pF
10000 = 150 pF + 5 pF

Note that any combination of these C_F settings is also supported by setting multiple bits to 1. For example, to obtain C_F = 100 pF, set D[7:3] = 01111.

Bits 2:0 **RF_LED[2:0]: Program R_F for LEDs**

000 = 500 kΩ
001 = 250 kΩ
010 = 100 kΩ
011 = 50 kΩ
100 = 25 kΩ
101 = 10 kΩ
110 = 1 MΩ
111 = None

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Figure 8-68. LEDCNTRL: LED Control Register (Address = 22h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	LED_RANGE[1:0]		LED1[7:0]			
11	10	9	8	7	6	5	4	3	2	1	0
LED1[7:0]				LED2[7:0]							

This register sets the LED current range and the LED1 and LED2 drive current.

Bits 23:18 **Must be 0**

Bits 17:16 **LED_RANGE[1:0]: LED range**

These bits program the full-scale LED current range for Tx. Table 8-9 details the settings.

Bits 15:8 **LED1[7:0]: Program LED current for LED1 signal**

Use these register bits to specify the LED current setting for LED1 (default after reset is 00h).
The nominal value of the LED current is given by Equation 7, where the full-scale LED current is either 0 mA or 50 mA (as specified by the LED_RANGE[1:0] register bits).

Bits 7:0 **LED2[7:0]: Program LED current for LED2 signal**

Use these register bits to specify the LED current setting for LED2 (default after reset is 00h).
The nominal value of LED current is given by Equation 8, where the full-scale LED current is either 0 mA or 50 mA (as specified by the LED_RANGE[1:0] register bits).

Table 8-9. Full-Scale LED Current across Tx Reference Voltage Settings(1)

LED_RANGE[1:0]	TX_REF = 0.25 V		TX_REF = 0.5 V		TX_REF = 0.75 V		TX_REF = 1.0 V	
	I_{MAX}	V_{HR} (2)	I_{MAX}	V_{HR}	I_{MAX}	V_{HR}	I_{MAX}	V_{HR}
00 (default after reset)	50 mA	0.75 V	100 mA	1.1 V	Do not use	—	Do not use	—
01	25 mA	0.7 V	50 mA	1.0 V	75 mA	1.3 V	100 mA	1.6 V
10	50 mA	0.75 V	100 mA	1.1 V	Do not use	—	Do not use	—
11	Tx is off	—	Tx is off	—	Tx is off	—	Tx is off	—

(1) For a 3-V to 3.6-V supply, use TX_REF = 0.25 or 0.5 V. For a 4.75-V to 5.25-V supply, use TX_REF = 0.75 V or 1.0 V.

(2) V_{HR} refers to the headroom voltage (over and above the LED forward voltage and cable voltage drop) needed on the LED_DRV_SUP. The V_{HR} values specified are for the H-bridge configuration. In the common anode configuration, V_{HR} can be lower by 0.25 V.

$$\frac{\text{LED1[7:0]}}{256} \times \text{Full-Scale Current} \quad (7)$$

$$\frac{\text{LED2[7:0]}}{256} \times \text{Full-Scale Current} \quad (8)$$

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Figure 8-69. CONTROL2: Control Register 2 (Address = 23h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	DYNAMIC 1	0	TX_REF1	TX_REF0	0	0	DYNAMIC 2	0	0
11	10	9	8	7	6	5	4	3	2	1	0
TXBRG MOD	DIGOUT_ TRI STATE	XTAL DIS	EN_ SLOW_ DIAG	0	0	0	DYNAMIC 3	DYNAMIC 4	PDNTX	PDNRX	PDNAFE

This register controls the LED transmitter, crystal, and the AFE, transmitter, and receiver power modes.

Bits 23:21 **Must be 0**

Bit 20 **DYNAMIC1**

0 = Transmitter is not powered down during dynamic power-down phase
1 = Transmitter is powered down during dynamic power-down phase

Bit 19 **Must be 0**

Bits 18:17 **TX_REF[1:0]: Tx reference voltage**

These bits set the transmitter reference voltage. This Tx reference voltage is available on the device TX_REF pin.

00 = 0.25-V Tx reference voltage (default value after reset)
01 = 0.5-V Tx reference voltage
10 = 1.0-V Tx reference voltage
11 = 0.75-V Tx reference voltage, D3

Bits 16:15 **Must be 0**

Bit 14 **DYNAMIC2**

0 = Part of the ADC is not powered down during dynamic power-down phase
1 = Part of the ADC is powered down during dynamic power-down phase

Bit 11 **TXBRGMOD: Tx bridge mode**

0 = LED driver is configured as an H-bridge (default after reset)
1 = LED driver is configured as a push-pull

Bit 10 **DIGOUT_TRISTATE: Tri-state bit for the ADC_RDY and DIAG_END pins**

0 = ADC_RDY and DIAG_END are not tri-stated
1 = ADC_RDY and DIAG_END are tri-stated

Bit 9 **XTALDIS: Crystal disable mode**

0 = The crystal module is enabled; the 8-MHz crystal must be connected to the XIN and XOUT pins
1 = The crystal module is disabled; an external 8-MHz clock must be applied to the XIN pin

Bit 8 **EN_SLOW_DIAG: Fast diagnostics mode enable**

0 = Fast diagnostics mode, 8 ms (default value after reset)
1 = Slow diagnostics mode, 16 ms

Bits 7:5 **Must be 0**

Bit 4 **DYNAMIC3**

0 = TIA is not powered down during dynamic power-down phase
1 = TIA is powered down during dynamic power-down phase

Bit 3 **DYNAMIC4**

0 = The rest of the ADC is not powered down during dynamic power-down phase
1 = The rest of the ADC is powered down during dynamic power-down phase

Bit 2 **PDN_TX: Tx power-down**

0 = The Tx is powered up (default after reset)
1 = Only the Tx module is powered down

Bit 1 **PDN_RX: Rx power-down**

0 = The Rx is powered up (default after reset)
1 = Only the Rx module is powered down

Bit 0 **PDN_AFE: AFE power-down**

0 = The AFE is powered up (default after reset)
1 = The entire AFE is powered down (including the Tx, Rx, and diagnostics blocks)

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Figure 8-70. SPARE2: SPARE2 Register For Future Use (Address = 24h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	0	0	0	0
11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0

This register is a spare register and is reserved for future use.

Bits 23:0 **Must be 0**

Figure 8-71. SPARE3: SPARE3 Register For Future Use (Address = 25h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	0	0	0	0
11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0

This register is a spare register and is reserved for future use.

Bits 23:0 **Must be 0**

Figure 8-72. SPARE4: SPARE4 Register For Future Use (Address = 26h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	0	0	0	0
11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0

This register is a spare register and is reserved for future use.

Bits 23:0 **Must be 0**

Figure 8-73. RESERVED1: RESERVED1 Register For Factory Use Only (Address = 27h, Reset Value = XXXXh)

23	22	21	20	19	18	17	16	15	14	13	12
X(1)	X	X	X	X	X	X	X	X	X	X	X
11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	X	X	X	X

(1) X = don't care.

This register is reserved for factory use. Readback values vary between devices.

Figure 8-74. RESERVED2: RESERVED2 Register For Factory Use Only (Address = 28h, Reset Value = XXXXh)

23	22	21	20	19	18	17	16	15	14	13	12
X(1)	X	X	X	X	X	X	X	X	X	X	X
11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	X	X	X	X

This register is reserved for factory use. Readback values vary between devices.

Figure 8-75. ALARM: Alarm Register (Address = 29h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	0	0	0	0
11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0

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This register controls the alarm pin functionality.

Bits 23:0 **Must be 0**

Figure 8-76. LED2VAL: LED2 Digital Sample Value Register (Address = 2Ah, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
LED2VAL[23:0]											
11	10	9	8	7	6	5	4	3	2	1	0
LED2VAL[23:0]											

Bits 23:0 **LED2VAL[23:0]: LED2 digital value**

This register contains the digital value of the latest LED2 sample converted by the ADC.

Figure 8-77. ALED2VAL: Ambient LED2 Digital Sample Value Register (Address = 2Bh, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
ALED2VAL[23:0]											
11	10	9	8	7	6	5	4	3	2	1	0
ALED2VAL[23:0]											

Bits 23:0 **ALED2VAL[23:0]: LED2 ambient digital value**

This register contains the digital value of the latest LED2 ambient sample converted by the ADC.

Figure 8-78. LED1VAL: LED1 Digital Sample Value Register (Address = 2Ch, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
LED1VAL[23:0]											
11	10	9	8	7	6	5	4	3	2	1	0
LED1VAL[23:0]											

Bits 23:0 **LED1VAL[23:0]: LED1 digital value**

This register contains the digital value of the latest LED1 sample converted by the ADC.

Figure 8-79. ALED1VAL: Ambient LED1 Digital Sample Value Register (Address = 2Dh, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
ALED1VAL[23:0]											
11	10	9	8	7	6	5	4	3	2	1	0
ALED1VAL[23:0]											

Bits 23:0 **ALED1VAL[23:0]: LED1 ambient digital value**

This register contains the digital value of the latest LED1 ambient sample converted by the ADC.

Figure 8-80. LED2-ALED2VAL: LED2-Ambient LED2 Digital Sample Value Register (Address = 2Eh, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
LED2-ALED2VAL[23:0]											
11	10	9	8	7	6	5	4	3	2	1	0
LED2-ALED2VAL[23:0]											

Bits 23:0 **LED2-ALED2VAL[23:0]: (LED2 – LED2 ambient) digital value**

This register contains the digital value of the LED2 sample after the LED2 ambient is subtracted.
Note that this value is inverted when compared to waveforms shown in many publications.

Figure 8-81. LED1-ALED1VAL: LED1-Ambient LED1 Digital Sample Value Register (Address = 2Fh, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12

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Figure 8-81. LED1-ALED1VAL: LED1-Ambient LED1 Digital Sample Value Register (Address = 2Fh, Reset Value = 0000h) (continued)

LED1-ALED1VAL[23:0]											
11	10	9	8	7	6	5	4	3	2	1	0
LED1-ALED1VAL[23:0]											

Bits 23:0 **LED1-ALED1VAL[23:0]: (LED1 – LED1 ambient) digital value**

This register contains the digital value of the LED1 sample after the LED1 ambient is subtracted from it. Note that this value is inverted when compared to waveforms shown in many publications.

Figure 8-82. DIAG: Diagnostics Flag Register (Address = 30h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	0	0	0	PD_ALM
11	10	9	8	7	6	5	4	3	2	1	0
LED_ ALM	LED2 OPEN	LED1 OPEN	LEDSC	OUTNSH GND	OUTPSH GND	PDOC	PDSC	INNSC GND	INPSC GND	INNSC LED	INPSC LED

This register is read only. This register contains the status of all diagnostic flags at the end of the diagnostics sequence. The end of the diagnostics sequence is indicated by the signal going high on DIAG_END pin.

Bits 23:13 **Read only**

Bit 12 **PD_ALM: Power-down alarm status diagnostic flag**

This bit indicates the status of PD_ALM .
0 = No fault (default after reset)
1 = Fault present

Bit 11 **LED_ALM: LED alarm status diagnostic flag**

This bit indicates the status of LED_ALM .
0 = No fault (default after reset)
1 = Fault present

Bit 10 **LED2OPEN: LED2 open diagnostic flag**

This bit indicates that LED2 is open.
0 = No fault (default after reset)
1 = Fault present

Bit 9 **LED1OPEN: LED1 open diagnostic flag**

This bit indicates that LED1 is open.
0 = No fault (default after reset)
1 = Fault present

This bit indicates that LED2 is open.
0 = No fault (default after reset)
1 = Fault present

Bit 8 **LEDSC: LED short diagnostic flag**

This bit indicates an LED short.
0 = No fault (default after reset)
1 = Fault present

Bit 7 **OUTNSHGND: OUTN to GND diagnostic flag**

This bit indicates that OUTN is shorted to the GND cable.
0 = No fault (default after reset)
1 = Fault present

Bit 6 **OUTPSHGND: OUTP to GND diagnostic flag**

This bit indicates that OUTP is shorted to the GND cable.
0 = No fault (default after reset)
1 = Fault present

Bit 5 **PDOC: PD open diagnostic flag**

This bit indicates that PD is open.
0 = No fault (default after reset)
1 = Fault present

Bit 4 **PDSC: PD short diagnostic flag**

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This bit indicates a PD short.
0 = No fault (default after reset)
1 = Fault present

Bit 3 **INNSCGND: INN to GND diagnostic flag**

This bit indicates a short from the INN pin to the GND cable.
0 = No fault (default after reset)
1 = Fault present

Bit 2 **INPSCGND: INP to GND diagnostic flag**

This bit indicates a short from the INP pin to the GND cable.
0 = No fault (default after reset)
1 = Fault present

Bit 1 **INNSCLED: INN to LED diagnostic flag**

This bit indicates a short from the INN pin to the LED cable.
0 = No fault (default after reset)
1 = Fault present

Bit 0 **INPSCLED: INP to LED diagnostic flag**

This bit indicates a short from the INP pin to the LED cable.
0 = No fault (default after reset)
1 = Fault present

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Figure 8-83. CONTROL3: Control Register (Address = 31h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	TX3_MODE	0	0	0
11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	SOMI_TRI	CLKOUT_TRI	CLKDIV[2:0]		

This register controls the clock divider ratio.

Bits 23:16 **Must be 0**

Bit 15 **TX3_MODE: Selection of third LED**

This bit transitions the control from the default two LEDs (on TXP, TXN) to the third LED on TX3.
0 = LEDs on TXP, TXN are active
1 = LED on TX3 is active. Timing engine controls on TXP are transferred to TX3. Maximum current setting supported for the third LED is 50 mA.

Bits 14:5 **Must be 0**

Bit 4 **SOMI_TRI: Serial data output 3-state mode**

This bit determines the state of the SPISOMI output pin. In order to avoid loading the SPI bus when multiple devices are connected, this bit must be set to 1 (3-state mode) whenever the device SPI is inactive.

0 = SPISOMI output buffer is active (normal operation, default)
1 = SPISOMI output buffer is in 3-state mode

Bit 3 **CLKOUT_TRI: CLKOUT output 3-state mode**

This bit determines the state of the CLKOUT output pin.

0 = CLKOUT buffer is active (normal operation, default)
1 = CLKOUT buffer is in 3-state mode

Bits 2:0 **CLKDIV[2:0]: Clock divider ratio**

These bits set the ratio of the clock divider and determine the frequency of CLKOUT relative to the input clock frequency.

Table 8-10 shows the clock divider ratio settings.

Table 8-10. Clock Divider Ratio Settings

CLKDIV[2:0]	DIVIDER RATIO	INPUT CLOCK FREQUENCY RANGE
000	Divide-by-2	8 MHz to 12 MHz(2)
001	Do not use	Do not use
010	Divide-by-4	16 MHz to 24 MHz(2)
011	Divide-by-6	24 MHz to 36 MHz
100	Divide-by-8	32 MHz to 48 MHz
101	Divide-by-12	48 MHz to 60 MHz
110	Do not use	Do not use
111	Divide by 1(1)	4 MHz to 6 MHz

(1) When using divide-by-1, the external clock should have a duty cycle between 48% to 52%.
(2) These frequency ranges can be used when generating the clock using the crystal.

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Figure 8-84. PDNCYCLESTC: PDNCYCLESTC Register (Address = 32h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	PDNCYCLESTC[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
PDNCYCLESTC[15:0]											

Bits 23:16 **Must be 0**

Bits 15:0 **PDNCYCLESTC[15:0]: Dynamic (cycle-to-cycle) power-down start count**

The contents of this register can be used to position the start of the PDN_CYCLE signal with respect to the pulse repetition period (PRP). The count is specified as the number of cycles of CLKOUT. If the dynamic power-down feature is not required, then do not program this register.

Figure 8-85. PDNCYCLEENDC: PDNCYCLEENDC Register (Address = 33h, Reset Value = 0000h)

23	22	21	20	19	18	17	16	15	14	13	12
0	0	0	0	0	0	0	0	PDNCYCLEENDC[15:0]			
11	10	9	8	7	6	5	4	3	2	1	0
PDNCYCLEENDC[15:0]											

Bits 23:16 **Must be 0**

Bits 15:0 **PDNCYCLEENDC[15:0]: Dynamic (cycle-to-cycle) power-down end count**

The contents of this register can be used to position the end of the PDN_CYCLE signal with respect to the pulse repetition period (PRP). The count is specified as the number of cycles of CLKOUT. If the dynamic power-down feature is not required, then do not program this register.

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9 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The AFE4403 is ideally suited as an analog front-end for processing PPG (photoplethysmography) signals. The information contained in PPG signals can be used for measuring SPO2 as well as for monitoring heart rate. The high dynamic range of the device enables measuring SPO2 with a high degree of accuracy, even under conditions of low perfusion (ac:dc ratio). An SPO2 measurement system involves two different wavelength LEDs: usually Red and IR. By computing the ratio of the ac:dc at the two different wavelengths, SPO2 can be calculated. Heart rate monitoring systems can also benefit from the high dynamic range of the AFE4403, which enables a high-fidelity pulsating signal to be captured, even in cases where the signal strength is low.

9.2 Typical Application

Device connections in a typical application is shown in Figure 9-1. The schematic shows a cabled application in which the LEDs and photodiode are connected to the device through a cable. However, in an application without cables, the LEDs and photodiode can be directly connected to the TXP, TXN, TX3, INP, and INN pins directly.

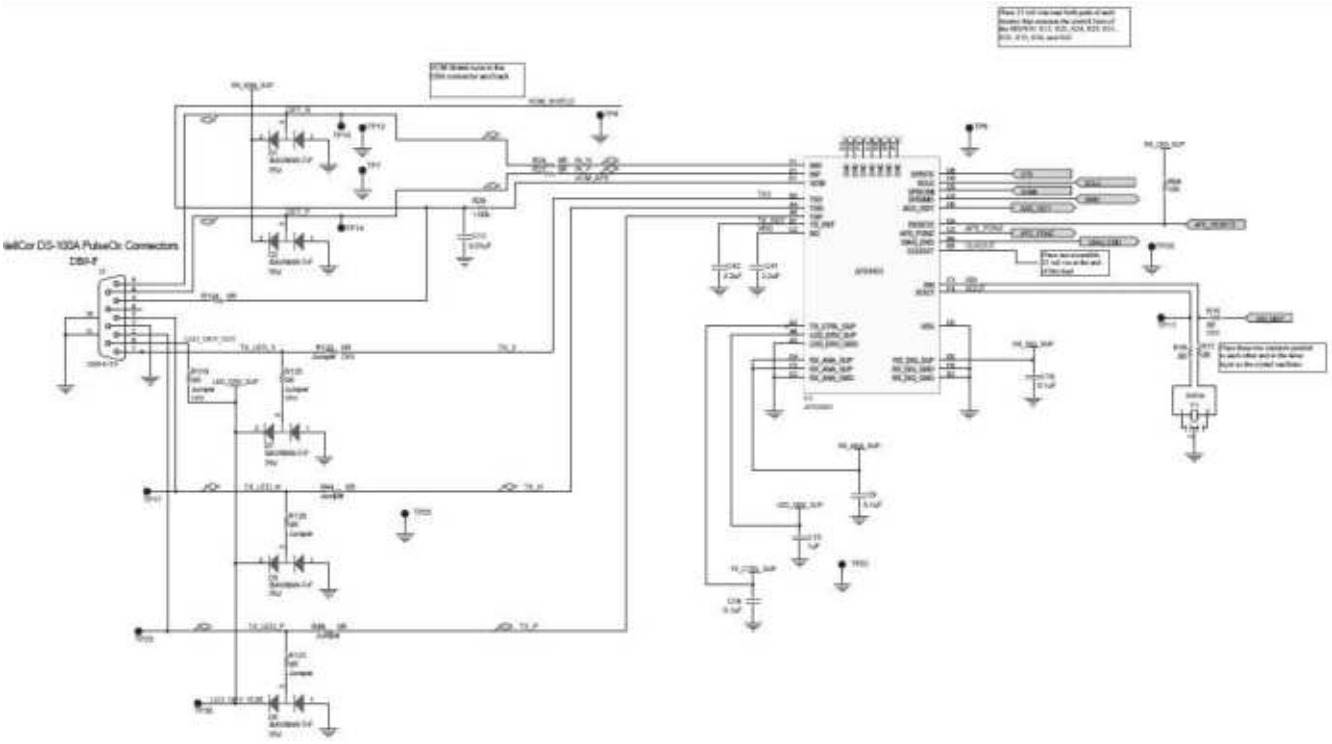


Figure 9-1. Schematic

9.2.1 Design Requirements

An SPO2 application usually involves a Red LED and IR LED. In addition, a heart rate monitoring application can use a different wavelength LED, such as a Green LED. The LEDs can be connected either in the common anode configuration or H-bridge configuration to the TXP, TXN pins. The LED connected to the TX3 pin can only be connected in the common anode configuration.

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9.2.2 Detailed Design Procedure

Refer to LED Configurations for different ways to connect the LEDs to the TXP, TXN, and TX3 pins. The photodiode (shown in Figure 9-2) receives light from both the Red and IR phases and usually has good sensitivities at both these wavelengths.



Figure 9-2. Photodiode

The photodiode connected as shown in Figure 9-2 operates in zero bias because of the negative feedback from the transimpedance amplifier. The signal current generated by the photodiode is converted into a voltage by the transimpedance amplifier, which has a programmable transimpedance gain. The rest of the signal chain then presents a voltage to the ADC. The full-scale output of the transimpedance amplifier is ±1 V and the full-scale input to the ADC is ±1.2 V. An automatic gain control (AGC) loop can be used to set the target dc voltage at the ADC input to approximately 50% of its full-scale. Such an AGC loop can control a combination of the LED current and TIA gain to achieve this target value.

9.2.3 Application Curves

This section outlines the trends seen in the *Typical Characteristics* curves from an application perspective.

Figure 7-5 illustrates the receiver currents in external clock mode with CLKOUT tri-stated. The curve in Figure 7-5 are taken without the dynamic power-down feature enabled, so much lower currents can be achieved using the dynamic power-down feature. Enabling the crystal mode or removing the CLKOUT tri-state increases the receiver currents from the values depicted in the curve.

Figure 7-6 illustrates the transmitter currents with a zero LED current setting. The average LED current can be computed based on the value of the PRF and LED pulse durations, and can be added to the LED_DRV_SUP current described in Figure 7-6.

Figure 7-7 illustrates the total receiver current (analog plus digital supply) for different clock divider ratios. For each clock divider ratio, the external clock frequency is swept in frequency such that the divided clock changes between 3 MHz to 7 MHz. Note however that the supported range for the divided clock is 4 MHz to 6 MHz at each division ratio. Also, the external clock should be limited to be between 4 MHz to 60 MHz.

Figure 7-8 illustrates the power savings arising out of the dynamic power-down mode. This mode can be set by defining the start and end points for the signal PDN_CYCLE within the pulse repetition period. In Figure 7-8, the LED pulse durations are chosen to be 100 µs and the conversions are also chosen to be 100 µs wide. Thus, the entire active period fits in 500 µs. With the timing margins for t_1 and t_2 indicated in Figure 8-30, the PDN_CYCLE pulse spans the rest of the pulse repetition period. As PRF reduces, the duty cycle of the PDN_CYCLE pulse (as a fraction of the pulse repetition period) increases, which is the reason for the power reduction at lower PRFs as seen in Figure 7-8.

Figure 7-9 illustrates the power savings as a function of the PDN_CYCLE duration at a fixed PRF of 100 Hz. A 100-Hz PRF corresponds to a period of 10 ms. Figure 7-9 indicates the PDN_CYCLE duration swept from 0 ms to 9 ms. With higher durations of PDN_CYCLE, the receiver power reduces.

Figure 7-10 illustrates the baseband response of the switched RC filter for a 5% and 25% duty cycle. When the duty cycle reduces, the effective bandwidth of the filter reduces.

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Figure 9-3 shows the SNR of the signal chain as a function of the output voltage level. The data are taken by looping back the transmitter outputs to the receiver inputs using an external op amp that converts the transmitter voltage to a receiver input current. The loopback op amp and external resistors are an extra source of noise in this measurement, so the actual noise levels are higher than the total noise of the transmitter plus the receiver. The SNR in this curve (and other curves) is expressed in terms of dBFS, where the full-scale of the channel is used as the reference level. Because the valid operating range of the signal chain is ±1 V, a full-scale of 2 V is used for converting the output noise to a dBFS number. %FS refers to the percentage of the output level as a function of the positive full-scale. For example, a 50 %FS curve corresponds to the case where the output level is 0.5 V. Also, the total noise in this curve is the total integrated noise in the digital output. All noise is contained in the Nyquist band, which extends from –PRF / 2 to PRF / 2.

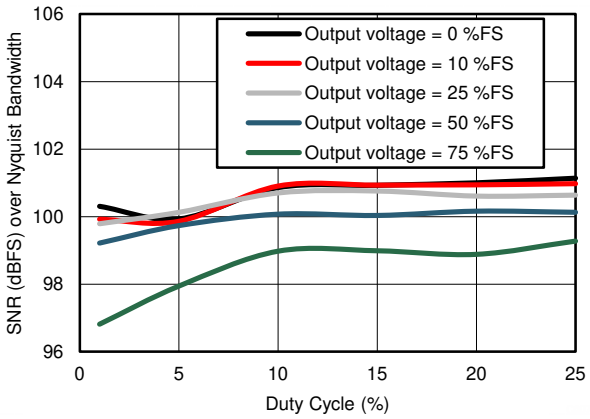


Figure 9-3. SNR over Nyquist Bandwidth vs Duty Cycle (Input Current with Tx-Rx Loopback)

Figure 9-4 is a representation of the same data as Figure 7-10. However, the noise is represented in terms of the input-referred noise current in pArms. By multiplying this number with the TIA gain setting (500 k in this case), the output noise voltage can be computed.

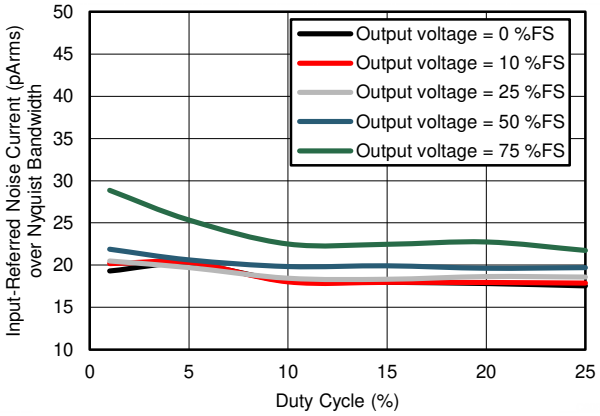


Figure 9-4. Input-Referred Noise Current over Nyquist Bandwidth vs Duty Cycle (Input Current with Tx-Rx Loopback)

Figure 7-13 illustrates the SNR from the receiver as a function of the sampling duty cycle (which is the sampling pulse duration referred to the pulse repetition period) for different settings of TIA gain. This curve is taken at 100-Hz PRF. The maximum duty cycle is limited to 25%. A lower sampling duty cycle also means a lower LED pulse duration duty cycle, which results in power saving.

Figure 7-14 illustrates the input-referred noise corresponding to Figure 7-13. Figure 7-15 and Figure 7-16 illustrate the SNR and input-referred noise current in a 0.1-Hz to 20-Hz band for the LED-ambient data. By performing a digital ambient subtraction, the low-frequency noise in the signal chain can be significantly attenuated. The noise levels in the bandwidth of interest are lower than the noise over the full Nyquist bandwidth. For a PPG signal, the signal band of interest is usually less than 10 Hz. By performing some digital low-pass

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filtering in the processor, this noise reduction can be achieved. Figure 7-17 and Figure 7-18 illustrate the noise reduction from ADC averaging. TI therefore recommends setting the number of ADC averages to the maximum allowed at a given PRF. Figure 7-19 and Figure 7-20 illustrate the noise at different PRFs over a 20-Hz bandwidth. At a higher PRF, the 20-Hz noise band is a smaller fraction of the Nyquist band. Thus, noise is lower at higher PRFs in these figures. Figure 7-21 and Figure 7-22 illustrate the noise at different PRFs over a 20-Hz bandwidth with dynamic power-down mode enabled. The active window remains as 500 µs and all samples and conversions are performed at this time. For the rest of the period, the device is in dynamic power-down with the t_1 and t_2 values as described in Figure 8-30. Again, the noise reduces with higher PRF. Figure 7-23 and Figure 7-24 illustrate the noise as a function of the PDN_CYCLE duration varied from 0 ms to 9 ms, with the active duration (available for conversion) occupying the rest of the period. With higher PDN_CYCLE durations, the number of allowed ADC averages reduces, ehich explains the slight increase in noise at higher PDN_CYCLE durations. Figure 7-25 and Figure 7-26 illustrate the noise as a function of temperature over a 20-Hz bandwidth. The measurements are performed with a transmit-receive loopback as explained earlier. The input current is maintained at 1 µA. Thus, for 250-k gain setting, the output voltage is 0.5 V and for a 500-k gain setting, the output voltage is 1 V. Figure 7-27 and Figure 7-28 illustrate the noise reduction using additional gain in stage 2. Figure 7-29 shows the noise as a function of the internal (divided) clock frequency. The external clock is varied from 7 MHz to 14 MHz with a clock division ratio of 2. This range of external clock results in the internal clock varying from 3.5 MHz to 7 MHz. Out of this range, 4 MHz to 6 MHz is the allowed range for the internal (divided) clock at all clock division ratios. Figure 7-30 illustrates the deviation in the measured LED current with respect to the calculated current when the LED current code is swept from 0 to 255 in steps of 1.

Figure 7-31 and Figure 7-32 illustrate the transmitter+receiver noise (in external loopback mode) as a function of the TX_REF voltage setting. At lower TX_REF voltages, there is a slight increase in the transmitter noise. This increase is not very apparent from the curves because the transmitter noise is at a level much lower than the total noise. Figure 7-33 illustrates the transmitter current as a function of the current setting code. Figure 7-34 illustrates the spread of the transmitter current taken across a large number of devices for the same current setting. Figure 7-35 illustrates how the LED current changes linearly with the TX_REF voltage for a fixed code.

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10 Power Supply Recommendations

The AFE4403 has two sets of supplies: the receiver supplies (RX_ANA_SUP, RX_DIG_SUP) and the transmitter supplies (TX_CTRL_SUP, LED_DRV_SUP). The receiver supplies can be between 2.0 V to 3.6 V, whereas the transmitter supplies can be between 3.0 V to 5.25 V. Another consideration that determines the minimum allowed value of the transmitter supplies is the forward voltage of the LEDs being driven. The current source and switches inside the AFE require voltage headroom that mandates the transmitter supply to be a few hundred millivolts higher than the LED forward voltage. TX_REF is the voltage that governs the generation of the LED current from the internal reference voltage. Choosing the lowest allowed TX_REF setting reduces the additional headroom required but results in higher transmitter noise. Other than for the highest-end clinical SPO2 applications, this extra noise resulting from a lower TX_REF setting can be acceptable.

Consider a design where the LEDs are meant to be used in common anode configuration with a current setting of 50 mA. Assume that the LED manufacturer mentions the highest forward voltage of the LEDs is 2.5 V at this current setting. Further, assume that the TX_REF voltage is set to 0.5 V. The voltage headroom required in this case is 1 V. Thus, the LED_DRV_SUP must be driven with a voltage level greater than or equal to 3.5 V (2.5 V plus 1 V).

LED_DRV_SUP and TX_CTRL_SUP are recommended to be tied together to the same supply (between 3.0 V to 5.25 V). The external supply (connected to the common anode of the two LEDs) must be high enough to account for the forward drop of the LEDs as well as the voltage headroom required by the current source and switches inside the AFE. In most cases, this voltage is expected to fall below 5.25 V; thus the external supply can be the same as LED_DRV_SUP. However, there may be cases (for instance when two LEDs are connected in series) where the voltage required on the external supply is higher than 5.25 V. Such a case must be handled with care to ensure that the voltage on the TXP and TXN pins remains less than 5.25 V and never exceeds the supply voltage of LED_DRV_SUP, TX_CTRL_SUP by more than 0.3 V.

Many scenarios of power management are possible.

Case 1: The LED forward voltage is such that a voltage of 3.3 V is acceptable on LED_DRV_SUP. In this case, a single 3.3-V supply can be used to drive all four pins (RX_ANA_SUP, RX_DIG_SUP, TX_CTRL_SUP, LED_DRV_SUP). Care should be taken to provide some isolation between the transmit and receive supplies because LED_DRV_SUP carries the high-switching current from the LEDs.

Case 2: A low-voltage supply of 2.2 V is available in the system. In this case, a boost converter can be used to derive the voltage for LED_DRV_SUP, as shown in Figure 10-1.

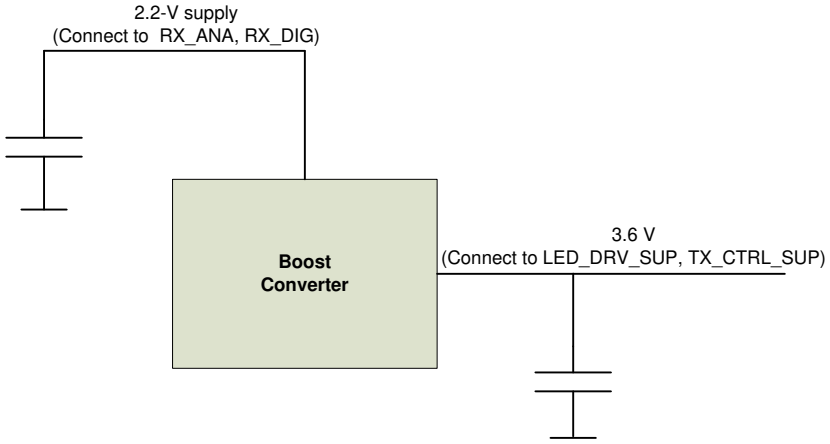


Figure 10-1. Boost Converter

The boost converter requires a clock (usually in the megahertz range) and there is usually a ripple at the boost converter output at this switching frequency. While this frequency is much higher than the signal frequency of interest (which is at maximum a few tens of hertz around dc), a small fraction of this switching noise can possibly alias to the low-frequency band. Therefore, TI strongly recommends that the switching frequency of the boost

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converter be offset from every multiple of the PRF by at least 20 Hz. This offset can be ensured by choosing the appropriate PRF.

Case 3: In cases where a high-voltage supply is available in the system, a buck converter or an LDO can be used to derive the voltage levels required to drive RX_ANA and RX_DIG, as shown in Figure 10-2.

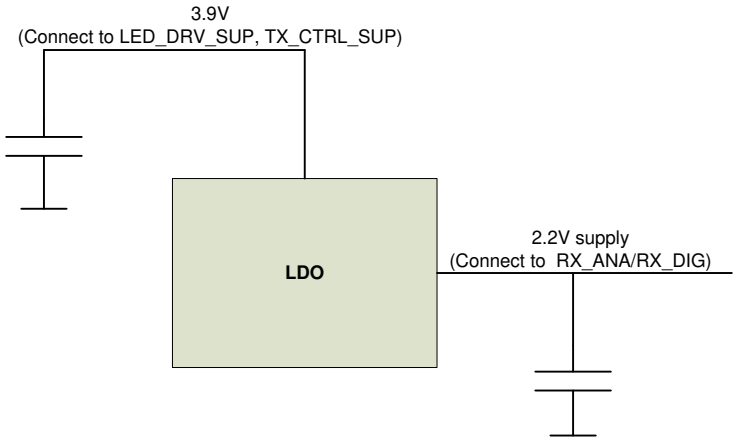


Figure 10-2. Buck Converter or an LDO

10.1 Power Consumption Considerations

The lowest power consumption mode of the AFE4403 corresponds to the following settings:

- PRF = 62.5 Hz,
- External clock mode (XTALDIS = 1), and
- CLKOUT tri-stated (CLKOUT_TRI = 1).

With the above settings, the currents taken from the supplies are as shown in Table 10-1. The LED driver current is with zero LED current setting.

Table 10-1. Current Consumption in Normal Mode

SUPPLY	VOLTAGE (V)	CURRENT (µA)
RX_ANA	2	490
RX_DIG	2	155
TX_CTRL_SUP	3	15
LED_DRV_SUP	3	55

Enabling the crystal (XTALDIS = 0) leads to an additional power consumption that can be estimated to be approximately equal to $(2 \times C_{sh} + 0.5 \times C1 + 0.5 \times C2) \times 0.4 \times f_{XTAL}$, where C_{sh} is the effective shunt capacitance of the crystal, C1 and C2 are the capacitances from the XIN and XOUT pins to ground, and f_{XTAL} is the frequency of the crystal.

Removing the CLKOUT tri-state leads to an additional power consumption of approximately $C_{LOAD} \times V_{SUP} \times f$, where V_{SUP} is the supply voltage of RX_DIG in volts, f = 4 MHz, C_{LOAD} = the capacitive load on the CLKOUT pin + 2 pF.

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The power consumption can be reduced significantly by using the dynamic power-down mode. An illustration of this mode is shown in Table 10-2, where:

- PRF = 62.5 Hz,
- Dynamic power-down is active for 14.7 ms every pulse repetition period,
- All four bits (DYNAMIC[4:1]) are set to 1,
- External clock mode (XTALDIS = 1), and
- CLKOUT is tri-stated (CLKOUT_TRI = 1).

Table 10-2. Current Consumption in Dynamic Power-Down Mode

SUPPLY	VOLTAGE (V)	CURRENT (µA)
RX_ANA	2	150
RX_DIG	2	155
TX_CTRL_SUP	3	5
LED_DRV_SUP	3	5

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11 Layout

11.1 Layout Guidelines

Some key layout guidelines are mentioned below:

1. TXP, TXN, and TX3 are fast-switching lines and should be routed away from sensitive reference lines as well as from the INP, INN inputs.
2. If the INP, INN lines are required to be routed over a long trace, TI recommends that VCM be used as a shield for the INP, INN lines.
3. The device can draw high-switching currents from the LED_DRV_SUP pin. Therefore, TI recommends having a decoupling capacitor electrically close to the pin.

11.2 Layout Example

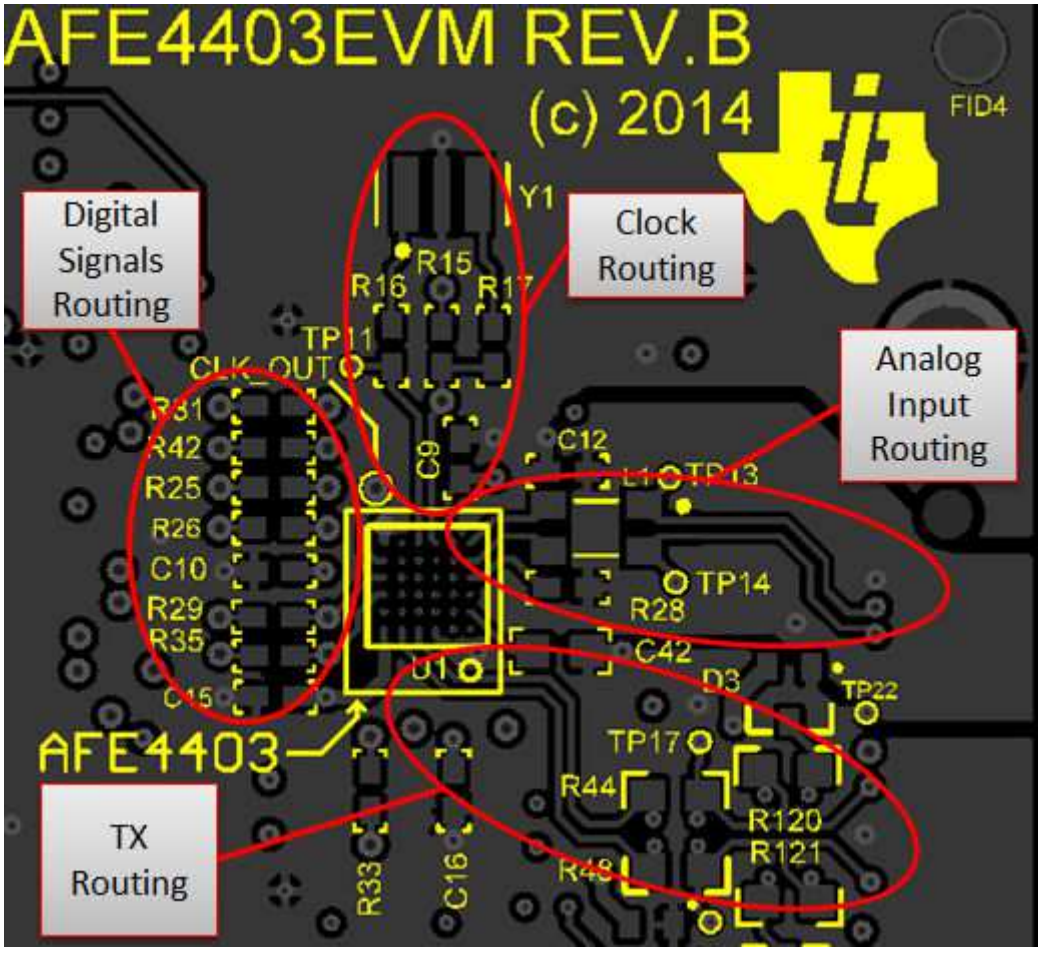


Figure 11-1. Example Layout

12 Device and Documentation Support

12.1 Trademarks

SPI™ is a trademark of Motorola.
All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.3 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AFE4403YZPR	Active	Production	DSBGA (YZP) | 36	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-20 to 70	AFE4403
AFE4403YZPR.A	Active	Production	DSBGA (YZP) | 36	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-20 to 70	AFE4403
AFE4403YZPT	Active	Production	DSBGA (YZP) | 36	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-20 to 70	AFE4403
AFE4403YZPT.A	Active	Production	DSBGA (YZP) | 36	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-20 to 70	AFE4403

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

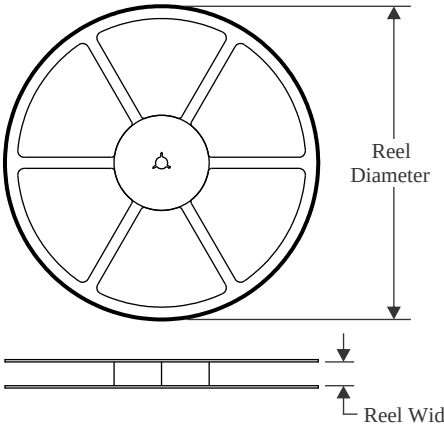
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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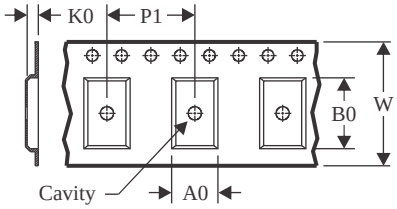
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

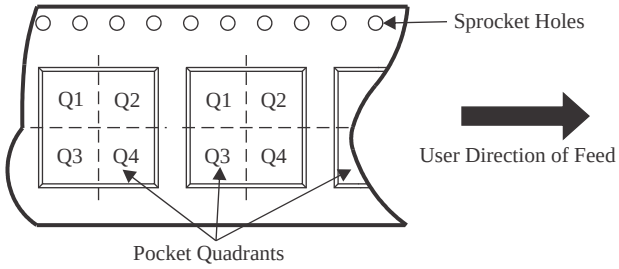


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

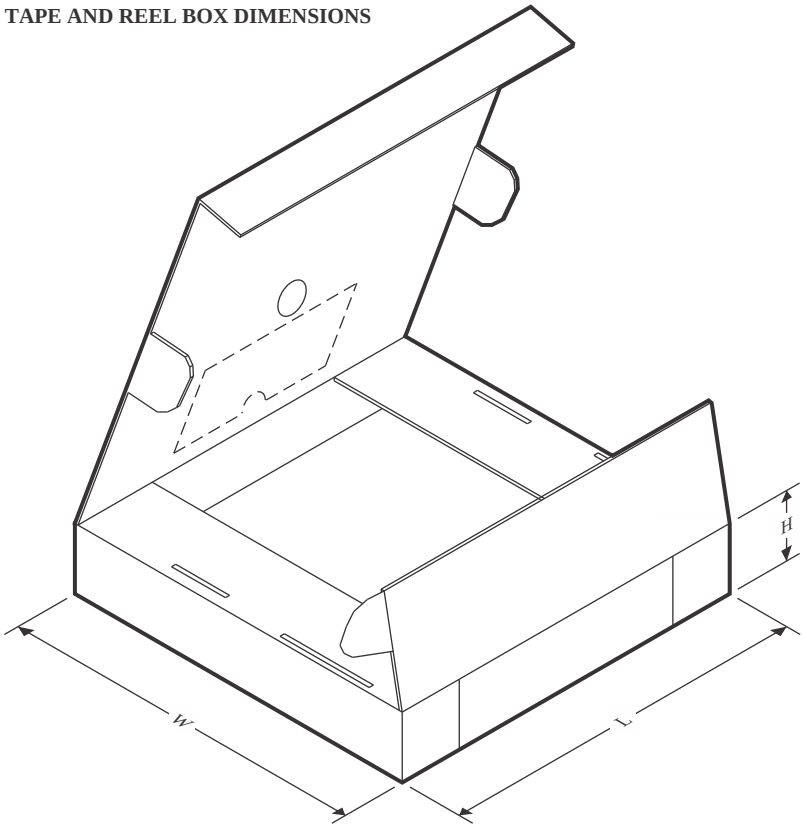
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AFE4403YZPR	DSBGA	YZP	36	3000	180.0	8.4	3.16	3.16	0.71	4.0	8.0	Q1
AFE4403YZPT	DSBGA	YZP	36	250	180.0	8.4	3.16	3.16	0.71	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

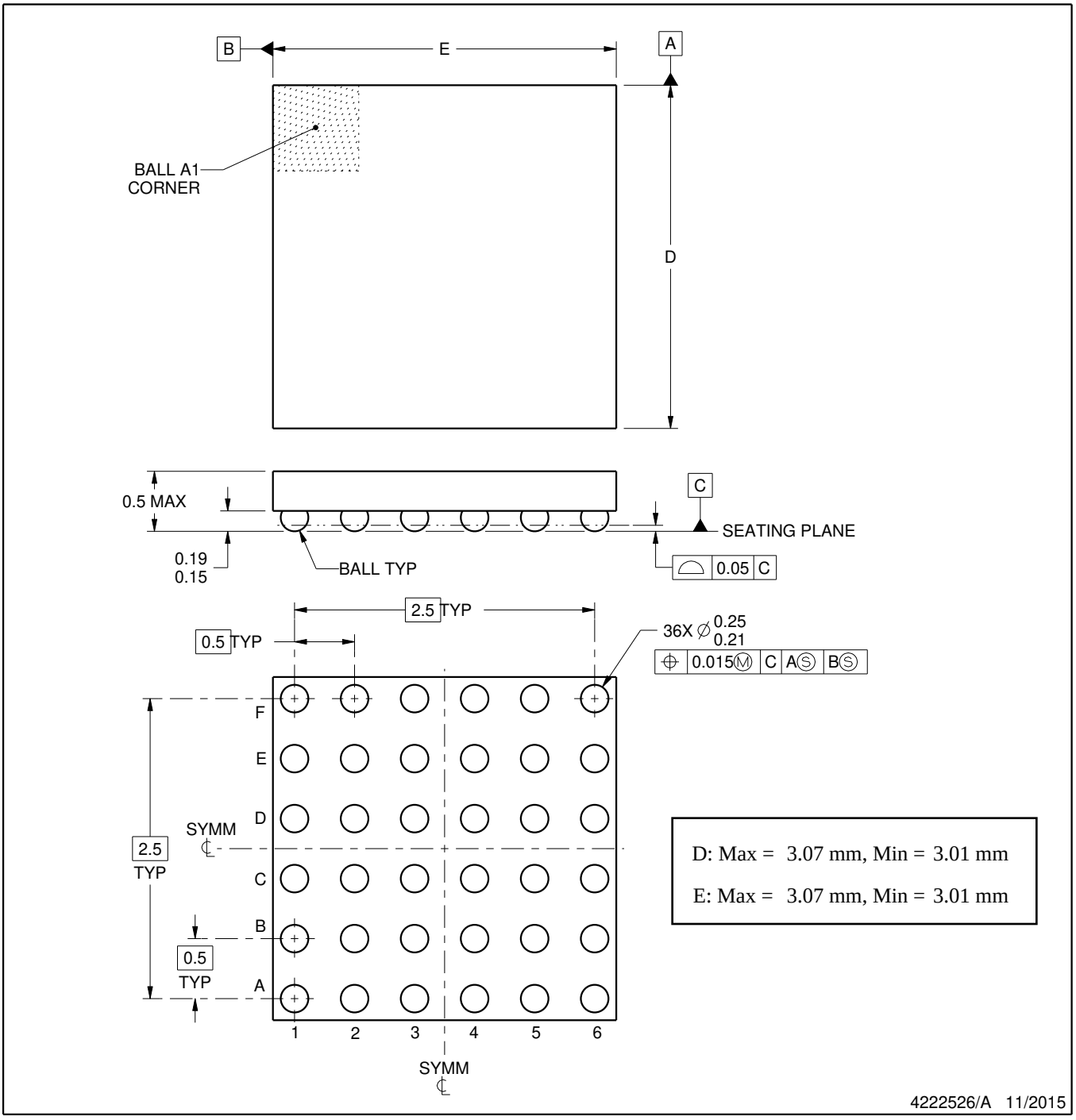
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AFE4403YZPR	DSBGA	YZP	36	3000	182.0	182.0	20.0
AFE4403YZPT	DSBGA	YZP	36	250	182.0	182.0	20.0

PACKAGE OUTLINE

YZP0036

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NanoFree Is a trademark of Texas Instruments.

NOTES:

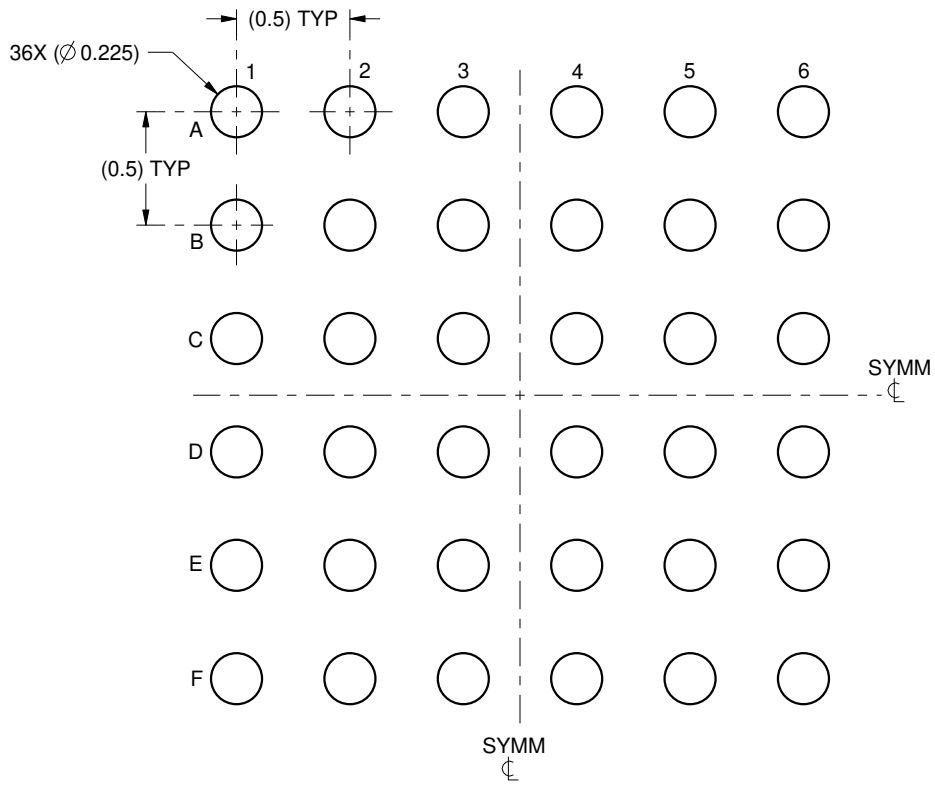
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

EXAMPLE BOARD LAYOUT

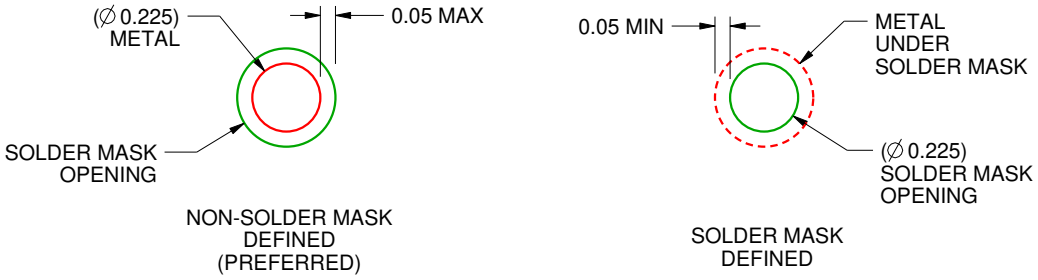
YZP0036

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

4222526/A 11/2015

NOTES: (continued)

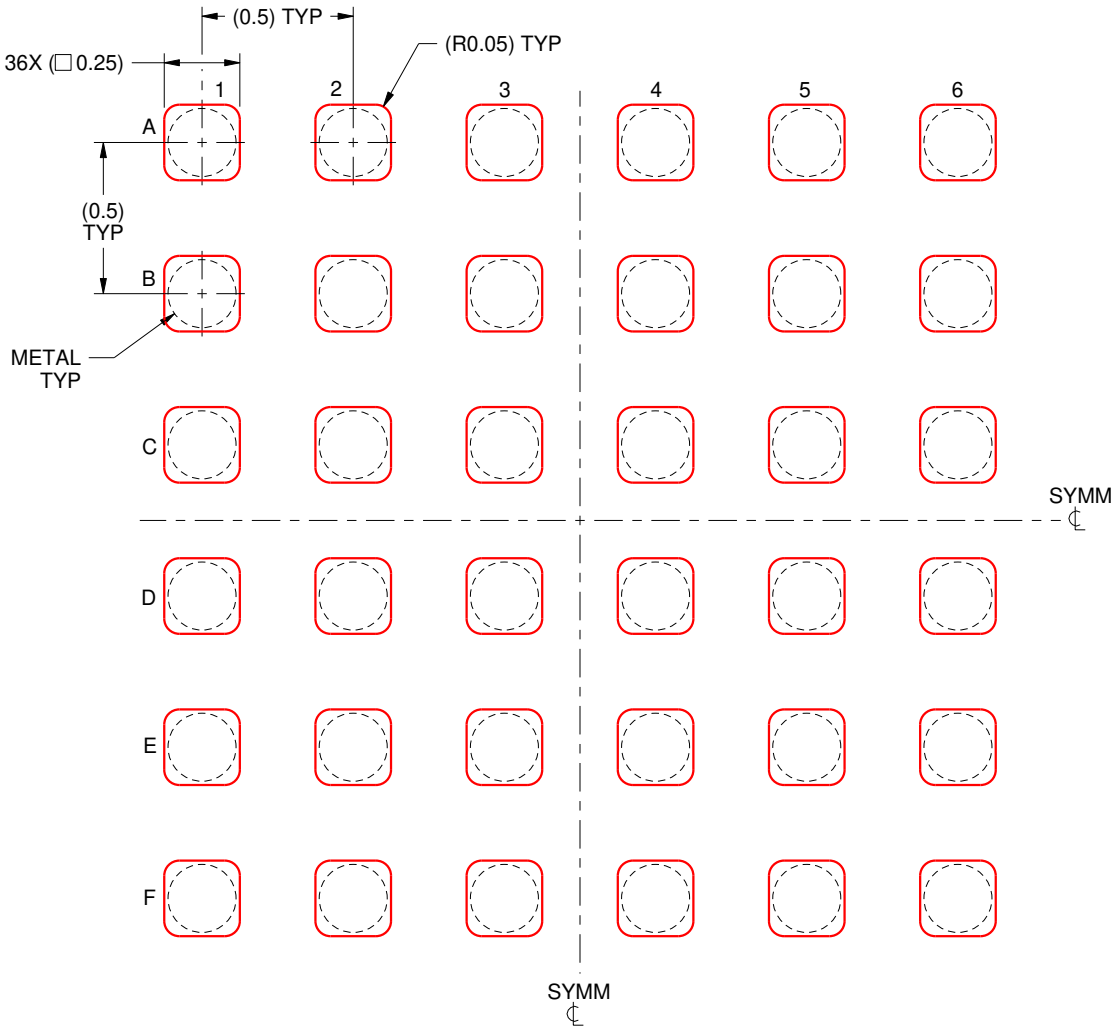
4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0036

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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