Analog Front End Wideband Mixed-Signal Transceiver

Check for Samples: AFE7222, AFE7225

1 INTRODUCTION

1.1 FEATURES

- **AFE7225**
  - **Dual 12-Bit 250MSPS TX DACs**
  - **Dual 12-Bit 125MSPS RX ADCs**
- **AFE7222**
  - **Dual 12-Bit 130MSPS TX DACs**
  - **Dual 12-Bit 65MSPS RX ADCs**
- **OPTIONS**
  - **Dual 12-Bit Auxiliary DACs**
  - **Dual Input 12-Bit Auxiliary ADC**
  - **TX Path Interpolation by 2 or 4**
  - **RX Path Decimation by 2**
  - **3.0V/1.8V Supplies, Low Power**
  - **Fast Wakeup Modes for Half-Duplex**
  - **Coarse or Fine Digital Mixer**
  - **Quadrature Modulation Corrections**
  - **Clock Input Divide/Multiply**
  - **Serial LVDS or Interleaved Parallel CMOS Interface**
  - **64-Pin QFN Package (9mm × 9mm)**

1.2 APPLICATIONS

- **Portable, Low Power Radio**
- **Wireless Infrastructure**
- **Point-to-Point Radio**
- **Pico-Cell BTS**

1.3 DESCRIPTION

The AFE7225/7222 is an analog front end designed for full- or half-duplex radios. Over-sampling transmit 12-bit DACs provide output frequencies from baseband to Nyquist. Under-sampling receive 12-bit ADCs allow analog inputs from baseband to ~230MHz. Most blocks within the AFE7225/7222 are independently controlled for optimization of power consumption versus utilization. Two auxiliary control 12-bit DACs and a dual input auxiliary monitoring 12-bit ADC are available via serial interface. Digital features include QMC (quadrature modulation correction), interpolation, decimation, RMS/peak power meter and mixers with independent NCOs for RX and TX path.

The AFE7225/7222 is available in a 64-pin 9x9mm QFN package (RGC). The AFE7225/7222 is built on Texas Instrument's low power analog CMOS process and is specified over the full industrial temperature range (–40°C to 85°C).

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

1.4 DETAILED BLOCK DIAGRAM

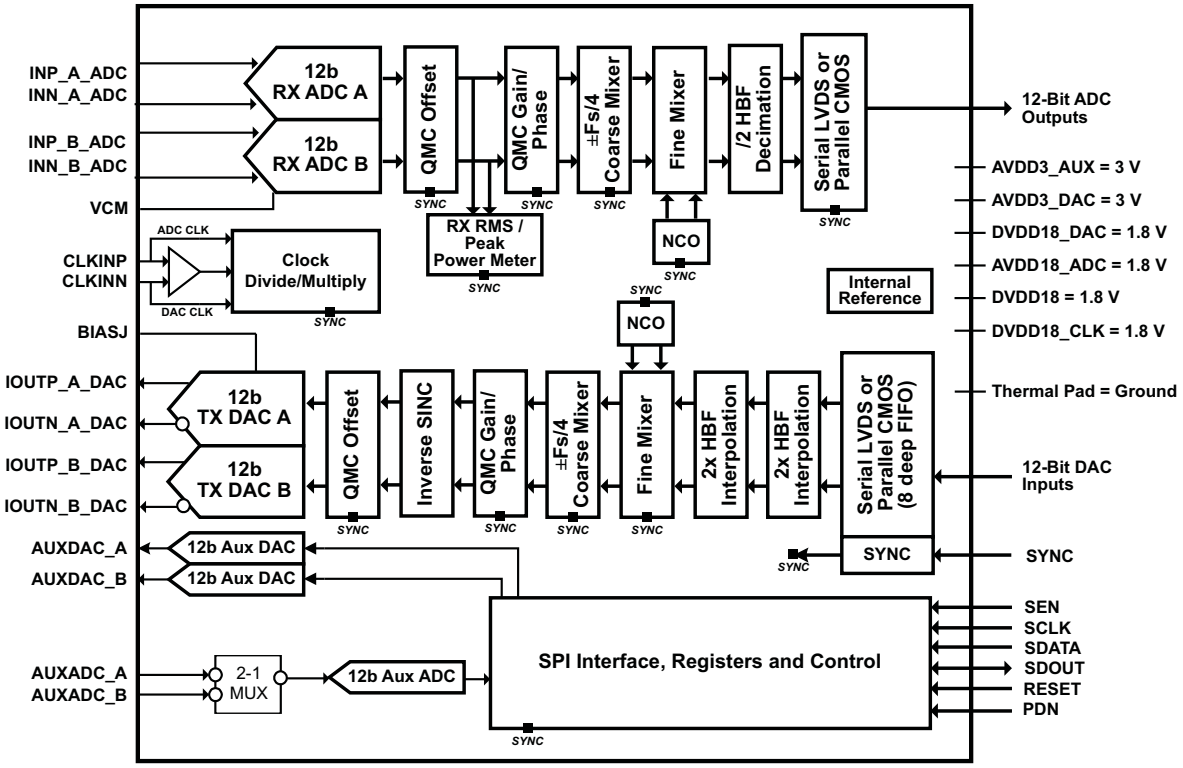

Figure 1-1. Block Diagram of AFE7222/AFE7225

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2 DEVICE INFORMATION

2.1 PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
AFE7222	QFN-64	RGC	–40°C to 85°C	AFE7222I	AFE7222IRGCT	Tape and Reel
					AFE7222IRGCR	Tape and Reel
					AFE7222IRGC25	Tape and Reel
AFE7225	QFN-64	RGC	–40°C to 85°C	AFE7225I	AFE7225IRGCT	Tape and Reel
					AFE7225IRGCR	Tape and Reel
					AFE7225IRGC25	Tape and Reel

2.2 DEVICE PINOUT, CMOS INPUT/OUTPUT MODE

RGC Package
(Top View)

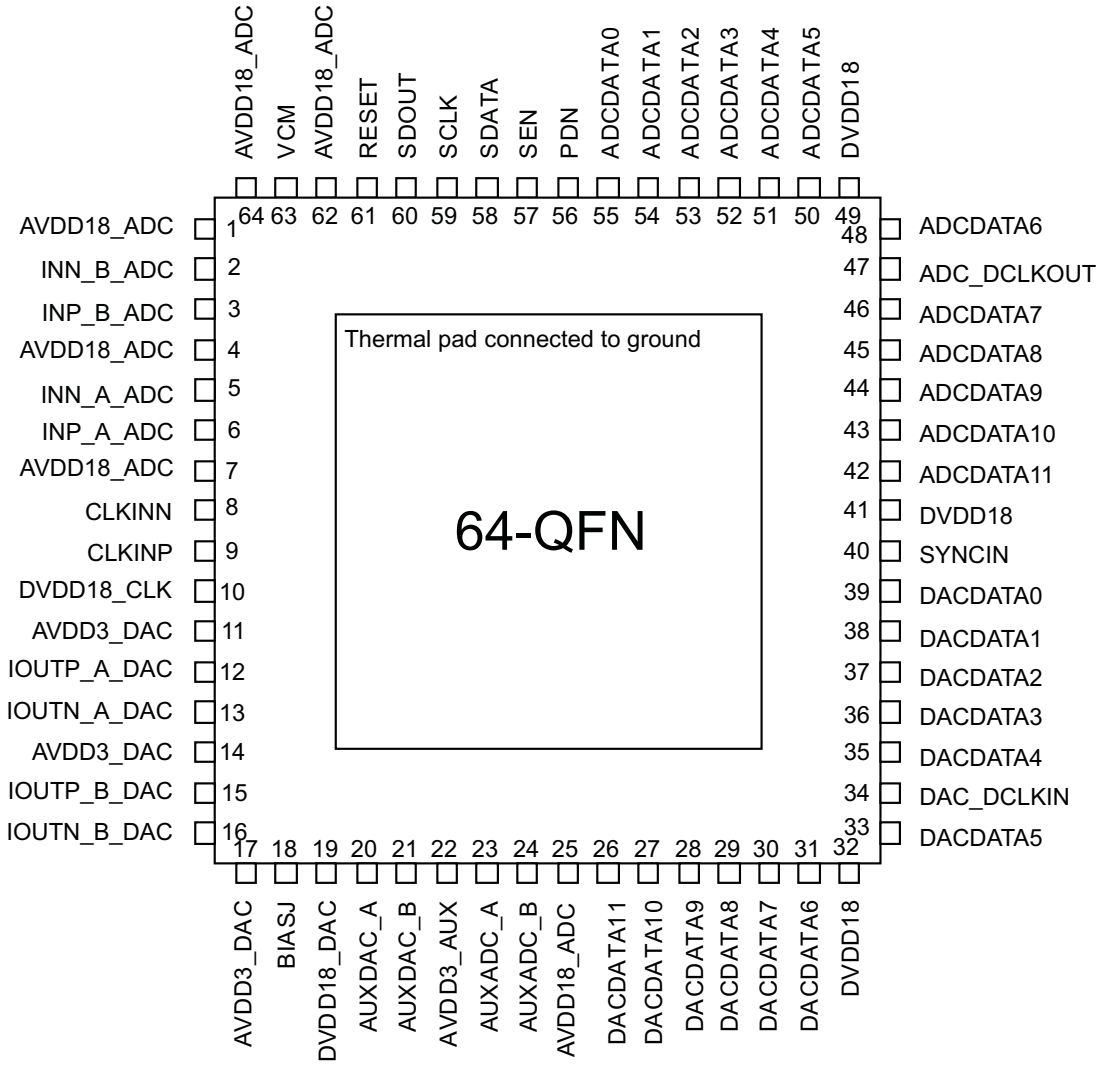

Figure 2-1. Device Pinout, CMOS Input/Output Mode

Table 2-1. Pin Configuration: CMOS Input/Output Mode

PIN		DESCRIPTION
NO.	NAME	
1	AVDD18_ADC	1.8V supply for RX ADCs
2	INN_B_ADC	RX ADC channel B analog input, negative
3	INP_B_ADC	RX ADC channel B analog input, positive
4	AVDD18_ADC	1.8V supply for RX ADCs
5	INN_A_ADC	RX ADC channel A analog input, negative
6	INP_A_ADC	RX ADC channel A analog input, positive
7	AVDD18_ADC	1.8V supply for RX ADCs
8	CLKINN	main clock input, negative side if differential mode, TX side if single-ended 2 clock mode
9	CLKINP	main clock input, positive side if differential mode, RX side if single-ended 2 clock mode
10	DVDD18_CLK	1.8V supply for Clocking circuit
11	AVDD3_DAC	3V supply for TX DACs
12	IOUTP_A_DAC	TX DAC channel A current output, positive (current sink DACs)
13	IOUTN_A_DAC	TX DAC channel A current output, negative (current sink DACs)
14	AVDD3_DAC	3V supply for TX DACs
15	IOUTP_B_DAC	TX DAC channel B current output, positive (current sink DACs)
16	IOUTN_B_DAC	TX DAC channel B current output, negative (current sink DACs)
17	AVDD3_DAC	3V supply for TX DACs
18	BIASJ	sets the TX DAC output current (resistor from pin to ground). Use 960 Ohm to set a full scale current of 20 mA.
19	DVDD18_DAC	1.8V DAC digital supply
20	AUXDAC_A	auxiliary DAC channel A output, current sourcing up to 7.5mA (SPI programmable)
21	AUXDAC_B	auxiliary DAC channel B output, current sourcing up to 7.5mA (SPI programmable)
22	AVDD3_AUX	3V supply for auxiliary ADC/DACs
23	AUXADC_A	auxiliary ADC channel A input
24	AUXADC_B	auxiliary ADC channel B input
25	AVDD18_ADC	1.8V supply for RX ADCs
26	DACDATA11	CMOS data input for TX data, MSB of TX DACs
27	DACDATA10	CMOS data input for TX data
28	DACDATA9	CMOS data input for TX data
29	DACDATA8	CMOS data input for TX data
30	DACDATA7	CMOS data input for TX data
31	DACDATA6	CMOS data input for TX data
32	DVDD18	1.8V supply for digital interface
33	DACDATA5	CMOS data input for TX data
34	DAC_DCLKIN	CMOS clock input for TX data. Send clock with data.
35	DACDATA4	CMOS data input for TX data
36	DACDATA3	CMOS data input for TX data
37	DACDATA2	CMOS data input for TX data
38	DACDATA1	CMOS data input for TX data
39	DACDATA0	CMOS data input for TX data. LSB of TX DACs
40	SYNCIN	CMOS sync input. Used to reset internal clock dividers and reset TX data FIFO pointer
41	DVDD18	1.8V supply for digital interface
42	ADCDATA11	CMOS data output for RX data, MSB of RX ADCs
43	ADCDATA10	CMOS data output for RX data
44	ADCDATA9	CMOS data output for RX data
45	ADCDATA8	CMOS data output for RX data
46	ADCDATA7	CMOS data output for RX data

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Table 2-1. Pin Configuration: CMOS Input/Output Mode (continued)

PIN		DESCRIPTION
NO.	NAME	
47	ADC_DCLKOUT	CMOS clock output for RX data
48	ADCDATA6	CMOS data output for RX data
49	DVDD18	1.8V supply for digital interface
50	ADCDATA5	CMOS data output for RX data
51	ADCDATA4	CMOS data output for RX data
52	ADCDATA3	CMOS data output for RX data
53	ADCDATA2	CMOS data output for RX data
54	ADCDATA1	CMOS data output for RX data
55	ADCDATA0	CMOS data output for RX data, LSB of RX ADCs
56	PDN	Can be programmed as global powerdown (deep sleep), fast recovery powerdown (light sleep) or TX/RX switch. Active high.
57	SEN	SPI enable (1.8V CMOS)
58	SDATA	SPI data input (1.8V CMOS)
59	SCLK	SPI clock input (1.8V CMOS)
60	SDOUT	SPI data output (1.8V CMOS)
61	RESET	Reset the SPI. Active high (1.8V CMOS).
62	AVDD18_ADC	1.8V supply for RX ADCs
63	VCM	Common mode voltage output. Outputs the ideal common mode input voltage for the ADC. Nominally around 0.95V.
64	AVDD18_ADC	1.8V supply for RX ADCs
Thermal pad	VSS	Connect thermal pad to the board ground

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2.3 DEVICE PINOUT, LVDS INPUT/OUTPUT MODE

RGC Package
(Top View)

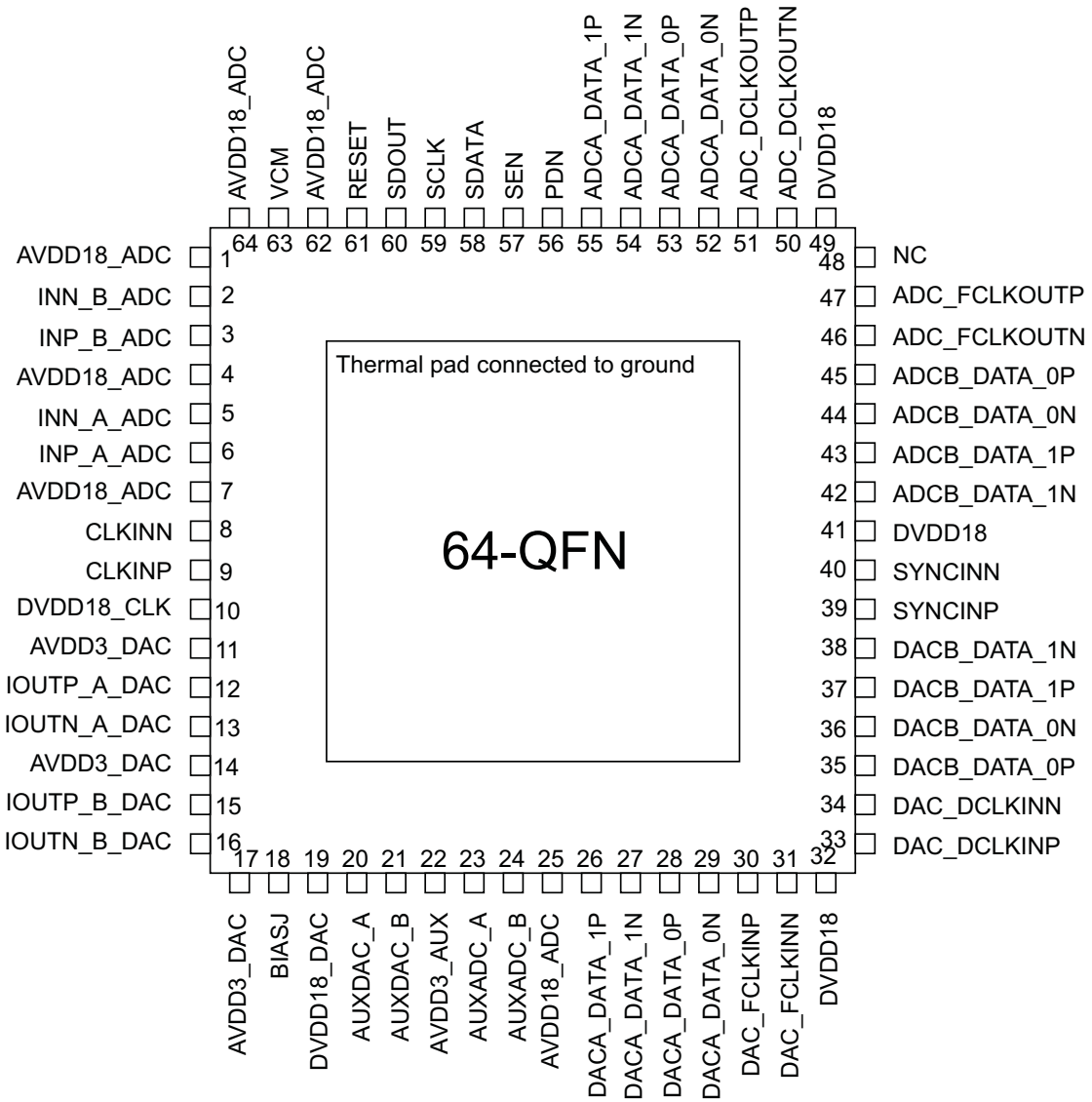

Figure 2-2. Device Pinout, LVDS Input/Output Mode

Table 2-2. Pin Configuration: LVDS Input/Output Mode

PIN		DESCRIPTION
NO.	NAME	
1	AVDD18_ADC	1.8V supply for RX ADCs
2	INN_B_ADC	RX ADC channel B analog input, negative
3	INP_B_ADC	RX ADC channel B analog input, positive
4	AVDD18_ADC	1.8V supply for RX ADCs
5	INN_A_ADC	RX ADC channel A analog input, negative
6	INP_A_ADC	RX ADC channel A analog input, positive
7	AVDD18_ADC	1.8V supply for RX ADCs
8	CLKINN	main clock input, negative side if differential mode, TX side if single-ended 2 clock mode

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Table 2-2. Pin Configuration: LVDS Input/Output Mode (continued)

PIN		DESCRIPTION
NO.	NAME	
9	CLKINP	main clock input, positive side if differential mode, RX side if single-ended 2 clock mode
10	DVDD18_CLK	1.8V supply for Clocking circuit
11	AVDD3_DAC	3V supply for TX DACs
12	IOUTP_A_DAC	TX DAC channel A current output, positive (current sink DACs)
13	IOUTN_A_DAC	TX DAC channel A current output, negative (current sink DACs)
14	AVDD3_DAC	3V supply for TX DACs
15	IOUTP_B_DAC	TX DAC channel B current output, positive (current sink DACs)
16	IOUTN_B_DAC	TX DAC channel B current output, negative (current sink DACs)
17	AVDD3_DAC	3V supply for TX DACs
18	BIASJ	sets the TX DAC output current (resistor from pin to ground). Use 960 Ohm to set a full scale current of 20 mA.
19	DVDD18_DAC	1.8V DAC digital supply
20	AUXDAC_A	auxiliary DAC channel A output, current sourcing up to 7.5mA (SPI programmable)
21	AUXDAC_B	auxiliary DAC channel B output, current sourcing up to 7.5mA (SPI programmable)
22	AVDD3_AUX	3V supply for auxiliary ADC/DACs
23	AUXADC_A	auxiliary ADC channel A input
24	AUXADC_B	auxiliary ADC channel B input
25	AVDD18_ADC	1.8V supply for RX ADCs
26, 27		LVDS Wire 1 data input for Channel A TX data – inactive in 1-wire mode, LSB byte in 2-wire mode
26	DAC_DATA_11	Positive
27	DAC_DATA_10	Negative
28, 29		LVDS Wire 0 data input for Channel A TX data – active in 1-wire mode, MSB byte in 2-wire mode
28	DAC_DATA_9	Positive
29	DAC_DATA_8	Negative
30, 31		LVDS frame clock input
30	DAC_FCLKINP	Positive
31	DAC_FCLKINN	Negative
32	DVDD18	1.8V supply for digital interface
33, 34		LVDS bit clock input
33	DAC_DCLKINP	Positive
34	DAC_DCLKINN	Negative
35, 36		LVDS Wire 0 data input for Channel B TX data – active in 1-wire mode, LSB byte in 2-wire mode
35	DACB_DATA_0P	Positive
36	DACB_DATA_0N	Negative
37, 38		LVDS Wire 1 data input for Channel B TX data – inactive in 1-wire mode, MSB byte in 2-wire mode
37	DACB_DATA_1P	Positive
38	DACB_DATA_1N	Negative
39, 40		LVDS SYNC input – Used to reset internal clock dividers and reset TX data FIFO pointer
39	SYNCINP	Positive
40	SYNCINN	Negative
41	DVDD18	1.8V supply for digital interface
42, 43		LVDS Wire 1 data output for Channel B RX data – inactive in 1-wire mode, MSB byte in 2-wire mode
42	ADCB_DATA_1N	Positive
43	ADCB_DATA_1P	Negative
44, 45		LVDS Wire 0 data output for Channel B RX data – active in 1-wire mode, LSB byte in 2-wire mode
44	ADCB_DATA_0N	Positive
45	ADCB_DATA_0P	Negative

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Table 2-2. Pin Configuration: LVDS Input/Output Mode (continued)

PIN		DESCRIPTION
NO.	NAME	
46, 47		LVDS frame clock output
46	ADC_FCLKOUTN	Positive
47	ADC_FCLKOUTP	Negative
48	NC	No Connect
49	DVDD18	1.8V supply for digital interface
50, 51		LVDS bit clock output
50	ADC_DCLKOUTN	Positive
51	ADCDCLKOUTP	Negative
52,53		LVDS Wire 0 data output for Channel A RX data – active in 1-wire mode, MSB byte in 2-wire mode
52	ADCA_DATA_0N	Positive
53	ADCA_DATA_0P	Negative
54,55		LVDS Wire 1 data output for Channel A RX data – inactive in 1-wire mode, LSB byte in 2-wire mode
54	ADCA_DATA_1N	Positive
55	ADCA_DATA_1P	Negative
56	PDN	Can be programmed as global powerdown (deep sleep), fast recovery powerdown (light sleep) or TX/RX switch. Active high.
57	SEN	SPI enable (1.8V CMOS)
58	SDATA	SPI data input (1.8V CMOS)
59	SCLK	SPI clock input (1.8V CMOS)
60	SDOUT	SPI data output (1.8V CMOS)
61	RESET	Reset the SPI. Active high (1.8V CMOS).
62	AVDD18_ADC	1.8V supply for RX ADCs
63	VCM	Common mode voltage output. Outputs the ideal common mode input voltage for the ADC. Nominally around 0.95V.
64	AVDD18_ADC	1.8V supply for RX ADCs
Thermal pad	VSS	Connect thermal pad to the board ground

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3 ELECTRICAL SPECIFICATIONS

3.1 ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
	Supply voltage range, *VDD3*	–0.3	3.6	V
	Supply voltage range, *VDD18*	–0.3	2.1	V
	Voltage betweeen *VDD3* to *VDD18*	–2.4	3.9	V
	INP_A_ADC, INM_A_ADC, INP_B_ADC, INM_B_ADC, AUXADC_A, AUXADC_B, CLKINN, CLKINP	–0.3	2.1	V
	RESET, SCLK, SDATA SEN	–0.3	3.9	V
	DAC*_DATA_nP/M, DAC_DCLK	–0.3	2.1	V
T_A	Operating free-air temperature range	–40	85	°C
T_J	Operating junction tamperature range		125	°C
T_{stg}	Storage temperature range	–65	150	°C
	ESD rating Human Body Model (HBM)		2	kV

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

3.2 THERMAL INFORMATION

THERMAL METRIC		AFE7222/AFE7225 RGC PACKAGE 64 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	22.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	6.7	
θ_{JB}	Junction-to-board thermal resistance	2.3	
ψ_{JT}	Junction-to-top characterization parameter	0.1	
ψ_{JB}	Junction-to-board characterization parameter	2.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.2	

3.3 RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	AFE7222			AFE7225			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
DVDD18 voltage range		1.7	1.8	1.9	1.7	1.8	1.9	V
AVDD3 voltage range		2.85	3.0	3.6	2.85	3.0	3.6	V
Common mode voltage at ADC input pins		VCM-0.05	VCM	VCM+0.05	VCM–0.05	VCM	VCM+0.05	V
Common mode voltage at DAC output pins			AVDD3			AVDD3		V
ADC_CLK speed(1)		2.5(2)		65	2.5(2)		125	MSPS
DAC_CLK speed(1)		1		130	1		250	MSPS

(1) See Table 10-1 and Table 10-2 for corresponding maximum interface rates.
(2) Minimum ADC_CLK speed can be reduced to 0.8 MSPS by writing the following serial interface registers:
- Register address 0x208, value 0x8
- Register address 0x4, value 0x8

3.4 SUPPLY CHARACTERISTICS

AVDD18_ADC=1.8V, DVDD18_CLK=1.8V, DVDD18=1.8V, DVDD18_DAC=1.8V, AVDD3_DAC=3.0V, AVDD3_AUX=3.0V, IOUTFS=20mA, typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	AFE7225			UNIT
POWER IN LVDS MODE		**Dual RX ADC, Dual TX DAC with Interpolate by 2, 2-wire LVDS interface F_{ADCCLK} = 125 MSPS f_{ADCIN} = 10 MHz F_{DACCLK} = 250 MSPS f_{DACOUT} = 10 MHz**			**UNIT**
		MIN	**TYP**	**MAX**	
Power dissipation, full duplex mode	RX and TX active, No input signal applied on ADC and DAC		577	650	mW
Supply current, full duplex mode	AVDD18_ADC, RX and TX active, No input signal applied on ADC and DAC		115		mA
	DVDD18, RX and TX active, No input signal applied on ADC and DAC		95		
	DVDD18_CLK, RX and TX active, No input signal applied on ADC and DAC		12		
	DVDD18_DAC, RX and TX active, No input signal applied on ADC and DAC		7		
	AVDD3_DAC, RX and TX active, No input signal applied on ADC and DAC		48		
	AVDD3_AUX, RX and TX active, No input signal applied on ADC and DAC		7		
Power dissipation, half duplex RX mode	RX active, TX in light sleep, TX clock is off, No input signal applied on ADC and DAC		362	417	mW
Power dissipation, half duplex TX mode	TX active, RX in light sleep, RX clock is on, No input signal applied on ADC and DAC		419	482	mW
Power dissipation in Sleep modes	Global powerdown enabled		12	40	mW
	Fast recovery powerdown enabled, TX/RX sleeping, clocks on		215	246	
	Fast recovery powerdown enabled, TX/RX sleeping, TX clock off, RX clock on		177	231	

PARAMETER	TEST CONDITIONS		AFE7222/AFE7225			UNIT
POWER IN CMOS MODE			**Dual RX ADC, Dual TX DAC with Interpolate by 2, CMOS interface F_{ADCCLK} = 65 MSPS f_{ADCIN} = 10 MHz F_{DACCLK} = 130 MSPS f_{DACOUT} = 10 MHz**			**UNIT**
			MIN	**TYP**	**MAX**	
Power dissipation, full duplex mode	RX and TX active, No input signal applied on ADC and DAC	Power (AVDD18_ADC, DVDD18_CLK, DVDD18_DAC, AVDD3_DAC, AVDD3_AUX)		326	391	mW
		Digital Power(1) (DVDD18)		72		mW
		Total Power		398		mW
Supply current, full duplex mode	AVDD18_ADC, RX and TX active, No input signal applied on ADC and DAC			77		mA
	DVDD18, RX and TX active, No input signal applied on ADC and DAC			40		
	DVDD18_CLK, RX and TX active, No input signal applied on ADC and DAC			9		
	DVDD18_DAC, RX and TX active, No input signal applied on ADC and DAC			4		
	AVDD3_DAC, RX and TX active, No input signal applied on ADC and DAC			48		
	AVDD3_AUX, RX and TX active, No input signal applied on ADC and DAC			7		
Power dissipation, half duplex RX mode	RX active, TX in light sleep, TX clock is off, No input signal applied on ADC and DAC	Power (AVDD18_ADC, DVDD18_CLK, DVDD18_DAC, AVDD3_DAC, AVDD3_AUX)		176	211	mW
		Digital Power(1) (DVDD18)		36		
		Total Power		212		
Power dissipation, half duplex TX mode	TX active, RX in light sleep, RX clock is on, No input signal applied on ADC and DAC	Power (AVDD18_ADC, DVDD18_CLK, DVDD18_DAC, AVDD3_DAC, AVDD3_AUX)		235	282	mW
		Digital Power(1) (DVDD18)		56		
		Total Power		291		

(1) These numbers belong to no-load capacitance present on board. The maximum DVDD18 current with CMOS interface depends on the actual load capacitance on the digital output lines.

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3.5 SUPPLY CHARACTERISTICS (Continued)

AVDD18_ADC=1.8V, DVDD18_CLK=1.8V, DVDD18=1.8V, DVDD18_DAC=1.8V, AVDD3_DAC=3.0V, AVDD3_AUX=3.0V, IOUTFS=20mA, typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	AFE7222/AFE7225			UNIT
POWER IN CMOS MODE		**Dual RX ADC, Dual TX DAC with Interpolate by 2, CMOS interface F_{ADCCLK} = 65 MSPS f_{ADCIN} = 10 MHz F_{DACCLK} = 130 MSPS f_{DACOUT} = 10 MHz**			
		MIN	**TYP**	**MAX**	
Power dissipation in Sleep modes	Global powerdown enabled		12	40	mW
	Fast recovery powerdown enabled, TX/RX sleeping, clocks on		140	165	
	Fast recovery powerdown enabled, TX/RX sleeping, TX clock off, RX clock on.		120	165	
Power Up and Power Down Time in Different Modes					
Global powerdown, RX recovery time	Differential input clock		25		µs
	Single-ended input clock		20		
Global powerdown in Low power RX CMOS mode, RX recovery time (ADC running at less than 40 MSPS)	Differential input clock		25		µs
	Single-ended input clock		13		
Global powerdown, TX recovery time	Differential input clock		25		µs
	Single-ended input clock		4		
RX recovery time in fast recovery mode	RX clock is ON during powerdown		5		µs
TX recovery time in fast recovery mode			4		µs
RX recovery time from RX powerdown	RX clock is on during powerdown		5		µs
TX recovery time fromTX powerdown			4		µs

3.6 RX ADC ELECTRICAL CHARACTERISTICS

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, supplies at nominal voltages, 50% clock duty cycle, LVDS output interface, –1dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	AFE7222			AFE7225			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Maximum Clock Rate					65			125	MSPS
Resolution					12			12	bits
ANALOG INPUTS									
	Differential input range			2			2		Vpp
V_{CM}	Common mode output voltage			0.95			0.95		V
	Input resistance (DC)	Differential		>1			>1		MΩ
	Input capacitance	Differential		4			4		pF
	Analog input bandwidth			550			550		MHz
CMRR	Common mode rejection ratio	Fin = 10MHz		40			40		dB
DYNAMIC ACCURACY									
DNL	Differential linearity error	No Missing Codes, Fin =10MHz	–0.95	±0.5	1.4	–0.95	±0.5	1.4	LSB
INL	Integral linearity error	Fin = 10MHz	–1.7	±0.2	1.7	–1.7	±0.2	1.7	LSB
	Offset error		–15	2	15	–15	3	15	mV
	Offset temperature co-efficient			>0.005			>0.005		mV/°C
	Gain error as a result of internal reference inaccuracy alone – EGREF		–2.5		2.5	–2.5		2.5	%FS
	Gain error of channel alone – EGCHAN			±1			±1		%FS
DYNAMIC AC CHARACTERISTICS									
SNR	Signal-to-noise ratio(1)	Fin = 10MHz	67.5	70.5		67	70.7		dBFS
		Fin = 70MHz		70			70.1		dBFS
		Fin = 140MHz		68.7			69.5		dBFS
SFDR	Spurious free dynamic range(1)	Fin = 10MHz	73	85		73	84		dBc
		Fin = 70MHz		81			79		dBc
		Fin = 140MHz		77			76		dBc

(1) Up to 65MSPS typical SNR and SFDR performance in CMOS interface is same as with LVDS interface.

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3.7 TX DAC ELECTRICAL CHARACTERISTICS

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, 50% clock duty cycle, supplies at nominal voltages, I_{OUTFS} = 20 mA, DAC output common mode voltage is AVDD3=3.0V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	AFE7222			AFE7225			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Maximum clock output rate					130			250	MSPS
Resolution					12			12	Bits
ANALOG OUTPUTS									
	Full scale output current, per DAC		2		20	2		20	mA
	Output voltage compliance range	I_{OUTFS} = 20 mA, Current sink output	AVDD3_DAC –0.5		AVDD3_DAC+0.5	AVDD3_DAC –0.5		AVDD3_DAC+0.5	V
	Output resistance			300			300		kΩ
	Output capacitance			5			5		pF
	Offset error	Mid code offset		±0.03			±0.03		%FS(1)
	Gain error	Internal reference		±1			±1		%FS(1)
	Gain mismatch	Internal reference dual DAC		±0.5			±0.5		%FS(1)
DC PERFORMANCE									
INL	Integral non-linearity	Fout = 10 MHz	–2	±1	2	–2	±1	2	LSB
DNL	Differential non-linearity	Fout = 10 MHz		±0.5			±0.5		LSB
AC PERFORMANCE									
	Noise spectral density	Fout = 10 MHz, 0 dBFS	145.5	149		148.5	151		dBc/Hz
SFDR	Spurious free dynamic range	Fout = 10 MHz, 0 dBFS	70	76		70	76		dBc
		Fout = 20 MHz, 0 dBFS		75			74		dBc
IMD	Inter-modulation distortion	Fout = 5.1/6.1 MHz, –7 dBFS each		73			73		dBc
ACLR	Adjacent channel leakage ratio	DAC clock = 122.88 MSPS, Fout = 30.72 MHz		75					dB
		DAC clock = 245.76 MSPS, Fout = 61.44 MHz					73		

(1) %FS = % Differential Full Scale

3.8 AUXILIARY ADC ELECTRICAL CHARACTERISTICS

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, supplies at nominal voltages, unless otherwise noted.

PARAMETER		TEST CONDITIONS	AFE7222 / AFE7225			UNIT
			MIN	TYP	MAX	
Maximum Clock Rate					100	kSPS
Resolution					12	Bits
ANALOG INPUTS						
	Input voltage range			1.5		V
	Input capacitance			4		pF
	Maximum input signal frequency			10		kHz
DC PERFORMANCE						
INL	Integral non-linearity	Static conditions (near DC input)	–4.5	±2	4.5	LSB

3.9 AUXILIARY DAC ELECTRICAL CHARACTERISTICS

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, supplies at nominal voltages, I_{OUTFS} = 5mA, 300 Ω termination, unless otherwise noted.

PARAMETER		TEST CONDITIONS	AFE7222/AFE7225			UNIT
			MIN	TYP	MAX	
Maximum Clock Rate		Continuous refresh of AUX DAC Channel A from SDATA and Channel B from SDOUT			3.33 (1)	MSPS
Resolution					12	Bits
ANALOG OUTPUTS						
	Output current, per auxDAC		2.5		7.5	mA
	Output voltage compliance range			1.5		V
DYNAMIC PERFORMANCE						
INL	Integral non-linearity	Static conditions (near DC input)	–1.7	±0.5	1.7	LSB
DNL	Differential non-linearity	Static conditions (near DC input)		±0.3		LSB

(1) 12 bits x (1/SCLK) in direct access mode, SCLK max limit is 40MHz

3.10 DIGITAL CHARACTERISTICS

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD18*, DVDD18* = 1.8V, AVDD3* = 3.0V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS – RESET, SCLK, SDATA, SEN, PDN						
	High-level input voltage	All these pins support 1.8V and 3V CMOS logic levels.	1.3			V
	Low-level input voltage				0.4	V
DAC DIGITAL INPUTS IN CMOS INTERFACE MODE						
	High-level input voltage	1.8V CMOS logic levels only	1.3			V
	Low-level input voltage				0.4	V
DAC DIGITAL INPUTS IN LVDS INTERFACE MODE						
V_{IDH}	High-level differential input voltage	Standard swing LVDS with external 100ohms termination		350		mV
V_{IDL}	Low-level differential input voltage	Standard swing LVDS with external 100ohms termination		–350		mV
V_{ICM}	Input common-mode voltage			1.2		V
DIGITAL OUTPUTS – CMOS INTERFACE – SDOUT, ADC OUTPUTS (IN CMOS INTERFACE MODE)						
	High-level output voltage		DVDD18 – 0.1	DVDD18		V
	Low-level output voltage			0	0.1	V
DIGITAL OUTPUTS – LVDS INTERFACE (ADC OUTPUTS IN LVDS MODE)						
V_{ODH}	High-level differential output voltage	Standard swing LVDS	235		375	mV
V_{ODL}	Low-level differential output voltage	Standard swing LVDS	–375		–235	mV
V_{OCM}	Output common-mode voltage		0.9	1.05	1.2	V

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3.11 TIMING REQUIREMENTS

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	AFE7222			AFE7225			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SCLK INPUT									
t_{SCLK}	CLOCK period		25			25			ns
t_{SCLKH}	CLOCK pulse width high	Assuming 50/50 duty cycle		12.5			12.5		ns
t_{SCLKL}	CLOCK pulse width low			12.5			12.5		ns

3.12 TIMING REQUIREMENTS FOR RECEIVE PATH – LVDS AND CMOS MODES

Typical values are at 25°C, AVDD3_DAC = 3.0 V, AVDD3_AUX = 3.0 V, AVDD18_ADC = 1.8 V, DVDD18_CLK = 1.8 V, DVDD18_DAC = 1.8 V, DVDD18 = 1.8 V, sampling frequency = 125 MSPS, sine wave input clock, 1.5 V_{pp} clock amplitude, C_{LOAD} = 5 pF (1), R_{LOAD} = 100 Ω (2), unless otherwise noted. Min and max values are across the full temperature range T_{MIN} = -40°C to T_{MAX} = 85°C, AVDD3_DAC = 3.0 V, AVDD3_AUX = 3.0 V, AVDD18_ADC = 1.8 V, DVDD18_CLK = 1.8 V, DVDD18_DAC = 1.8 V, DVDD18 = 1.7 V to 1.9 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A	Aperture delay			2		ns
	Aperture delay matching	Between two channels on the same device		±120		ps
	Aperture delay matching	Between two devices at same temperature and DVDD18 supply		±450		ps
T_J	Aperture jitter	Jitter added by internal clock distribution, specified as it relates to the receive ADC		250		fs rms
	ADC Latency(3)	Default Mode		16		clock cycles
		Mixer Enabled (RX_MIXER_EN = 1)		33		
		RX QMC Gain Phase Correction Enabled (RX_QMC_CORR_ENA=1, RX_QMC_CORR_ENB=1)		22		
LVDS OUTPUT INTERFACE						
2-WIRE MODE, DDR CLOCK(4), Sampling frequency = 125MSPS						
t_{su}	Data setup time (5)	Data valid(5) to zero-crossing of CLKOUTP	0.29	0.42		ns
t_h	Data hold time (5)	Zero-crossing of CLKOUTP to data becoming invalid (5)	0.3	0.47		ns
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over 10 MSPS ≤ Sampling frequency ≤ 125 MSPS Ts = 1/Sampling frequency		$t_{PDI} = t_{DELAY}$		ns
t_{delay}			11.5	13.8	15.5	ns
	Variation of t_{delay}	Between two devices at same temperature and DVDD18 supply		±300		ps
	LVDS bit clock duty cycle	Duty cycle of differential clock, (ADC_DCLKOUTP-ADC_DCLKOUTM) 10 MSPS ≤ Sampling frequency ≤ 125 MSPS		50%		
2-WIRE MODE, SDR CLOCK(4), Sampling frequency = 65MSPS						
t_{su}	Data setup time (5)	Data valid (5) to zero-crossing of CLKOUTP	0.85	1.08		ns
t_h	Data hold time (5)	Zero-crossing of CLKOUTP to data becoming invalid (5)	1.08	1.21		ns
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over 10 MSPS ≤ Sampling frequency ≤ 65 MSPS Ts = 1/Sampling frequency		$t_{PDI} = 0.5*Ts + t_{DELAY}$		ns
t_{delay}			11.5	14	16.5	ns
	Variation of t_{delay}	Between two devices at same temperature and DVDD18 supply		±300		ps
	LVDS bit clock duty cycle	Duty cycle of differential clock, (CLKOUTP-CLKOUTM) 10 MSPS ≤ Sampling frequency ≤ 65 MSPS		50%		
1-WIRE MODE (DDR CLOCK ONLY)(4), Sampling frequency = 65MSPS						
t_{su}	Data setup time (5)	Data valid (5) to zero-crossing of CLKOUTP	0.25	0.39		ns

(1) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground
(2) R_{LOAD} is the differential load resistance between the LVDS output pair.
(3) At higher frequencies, t_{PDI} is greater than one clock period and overall latency = ADC latency + 1.
(4) Measurements are done with a transmission line of 100-Ω characteristic impedance between the device and the load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(5) Data valid refers to LOGIC HIGH of +100.0 mV and LOGIC LOW of -100.0 mV.

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Typical values are at 25°C, AVDD3_DAC = 3.0 V, AVDD3_AUX = 3.0 V, AVDD18_ADC = 1.8 V, DVDD18_CLK = 1.8 V, DVDD18_DAC = 1.8 V, DVDD18 = 1.8 V, sampling frequency = 125 MSPS, sine wave input clock, 1.5 V_{pp} clock amplitude, C_{LOAD} = 5 pF (1), R_{LOAD} = 100 Ω (2), unless otherwise noted. Min and max values are across the full temperature range T_{MIN} = -40°C to T_{MAX} = 85°C, AVDD3_DAC = 3.0 V, AVDD3_AUX = 3.0 V, AVDD18_ADC = 1.8 V, DVDD18_CLK = 1.8 V, DVDD18_DAC = 1.8 V, DVDD18 = 1.7 V to 1.9 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_h	Data hold time (5)	Zero-crossing of CLKOUTP to data becoming invalid (5)	0.26	0.4		ns
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over 10 MSPS ≤ Sampling frequency ≤ 65 MSPS Ts = 1/Sampling frequency	t_{PDI} = 0.5*Ts + t_{DELAY}			ns
t_{delay}			11.5	13.5	15.5	ns
	Variation of t_{delay}	Between two devices at same temperature and DVDD18 supply		±300		ps
	LVDS bit clock duty cycle	Duty cycle of differential clock, (CLKOUTP-CLKOUTM) 10 MSPS ≤ Sampling frequency ≤ 65 MSPS		50%		
COMMON						
t_{RISE}, t_{FALL}	Data rise time, Data fall time	Rise time measured from -100 mV to +100 mV Fall time measured from +100 mV to -100 mV 10 MSPS ≤ Sampling frequency ≤ 125 MSPS		0.08		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from -100 mV to +100 mV Fall time measured from +100 mV to -100 mV 10 MSPS ≤ Sampling frequency ≤ 125 MSPS		0.1		ns
CMOS OUTPUT INTERFACE (6), Sampling frequency = 105MSPS (7)						
t_{su}	Data setup time (8)	Data valid to cross-over of ADC_DCLKOUT (8)	0.5	1.4		ns
t_h	Data hold time (8)	Cross-over of ADC_DCLKOUT to data becoming invalid (8)	1.4	1.8		ns
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over 10 MSPS ≤ Sampling frequency ≤ 105 MSPS Ts = 1/Sampling frequency	t_{PDI} = 0.5*Ts + t_{DELAY}			ns
t_{delay}			14	16.5	19	ns
	Variation of t_{delay}	Between two devices at same temperature and DVDD18 supply		±350		ps
	Output clock duty cycle	Duty cycle of output clock, ADC_DCLKOUT 10 MSPS ≤ Sampling frequency ≤ 105 MSPS		46%		
t_{RISE}, t_{FALL}	Data rise time, Data fall time	Rise time measured from 20% to 80% of DVDD18 Fall time measured from 80% to 20% of DVDD18 1 ≤ Sampling frequency ≤ 105 MSPS		0.76		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from 20% to 80% of DVDD18 Fall time measured from 80% to 20% of DRVDD 1 ≤ Sampling frequency ≤ 105 MSPS		0.74		ns

(6) For Fs > 105 MSPS, it is recommended to use external clock for data capture and NOT the device output clock signal (ADC_DCLKOUT).
(7) For Fs > 65MSPS, CMOS output buffers strength is increased by writing serial register bits STR_CTRL<1:0> = '10'.

(8) Data valid refers to LOGIC HIGH of 1.26 V and LOGIC LOW of 0.54 V.

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Table 3-1. LVDS Timings at Lower Sampling Frequencies

2-WIRE MODE DDR CLOCK						
Sampling Frequency, MSPS	Setup time, ns			Hold time, ns		
	MIN	TYP	MAX	MIN	TYP	MAX
20	3.75	3.93		3.64	3.9	
35	1.99	2.18		1.96	2.2	
50	1.28	1.46		1.28	1.51	
65	0.84	1.06		0.85	1.14	
80	0.59	0.81		0.70	0.90	
95	0.46	0.67		0.49	0.70	
110	0.31	0.52		0.36	0.58	
125	0.29	0.42		0.30	0.47	
Fs ≤ 125MSPS	Clock propagation delay, $t_{PDI} = t_{DELAY}$			t_{DELAY}, ns		
	11.5	13.8	15.5	11.5	13.8	15.5
2-WIRE MODE, SDR CLOCK						
Sampling Frequency, MSPS	Setup time, ns			Hold time, ns		
	MIN	TYP	MAX	MIN	TYP	MAX
10	8.14	8.32		7.90	8.06	
20	3.89	4.08		3.85	4.01	
30	2.33	2.6		2.51	2.71	
40	1.68	1.91		1.81	2.03	
50	1.22	1.48		1.41	1.64	
65	0.85	1.08		1.08	1.21	
Fs ≤ 65MSPS	Clock propagation delay, $t_{PDI} = 0.5*Ts + t_{DELAY}$			t_{DELAY}, ns		
				11.5	14	16.5
1-WIRE MODE, DDR CLOCK						
Sampling Frequency, MSPS	Setup time, ns			Hold time, ns		
	MIN	TYP	MAX	MIN	TYP	MAX
20	1.71	1.90		1.67	1.92	
35	0.77	0.99		0.82	1.04	
50	0.36	0.61		0.39	0.62	
65	0.25	0.39		0.26	0.40	
Fs ≤ 65MSPS	Clock propagation delay, $t_{PDI} = 0.5*Ts + t_{DELAY}$			t_{DELAY}, ns		
				MIN	TYP	MAX
				11.50	13.50	15.50

Table 3-2. CMOS Timings at Lower Sampling Frequencies

Sampling Frequency, MSPS	Timings specified with respect to CLKOUT					
	Setup time, ns			Hold time, ns		
	MIN	TYP	MAX	MIN	TYP	MAX
20	10.90	11.50		11.22	11.60	
40	4.62	5.25		4.99	5.33	
65	2.06	2.66		2.46	2.86	
90	1	1.9		1.8	2.3	
105	0.5	1.4		1.4	1.8	
Fs ≤ 105MSPS	Clock propagation delay, $t_{PDI} = 0.5*Ts + t_{DELAY}$			t_{DELAY}, ns		
				MIN	TYP	MAX
				14	16.50	19

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3.13 TIMING REQUIREMENTS FOR TRANSMIT PATH – LVDS AND CMOS MODES(1)

Typical values are at 25°C, AVDD3_DAC = 3.0 V, AVDD3_AUX = 3.0 V, AVDD18_ADC = 1.8 V, DVDD18_CLK = 1.8 V, DVDD18_DAC = 1.8 V, DVDD18 = 1.8 V, sine wave input clock, 1.5 V_{pp} clock amplitude, unless otherwise noted. Min and max values are across the full temperature range T_{MIN} = -40°C to T_{MAX} = 85°C, AVDD3_DAC = 3.0 V, AVDD3_AUX = 3.0 V, AVDD18_ADC = 1.8 V, DVDD18_CLK = 1.8 V, DVDD18_DAC = 1.8 V, DVDD18 = 1.7 V to 1.9 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC Latency		Default Mode		16		clock cycles
LVDS INPUT INTERFACE						
t_{su}	Data setup time	Data valid(2) to zero-crossing of DAC_DCLKINP	0.5			ns
t_h	Data hold time	Zero-crossing of DAC_DCLKINP to data becoming invalid (2)	0.3			ns
CMOS INPUT INTERFACE						
t_{su}	Data setup time	Data valid to cross-over of DAC_DCLKIN (3)	0.3			ns
t_h	Data hold time	Cross-over of DAC_DCLKIN to data becoming invalid (3)	0.5			ns

(1) Timing parameters are ensured by design and characterization and not tested in production.
(2) Data valid refers to LOGIC HIGH of +100 mV and LOGIC LOW of -100 mV.
(3) Data valid refers to LOGIC HIGH of 1.26 V and LOGIC LOW of 0.54 V.

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4 SERIAL PERIPHERAL INTERFACE

4.1 DESCRIPTION

The SPI (serial peripheral interface) is used to program the AFE7225/7222. It is used to read data from and write data to the registers, from the rms/peak power meter and the auxiliary ADC. It is also used to send data to the auxiliary DACs.

The interface is formed with pins SEN (Serial Interface Enable), SCLK (Serial Interface Clock), SDATA (Serial interface input data) and SDOUT (Serial interface output data).

The serial shift of bits into the device is enabled when SEN is low. Serial data SDATA is latched at every rising edge of SCLK when SEN is active (low). The SPI uses a 20-bit serial arrangement – the first 12-bits are the register address, and the last 8-bits represent the data for the address.

The interface can work with SCLK frequency from a frequency of 40MHz down to a few Hertz and also with non-50% SCLK duty cycle.

Direct access modes exist for reading from the auxiliary ADC and writing to the auxiliary DACs by using the SPI pins.

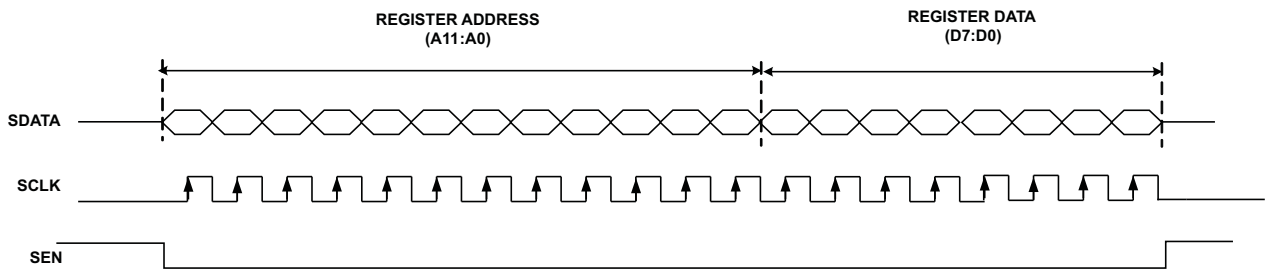

Figure 4-1. Timing

Address bits (A11:A8) are referred to as the Page address of the register, and address bits (A7:A0) are referred to as the Row address of the register.

4.2 SPI REGISTER READOUT

Data stored in a register corresponding to a page can be read out by programming the readout bit corresponding to that page. The read out bit for a register addressed by (A11:A0) is the D0 bit of the register with the Page address of (A11:A8) and row address of 00000000.

To read out a particular register, the following steps have to be followed:

1. Configure SDOUT as a digital output pin using bits
2. Set the register specific readout bit. This bit can be set by writing the following 20-bit sequence – A11:A8,00000000,00000001 where (A11..A8) is the page address of the register whose contents are desired to be read out
3. Once in the readout mode, write the address of the register to be readout as below. The new data write is ignored. The data contents of the register come out serially on the SDOUT pin (with MSB first format) as shown below.

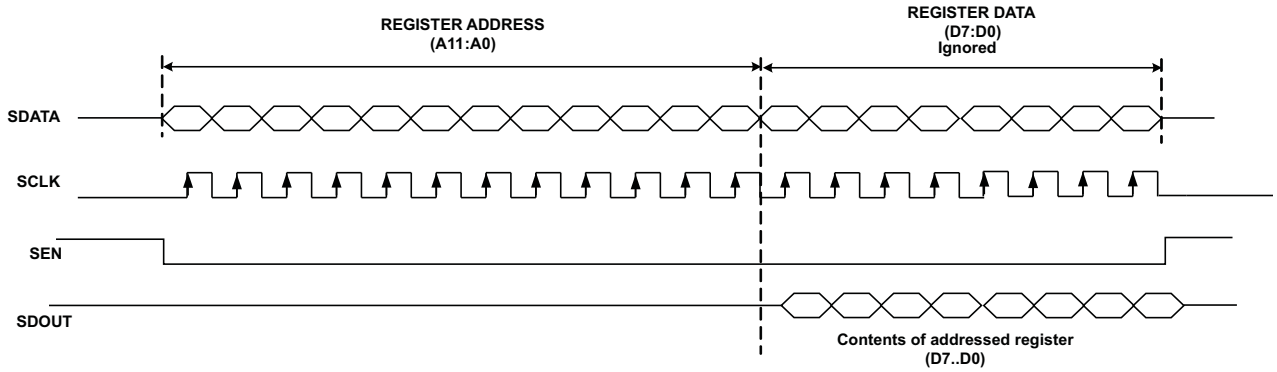

Figure 4-2. Timing

4. If the next register to be read out has the same page address, then repeat Step 3 with the new address to be read out.
5. To exit the register readout mode, write A11:A8,00000000,00000000.

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5 REGISTER DESCRIPTIONS

5.1 TRANSMIT DIGITAL SIGNAL CHAIN REGISTERS

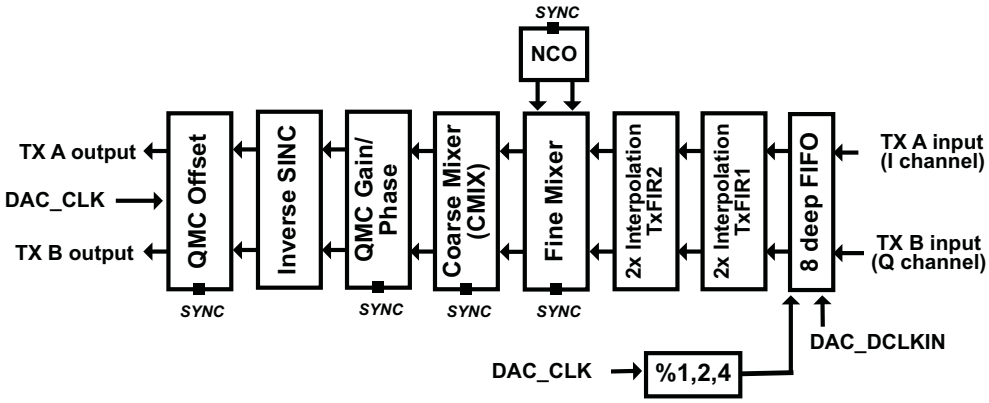

Figure 5-1. Signal Chain

Input data is shifted into the 8-deep FIFO at the rate of DAC_DCLKIN. At its output, the FIFO hands off the data using a divided version of the DAC_CLK (based on the interpolation factor). The rest of the signal chain runs off DAC_CLK and its divided derivatives.

Register Name – CONFIG0 – Address 0x103, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
	Tx_BYP_SRC	TX_BYP	TX_ChB_PDN_SRC	TX_CHB_PDN	TX_CHA_PDN_SRC	TX_CHA_PDN	TX_DIS

TX_DIS – Disables the digital signal chain of both channels in TX . All blocks in digital signal chain are powered down, and the output is DAC mid-code. Note: the DACs are not powered down in this mode.

TX_CHA_PDN – Powers down digital signal chain of Channel A in Tx . Output of the channel is mid code. Set **TX_CHA_PDN_SRC** for this to take effect.

TX_CHA_PDN_SRC – Setting this causes the value programmed into **TX_CHA_PDN** to take effect.

TX_CHB_PDN – Powers down digital signal chain of Channel B in Tx . Output of the channel is mid code. Set **TX_CHB_PDN_SRC** for this to take effect.

TX_CHB_PDN_SRC – Setting this causes the value programmed into **TX_CHB_PDN** to take effect.

Note that when in default mode of operation (none of the register-selectable digital features enabled), all 4 of above bits (TX_CHA_PDN, TX_CHA_PDN_SRC, TX_CHB_PDN, TX_CHB_PDN_SRC) have to be set together to '1' for them to take effect. However, if any of the digital features (like interpolation, Fine mixer, Coarse mixer, or QMC gain/phase or offset) are enabled, then the channel A can be independently powered down using bits TX_CHA_PDN and TX_CHA_PDN_SRC, and channel B can be independently powered down using bits TX_CHB_PDN and TX_CHB_PDN_SRC.

TX_BYP – The inputs to both the Tx channels are directly passed to the outputs. FIFO is bypassed. Set **TX_BYP_SRC** for this to take effect.

TX_BYP_SRC – Setting this causes the value programmed into **TX_BYP** to take effect.

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Register Name – CONFIG1 – Address 0x104, Default = 0x10

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MASK_2_AWAY_DET	TX_CHB_8_IP_EN	TX_CHA_8_IP_EN					

TX_CHA_8_IP_EN – Enable the 8- sample mode FIFO mode for Channel A . The 8 samples written into the regs 0x11F to 0x12E are repeatedly cycled through, and sent to the DAC A. This is a useful diagnostic mode.

TX_CHB_8_IP_EN – Enable the 8- sample mode FIFO mode for Channel B . The 8 samples written into the regs 0x12F to 0x13E are repeatedly cycled through, and sent to the DAC B.

MASK_2_AWAY_DET – Refer CONFIG58 for a description of the collision condition in the FIFO. Setting the MASK_2_AWAY_DET prevents the 2-away condition from triggering collision detection. If collision detection is enabled, and 2-away condition occurs, the output samples will be forced to DAC mid code, unless **MASK_2_AWAY_DET** is set.

Register Name – CONFIG2 – Address 0x105, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
				STORE_FIFO_PTRS		RX_TX_LPBK_SRC	RX_TX_LPBK

STORE_FIFO_PTRS – When set , the FIFO Read and Write pointers are written into the register 0x141 at the rate of the divided DAC_CLK. The pointers are no longer written to the serial interface regs when Register readout is enabled.

RX_TX_LPBK – When this bit and RX_TX_LPBK_SRC are both set , the input to the TX signal chain is tapped from the the final output of the RX signal chain. As is obvious, the ADC_CLK and DAC_CLK rates should be the same when using this mode.

RX_TX_LPBK_SRC – When this bit and RX_TX_LPBK are both set , the input to the TX signal chain is tapped from the the final output of the RX signal chain

The RX to TX loopback is shown below. The dotted arrows illustrate the loopback path.

Note that though the data going into the TX digital signal chain is looped back internally from the RX Digital signal chain, it is still required to give an active DAC_DCLKIN in this mode because the Tx FIFO requires it for proper data transfer.

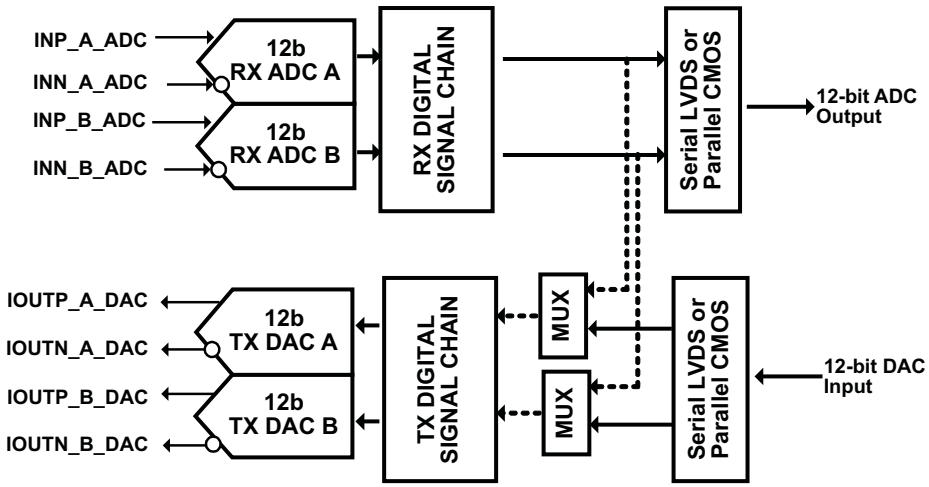

Figure 5-2. Loopback

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Register Name – CONFIG3 – Address 0x106, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
	FIR2B_MODE	FIR1B_MODE	FIR2A_MODE	FIR1A_MODE	TX_INT_MODE_SRC	TX_INT_MODE(1:0)	

TX_INT_MODE(1:0) – Specifies the interpolation factor. To use this mode, set TX_INT_MODE_SRC to 1.

VALUE	INTERPOLATION FACTOR
0	1
1	2
2	4
3	4

While interpolating by a factor of 2, the DAC_DCLKIN rate should be set to half of the DAC_CLK rate. While interpolating by a factor of 4, the DAC_DCLKIN rate should be set to one fourth of the DAC_CLK rate. In interpolate by 2 mode , TxFIR1 alone is used. In Interpolate by 4 mode, both TxFIR1, and TxFIR2 are used.

TX_INT_MODE_SRC – Needs to be set to 1 when programming TX_INT_MODE(1:0)

FIR1A_MODE – Specifies whether TxFIR1 in Channel A is in low pass or high pass mode . Set this bit to configure the filter in high pass mode. In interpolate by 4 mode, always set TxFIR1 to low pass mode.

FIR2A_MODE – Specifies whether TxFIR2 in Channel A is in low pass or high pass mode. Set this bit to configure the filter in high pass mode

FIR1B_MODE – Specifies whether TxFIR1 in Channel B is in low pass or high pass mode. Set this bit to configure the filter in high pass mode

FIR2B_MODE – Specifies whether TxFIR2 in Channel B is in low pass or high pass mode . Set this bit to configure the filter in high pass mode

Register Name – CONFIG4 – Address 0x107, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
		TX_CMIX_PHASE(1:0)		TX_CMIX_PHASE_INCR	TX_CMIX_MODE(1:0)		TX_CMIX_EN

TX_CMIX_EN – Enables the Tx Coarse Mixer.

TX_CMIX_MODE (1:0) – Specifies the mode in which the TX CMIX is configured. Set **TX_CMIX_EN** for this to take effect.

VALUE	MIXING MODE
0	Normal(Low pass)
1	Fs /2 (High Pass) – real mixing mode
2	+ Fs/4 – complex mixing mode
3	– Fs/4 – complex mixing mode

TX_CMIX_PHASE_INCR – This bit is a method to control the mixing phase without using the SYNC pin. A 0 to 1 transition on this bit causes the phase of mixing in the TX CMIX to be incremented by 1 with respect to the current phase of mixing. To increment the phase of mixing more than once, clear and then set this bit once again. Syncing needs to be disabled for Tx CMIX for this mode to work. (This means that global syncing should be disabled, and CMIX-specifc syncing should also be disabled).

TX_CMIX_PHASE (1:0) – The value programmed into this is applied as the current TX CMIX phase, when the CMIX is synced, Syncing needs to be enabled for CMIX for this mode to work. This mode is meant to synchronize the phase of mixing across multiple chips.

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Register Name – CONFIG5 – Address 0x108, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
Tx_INV_SINC_FIL_EN_SRC	Tx_INV_SINC_FIL_EN	TX_DIV_PHASE_ INCR	TX_DIV_PHASE(1:0)		TX_DATA_ROUTE_ ORDER (1:0)		

TX_DATA_ROUTE_ORDER (1:0) – Specifies the order in which the A and B outputs of the TX Signal Chain are routed to the DACs

VALUE	ROUTING ORDER
0	Normal – DACA gets TX Output A and DACB gets TX Output B
1	Both DACs get TX Output A
2	Both DACs get TX Output B
3	Swapped – DACA gets TX Output B and DACB gets TX Output A

TX_DIV_PHASE (1:0) – The value programmed into this is applied as the TX Divider phase, when the divider is synced. The divider here refers to the clock divider that divides the DAC_CLK depending on the interpolation factor. For division by 2, there are 2 possible phases of the divided clock. For division by 4, there are 4 possible phases. If the divider phase is not synced across chips, then it will cause a phase uncertainty in the DAC analog output, and can also cause uncertainty in the CMIX operation.

TX_DIV_PHASE_INCR – This bit is a method to control the phase of the divided clock without using the SYNC pin. A 0 to 1 transition on this bit causes the phase of division in the TX Divider to be incremented by 1 with respect to the current phase of division. To increment the phase of division more than once, clear and then set this bit once again. Global syncing as well as Syncing for the Tx Divider needs to be disabled for this mode to work.

Tx_INV_SINC_FIL_EN – Enables the Tx Inverse Sinc Filter. Set **Tx_INV_SINC_FIL_EN_SRC** for this to take effect.

Tx_INV_SINC_FIL_EN_SRC – When set, this allows **Tx_INV_SINC_FIL_EN** to take effect.

Register Name – CONFIG6 – Address 0x10B, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
TX_CMIX_SYNC_ SRC		TX_GLOBAL_ SYNC_DIS	TX_QMC_GAIN_PH_ SYNC_DIS	TX_QMC_OFF_ SYNC_DIS	TX_DIV_ SYNC_DIS	TX_CMIX_ SYNC_DIS	TX_FIFO_ SYNC_DIS

TX_FIFO_SYNC_DIS – Disables Syncing of the FIFO. This takes effect only when TX_GLOBAL_SYNC_DIS is set. This is only a enable/ disable bit – the actual sync source can be set to pin or serial interface. When the FIFO is synced, the read and write pointers are initialized such that they are separated by 4 positions.This mode is common for both channels.

TX_CMIX_SYNC_DIS – Disables Syncing of the Tx CMIX .This takes effect only when TX_GLOBAL_SYNC_DIS is set. CMIX syncing refers to setting the phase of the complex mixing. This mode is common for both channels.

TX_DIV_SYNC_DIS – Disables Syncing of the Tx Divider phase .This takes effect only when TX_GLOBAL_SYNC_DIS is set. Common for both channels.

TX_QMC_OFF_SYNC_DIS – Disables Syncing of Tx QMC Offset Correction .This takes effect only when TX_GLOBAL_SYNC_DIS is set. This mode is common for both channels.

TX_QMC_GAIN_PH_SYNC_DIS – Disables Syncing of Tx QMC Gain Phase Correction .This takes effect only when TX_GLOBAL_SYNC_DIS is set. This mode is common for both channels.

TX_GLOBAL_SYNC_DIS – When set, disables global syncing of TX and enables block level syncing. When cleared, a rising edge on the selected sync source causes all TX blocks to be synced.

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TX_CMIX_SYNC_SRC – Specifies the sync source for TX CMIX. When cleared, SYNC pin is used as the sync source. When set, a rising edge on serial interface bit TX_CMIX_SER_IF_SYNC in Register 0x10D is used as the sync source for TX CMIX. This is applicable when **TX_GLOBAL_SYNC_DIS** is set and **TX_CMIX_SYNC_DIS** is cleared.

VALUE	SYNC SOURCE
0	Pin
1	Serial interface bit

Register Name – CONFIG7 – Address 0x10C, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
		TX_GLOBAL_ SYNC_SRC	TX_QMC_GAIN_PH_ SYNC_SRC	TX_QMC_OFF_SYNC_ SRC	TX_DIV_SYNC_ SRC		TX_FIFO_SYNC_ SRC

TX_FIFO_SYNC_SRC – Specifies the Sync source for TX FIFO. It is applicable when **TX_GLOBAL_SYNC_DIS** is set and **TX_FIFO_SYNC_DIS** is cleared.

VALUE	SYNC SOURCE
0	Pin
1	Serial interface bit

When the value programmed is 1, a rising edge on the serial interface bit **TX_FIFO_SER_IF_SYNC** in register 0x10D is used as the sync source for the FIFO.

TX_DIV_SYNC_SRC – Specifies the sync source for TX Divider. When cleared, SYNC pin is used as the sync source. When set, a rising edge on serial interface bit TX_DIV_SER_IF_SYNC in register 0x10D is used as the sync source for TX Divider. This is applicable when **TX_GLOBAL_SYNC_DIS** is set and **TX_DIV_SYNC_DIS** is cleared.

TX_QMC_OFF_SYNC_SRC – Specifies the sync source for TX QMC Offset Correction. When cleared, SYNC pin is used as the sync source. When set, a rising edge on serial interface bit TX_QMC_OFF_SER_IF_SYNC in register 0x10D is used as the sync source for TX QMC Offset Correction. This is applicable when **TX_GLOBAL_SYNC_DIS** is set and **TX_QMC_OFF_SYNC_DIS** is cleared.

TX_QMC_GAIN_PH_SYNC_SRC – Specifies the sync source for TX QMC Gain Phase Correction. When cleared, SYNC pin is used as the sync source. When set, a rising edge on serial interface bit TX_QMC_GAIN_PH_SER_IF_SYNC in register 0x10D is used as the sync source for TX QMC Gain Phase Correction. This is applicable when **TX_GLOBAL_SYNC_DIS** is set and **TX_QMC_GAIN_PH_SYNC_DIS** is cleared.

TX_GLOBAL_SYNC_SRC – Specifies the sync source for TX. This is applicable when **TX_GLOBAL_SYNC_DIS** is cleared.

VALUE	SYNC SOURCE
0	All blocks synced from the SYNC pin
1	All blocks synced using serial Interface bit

When serial interface is specified to be the sync source, a rising edge on the serial interface bit **TX_GLOB_SER_IF_SYNC** in register 0x10D is used as the sync source.

Register Name – CONFIG8 – Address 0x10D, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
	TX_GLOBAL_SER_IF_SYNC		TX_QMC_GAIN_PH_SER_IF_SYNC	TX_QMC_OFF_SER_IF_SYNC	TX_DIV_SER_IF_SYNC	TX_CMIX_SER_IF_SYNC	TX_FIFO_SER_IF_SYNC

TX_FIFO_SER_IF_SYNC – A rising edge on this bit is used as the sync source for TX FIFO. This is applicable when **TX_GLOBAL_SYNC_DIS** is set, and **TX_FIFO_SYNC_DIS** is cleared, and **TX_FIFO_SYNC_SRC** specifies serial interface bit to be the sync source for the FIFO.

TX_CMIX_SER_IF_SYNC – A rising edge on this bit is used as the sync source for TX CMIX. This is applicable when **TX_GLOBAL_SYNC_DIS** is set, and **TX_CMIX_SYNC_DIS** is cleared, and **TX_CMIX_SYNC_SRC** specifies serial interface bit to be the sync source for the TX CMIX.

TX_DIV_SER_IF_SYNC – A rising edge on this bit is used as the sync source for TX Divider. This is applicable when **TX_GLOBAL_SYNC_DIS** is set, and **TX_DIV_SYNC_DIS** is cleared, and **TX_DIV_SYNC_SRC** specifies serial interface bit to be the sync source for the TX Divider.

TX_QMC_OFF_SER_IF_SYNC – A rising edge on this bit is used as the sync source for TX QMC Offset correction block. This is applicable when **TX_GLOBAL_SYNC_DIS** is set, and **TX_QMC_OFF_SYNC_DIS** is cleared, and **TX_QMC_OFF_SYNC_SRC** specifies serial interface bit to be the sync source for the TX QMC Offset correction.

TX_QMC_GAIN_PH_SER_IF_SYNC – A rising edge on this bit is used as the sync source for TX QMC Gain Phase correction block. This is applicable when **TX_GLOBAL_SYNC_DIS** is set, and **TX_QMC_GAIN_PH_SYNC_DIS** is cleared, and **TX_QMC_GAIN_PH_SYNC_SRC** specifies serial interface bit to be the sync source for the TX QMC Gain Phase correction.

TX_GLOBAL_SER_IF_SYNC – A rising edge on this is used as the sync source for TX. This is applicable when **TX_GLOBAL_SYNC_DIS** is cleared, and **TX_GLOBAL_SYNC_SRC(1:0)** specifies serial interface bit to be the sync source for TX.

Register Name – CONFIG9 – Address 0x10E, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
TX_QMC_CORR_ENA	TX_QMC_OFFSET_ENA					TX_QMC_GAIN_PH_SYNC_NEEDED	TX_QMC_OFF_SYNC_NEEDED

TX_QMC_OFF_SYNC_NEEDED – Specifies if syncing is needed for TX QMC Offset Correction . If set, QMC Offset values programmed in the serial interface registers are not applied to the QMC Offset correction block until a sync is applied.

TX_QMC_GAIN_PH_SYNC_NEEDED – Specifies if syncing is needed for TX QMC Gain Phase Correction. If set, QMC gain and Phase values programmed into the serial interface registers are not applied to the QMC Gain Phase correction block until a sync is applied.

TX_QMC_OFFSET_ENA – Enables TX QMC Offset Correction. Common for both channels.

TX_QMC_CORR_ENA – Enable TX QMC Gain Phase Correction. Common for both channels. Note that by default, the TX_QMC_GAINA(2:0) and TX_QMC_GAINB(2:0) are set to 0. So when TX_QMC_CORR_ENA is written, the output goes to zero until the time TX_QMC_GAINA(2:0) and TX_QMC_GAINB(2:0) are written to the desired value.

Register Name – CONFIG10 – Address 0x10F Default = 0x00 (Optionally Synced)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
TX_QMC_OFFSETA(12:5)							

TX_QMC_OFFSETA(12:5) – Upper 8 bits of DAC A Offset Correction . The lower 5 bits are in **CONFIG11** Register. Offset is a signed value (2s complement).

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Register Name – CONFIG11 – Address 0x110 Default = 0x00 (Optionally Synced)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
TX_QMC_OFFSETA(4:0)					TX_QMC_GAINA(2:0)		

TX_QMC_OFFSETA(4:0) – Lower 5 bits of DAC A Offset Correction .

TX_QMC_GAINA(2:0) – Lower 3 bits of the 11 bit QMC Gain word for DAC A. The upper 8 bits are in **CONFIG12** register.The full 11 bit TX_QMC_GAINA(10:0) word is formatted as UNSIGNED with a range or 0 to 1.9990 . The implied decimal point for the multiplication is between bits (9) and (10).

Register Name – CONFIG12 – Address 0x111 Default = 0x00 (Synced)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
TX_QMC_GAINA(10:3)							

TX_QMC_GAINA(10:3) –Upper 8 bits if the 11 bit QMC Gain word for DAC A.

Register Name – CONFIG13 – Address 0x112 Default = 0x00 (Synced)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
TX_QMC_OFFSETB(12:5)							

TX_QMC_OFFSETB(12:5) –Upper 8 bits of DAC B Offset Correction. The lower 5 bits are in **CONFIG14** Register.

Register Name – CONFIG14 – Address 0x113 Default = 0x00 (Synced)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
TX_QMC_OFFSETB(4:0)					TX_QMC_GAINB(2:0)		

TX_QMC_OFFSETB(4:0) – Lower 5 bits of DAC B Offset Correction .

TX_QMC_GAINB(2:0) – Lower 3 bits of the 11 bit QMC Gain word for DAC B. The upper 8 bits are in **CONFIG15** register.The full 11 bit TX_QMC_GAINB(10:0) word is formatted as UNSIGNED with a range or 0 to 1.9990.

Register Name – CONFIG15 – Address 0x114 Default = 0x00 (Synced)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
TX_QMC_GAINB(10:3)							

TX_QMC_GAINB(10:3) – Upper 8 bits if the 11 bit QMC Gain word for DAC B.

Register Name – CONFIG16 – Address 0x115 Default = 0x00 (Synced)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
TX_QMC_PHASE(9:2)							

TX_QMC_PHASE(9:2) – Upper Upper 8 bits if the 10 bit QMC Phase word. The lower two bits are in the **CONFIG17** register. The full QMC_PHASE(9:0) correction word is formatted as 2s complement and scaled to occupy a range of -0.125 to 0.12475. To acomplish QMC Phase correction, this value is multiplied by the current Q sample, then summed to the I sample.

Register Name – CONFIG17 – Address 0x116 Default = 0x00 (Synced)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
						TX_QMC_PHASE(1:0)	

TX_QMC_PHASE(1:0) – Lower 2 bits of the 10 bit QMC Phase word .

Register Name – CONFIG18 – Address 0x117 Default = 0x00 (Synced)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
TX_NCO_FREQ_WORD(31:24)							

TX_NCO_FREQ_WORD(31:24) – See CONFIG21 below.

Register Name – CONFIG19 – Address 0x118 Default = 0x00 (Synced)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
TX_NCO_FREQ_WORD(23:16)							

TX_NCO_FREQ_WORD(23:16) – See CONFIG21 below.

Register Name – CONFIG20 – Address 0x119 Default = 0x00 (Synced)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
TX_NCO_FREQ_WORD(15:8)							

TX_NCO_FREQ_WORD(15:8) – See CONFIG21 below.

Register Name – CONFIG21 – Address 0x11A Default = 0x00 (Synced)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
TX_NCO_FREQ_WORD(7:0)							

TX_NCO_FREQ_WORD(7:0) – This is used to determine the frequency, F_{mix} of the NCO. The twos complement formatted value can be positive or negative, and the LSB is equal to $Fs/2^{32}$

Register Name – CONFIG22 – Address 0x11B Default = 0x00 (Synced)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
TX_NCO_PHASE_OFF(15:8)							

TX_NCO_FREQ_WORD(15:8) – See CONFIG23 below.

Register Name – CONFIG23 – Address 0x11C Default = 0x00 (Synced)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
TX_NCO_PHASE_OFF(7:0)							

TX_NCO_PHASE_OFF(7:0) – This is the 2s complement Phase offset added to the NCO accumulator just before the generation of the SIN and COS values.

Register Name – CONFIG24 – Address 0x11D, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
				TX_MIXER_EN	TX_MIXER_GAIN(1:0)		

TX_MIXER_GAIN(1:0) – The fine mixer realizes the functions $\{A\cos(\omega_{mix}t) - B\sin(\omega_{mix}t)\}$ and $\{A\sin(\omega_{mix}t) + B\cos(\omega_{mixt})\}$ This can cause the fine mixer output to be up to 3 dB higher than the individual inputs.The mixer gain can restore the signal level to the desired level by providing a programmable attenuation.

VALUE	GAIN
0	–2.5 dB (default) – use when complex mixing
1	–6 dB
2	0 dB – use when one input is zero
3	0 dB

TX_MIXER_EN – This enables the fine mixer, which also causes the NCO to be enabled.

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Register Name – CONFIG25– Address 0x11E Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
TX_NCO_SYNC_ DIS	TX_NCO_SYNC_ SRC	TX_NCO_SER_IF_ SYNC	TX_NCO_SYNC_ NEEDED				

TX_NCO_SYNC_NEEDED – Specifies if syncing is needed for TX NCO. If set, NCO Frequency and Offset words programmed into the serial interface registers are not applied to the NCO until a sync is applied

TX_NCO_SER_IF_SYNC – A rising edge on this bit is used as the sync source for TX NCO. This is applicable when **TX_GLOBAL_SYNC_DIS** is set, and **TX_NCO_SYNC_DIS** is cleared, and **TX_NCO_SYNC_SRC** specifies serial interface bit to be the sync source for the NCO.

TX_NCO_SYNC_SRC – Specifies the sync source for TX NCO. When cleared, SYNC pin is used as the sync source. When set, a rising edge on serial interface bit TX_NCO_SER_IF_SYNC is used as the sync source for TX NCO. This is applicable when **TX_GLOBAL_SYNC_DIS** is set.

TX_NCO_SYNC_DIS – Disables Syncing of the Tx NCO. This takes effect only when TX_GLOBAL_SYNC_DIS is set.

Register Name – CONFIG26 – Address 0x11F, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHA_REG1(15:8)							

CHA_REG1(15:8) – Upper 8 bits for sample 1 for DAC A in 8-sample FIFO mode . **TX_CHA_8_IP_EN** in CONFIG 1 needs to be set for Regs CONFIG26 to CONFIG41 to take effect.

Register Name – CONFIG27 – Address 0x120, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHA_REG1(7:0)							

CHA_REG1(7:0) – Lower 8 bits for sample 1 for DAC A

Register Name – CONFIG28 – Address 0x121, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHA_REG2(15:8)							

CHA_REG2(15:8) – Upper 8 bits for sample 2 for DAC A .

Register Name – CONFIG29 – Address 0x122, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHA_REG2(7:0)							

CHA_REG2(7:0) – Lower 8 bits for sample 2 for DAC A

Register Name – CONFIG30 – Address 0x123, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHA_REG3(15:8)							

CHA_REG3(15:8) – Upper 8 bits for sample 3 for DAC A

Register Name – CONFIG31 – Address 0x124, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHA_REG3(7:0)							

CHA_REG3(7:0) – Lower 8 bits for sample 3 for DAC A

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Register Name – CONFIG32 – Address 0x125, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHA_REG4(15:8)							

CHA_REG4(15:8) – Upper 8 bits for sample 4 for DAC A .

Register Name – CONFIG33 – Address 0x126, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHA_REG4(7:0)							

CHA_REG4(7:0) – Lower 8 bits for sample 4 for DAC A

Register Name – CONFIG34 – Address 0x127, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHA_REG5(15:8)							

CHA_REG5(15:8) – Upper 8 bits for sample 5 for DAC A

Register Name – CONFIG35 – Address 0x128, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHA_REG5(7:0)							

CHA_REG5(7:0) – Lower 8 bits for sample 5 for DAC A .

Register Name – CONFIG36 – Address 0x129, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHA_REG6(15:8)							

CHA_REG6(15:8) – Upper 8 bits for sample 6 for DAC A

Register Name – CONFIG37 – Address 0x12A, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHA_REG6(7:0)							

CHA_REG6(7:0) – Lower 8 bits for sample 6 for DAC A

Register Name – CONFIG38 – Address 0x12B, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHA_REG7(15:8)							

CHA_REG7(15:8) – Upper 8 bits for sample 7 for DAC A

Register Name – CONFIG39 – Address 0x12C, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHA_REG7(7:0)							

CHA_REG7(7:0) – Lower 8 bits for sample 7 for DAC A.

Register Name – CONFIG40 – Address 0x12D, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHA_REG8(15:8)							

CHA_REG8(15:8) – Upper 8 bits for sample 8 for DAC A

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Register Name – CONFIG41 – Address 0x12E, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHA_REG8(7:0)							

CHA_REG8(7:0) – Lower 8 bits for sample 8 for DAC A

Register Name – CONFIG42 – Address 0x12F, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHB_REG1(15:8)							

CHB_REG1(15:8) – Upper 8 bits for sample 1 for DAC B . **TX_CHB_8_IP_EN** in CONFIG 1 needs to be set for Regs CONFIG42 to CONFIG57 to take effect.

Register Name – CONFIG43 – Address 0x130, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHB_REG1(7:0)							

CHB_REG1(7:0) – Lower 8 bits for sample 1 for DAC B

Register Name – CONFIG44 – Address 0x131, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHB_REG2(15:8)							

CHB_REG2(15:8) – Upper 8 bits for sample 2 for DAC B.

Register Name – CONFIG45 – Address 0x132, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHB_REG2(7:0)							

CHB_REG2(7:0) – Lower 8 bits for sample 2 for DAC B

Register Name – CONFIG46 – Address 0x133, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHB_REG3(15:8)							

CHB_REG3(15:8) – Upper 8 bits for sample 3 for DAC B.

Register Name – CONFIG47 – Address 0x134, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHB_REG3(7:0)							

CHB_REG3(7:0) – Lower 8 bits for sample 3 for DAC B

Register Name – CONFIG48 – Address 0x135, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHB_REG4(15:8)							

CHB_REG4(15:8) – Upper 8 bits for sample 4 for DAC B.

Register Name – CONFIG49 – Address 0x136, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHB_REG4(7:0)							

CHB_REG4(7:0) – Lower 8 bits for sample 4 for DAC B.

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Register Name – CONFIG50 – Address 0x137, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHB_REG5(15:8)							

CHB_REG5(15:8) – Upper 8 bits for sample 5 for DAC B.

Register Name – CONFIG51 – Address 0x138, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHB_REG5(7:0)							

CHB_REG5(7:0) – Lower 8 bits for sample 5 for DAC B

Register Name – CONFIG52 – Address 0x139, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHB_REG6(15:8)							

CHB_REG6(15:8) – Upper 8 bits for sample 6 for DAC B.

Register Name – CONFIG53 – Address 0x13A, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHB_REG6(7:0)							

CHB_REG6(7:0) – Lower 8 bits for sample 6 for DAC B.

Register Name – CONFIG54 – Address 0x13B, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHB_REG7(15:8)							

CHB_REG7(15:8) – Upper 8 bits for sample 7 for DAC B.

Register Name – CONFIG55 – Address 0x113C, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHB_REG7(7:0)							

CHB_REG7(7:0) – Lower 8 bits for sample 7 for DAC B

Register Name – CONFIG56 – Address 0x13D, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHB_REG8(15:8)							

CHB_REG8(15:8) – Upper 8 bits for sample 8 for DAC B.

Register Name – CONFIG57 – Address 0x13E, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CHB_REG8(7:0)							

CHB_REG8(7:0) – Lower 8 bits for sample 8 for DAC B

Register Name – CONFIG58 – Address 0x13F, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
EN_IP_CLK_STOP_DET	EN_FIFO_COLLISION_DET						

EN_FIFO_COLLISION_DET – On RESET (and when synced), the read and write pointers of the FIFO are set 4 positions away. The read pointer increments at the DAC_DCLKIN rate whereas the write pointer increments at the divided DAC_CLK rate. While the frequencies of these 2 clocks are expected to be the same, relative phase drifts can cause this relative difference of 4 positions to drift. When the EN_FIFO_COLLISION_DET bit is set, a collision condition is detected when the relative difference

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between the read and write pointers becomes either 0,1 or 2. Detection of this collision condition automatically causes masks the DACs to give out an output corresponding to mid code. The read and write pointer differing by 2 is referred to as 2-way detection. 2-away detection can be prevented from triggering collision by setting **MASK_2_AWAY_DET** in CONFIG 1. Collision detection is done once every 8 input samples.

EN_IP_CLK_STOP_DET – When set, the condition of input clock being stopped causes the DAC outputs to be forced to mid code.

Register Name – CONFIG59 – Address 0x140, Default = 0x00 (Read Only)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
FIFO_ERROR	FIFO_COLLISION	FIFO_1_AWAY	FIFO_2_AWAY	INP_CLK_STOP			

These are refreshed at the rate of the divided DAC_CLK.

INP_CLK_STOP – If set, it indicates that the input clock has been detected as having been stopped.

FIFO_2_AWAY – If set, it indicates that the condition of the read and write pointers being 2 locations away from each other has been detected.

FIFO_1_AWAY – If set, it indicates that the condition of the read and write pointers being 1 location away from each other has been detected.

FIFO_COLLISION – If set, this indicates that the read and write pointers have been detected as overlapping with each other

FIFO_ERROR – If set, this indicates that either Collision , or 1-away or 2-away condition has been detected.

Register Name – CONFIG60 – Address 0x141, Default = 0x00 (Read Only)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
FIFO_INP_PTR(2:0)			FIFO_OP_PTR(2:0)				

FIFO_OP_PTR(2:0) – Containts the FIFO read pointer value. Its written into the register when **STORE_FIFO_PTRS** is set in CONFIG2. It is not updated once the device is configured into readout mode.

FIFO_INP_PTR(2:0) – Containts the FIFO write pointer value. Its written into the register when **STORE_FIFO_PTRS** is set in CONFIG2. It is not updated once the device is configured into readout mode.

5.2 RECEIVE DIGITAL SIGNAL CHAIN REGISTERS

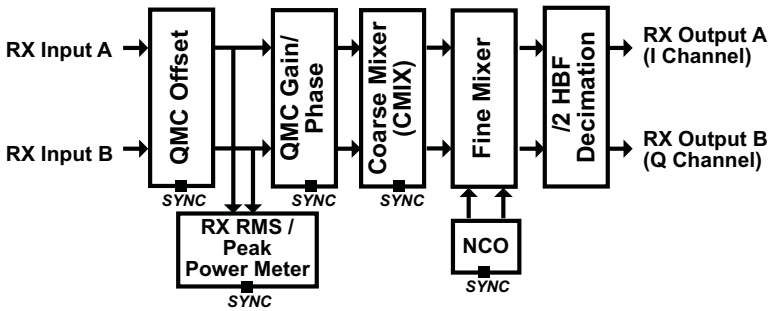

Figure 5-3. Signal Chain

Register Name – CONFIG61 – Address 0x165, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
TX_RX_LPBK_ SRC	TX_RX_LPBK			RX_DECB_MODE	RX_DECA_MODE	RX_DEC_FIL_ EN_SRC	RX_DEC_FIL_ EN

RX_DEC_FIL_EN – Enables the decimation filter in the RX path in both the A and B channels. Set **RX_DEC_FIL_EN_SRC** for this to take effect. Output clock automatically set to 0.5X.

RX_DEC_FIL_EN_SRC – When set, this allows **RX_DEC_FIL_EN** to take effect.

RX_DECA_MODE – When set, configures the decimation filter in Channel A in high pass mode. By default, the filter is in low pass mode.

RX_DECB_MODE – When set, configures the decimation filter in Channel B in high pass mode. By default, the filter is in low pass mode.

TX_RX_LPBK – When this bit and **TX_Rx_LPBK_SRC** are both set , the input to the RX signal chain is tapped from the the final output of the TX signal chain.

TX_Rx_LPBK_SRC – When this bit and **TX_RX_LPBK** are both set , the input to the RX signal chain is tapped from the the final output of the TX signal chain.

The TX to RX loopback is illustrated below. The dotted arrows show the loopback mode.

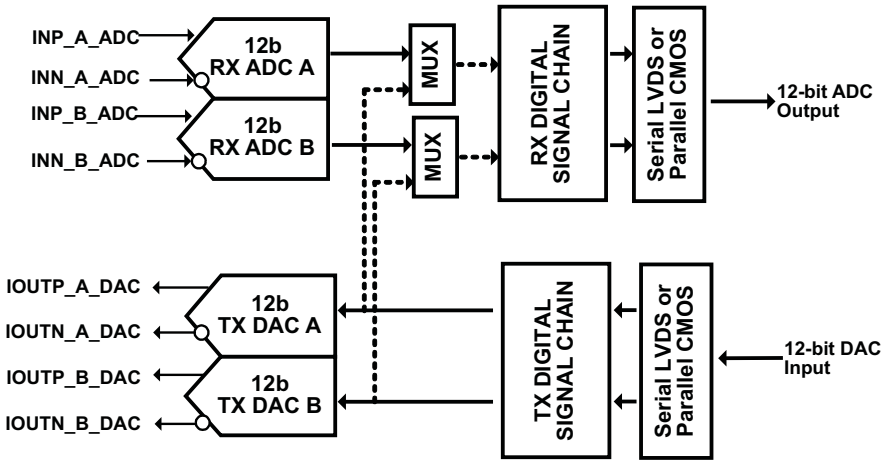

Figure 5-4. Signal Chain

Register Name – CONFIG62 – Address 0x166, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
RX_DIV_PHASE_INV	RX_DIV_PHASE	RX_CMIX_PHASE(1:0)		RX_CMIX_PHASE_ INCR	RX_CMIX_MODE(1:0)		RX_CMIX_EN

RX_CMIX_EN – Enables the RX Coarse mixer.

RX_CMIX_MODE(1:0) – Specifies the mode in which the RX Coarse mixer is configured . Set RX_CMIX_EN for this to take effect.

VALUE	MIXING MODE
0	Normal(Low pass)
1	Fs /2 (High Pass)
2	+ Fs/4
3	– Fs/4

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RX_CMIX_PHASE_INCR – This bit can be used to control the mixing phase without the need for the SYNC pin. A 0 to 1 transition on this bit causes the phase of mixing in the RX CMIX to be incremented by 1 with respect to the current phase of mixing . To increment the phase of mixing more than once, clear and then set this bit once again. Syncing needs to be disabled for RX CMIX for this mode to work. (This means that both global syncing, as well as block level syncing needs to be disabled for CMIX)

RX_CMIX_PHASE(1:0) – The value programmed into this is applied as the RX CMIX phase, when the CMIX is synced, Syncing needs to be enabled for CMIX for this mode to work.

RX_DIV_PHASE – The value programmed into this is applied as the RX Divider phase, when the divider is synced. If divider is not synced, then output latency can differ by 1 with respect to the sampling clock. The RX divider is used whenever the decimation filter is enabled.

RX_DIV_PHASE_INV – This bit is used to control the phase of the RX divider without the need for the SYNC pin. A 0 to 1 transition on this bit causes the phase of division in the RX Divider to be inverted by 1 with respect to the current phase of division. To invert the phase of division more than once, clear and then set this bit once again. Syncing needs to be disabled for RX Divider for this mode to work.

Register Name – CONFIG63 – Address 0x167, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
	RX_BYP_SRC	RX_BYP	RX_CHB_PDN_SRC	RX_CHB_PDN	RX_CHA_PDN	RX_CHA_PDN_SRC	RX_DIS

RX_DIS – Disables the RX signal chain of both channels. All blocks in the signal chain are powered down, and the RX output is mid-code.

RX_CHA_PDN_SRC – Setting this causes the value programmed into **RX_CHA_PDN** to take effect.

RX_CHA_PDN – Powers down Channel A in Rx signal chain. Output of the channel is mid code. Set **RX_CHA_PDN_SRC** for this to take effect. Output clock is not powered down.

RX_CHB_PDN – Powers down Channel B in Rx signal chain. Output of the channel is mid code. Set **RX_CHB_PDN_SRC** for this to take effect. Output clock is not powered down.

RX_CHB_PDN_SRC – Setting this causes the value programmed into **RX_CHB_PDN** to take effect.

Note that when in default mode of operation (none of the register-selectable digital features enabled), all 4 of above bits (RX_CHA_PDN, RX_CHA_PDN_SRC, RX_CHB_PDN, RX_CHB_PDN_SRC) have to be set together to '1' for them to take effect. However, if any of the digital features (like interpolation, Fine mixer, Coarse mixer, or QMC gain/phase or offset) are enabled, then the channel A can be independently powered down using bits RX_CHA_PDN and RX_CHA_PDN_SRC, and channel B can be independently powered down using bits RX_CHB_PDN and RX_CHB_PDN_SRC.

RX_BYP – The inputs to both the Rx channels are directly passed to the outputs. Set **RX_BYP_SRC** for this to take effect. Use this mode to operate the Rx with lowest latency.

RX_BYP_SRC – Setting this causes the value programmed into **RX_BYP** to take effect.

Register Name – CONFIG64 – Address 0x168, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
			RX_GLOBAL_SYNC_DIS	RX_QMC_GAIN_PH_SYNC_DIS	RX_QMC_OFF_SYNC_DIS	RX_DIV_SYNC_DIS	RX_CMIX_SYNC_DIS

RX_CMIX_SYNC_DIS – Disables Syncing of the Rx Coarse mixer. This takes effect only when **RX_GLOBAL_SYNC_DIS** is set.

RX_DIV_SYNC_DIS – Disables Syncing of the Rx clock divider .This takes effect only when **RX_GLOBAL_SYNC_DIS** is set.

RX_QMC_OFF_SYNC_DIS – Disables Syncing of Rx QMC Offset Correction .This takes effect only when **RX_GLOBAL_SYNC_DIS** is set.

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RX_QMC_GAIN_PH_SYNC_DIS – Disables Syncing of Rx QMC Gain Phase Correction.

This takes effect only when **RX_GLOBAL_SYNC_DIS** is set.

RX_GLOBAL_SYNC_DIS – When set, disables global syncing of RX signal chain. When cleared, a rising edge on the selected sync source causes RX blocks to be synced.

Register Name – CONFIG65 – Address 0x169, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
			RX_GLOBAL_SYNC_SRC	RX_QMC_GAIN_PH_SYNC_SRC	RX_QMC_OFF_SYNC_SRC	RX_DIV_SYNC_SRC	RX_CMIX_SYNC_SRC

RX_CMIX_SYNC_SRC – Specifies the sync source for the RX Coarse mixer. When cleared, SYNC pin is used as the sync source . When set, a rising edge on serial interface bit RX_CMIX_SER_IF_SYNC in Register 0x16A is used as the sync source for RX CMIX. This is applicable when **RX_GLOBAL_SYNC_DIS** is set, and **RX_CMIX_SYNC_DIS** is cleared.

RX_DIV_SYNC_SRC – Specifies the sync source for the RX Divider. When cleared, SYNC pin is used as the sync source . When set, a rising edge on serial interface bit RX_DIV_SER_IF_SYNC in register 0x16A is used as the sync source for RX Divider. This is applicable when **RX_GLOBAL_SYNC_DIS** is set and **RX_DIV_SYNC_DIS** is cleared.

RX_QMC_OFF_SYNC_SRC – Specifies the sync source for RX QMC Offset Correction. When cleared, SYNC pin is used as the sync source . When set , a rising edge on serial interface bit RX_QMC_OFF_SER_IF_SYNC in register 0x16A is used as the sync source for RX QMC Offset Correction. This is applicable when **RX_GLOBAL_SYNC_DIS** is set and **RX_QMC_OFF_SYNC_DIS** is cleared.

RX_QMC_GAIN_PH_SYNC_SRC – Specifies the sync source for RX QMC Gain Phase Correction. When cleared, SYNC pin is used as the sync source. When set, a rising edge on serial interface bit RX_QMC_GAIN_PH_SER_IF_SYNC in register 0x16A is used as the sync source for RX QMC Gain Phase Correction. This is applicable when **RX_GLOBAL_SYNC_DIS** is set and **RX_QMC_GAIN_PH_SYNC_DIS** is cleared.

RX_GLOBAL_SYNC_SRC – Specifies the sync source for RX. When cleared, SYNC pin is used as the sync source. When set, a rising edge on serial interface bit RX_GLOB_SER_IF_SYNC in register 0x16A is used as the sync source for RX. This is applicable when **RX_GLOBAL_SYNC_DIS** is cleared.

Register Name – CONFIG66 – Address 0x16A, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
			RX_GLOBAL_SER_IF_SYNC	RX_QMC_GAIN_PH_SER_ IF_SYNC	RX_QMC_OFF_SER_IF_SYNC	RTX_DIV_SER_IF_SYNC	RX_CMIX_SER_IF_SYNC

RX_CMIX_SER_IF_SYNC – A rising edge on this bit is used as the sync source for RX CMIX. This is applicable when **RX_GLOBAL_SYNC_DIS** is set, and **RX_CMIX_SYNC_DIS** is cleared, and **RX_CMIX_SYNC_SRC** specifies serial interface bit to be the sync source for the RX CMIX.

RX_DIV_SER_IF_SYNC – A rising edge on this bit is used as the sync source for RX Divider. This is applicable when **RX_GLOBAL_SYNC_DIS** is set, and **RX_DIV_SYNC_DIS** is cleared, and **RX_DIV_SYNC_SRC** specifies serial interface bit to be the sync source for the RX Divider.

RX_QMC_OFF_SER_IF_SYNC – A rising edge on this bit is used as the sync source for RX QMC Offset correction block. This is applicable when **RX_GLOBAL_SYNC_DIS** is set, and **RX_QMC_OFF_SYNC_DIS** is cleared, and **RX_QMC_OFF_SYNC_SRC** specifies serial interface bit to be the sync source for the RX QMC Offset correction.

RX_QMC_GAIN_PH_SER_IF_SYNC – A rising edge on this bit is used as the sync source for RX QMC Gain Phase correction block. This is applicable when **RX_GLOBAL_SYNC_DIS** is set, and **RX_QMC_GAIN_PH_SYNC_DIS** is cleared, and **RX_QMC_GAIN_PH_SYNC_SRC** specifies serial interface bit to be the sync source for the RX QMC Gain Phase correction.

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RX_GLOBAL_SER_IF_SYNC – A rising edge on this is used as the sync source for RX . This is applicable when **RX_GLOBAL_SYNC_DIS** is cleared, and **RX_GLOBAL_SYNC_SRC** specifies serial interface bit to be the sync source for RX.

Register Name – CONFIG67 – Address 0x16B, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
			RX_QMC_CORR_ ENA	RX_QMC_OFFSET_ ENA		RX_QMC_GAIN_PH_SYNC_ NEEDED	RX_QMC_OFF_SYNC_ NEEDED

RX_QMC_OFF_SYNC_NEEDED – Specifies if syncing is needed for RX QMC Offset Correction. If set, QMC Offset values programmed into the serial interface registers are not applied to the QMC Offset correction block until a Sync is applied.

RX_QMC_GAIN_PH_SYNC_NEEDED – Specifies if syncing is needed for RX QMC Gain Phase Correction. If set, QMC gain and Phase values programmed into the serial interface registers are not applied to the QMC Gain Phase correction block until a sync is applied.

RX_QMC_OFFSET_ENA – Enables RX QMC Offset Correction.

RX_QMC_CORR_ENA – Enable RX QMC Gain Phase Correction.

Register Name – CONFIG68 – Address 0x16C, Default = 0x00 (Synced)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
RX_QMC_OFFSETA(12:5)							

RX_QMC_OFFSETA(12:5) – Upper 8 bits of ADC A Offset Correction . The lower 5 bits are in **CONFIG69** Register.

Register Name – CONFIG69 – Address 0x16D, Default = 0x00 (Synced)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
RX_QMC_OFFSETA(4:0)				RX_QMC_GAINA(2:0)			

RX_QMC_OFFSETA(4:0) – Lower 5 bits of ADC A Offset Correction .

RX_QMC_GAINA(2:0) – Lower 3 bits of the 11 bit QMC Gain word for ADC A. The upper 8 bits are in **CONFIG70** register.The full 11 bit RX_QMC_GAINA(10:0) word is formatted as UNSIGNED with a range or 0 to 1.9990. The implied decimal point for the multiplication is between bits (9) and (10).

Register Name – CONFIG70 – Address 0x16E, Default = 0x00 (Synced)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
RX_QMC_GAINA(10:3)							

RX_QMC_GAINA(10:3) – Upper 8 bits if the 11 bit QMC Gain word for ADC A

Register Name – CONFIG71 – Address 0x16F, Default = 0x00 (Synced)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
RX_QMC_OFFSETB(12:5)							

RX_QMC_OFFSETB(12:5) – Upper 8 bits of ADC B Offset Correction . The lower 5 bits are in **CONFIG72** Register.

Register Name – CONFIG72 – Address 0x170, Default = 0x00 (Synced)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
RX_QMC_OFFSETB(4:0)				RX_QMC_GAINB(2:0)			

RX_QMC_OFFSETB(4:0) – Lower 5 bits ofADC B Offset Correction .

RX_QMC_GAINB(2:0) – Lower 3 bits of the 11 bit QMC Gain word for ADC B. The upper 8 bits are in **CONFIG73** register.The full 11 bit RX_QMC_GAINB(10:0) word is formatted as UNSIGNED with a range or 0 to 1.9990.

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Register Name – CONFIG73 – Address 0x171, Default = 0x00 (Synced)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
RX_QMC_GAINB(10:3)							

RX_QMC_GAINB(10:3) – Upper 8 bits of the 11 bit QMC Gain word for ADC B.

Register Name – CONFIG74 – Address 0x172, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
RX_QMC_PHASE(9:2)							

RX_QMC_PHASE(9:2) – Upper 8 bits of the 10 bit QMC Phase word. The lower two bits are in the **CONFIG75** register. The full QMC_PHASE(9 :0) correction word is formatted as 2s complement and scaled to occupy a range of -0.125 to 0.12475. To acomplish QMC Phase correction, this value is multiplied by the current Q sample, then summed to the I sample.

Register Name – CONFIG75 – Address 0x173, Default = 0x00 (Synced)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
						RX_QMC_PHASE(1:0)	

RX_QMC_PHASE(1:0) – Lower 2 bits of the 10 bit QMC Phase word.

Register Name – CONFIG76 – Address 0x174, Default = 0x00 (Synced)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
RX_NCO_FREQ_WORD(31:24)							

RX_NCO_FREQ_WORD(31:24) – See CONFIG79 below.

Register Name – CONFIG77 – Address 0x175, Default = 0x00 (Synced)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
RX_NCO_FREQ_WORD(23:16)							

RX_NCO_FREQ_WORD(23:16) – See CONFIG79 below.

Register Name – CONFIG78 – Address 0x176, Default = 0x00 (Synced)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
RX_NCO_FREQ_WORD(15:8)							

RX_NCO_FREQ_WORD(15:8) – See CONFIG79 below.

Register Name – CONFIG79 – Address 0x177, Default = 0x00 (Synced)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
RX_NCO_FREQ_WORD(7:0)							

RX_NCO_FREQ_WORD(7:0) – This 32-bit word specifies the frequency of the NCO used by the fine mixer. The twos complement formatted value can be positive or negative, and the LSB is equal to ($Fs/2^{32}$).

Register Name – CONFIG80 – Address 0x178, Default = 0x00 (Synced)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
RX_NCO_PHASE_OFF(15:8)							

RX_NCO_PHASE_OFF(15:8) – See CONFIG81 below.

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Register Name – CONFIG81 – Address 0x179, Default = 0x00 (Synced)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
RX_NCO_PHASE_OFF(7:0)							

RX_NCO_PHASE_OFF(7:0) – This is the Phase offset added to the NCO accumulator just before the generation of the SIN and COS values.

Register Name – CONFIG82 – Address 0x17A, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PWR_MTR_COARSE_SAMPLES(2:0)				RX_MIXER_EN	RX_MIXER_GAIN(1:0)		

RX_MIXER_GAIN(1:0) – This specifies the gain to be applied to the mixer output to prevent it from saturating.

VALUE	GAIN
0	-2.5 dB
1	-6 dB
2	0 dB
3	0 dB

RX_MIXER_EN – This enables the Full mixer, which also causes the NCO to be enabled.

PWR_MTR_COARSE_SAMPLES(2:0) – Specifies the number of samples, 'N' over which power is to be computed when the power meter is configured in the coarse mode. Keeps refreshing every 'N' samples but writes to serial interface register only when serial clock is available – which requires a write to this page. Stops refreshing once you get into readout mode.

VALUE	NUMBER OF SAMPLES
0	16
1	32
2	64
3	128
4	256
5	512
6	1024
7	16

Register Name – CONFIG83 – Address 0x17B, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PWR_MTR_ SYNC_DIS	PWR_MTR_ SYNC_SRC	PWR_MTR_ SER_IF_SYNC	PWR_MTR_ SYNC_NEEDED	RX_NCO_ SYNC_DIS	RX_NCO_ SYNC_SOURCE	RX_NCO_SER_ IF_SYNC	RX_NCO_ SYNC_ NEEDED

RX_NCO_SYNC_NEEDED – Specifies if syncing is needed for RX NCO. If set , NCO Frequency and Offset words programmed into the serial interface registers are not applied to the NCO until a sync is applied

RX_NCO_SER_IF_SYNC – A rising edge on this bit is used as the sync source for RX NCO. This is applicable when **RX_GLOBAL_SYNC_DIS** is set, and **RX_NCO_SYNC_DIS** is cleared, and **RX_NCO_SYNC_SRC** specifies serial interface bit to be the sync source for the NCO.

RX_NCO_SYNC_SRC – Specifies the sync source for RX NCO. When cleared, SYNC pin is used as the sync source. When set, a rising edge on serial interface bit RX_NCO_SER_IF_SYNC is used as the sync source for RX NCO. This is applicable when **RX_GLOBAL_SYNC_DIS** is set

RX_NCO_SYNC_DIS – Disables Syncing of the RX NCO .This takes effect only when RX_GLOBAL_SYNC_DIS is set

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PWR_MTR_SYNC_NEEDED – Specifies if syncing is needed for the RX Power Meter . If set, power computation begins a programmable number of cycles after the detection of a sync pulse. Applies for both the coarse and fine power meters.

PWR_MTR_SER_IF_SYNC – A rising edge on this bit is used as the sync source for RX Power Meter. This is applicable when **RX_GLOBAL_SYNC_DIS** is set, and **PWR_MTR_SYNC_DIS** is cleared, and **PWR_MTR_SYNC_SRC** specifies serial interface bit to be the sync source for the Power Meter.

PWR_MTR_SYNC_SRC – Specifies the sync source for RX Power Meter . When cleared, SYNC pin is used as the sync source . When set, a rising edge on serial interface bit **PWR_MTR_SER_IF_SYNC** is used as the sync source for RX Power Meter. This is applicable when **RX_GLOBAL_SYNC_DIS** is set

PWR_MTR_SYNC_DIS – Disables Syncing of the RX Power Meter .This takes effect only when **RX_GLOBAL_SYNC_DIS** is set.

Register Name – CONFIG84 – Address 0x17C, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
INTGR_CNT (20:13)							

INTGR_CNT(20:13) – Upper 8 bits of the 21 bit Integration count for the fine power meter. Integration is done over (8N + 3) samples where N is the unsigned integer represented by INTGR_CNT (20:0)

Register Name – CONFIG85 – Address 0x17D, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
INTGR_CNT(12:5)							

INTGR_CNT(12:5) – Middle 8 bits of the 21 bit Integration count for the Power meter.

Register Name – CONFIG86 – Address 0x17E, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
INTGR_CNT(4:0)					SYNC_CNT(8:6)		

SYNC_CNT(8:6) – Upper 3 bits of the 9 bit Sync count for the fine power meter. After the detection of a sync pulse, there is a delay of 8N +4 cycles before Integration begins, where N is the unsigned integer represented by SYNC_CNT(8:0)

INTGR_CNT(4:0) – Lower 5 bits of the 21 bit Integration count for the fine power meter.

Register Name – CONFIG87 – Address 0x17F, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
SYNC_CNT(5:0)							

SYNC_CNT(5:0) – Lower 3 bits of the 9 bit Sync count.

Register Name – CONFIG88 – Address 0x180, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
INTRV_CNT (20:13)							

INTRV_CNT (20:13) – Upper 8 bits of the 21 bit Interval count for the fine power meter. The actual Interval period is (8N + 3) samples where N is the unsigned integer represented by INTRV_CNT (20:0)

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Register Name – CONFIG89 – Address 0x181, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
INTRV_CNT(12:5)							

INTRV_CNT(12:5) – Middle 8 bits of the 21 bit Interval count for the Power meter

Register Name – CONFIG90 – Address 0x182, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
INTRV_CNT (4:0)					PWR_MTR_MODE	PWR_MTR_FINE	PWR_MTR_EN

INTRV_CNT(4:0) – Lower 4 bits of the 21 bit Interval count for the Power meter

PWR_MTR_EN – Enables the power meter. Common for fine and coarse power meters.

PWR_MTR_FINE – When cleared, configures the power meter in 'Fine ' mode where it gives linear output . When set, configures it in the coarse mode, where it gives output in the db scale.In coarse mode, the number of samples over which power is computed is specified in the PWR_MTR_COARSE_SAMPLES(2:0) in CONFIG82.

PWR_MTR_MODE – When cleared, configures the power meter in the real mode – Output I = I^2, Output Q = Q^2. When set, configures it in complex mode – Output = $I^2 + Q^2$.

Register Name – CONFIG91 – Address 0x183, Default = 0x00 (Read Only)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PWR_OP_I(57:50)							

PWR_OP_I(57:50) – Upper 8 bits of the Power meter output for I channel when it is configured in the Fine mode. This represents power of I channel when configured in the real mode, and the complex power when configured in the complex mode.

Register Name – CONFIG92 – Address 0x184, Default = 0x00 (Read Only)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PWR_OP_I(49:42)							

PWR_OP_I(49:42)

Register Name – CONFIG93 – Address 0x185, Default = 0x00 (Read Only)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PWR_OP_I(41:34)							

PWR_OP_I(41:34)

Register Name – CONFIG94 – Address 0x186, Default = 0x00 (Read Only)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PWR_OP_I(33:26)							

PWR_OP_I(33:26)

Register Name – CONFIG95 – Address 0x187, Default = 0x00 (Read Only)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PWR_OP_I(25:18)							

PWR_OP_I(25:18)

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Register Name – CONFIG96 – Address 0x188, Default = 0x00 (Read Only)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PWR_OP_I(17:10)							

PWR_OP_I(17:10)

Register Name – CONFIG97 – Address 0x189, Default = 0x00 (Read Only)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PWR_OP_I(9:2)							

PWR_OP_I(9:2)

Register Name – CONFIG98 – Address 0x18A, Default = 0x00 (Read Only)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PWR_OP_I(1:0)		PWR_OP_Q(57:52)					

PWR_OP_Q(57:0) – Power meter output for Q channel when it is configured in the Fine mode . This represents power of Q channel when configured in the real mode. In the complex mode, this does not contain any information. For a 12-bit output (as is the case in AFE722x), the lower eight bits will not contain any information; so it is sufficient to read out PWR_OP_Q(57:8).

PWR_OP_I(57:0) – Power meter output for I channel when it is configured in the Fine real mode. This represent the power of the I channel, and in the complex mode, it represents the complex power. For a 12-bit output (as is the case in AFE722x), the lower eight bits will not contain any information; so it is sufficient to read out PWR_OP_I(57:8).

Register Name – CONFIG99 – Address 0x18B, Default = 0x00 (Read Only)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PWR_OP_Q(51:44)							

PWR_OP_Q(51:44)

Register Name – CONFIG100 – Address 0x18C, Default = 0x00 (Read Only)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PWR_OP_Q(43:36)							

PWR_OP_Q(43:36)

Register Name – CONFIG101 – Address 0x18D, Default = 0x00 (Read Only)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PWR_OP_Q(35:28)							

PWR_OP_Q(35:28)

Register Name – CONFIG102 – Address 0x18E, Default = 0x00 (Read Only)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PWR_OP_Q(27:20)							

PWR_OP_Q(27:20)

Register Name – CONFIG103 – Address 0x18F, Default = 0x00 (Read Only)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PWR_OP_Q(19:12)							

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PWR_OP_Q(19:12)

Register Name – CONFIG104 – Address 0x190, Default = 0x00 (Read Only)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PWR_OP_Q(11:4)							

PWR_OP_Q(11:4)

Register Name – CONFIG105 – Address 0x191, Default = 0x00 (Read Only)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PWR_OP_Q(3:0)						PWR_OP_Q_RDY	PWR_OP_I_RDY

PWR_OP_I_RDY – Set when the very first computation from the 'I' power meter is complete.

PWR_OP_Q_RDY – Set when the very first computation from the 'Q' power meter is complete.

PWR_OP_Q(3:0) – Lowest two bits of the power meter output for Q channel when it is configured to do fine power computation in the real mode.

Register Name – CONFIG106 – Address 0x1B2, Default = 0x00 (Read Only)

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
COARSE_PWR_OP_I(3:0)				COARSE_PWR_OP_Q(3:0)			

COARSE_PWR_OP_Q(3:0) – Represents the power in the Q channel when power meter is configured in the coarse power computation mode. In complex power computation mode, this output should be ignored. The mapping of this value to the db scale is given below table.

COARSE_PWR_OP_I(3:0) – Represents the power in the I channel when power meter is configured in the coarse power computation mode. In complex power computation mode, this output represents the complex power.

Note – In complex power computation mode, the full scale is twice of what it is in the real power computation mode.

VALUE	POWER IN DB SCALE
15	Greater than –1 dbFS
14	Greater than –2 dbFS
13	Greater than –3 dbFS
12	Greater than –4 dbFS
11	Greater than –5 dbFS
10	Greater than –6 dbFS
9	Greater than –7 dbFS
8	Greater than –8 dbFS
7	Greater than –9 dbFS
6	Greater than –10 dbFS
5	Greater than –11 dbFS
4	Greater than –12 dbFS
3	Greater than –13 dbFS
2	Greater than –14 dbFS
1	Greater than –15 dbFS
0	Lesser than –15 dbFS

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5.3 CHIP CONTROL REGISTERS

Register Name – CONFIG107 – Address 0x000, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
						SOFTWARE_RESET	

SOFTWARE_RESET:-Register bit to reset the device. Once set, the bit generates a reset pulse, which resets all the register bits including itself.

Register Name – CONFIG108 – Address 0x207, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
REG_PDNFRM_REG	REG_PDN_FAST	REG_PDN_GBL	REG_PDNQ	REG_PDNI	REG_PDN_RX	REG_PDN_TX	

REG_PDN_FRM_REG : Specifies whether the PDN control is through PIN or register bit. When cleared, PDN pin is used as the master control.

For all the below power down modes to work, either set REG_PDN_FRM_REG or pull PDN pin to 'High'.

REG_PDN_FAST : When REG_PDN_FRM_REG is low, this bit configures the PDN pin for fast powerdown control. When REG_PDN_FRM_REG is high, this bit directly controls the fast powerdown mode. When set, it power downs both transmitter and receiver but keeps certain blocks like reference circuitry active. Also the Rx output clock is still active. This mode can be used where fast wake up times are required.

REG_PDN_GBL : When REG_PDN_FRM_REG is low, this bit configures the PDN pin for global powerdown control. When REG_PDN_FRM_REG is high, this bit directly controls the global powerdown mode. When set, it powers down almost all circuitry inside the chip. Thus this mode can be used when lowest power is desired. The wakeup times in this mode are much higher than in the fast powerdown mode.

REG_PDNQ : Power downs Q channel of both transmitter and reciever.

REG_PDNI : Power down I channel of both transmitter and reciever.

REG_PDN_RX : Power downs reciever i.e both the ADC's. Clock path is still active.

REG_PDN_TX : Power downs transmitter i.e both the DAC's.

REG_PDN_FRM_REG has a similar role to play for the above modes (REG_PDNQ, REG_PDNI, REG_PDN_RX, REG_PDN_TX). When REG_PDN_FRM_REG is low, it configures the PDN pin to the function of the bit that is set. When REG_PDN_FRM_REG is high, the set bit directly controls the described powerdown mode.

At 20 MHz Fs, the typical power consumption in different modes are as follows:

CONDITION	CURRENT ON 1.8 V SUPPLY (mA)	CURRENT ON 3 V SUPPLY (mA)
Normal	63	58
Global Power down (REG_PDN_GBL = 1)	2.4	3
Fast power down (REG_PDN_FAST = 1)	25	13
Rx_power down (REG_PDN_RX = 1)	27	58
Tx power down (REG_PDN_TX = 1)	62	13
Both Rx and Tx (REG_PDN_TX = 1, REG_PDN_RX = 1)	25	13

Register Name – CONFIG109 – Address 0x208, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
REG_PDNI_TX	REG_PDNQ_TX	REG_PDNI_RX	REG_PDNQ_RX	MODE_LP_CMOS	REG_SINGLE		

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REG_PDNI_TX : Power downs TX Channel A (I Channel) alone.

REG_PDNQ_TX : Power downs TX Channel B (Q Channel) alone.

REG_PDNI_RX : Power downs RX Channel A (I Channel) alone.

REG_PDNQ_RX : Power downs RX Channel B (Q Channel) alone.

REG_PDN_FRM_REG has a similar role to play for the above modes (REG_PDNI_TX, REG_PDNQ_TX, REG_PDNI_RX, REG_PDNQ_RX). When REG_PDN_FRM_REG is low, it configures the PDN pin to the function of the bit that is set. When REG_PDN_FRM_REG is high, the set bit directly controls the described powerdown mode.

MODE_LP_CMOS : Low power RX CMOS mode. When the RX interface is set to CMOS interface, the device power can be lowered by about 20 mW by setting this bit. Use this mode only for Fs less than 40 MSPS. Refer to section **Low power RX CMOS mode**.

REG_SINGLE : Setting this bit power downs one ADC (Channel A) and One DAC (Channel A). The output data format is SDR. In this mode DAC Channel B and ADC Channel B are active.

Register Name – CONFIG110 – Address 0x209, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
	REG_OEZ_ LVDS_ CHB	REG_OEZ_ LVDS_ CHA	REG_OEZ_ LVDS_CLK			REG_OEZ_ CMOS_ CLK	REG_OEZ_ CMOS_DAT

REG_OEZ_CMOS_DAT: 3-state RX CMOS data buffers (use for Half Duplex TX mode when using CMOS interface)

REG_OEZ_CMOS_CLK: 3-state RX CMOS clock buffer (use for Half Duplex TX mode when using CMOS interface)

REG_OEZ_LVDS_CLK: 3-state RX LVDS clock buffer (use for Half Duplex TX mode when using LVDS interface)

REG_OEZ_LVDS_CHA: 3-state RX LVDS data buffers for Channel A (use for Half Duplex TX mode when using LVDS interface)

REG_OEZ_LVDS_CHB: 3-state RX LVDS data buffers for Channel B (use for Half Duplex TX mode when using LVDS interface)

Register Name – CONFIG111 – Address 0x20A, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
		REG_SE_CLK		REG_LVDS_TX	REG_LVDS_RX	WHAT_IS_SDOUT<1:0>	

REG_SE_CLK: When set, the device is configured to expect two single ended clocks on CLKINP and CLKINN. DAC_CLK gets derived from the clock on CLKINN and ADC_CLK from the clock on CLKINP. The differential clock buffer is turned off, saving about 6mA of current on the 1.8 V supply.

REG_LVDS_TX: By default both RX and TX interfaces are in CMOS mode, this bit sets the TX input interface in LVDS mode

REG_LVDS_RX: this bit sets the RX output interface in LVDS mode. In addition to setting this bit, also set bit MASTER_OVERRIDE_RX (in CONFIG131) for proper LVDS settings.

WHAT_IS_SDOUT<1:0>: Configures the SDOUT pin.

WHAT_IS_SDOUT<1:0>	Mode
00	Floating
01	Analog test o/p (Do not use)
10	Digital o/p (Use for Aux ADC and register readout)
11	Digital i/p (Use for Aux DAC input mode)

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5.4 TX DAC CONTROL REGISTERS

Register Name – CONFIG112 – Address 0x237, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
DACQ_GAIN<7:0>							

DACQ_GAIN<7:0>: Fine control of Channel B (DACQ) output current.

Output current range is 0.04*FS to -0.04*FS, where FS is Full scale current of DACQ. The word is in 2's complement format.

DACQ_GAIN<7:0>(decimal equivalent)	OUTPUT CURRENT
0	FS
127	FS+.04*FS
128	FS-.04*FS

Register Name – CONFIG113 – Address 0x238, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
DACI_GAIN<7:0>							

DACI_GAIN<7:0>: Fine control of Channel A (DACI) output current. Similar to DACQ_GAIN<7:0>.

Register Name – CONFIG114 – Address 0x239, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
DACI_COARSEZ<3:0>				DACQ_COARSEZ<3:0>			

DACI_COARSEZ<3:0>: Coarse control of the Channel A (DACI) output current. Let FS be full scale current then,

DACI_COARSEZ<3:0>	OUTPUT CURRENT
0000	FS
0001	15*FS/16
0010	14*FS/16
0011	13*FS/16
0100	12*FS/16
0101	11*FS/16
0110	10*FS/16
0111	9*FS/16
1000	8*FS/16
1001	7*FS/16
1010	6*FS/16
1011	5*FS/16
1100	4*FS/16
1101	3*FS/16
1110	2*FS/16
1111	FS/16

DACQ_COARSEZ<3:0>: Coarse control of the Channel B (DACQ) output current - similar to DACI_COARSEZ<3:0>.

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5.5 CLOCKING CONTROL REGISTERS

Register Name – CONFIG115 – Address 0x23C, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
STR_CTRL<1:0>			DIV_ADC<1:0>		DIV_DAC<1:0>		

STR_CTRL<1:0>: Controls the strength of the RX CMOS output clock (ADC_DCLKOUT) and data buffers (increases the strength). When running at Fs higher than 90 MSPS, set to '10' to get more timing margins. Enabling this mode might increase the digital noise coupled to analog and may degrade the ADC SNR by up to a dB.

DIV_ADC<1:0>: Divides the clock going to the ADC.

DIV_ADC<1:0>	DIVISION FACTOR
00	Default (no division)
01	2
10	4
11	2

DIV_DAC<1:0>: Divides the clock going to the DAC.

DIV_ADC<1:0>	DIVISION FACTOR
00	Default (no division)
01	2
10	4
11	2

Register Name – CONFIG116 – Address 0x23D, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PLL_ENABLE				PLL_DIVM<1:0>			PLL_DIVN

PLL_ENABLE: Setting this bit enables the PLL. Output clock of the PLL is either 2X or 4X of Fs (input clock rate).

PLL_DIVN: Selects multiplication by 4 (default is multiplication by 2).

PLL_DIVM<1:0>: Different values as listed in the below table need to be programmed for different Fs ranges.

	PLL_DIVM<1:0>	
FS in MSPS	**Multiplication by 2**	**Multiplication by 4**
15-20	3	2
20-35	2	1
35-80	1	0
> 80-180	0	Out of range

While operating PLL with a multiplication factor set by PLL_DIVN = X, there can be significant spurs at (NFs/X+/-Fin) where N is an integer. At Fin = 10 MHz, these spurs can be about -60dBc.

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Register Name – CONFIG117A – Address 0xDB, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
							ENABLE_DCC_CHB

ENABLE_DCC_CHB: Enables the duty cycle correction circuit (DCC) for the ADC_CLK for ADC Channel B. It is recommended to use the DCC when operating at frequencies of ADC_CLK higher than 65 MSPS.

Register Name – CONFIG117B – Address 0xF2, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
				ENABLE_DCC_CHA			

ENABLE_DCC_CHA: Enables the duty cycle correction circuit (DCC) for the ADC_CLK for ADC Channel A. It is recommended to use the DCC when operating at frequencies of ADC_CLK higher than 65 MSPS.

5.6 AUX DAC REGISTERS

Register Name – CONFIG118 – Address 0x242, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
AUX_DAC_TERM_N<2:0>						EN_AUXDACB	EN_AUXDACA

AUX_DAC_TERM_N<2:0>: Termination resistor for the negative terminal of the AUX DAC (internal node). Choose it to be close to the termination resistor on the pin.

AUX_DAC_TERM_N<2:0>	TERMINTION RESISTOR (ohm)
0	200 (default)
1	infinite
10	67
11	100
100	133
101	400
110	57
111	80

EN_AUXDACB: Enables AUXDACB.

EN_AUXDACA: Enables AUXDACA.

Register Name – CONFIG119 – Address 0x243, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
REG_AUXDACA_IN<11:4>							

REG_AUXDACA_IN<11:4> – Register bits for DACA data in Register Access mode

Register Name – CONFIG120 – Address 0x244, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
REG_AUXDACA_IN<3:0>							

REG_AUXDACA_IN<3:0> – Register bits for DACA data in Register Access mode.

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Register Name – CONFIG121 – Address 0x245, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
REG_AUXDACB_IN<11:4>							

REG_AUXDACB_IN<11:4> – Register bits for DACB data in Register Access mode

Register Name – CONFIG122 – Address 0x246, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
REG_AUXDACB_IN<3:0>							

REG_AUXDACB_IN<3:0> – Register bits for DACB data in Register Access mode

Register Name – CONFIG123 – Address 0x248, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
				FS_AUXDACI<3:0>			

FS_AUXDACI<3:0> – Sets full scale output current for AUXDACA. The 16 levels in mA are:

FS_AUXDACI<3:0>	OUTPUT CURRENT(mA)
0000	5
0001	5.5
0010	4
0011	4.5
0100	7
0101	7.5
0110	6
0111	6.5
1000	Do not use
1001	Do not use
1010	Do not use
1011	Do not use
1100	3
1101	3.5
1110	Do not use
1111	2.5

Register Name – CONFIG124 – Address 0x249, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
				FS_AUXDACQ<3:0>			

FS_AUXDACQ<3:0> – Sets full scale input current for AUXDACB. This register is similar to Register 0x248.

5.7 LVDS TX INPUT INTERFACE REGISTERS

Register Name – CONFIG125 – Address 0x30B, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
TWOWIRE_TX	RESOLUTION_TX<2:0>			MSB_FIRST_TX	SERIALIZATION_TX<1:0>		SDR_TX

All the modes of register 0x30B works only if MASTER_OVERRIDE_TX (Bit <2> in Address 0x30C) is enabled.

TWOWIRE_TX: Sets two wire modes in the transmitter side.

RESOLUTION_TX<2:0>: To set the input resolution of the Transmitter.

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RESOLUTION_TX<2:0>	RESOLUTION
000	12

MSB_FIRST_TX<1:0>: Decides whether LSB first or MSB first. Default is LSB first..

MSB_FIRST_TX	DATA PATTERN
0	LSB first
1	MSB first

SERIALIZATION_TX<1:0>: Sets serialization factor of the transmitter.

SERIALIZATION_TX<1:0>	SERIALIZATION FACTOR
00	12x (default)
01	14x
10	16x

SDR_TX: By setting this Tx expects SDR input pattern, where as the default is DDR. Bit clock is double rate in SDR mode.

Register Name – CONFIG126 – Address 0x30C, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
					MASTER_OVERRIDE_TX	BITWISE_TX	DFS_TX

All the modes of register 0x30C works only if MASTER_OVERRIDE_TX (Bit <2> in Address 0x30C) is enabled.

MASTER_OVERRIDE_TX: Master bit for various override modes

BITWISE_TX: To set the device in bitwise mode.

DFS_TX: Determines the data format of the incoming data.

DFS_TX	DATA FORMAT
0	2's complement (default)
1	straight offset binary

Register Name – CONFIG127 – Address 0x30d, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
		WORDWISE_TX					

All the modes of register 0x30D works only if MASTER_OVERRIDE_TX (Bit <2> in Address 0x30C) is enabled.

WORDWISE_TX: If set, TX expects word mode format data.

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5.8 LVDS RX OUTPUT INTERFACE REGISTERS

Register Name – CONFIG128 – Address 0x337, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
		OVR_EN_RX		WORDWISE_ RX	PATTERN_SEL_RX<2:0>		

All the modes of register 0x337 work only if MASTER_OVERRIDE_RX (Bit <7> in Address 0x33A) is enabled.

OVR_EN_RX: Overrange indicator enable bit. When 0 – Overrange is not sent along with data. If 1 – D0 is replaced by Overrange indicator bit.

WORDWISE_RX: When selected, wordwise mode is enabled.

PATTERN_SEL_RX<2:0>: To select the output pattern from the serializer

PATTERN_SEL<2:0>	OUTPUT PATTERN
000	Normal ADC pattern
001	All Zeros
010	All ones
011	alternate between 1 and 0 (D11..D0 alternates between 010101010101 and 101010101010)
100	Data ramp pattern (D11..D0 ramps continuously every 4 clock cycles in steps of 1 LSB)
101	Output custom pattern
110	Deskew pattern – D11..D0 replaced by 010101010101
111	Sync pattern – D11..D0 replaced by 111111000000 in 1-wire mode and by 111000111000 in 2-wire mode

Register Name – CONFIG129 – Address 0x338, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CUSTOM PATTERN <15:8>							

Register Name – CONFIG130 – Address 0x339, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
CUSTOM PATTERN <7:0>							

Register Name – CONFIG131 – Address 0x33A, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MASTER_OVERRIDE_RX	SERIALIZATION_RX<1:0>		DFS_RX	MSB_FIRST_RX		TWOWIRE_RX	SDR_RX

All the modes of register 0x33A work only if MASTER_OVERRIDE_RX (Bit <7> in Address 0x33A) is enabled.

MASTER_OVERRIDE_RX: Master override bit for RX interface registers. This bit needs to be set to 1 whenever the RX interface mode is chosen to be LVDS interface.

SERIALIZATION_RX<1:0>: Sets the serialization factor.

SERIALIZATION_RX<1:0>	SERIALIZATION
00	12
01	14
10	16

In two wire mode for 14x serialization the frame clock is 0.5X, where as 12X and 16X frame clock is still 1X.

DFS_RX: Sets the output data format.

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DFS_RX	DATA FORMAT
0	2s-complememt
1	straight offset binary

MSB_FIRST_RX: Flips the out data order to MSB first.

MSB_FIRST_RX	DATA ORDER
0	LSB first
1	MSB first

TWOWIRE_RX: Configure the device to give data in two wire mode.

SDR_RX: Configure the device to give data in SDR mode.

Register Name – CONFIG132 – Address 0x33B, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
						HALFX_IN_2WIRE_RX	BITWISE_RX

All the modes of register 0x33B work only if MASTER_OVERRIDE_RX (Bit <7> in Address 0x33A) is enabled.

BITWISE_RX: Configure the device to give data in bit wise mode.

HALFX_IN_2WIRE_RX: Makes the frame clock output 0.5X (default is 1X). To be used when in wordwise mode.

Register Name – CONFIG133 – Address 0x23A, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
				CLK_STR_2X	DATA_STR_2X		

CLK_STR_RX: When set, the LVDS clock buffers has double strength (to be used with 50 ohms external termination)

DATA_STR_2X: When set, all the LVDS clock buffers have double strength (to be used with 50 ohms external termination)

Register Name – CONFIG134 – Address 0x001, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
LVDS_SWING<5:0>							

5.9 AUX ADC REGISTERS

Register Name – CONFIG135 – Address 0x364, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
SHIGH_WIDTH<1:0>		NO_OF_SAMPLES_AVGED<1:0>		NO_OF_SAMPLES<2:0>			CONV_START

SHIGH_WIDTH<1:0>: No. of clock cycles width of sampling clock.

SHIGH_WIDTH<1:0>	NO.OF CLOCK CYCLE WIDTH
00	15(default)
01	30
10	60
11	150

NO_OF_SAMPLES<2:0>: No. of samples to convert in 1 conversion cycle.

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NO_OF_SAMPLES<2:0>	NO.OF SAMPLES TO CONVERT
000	1
001	2
010	4
011	8
100	16
101	Continuous
110	Continuous
111	Continuous

NO_OF_SAMPLES_AVERAGED<1:0>: No. of samples within the same conversion cycle to be averaged. Should be less than or equal to NO_OF_SAMPLES.

NO_OF_SAMPLES_AVERAGED<1:0>	NO. OF SAMPLES TO BE AVERAGED
00	No averaging
01	2
10	4
11	8

If averaging is set, then the Aux ADC output is updated once in every X samples where X is equal to the no. of samples to be averaged.

CONV_START: Starts Conversion.

Register Name – CONFIG136 – Address 0x36F, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
	BYPASSZ_BUF	RANGE_AUXADC					

BYPASSZ_BUF: Enables the high impedance input buffer.

RANGE_AUXADC: Sets the input full scale range of the Aux ADC. Default is 0-1.5V. Setting this bit to 1 makes the input full scale range 0-DVDD18.

Register Name – CONFIG137 – Address 0x370, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
	EN_AUX_ADC		MODE_INPUT<1:0>				

EN_AUX_ADC: Static control bit that “wakes up” the Aux ADC.

MODE_INPUT<1:0>: selects which of the 4 inputs (2 external and 2 internal) is multiplexed into the Aux ADC. Default is AUXADC_A.

MODE_INPUT<1:0>	AUX_ADC_INPUT
00	AUX_ADC_A
01	AUX_ADC_B

5.10 HALF DUPLEX MODE REGISTERS

Register Name – CONFIG138 – Address 0x24D, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
					REG_HALF_DUPLEX_ THRU_PIN		

REG_HALF_DUPLEX_THRU_PIN: Configures the PDN pin as a toggle pin between half duplex RX mode and half duplex TX mode. When this bit is set, a '1' on the PDN pin puts the device in half duplex RX mode (TX shutdown), and a '0' on the PDN pin puts the device in half duplex TX mode (RX shutdown).

5.11 LOW POWER RX CMOS MODE REGISTERS

In Low power CMOS mode, there are various ways to move output data of ADC with respect to output clock to achieve required setup and hold time. This can be done using following register.

Register Name – CONFIG139 – Address 0x33D, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
						DELAY_CLK_LP_CMOS<1:0>	

DELAY_CLK_LP_CMOS<1:0>: Programmable delay for the output clock (ADC_DCLKOUT) when in low power CMOS mode.

DELAY_CLK_LP_CMOS<1:0>	DELAY(1) (ns)
00	4*X - 0.3
01	5*X - 0.3
10	2*X - 0.3
11	3*X - 0.3

(1) X is the unit delay programmed by CHANGE_UNIT_DELAY<2:0> bits.

Register Name – CONFIG140 – Address 0x33F, Default = 0x00

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
DELAY_DATA_LP_CMOS<2:0>			CHANGE_UNIT_DELAY<2:0>				

CHANGE_UNIT_DELAY<2:0>: Changes the delay step for the DELAY_CLK_LP_CMOS and DELAY_DATA_LP_CMOS programming when in low power CMOS mode (MODE_LP_CMOS='1').

CHANGE_UNIT_DELAY<2:0>	DELAY UNIT "X" (ns)
000	1.12
001	1.5
010	0.55
011	0.9
100	1.85
101	2.2
110	1.25
111	1.62

DELAY_DATA_LP_CMOS<2:0>: Programmable delay for the output data when in low power CMOS mode (MODE_LP_CMOS='1').

DELAY_DATA_LP_CMOS<2:0>	DELAY(1) (ns)
000	4*X - 0.3
001	5*X - 0.3
010	6*X - 0.3
011	7*X - 0.3
100	NA
101	1*X - 0.3
110	2*X - 0.3
111	3*X - 0.3

(1) X is the unit delay programmed by CHANGE_UNIT_DELAY<2:0> bits.

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6 TYPICAL CHARACTERISTICS FOR AFE7222

6.1 RECEIVE PATH

All plots are at 25°C, AVDD18_ADC=1.8V, DVDD18_CLK=1.8V, DVDD18=1.8V, DVDD18_DAC=1.8V, AVDD3_DAC=3.0V, AVDD3_AUX=3.0V, maximum rated clock frequency, sine wave input clock. 1.5 VPP differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, 0 dB gain, CMOS output interface for AFE7222, 32k point FFT (unless otherwise noted)

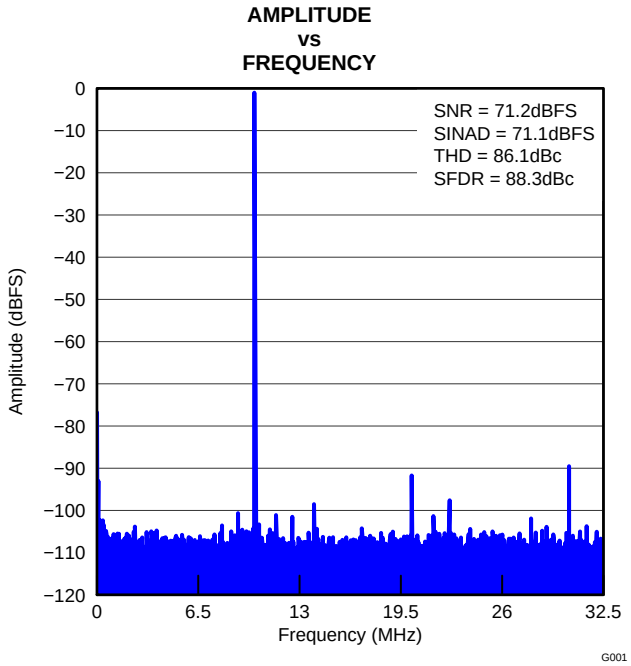

Figure 6-1. FFT Plot 10MHz 65MSPS

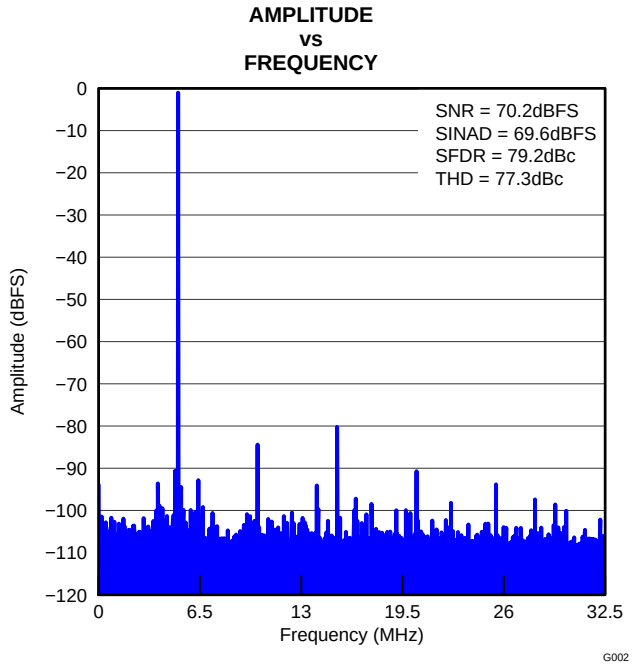

Figure 6-2. FFT Plot 70MHz 65MSPS

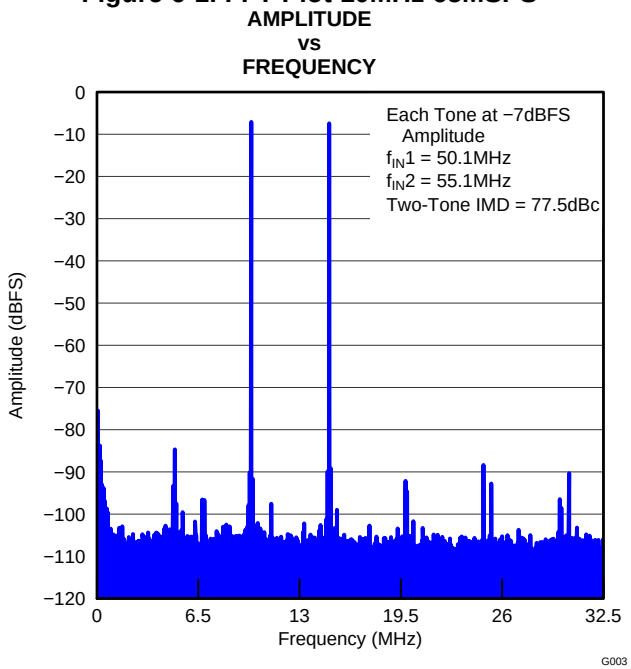

Figure 6-3. FFT Two-Tone Signal

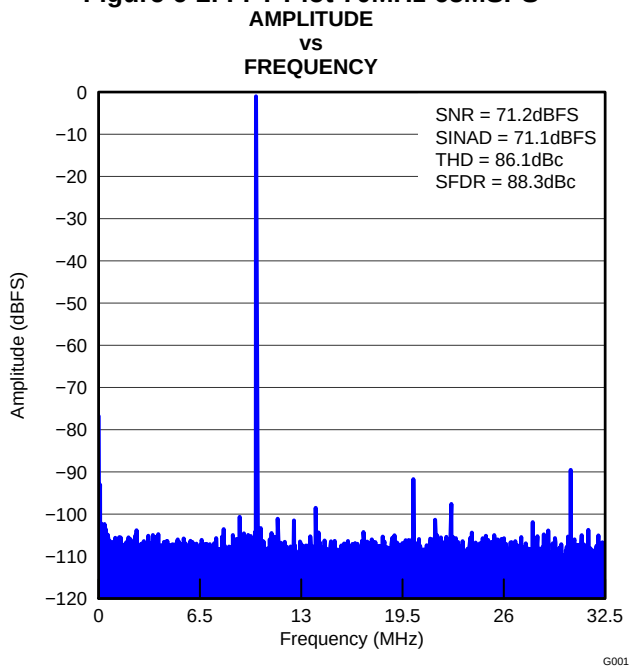

Figure 6-4. Spectrum With Decimation Filter OFF

All plots are at 25°C, AVDD18_ADC=1.8V, DVDD18_CLK=1.8V, DVDD18=1.8V, DVDD18_DAC=1.8V, AVDD3_DAC=3.0V, AVDD3_AUX=3.0V, maximum rated clock frequency, sine wave input clock. 1.5 VPP differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, 0 dB gain, CMOS output interface for AFE7222, 32k point FFT (unless otherwise noted)

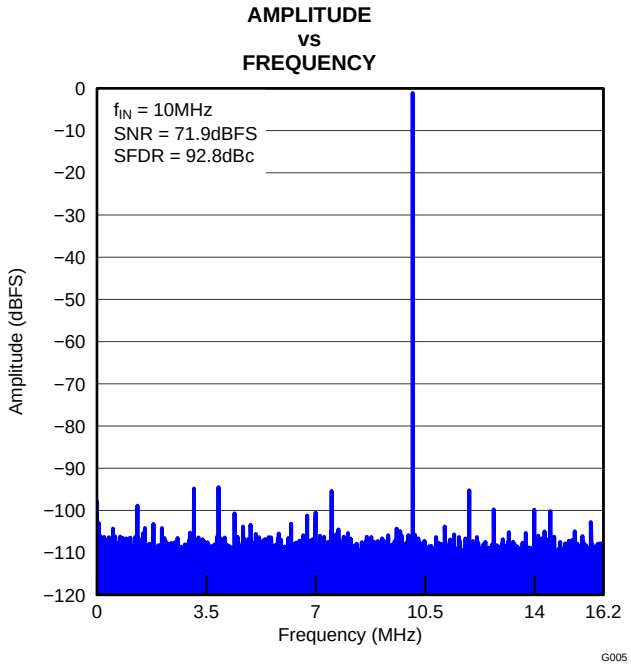

Figure 6-5. Spectrum With Decimation Filter ON

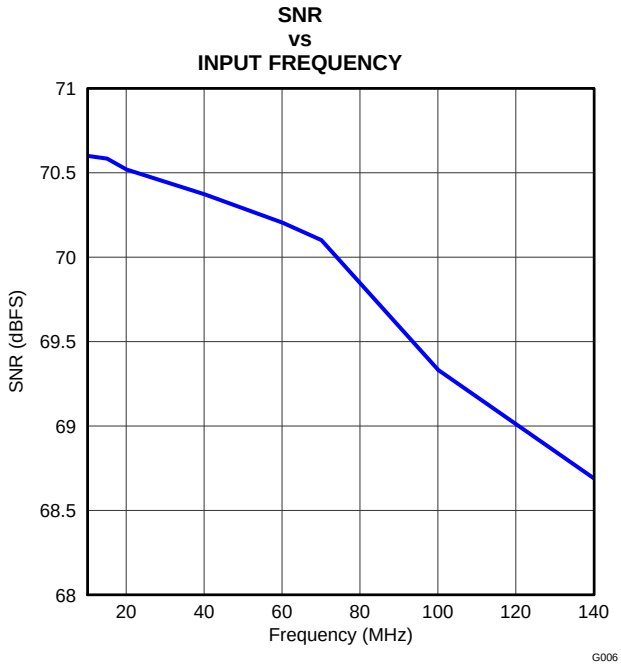

Figure 6-6. SNR vs Input Frequency

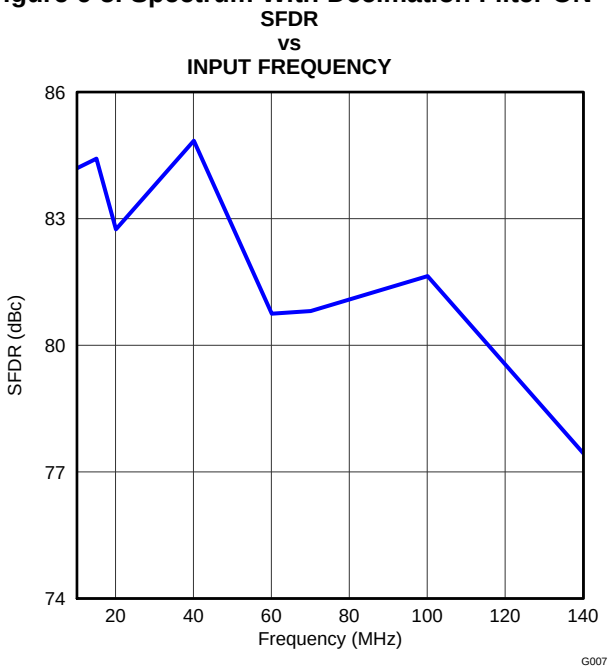

Figure 6-7. SFDR vs Input Frequency

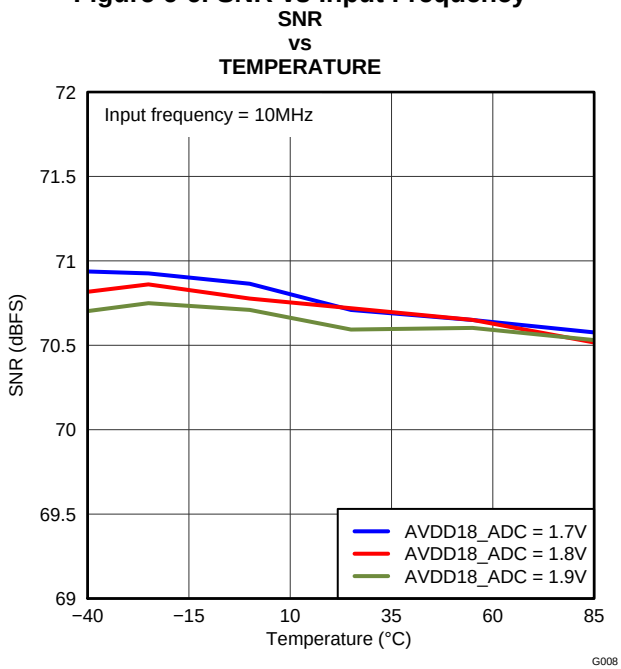

Figure 6-8. SNR Across Temperature and ADC Analog Supply

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All plots are at 25°C, AVDD18_ADC=1.8V, DVDD18_CLK=1.8V, DVDD18=1.8V, DVDD18_DAC=1.8V, AVDD3_DAC=3.0V, AVDD3_AUX=3.0V, maximum rated clock frequency, sine wave input clock. 1.5 VPP differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, 0 dB gain, CMOS output interface for AFE7222, 32k point FFT (unless otherwise noted)

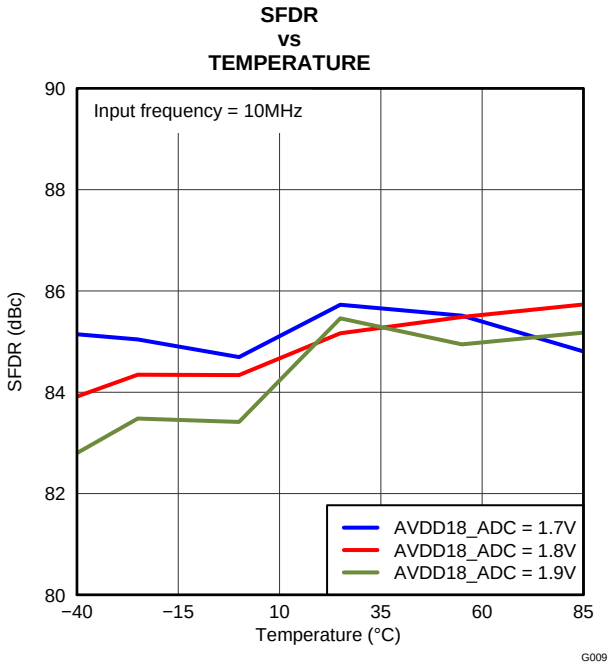

Figure 6-9. SFDR vs Temperature

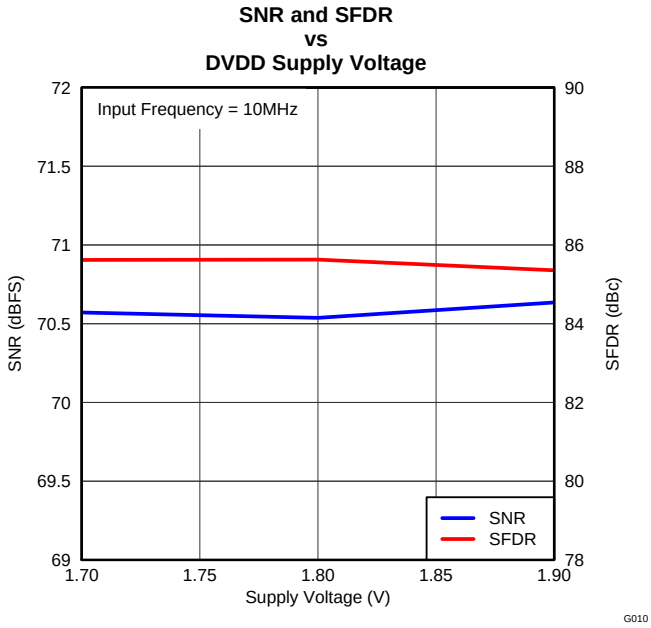

Figure 6-10. Performance Across DVDD Supply Voltage

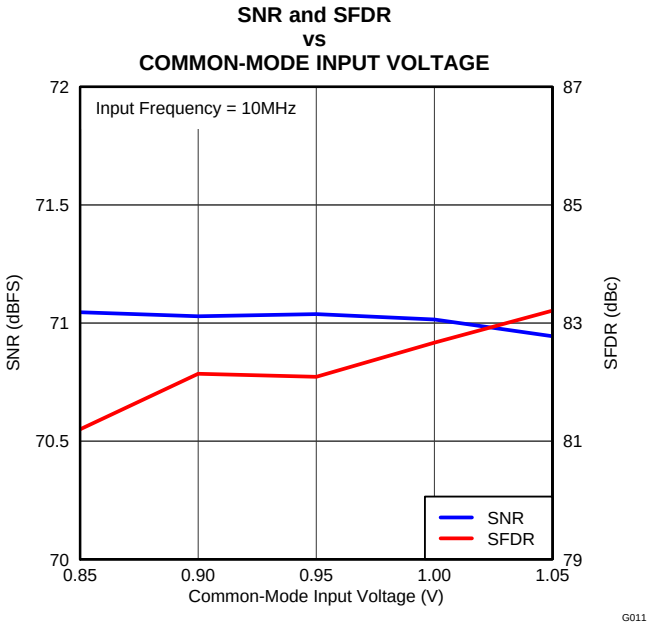

Figure 6-11. Performance Across Common-Mode Input Voltage

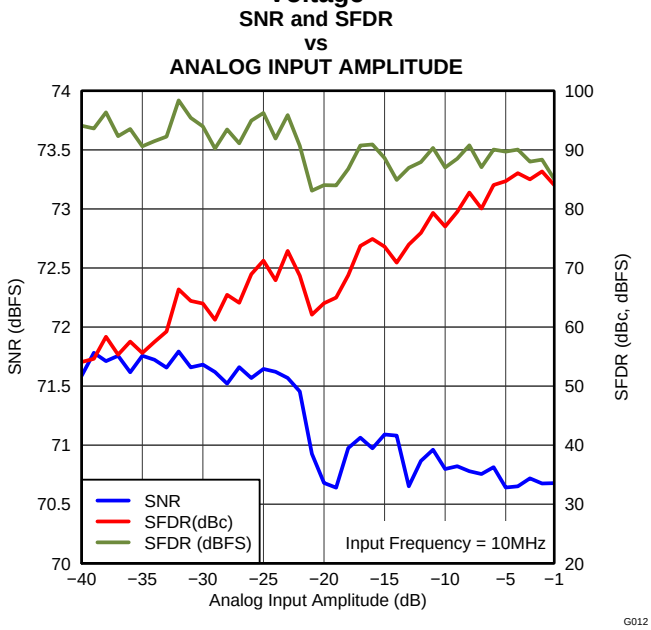

Figure 6-12. Performance Across Input Amplitude

All plots are at 25°C, AVDD18_ADC=1.8V, DVDD18_CLK=1.8V, DVDD18=1.8V, DVDD18_DAC=1.8V, AVDD3_DAC=3.0V, AVDD3_AUX=3.0V, maximum rated clock frequency, sine wave input clock. 1.5 VPP differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, 0 dB gain, CMOS output interface for AFE7222, 32k point FFT (unless otherwise noted)

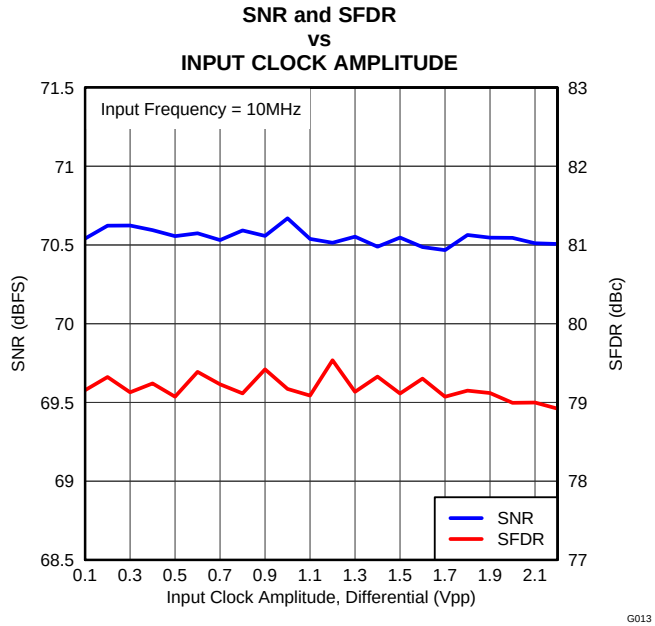

Figure 6-13. Performance Across Input Clock Amplitude

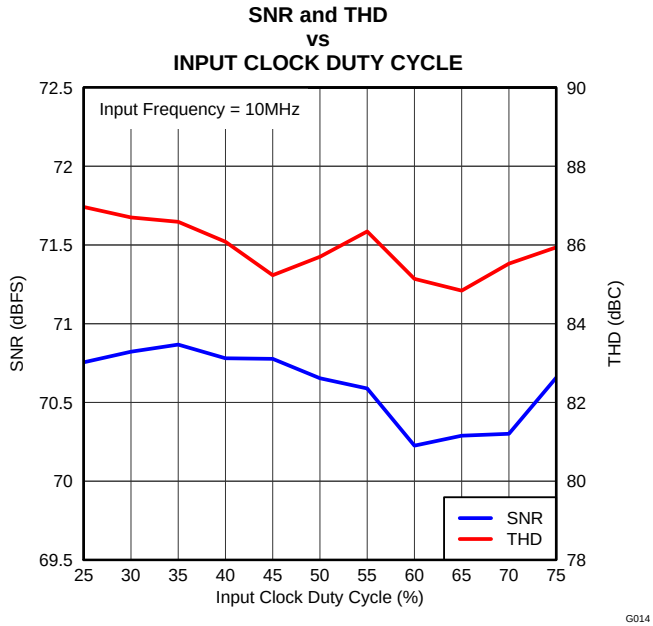

Figure 6-14. Performance Across Input Clock Duty Cycle

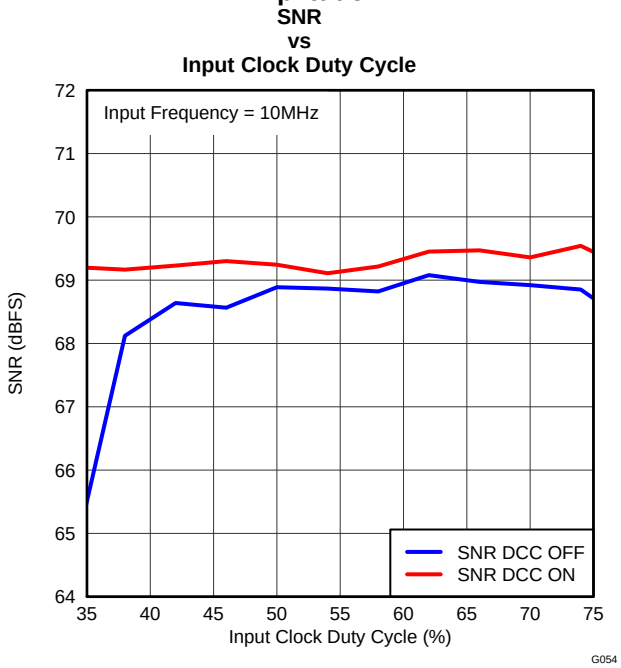

Figure 6-15. SNR vs Input Clock Duty Cycle

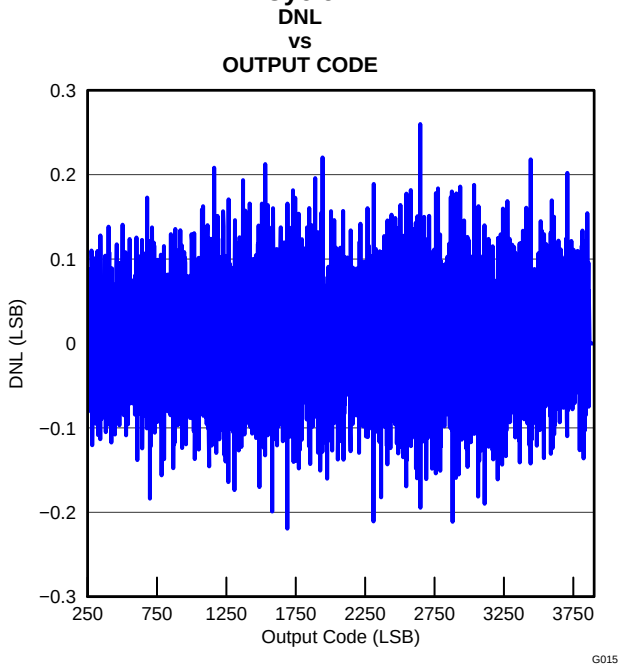

Figure 6-16. DNL Plot

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All plots are at 25°C, AVDD18_ADC=1.8V, DVDD18_CLK=1.8V, DVDD18=1.8V, DVDD18_DAC=1.8V, AVDD3_DAC=3.0V, AVDD3_AUX=3.0V, maximum rated clock frequency, sine wave input clock. 1.5 VPP differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, 0 dB gain, CMOS output interface for AFE7222, 32k point FFT (unless otherwise noted)

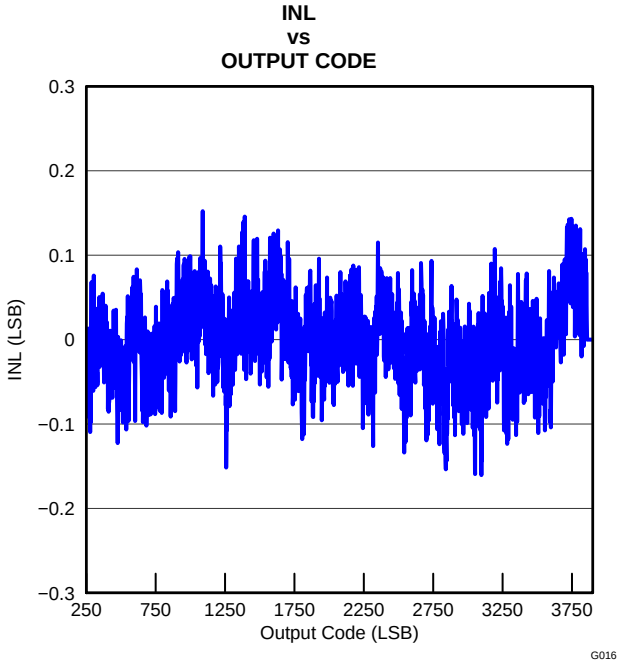

Figure 6-17. INL Plot

6.2 TRANSMIT PATH

All plots are at 25°C, AVDD18_ADC=1.8V, DVDD18_CLK=1.8V, DVDD18=1.8V, DVDD18_DAC=1.8V, AVDD3_DAC=3.0V, AVDD3_AUX=3.0V, maximum rated clock frequency, sine wave input clock. 1.5 VPP differential clock amplitude, 50% clock duty cycle, 0 dBFS digital input, 0 dB gain, CMOS input interface for AFE7222, 32k point FFT (unless otherwise noted)

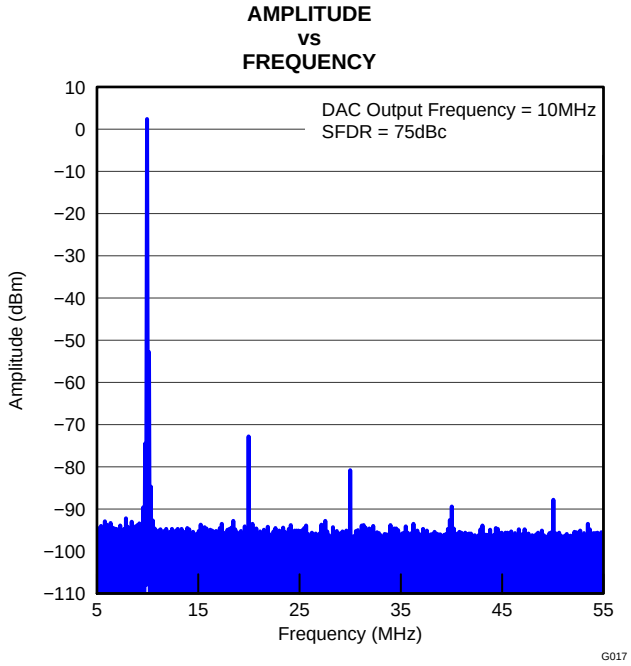

Figure 6-18. Spectrum Analyzer Plot CMOS Mode 10MHz IF

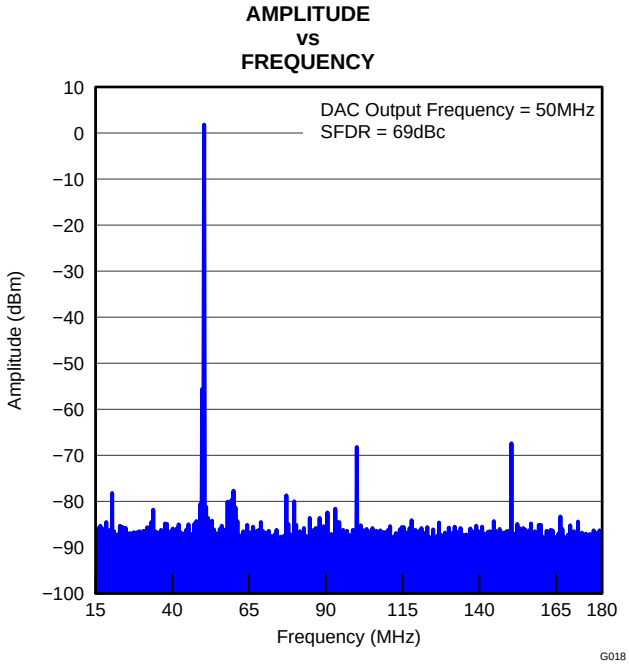

Figure 6-19. Spectrum Analyzer Plot CMOS Mode 50MHz IF

All plots are at 25°C, AVDD18_ADC=1.8V, DVDD18_CLK=1.8V, DVDD18=1.8V, DVDD18_DAC=1.8V, AVDD3_DAC=3.0V, AVDD3_AUX=3.0V, maximum rated clock frequency, sine wave input clock. 1.5 VPP differential clock amplitude, 50% clock duty cycle, 0 dBFS digital input, 0 dB gain, CMOS input interface for AFE7222, 32k point FFT (unless otherwise noted)

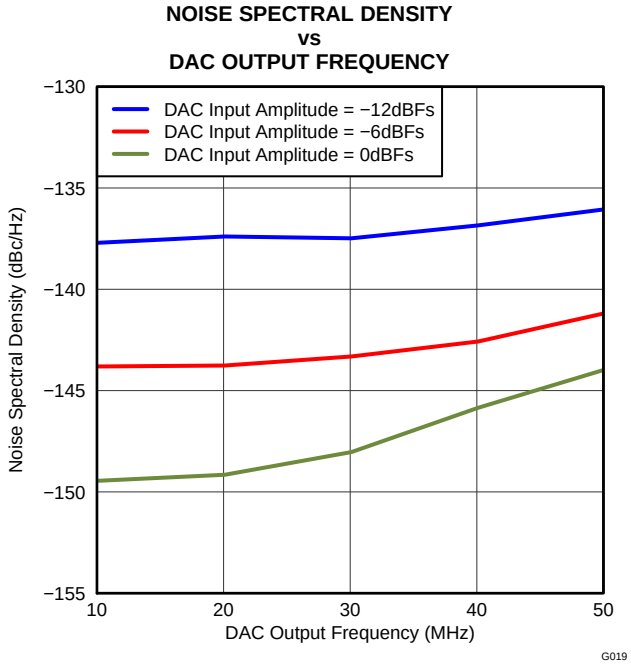

Figure 6-20. NSD vs Frequency Across Input Scale

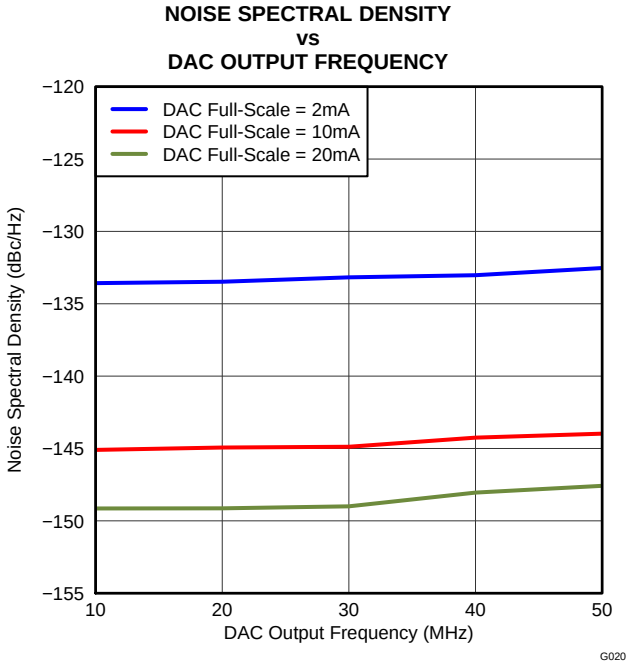

Figure 6-21. NSD Vs Iouts

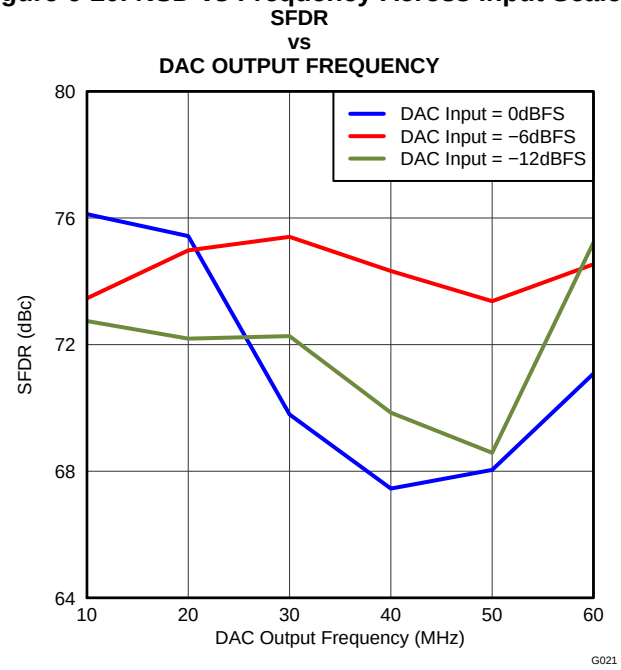

Figure 6-22. SFDR vs Frequency

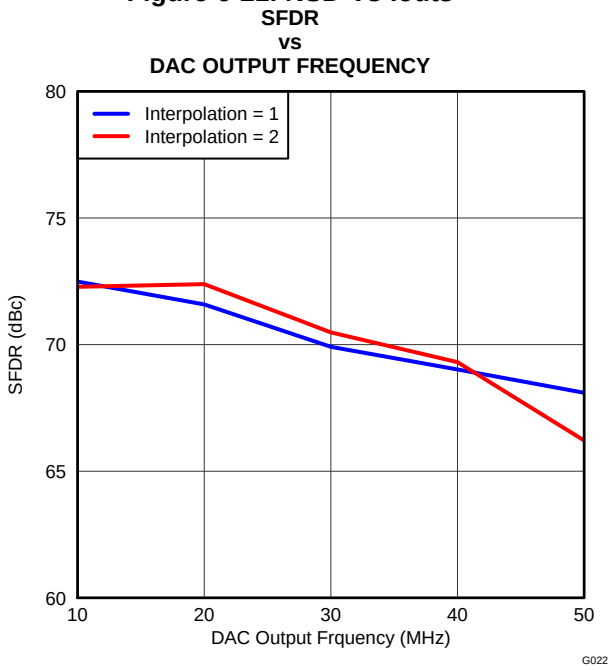

Figure 6-23. SFDR vs Interpolation

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All plots are at 25°C, AVDD18_ADC=1.8V, DVDD18_CLK=1.8V, DVDD18=1.8V, DVDD18_DAC=1.8V, AVDD3_DAC=3.0V, AVDD3_AUX=3.0V, maximum rated clock frequency, sine wave input clock. 1.5 VPP differential clock amplitude, 50% clock duty cycle, 0 dBFS digital input, 0 dB gain, CMOS input interface for AFE7222, 32k point FFT (unless otherwise noted)

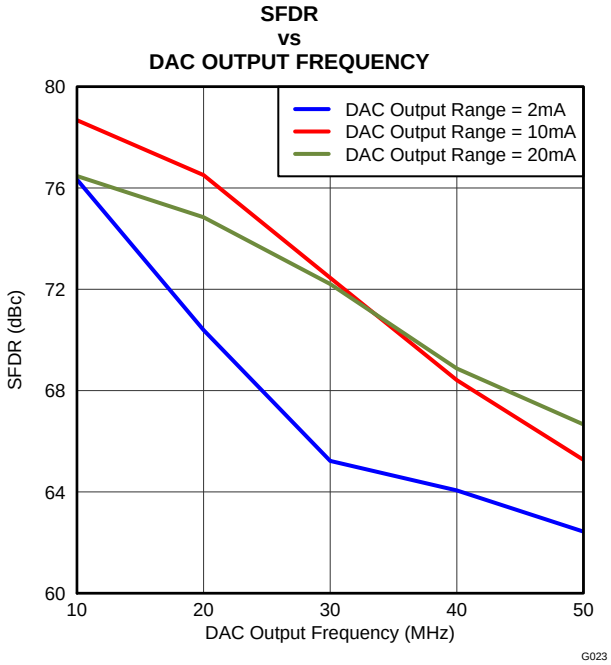

Figure 6-24. SFDR Vs IOUTFS

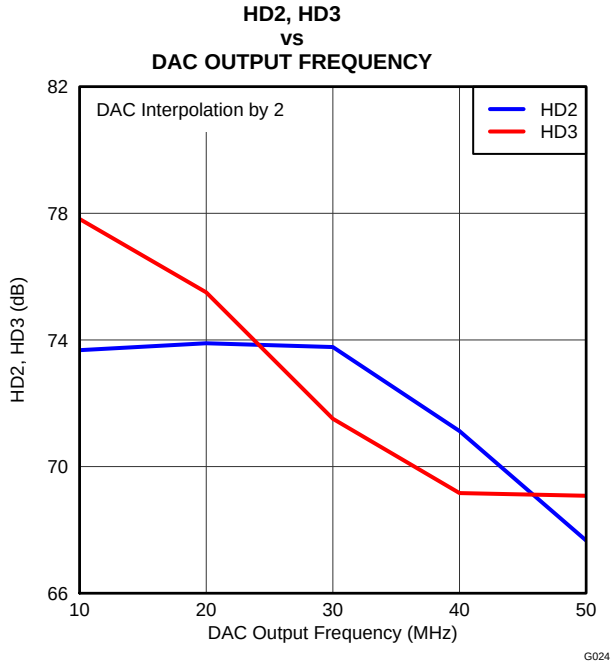

Figure 6-25. HD2, HD3 Across Frequency

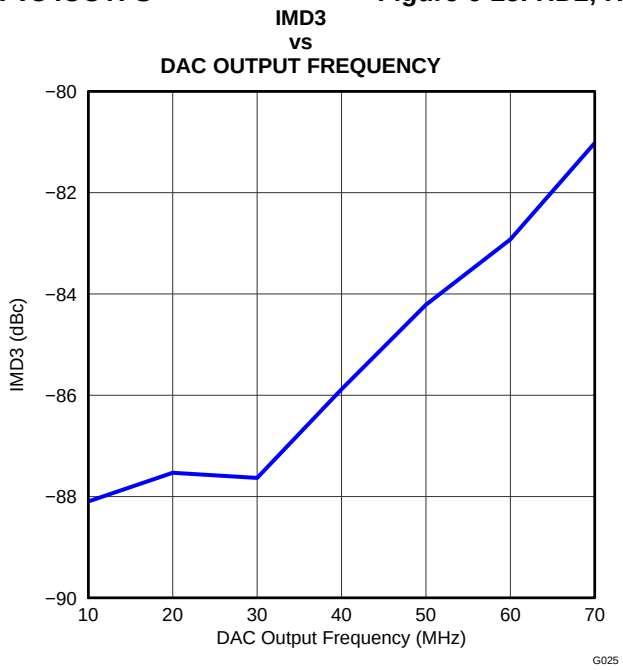

Figure 6-26. IMD3 vs Frequency CMOS

7 TYPICAL CHARACTERISTICS FOR AFE7225

7.1 RECEIVE PATH

All plots are at 25°C, AVDD18_ADC=1.8V, DVDD18_CLK=1.8V, DVDD18=1.8V, DVDD18_DAC=1.8V, AVDD3_DAC=3.0V, AVDD3_AUX=3.0V, maximum rated clock frequency, sine wave input clock. 1.5 VPP differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, 0 dB gain, LVDS output interface for AFE7225, 32k point FFT (unless otherwise noted)

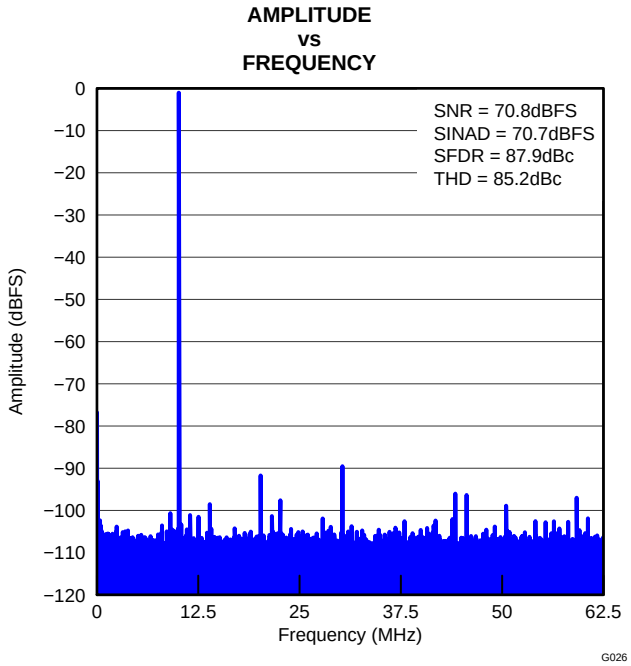

Figure 7-1. FFT Plot 10MHz 125MSPS

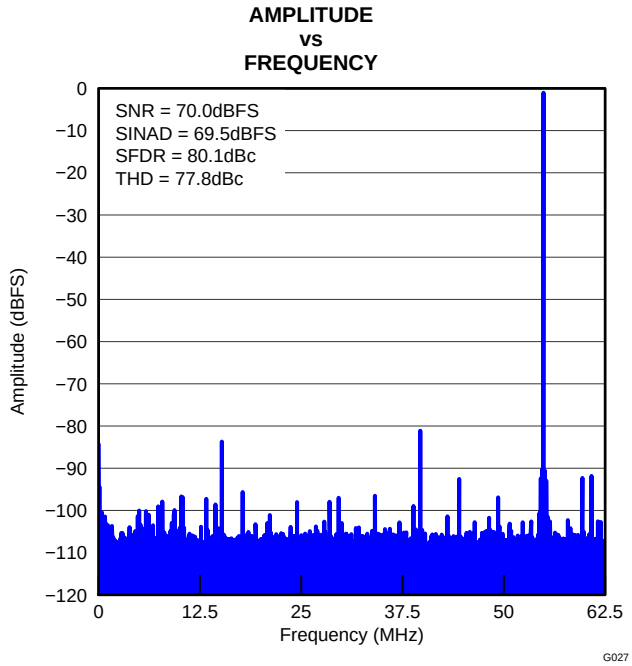

Figure 7-2. FFT Plot 70MHz 125MSPS

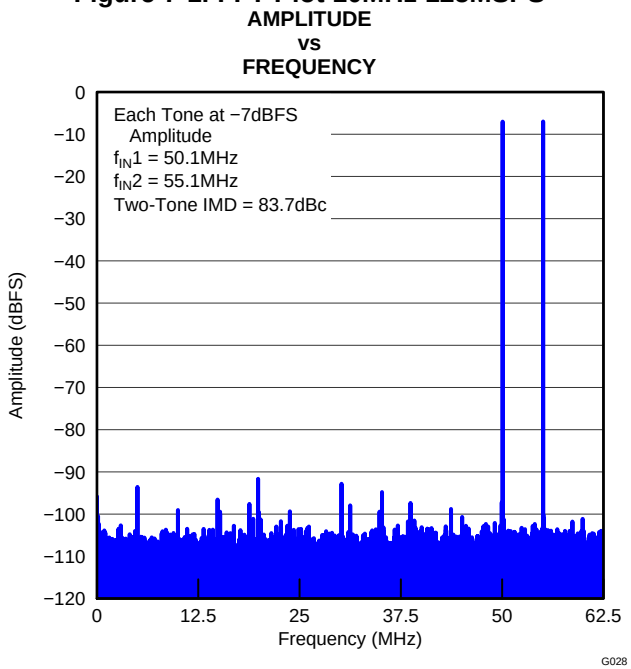

Figure 7-3. FFT Two-Tone Signal

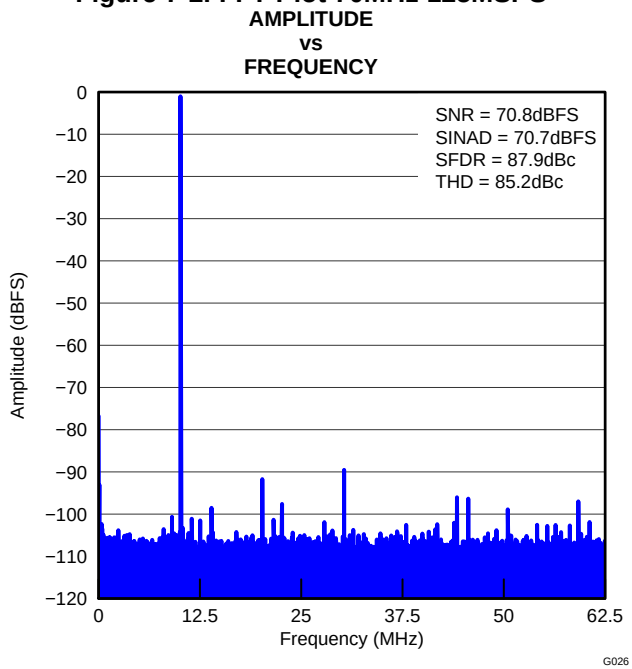

Figure 7-4. Spectrum With Decimation Filter OFF

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All plots are at 25°C, AVDD18_ADC=1.8V, DVDD18_CLK=1.8V, DVDD18=1.8V, DVDD18_DAC=1.8V, AVDD3_DAC=3.0V, AVDD3_AUX=3.0V, maximum rated clock frequency, sine wave input clock. 1.5 VPP differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, 0 dB gain, LVDS output interface for AFE7225, 32k point FFT (unless otherwise noted)

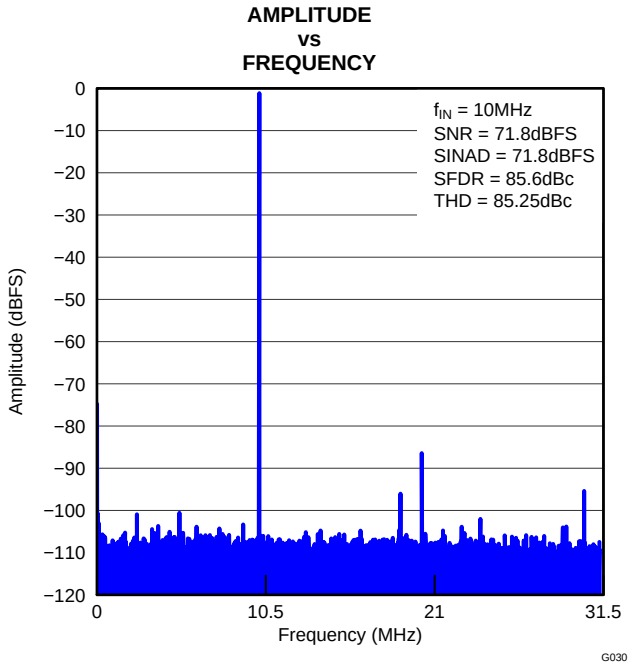

Figure 7-5. Spectrum With Decimation Filter ON

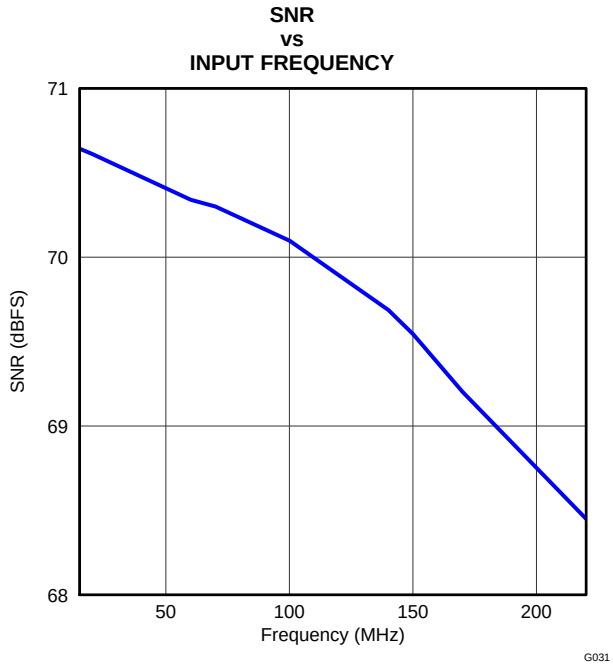

Figure 7-6. SNR vs Input Frequency

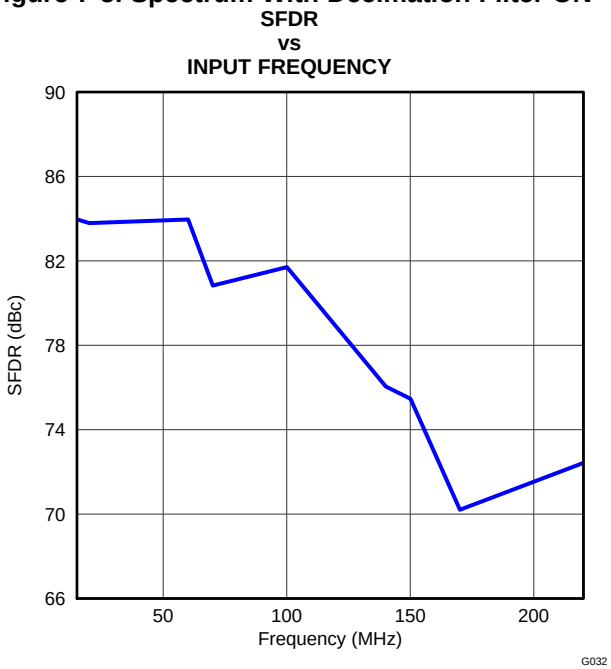

Figure 7-7. SFDR vs Input Frequency

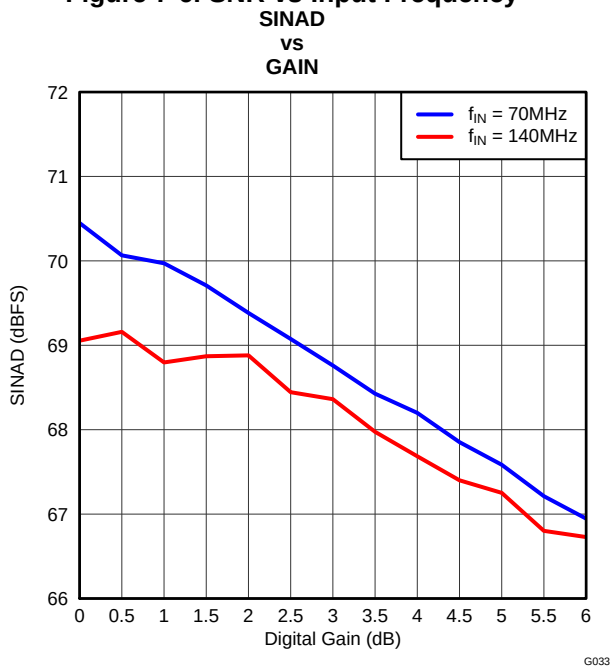

Figure 7-8. SINAD Across Gain

All plots are at 25°C, AVDD18_ADC=1.8V, DVDD18_CLK=1.8V, DVDD18=1.8V, DVDD18_DAC=1.8V, AVDD3_DAC=3.0V, AVDD3_AUX=3.0V, maximum rated clock frequency, sine wave input clock. 1.5 VPP differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, 0 dB gain, LVDS output interface for AFE7225, 32k point FFT (unless otherwise noted)

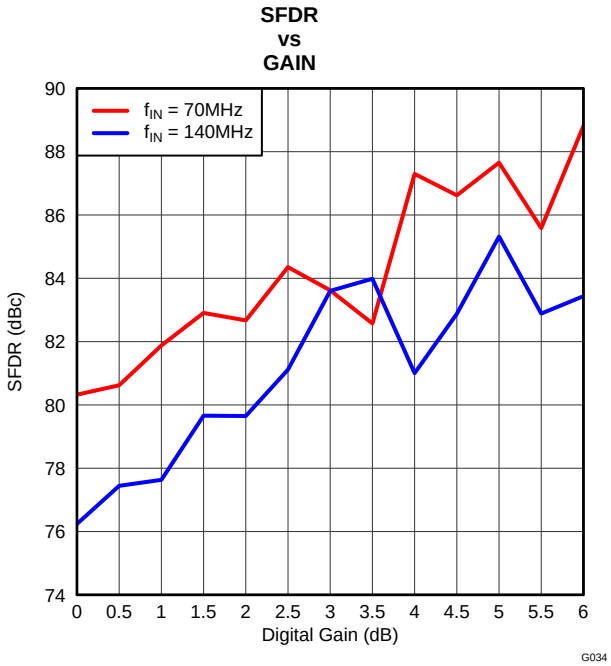

Figure 7-9. SFDR vs Gain

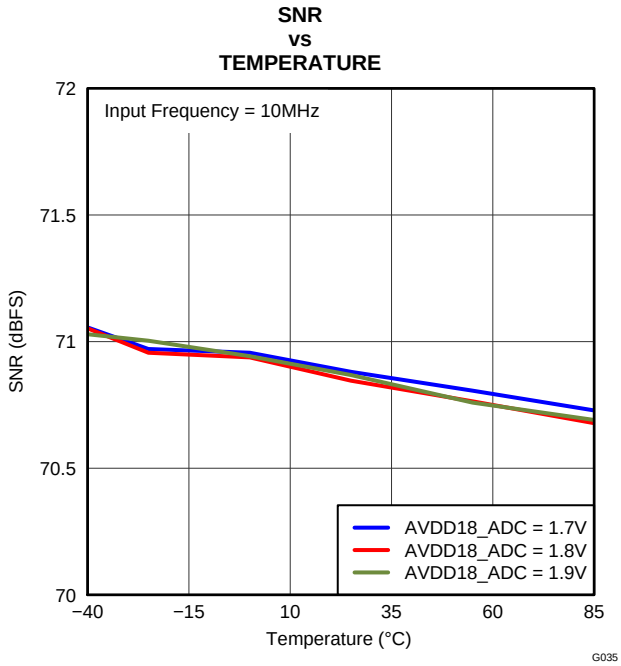

Figure 7-10. SNR Across Temperature and ADC Analog Supply

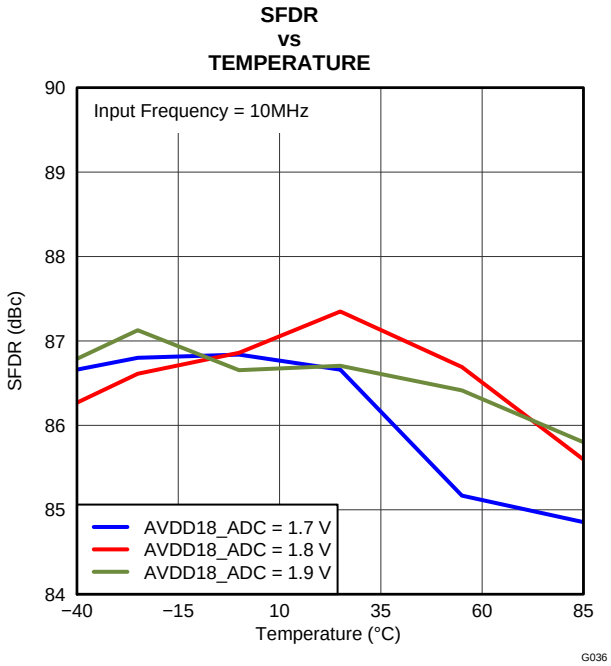

Figure 7-11. SFDR Across Temperature and ADC Analog Supply

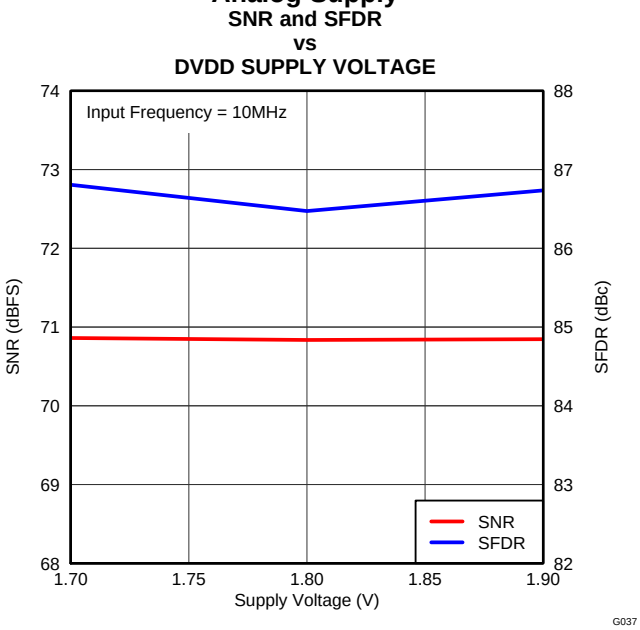

Figure 7-12. Performance Across DVDD Supply Voltage

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All plots are at 25°C, AVDD18_ADC=1.8V, DVDD18_CLK=1.8V, DVDD18=1.8V, DVDD18_DAC=1.8V, AVDD3_DAC=3.0V, AVDD3_AUX=3.0V, maximum rated clock frequency, sine wave input clock. 1.5 VPP differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, 0 dB gain, LVDS output interface for AFE7225, 32k point FFT (unless otherwise noted)

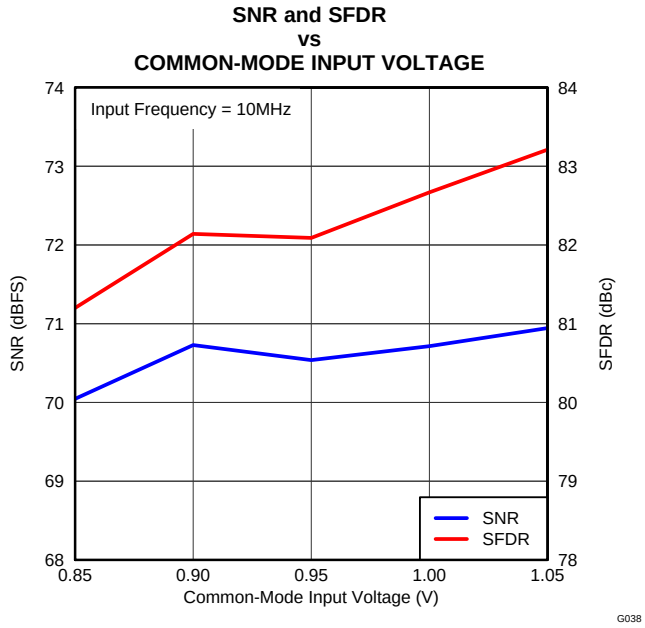

Figure 7-13. Performance Across Common-Mode Input Voltage

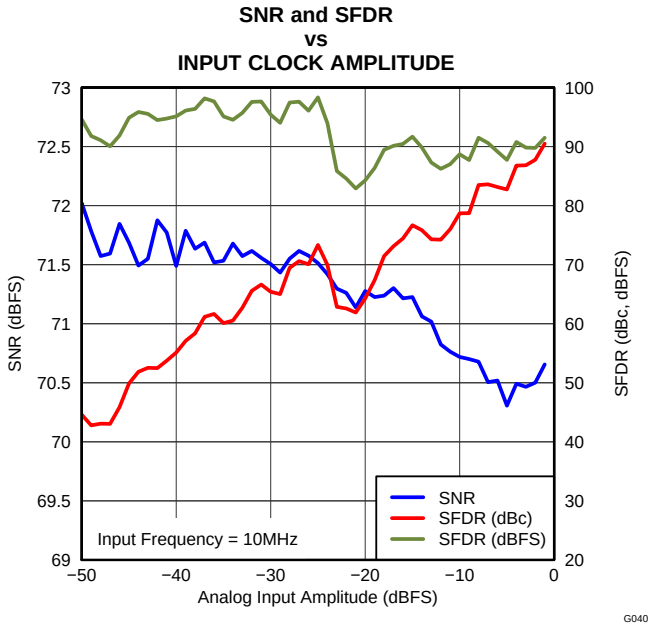

Figure 7-14. Performance Across Input Clock Amplitude

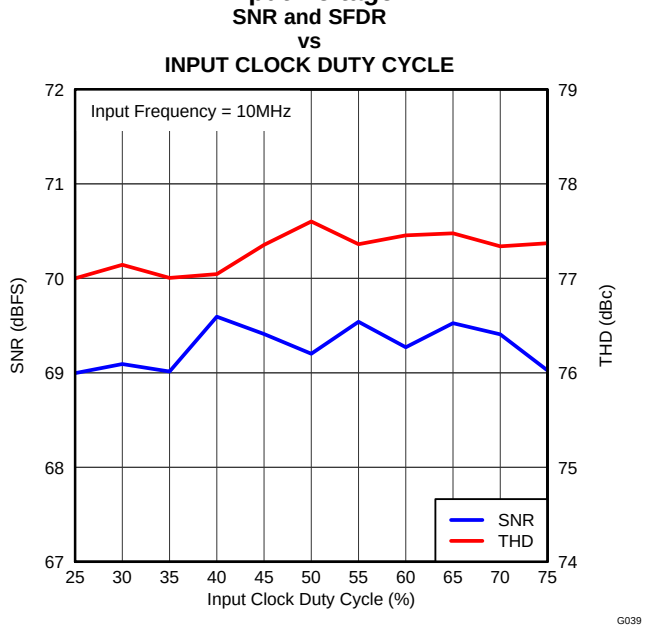

Figure 7-15. Performance Across Input Clock Duty Cycle

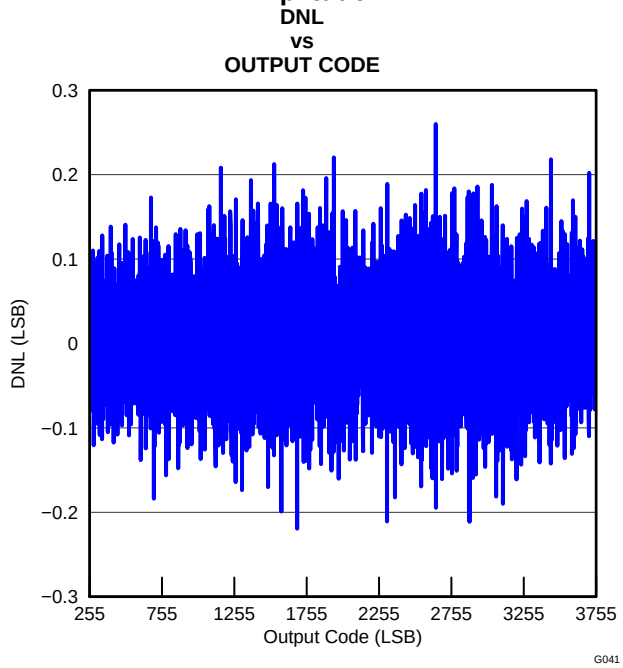

Figure 7-16. DNL Plot

All plots are at 25°C, AVDD18_ADC=1.8V, DVDD18_CLK=1.8V, DVDD18=1.8V, DVDD18_DAC=1.8V, AVDD3_DAC=3.0V, AVDD3_AUX=3.0V, maximum rated clock frequency, sine wave input clock. 1.5 VPP differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, 0 dB gain, LVDS output interface for AFE7225, 32k point FFT (unless otherwise noted)

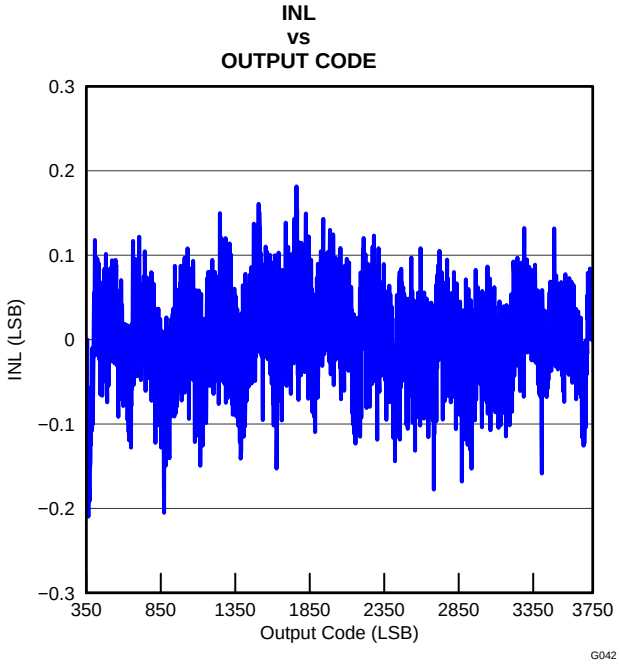

Figure 7-17. INL Plot

7.2 TRANSMIT PATH

All plots are at 25°C, AVDD18_ADC=1.8V, DVDD18_CLK=1.8V, DVDD18=1.8V, DVDD18_DAC=1.8V, AVDD3_DAC=3.0V, AVDD3_AUX=3.0V, maximum rated clock frequency, sine wave input clock. 1.5 VPP differential clock amplitude, 50% clock duty cycle, 0 dBFS digital input, 0 dB gain, LVDS input interface for AFE7225, 32k point FFT (unless otherwise noted)

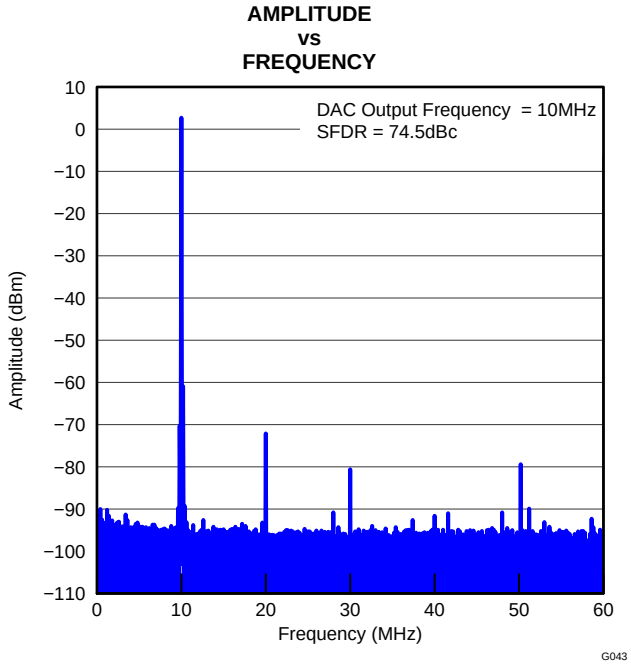

Figure 7-18. Spectrum Analyzer Plot LVDS Mode 10MHz IF

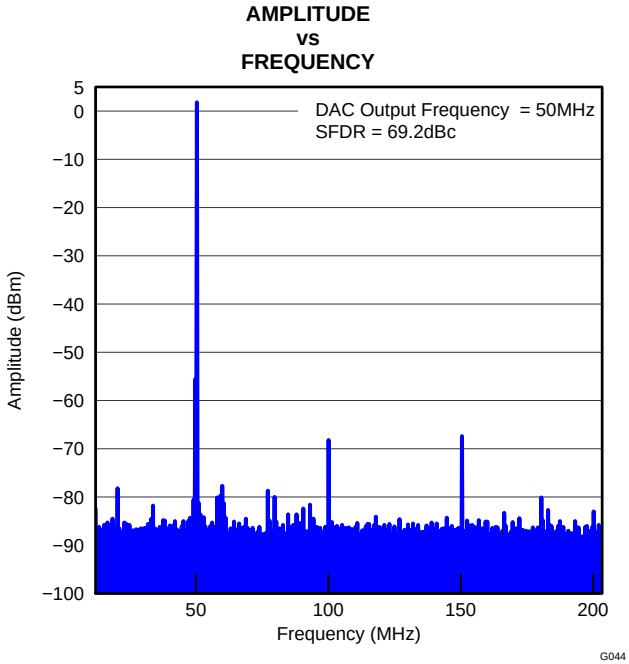

Figure 7-19. Spectrum Analyzer Plot LVDS Mode 50MHz IF

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All plots are at 25°C, AVDD18_ADC=1.8V, DVDD18_CLK=1.8V, DVDD18=1.8V, DVDD18_DAC=1.8V, AVDD3_DAC=3.0V, AVDD3_AUX=3.0V, maximum rated clock frequency, sine wave input clock. 1.5 VPP differential clock amplitude, 50% clock duty cycle, 0 dBFS digital input, 0 dB gain, LVDS input interface for AFE7225, 32k point FFT (unless otherwise noted)

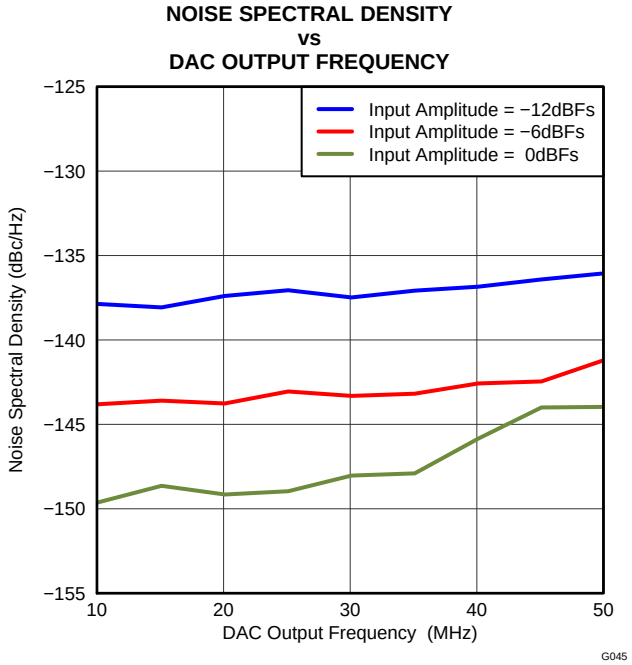

Figure 7-20. NSD vs Frequency Across Input Scale

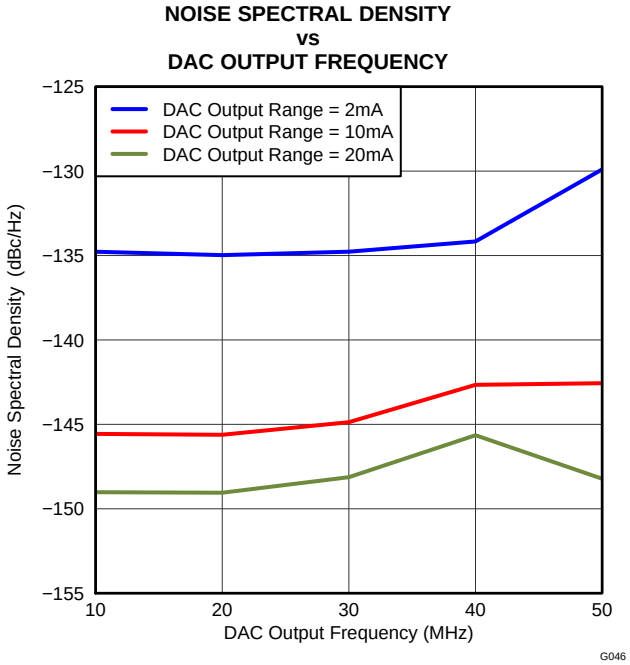

Figure 7-21. NSD Vs Iouts

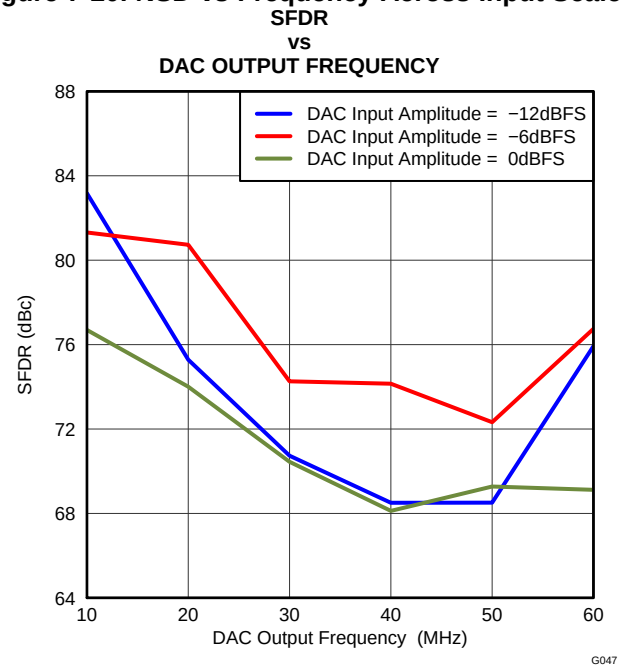

Figure 7-22. SFDR vs Frequency

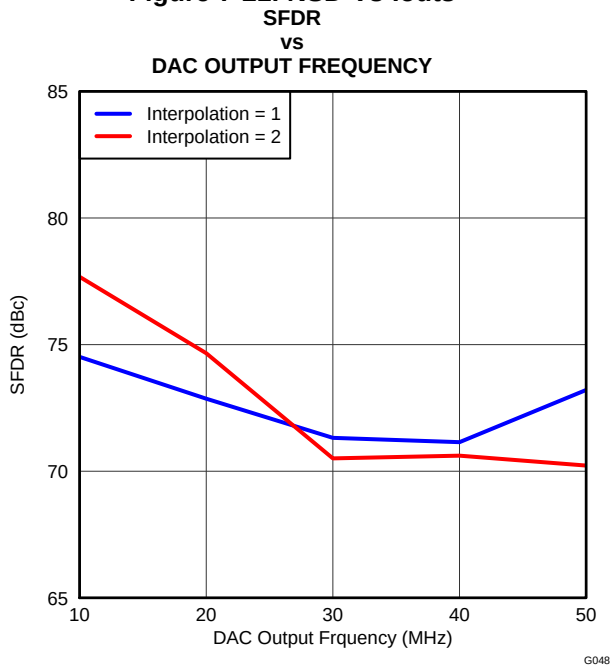

Figure 7-23. SFDR vs Interpolation

All plots are at 25°C, AVDD18_ADC=1.8V, DVDD18_CLK=1.8V, DVDD18=1.8V, DVDD18_DAC=1.8V, AVDD3_DAC=3.0V, AVDD3_AUX=3.0V, maximum rated clock frequency, sine wave input clock. 1.5 VPP differential clock amplitude, 50% clock duty cycle, 0 dBFS digital input, 0 dB gain, LVDS input interface for AFE7225, 32k point FFT (unless otherwise noted)

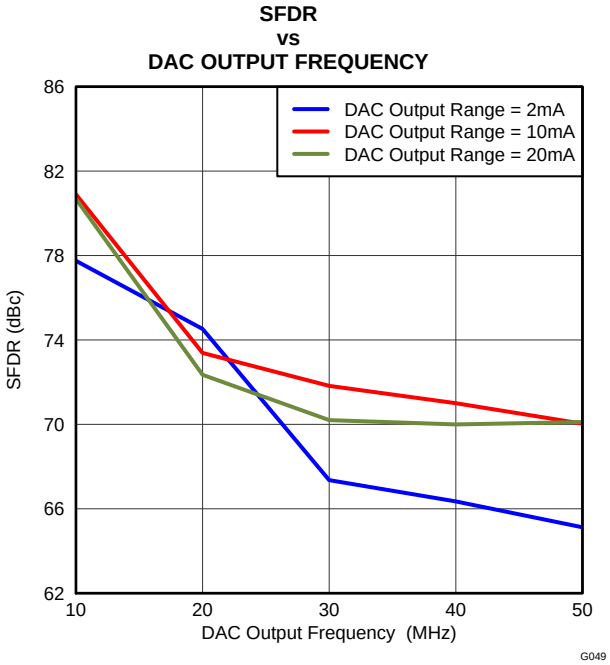

Figure 7-24. SFDR Vs IOUTFS

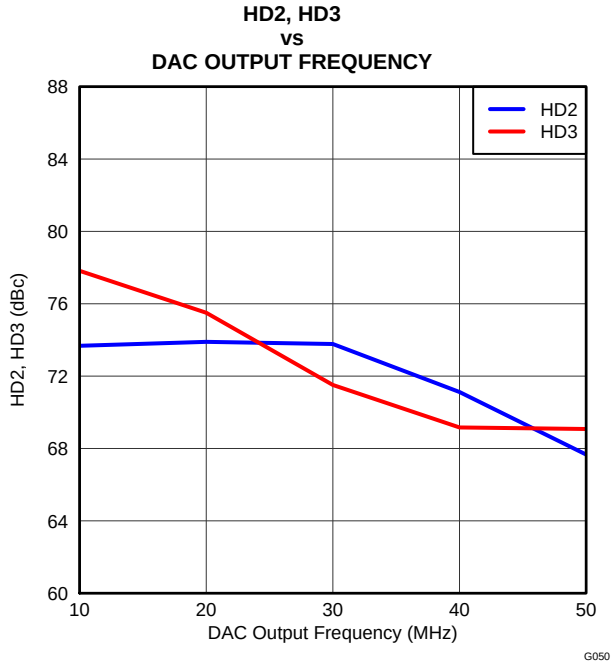

Figure 7-25. HD2, HD3 Across Frequency

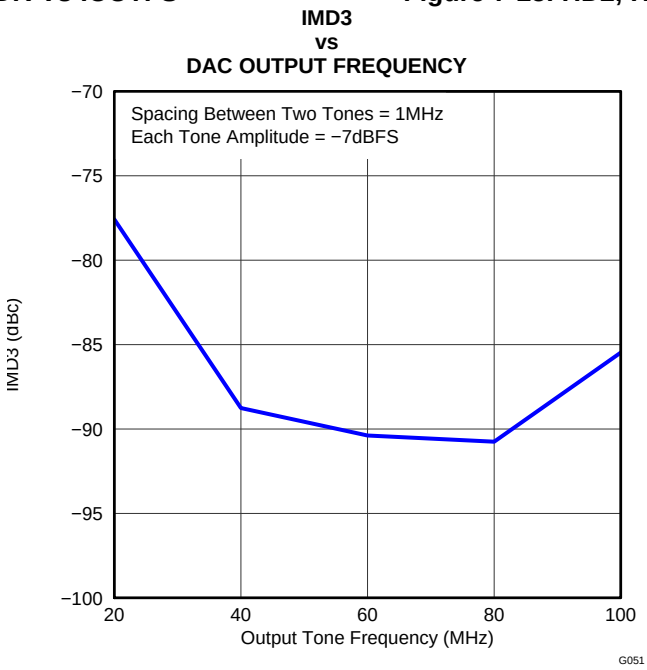

Figure 7-26. IMD3 vs Frequency

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8 TYPICAL CHARACTERISTICS FOR COMMON PLOTS

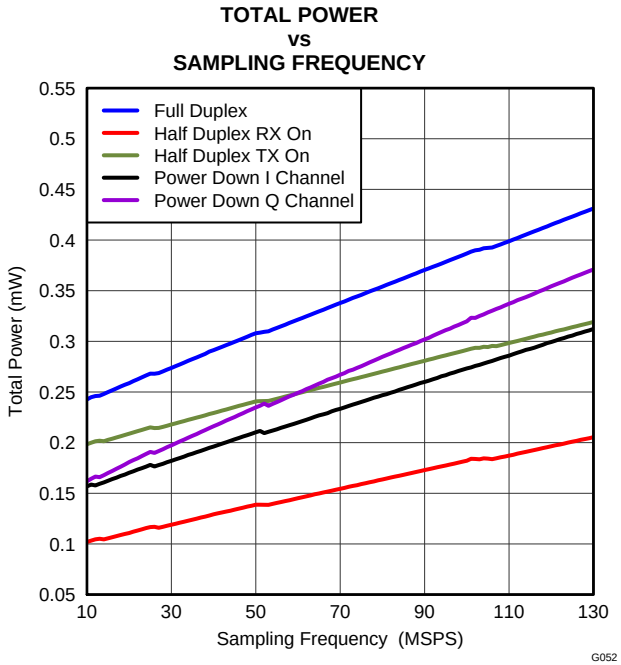

Figure 8-1. Power vs fclk CMOS

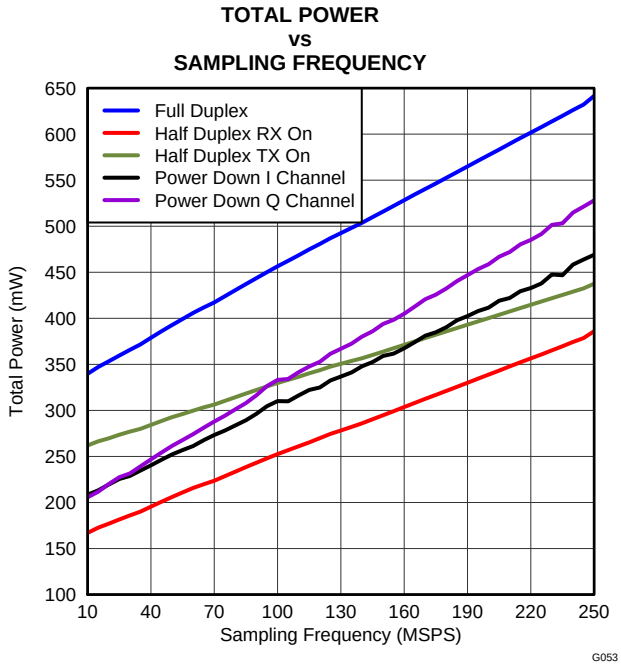

Figure 8-2. Power vs fclk 2-Wire LVDS

9 APPLICATION INFORMATION

9.1 DEVICE DESCRIPTION

The AFE7225/7222 is designed to offer small footprint, high performance, low power and flexibility in applications that require half or full duplex software defined radios. The receive path consists of dual 12-bit 125MSPS ADCs, a digital quadrature modulation correction block, FCLK/4 digital frequency shifter and /2 decimation filter. The transmit path consists of dual 12-bit 250MSPS DACs, a digital quadrature modulation correction block, FCLK /4 digital frequency shifter, and x2/x4 interpolation filters as well as a FIFO. A peak/rms power meter is available to the receive path. Fine Mixers with NCOs are available for both receive and transmit path. These NCOs can be programmed independently. The primary digital interface is selectable as either interleaved parallel CMOS or serialized LVDS. Device control is provided via SPI (serial peripheral interface).

An auxiliary 12-bit 100kSPS ADC with two single-ended voltage inputs via a multiplexer is provided for voltage monitoring. A dual auxiliary 12-bit 2MSPS single-ended current source output DAC is available for control and/or board calibration. Most blocks can be independently powered on/off as needed to save power. All of this capability is available in a small 9mm x 9mm 64-pin QFN package.

9.2 RECEIVER SIGNAL CHAIN

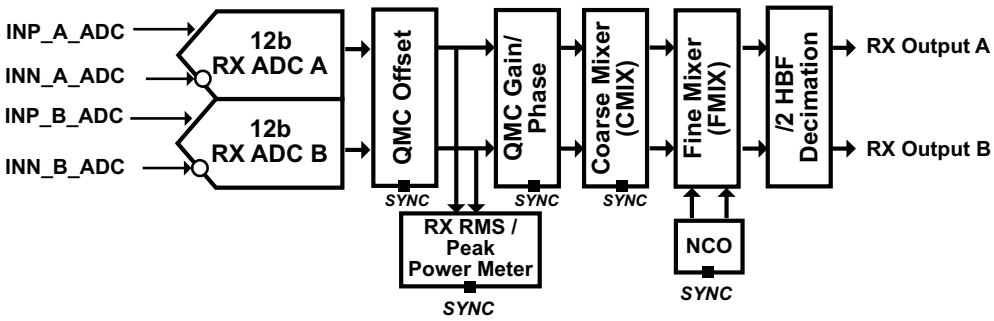

Figure 9-1. Signal Chain

9.3 RECEIVE ADC

The dual receive ADCs are created using a pipeline architecture and are powered from a 1.8V analog supply (AVDD18_ADC). The common-mode of the differential inputs is 0.95V. A VCM pin is provided which outputs the common-mode voltage for use in setting up the proper input level. If the VCM pin cannot be used in your application, ensure that the analog inputs are centered at 0.95V. The full scale range of the inputs is 2.0Vpp differential, or 0.95 ± 0.5V on both INN and INP pins.

The receive ADCs are capable of under-sampling intermediate frequencies (IF) at high frequency. The 3dB full power input bandwidth (FPBW) is approximately 550MHz. Good distortion and noise is maintained to ~230MHz. The dual ADCs can be used to capture complex I/Q inputs from a quadrature demodulator, or two independent IFs or used in a diversity configuration. In order to obey the Nyquist-Shannon sampling theorem, ensure that the bandwidth to be sampled does not exceed FADCCLK/2. An external anti-aliasing filter is recommended that confines the analog input energy to a single Nyquist band (multiple of FADCCLK/2) to avoid unwanted aliasing and reduced overall performance.

9.4 RECEIVE DECIMATION FILTER

The user has the option of a decimation filter in the receive data path. The decimation filter can be used to reduce the ADC data sample rate by half. The extra sampling bandwidth could be used for processing gain and to ease the roll-off requirements of an external anti-aliasing filter. The decimation filter is a 43 tap half-band filter. The transition band is from 0.38 to 0.62 of $F_{ADCCLK}/4$, and the stop band attenuation is greater than 80dB. The pass-band ripple is less than 0.1dB. Coefficients 1 to 22 are listed. Coefficients 23 to 43 are the same as those from 22 to 1.

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RXFIR (decimation filter)
coefficients = [+9 0 –33 0 +88 0 –196 0 +387 0 –704 0 +1210 0 –2024 0 +3432 0 –6485 0 +20700 +32768]

The frequency response of the filter is shown below.

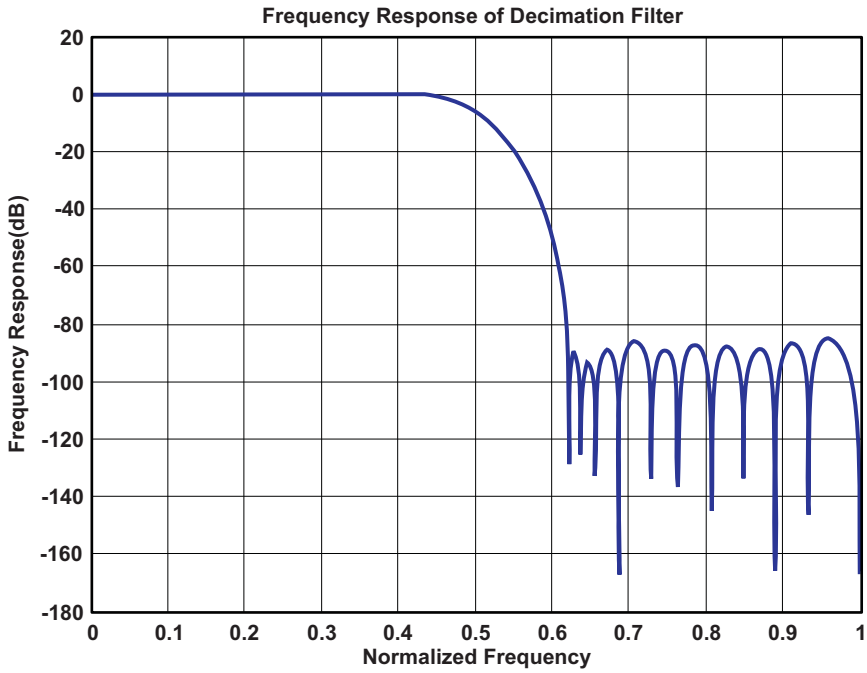

Figure 9-2. Decimation Filter Frequency Response (from 0 to $F_{ADCCLK}/2$)

9.5 RECEIVE FINE FREQUENCY MIXER (FMIX)

The fine mixer uses a Numerically Controlled Oscillator (NCO) to generate two complementary outputs of a finely programmable frequency, which is then mixed with the A and B inputs to generate complex outputs.

The mixer computes two outputs as follows:
Output I = $\{A\cos(\omega_{mix}t) - B\sin(\omega_{mix}t)\}$ and
Output Q = $\{A\sin(\omega_{mix}t) + B\cos(\omega_{mix}t)\}$
where ω_{mix} is the programmed fine frequency.

The NCO has a 32 bit frequency register, and a 20 bit phase register. The 32 bit frequency register can be used to set the mixing frequency over a range of ±Fs/2 in steps of $Fs/2^{32}$.

9.6 RECEIVE COARSE FREQUENCY MIXER (CMIX)

The receive path contains an optional $\pm F_{ADCCLK}/4$ coarse digital frequency mixer. An example of its use is the capture of an IF centered in the middle of a Nyquist band. The digital mixer can move the carrier or block of carriers to baseband or near baseband. If the total bandwidth of the carrier or summation of carriers is less than $0.4 \times F_{ADCCLK}/4$, the decimation filter can also be employed.

The CMIX block does a complex mixing on the A and B channels as shown below. The SYNC pin can be used to ensure that across chips, the phase of mixing is maintained.

MIXING MODE	MIXING	MIXING PATTERN(1)
00	Normal (Low Pass, No Mixing)	Iout = { +A, +A , +A, +A } Qout = { +B, +B , +B, +B }
01	High Pass (Fs/2)	Iout = { +A, –A , +A, –A } Qout = { +B, –B , +B, –B }
10	+Fs/4	Iout = { +A, –B , –A, +B } Qout = { +B, +A , –B, –A }
11	–Fs/4	Iout = { +A, +B , –A, –B } Qout = { +B, –A , –B, +A }

(1) A and B are the inputs to the CMIX block. Iout and Qout are the outputs.

9.7 RMS POWER METER

The RX signal chain has two power meters – the coarse power meter and fine power meter.

9.7.1 Coarse Power Meter

The fine power meter estimates the total integrated power in linear scale based on a much larger set of samples. The resulting integrated power number is stored in a register for readout. The interval time (how often to start integration) and integration time (number of samples to integrate) is programmable. The power meter can be configured in either real mode (where the power of each channel is calculated individually) or in a complex mode {where the power of (I^2+Q^2) is calculated}. This is illustrated below.

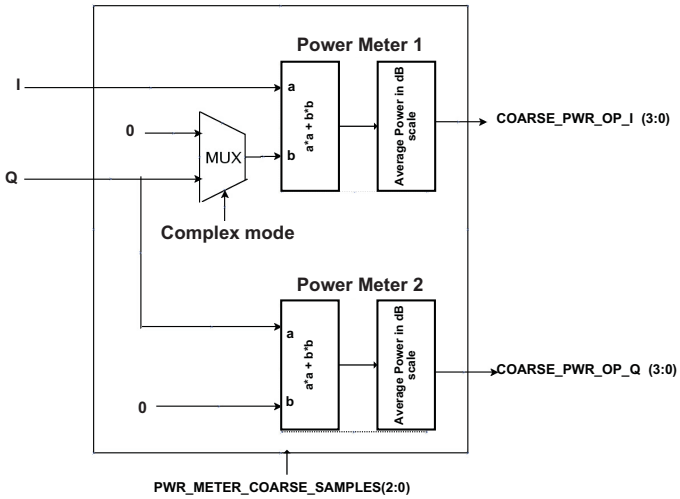

Figure 9-3. Coarse Power Meter

9.7.2 Fine Power Meter

The fine power meter estimates the total integrated power in linear scale based on a much larger set of samples. The resulting integrated power number is stored in a register for readout. The interval time (how often to start integration) and integration time (number of samples to integrate) is programmable. The power meter can be configured in either real mode (where the power of each channel is calculated individually) or in a complex mode {where the power of (I^2+Q^2)is calculated}. This is illustrated below.

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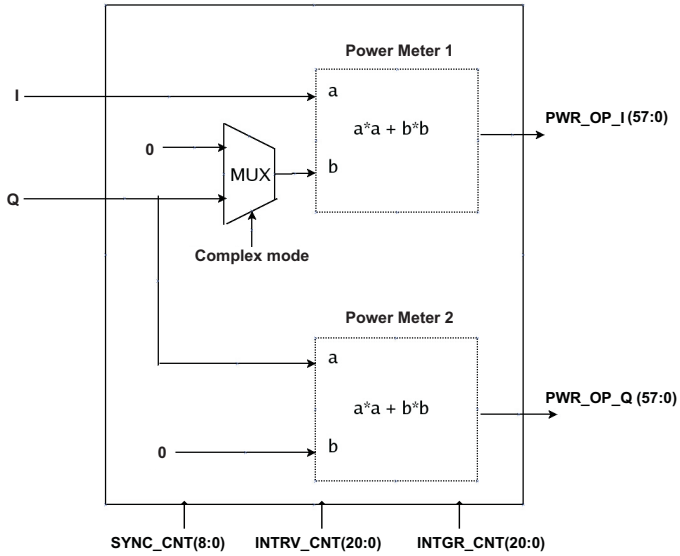

Figure 9-4. Fine Power Meter

Power in the fine power meter is calculated by squaring each I (I and Q for complex inputs) sample, summing, and then integrating the summed-squared results into a 58 bit accumulator over a programmable integration period.

The integration period is programmed into the 21 bit counter, in 8 sample increments. The power stored in the 58-bit register is:

Power = [(I*I) x (Nx8 + 3)] for real inputs where N is the integration count.

Power = [(I*I + Q*Q) x (Nx8 + 3)] for complex inputs where N is the integration count.

The power meter operation can be optionally synced. If power meter syncing is enabled, it waits for a programmable number of cycles after a valid sync, and then starts computation. If syncing is disabled, it starts computation as soon as the power meter is enabled. Once the computation interval is completed, the computed power is written to a set of serial interface registers, and the next computation interval begins. The contents of these registers can be read out serially through SDOUT.

The process begins with a sync event starting the 9 bit delay counter. After (8xsync_delay + 4) samples, the integration interval is started. Integration continues until the integration count is met, at which point the 58 bit integrator results are transferred to the read only register. A new measurement period will start at the end of the interval period.

A more detailed diagram of the power meter is shown below (the I and Q are represented as 16-bit numbers).

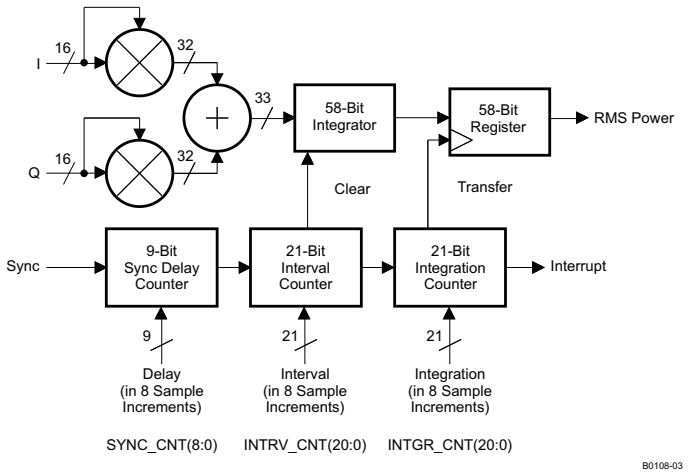

Figure 9-5. Power Meter Detailed Diagram

The power meter timing is shown below:

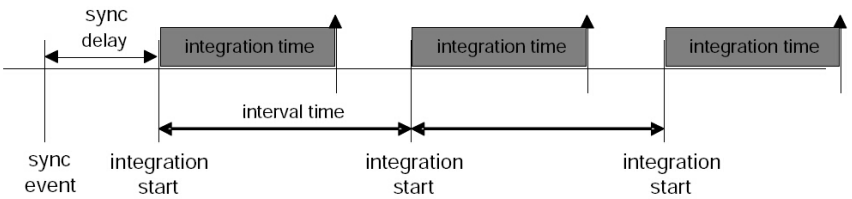

Figure 9-6. Power Meter Timing

9.8 TRANSMIT SIGNAL CHAIN

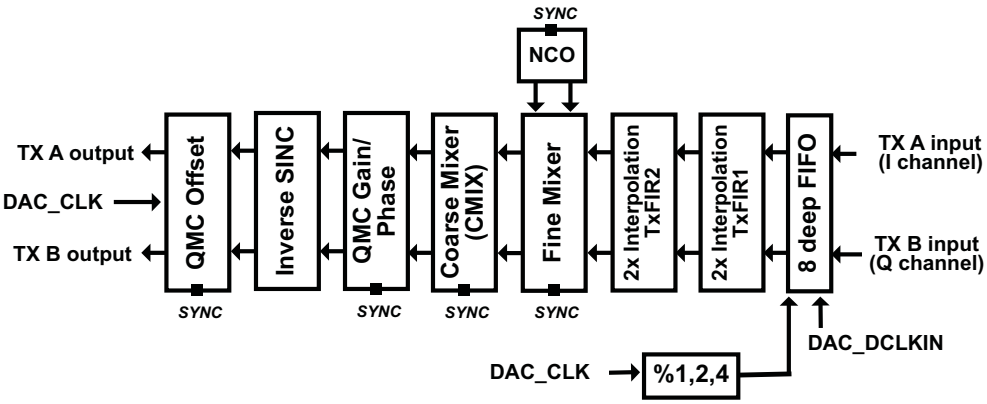

Figure 9-7. Transmit Signal Chain

9.9 TRANSMIT DAC

The transmit DAC is a current-steering architecture, capable of clock rates up to 250MSPS and output currents up to 20mA. The DAC is structured as a current sink from the load. The DAC is powered from AVDD3_DAC, a 3V analog supply. This provides for an output compliance range of AVDD3_DAC ± 0.5V. To benefit from the full 1V swing available on each DAC output pin, a voltage divider load referenced to a higher voltage supply, like 5V, is recommended. The current-steering architecture will sink current into the + and – DAC outputs. The sum of the current will always be equal to the full-scale current. The full scale current is set with a resistor (RBIAS) to ground on the BIASJ pin, and will be equal to

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I_{OUTFS} = 16 × (VREF/RBIAS), where VREF = 1.2V.

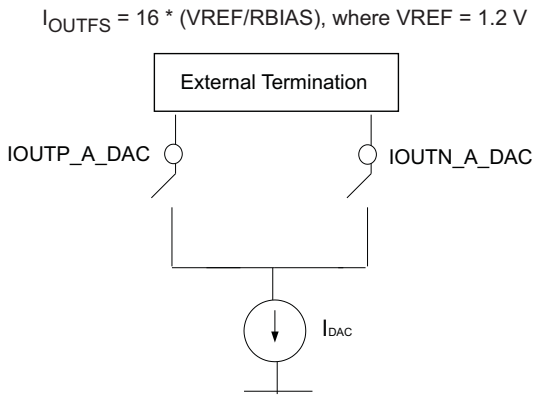

Figure 9-8. Current Steering Architecture of DAC

9.10 FIFO

The 8-Deep FIFO is used to handoff the data from the digital clock (DAC_DCLKIN) domain to the DAC_CLK domain (or the divided version of DAC_CLK if interpolation is used). The FIFO has a read and write pointer, which are initialized to 4 away from each other when the chip is either reset or synchronized. The write pointer increments with DAC_DCLKIN whereas the read pointer increments with DAC_DCLKIN (or the divided version). Ideally, the read and write pointers maintain the difference of 4. However, if there is a drift in the relative phases of the two clocks, the instantaneous values of the read and write pointers can differ from 4. If the pointers come to within 2 positions of each other, the FIFO can be set to identify that condition as a possible "collision" condition and can shut off the DAC outputs by pulling it to mid code. A stoppage of the input clock can also be detected by the FIFO.

9.11 TRANSMIT INTERPOLATION FILTERS

The AFE7225/7222 can enable 2x or 4x interpolation using on-chip half-band interpolation filters. The additional oversampling provided by interpolation can be used to reduce the order of the low pass anti-aliasing filter that follows the transmit DACs or so that the digital carrier can be block shifted by the coarse mixer to a higher output IF.

While interpolating by a factor of 2, the DAC_DCLKIN rate should be set to half of the input clock rate.

While interpolating by a factor of 4, the DAC_DCLKIN rate should be set to one fourth of the input clock rate.

Each channel has two filters TxFIR1, and TxFIR2, of which TxFIR1 alone is enabled in the Interpolate by 2 mode, Both filters are enabled in Intertpolate by 4 mode. The 2 filters in each of the two channels can individually be configured to operate in the ‘low pass ‘ or the high pass mode. By default, all filters are configured to opearate in the low pass mode. The following table lists the address and data mask values to be programmed to configure each of these filters in the high pass mode.

TXFIR1 is a 43 tap half-band filter. The transition band is from 0.4 to 0.6 of $F_{CLKFIR1}/2$, and the stop band attenuation is 70 dB. Pass band ripple is less than 0.1dB. It has the following coefficients (listed only up to the middle one)

TXFIR1 (interpolation filter 1)
coefficients = [12 0 –33 0 73 0 –143 0 254 0 –426 0 685 0 –1090 0 1781 0 –3286 0 10365 16384]

The frequency response is shown below.

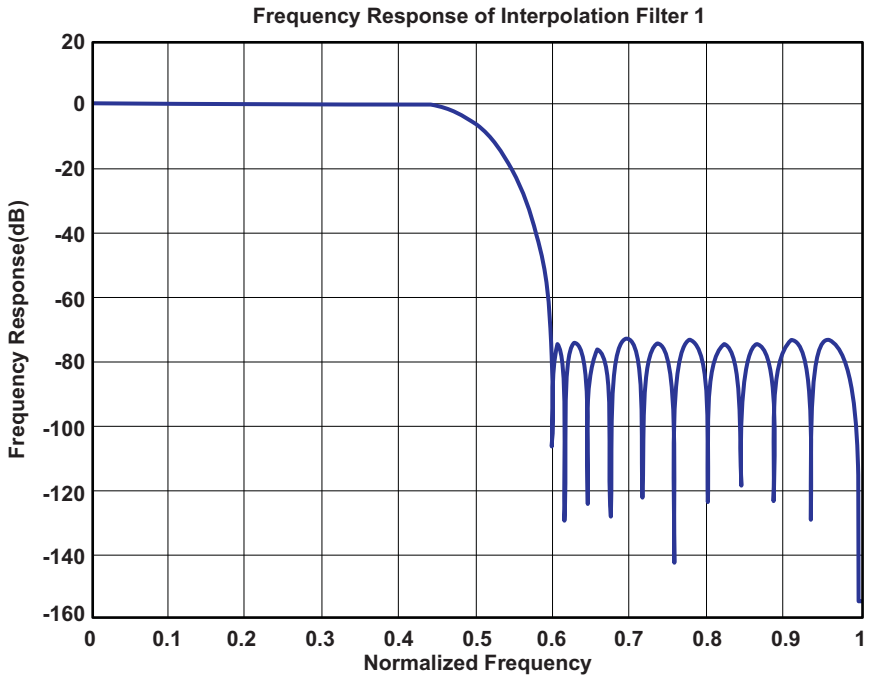

Figure 9-9. Interpolation Filter 1 freq Response (from 0 to $F_{DACCLK}/2$) (2X Interpolation mode)

TXFIR2 is a 19 tap half-band filter. The transition band is from 0.27 to 0.75 of $F_{CLKFIR2}/2$, and the stop band attenuation is 70dB. Pass band ripple is less than 0.1dB. It has the following coefficients (listed only up to the middle one).

TXFIR2 (interpolation filter 2)
coefficients = [11 0 –64 0 224 0 –648 0 2525 4096]

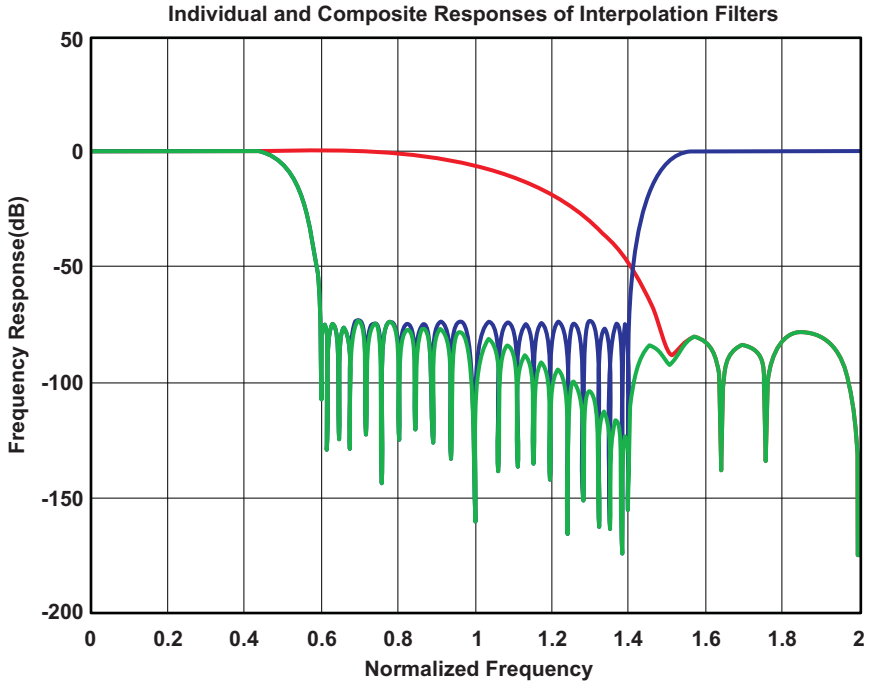

Figure 9-10. Interpolation filters individual and composite responses – TXFIR1 response is shown in blue, TXFIR2 response is in red, and the composite response is in green. (4X interpolation mode, from 0 to $F_{DACCLK}/2$)

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9.12 TRANSMIT FINE FREQUENCY MIXER (FMIX)

The fine mixer uses a Numerically Controlled Oscillator (NCO) to generate two complementary outputs of a finely programmable frequency, which is then mixed with the A and B inputs to generate complex outputs.

The mixer computes two outputs as follows:

Output I = $\{A\cos(\omega_{mix}t) - B\sin(\omega_{mix}t)\}$ and

Output Q = $\{A\sin(\omega_{mix}t) + B\cos(\omega_{mix}t)\}$

where ω_{mix} is the programmed fine frequency.

The NCO has a 32 bit frequency register, and a 20 bit phase register. The 32 bit frequency register can be used to set the mixing frequency over a range of ±Fs/2 in steps of $Fs/2^{32}$.

9.13 TRANSMIT COARSE FREQUENCY MIXER

The transmit path contains an optional $\pm F_{DACCLK}/4$ coarse digital frequency mixer. An example of its use is the processing of an input pattern to the AFE7225/7222 at or near baseband. The digital mixer can move the carrier or block of carriers to a higher IF after interpolation. This is useful especially in quadrature modulation as it creates more separation between the wanted signal and its image, making it easier to filter the unwanted image at RF after the analog quadrature modulator.

MIXING MODE	MIXING	MIXING PATTERN(1)
00	Normal (Low Pass, No Mixing)	Iout = { +A, +A , +A, +A } Qout = { +B, +B , +B, +B }
01	High Pass (Fs/2)	Iout = { +A, –A , +A, –A } Qout = { +B, –B , +B, –B }
10	+Fs/4	Iout = { +A, –B , –A, +B } Qout = { +B, +A , –B, –A }
11	–Fs/4	Iout = { +A, +B , –A, –B } Qout = { +B, –A , –B, +A }

(1) A and B are the inputs to the CMIX block. Iout and Qout are the outputs.

9.14 TRANSMIT INVERSE SINC FILTER

The inverse SINC filter is 9-tap and has a response that is inverse of the natural DAC droop versus frequency (due to sin(x)/x roll-off caused by zero-order hold of DAC sampling. It uses the same coefficients as in DAC5688. The inverse sinc filter has a gain > 1 at all frequencies. Therefore, the signal input to the inverse SINC must be reduced from full scale to prevent saturation in the filter. The amount of backoff required depends on the signal frequency, and is set such that at the signal frequencies the combination of the input signal and filter response is less than 1 (0dB). For example, if the signal input to the inverse SINC filter is at $F_{DACCLK}/4$, the response of the inverse SINC is 0.9 dB, and the signal must be backed off from full scale by 0.9 dB. The gain function in the QMC block can be used to reduce the amplitude of the input signal. The coefficients are same as those in the inverse SINC filter in DAC5688 (listed only up to the middle one).

Coefficients = [1 –4 13 –50 592]

Its frequency response is shown below:

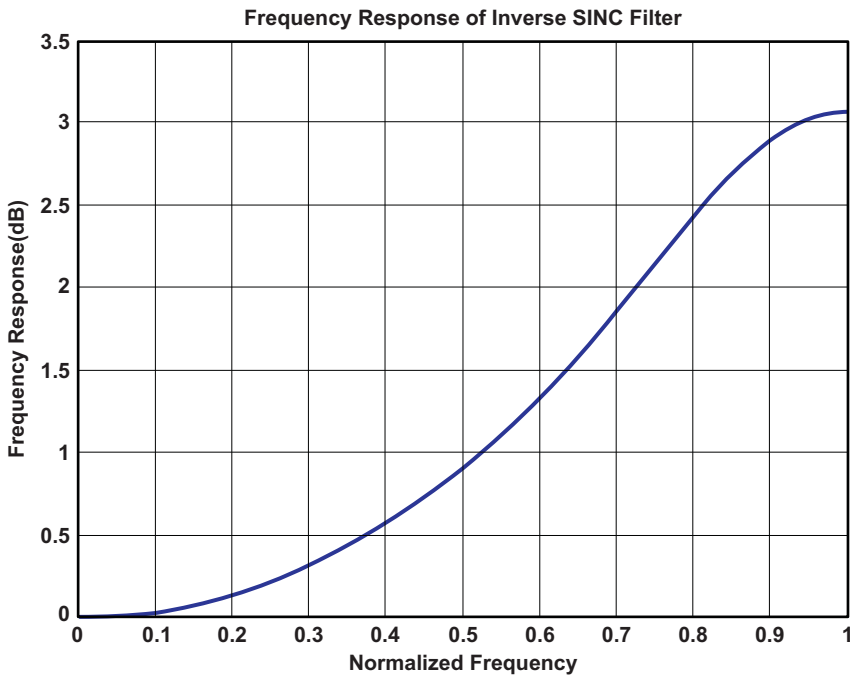

Figure 9-11. Inverse SINC Filter Frequency Response (0 to $F_{dac}/2$)

9.15 QUADRATURE MODULATION CORRECTION (QMC) – SIMILAR FOR TRANSMIT AND RECEIVE

The Quadrature Modulator Correction (QMC) block provides a means for changing the phase balance of the complex signal to compensate for I and Q imbalance present in an analog quadrature modulator. The block diagram for the QMC block is shown below. The QMC block contains 3 programmable parameters. Registers QMC_GAINA(10:0) and QMC_GAINB(10:0) control the I and Q path gains and are 11 bit values with a range of 0 to 1.99. The gain adjustment value is determined by dividing the register value by 1024. A value of 1024 is therefore a gain of 1, a value of 512 is a gain of 0.5 and a value of 2047 is a gain of 1.99. Note that the I and Q gain can also be controlled by setting the DAC full scale output current. Register QMC_PHASE(9:0) controls the phase imbalance between I and Q and is a 10-bit value with a range of –0.125 to +0.125 that is multiplied by the Q sample and added to the I sample.

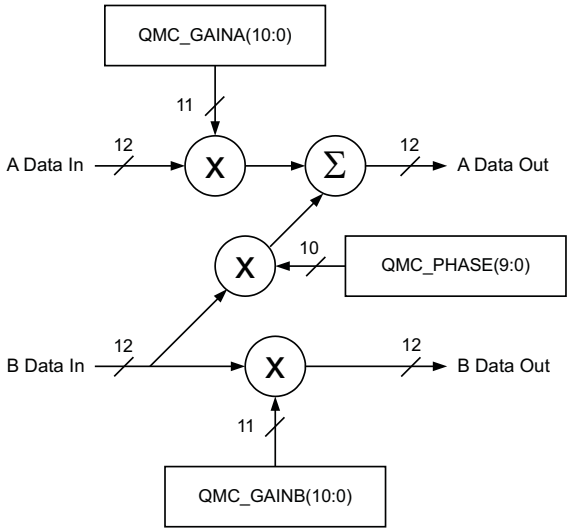

Figure 9-12. QMC Block Diagram

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9.16 DIGITAL OFFSET CONTROL

Registers QMC_OFFSETA(12:0) and QMC_OFFSETB(12:0) control the A and B path offsets and are 13-bit values with a range of -4096 to 4095. The offset adjustment value is got by dividing the register value by 16, so the range of the offset adjustment is ±256 LSB. The DAC offset value adds a digital offset to the digital data before digital-to-analog conversion. The data and offset values are LSB aligned.

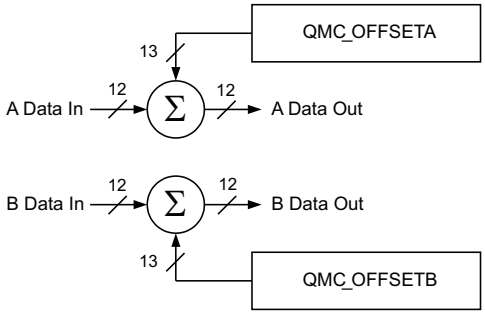

Figure 9-13. Digital Offset Block Diagram

9.17 SYNCHRONIZING MULTIPLE CHIPS

The AFE722x has a SYNC pin that can be used to synchronize multiple chips. When such synchronization is not required, the SYNC pin can be tied to ground (or in the case of differential SYNC input, tie SYNCINP to logic low and SYNCINN to logic high).

On the transmit side, several blocks need to be synchronized. These include the clock divider, FIFO read and write pointersm, coarse mixer mixing phase, NCO phase, power meter, QMC gain/ phase correction block. Note however that all these blocks can function even without synchronization.

The simplest way to synchronize all blocks is using the global synchronizing mode, which is enabled by default. The synchronization source, by default, is the SYNC pin. A rising edge on the SYNC pin will cause all blocks to be synced in an order that is internally controlled. The synchronization source can also be set to a serial interface bit (TX_GLOBAL_SYNC_SRC and RX_GLOBAL_SYNC_SRC). When using the serial interface bit, a 0-1 transition on the register bit triggers syncing.

In most cases, global synchronizing mode is sufficient. However, each block can be independently synchronized by disabling the global synchronization modes (TX_GLOBAL_SYNC_DIS and RX_GLOBAL_SYNC_DIS) and enabling the block-specific synchronization register controls. The block-specific synchronization can also be done either using the SYNC pin or using 0-1 transitions on specific register bits.

For some blocks, there is an option to specify whether or not syncing is neede. An example is the QMC offset register control. When syncing is specified as not needed, the values in the QMC offset register are applied as soon as they are written into. However when syncing is specified as needed, the values written into this register are applied to the block only when a valid SYNC pulse is applied.

When applying block specific syncing, it is recommended that the following order be followed:

1. Synchronize the clock divider first
2. Synchronize the FIFO next
3. Synchronize all other other blocks next in no specific order

The effect on synchronizing on various blocks is listed below:

- **FIFO –** the write pointer is reset to zero and the read pointer is reset to 4.
- **QMC offset correction –** The QMC offset correction values programmed into the serial interface registers are loaded into the block
- **QMC Gain/ Phase correction block –** The gain and phase correction values programmed into the serial interface registers are loaded into the block

- **Fine mixer –** The NCO frequency and phase register values programmed into the serial interface registers are loaded into the block. Also the NCO phase accumulator is initialized to the programmed phase offset.
- **Coarse mixer –** The phase programmed for the mixing is applied on SYNC.
- **Power meter –** After a SYNC event, power computation begins after a programmable number of cycles.

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10 DIGITAL INTERFACE

The digital interface is capable of operating in two distinct modes – interleaved parallel CMOS and serialized LVDS. The supported maximum speed of operation varies depending upon mode in which digital interface is operating. AFE722x has constraints on maximum frequencies of ADC_CLK and DAC_CLK. Using these constraints, a comprehensive table showing maximum frequencies of different clocks in different interfaces is listed in Table 10-1.

The following table shows the maximum frequency of operation of various clocks of AFE7225 in **LVDS** interface mode (set register bit REG_LVDS_TX='1' to put DAC in LVDS interface mode, and MASTER_OVERRIDE_RX='1' and REG_LVDS_RX='1' to put ADC in LVDS interface mode.)

Table 10-1. Maximum Interface Rates in LVDS Mode

RX PATH						
Wire Mode (register bit TWOWIRE_RX)	SDR or DDR (register bit SDR_RX)	Decimation Factor (register bits RX_DEC_FIL_EN, RX_DEC_FIL_EN_SRC)	Max ADC Sampling Clock (ADC_CLK(1)) MHz	Max ADC Frame Clock (ADC_FCLKOUTP/N) MHz	Max ADC Bit Clock (ADC_DCLKOUTP/N) MHz	Max Serial Output Data Rate (ADCx_DATA_nP/N) Mbps, per wire
1-wire	DDR	1	65	65	390	780
		2		32.5	195	390
2-wire	DDR	1	125	125	375	750
		2		62.5	187.5	375
2-wire	SDR	1	65	65	390	390
		2		32.5	195	195
TX PATH						
Wire Mode (register bit TWOWIRE_TX)	SDR or DDR (register bit SDR_TX)	Interpolation By (register bits TX_INT_MODE(1:0), TX_INT_MODE_SRC)	Max DAC Output Clock (DAC_CLK(1)) MHz	Max DAC Frame Clock (DAC_FCLKINP/N) MHz	Max DAC Bit Clock (DAC_DCLKINP/N) MHz	Max Serial Input Data Rate (ADCx_DATA_nP/N) Mbps, per wire
1-wire	DDR	1	65	65	390	780
		2	130	65	390	780
		4	250	62.5	375	750
2-wire	SDR	1	65	65	390	390
		2	130	65	390	390
		4	250	62.5	375	375
2-wire	DDR	1	130	130	390	780
		2	250	125	375	780
		4	250	62.5	187.5	375

(1) ADC_CLK and DAC_CLK are derived from clocks on CLKINP and CLKINN (differential clock, a single-ended clock or two independent single-ended clocks). See Clocking section for details. For Full-Duplex operation requiring two single-ended clocks, see section Full Duplex Operation – Coupling Considerations.

Table 10-2 shows the maximum frequency of operation of various clocks of AFE7225 in **CMOS** interface mode (by default after reset, AFE722x operates in CMOS interface mode for both RX and TX path).

Table 10-2. Maximum Interface Rates in CMOS Mode

RX PATH				
Low Power CMOS Mode (register bit MODE_LP_CMOS)	Decimation Factor (register bits RX_DEC_FIL_EN, RX_DEC_FIL_EN_SRC)	Max ADC Sampling Clock (ADC_CLK(1)) MHz	Max ADC_DCLKOUT MHz	Max Parallel Output Data Rate Mbps, per pin
Disabled (default)	1	105	105	210
	2		52.5	105
Enabled	1	40	40	80
	2		20	40
TX PATH				
Interpolation Factor (register bits TX_INT_MODE(1:0), TX_INT_MODE_SRC)	Max DAC Output Clock (DAC_CLK(1)) MHz	Max DAC_DCLKIN MHz	Max Parallel Input Data Rate Mbps, per pin	
1	130	130	260	
2		65	130	
4		32.5	65	

(1) ADC_CLK and DAC_CLK are derived from clocks on CLKINP and CLKINN (differential clock, a single-ended clock or two independent single-ended clocks). See Clocking section for details. For Full-Duplex operation requiring two single-ended clocks, see section Full Duplex Operation – Coupling Considerations.

10.1 PARALLEL CMOS ADC RX DATA

The 12-bit ADC-A and ADC-B data is interleaved (A then B) into one 12-bit word on pins ADCDATA0:ADCDATA11 at twice the rate of each pattern with a DDR clock (data transitions on rising and falling edges). This can be quadrature data or two independent receive channels. Note that in the default RX CMOS mode, the edges of the ADC_DCLKOUT are aligned in the middle of the data window.

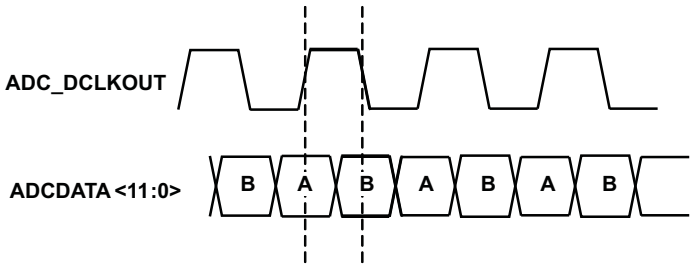
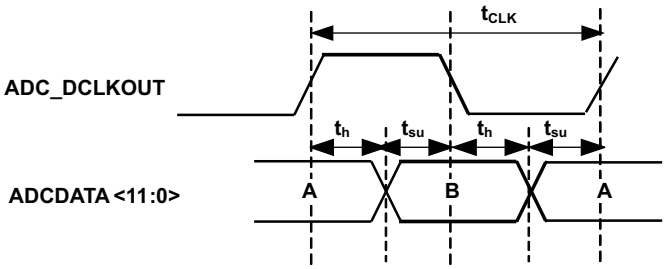


Figure 10-1. RX CMOS Interleaved Output

10.2 TIMING INFORMATION FOR PARALLEL CMOS ADC RX DATA



t_{CLK} = Time period of ADC output data clock (same as time period of ADC sampling clock when decimation is set to 1).

Figure 10-2. RX CMOS Output Timing

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10.3 PARALLEL CMOS DAC TX DATA

The 12-bit DAC-A and DAC-B data is interleaved (A then B) into one 12-bit word on pins DACDATA0:DACDATA11 at twice the rate of each pattern with a DDR clock (data transitions on rising and falling edges). This can be quadrature data or two independent transmit channels.

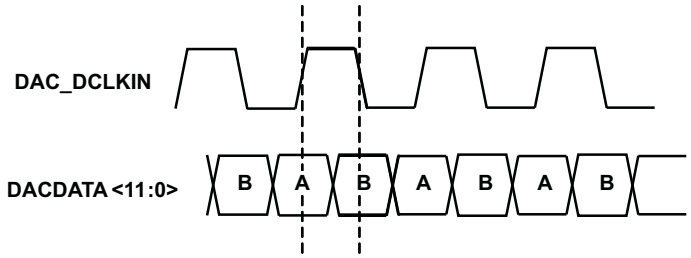
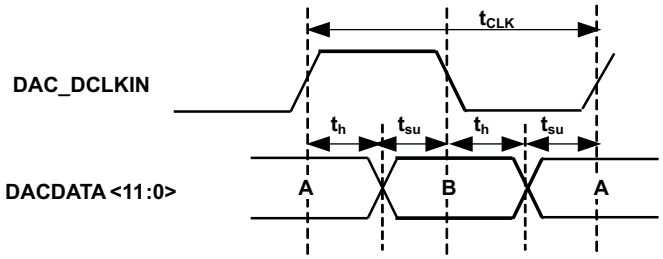


Figure 10-3. TX CMOS Interleaved Input

10.4 TIMING INFORMATION FOR PARALLEL CMOS DAC TX DATA



t_{CLK} = Time period of DAC input data clock (same as time period of DAC output clock when interpolation is set to 1).

Figure 10-4. TX CMOS Input Timing

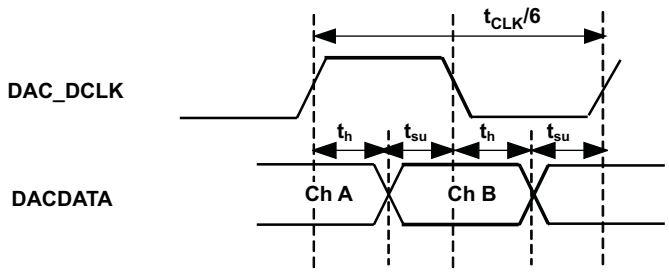
10.5 LOW POWER RX CMOS MODE

The default RX CMOS mode uses an internal PLL to position the clock edges in the middle of the data window. While operating at speeds lower than 40 MSPS, a low power CMOS mode can be enabled (set bit MODE_LP_CMOS to 1). In this mode, the PLL is bypassed and the clock edges are set relative to the data transitions through delay elements. Bypassing the PLL saves about 20 mW of power. However, because the delay elements operate in open loop, there is no tight control on the precise delay and there can be a chip to chip variation. At low speeds, there will be sufficient set up and hold time inspite of the variations in the clock edge relative to the data. An advantage of the low power RX CMOS mode is that the recovery of the RX from powerdown is much faster because of the absence of the PLL. For example, with the low power RX CMOS mode enabled, the RX recovers from a state of OFF clock to a state of ON clock in 5 us (as compared to 20 us when in default RX CMOS mode). Another advantage of this low power RX CMOS mode is that the minimum frequency of operation is extended down to 2.5 MSPS (from 10 MSPS).

10.6 SERIAL LVDS DAC TX INTERFACE

12-bit DAC input data is serialized onto one or two LVDS pairs per DAC. DACA and DACB data inputs can be quadrature data or two independent receive channels. Two serialization modes are available.

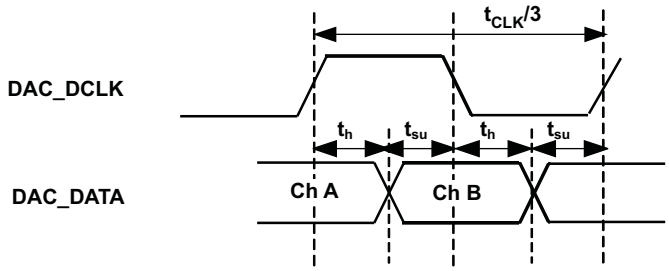
- **1-Wire mode:** 1 LVDS pair for the data to each DAC. It will operate in a DDR fashion serialized to a frequency of 6x the pattern word rate. A frame clock (DAC_FCLKINP/N) at the word rate and a bit clock (DAC_DCLKINP/N) at 6x. Example: 50MSPS 12-bit pattern will serialize to 300MHz on each LVDS pair, frame clock of 50MHz and bit clock of 300MHz. Effective serial data rate is 600Mbps due to bit transitions on rising and falling edge of bit clock. Recommended maximum word rate is ~65MSPS in this mode.



A. t_{CLK} = Time period of DAC input data clock (same as time period of DAC output clock when interpolation is set to 1).
B. t_h is minimum hold time required at the AFE722x input.
C. t_{su} is minimum setup time required at the AFE722x input.

Figure 10-5. TX 1-Wire Mode Timing Diagram

- **2-Wire mode, DDR clock:** 2 LVDS pairs for the data to each DAC. It will operate in a DDR fashion serialized to a frequency of 3x the pattern word rate. A frame clock (DAC_FCLKINP/N) at half the word rate and a bit clock (DAC_DCLKINP/N) at 3x. Example: 50MSPS 12-bit pattern will serialize to 150MHz on each LVDS pair, frame clock of 25MHz and bit clock of 150MHz. Effective serial data rate is 300Mbps on each LVDS pair due to bit transitions on rising and falling edge of bit clock. Recommended maximum word rate is ~125MSPS in this mode.



A. t_{CLK} = Time period of DAC input data clock (same as time period of DAC output clock when interpolation is set to 1).
B. t_h is minimum hold time required at the AFE722x input.
C. t_{su} is minimum setup time required at the AFE722x input.

Figure 10-6. TX 2-Wire Mode, DDR Clock Timing Diagram

- **2-Wire mode, SDR clock:** 2 LVDS pairs for the data to each DAC. It will operate in a SDR fashion serialized to a frequency of 6x the pattern word rate. A frame clock (DAC_FCLKINP/N) at the word rate and a bit clock (DAC_DCLKINP/N) at 6x. Example: 50MSPS 12-bit pattern will serialize to 300MHz on each LVDS pair, frame clock of 50MHz and bit clock of 300MHz. Effective serial data rate is 300Mbps on each LVDS pair due to bit transitions on rising edge of bit clock. Recommended maximum word rate is ~65MSPS in this mode.

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10.6.1 LVDS TX Interface

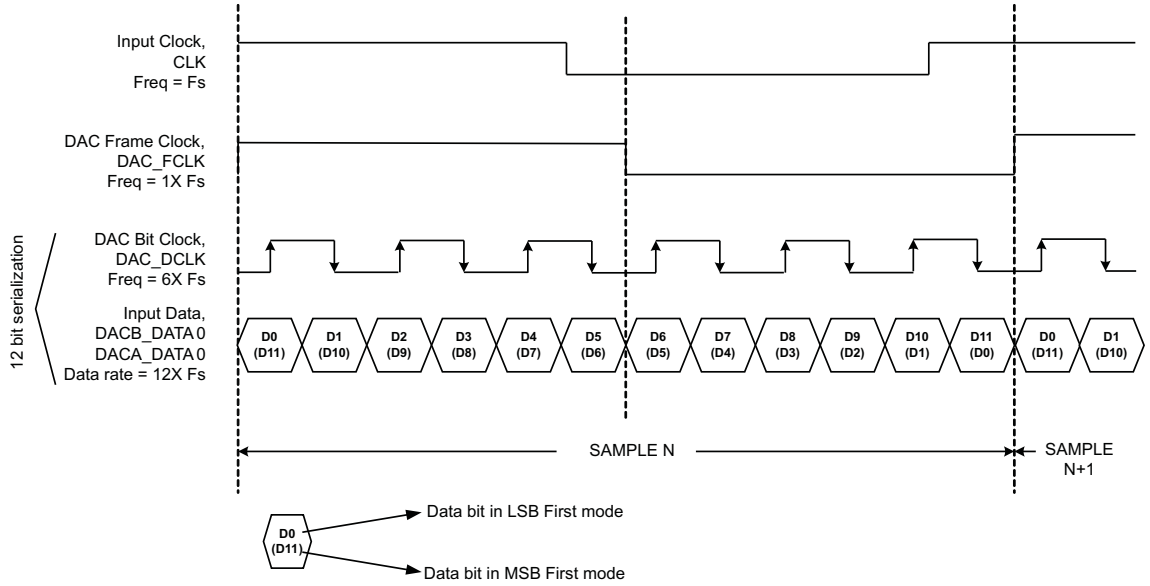


Figure 10-7. 1-WIRE MODE

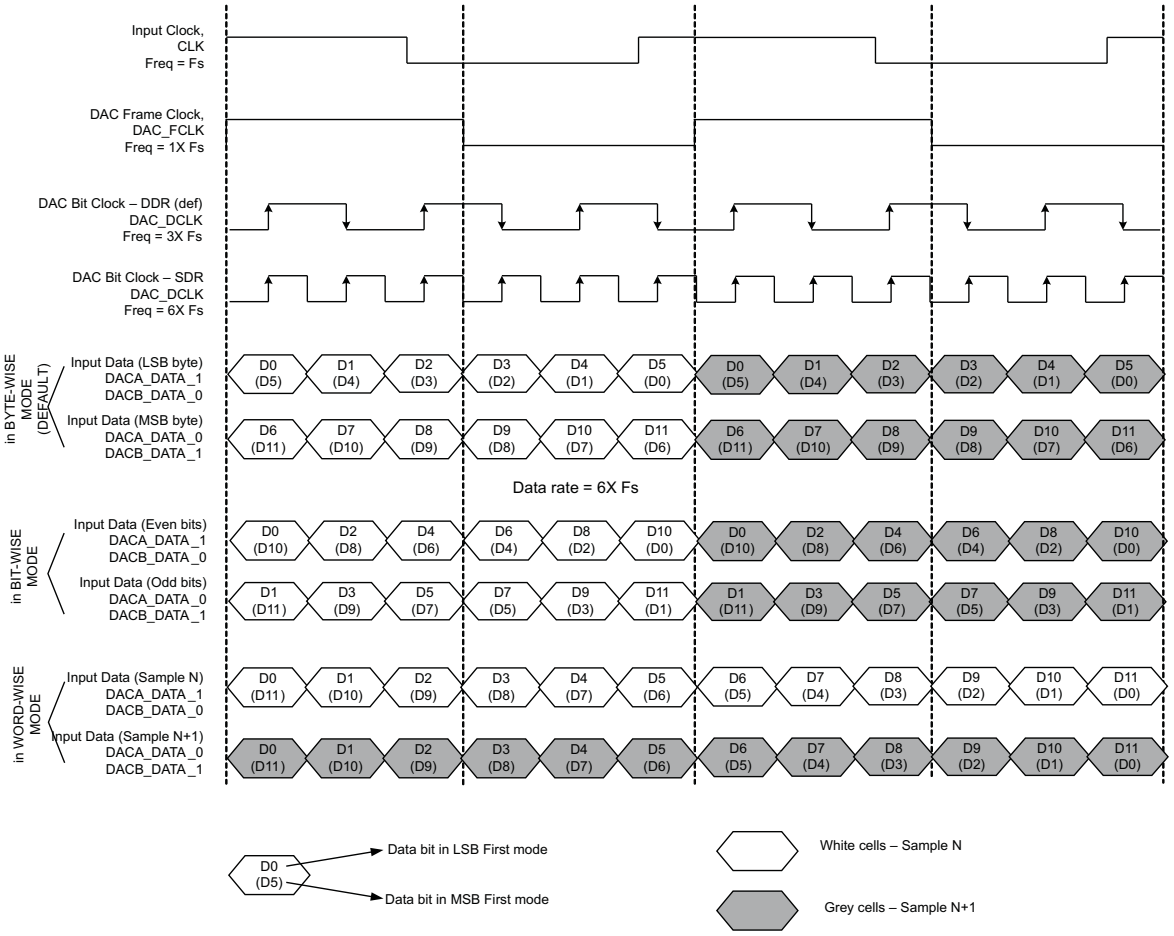


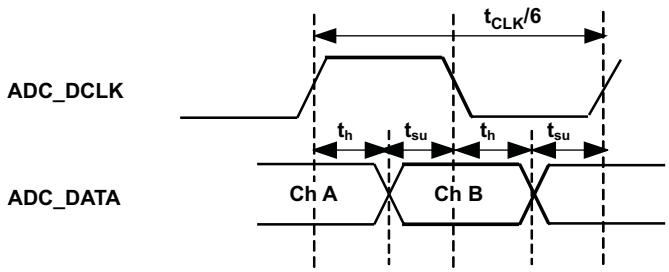
Figure 10-8. 2-WIRE MODE

10.7 SERIAL LVDS ADC RX INTERFACE

Note: Set MASTER_OVERRIDE_RX bit to '1' before entering RX LVDS interface.

The 12-bit ADC output data is serialized onto one or two LVDS pairs per ADC. ADCA and ADCB data outputs can be quadrature data or two independent receive channels. Two serialization modes are available.

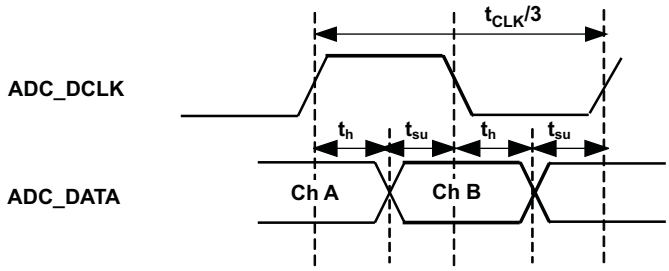
- **1-Wire mode:** 1 LVDS pair for the data from each ADC. It will operate in a DDR fashion serialized to a frequency of 6x the pattern word rate. A frame clock (ADC_FCLKOUT) at the word rate and a bit clock (ADC_DCLKOUT) at 6x. Example: 50MSPS 12-bit pattern will serialize to 300MHz on each LVDS pair, frame clock of 50MHz and bit clock of 300MHz. Effective serial data rate is 600Mbps due to bit transitions on rising and falling edge of bit clock.



A. t_{CLK} = Time period of ADC output frame clock.
B. t_h is minimum hold time required at the AFE722x output.
C. t_{su} is minimum setup time required at the AFE722x output.

Figure 10-9. RX 1-Wire Mode Timing Diagram

- **2-Wire mode, DDR clock:** 2 LVDS pairs for the data from each ADC. It will operate in a DDR fashion serialized to a frequency of 3x the pattern word rate. A frame clock (ADC_FCLKOUT) at half the word rate and a bit clock (ADC_DCLKOUT) at 3x. Example: 50MSPS 12-bit pattern will serialize to 150MHz on each LVDS pair, frame clock of 25MHz and bit clock of 150MHz. Effective serial data rate is 300Mbps on each LVDS pair due to bit transitions on rising and falling edge of bit clock.



A. t_{CLK} = Time period of ADC output frame clock.
B. t_h is minimum hold time required at the AFE722x output.
C. t_{su} is minimum setup time required at the AFE722x output.

Figure 10-10. RX 2-Wire Mode, DDR Clock Timing Diagram

- **2-Wire mode, SDR clock:** 2 LVDS pairs for the data from each ADC. It will operate in a SDR fashion serialized to a frequency of 6x the pattern word rate. A frame clock (ADC_FCLKOUT) at the word rate and a bit clock (ADC_DCLKOUT) at 6x. Example: 50MSPS 12-bit pattern will serialize to 300MHz on each LVDS pair, frame clock of 50MHz and bit clock of 300MHz. Effective serial data rate is 300Mbps on each LVDS pair due to bit transitions on rising edge of bit clock.

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10.7.1 LVDS RX Interface

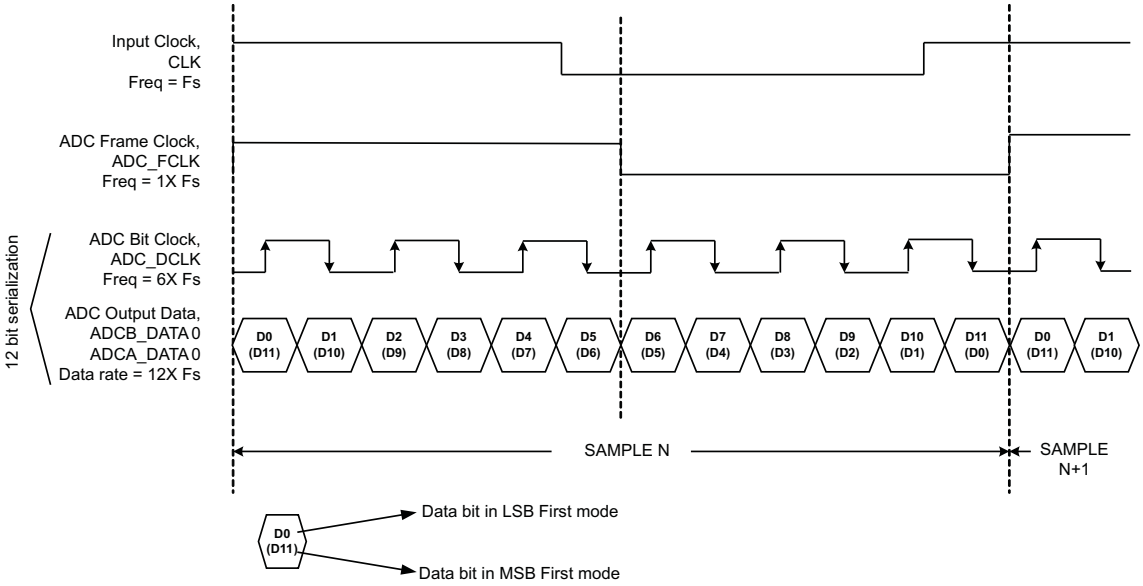

Figure 10-11. 1-WIRE MODE

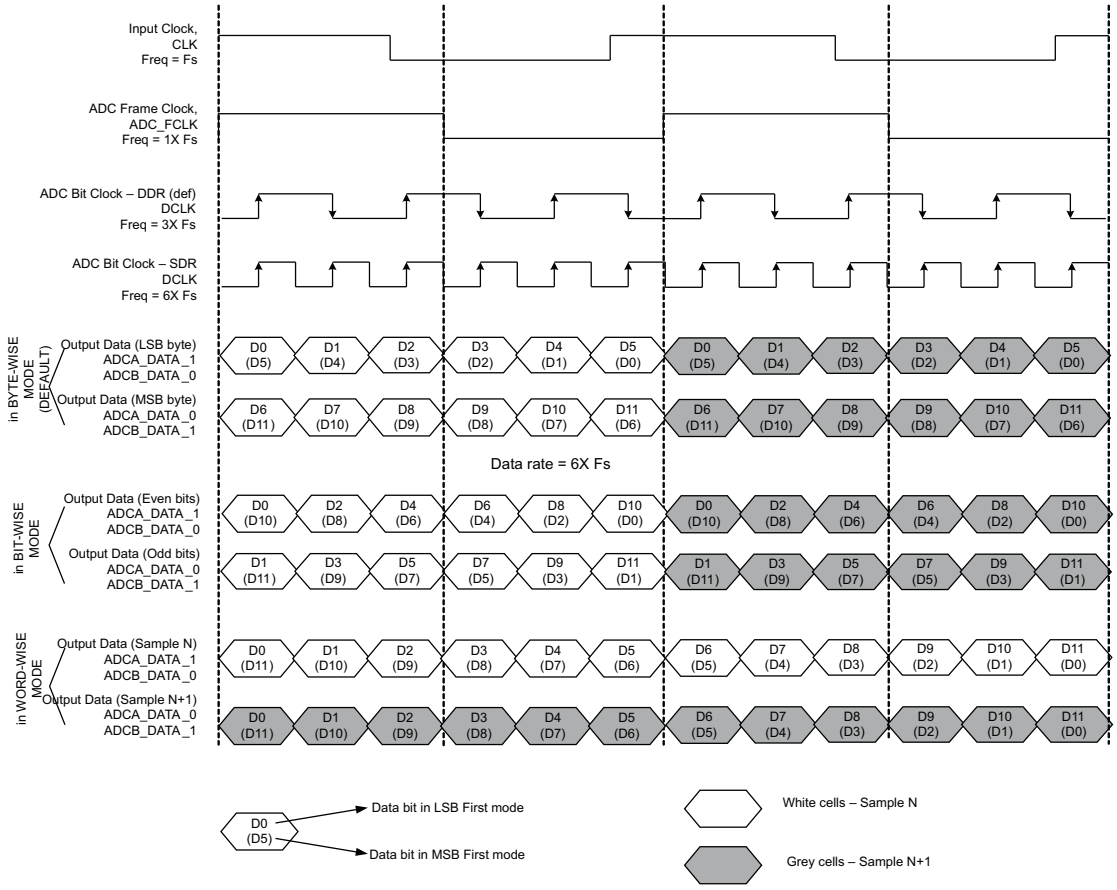

Figure 10-12. 2-WIRE MODE

10.7.2 CLOCKING

The clock inputs are versatile. The AFE7225/7222 can be driven by a differential clock, a single-ended clock or two independent single-ended clocks. Low voltage CMOS for single-ended and LVDS for differential are supported clock levels. Since routing single-ended clocks on the printed circuit board is different from system to system, it is possible to see some performance degradation in the data converters if the clock becomes corrupted prior to entering the AFE7225/7222. This is less likely to occur if using a differential clock routed on the board due to the common-mode noise rejection of the differential clock receiver.

The full block diagram of the clocking to the ADC and DAC is shown below.

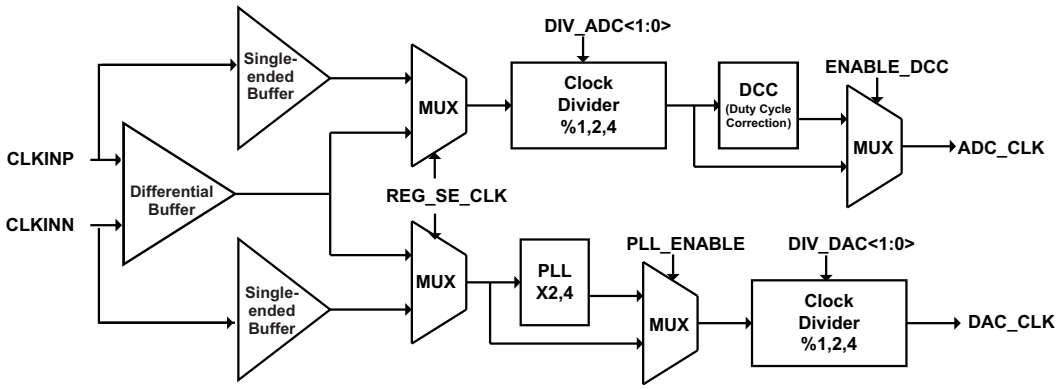

Figure 10-13. Clocking

Depending on the ADC input frequency and the target SNR of the receiver, it may be important to provide a low jitter clock source to the AFE7225/7222. A good estimate for required clock jitter to achieve a certain SNR can be found using SNR = 20*log10(2*pi*FINadc *JITTERtotal). The JITTERtotal is the rms summation of the external clock jitter and the internal AFE7225/7222 RX ADC clocking aperture jitter, specified in the timing characteristics table. A good target for the total jitter is a value that allows an SNR that meets or exceeds the ADC SNR so that the clock source jitter will not degrade the SNR. Note that the SNR is dependent on the analog input frequency and not the clock frequency.

When different rate clocks are required for the ADC and the DAC (for example, DAC_CLK is 2X rate of ADC_CLK), it is strongly recommended that the input clock be at the higher of the two rates. Dividing the high speed clock to derive the half rate clock always gives much lower jitter than using the PLL to multiply the lower rate clock to derive the higher rate inside the chip. Use the PLL only when performance requirements are relaxed and the additional jitter is tolerable (usually when the analog I/O frequencies are low).

The equivalent circuit model of the differential buffer is shown below. Note that even with the single ended buffer is enabled, the loading from the passive components in the differential buffer circuit (including the 2 pF differential cap, the two 5 kOhm resistors and the equivalent input load, Ceq are still present).

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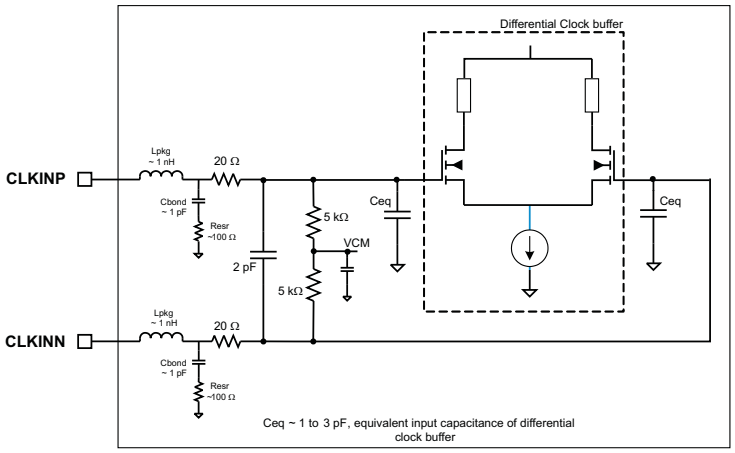

Figure 10-14. Input Clock Equivalent Circuit

10.8 Auxiliary ADC

The schematic of the Auxiliary ADC is shown below.

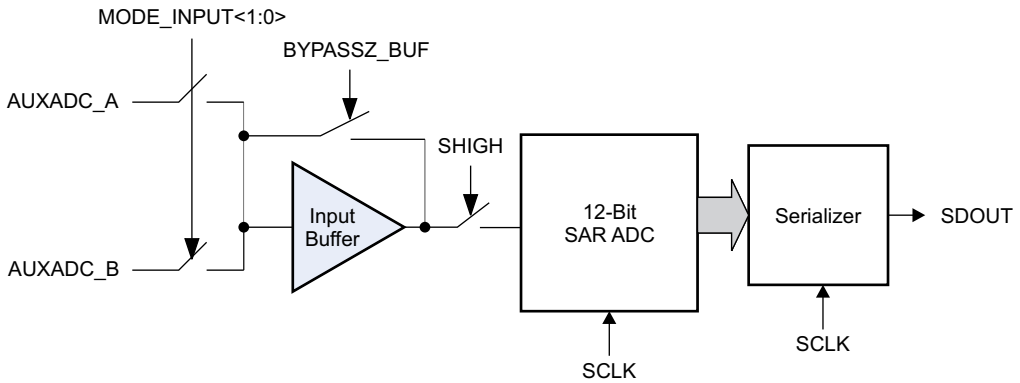

Figure 10-15. Auxiliary ADC Schematic

The Auxiliary ADC comprises a 12-bit SAR ADC with a high impedance input buffer that is bypassed by default (BYPASSZ_BUF=0). The Auxiliary ADC can select its input from 2 external pins called AUXADC_A and AUXADC_B. This selection is done using the bits MODE_INPUT <1:0>. The conversion is started by setting bit CONV_START to 1, and SCLK is used as the conversion clock. The SAR ADC converts the selected input and the 12-bit output is serialized using the SCLK and given out on the SDOUT pin. After setting CONV_START to 1, the Auxiliary ADC can be configured for either a single conversion, multiple conversions or in continuous conversion mode.

With the input buffer bypassed, the input range of the Auxiliary ADC is 0-1.5V when RANGE_AUXADC is set to 0. When the Auxiliary ADC is converting, the SAR ADC draws switching current from the input pin if the input buffer is bypassed. This may not be desirable for applications where the voltage being monitored does not have drive capability. With the input buffer introduced in the path of the input, the AUXADC inputs are high impedance and do not draw current. However, the input voltage range (at the AUXADC pins) is slightly reduced to 0.1-1.5V.

With RANGE_AUXADC set to 1, the input range is increased to 0-DVDD18 with the buffer bypassed and 0.1-(DVDD18-0.1)V with the buffer enabled.

10.8.1 Enabling the Auxiliary ADC

The Auxiliary ADCs are disabled by default.

Below is the timing diagram illustrating the Aux ADC operation.

Before starting conversion, set bit EN_AUX_ADC to '1'. Also set WHAT_IS_SDOUT<1:0> to configure SDOUT as a digital output pin.

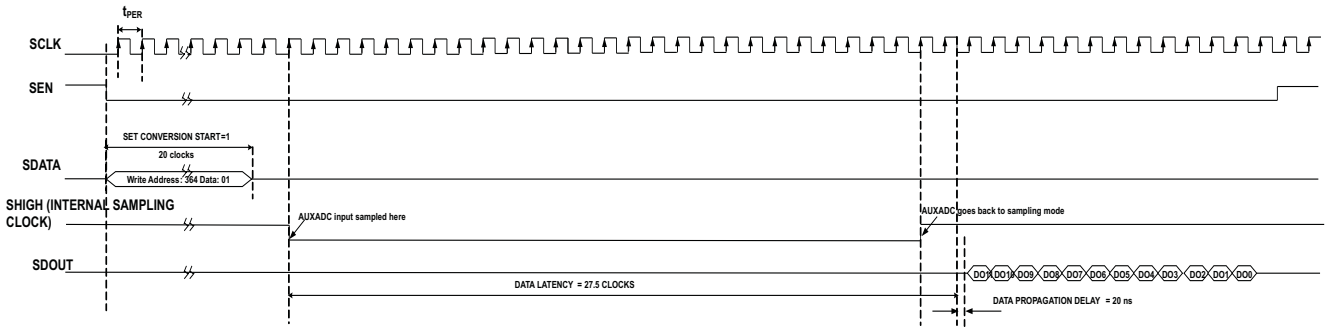

Figure 10-16. AUX ADC Timing Diagram

Note that throughout the Aux ADC conversion, SEN is kept low (active). Also keep SDATA low once the CONV_START bit has been written.

To get out of Aux ADC conversion mode, pull SEN high, then pull it low again and write the bit to make CONV_START=0.

10.9 Auxiliary DAC

The schematic of the Auxiliary DAC (for channel A) is shown below.

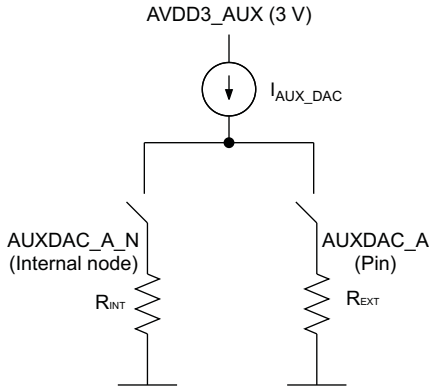

Figure 10-17. Auxiliary DAC Schematic

The Auxiliary DAC is a 12-bit current output DAC with the current steered into the AUXDAC_A pin dependent on the digital code. The data format of the Auxiliary DAC input is offset binary.

R_{EXT} is the external connected to the AUXDAC_A pin and along with the value of the full scale current, sets the full scale output voltage range. For zero input code, voltage on AUXDAC_A is equal to 0 V.

For maximum input code, voltage on AUXDAC_A is equal to IA_{UX_DAC}*R_{EXT}.

I_{AUX_DAC} is the full scale current of the Auxiliary DAC, and can be programmed from 2.5 mA to 7.5 mA (using bits FS_AUXDACI<3:0>).

For best linearity, limit the maximum voltage at AUXDAC_A to 1.5V. For example, with I_{AUX_DAC} set to 5 mA, and R_{EXT} set to 300 Ohm, the voltage on AUXDAC_A will swing from 0 to 1.5V.

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AUXDAC_A_N is the internal complementary node and has an internal resistor, R_{INT} programmable from 57 Ohm to 400 Ohm (using bits AUX_DAC_TERM_N<2:0>). For best linearity, choose a value of this resistor to be as close to R_{EXT} as possible.

10.10 Enabling the Auxiliary DAC

The Auxiliary DACs are disabled by default.

Note that address of the 20 bit serial interface write bus is the 1st 12 bits out of which the 1st 4 bits determine the access mode for the Auxiliary DAC.

Let us denote this address as ADDR<11:0>.

Following are Aux DAC modes:

If ADDR<11:8> = 0100, then we enter Direct Access mode for DAC. In this mode, DAC data is dynamically written through SDATA (and SDOUT).
If ADDR<11:8> = 0101, then we enter the Register Access mode. In this mode, DAC is loaded with the data from contents of pre-loaded registers.

In direct access mode

If ADDR<7:6> = 01: DAC_A will get written with the 12 serial bits from SDATA, DAC_B will get written with the 12 serial bits from SDOUT (both at the rising edge of SCLK)
If ADDR<7:6> = 10: DAC_A will get 12 bits from SDATA, DAC_B will get next 12 bits from SDATA (both at the rising edge of SCLK)
If ADDR<7:6> = 11: DAC_A will get 12 bits from SDATA at the rising edge of SCLK, DAC_B will get 12 bits from SDATA at the falling edge of SCLK.

In register access mode:

ADDR<7:6> = 01: Only DAC_A will be loaded with the register
ADDR<7:6> = 10: Only DAC_B will be loaded
ADDR<7:6> = 11: Both DAC_A and DAC_B are loaded.

For either direct access or register access modes, only the 1st 6 bits of the address need to be written for the serial interface state machine. Remainig bits are considered as applicable to the DAC data.

Below diagram shows the Aux DAC timing for the direct access mode where DAC_A is written through SDATA and DAC_B through SDOUT.

Start by already setting EN_AUXDACA and EN_AUXDACB bits high.

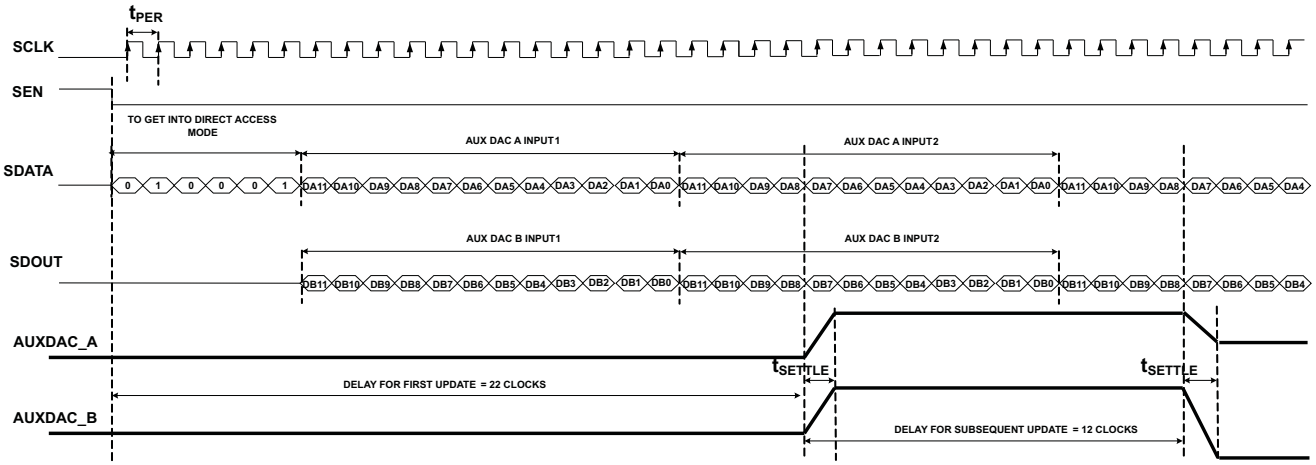

Figure 10-18. Aux DAC Timing Diagram: DAC_A is Written Through SDATA and DAC_B Through SDOUT

t_{PER} = SCLK period > 25 ns
t_{SETTLE} = Settling time of Aux DAC for full scale output (0-1.5V) = 40 ns

Therefore fastest update time:
First update = 22*25ns + 40ns = 590 ns
Subsequent update = 12*25ns = 300 ns

For the direct access mode where DAC_A and DAC_B are both written through SDATA, the timing is shown in figure below.

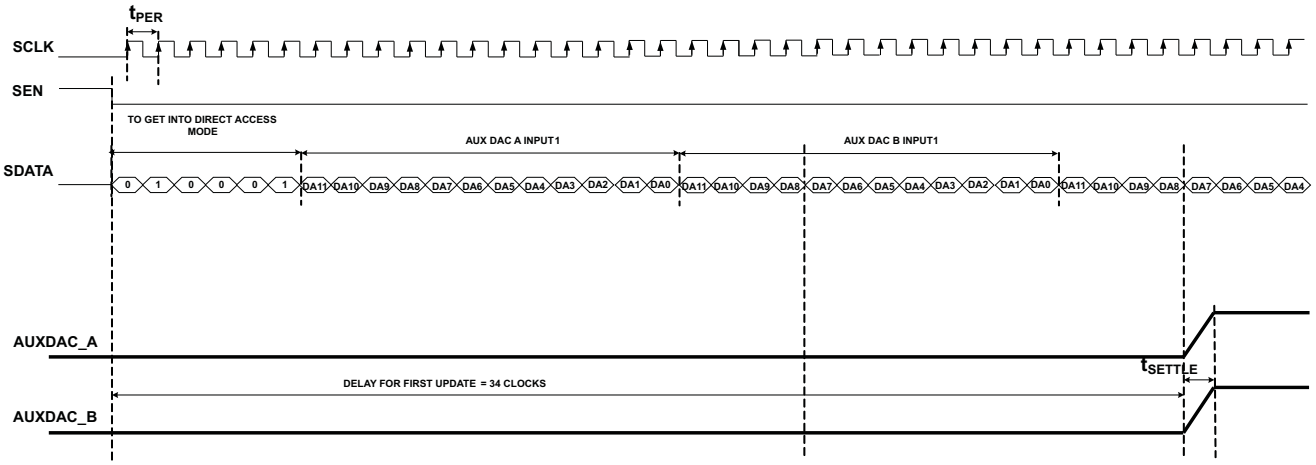

Figure 10-19. Aux DAC Timing Diagram: DAC_A and DAC_B are Both Written Through SDATA

Therefore fastest update time:

First update = 34*25ns + 40ns = 890 ns

Subsequent update = 24*25ns = 600 ns

After the first Aux DAC refresh, subsequent refresh of the Aux DAC outputs in the above mentioned direct access mode takes place after every 24 clocks. Note that the Aux DAC takes about 12 mA on AVDD3_AUX (when full scale output is set to 5 mA each Aux DAC).

10.11 Full Duplex Operation – Coupling Considerations

When operating the transmit and receive channels simultaneously, several factors need to be considered in order to minimize the coupling between the transmit and receive channels. In a general case, the DAC and ADC clocks can be at arbitrary rates, with or without harmonic relations to each other. In such a case, there exist serious possibilities of coupling between the ADC and DAC. As far as possible, we recommend driving the ADC and DAC with the same clock rate externally, and use the internal clock division and multiplication to adjust to the required ADC and DAC clock rates internally.

The internal block diagram of the clocking path is repeated below.

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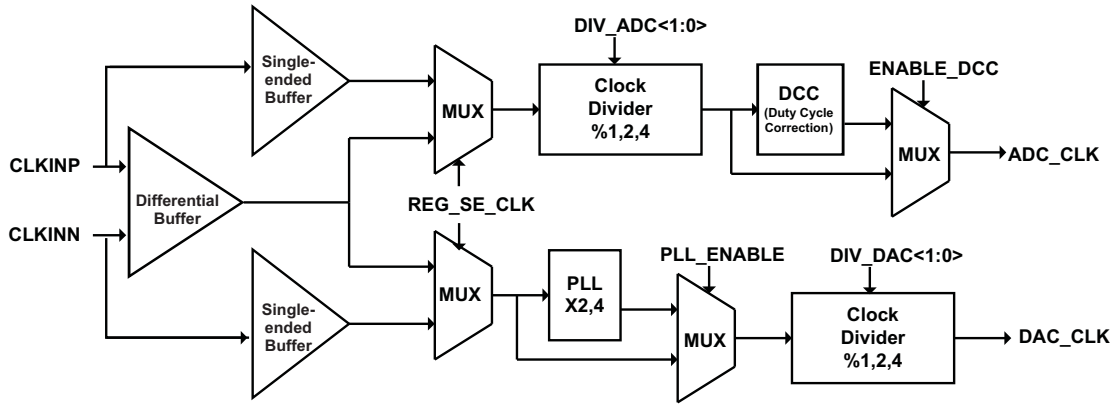

Figure 10-20. Block Diagram of Clocking Path

Three cases are considered:

Case 1: DAC_CLK and ADC_CLK are at same rate: In this case, either CLKINP and CLKINN should be driven by a differential clock (common to both the ADC and DAC) or two single ended clocks, both at the same rate.

Case 2: DAC_CLK and ADC_CLK are at different rates such that the higher rate is 2X or 4X of the lower rate: In this case, we again recommend driving CLKINP/CLKINN differentially (or by two equal rate single ended clocks) at the higher of two rates and dividng internally by the factor of 2 (or 4) on the channel that requires the lower rate clock.

Case 3: DAC_CLK and ADC_CLK are at different rates with the DAC_CLK being at 8X or 16X of the ADC_CLK: In this case, we recommend driving CLKINP/CLKINN differentially (or by two equal rate single ended clocks) at 4X of ADC_CLK rate, dividing it by 4 for the ADC, and multiplying it by 2 (or 4) for the DAC.

Case 4: DAC_CLK and ADC_CLK are at different rates that are harmonically related but not at rates covered by Case 2 or Case 3: In this case, there is no alternative but to drive CLKINP and CLKINN with two different rate clocks. If phase control of the two clocks is possible, we recommend that the phases be adjusted such that the two clocks have rise/fall edges that do not come within 5 ns of each other. We also recommend that the driving clock rates be as close to each other as possible.

Case 5: DAC_CLK and ADC_CLK are at different rates that are non-harmonically related: This is the worst case and it is recommended to avoid operating the AFE in full duplex mode with such clock rates. The presence of non-harmonically related clocks at two adjacent pins can cause periodic modulation in the sampling instant that can result in huge spurs that get worse at higher ADC input frequencies (and DAC output frequencies). At 70 MHz IF, these spur levels could be as large as –45 dBc.

10.12 Half Duplex Operation – Coupling Considerations

If the ADC and DAC are driven externally by unequal rate clocks, then ensure that these clocks are not on simultaneously. For example, in half duplex mode with the Tx active, ensure that the ADC clock to the device is shut off. If the ADC and DAC are driven by equal rate clocks, then it is not required to shut off the ADC clock when the Tx is active (and DAC clock when the Rx is active).

10.13 Half Duplex Operation Through a Common I/O Interface

If the AFE7222/7225 is to be always operated in Half Duplex mode through a common I/O interface for the RX and TX (to reuse the same bus), then the RX and TX data and clocks can be tied on the board as illustrated below:

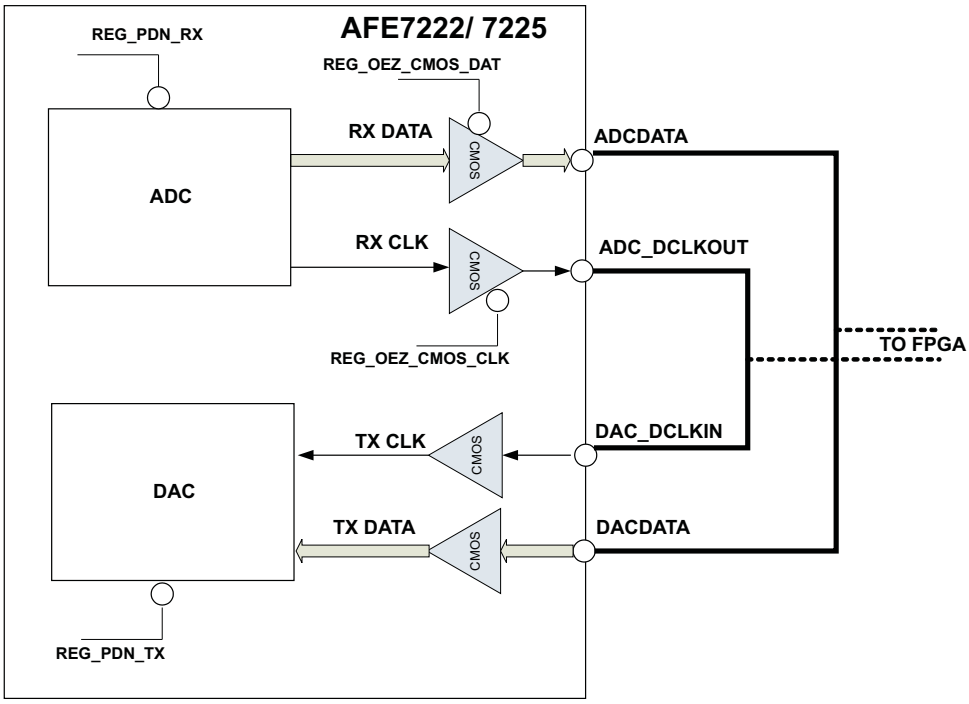

Figure 10-21. I/O Interface

To enable the TX in Half Duplex mode, set:

REG_PDN_RX=1, REG_OEZ_CMOS_DAT=1, REG_OEZ_CMOS_CLK=1, and drive the DACDATA and DAC_DCLKIN pins as TX input pins.

To enable the RX in Half Duplex mode, set:

REG_PDN_TX=1 and receive data and clock from the RX on the same bus.

For a pin control to be able to toggle between RX half duplex and TX half duplex modes, set bit REG_HALF_DUPLEX_THRU_PIN. When this mode is set, the PDN pin serves as a toggle pin – when the PDN pin is high, the device operates in Half duplex RX mode and when the PDN pin is low, the device operates in Half duplex TX mode.

Note that half duplex mode through a common I/O interface and the full duplex mode will require different board configurations, since in the former mode, the I/O bus is shared.

11 QUICK GUIDE

Supplies:
We recommend driving the Device with 3 supplies :
3V supply – Tie pins 11, 14, 17, 22 to this supply
1.8V analog supply – Tie pins 1, 4, 7, 10, 19, 25, 62, 64 to this supply
1.8V digital supply – Tie pins 32, 41, 49 to this supply

Power up sequence:
Power on the 3V and 1.8V supplies in any sequence
Apply a high going pulse on RESET of minimum width 100 ns to reset the internal registers of the device.

Software RESET:
In addition to the hardware RESET pin, the device also has a software RESET bit. This is a self-clearing bit, so it needs to be only asserted whenever the device needs to be reset. The software RESET can be applied by programming register address 000, Data 02.

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Clocking:
By default, the device expects a differential clock on CLKINP and CLKINN. This differential clock is used to drive both the ADC and DAC.
In case the clock source is single ended, then short CLKINN to a voltage of 0.95V and apply the single ended clock source on CLKINP – alternatively, CLKINP can be driven with a voltage of 0.95V and the single ended clock source can be applied on CLKINN.
A third alternative is to use the single ended clock buffer inside the device. This mode saves about 9 mW of power since the differential clock buffer is shut down. By setting register (address 20A, Data 20), the single ended clock buffer can be enabled. In that case, Pin 8 provides the single ended clock for the DAC whereas Pin 9 provides the single ended clock for the ADC – if a single clock source is to be used for both, then tie pins 8 and 9 to this clock source.

Biasing the ADC inputs:
The common mode of the ADC input pins should set to VCM, which is nominally 0.95V (measured after programming the initialization registers). Deviating from this input common mode can cause degraded performance. The full scale input swing on the inputs is 2 Volt differential peak-to-peak. When biased optimally at 0.95V, the device gives a full scale output code when the positive input swings between roughly 0.45V and 1.45V (and correspondingly the negative input swings between 1.45V and 0.45V). It is recommended to operate the ADC at an input that is at least 1 dB below full scale.

ADC output format:
The ADC gives out a 12-bit output in 2s complement format. For the most negative input, the ADC gives out a code of 100000000000. For the most positive input, the output code is 011111111111.

RX data output capture (CMOS mode) :
The RX output data format is DDR (Dual data rate) CMOS. The output of the ADC channel A can be captured using the rising edge of ADC_DCLKOUT. The output of ADC channel B can be captured using the falling edge of ADC_DCLKOUT. The clock rate of ADC_DCLKOUT matches with the input clock rate (on CLKINP, CLKINN).

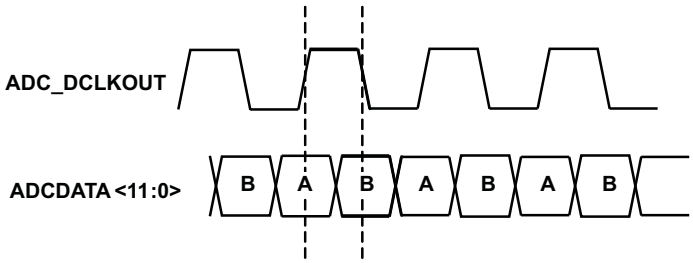

Figure 11-1. RX CMOS Output Interface

A variety of test patterns can be output by the device in order to debug issues with the capture. To enable the test patterns, program register address 042, Data 08. Once this register is programmed, we can change the output pattern as follows :

TO REPLACE NORMAL DATA WITH THE FOLLOWING	.. ON CHANNEL A WRITE	.. ON CHANNEL B WRITE
All bits 0	Address 031, Data 01	Address 037, Data 01
All bits 1	Address 031, Data 02	Address 037, Data 02
All bits toggle between 0 and 1	Address 031, Data 03	Address 037, Data 03
Linearly ramping code that ramps through min to max code	Address 031, Data 04	Address 037, Data 04
12-bit Custom code	Address 031, Data 05	Address 037, Data 05

The 12 bits for the custom code (C<11 :0>) can be set (common for Channel A and B) using the following bits:

C<11> = Bit D5 of regster address 03F
C<10> = Bit D4 of regster address 03F
C<9> = Bit D3 of regster address 03F

C<8> = Bit D2 of regster address 03F
C<7> = Bit D1 of regster address 03F
C<6> = Bit D0 of regster address 03F
C<5> = Bit D7 of regster address 040
C<4> = Bit D6 of regster address 040
C<3> = Bit D5 of regster address 040
C<2> = Bit D4 of regster address 040
C<1> = Bit D3 of regster address 040
C<0> = Bit D2 of regster address 040

For example, programming registers (Address 03F Data 29) and (Address 040 Data 34) replaces the normal ADC data for both channels with the static binary code 101001001101.

DAC input format:
The DAC input format is also 2s complement similar to the ADC.

Full scale DAC current:
The full scale DAC current (IOUTFS) is set by the resistor (of value RBIASJ) on the BIASJ pin.

IOUTFS = 19.2/RBIASJ.
For RBIASJ=960Ω, IOUTFS = 20 mA

For the 12-bit input code (where CODE is the decimal representation of the DAC data input word in straight offset binary format):

IOUTP = IOUTFS × CODE / 4096
IOUTN = IOUTFS × (4096 – CODE) / 4096

TX data input (CMOS mode):
The TX input data format is also DDR CMOS. The rising edge of the DAC_DCLKIN latches the Channel A data inside the AFE7225/7222, and the falling edge latches the Channel B data. The clock rate of DAC_DCLKIN is same as the input clock rate when interpolation is not set. When 2X interpolation is set, it should be half the input clock rate, and when 4X interpolation is set, it should be one-fourth the input clock rate.

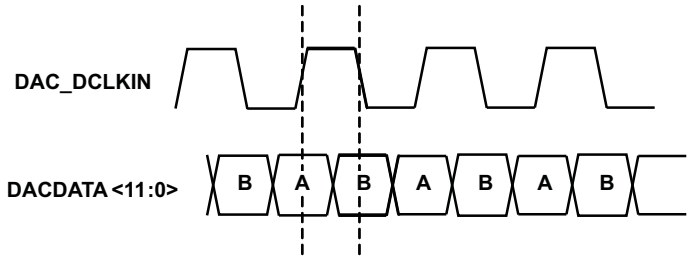

Figure 11-2. TX CMOS Input Interface

Interpolation:
While interpolating by a factor of 2, the DAC_DCLKIN rate should be set to half of the input clock rate.
The 2X interpolation mode on the TX side can be set by the following register : Address 106, Data 05.

Powerdown modes:
The device has several powerdown modes which provide a tradeoff between power consumed and speed of recovery from powerdown. The nature of the powerdown mode can be set through the registers. Also the assertion of the powerdown can be done either through the PDN pin or through a register bit.

While using the PDN pin to control the powerdown state, the following are the register configurations (see specifications table for recovery times)

Global powerdown mode through PDN pin : Set Address 207, Data 20, and control PDN pin to assert/ de-assert global powerdown mode. Most functions are shutdown.

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Fast recovery powerdown mode through PDN pin : Set Address 207, Data 40, and control PDN pin to assert/ de-assert fast recovery powerdown mode. RX and TX are both put to light sleep, for fast recovery.

Powerdown TX through PDN pin : Set Address 207, Data 02, and control PDN pin to assert/ de-assert TX powerdown mode. In this mode, the TX path is shut down and the RX is fully active, but TX is waiting for fast recovery.

Powerdown RX through PDN pin : Set Address 207, Data 04, and control PDN pin to assert/ de-assert RX powerdown mode. In this mode, the RX path is shut down and the TX is fully active, but RX is waiting for fast recovery.

In the above cases, the PDN pin was used to assert/ de-assert the powerdown state. Alternatively, a register bit can be used to assert/ de-assert the powerdown state. This is bit D7 of register address 207. The corresponding register configurations to assert/ de-assert the powerdown through the register bit are as follows (in this case, keep the PDN pin low).

MODE	TO ASSERT POWERDOWN WRITE	TO DE-ASSERT POWERDOWN WRITE
Global powerdown through register	Address 207, Data A0	Address 207, Data 20
Fast recovery powerdown through register	Address 207, Data C0	Address 207, Data 40
TX powerdown through register	Address 207, Data 82	Address 207, Data 02
RX powerdown through register	Address 207, Data 84	Address 207, Data 04

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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• Changed DETAILED BLOCK DIAGRAM	2
• Deleted product preview for AFE7225 from PACKAGE/ORDERING INFORMATION	3
• Changed SUPPLY CHARACTERISTICS	10
• Changed TX DAC ELECTRICAL CHARACTERISTICS	13
• Changed Data setup times	16
• Changed Data hold times	16
• Added Note to TIMING REQUIREMENTS FOR RECEIVE PATH – LVDS AND CMOS MODES	16
• Changed t_{delay} times	16
• Changed Output clock duty cycle	16
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• Added note to RECOMMENDED OPERATING CONDITIONS	9
• Changed SUPPLY CHARACTERISTICS table	10
• Added RX and TX active, No input signal applied on ADC and DAC to Supply current, full duplex mode test conditions	10
• Changed Power dissipation to Supply current in POWER IN CMOS MODE	10
• Added RX and TX active, No input signal applied on ADC and DAC to Supply current, full duplex mode test conditions	10
• Added Power dissipation in Sleep modes MAX values	11
• Added (with MSB first format) to SPI REGISTER READOUT 3rd bullet	20
• Changed Figure 8-1	69
• Changed Figure 9-3 figure title	72
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• Changed Figure 9-8 figure title	75
• Added Figure 10-5 figure title	84
• Added Figure 10-6 figure title	84
• Added Figure 10-9 figure title	86
• Added Figure 10-10 figure title	86
• Changed BYPASS_BUF to BYPASSZ_BUF in Figure 10-15	89

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AFE7222IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AFE7222I
AFE7222IRGCR.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AFE7222I
AFE7222IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AFE7222I
AFE7222IRGCT.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AFE7222I
AFE7225IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AFE7225I
AFE7225IRGCR.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AFE7225I
AFE7225IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AFE7225I
AFE7225IRGCT.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AFE7225I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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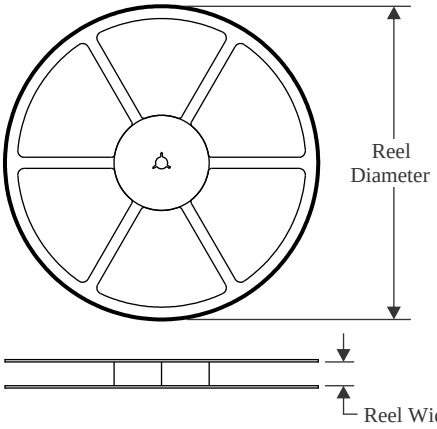
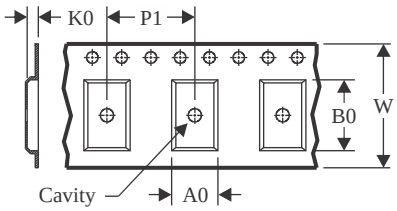
TAPE AND REEL INFORMATION

REEL DIMENSIONS

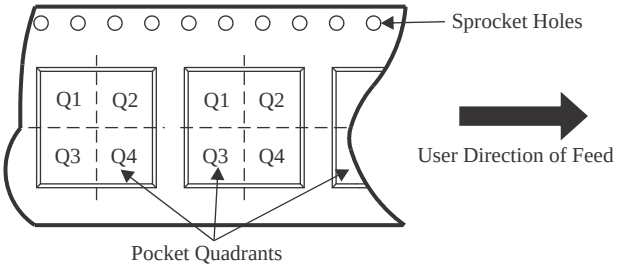


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

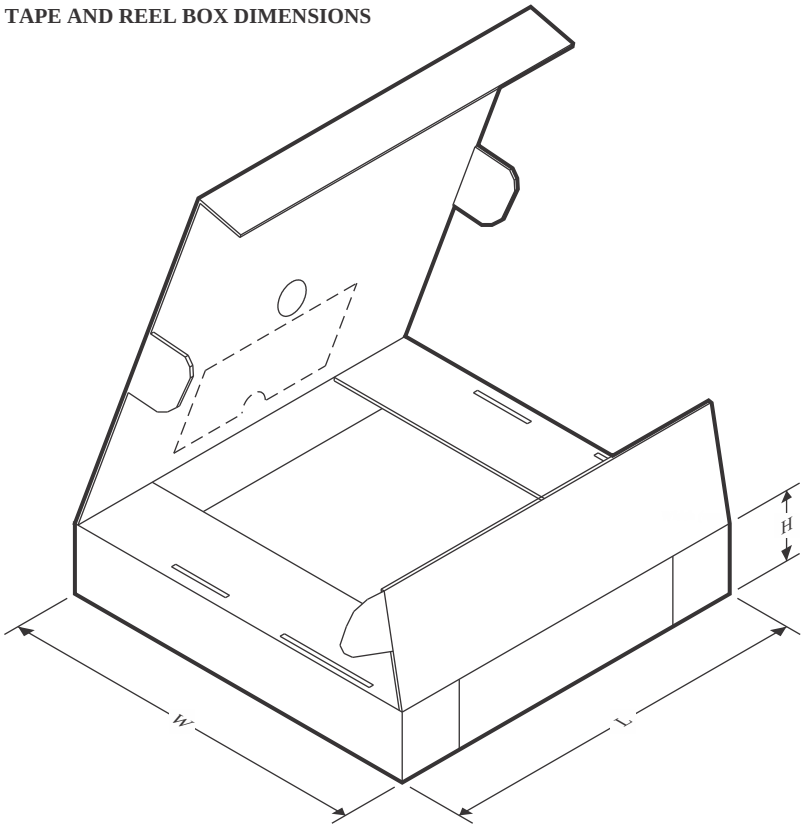
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AFE7222IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
AFE7225IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AFE7222IRGCR	VQFN	RGC	64	2000	350.0	350.0	43.0
AFE7225IRGCR	VQFN	RGC	64	2000	350.0	350.0	43.0

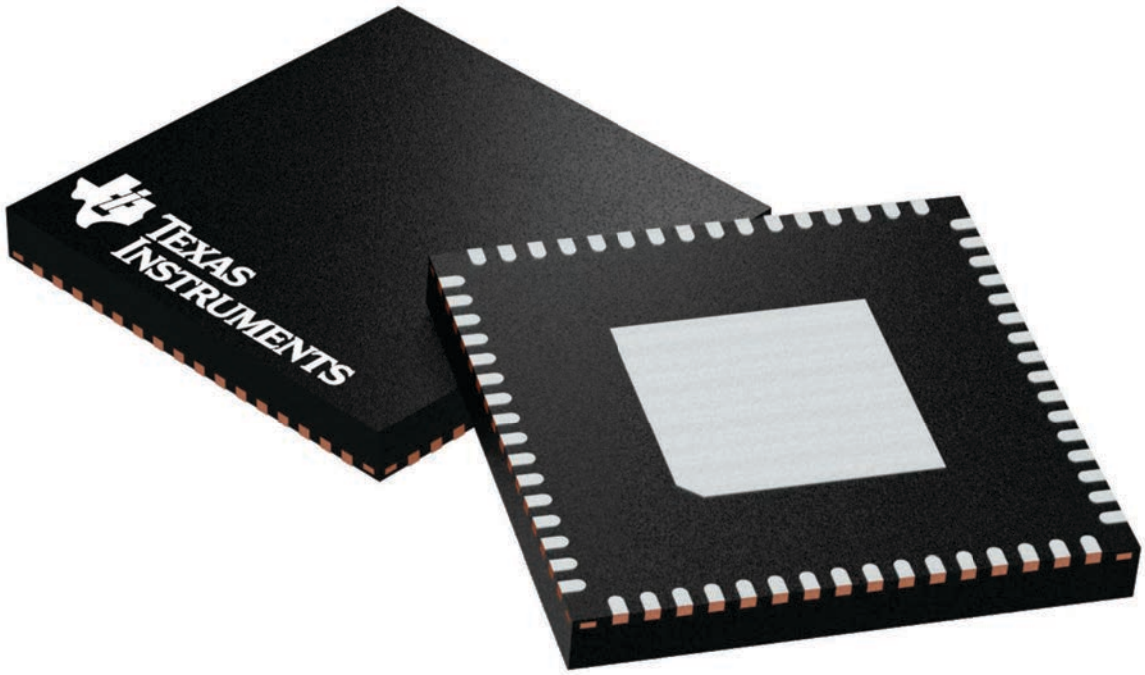
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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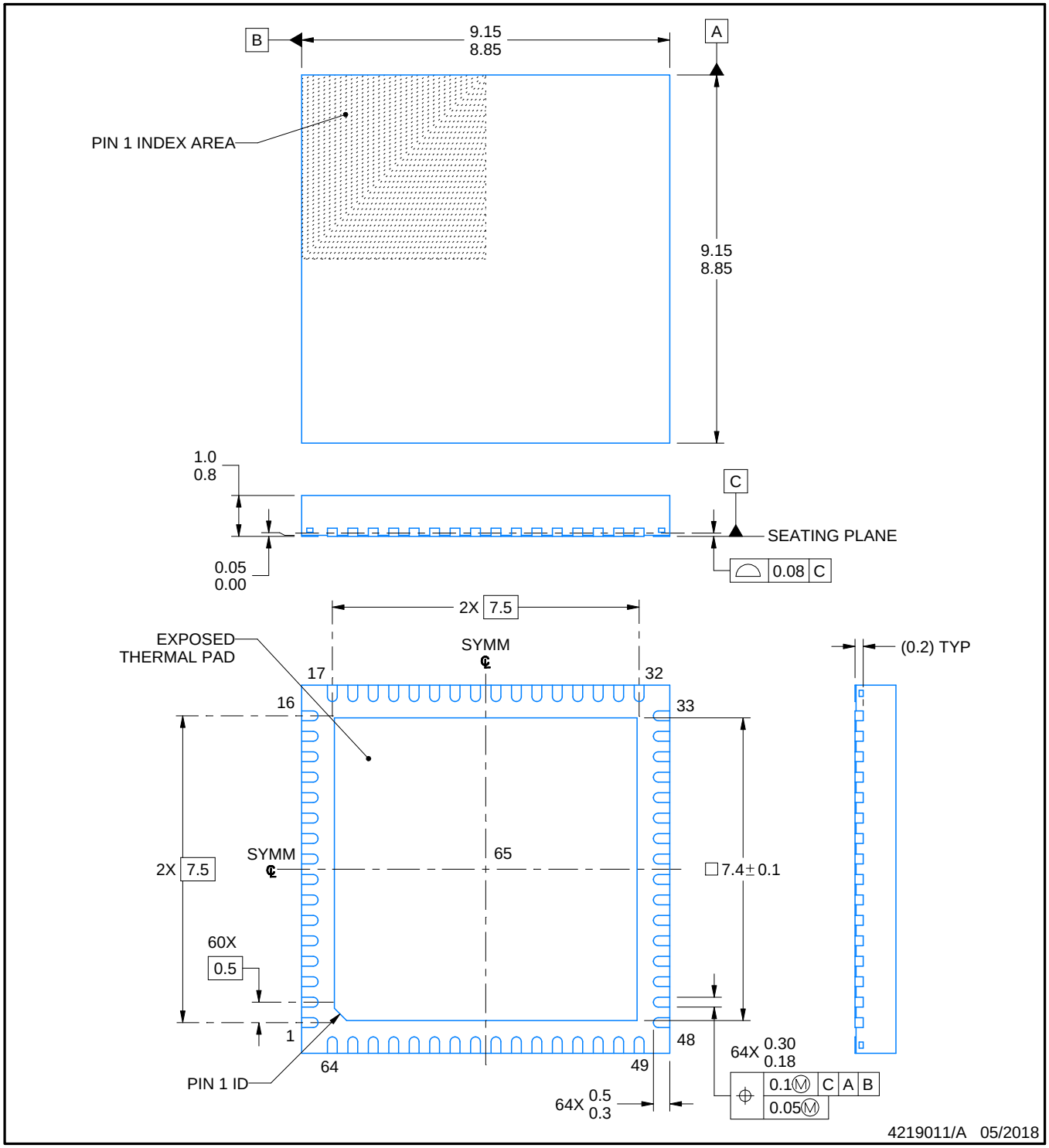
PACKAGE OUTLINE

RGC0064H

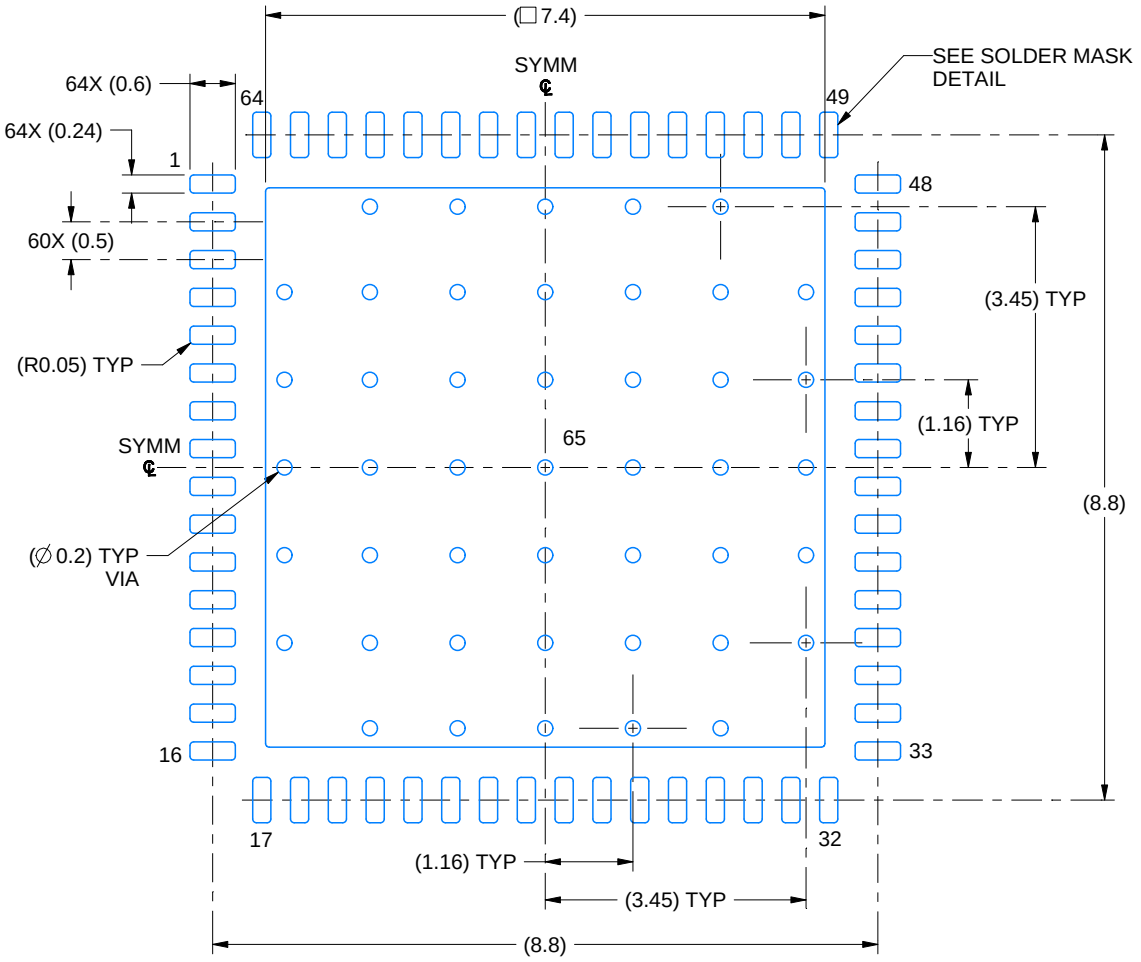
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

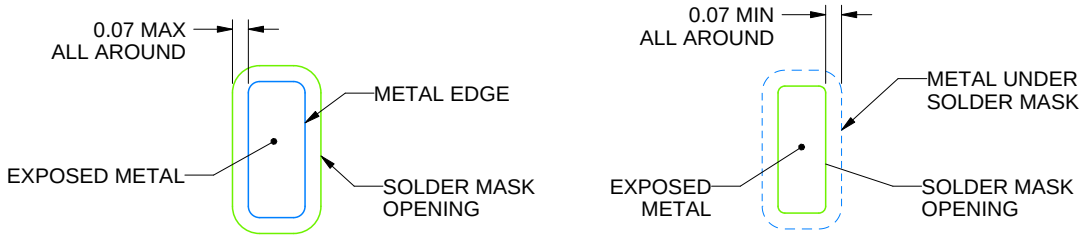


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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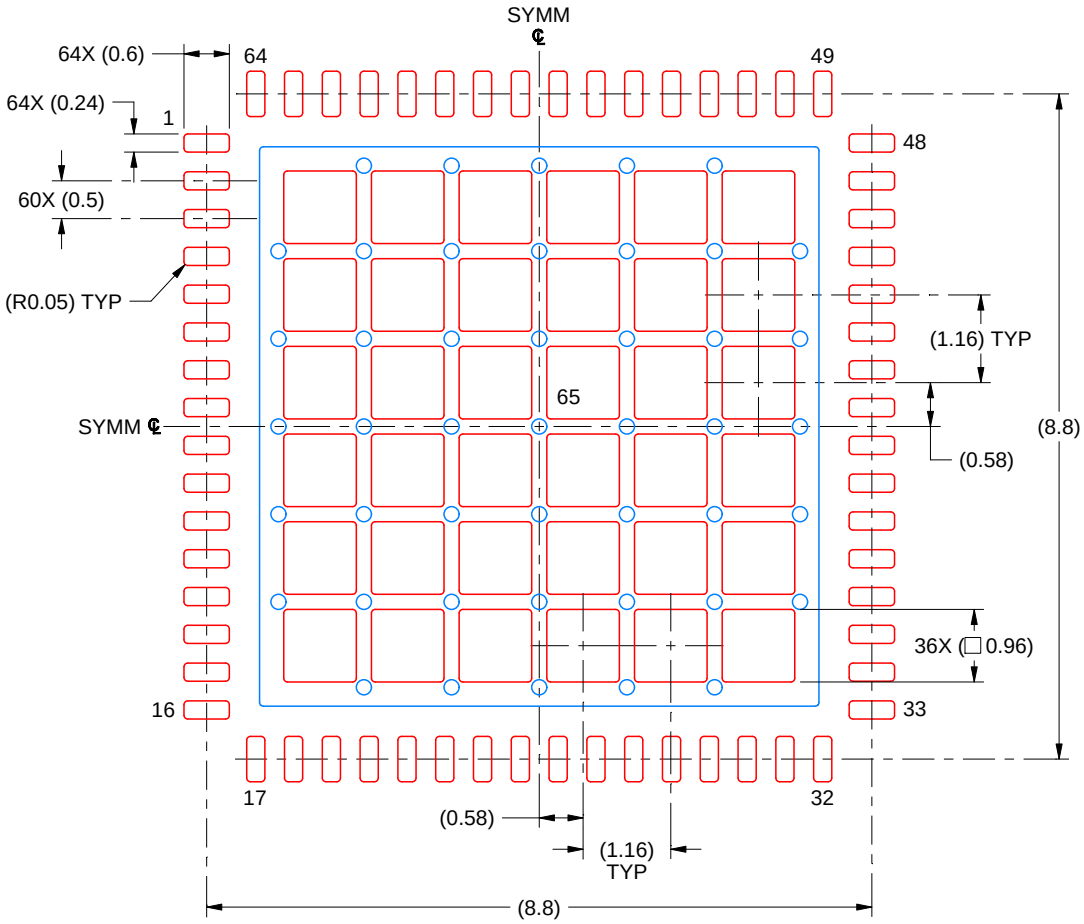
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
61% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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