AK1595
Bluetooth® Low Energy transmitter

1. General Description

The AK1595 is a Bluetooth® 5.2 transmitter IC that greatly simplifies the addition of wireless connectivity to a system. There is no need to develop complicated, proprietary micro controller code; Bluetooth® Low Energy compliant advertising transmission can be achieved by simply configuring the transmission power, data, and transmission start trigger via the AK1595's UART or I²C interface. Using the AK1595 to add wireless connectivity to a product can simplify system design and reduce BOM cost.

2. Features

- Bluetooth® 5. 2
  - Bluetooth® 5.2 compliant
  - Support 31 octets Advertising data length
  - Supports 2402MHz, 2426MHz, 2480MHz frequencies
  - Supports 1Mbps data rate
  - Built–in interface and test circuitry for Bluetooth® certification tests

  Note: AK1595 does not support extended advertising PDU, secondary advertising, LE2M, AoA, AoD options

- Microprocessor Interface
  - UART and I²C
  - UART Baud Rate: 9600bps or 115200bps

- RF transmission
  - Maximum RF power: 0dBm
  - RF power adjustable range: 0dBm to -32dBm
  - Initiate transmission via register or TXON pin

- Whitening, CRC, GFSK
  - Built–in data whitening feature and CRC compliant with Bluetooth® Low Energy.
  - Support GFSK(1Mbps)

- Power-supply voltage
  - 2.0V to 3.7V

- Package
  - 20-pin HWQFN (3mm x 3mm, 0.4mm pitch)

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4. Notation

The following notations are used for specific signals and register names

- Name: Internal signal name
- <name>: Register addresses
- {Name}: Register bit name

The numerical values are expressed as follows

- 0x4D2: Hexadecimal numbers
- 0d1234 or 1234: Decimal numbers
- 0b100 1101 0010: Binary numbers

Combination of bit number and numerical value

- 8'hAB: 8-bit hexadecimal data.
- 8'b1010 1011: 8-bit binary data.

ex)
6'h12 = 6'b010002
8'h12 = 8'00010002

Terms and acronyms

- AdvA Advertiser's Device Address
- BLE Bluetooth® Low Energy
- CRC Cyclic Redundancy Check
- GFSK Gaussian Frequency Shift Keying
- I^2C Inter-Integrated Circuit
- LDO Low Drop Out
- LSB Least Significant Bit
- MCU Micro Controller Unit
- MSB Most Significant Bit
- PDU Protocol Data Unit
- PLL Phase Locked Loop
- PPM Part Per Million
- RF Radio Frequency
- SW Switch
- TX Transmit
- UART Universal Asynchronous Receiver Transmitter

These 3 terms describe the packet data of Bluetooth® Low Energy Advertising channel. The data format is shown in Figure 1.

- Payload
- AdvA
- AdvData

LSB MSB

<table>
<tr><td rowspan="3">Preamble</td><td rowspan="3">Access Address</td><td colspan="3">PDU</td><td rowspan="3">CRC</td></tr>
<tr><td rowspan="2">Header</td><td colspan="2">Payload</td></tr>
<tr><td>AdvA</td><td>AdvData</td></tr>
<tr><td>1octet</td><td>4octets</td><td>2octets</td><td>6octets</td><td>0 to 31octets</td><td>3octets</td></tr>
</table>

Figure1. Bluetooth® Low Energy Advertising Channel packet format

5. Block Diagram and Functions

5.1. Block Diagram

Power supply and ground pins are not included.

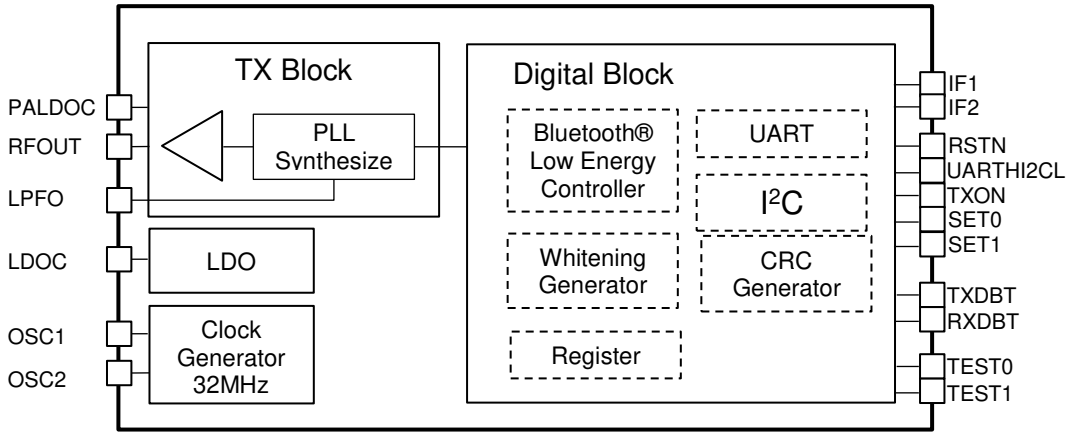


Figure 2. Overall Block Diagram

5.2. Functions

- Digital Block
  - Write/read registers via the UART or I²C interface
  - Power-down and timing control
  - Generation of transmit data and CRC code
  - Data whitening processing
  - Bluetooth authentication test

- Clock generator 32MHz
  - This block generates a reference oscillator frequency of 32MHz.

- LDO
  - This block generates power to the digital and TX Block from AVDD power supply.

- TX Block
  - Configure the TX Block using PLLs and RFAMP. This block generates BLE advertising channels of 2402MHz, 2426MHz, and 2480MHz based on an external crystal oscillator and a 32MHz clock generated by the Clock Generator. GFSK is modulated based on the transmitted data generated by the digital block. The RFAMP amplifies and outputs the signals generated by the PLLs. The output power can be adjusted from 0dBm to -32dBm in the registers.

6. Pin Configurations and Functions

6.1. Pin Configurations

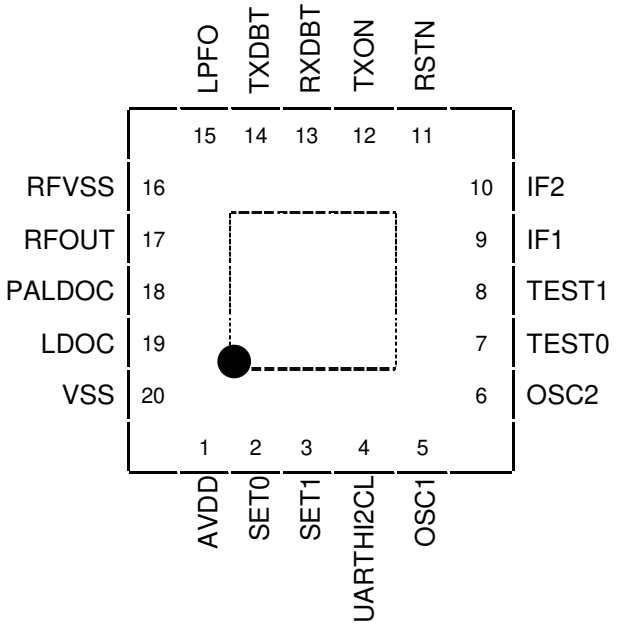


Figure 3. Pin configurations (Top view)

6.2. Functions

<The meaning of abbreviations used in the "I/O" column of the pin table is shown below>

AI:	Analog input pin	DO:	Digital output pin
AO:	Analog output pin	DIO:	Digital I/O pin
AIO:	Analog I/O pin	P:	Power supply pin
DI:	Digital input pins	G:	Ground pin

Pin No.	Pin name	I/O	Pin Functions	State after reset	Max. load capacitance	Pull-up/ Pull-down	Remarks
TX Section							
17	RFOUT	AO	RF signal Output				
18	PALDOC	AO	Connection for an external TX output adjustment inductor to RFOUT pin.				
External Interface							
11	RSTN	DI	Reset pin				
9	IF1	DI	Interface input pin UART: RXD I^2C: SCL				Note2
10	IF2	DIO	Interface input/output pin UART: TXD I^2C: SDA	UART:H I^2C: Hi-Z	UART:15 pF I^2C: 400 pF		Note2
2	SET0	DI	Interface setting pin UART: UART Baud Rate setting L: 9,600bps H: 115,200bps I^2C: I^2C slave address setting				
3	SET1	DI	Interface setting pin UART: UART interface Enable I^2C: I^2C slave address setting				
13	RXDBT	DI	Inputs for Bluetooth certification tests			Pull-up	Note3
14	TXDBT	DO	Outputs pin for Bluetooth certification test	L	15pF		
4	UARTHI2CL	DI	Interface selection pin H: UART L: I^2C				
12	TXON	DI	RF transmit trigger pin				Note1
7	TEST0	DI	For AKM Test			Pull-down	Note1
8	TEST1	DI	For AKM Test			Pull-down	Note1
Common Section							
19	LDOC	AO	Connection for external LDO output capacitor				Note4
5	OSC1	AI	32MHz Crystal oscillator				
6	OSC2	AO	32MHz Crystal oscillator				
15	LPFO	AIO	Connection for an external capacitor for the loop filter				
Power supply							
1	AVDD	P	Power supply				
16	RFVSS	G	Ground for RFAMP				
20	VSS	G	Ground				

Note1 Must be connect to VSS if the pin is unused.
Note2 When using AK1595 with I^2C interface, the voltage to be pulled up must be the same as the AK1595 power supply voltage.
Note3 This pin must remain unconnected except during Bluetooth certification testing.
Note4 The LDOC pin must only be connected to a capacitor. Connecting it to any external device is prohibited.
Note5 Leave the exposed pad on the bottom surface of the package disconnected.

7. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	VDD	-0.3	6.0	V	Note 1
Ground Level	VSS	0	0	V	
Input Voltage1	Vin1	VSS-0.3	VDD+0.3	V	Note 1, Note2
Input Voltage2	Vin2	VSS-0.3	2.5	V	Note3
Input Current	Iin	-50	+50	mA	
Output Current	Iout	-50	+50	mA	
Storage Temperature	Tstg	-55	+125	ºC	

Note1 All voltages with respect to ground level (0V).
Note2 Except LPFO pin and RFOUT pins
Note3 LPFO pin and RFOUT pin
WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

8. Recommended Operating Conditions

The specifications are applicable within the operating range (supply voltage/operating temperature) specified below.

Parameter	Symbol	Voltage	Ground pin	Remarks
Ground pin	VSS	0V	VSS, RFVSS	

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Operating Temperature	Ta	-40		85	ºC	
Supply Voltage	VDD	2.0	3.0	3.7	V	AVDD pin

Note 1 All voltages with respect to ground level (0V).
Note 2 AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

9. Electrical Characteristics

The specifications below apply within the Recommended Operating Range (supply/operating temperatures) and external matching circuits as shown in the Recommended External Circuits section.

9.1. Characteristics of RF Outputs

Parameter		Min.	Typ.	Max.	Unit	Remarks
Center Frequency Note1	Frequency 1	-	2402	-	MHz	
	Frequency 2	-	2426	-	MHz	
	Frequency 3	-	2480	-	MHz	
Output power	Power setting 1		0		dBm	
	Power setting 2		-32		dBm	
Adjustable step for output power		0		-	dB	Note 3
GFSK Note2	Average frequency deviation for 00001111 sequence (Δf).	±225	±250	±275	kHz	
	Ratio average frequency deviation (10101010 sequence / 00001111 sequence)	80	-	-	%	
	Minimum frequency deviation (Δfmin)	±185	-	-	kHz	
	Bit rate	-	1.0	-	Mbps	
	BT(Bandwidth-Time)	-	0.5	-		
	Modulation index (m)	0.45	0.50	0.55		m=(2*|Δf|) / (bit rate)
	In-band spurious emission			-20 -30	dBm dBm	1MHzBW @2MHz offset 1MHzBW @>3MHz offset

Note 1 Channel frequency means center frequency of modulation.
Note 2 GFSK characteristics based on Bluetooth® Low Energy test specification (RF-PHY)
Note 3 This is a reference value and not a guaranteed value.

9.2. Current Consumptions

The specifications below apply within the Recommended Operating Range (supply/operating temperatures) and external matching circuits as shown in the Recommended External Circuits section.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Full Power Down	SIDD1	Note 1	-	15		nA
Advertising	IDD1	Note 2	-	8		mA
Intermission	IDD2	Note3	-	0.9		mA

Note 1 VDD=3.0V, Room Temperature (25deg. C).
Note 2 VDD=2.0 to 3.7V, Temperature range = -40 to 85deg. C, TX_ch:2426MHz, RFOUT:0dBm
Note 3 VDD=2.0 to 3.7V, Temperature range = -40 to 85deg. C, <Address 0x03> EVENTNUM[2:0] bits ≠ 3'd1

9.3. Characteristics of 32 MHz Crystal Oscillator

Parameter	Min.	Typ.	Max.	Unit	Remarks
Oscillator frequency		32.000		MHz	Note1
Stabilization time after startup			2	msec	Note2

Note1 Frequency tolerance should be ±50ppm or less including external components.
Note2 This is a reference value and not a guaranteed value.
Note3 Request a sample from the oscillator manufacturer for evaluation on the board, and check the oscillation characteristics before use.

9.4. Characteristics of Timer

Transmission interval

Parameter	Min.	Typ.	Max.	Unit	Remarks
Tch_int		(8+PDULEN[5:0]) * 8 + 30		µsec	Note1
AdvInterval	0.02		10.24	sec	15 control bits which is programmed by register Note2
AdvDelay	0		10	msec	Randomly generated Note2

Note1 When Bluetooth RF-PHY certification testing, Tch_int = 625 µsec
Note2 <Address 0x03> EVENTNUM[2:0] bits ≠ 3'd1

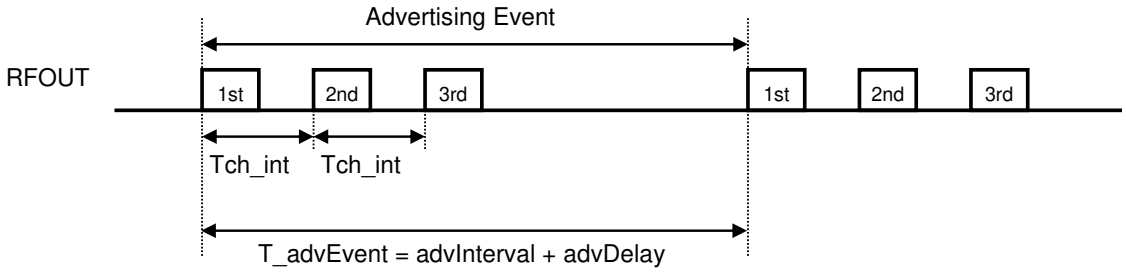


Figure 4. Interval of Advertising Event

10. Electric Characteristics of Digital Interface

The specifications are applicable within recommended operating range (supply voltage/operating temperature).

10.1. Digital DC Characteristics

Parameter	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
High level input voltage	Vih	Note 1		0.7×VDD	-	-	V
Low level input voltage	Vil	Note 1		-	-	0.3×VDD	V
High level input current	Iih1	Note 2 Note 3	Vih = VDD	-10	-	+10	μA
Low level input current	Iil1	Note 2 Note 4	Vil = VSS	-10	-	+10	μA
High level input current	Iih2	Note 4	Vih = VDD	40	100	170	μA
Low level input current	Iil2	Note 3	Vil = VSS	-170	-100	-40	μA
High level output voltage	Voh	Note 5	Ioh = -100μA	0.8×VDD	-	-	V
Low level output voltage (except SDA pin)	Vol1	Note 5	Iol = 100μA	-	-	0.2×VDD	V
Low level output voltage for SDA pin	Vol2	Note 6	Iol = 3mA	-	-	0.4	V

Note 1 Digital input pins: RSTN, IF1, IF2, SET0, SET1, RXDBT, UARTHI2CL, TXON pins
Note 2 Digital input pins: RSTN, IF1, IF2, SET0, SET1, UARTHI2CL, TXON pins
Note 3 Digital input pin: RXDBT pin
Note 4 Digital input pins: TEST0, TEST1 pins
Note 5 Digital output pins: TXDBT, IF2(TXD) pins
Note 6 Digital output pin: IF2(SDA) pin

10.2. Digital AC Characteristics

Switchover timing of digital AC characteristics are specified at ½ VDD level unless otherwise noted.

10.2.1. System Reset

10.2.1.1. Hardware Reset

The AK1595 executes a hardware reset when the RSTN pin detects “Low” for more than 1µsec and initializes all internal states. In order to ensure the AK1595’s full hardware reset, the following setup and timing are required.

The AK1595 selects the UART interface;
IF1 pin = “High”, TXON pin = “Low”.

The AK1595 selects the I²C interface
IF1 pin = “High”, IF2 pin = “Hi-Z”, TXON pin = “Low”.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Reset pulse width	tRSTN	1	-	-	µsec	

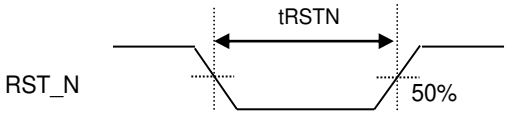


Figure 5. AC Timing of Hardware Reset

10.2.1.2. Software Reset

The AK1595 executes a software reset when <Address 0x3F>SOFTRST[7:0] bits are set to =8'b1010_1010 initializing internal digital blocks. The AK1595 state is changed to sleep when the I²C interface is used. It is changed to standby state when the UART interface is used. Therefore, the AK1595 needs reconfiguration of all blocks afterwards. The SOFTRST[7:0] bits automatically return to 8'b0000_0000 after software reset is executed. In order to ensure the AK1595 software reset, the following setup is required during reset period.

TXON pin = “Low"

10.2.1.3. UART Interface Reset (UENABLE)

When the UART interface is selected, the UART I/F controller block is initialized when the SET1 pin (UENABLE) detects “Low” for more than 1µsec. In order to ensure the AK1595 UART interface is reset, the following setup and timing are required.

UARTHI2CL pin = “High” and IF1 pin = “High”

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
UART reset pulse width	tURSTN	1	-	-	µsec	

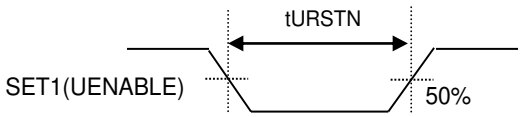


Figure 6. AC Timing of UART Interface Reset

10.2.2. TXON

The AK1595 starts transmission when the TXON pin detects “High” while the device is not in reset. The AK1595 stops transmission after a number of advertising events that as defined by <Address 0x03> EVENTNUM[2:0] bits ≠ 3'd0 even if TXON is set to “High”. The AK1595 will be able to start transmission again after TXON pin transitions from “Low” to “High”. In this case, minimum 10 µsec low period is required.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
TXON "L" Pulse Width	tTXONL	10	-	-	µsec	

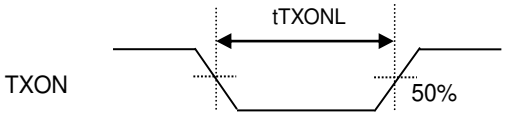


Figure 7. AC Timing of TXON

10.2.3. Serial Interface Timing of UART

When the UARTHI2CL pin is "H", the IF1 pin and IF2 pin operate as UART interfaces.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Baud Rate1	rBAUD	-	9,600	-	bps	SET0 pin:"L"
Baud Rate2	rBAUD	-	115,200	-	bps	SET0 pin:"H"
Baud Rate Accuracy	bERR	-	-	±2.5	%	Note1
Byte Data Send Wait Time	tMIN	0	-	-	msec	
Command Turnaround Time	tTURN	0	-	-	msec	

Note1 This is a reference value and not a guaranteed value.
Note2 While data is being received from the IF1 (RXD), the AK1595 does not transmitt from the IF2 (TXD).
Note3 Do not transmit data to the IF1 (RXD) while data is being transmitted from the IF2 (TXD).

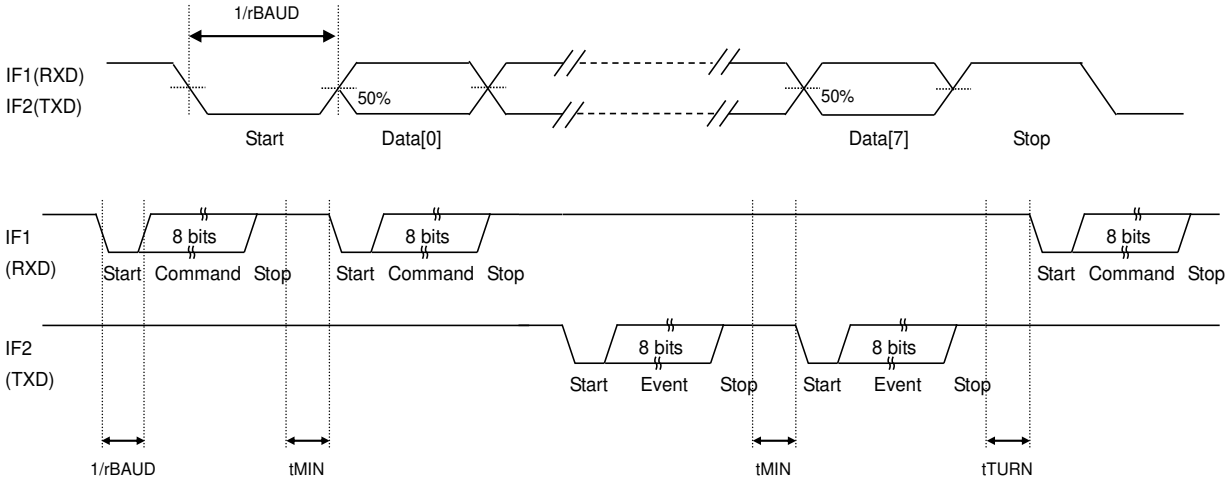


Figure 8. AC Timing of UART

10.2.4. Serial Interface Timing of I²C

When the UARTHI2CL pin is "L", the IF1 pin and IF2 pin operate as I²C interfaces. The AK1595 supports fast mode I²C interface (max:400kHz).

Item	Symbol	Min	Typ	Max	Unit
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µsec
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µsec
Clock Low Time	tLOW	1.3		-	µsec
Clock High Time	tHIGH	0.6		-	µsec
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µsec
SDA Hold Time from SCL Falling	tHD:DAT	0		-	µsec
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µsec
Rise Time of Both SDA and SCL Lines	tR	-		0.3	µsec
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µsec
Setup Time for Stop Condition	tSU:STO	0.6		-	µsec
Capacitive load on bus	Cb	-		400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP			50	nsec

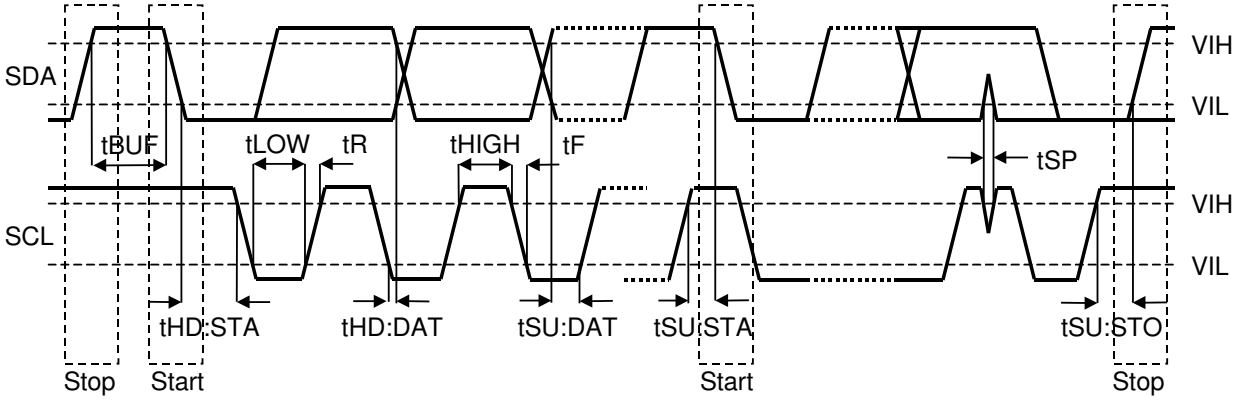


Figure 9. AC Timing of I²C

11. Serial Interface

The AK1595 supports UART and I²C interfaces and registers may be read from and written to using both interfaces. The AK1595 configures its selected interface by the UARTHI2CL, SET1, SET0 pins. The table below shows the interface configuration.

UARTHI2CL pin	Interface	SET1 pin	SET0 pin
L	I²C	I²C slave address setting (CAD1)	I²C slave address setting (CAD0)
H	UART	UART interface Enable (UENABLE)	UART Baud Rate setting (BRATE)

11.1. UART interface

11.1.1. Pin Condition

Connect the UARTHI2CL pin to VDD when the UART interface is used.
The IF1 pin = RX data (RXD)
The IF2 pin = TX data (TXD)
UART flow control is not supported.
The Baud Rate of the UART can be switched by the SET0 pin.
SET0 pin= “Low”, 9600bps
SET0 pin= “High”, 115200bps

The UART interface is disabled when the SET1 pin (UENABLE) is set to "Low". In this disable status, Data transfer from RXD and TXD both are disabled because the UART Interface control block is initialized.
When the AK1595 UART interface is used, the UART interface should be enabled by changing UENABLE “Low” to “High”. At least 3 msec is required to start UART interface after UENABLE is set “Low” to “High”.
Switching between UARTHI2CL and BRATE settings after reset release is prohibited. Switching between UARTHI2CL and BRATE settings during reset.

11.1.2. UART Format

The start bit is a single bit set to "0". The data is 8 bits and has no parity. The stop bit is a single bit, and this bit is set to 1. 8-bit data performs LSB (Least Significant Bit) first communication. Data received by the IF1 pin through the UART interface are defined as commands, and data sent by the IF2 pin are defined as events. The command and event formats are as follows:

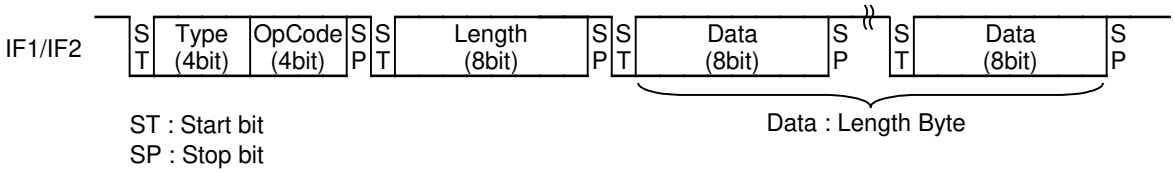


Figure.10 UART command/event format

The Type consists of 4 bits. When inputting commands from the RXD, set the Type bit to 4 b0001. Events from TXD are Type = 4 b0100.

Type	Function
4'b0001	Command
4'b0100	Event
Other than above	Prohibited

The OpCode consists of 4 bits. Specify an OpCode of 4'b0001 or 4'b0010 when accessing the register for Write or Read.

OpCode	Function
4'b0001	Write
4'b0010	Read
Other than above	Prohibited

The Length field shows the length of the subsequent command or data byte. The communication format for Data is specified in 11.1.3 Write Access and 11.1.4 Read Access.

11.1.3. Write Access

The Figure 11 shows the format for write access to the AK1595 registers.
Type = 4'b0001
OpCode = 4'b0001.

The Length field shows total byte length of Start Address and Data for the write access. Total byte length is specified by the 6 LSBs (the two MSBs are Don't Care).

The Start Address byte specifies starting register access. Specify the register address with 6 bits of LSB. The first bit of MSB is "Don't Care" and the second MSB should be "0".

Data field specifies the data to be written to the register.

The AK1595 can write multi-byte data with a single operation. When the Length is set 3 or more and data is sent after the first one-byte transfer, the AK1595's internal address counter is automatically incremented and data is written to the next address. The increment of the internal address counter stops at 6'h37. It is prohibited to set the Length and Start Address to 6'h37 when the last data is received. In addition, the <Address 0x3F> SOFTRST[7:0] cannot be written by counter increment. <Address 0x3F> When accessing SOFTRST[7:0], set Length to 6'h02 and Start Address A[5:0] to 6'h3F

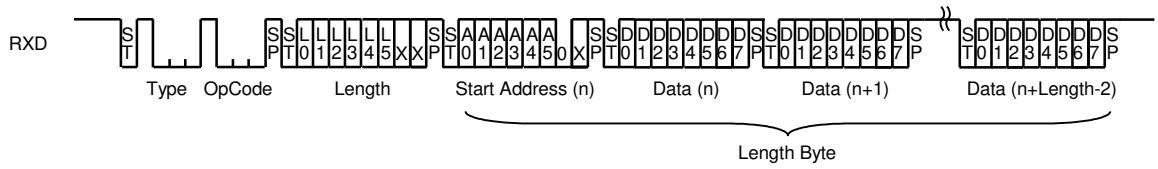


Figure 11. Write access command (RXD)

When the write access command is done, the TXD outputs events within 2msec. The event format is as follows.

Type = 4'b0100
OpCode = 4'b0001
Length is 8'b0000_0001

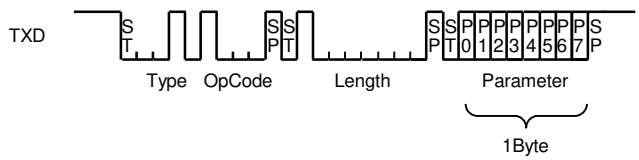


Figure 12. Write access event (TXD)

The parameter is as follows. When a command error occurs, the TXD output 8'b0000 0001 (command failed) as a parameter.

Parameter	Function
8'b0001_0000	Command succeeded
Other than above	Command failed

11.1.4. Read Access

The following format shows the read access to the registers from RXD.
Type = 4'b0001
OpCode = 4'b0010
The Length shows total byte length of Start Address and Stop Address for the read access. Total byte length is specified by the 6 bits LSBs (the two MSBs are Don't Care). 6'h02 should be specified in Length.

The Stop Address setting can be omitted by setting Length to 6'h01 when a single address is read. The Start Address is the byte that specifies starting register access. The Stop Address specifies ending register access. Specify register addresses with the six LSBs. The first MSB is "Don't Care" and the second MSB should be "0". When the same data is set to both the Start Address and Stop Address, a single address is read. When the Start Address and Stop Address are set to different addresses, the AK1595 supports multi-byte data read. Stop Address data should be higher than Start Address data.

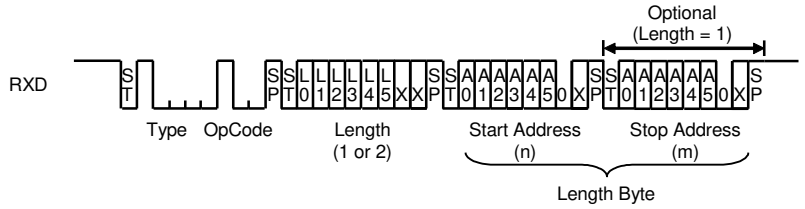


Figure 13. Read access command (RXD)

When the write access command is done, the TXD outputs events within 2msec. The event format is as follows.
Type = 4 and b0100
OpCode = 4 b0010
The Length is total data from Start Address and Stop Address.

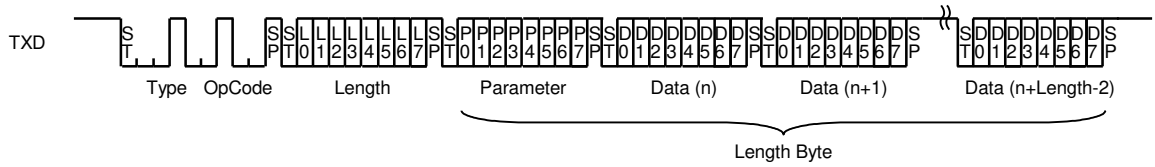


Figure 14. Read access event (TXD)

The Parameter is as follows. When a command error occurs, the TXD output 8'b0000 0001 (command failed) as a parameter. In this case, the AK1595 outputs TXD to Parameter and data is not transmitted. Refer to Section 11.1.5 Command Failed for the condition of commands errors.

Parameter	Function
8'b0001_0000	Command succeeded
Other than above	Command failed

On command success, the AK1595 can read the data as specified by the Start Address and Stop Address. The AK1595 transfers one-byte of Data and then increments the internal address counter to read the next address's data. The incrementation of the internal address counter stops at 6'h3F. The result of reading an address not defined on on the Register Map or a write-only address is "0".

11.1.5. Command Failed

The following state shows error condition of Write or Read access to the AK1595 register. The TXD outputs 8'b0000 0001 (command failed) as an event parameter when command error occurs. The TXD outputs OpCode 4'b0000 when an error is caused by OpCode.

Error judgment item	Error condition of Write command	Error condition of Read command
Type	Other than 4' b0001	
OpCode	Other than 4' b0001 and 4'b0010	
Length	6'h00, 6'h01, 8'h39 or more	Other than 6'h01, 6'h02
Relation between Start Address and Stop Address	-	Start Address > Stop Address
Last value of internal address counter	6'h37	-

11.1.6. Command and Event Timing

The commands to the RXD and the events from the TXD as follows. The TXD doesn't output data while the RXD is receiving data. It is not allowed to transmit Data to the RXD while the TXD is transmitting.
It is required to input whole byte data that is specified in Length to RXD. TXD doesn't output events unless commend transfer is finished. The TXD outputs events in 2 msec when all command, that is specified in Length, is received

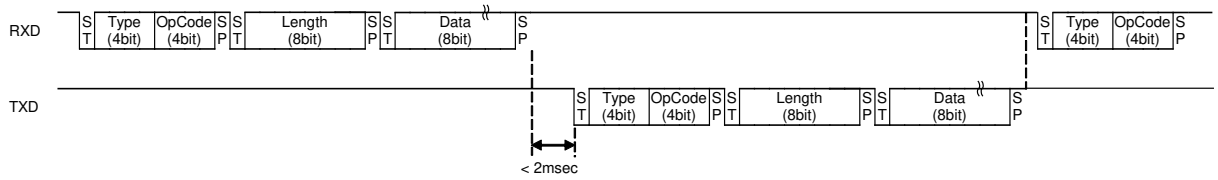


Figure 15. UART Command and Event Timing

If the start bit is not detected by TXD more than (1/rBAUD*10) sec when the Length specified bytes of data have not been transmitted, the following process is required.

To set ENABLE to "Low"; This is to initialize I/F control block.
To set ENABLE to "High"
To wait minimum TBDmsec
To resend commands

Or

Execute a hardware reset; This is to initialize all internal blocks.
Set all AK1595 setting again.

11.2. I²C interface

The I²C bus interface of AK1595 supports the Standard mode (100 kHz max.) and the Fast mode (400 kHz max.).

11.2.1. Pin Condition

When using the I²C interface, connect the UARTHI2CL pin to VSS. For the I²C interface, IF1 pin corresponds to the clock (SCL) and IF2 pin corresponds to the data (SDA). The lower 2 bits of the I²C slave address of this IC can be switched by SET1, SET0 pin. The SET1 pin supports CAD0 by CAD1, SET0 pin. The slave address is as follows:

CAD1 (SET1 pin)	CAD0 (SET0 pin)	I²C slave address
0	0	7'b01010_00
0	1	7'b01010_01
1	0	7'b01010_10
1	1	7'b01010_11

It is prohibited to change the setting of UARTHI2CL pin and CAD1, CAD0 outside of reset. Before changing the settings, be sure to perform a hardware reset.

11.2.2. Data transfer

To access AK1595 on the bus, generate a start condition first.
Next, transmit a one-byte slave address including a device address. The AK1595 compares the slave address with its own address. If these addresses match, AK1595 generates an acknowledgement, and then executes READ or WRITE instruction. At the end of instruction execution, generate a stop condition.

11.2.2.1. Change of data

A change of data on the SDA line must be made during the “Low” period of the clock on the SCL line. When the clock signal on the SCL line is “High”, the state of the SDA line must be stable. (Data on the SDA line can be changed only when the clock signal on the SCL line is “Low”.)
While the SCL line is “High”, the state of data on the SDA line is changed only when a start condition or a stop condition is generated.

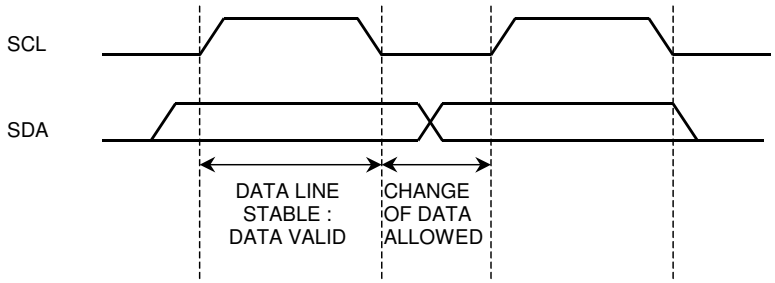


Figure 16. Data Change

11.2.2.2. Start / Stop Condition

If the SDA line is driven to “Low” from “High” when the SCL line is “High”, a start condition is generated. Every instruction starts with a start condition.
If the SDA line is driven to “High” from “Low” when the SCL line is “High”, a stop condition is generated. Every instruction stops with a stop condition.

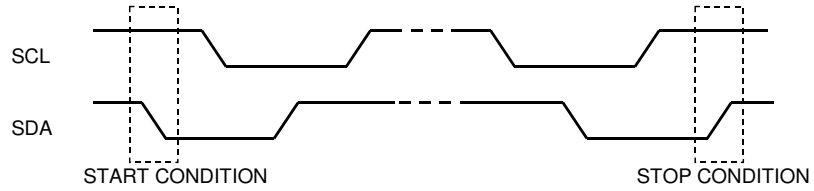


Figure 17. Start / Stop Conditions

11.2.2.3. Acknowledge

The IC that is transmitting data releases the SDA line (in the “High” state) after sending 1-byte data.
The IC that receives the data drives the SDA line to “Low” on the next clock pulse. This operation is referred to as “acknowledge.” This operation may be used to verify that data has been transferred successfully.

AK1595 generates an acknowledge after reception of a start condition and slave address.
When a WRITE instruction is executed, AK1595 generates an acknowledge after every byte is received.
When a READ instruction is executed, AK1595 generates an acknowledge then transfers the data stored at the specified address. Next, AK1595 releases the SDA line then monitors the SDA line. If a master IC generates an acknowledge instead of a stop condition, AK1595 transmits the 8bit data stored at the next address. If no acknowledge is generated, AK1595 stops data transmission.

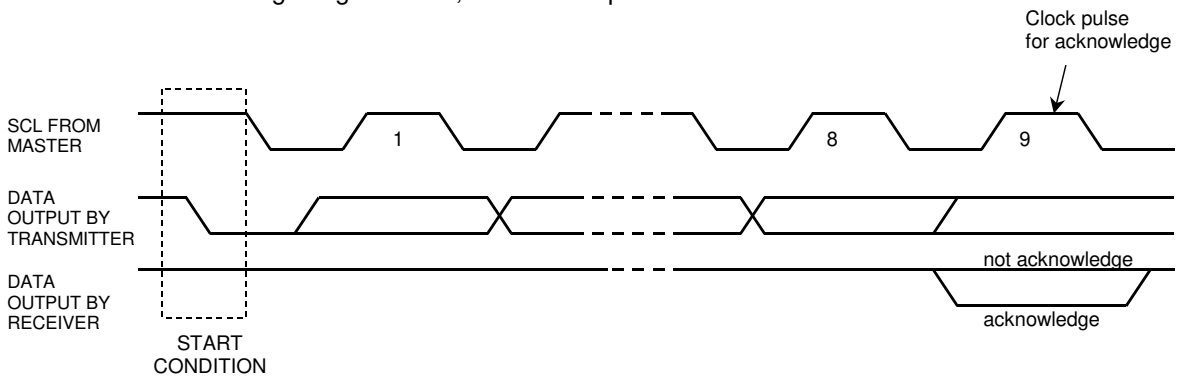


Figure 18. Generation of acknowledge

11.2.2.4. First Byte

The first byte, including the slave address, is entered after the start condition, and the slave address selects the IC on the bus to be accessed.

The slave address consists of the upper 7 bits. The upper 5 bits are fixed to 5'b01110 and the lower 2 bits can be selected by SET1 pin or SET0 pin. When a slave address is input, the IC that matches the device address generates an acknowledge and then executes the instruction. The 8th bit (least significant bit) of the first byte is R/W bit. When R/W bit = "1", the Read instruction is executed. When R/W bit = "0", the Write instruction is executed.

MSB 5 bit (fixed)					CAD1	CAD0	R/W bit
0	1	0	1	0	0/1	0/1	R/W

Figure 19. Structure of the first byte

11.2.3. Write Instruction

When the R/W bit is set to “0”, AK1595 performs a write operation.
In a write operation, AK1595 generates an acknowledge after receiving a start condition and the first byte (slave address) then receives the second byte. The second byte is used to specify the address of an internal control register and is based on the MSB-first configuration.
The second byte MSB 1st bit is don't care. The second byte MSB second bit is "0".

X	0	A5	A4	A3	A2	A1	A0

Figure 20. Configuration of the second byte (Register Address)

After receiving the second byte (register address), AK1595 generates an acknowledge then receives the third byte. The third and the following bytes represent control data. Control data consists of 8 bits and is based on the MSB-first configuration. AK1595 generates an acknowledge after every byte is received. Data transfer always stops with a stop condition generated by the master.

D7	D6	D5	D4	D3	D2	D1	D0

Figure 21. Configuration of the 3rd byte or later (Control Data)

AK1595 can write multiple bytes of data at a time. After reception of the third byte (control data), AK1595 generates an acknowledge then receives the next data. If, after receiving one byte of data, additional data is received instead of a stop condition, the address counter inside the IC is automatically incremented and the data is written to the next address. The address is incremented from 0x00 to 0x36. When the start address is “0x00”, the address is repeatedly incremented as. “0x00 -> 0x01 ->…-> 0x35 -> 0x36 -> 0x00 -> 0x01…
Address 0x3F cannot be written by the incrementing function. If accessing address 0x3F, set the address of the internal address counter to 6'h3F.

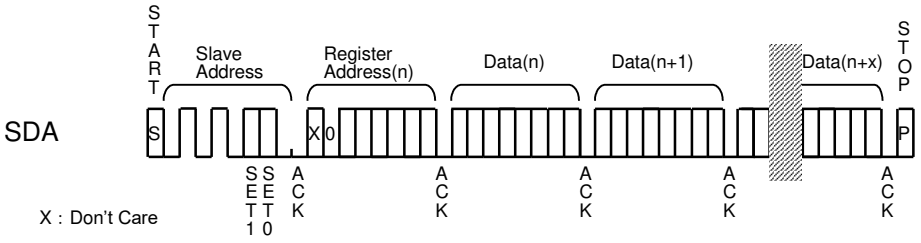


Figure 22. Write instruction

11.2.4. Read Access

When the R/W bit is set to “1”, AK1595 performs a read operation.
If a master IC generates an acknowledge instead of a stop condition after AK1595 transfers the data at a specified address, the data at the next address can be read.
Address can be 0x00h to 0x36.
The address is incremented 0x00 -> 0x01 ->…-> 0x35 -> 0x36 and the address goes back to 0x00 after 0x36.

11.2.4.1. Current Address Read

AK1595 has an address counter. In a current address read operation, the data at the address specified by this counter is read. The internal address counter holds the address that follows the most recently accessed address. For example, if the address most recently accessed (for READ instruction) is address “n”, and a current address read operation is attempted, the data at address “n+1” is read. In current address read operation, AK1595 generates an acknowledge after receiving a slave address for the READ instruction (R/W bit = “1”). Next, AK1595 transfers the data specified by the internal address counter starting with the next clock pulse, then increments the internal counter by one. If the master IC generates a stop condition instead of an acknowledge after AK1595 transmits one byte of data, the read operation stops.

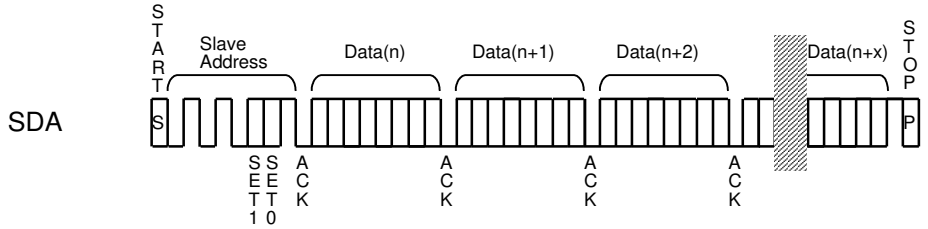


Figure 23. Current address read instruction

11.2.4.2. Random Read

By random address read operation, data at an arbitrary address can be read.
The random address read operation requires sending a dummy WRITE instruction before the slave address for the READ instruction (R/W bit = “1”) is transmitted. In random read operation, a start condition is first generated then a slave address for the WRITE instruction (R/W bit = “0”) and a read address are transmitted sequentially.
After AK1595 generates an acknowledge in response to this address transmission, a start condition and a slave address for the READ instruction (R/W bit = “1”) are generated again. AK1595 generates an acknowledge in response to this slave address transmission. Next, AK1595 transfers the data at the specified address then increments the internal address counter by one. If the master IC generates a stop condition instead of an acknowledge after data is transferred, the read operation stops.

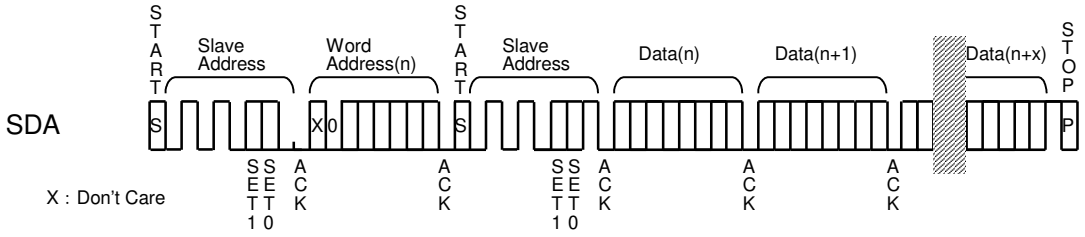


Figure 24. Random read instruction

12. Operational States

The following states are managed by the power-down control and timing control block of the digital part. For transition conditions, refer to Power-up Flow.

State	Symbol	Description
Full power down	FPD	RSTN pin = “L”. All blocks are powered down. All registers have been initialized.
Sleep	SLP	(RSTN pin = “H” and UARTHI2CL pin = “L” or RSTN pin = “H” and UARTHI2CL pin = "L" and SET1 pin = "L") and No advertising event. The AK1595 holds the register value in the sleep state.
Stand-by	STB	RSTN pin = “H” and UARTHI2CL = “H” and SET1 pin = H and No advertising event
Advertising	ADV	TX_ENB bit = “1” or TXON pin = “H” Transmitting RF during advertising.
Intermission	IMS	There are two types of intermission states. 1. (EVENTNUM[2:0] bits ≠ 3'd1 and TX_ENB bit = 1'b1 or EVENTNUM[2:0] bits ≠ 3'd1 and TXON pin = "H”) and No RF transmission is being performed for the period from the end of the advertising state to the next advertising state. 2. In Bluetooth Certification mode, waiting for HCI command or, waiting for the duration of the period between the end of one advertising state and the next.

The term” burst transmission” means repeating the advertising and intermission states.

13. Power-up Flow

13.1. Power-up Flow

Flowcharts and transition conditions after power-on for UART interface communication and I²C interface communication are shown below.

13.1.1. Power-up Flow (UART Interface)

The figure below shows the status transition when the UART interface is selected (UARTHI2CL pin = "H"). The table below shows the transition conditions.

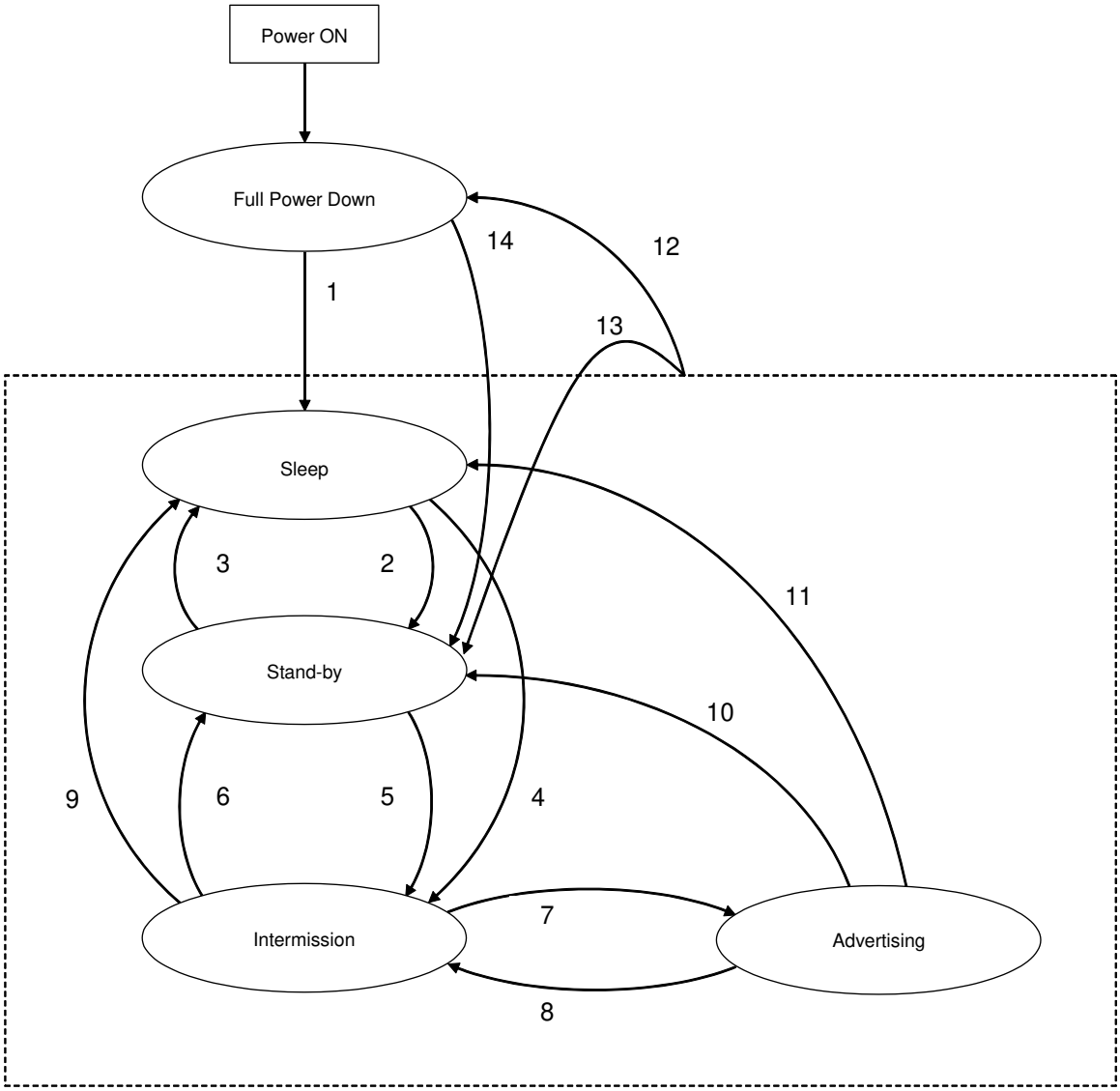


Figure 25. AK1595 UART power up flow

Transition	Transition condition
1	Release the reset when SET1 pin = "L" (RSTN pin = "H").
2	Enable UART interface (SET1 pin = "H").
3	Disable the UART interface (SET1 pin = "L").
4	Starts sending (TXONpin = "H")
5	Starts transmitting (either TXON pin = "H" or <Address 0x36> TX_ENB bit = 1'b1) or Transition to Bluetooth certification test mode (<Address 0x36> BLE_TEST_ENB bit = 1'b1)
6	When the UART interface is enabled (SET1 pin = "H"), Transmit stopped (TXON pin = "L" or <Address 0x36> TX_ENB bit = 1'b0) or End of Bluetooth certification test mode (<Address 0x36> BLE_TEST_ENB bit = 1'b0)
7	When the HCI LE Transmitter Test or HCI LE Set Advertising Enable (Enable) command is entered in the Bluetooth certification test mode, <Address 0x03> When the advertising interval ends (ADVINTVL_EXPIRE = 1'b1) because the number of events specified by the EVENTNUM[2:0] bits has not been transmitted.
8	At the end of transmission of the selected advertising channel, <Address 0x03> The number of events specified by the EVENTNUM[2:0] bits have not been transmitted, When HCI LE Test End or HCI LE Set Advertising Enable (Disable) or HCI Reset commands are inputted in Bluetooth certification test mode.
9	When the UART interface is disabled (SET1 pin = "L"), Transmit stopped (TXON pin = "L")
10	When the UART interface is enabled (SET1 pin = "H"), Transmission of the number of events specified by the <Address 0x03>EVENTNUM[2:0] bits is completed at the end of transmission of the selected advertising channel, or Transmit stopped (TXON pin = "L" or <Address 0x36> TX_ENB bit = 1'b0) or When HCI LE Test End or HCI LE Set Advertising Enable (Disable) or HCI Reset commands are entered in the Bluetooth certification test mode.
11	When the UART interface is disabled (SET1 pin = "L"), At the end of transmission of the selected advertising channel, the transmission of the number of events specified by the <Address 0x03>EVENTNUM[2:0] bits are completed, or Transmit stopped (TXON pin = "L")
12	Hardware reset with TXON pin = "L" (RSTN pin = "L") Note: Hardware resets are prohibited while TXON pin = "H".
13	Software reset (<Address 0x3F> SOFTRST[7:0] bits = 8'hAA) with TXON pin = "L" Note1 Software reset is prohibited when TXON pin = "H". Note2 The AK1595 initializes internal registers by the software reset.
14	Release the reset when SET1pin = "H" (RSTN pin = "H").

13.1.2. Power-up Flow (I²C Interface)

The figure below shows the state transition when the I²C interface is selected (UARTHI2CL pin = "L"). The table below shows the transition conditions.

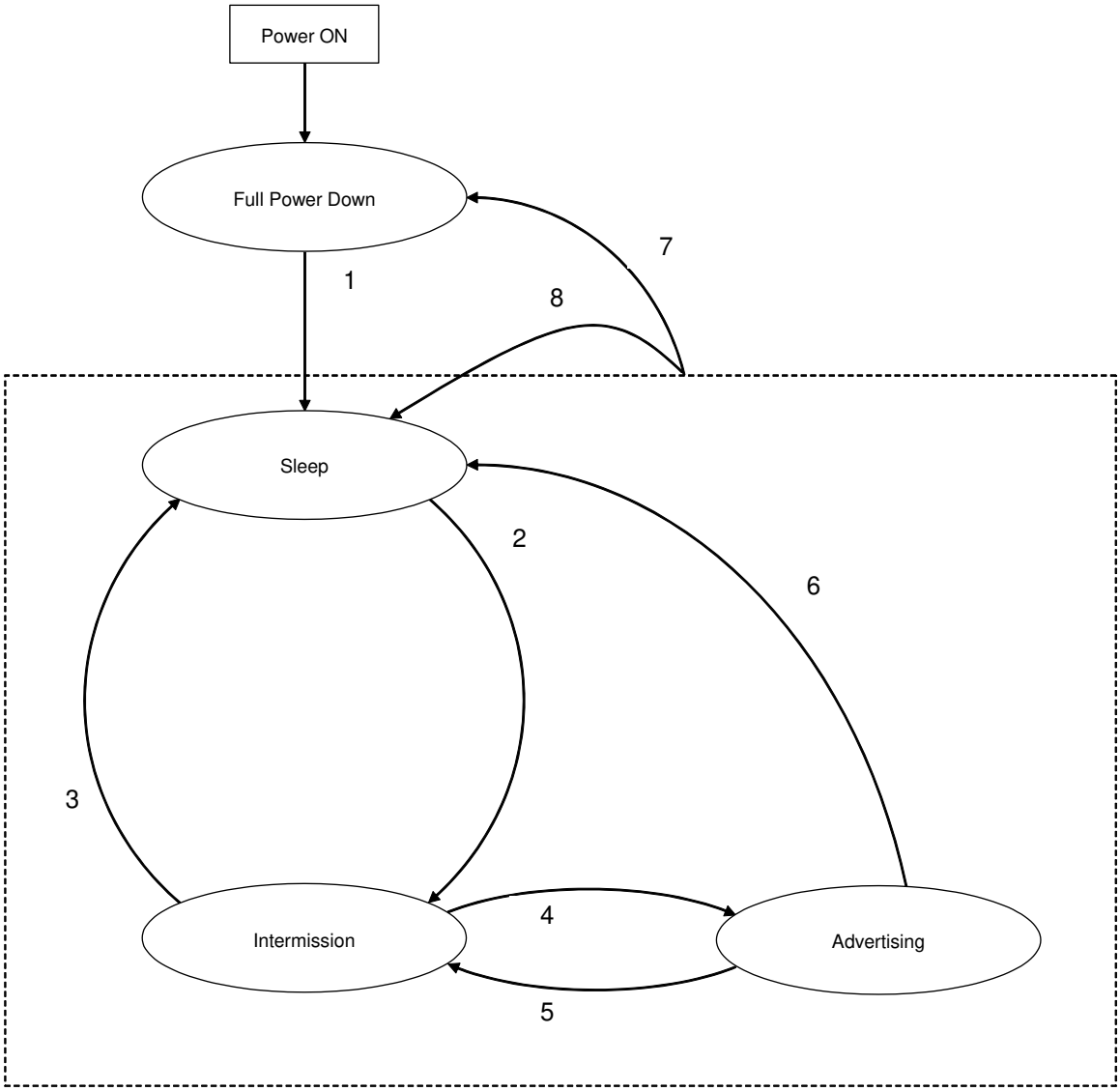


Figure 26. AK1595 I²C power up flow

Transitioned	Transition condition
1	Release of reset (RSTN pin = "H")
2	Starts transmitting (either TXON pin = "H" or <Address 0x36> TX_ENB bit = 1'b1) or Transition to Bluetooth certification test mode (<Address 0x36> BLE_TEST_ENB bit = 1'b1)
3	Transmit stopped (TXON pin = "L" or <Address 0x36> TX_ENB bit = 1'b0) or End of Bluetooth certification test mode (<Address 0x36> BLE_TEST_ENB bit = 1'b0)
4	When the HCI LE Transmitter Test or HCI LE Set Advertising Enable (Enable) command is entered in the Bluetooth certification test mode, <Address 0x03> When the advertising interval ends (ADVINTVL_EXPIRE = 1'b1) because the number of events specified by the EVENTNUM[2:0] bits has not been transmitted.
5	At the end of transmission of the selected advertising channel, <Address 0x03> The number of events specified by the EVENTNUM[2:0] bits have not been transmitted, When HCI LE Test End or HCI LE Set Advertising Enable (Disable) or HCI Reset commands are entered in Bluetooth certification test mode.
6	When transmission of the selected advertising channel ends for the number of events specified by the <Address 0x03>EVENTNUM[2:0] bits. Or stop transmitting (TXON pin = "L" or <Address 0x36> TX_ENB bit = 1'b0).
7	Hardware reset (RSTN pin = "L") or Note: It is prohibited to perform a hardware reset while TXON pin = "H".
8	Software reset (<Address 0x3F> SOFTRST[7:0] bits = 8'hAA). Note: It is prohibited to perform a software reset while TXON pin = "H

13.2. UART power up Sequence

The diagram below shows a sample startup sequence using the UART interface.
Connect the UARTHI2CL pin to VDD. <Address 0x03> EVENTNUM[2:0] bits = 3'd1 setting

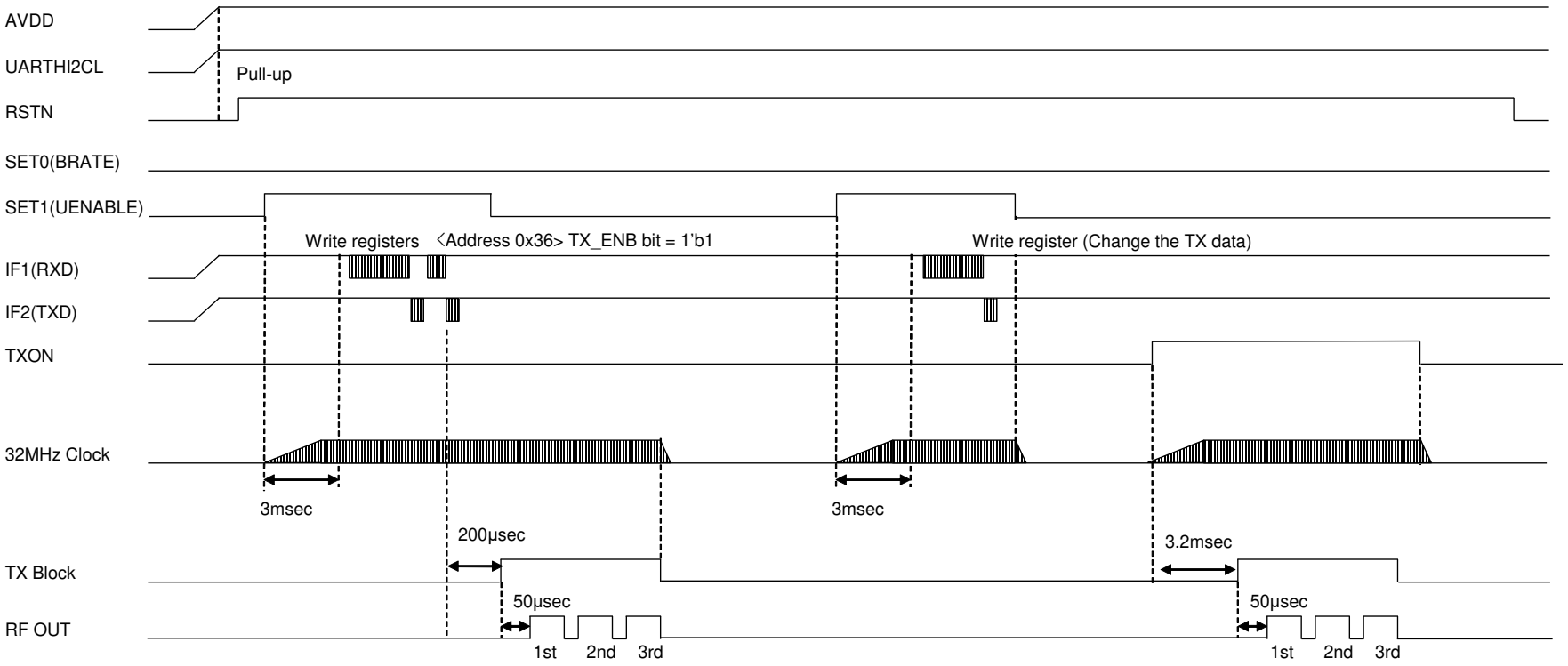


Figure 27. Flow of power up sequence (UART Interface)

13.3. I²C power up sequence

An example of the startup sequence using the I²C interface is shown in the figure below.
Connect the UARTHI2CL pin to VSS. <Address 0x03> EVENTNUM[2:0] bits = 3'd2 setting

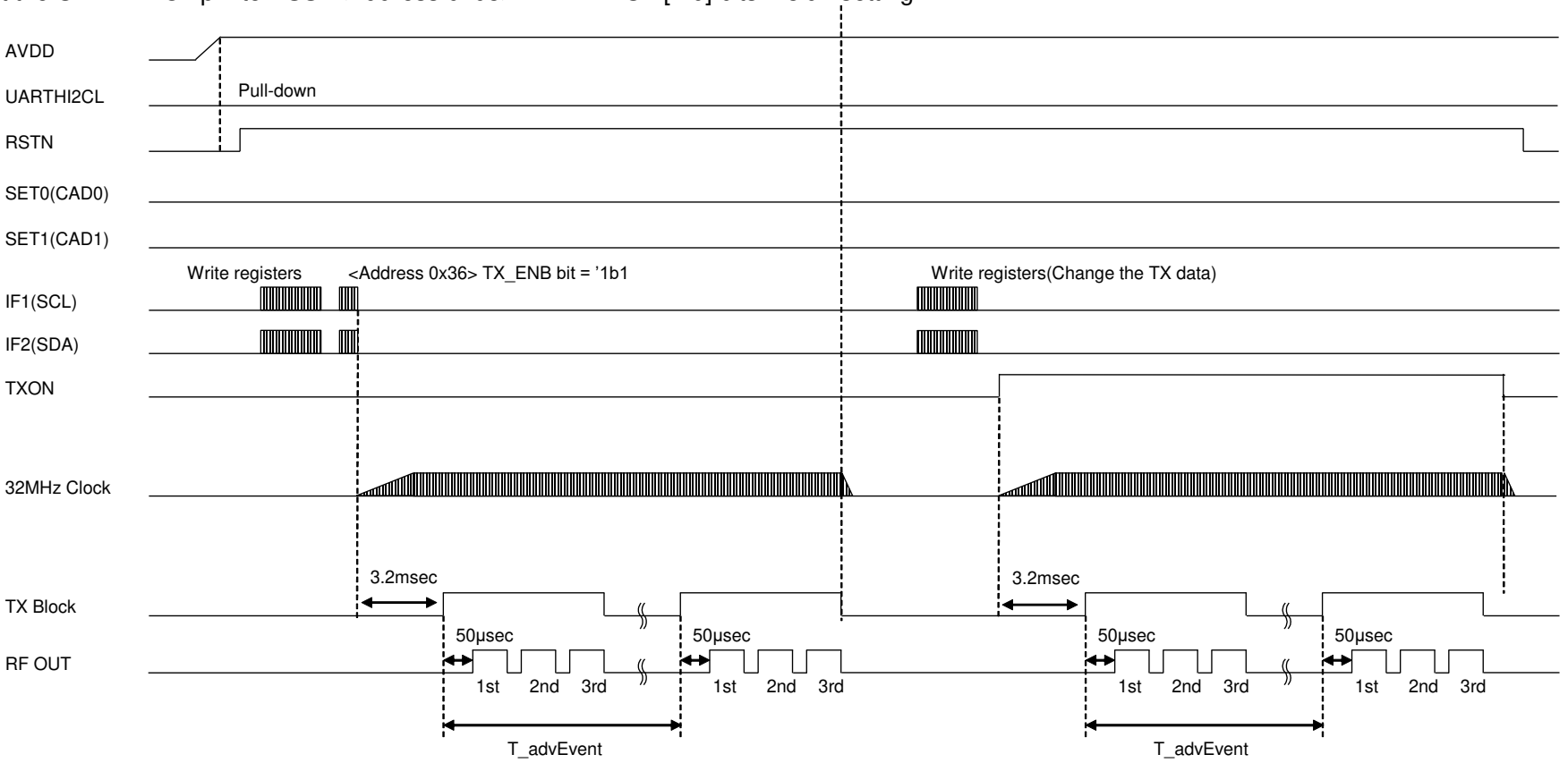


Figure 28. Flow of power up sequence (I²C Interface)

14. TX Block

14.1. RF Transmitter

Transmits modulated data from the high-efficiency RFAMP.

14.2. PLL Synthesizer

The RF signal generated from the 32 MHz clock generator.
The frequencies can be set to 2402MHz, 2426MHz, or 2480MHz with internal Fractional-N PLL.

14.3. PLL TX Modulator

AK1595 supports 1Mbps GFSK +/- modulation.
The modulation clock is generated from 32MHz clock generator.

15. Start of Transmission

<Address 0x36> Writing TX_ENB bit = 1'b1 or switching the TXON pin from "L" to "H" generates an advertising event and allows the data set in the register to be transmitted by RF. When TXON pin is set to "H", a 32-MHz clock is generated. TXON pin levels are detected after waiting 32768 clocks for clock stabilization.

<Address 0x36> If an advertising transmission is started by writing 1 to the TX_ENB bit, the burst transmission is terminated and the <Address 0x36> TX_ENB bit is initialized after the number of advertising events specified by the <Address 0x03> EVENTNUM[2:0] bits.

<Address 0x03> When EVENTNUM[2:0] bits = 3'd0, after advertising transmission is started, burst transmission continues until <Address 0x36> TX_ENB bit = 1'b0 and TXON pin is "L".

If the TXON pin is set to "H" to start transmission and the specified number of Interval of Advertising Event ends when <Address 0x03> EVENTNUM[2:0] bits ≠ 3'd0, transmission will not be performed again even if TXON pin remains "H". Transmission can be restarted by setting the TXON pin to "L" for 10 µsec or longer and then setting the TXON pin to "H" again.

<Address 0x03> If EVENTNUM[2:0] bits ≠ 3'd0, burst transmission can be forcibly terminated when <Address 0x36> TX_ENB bit = 1'b0 and TXON pin is "L"

<Address 0x36> Control by the TXON pin is disabled while RF transmission is being performed by the TX_ENB bit or <Address 0x36> BLE_TEST_ENB bit. Control of RF transmission start/stop by the <Address 0x36> TX_ENB bit or <Address 0x36> BLE_TEST_ENB bit is also disabled while RF transmission is being performed by the TXON pin.

16. Advertising Event

<Address 0x03> The number of advertising events can be set in the EVENTNUM[2:0] bits. The unit automatically enters sleep or standby after sending the specified number of times.
<Address 0x04~0x05> The interval (advInterval) of the advertising event can be changed via the ADVINTVL[14:0] bits.

17. Bluetooth Test Specification

17.1. Bluetooth Test Circuit

AK1595 integrated Bluetooth certification test function.

If performing a Bluetooth certification test, the AK1595 should be connected to the level shifter circuit and Bluetooth tester as shown below, and set the BLE_TEST_ENB bit = 1.

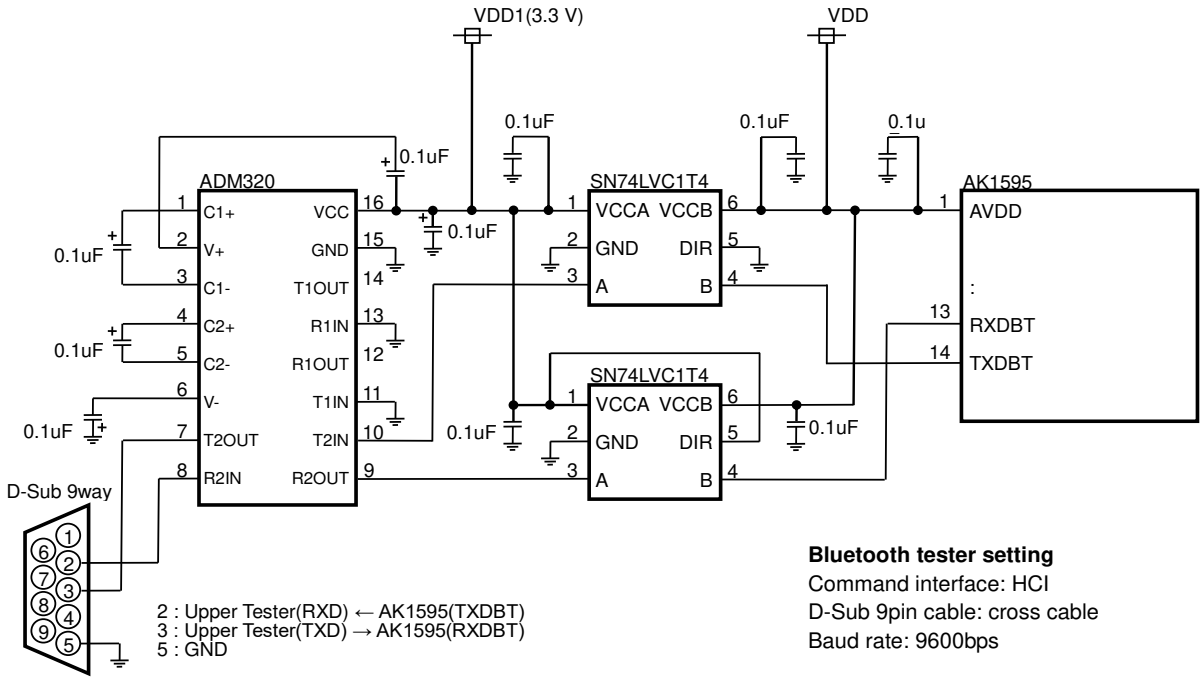


Figure 29. Bluetooth Test Setup

17.2. Test Plan

Bluetooth test plans except listed below are not guaranteed.

RF-PHY

RF-PHY/TRM-LE/CA/BV-01-C	Output power
RF-PHY/TRM-LE/CA/BV-03-C	In-band emissions
RF-PHY/TRM-LE/CA/BV-05-C	Modulation characteristics
RF-PHY/TRM-LE/CA/BV-06-C	Carrier frequency offset and drift

17.3. Register Setting for Bluetoth test

The AK1595 register settings for Bluetooth certifiation testing are as follows.

ADDR	DATA
	RF-PHY
0x00	0x00
0x01	0x06
0x02	0x00
0x03	0x00
0x04	0x00
0x05	0x00
0x06	0x27
0x07	0x55
0x08	0x29
0x09	0x41
0x0A	0x76
0x0B	0x71
0x0C	0x00
0x0D	0x25
0x0E	0x00
0x0F	0x00
0x10	0x00
0x11	0x00
0x12	0x00
0x13	0x00
0x14	0x00
0x15	0x00
0x16	0x00
0x17	0x00
0x18	0x00
0x19	0x00
0x1A	0x00
0x1B	0x00
0x1C	0x00
0x1D	0x00
0x1E	0x00
0x1F	0x00
0x20	0x00
0x21	0x00
0x22	0x00
0x23	0x00
0x24	0x00
0x25	0x00
0x26	0x00
0x27	0x00
0x28	0x00
0x29	0x00
0x2A	0x00
0x2B	0x00
0x2C	0x00
0x2D	0x00
0x2E	0x00
0x2F	0x00
0x30	0x00
0x31	0x00
0x32	0x00
0x33	0x55
0x34	0x55
0x35	0x55
0x36	0x00
0x3F	0x00

17.4. Timing Chart for Bluetooth Specification Test Mode

The timing charts for the RF-PHY and LL tests are shown below.

17.4.1. Bluetooth Specification Test Mode using UART Interface

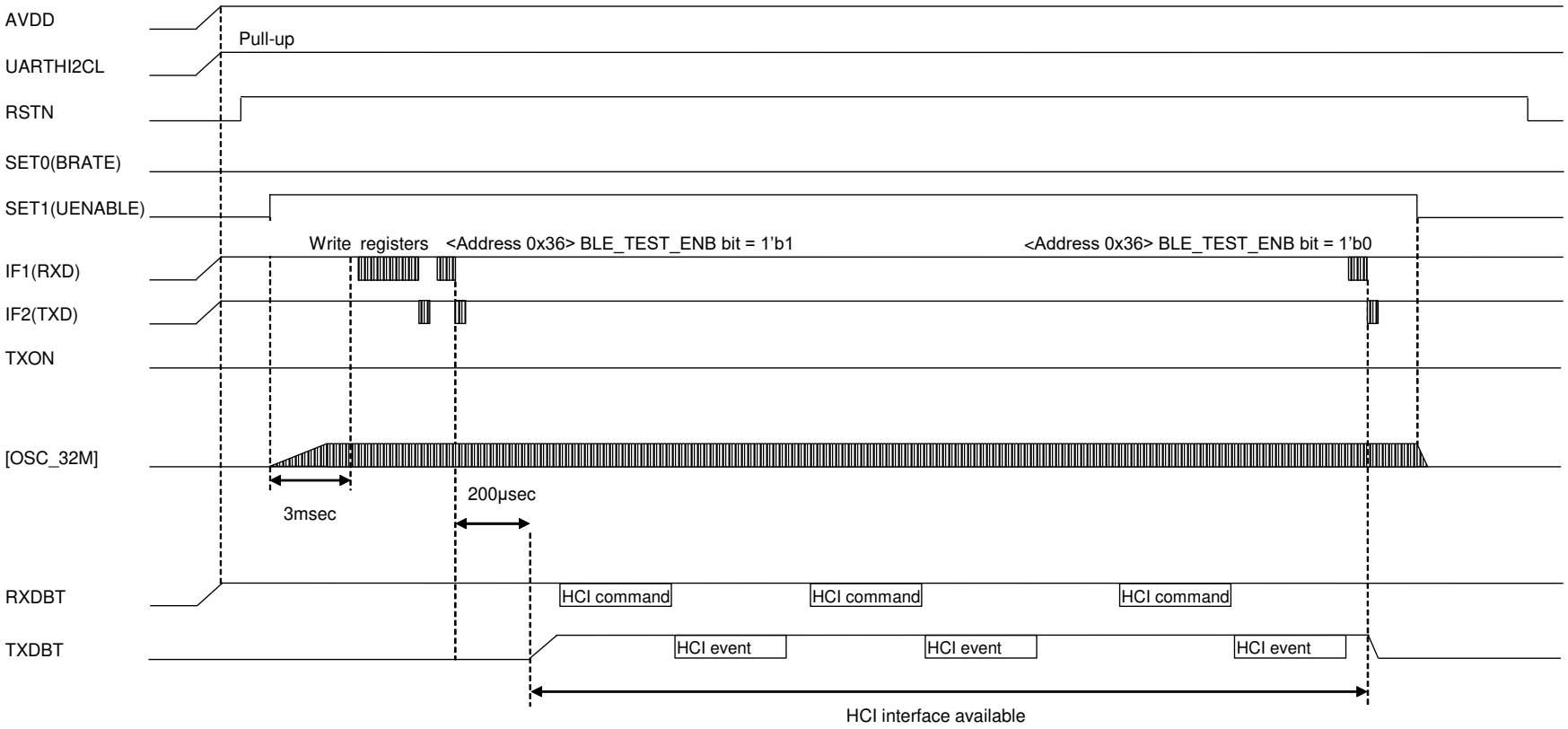


Figure 30. Timing chart of RF-PHY using UART Interface

17.4.2. Bluetooth Specification Test Mode using I²C Interface

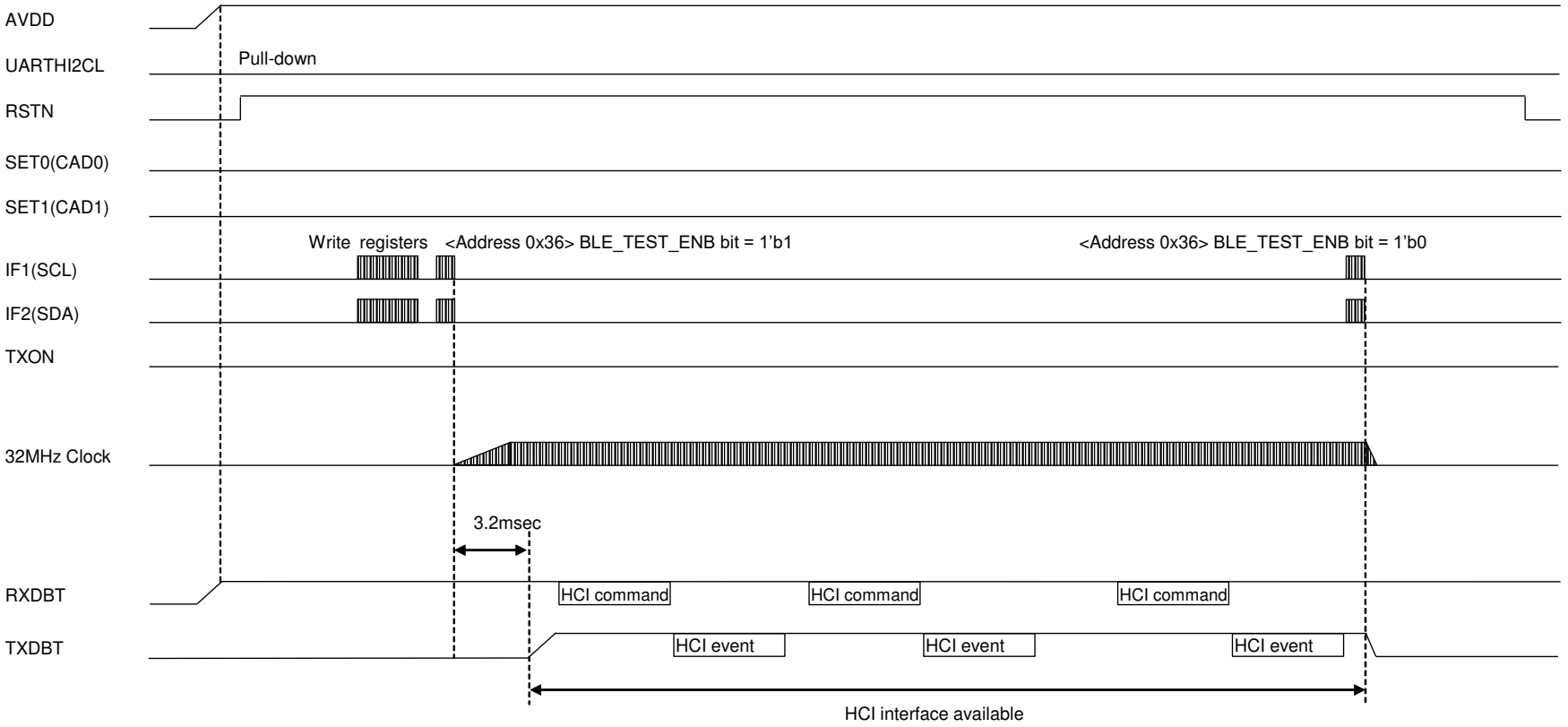


Figure 31. Timing chart of RF-PHY using I²C Interface

18. Register Function

18.1. Register Map

The AK1595 register address consists of 8 bits of data. Data is transferred to or received from the external MCU via the UART or I²C interface described previously.

<Name>	Addr.	R/W Defaults	D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
Reserved	0x00	R/W	FIXED"0"	FIXED"0"	FIXED"0"	FIXED"0"	FIXED"0"	FIXED"0"	FIXED"0"	FIXED"0"
		defaults	0	0	0	0	0	0	0	0
Setting1	0x01	R/W	FIXED"0"	FIXED"0"	ADVCH1[1]	ADVCH1[0]	ADVCH2[1]	ADVCH2[0]	ADVCH3[1]	ADVCH3[0]
		defaults	0	0	0	0	0	1	1	0
Setting2	0x02	R/W	FIXED"0"	FIXED"0"	FIXED"0"	FIXED"0"	FIXED"0"	POWERD[2]	POWERD[1]	POWERD[0]
		defaults	0	0	0	0	0	0	0	0
Setting3	0x03	R/W	FIXED"0"	FIXED"0"	FIXED"0"	TXDATA_LOOP	TXDATA_CW	EVENTNUM[2]	EVENTNUM[1]	EVENTNUM[0]
		defaults	0	0	0	0	0	0	0	0
Setting4	0x04	R/W	ADVDELAY_ENB	ADVINTVL[14]	ADVINTVL[13]	ADVINTVL[12]	ADVINTVL[11]	ADVINTVL[10]	ADVINTVL[9]	ADVINTVL[8]
		defaults	1	0	0	0	0	0	0	0
Setting5	0x05	R/W	ADVINTVL[7]	ADVINTVL[6]	ADVINTVL[5]	ADVINTVL[4]	ADVINTVL[3]	ADVINTVL[2]	ADVINTVL[1]	ADVINTVL[0]
		defaults	0	0	0	0	0	0	0	0
Setting6	0x06	R/W	CRC_ENB	WHITE_ENB	PDULEN[5]	PDULEN[4]	PDULEN[3]	PDULEN[2]	PDULEN[1]	PDULEN[0]
		defaults	1	1	1	0	0	1	1	1
Preamble	0x07	R/W	PRAMBL[7:0]							
		defaults	1	0	1	0	1	0	1	0
Access Address	0x08	R/W	ACCS_ADRS1[7:0]							
		defaults	1	1	0	1	0	1	1	0
	0x09	R/W	ACCS_ADRS2[7:0]							
		defaults	1	0	1	1	1	1	1	0
	0x0A	R/W	ACCS_ADRS3[7:0]							
		defaults	1	0	0	0	1	0	0	1
	0x0B	R/W	ACCS_ADRS4[7:0]							
		defaults	1	0	0	0	1	1	1	0
PDU	0x0C	R/W	PDU1[7:0]							
		defaults	0	0	0	0	0	0	1	0
	0x0D	R/W	PDU2[7:0]							
		defaults	0	0	1	0	0	1	0	1
	0x0E	R/W	PDU3[7:0]							
		defaults	0	0	0	0	0	0	0	0
PDU	0x0F	R/W	PDU4[7:0]							
		Defaults	0	0	0	0	0	0	0	0

<Name>	Addr.	R/W Defaults	D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
	0x10	R/W	PDU5[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x11	R/W	PDU6[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x12	R/W	PDU7[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x13	R/W	PDU8[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x14	R/W	PDU9[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x15	R/W	PDU10[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x16	R/W	PDU11[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x17	R/W	PDU12[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x18	R/W	PDU13[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x19	R/W	PDU14[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x1A	R/W	PDU15[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x1B	R/W	PDU16[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x1C	R/W	PDU17[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x1D	R/W	PDU18[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x1E	R/W	PDU19[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x1F	R/W	PDU20[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x20	R/W	PDU21[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x21	R/W	PDU22[7:0]							
PDU	0x21	Defaults	0	0	0	0	0	0	0	0
	0x22	R/W	PDU23[7:0]							
		Defaults	0	0	0	0	0	0	0	0

<Name>	Addr.	R/W Defaults	D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
	0x23	R/W	PDU24[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x24	R/W	PDU25[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x25	R/W	PDU26[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x26	R/W	PDU27[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x27	R/W	PDU28[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x28	R/W	PDU29[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x29	R/W	PDU30[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x2A	R/W	PDU31[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x2B	R/W	PDU32[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x2C	R/W	PDU33[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x2D	R/W	PDU34[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x2E	R/W	PDU35[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x2F	R/W	PDU36[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x30	R/W	PDU37[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x31	R/W	PDU38[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x32	R/W	PDU39[7:0]							
		Defaults	0	0	0	0	0	0	0	0
CRC	0x33	R/W	CRC1[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x34	R/W	CRC2[7:0]							
		Defaults	0	0	0	0	0	0	0	0
	0x35	R/W	CRC3[7:0]							

<Name>	Addr.	R/W Defaults	D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
		Defaults	0	0	0	0	0	0	0	0
MODE	0x36	R/W	FIXED"0"	FIXED"0"	FIXED"0"	TX_START	FIXED"0"	FIXED"0"	BLE_TEST_ENB	TX_ENB
		Defaults	0	0	0	0	0	0	0	0
SOFT RST	0x3F	W	SOFTRST[7]	SOFTRST[6]	SOFTRST[5]	SOFTRST[4]	SOFTRST[3]	SOFTRST[2]	SOFTRST[1]	SOFTRST[0]
		Defaults	0	0	0	0	0	0	0	0

Note1 Writing to registers with addresses from 0x00 to 0x35 is prohibited during the advertising and intermission states.
Note2 FIXED”0” bits must be written with zeroes. Writing ones to these locations is not supported.

18.1.1. <0x01> Setting1

18.1.1.1. ADVCH1[1:0]

Advertising channel 1st setting

ADVCH1[1]	ADVCH1[0]	Function
0	0	37ch :2402 MHz (default)
0	1	38ch : Center frequency 2426 MHz
1	0	39ch : Center frequency 2480 MHz
1	1	37ch : Center frequency 2402 MHz

18.1.1.2. ADVCH2[1:0]

Advertising channel 2nd setting

ADVCH2[1]	ADVCH2[0]	Function
0	0	37ch : Center frequency 2402 MHz
0	1	38ch : Center frequency 2426 MHz (default)
1	0	39ch : Center frequency 2480 MHz
1	1	No transmission output. (Note 1) (Note 2)

Note1 When <Address 0x01> ADVCH2[1:0] bits = 2'b11, must set <Address 0x03> EVENTNUN[2:0] bits = 3'b001.

Note2 In case of <Address 0x01> ADVCH2[1:0] bits = 2'b11, the AK1595 doesn't output 2nd, 3rd advertising channel output.

18.1.1.3. ADVCH3[1:0]

Advertising channel 3rd setting

ADVCH3[1]	ADVCH3[0]	Function
0	0	37ch : Center frequency 2402 MHz
0	1	38ch : Center frequency 2426 MHz
1	0	39ch : Center Frequency 2480MHz (default)
1	1	No transmission output. (Note1)

Note1 When <Address 0x01> ADVCH3[1:0] bits = 2'b11, must set <Address 0x03> EVENTNUN[2:0] bits = 3'b001.

18.1.2. <0x02> Setting2

18.1.2.1. POWERD[2:0]

TX output power setting

POWERD[2]	POWERD[1]	POWERD[0]	TX Power[dBm] typ.
0	0	0	0(default)
0	0	1	-3
0	1	0	-6
0	1	1	-9
1	0	0	-12
1	0	1	-15
1	1	0	-20
1	1	1	-32

Note The specifications apply within the Recommended Operating Range (supply/operating temperatures) and external matching circuits as shown in the Recommended External Circuits section.

18.1.2.2. <0x03> Setting3TXDATA_LOOP

TXDATA_LOOP	Function
0	Burst Transmission (default)
1	Continuous transmission

Please set {TXDATA_LOOP} =”1b0” except regulatory testing. The AK1595 transmits continuous signal via RFOUT pin. Channel frequencies are set by{ADVCH1[1:0]}. Data whitening is done by based on {ADVCH1[1]} setting when {WHITE_ENB} = “1b1”

18.1.2.3. TXDATA_CW

Modulation mode select

TXDATA_CW	Function
0	GFSK. (default)
1	Continuous Wave

When this register is set to "1", fixed frequencies can be outputted from the RFOUT pin. For the output frequency,
37ch = 2402MHz, 38ch = 2426MHz, 39ch = 2480MHz.

18.1.2.4. EVENTNUM[2:0]

The number of advertising event setting

EVENTNUM[2]	EVENTNUM[1]	EVENTNUM[0]	Function
0	0	0	Repeat Advertising event(default)
0	0	1	1 time Advertising event, Note2
0	1	0	2 times Advertising event
0	1	1	3 times Advertising event
1	0	0	4 times Advertising event
1	0	1	5 times Advertising event
1	1	0	6 times Advertising event
1	1	1	7 times Advertising event

Note 1 When TXON pin is changed from “H” to “L” or <Address 0x36> TX_ENB bit = 1'b0, the AK1595 stops Advertising event output.
Note2 When <Address 0x01> ADVCH2[1:0] bits = 2'b11 or ADVCH3[1:0] bits = 2'b11, the <Address 0x03> EVENTNUM[2:0] must be set 3'b001. Other settings are prohibited.

18.1.3. <0x04~0x05> Setting4, 5

18.1.3.1. ADVDELAY_ENB

AdvDelay Enable

ADVDELAY_ENB	Function
0	AdvDelay disable
1	AdvDelay Enable (default)

18.1.3.2. AVDINTVL[14:0]

Advertising interval setting

ADVINTVL[14:0]	Advertising Interval [msec]
000_0000_0000_0000	20.000(default)
000_0000_0000_0001	20.000
~	~
000_0000_0001_1111	20.000
000_0000_0010_0000	20.000
000 0000_0010_0001	20.625
~	~
000_0000_1001_1111	99.375
000_0000_1010_0000	100.000
000_0000_1010_0001	100.625
~	~
011_1111_1111_1110	10238.750
011_1111_1111_1111	10239.375
100_0000_0000_0000	10240.000
Other setting	10240.000

Note1 <Address 0x04 > ADVDELAY_ENB bit = "1b1", the advertising event time (T_advEvent) meets the Bluetooth Core Specifications.

18.1.4. <0x06> Settings6

18.1.4.1. CRC_ENB

CRC setting

CRC_ENB	Function
0	CRC disable
1	CRC enable

Note 1 Please set {CRC_ENB} =”1b1” except regulatory testing.
Note 2 For details of CRC function, refer to Bluetooth® specification

18.1.4.2. WHITE_ENB

Data Whitening setting

WHITE_ENB	Function
0	Data whitening disable
1	Data whitening enable (default)

Note 1 Please set {CRC_EN} =”0b1” except during regulatory testing.
Note 2 For details of whitening function, refer to Bluetooth® specification

18.1.4.3. PDULEN[5:0]

PDU Length setting

PDULEN[5:0]	PDU Length[octet]
00_0000	Prohibited
00_0001	Prohibited
00_0010	2
00_0011	3
~	~
10_0101	37
10_0110	38
10_0111	39 (default)
Other setting	Prohibited

18.1.5. <0x07~0x35> TX Data

Write TX data to the following addresses.
Preamble (<Address 0x07>)
Access Address (<Address 0x08 to 0x0B>)
PDU (<Address 0x0C to 0x32>),
CRC (<Address 0x33 to 0x35>)

Maximum TX data size is 47 octets.
Unused sectors value must set “0”.

Data is sent in the following format.

Preamble (1 octet)	Access Address (4 octets)	PDU (2~39 octets)	CRC (3 octets)

The output order of the data bits is as follows

<Name>	Addr.	R/W Defaults	D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
-	0x07 to 0x35	R/W	Data[7]	Data[6]	Data[5]	Data[4]	Data[3]	Data[2]	Data[1]	Data[0]
		Defaults								

Data[0] → Data[1] → Data[2] → Data[3] → Data[4] → Data[5] → Data[6] → Data[7]

18.1.5.1. <0x07> PRAMBL[7:0]

Preamble setting. Please set default values 0xAA except regulatory testing.

18.1.5.2. <0x08 to 0x0B> ACCS_ADRS1[7:0]~ACCS_ADRS4[7:0]

Access Address setting. Please set following default values.
<Address 0x08> ACCS_ADRS1[7:0] bits = 8'hD6
<Address 0x09> ACCS_ADRS2[7:0] bits = 8'hBE
<Address 0x0A> ACCS_ADRS3[7:0] bits = 8'h89
<Address 0x0B> ACCS_ADRS4[7:0] bits = 8'h8E

18.1.5.3. <0x0C to 0x32> PDU1[7:0]~PDU39[7:0]

The PDU setting. Please set the send data that complies with BLE.

18.1.5.4. <0x33 to 0x35> CRC1[7:0]~CRC3[7:0]

The CRC data setting.
When CRC_ENB bit = “1”, CRC(0x33 to 0x35) is not need to be set.
When CRC_ENB bit = “0”, please is set CRC value that complies with BLE.

18.1.6. <0x36> MODE

18.1.6.1. TX_START

Check AK1595 state (read-only)

TX_START	Function
0	The AK1595 state is either full power-down, sleep, or standby(default).
1	The AK1595 state is either advertising or intermission

Note1 TX_START bit is read-only.

18.1.6.2. BLE_TEST_ENB, TX_ENB

BLE Test mode enable, RF transmission enable

BLE_TEST_ENB	TX_ENB	Function
0	1	Start RF transmission. This is the same operation mode as when TXON pin is set to "H".
1	0	The unit enters the Bluetooth certification test mode. This mode is used to perform a certification test. Refer to 17 Bluetooth Test Specification.
0	0	Stop RF transmission when TX_ENB bit set is set “1” to “0”. Exit Bluetooth certification test mode when TX_TEXT_ENB bit is set “1” to “0”.
1	1	Prohibited

Note1 Do not change TXON pin state and TX_ENB bit at the same time.
Note2 When controlling start and stop RF transmisshion with TX_ENB bit , set TXON pin = “Low”

18.1.7. <0x3F> SOFTRST

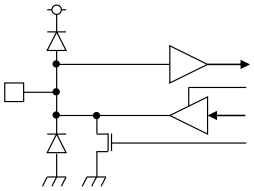
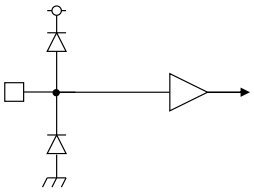
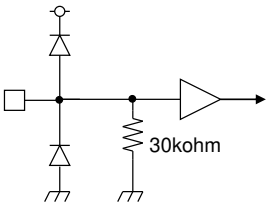
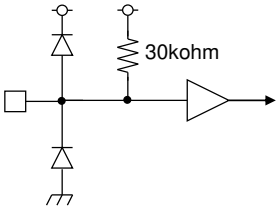
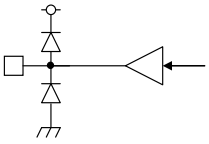
18.1.7.1. SOFTRST[7:0]

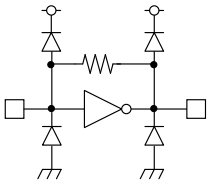
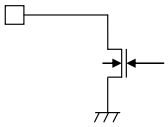
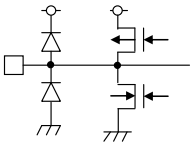
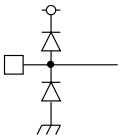
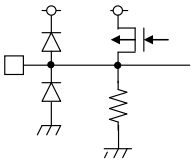
Software reset

SOFTRST[7:0]	Function
0xAA	Execute a software reset. This is to initialize the digital block. To set all AK1595 setting again. <Address 0x3F> SOFTRST[7:0] bits automatically turns 0x00 after the software reset is completed.
Other than above	If a value other than the above is written, a software reset is not executed.

Note1: Default is 0x00. This register is write-only.
Note2: The AK1595 doesn't generate an acknowledge when a software reset is executed by the I^2C interface. Even though the AK1595 doesn't generate an acknowledge in this state, it is still necessary to provide all nine SCL clock cycles as usual (eight cycles for data + one cycle for the acknowledge).
Note3: The AK1595 doesn't output an event when a software reset is executed via the UART interface.
Note4: In order to ensure the AK1595 software reset, TXON pin must be set low during the reset period.

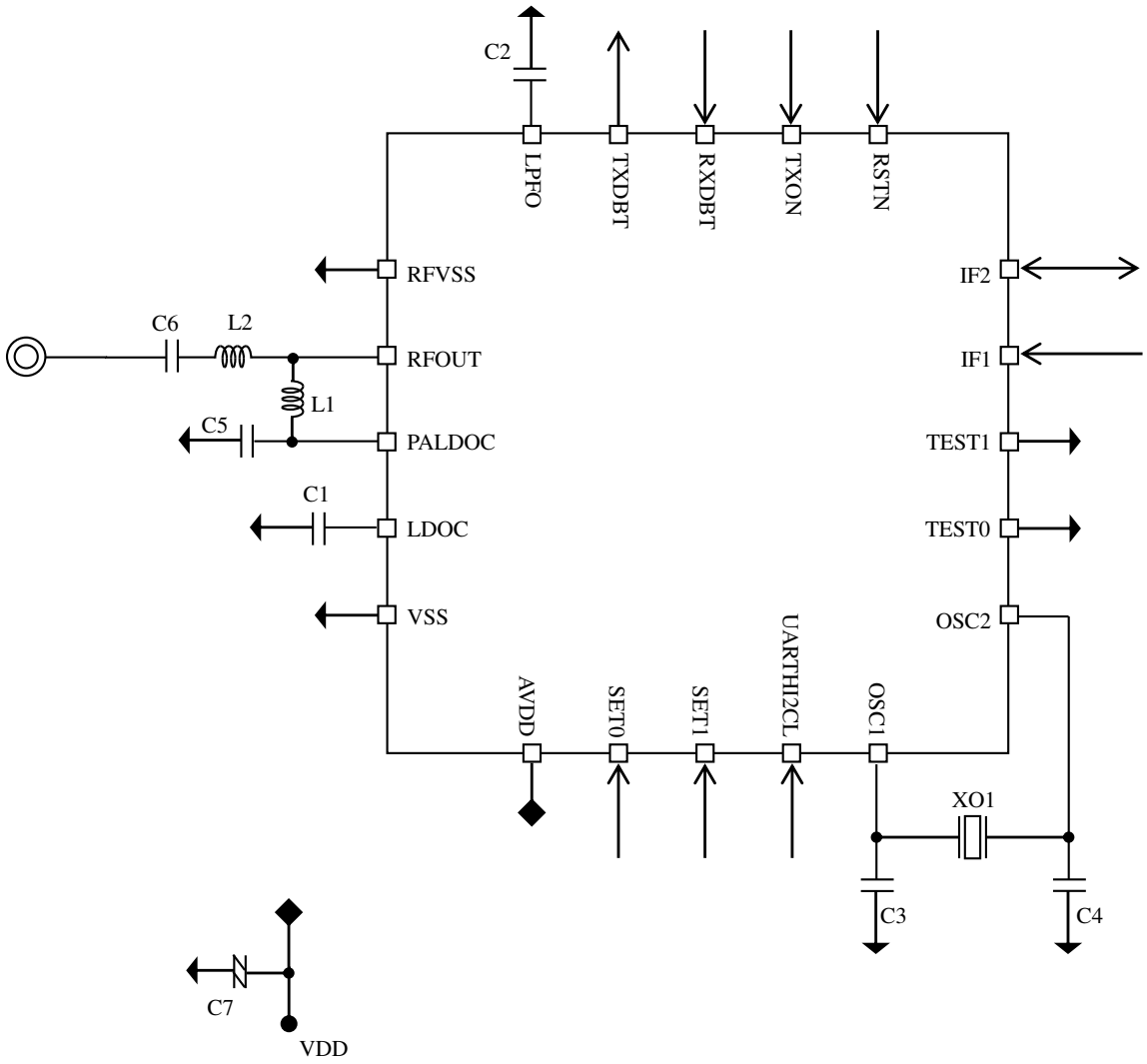
19. IC Interface Circuits

Pin Number	Pin Name	I/O	Function
10	IF2	IO	**Digital input/output pin** 
4	UARTHI2CL	I	**Digital input pin** 
2	SET0	I	
3	SET1	I	
9	IF1	I	
11	RSTN	I	
12	TXON	I	
7	TEST0	I	**Digital input pin** 
8	TEST1	I	
13	RXDBT	I	**Digital input pin** 
14	TXDBT	O	**Digital output pin** 

Pin Number	Pin Name	I/O	Function
5	OSC1	I	**Analog input pin** 
6	OSC2	O	
17	RFOUT	O	**Analog output pin** 
18	PALDOC	O	**Analog output pin** 
15	LPFO	IO	**Analog input/output pins** 
19	LDOC	O	**Analog output pin** 

20. Recommended External Circuits

20.1. Recommended External Circuits



Note1 RF specification, number of components and values may change depending upon the RF matching network and PCB design.

Figure 32. Recommended external circuits

20.2. Parts list

Number	Value	Part
C1	100nF	
C2	680pF	
C3	6.8pF	
C4	6.8pF	
C5	1nF	
C6	1.2pF	
C7	0.1uF	
L1	8.2nH	
L2	6.8nH	
XO1	32MHz(6pF)	EPSON, FA-128, Q22FA12800517xx

Note1 RF specification, number of components and values may change depending upon the RF matching network and PCB design.

21. Package

21.1. Outline Dimensions

20-pin HWQFN(3.0mm x 3.0mm x 0.75mm, 0.4mm pitch)

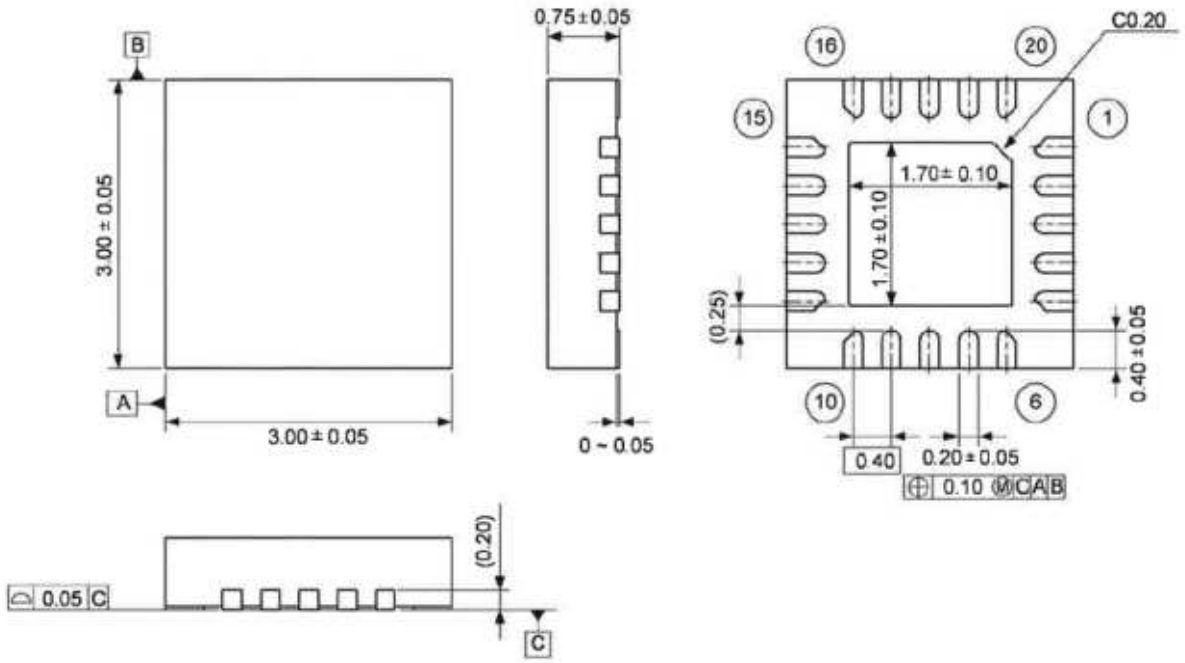


Figure 33. Package outer dimension

Note1 Leave the exposed pad on the bottom surface of the package unconnected.

21.2. Marking

a. Style : HWQFN
b. Number of pins : 20pins
c. A1 pin marking : Circle mark
d. Product number : 1595
e. Date code : XXXX (4 digits)

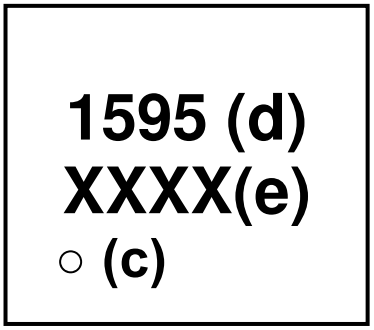


Figure 34. Marking

22. Ordering Guide

-AK1595 20-pin HWQFN (3.0mm x 3.0mm x 0.75mm, 0.4mm pitch)

23. Revision history

Date (Y/M/D)	Revision	Reason	Page	Contents
20/5/20	00	First edition		

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