AsahiKASEI

AK2363

Radio Signaling LSI

Features

- DTMF Receiver including an AGC circuit
- Built-in MSK modem allowing selection from 1200 and 2400 bit/s
- Programmable modem frame detection pattern
- Built-in 3.6864MHz oscillator circuit
- Support of external clocks with frequencies twice, three times, and four times higher than 3.6864MHz
- Operating voltage range: 2.6V to 3.7V
- Operating temperature range: -40°C to +85°C
- Package: 24-pin QFNJ (4.0 x 4.0 x 0.75mm, 0.5mm pitch)

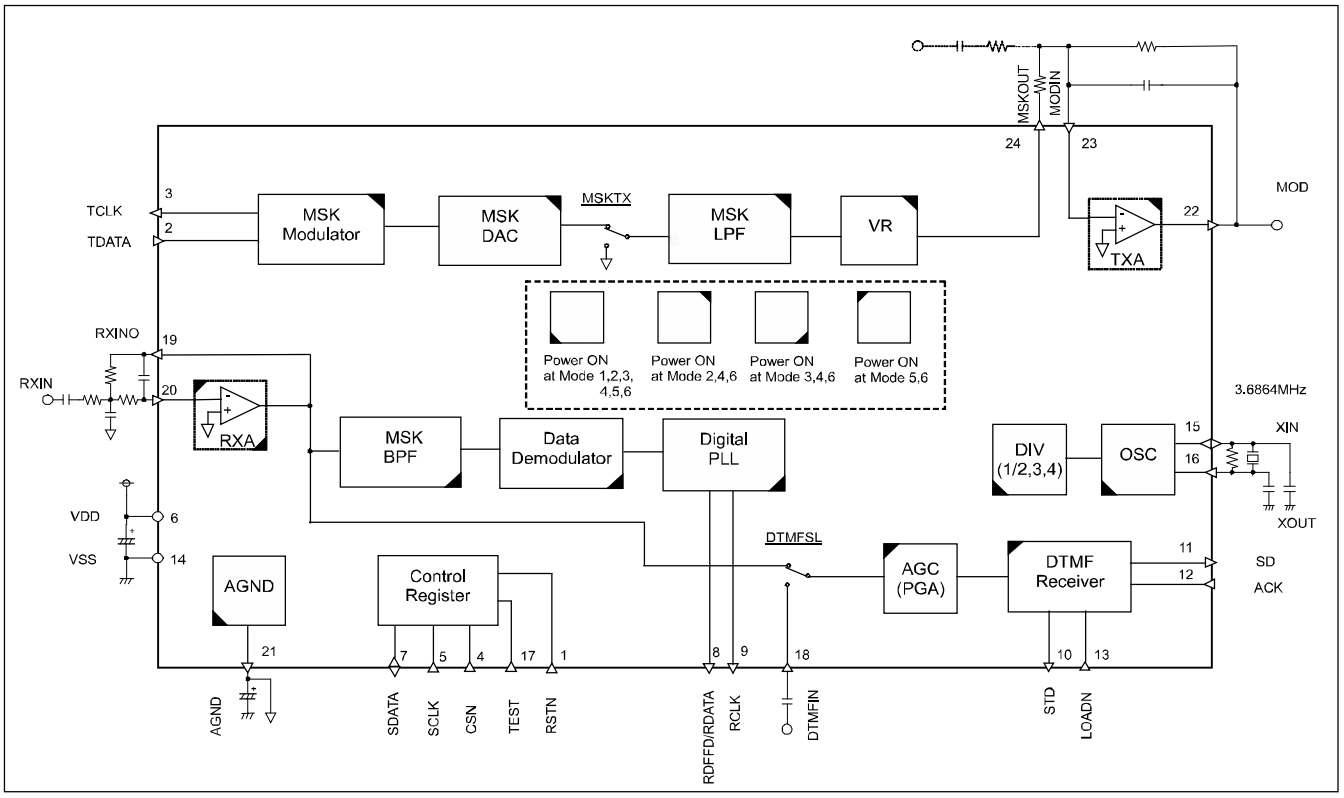
Overview

The AK2363 is a radio signaling LSI device into which an MSK modem and a DTMF Receiver are integrated on a single chip.
The MSK modem supports 1200 and 2400 bit/s, and the demodulator has a 16-bit frame pattern detection function that allows any settings. When the signal-to-noise (S/N) ratio is 12dB, the BER characteristic at 1200 bit/s is 5.0E-06, and the BER characteristic at 2400 bit/s is 1.0E-04.
The DTMF Receiver operates in two modes: Normal mode (AGD Disable) indicating input signal detection levels ranging from -27dBx to 0dBx and high sensitivity mode (AGC Enable) in which the receiver operates at –40dBx to 0dBx.
In addition to a fundamental frequency of 3.686MHz, the oscillator circuit supports external clock input with frequencies of 7.3728MHz (twice higher than 3.6864MHz), 11.0592MHz (three times higher than 3.6864MHz), and 14.7456MHz (four times higher than 3.6864MHz).
The internal operation is controlled by the three-wire serial method in which serial input data (SDATA) consisting of a 1-bit instruction, a 4-bit address, and 8-bit data is set in synchronization with the CSN and SCLK signals.
The 24-pin QFNJ package (4.0mm × 4.0mm) is employed to realize compact, high-density packaging.

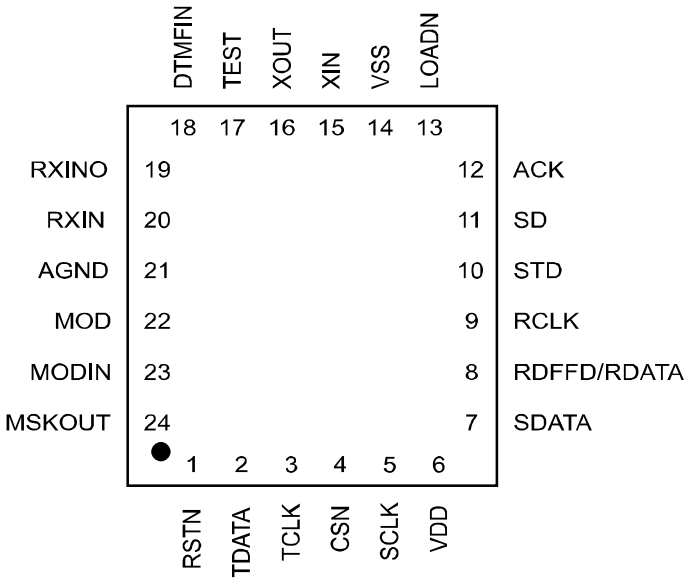
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Block Diagram



Pin Assignments



Block Functions

Block	Function
MSK Modulator	This circuit generates an MSK signal according to the logic of a digital signal input from the TDATA pin.
MSK DAC	DAC that converts data generated by the MSK Modulator into an analog signal.
MSK LPF	This circuit is a low-pass filter for eliminating the clock component included in the MSK DAC signal. A switch for changing between the mute and active states is provided between this filter and VR and is set by setting register MSKTX.
VR	This control adjusts the output level of the transmit MSK signal. Setting register: VR[4:0] Adjustment range: -6.0dB to +6.0dB in 0.5dB steps
TXA	Operational amplifier for gain adjustment of the transmit MSK signal and for forming a smoothing filter for removing noise components included in the output signal. Use an external resistor and capacitor to set the gain to 0dB and the cut-off frequency to around 13kHz.
RXA	Operational amplifier for gain adjustment of the receive demodulation signal and for forming a filter for preventing aliasing noise in the SCF circuit in the subsequent stage. Use external resistors and capacitors to set the gain to 20dB or less and the cut-off frequency to around 40kHz.
MSK BPF	Band-pass filter to eliminate out-of-band components included in the receive MSK signal.
Data Demodulator	This circuit demodulates the MSK signal and generates data.
Digital PLL	This circuit detects the carrier signal from the MSK signal and regenerates a clock signal.
AGC(PGA)	AGC (Auto Gain Control) circuit for adjusting the input level of the DTMF signal automatically. Setting register: AGCSW or AGCSW. When disabled, this circuit functions as a PGA (Programmable Gain Amp) circuit. Setting register: PGA[1:0] Adjustment range: 0dB to +12dB in 4dB steps A switch for changing the input is provided between this circuit and RXA and is set by setting register DTMFSL.
DTMF Receiver	DTMF signal detection circuit. It decodes the input signal and outputs 4-bit code.
OSC	This circuit generates a 3.6864MHz reference clock signal from an external crystal oscillator and resistor.
DIV (1/2,1/3,1/4)	When a signal of which frequency is twice, three times, or four times higher than 3.6864MHz is input from the outside, this circuit divides the signal frequency by two, three, or four. Setting register: MCKSL[1:0]
AGND	This circuit generates the reference voltage (1/2VDD) for internal analog signals.
Control Register	Control registers set the switches and control in the IC according to the serial input data consisting of a 1-bit instruction, a 4-bit address, and 8-bit data. A built-in data buffer is provided to hold 8-bit MSK receive data for easier interfacing with the CPU. At power-on, a system reset is caused by the RSTN pin. A soft reset is set by the SRST register. (Refer to the description of the registers.)

Pin Functions

Pin No.	Pin name	Pin type	Pin status at power-down	Function
1	RSTN	DI	Z	Reset pin
2	TDATA	DI	Z	MSK signal transmit data input pin Data is input from this pin on the rising edge of the clock signal on the TCLK pin.
3	TCLK	DO	L	MSK signal transmit clock output pin
4	CSN	DI	Z	Chip select input pin for serial data
5	SCLK	DI	Z	Clock input pin for serial data
6	VDD	PWR	-	VDD power supply pin Connect this pin to a power supply ranging from 2.6V to 3.7V with less noise. Connect a bypass capacitor of 0.1μF or higher between this pin and the VSS pin.
7	SDATA	DB	Z	Serial data I/O pin
8	RDFFD/ RDATA	DO	L	MSK signal receive flag/frame detection signal/RDATA signal output pin Two types of information is output depending on the FSL register status. If FSL is set to 1 to set the MSK signal receive flag output mode (RDF), this pin is set to the low output level when 8 bits of the MSK receive signal have been written to the receive data register. If FSL is set to 0 to set the frame detection signal output mode (FD), a low-level pulse is output on this pin when a frame pattern is detected. If setting register MSKRCLK is set to 1, the RDATA signal is output.
9	RCLK	DO	L	MSK signal receive clock output pin
10	STD	DO	L	Steering delay output pin for DTMF signal detection This pin goes high when internal data has been updated after completion of DTMF RX signal decoding.
11	SD	DO	L	DTMF signal receive data output pin If the LOADN pin input is low, the result of DTMF RX signal decoding is output serially starting from the MSB in synchronization with the falling edge of the ACK pin input. If the LOADN pin input is high, the high level is output.
12	ACK	DI	Z	Clock input pin for DTMF signal receive data read
13	LOADN	DI	Z	Enable signal input pin for DTMF signal receive data read If the low level is input, DTMF signal receive data can be read.

Pin No.	Pin name	Pin type	Pin status at power-down	Function
14	VSS	PWR	-	VSS power supply pin Always apply 0V.
15	XIN	DI/AO	*4)	Pin for connecting a crystal oscillator A reference clock used within this IC is generated by connecting a 3.6864MHz oscillator between this pin and the adjacent XOUT pin. For detailed information about the connection method and the method for supplying an external clock, refer to "Recommended External Circuit Examples."
16	XOUT	AI	*4)	Pin for connecting a crystal oscillator
17	TEST	DI	Z	Test output pin This pin is used as a test pin before shipment. Normally, connect this pin to VSS.
18	DTMFIN	AI	Z	DTMF signal input pin
19	RXINO	AO	Z	RXA amplifier output pin *1)
20	RXIN	AI	Z	Demodulated receive signal input pin Inverted input pin of the RXA amplifier. This pin, with resistors and capacitors externally connected, forms a pre-filter.
21	AGND	AO	*3)	Analog ground output pin Connect a 0.1μF capacitor between this pin and the VSS pin to stabilize the analog ground level.
22	MOD	AO	Z	Modulated transmit signal output pin *2)
23	MODIN	AI	Z	Modulated transmit signal input pin Inverted input pin of the TXA amplifier. This pin, with a resistor and capacitor externally connected, forms a smoothing filter.
24	MSKOUT	AO	Z	MSK signal level output pin *1)

Note **A**: Analog, **D**: Digital, **PWR**: Power, **I**: Input, **O**: Output, **B**: Bidirectional, **Z**: High-Z, **L**: Low

*1) Output load requirement: Load impedance > 30kΩ, load capacitance < 15pF
*2) Output load requirement: Load impedance > 10kΩ, load capacitance < 50pF

*3) AGND level
*4) The XIN pin output level is determined by the XOUT pin input level.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Power supply voltage	VDD	-0.3	4.6	V
Ground level	VSS	0	0	V
Input voltage	V_{IN}	-0.3	VDD+0.3	V
Input current (except power pin)	I_{IN}	-10	+10	mA
Storage temperature	T_{stg}	-55	130	°C

Note All voltages are relative to the VSS pin.

Caution If the device is used in conditions exceeding these values, the device may be destroyed. Normal operations are not guaranteed in such extreme conditions.

Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating temperature	Ta		-40		85	°C
Operating power supply voltage	VDD		2.6	3.0	3.7	V
Analog reference voltage	AGND			1/2VDD		V

Note All voltages are relative to the VSS pin.

Digital DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}	SCLK, SDATA, CSN, LOADN, ACK, TDATA, RSTN,	0.8VDD			V
Low level input voltage	V_{IL}	SCLK, SDATA, CSN, LOADN, ACK, TDATA, RSTN,			0.2VDD	V
High level input current	I_{IH}	V_{IH}=VDD SCLK, SDATA, CSN, LOADN, ACK, TDATA, RSTN,			10	μA
Low level input current	I_{IL}	V_{IL}=0V SCLK, SDATA, CSN, LOADN, ACK, TDATA, RSTN,	-10			μA
High level output voltage	V_{OH}	I_{OH}=+0.2mA SDATA, RDFFD/RDATA, RCLK, STD, SD, TCLK	VDD-0.4		VDD	V
Low level output voltage	V_{OL}	I_{OL}=-0.4mA SDATA, RDFFD/RDATA, RCLK, STD, SD, TCLK	0.0		0.4	V

Clock Input Characteristics

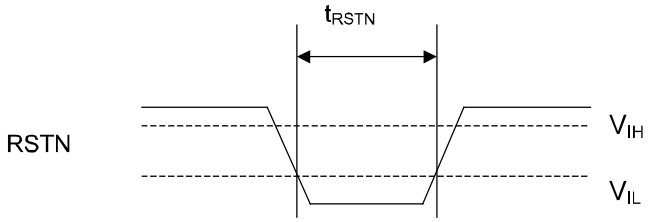
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Clock frequency	MCK0	XIN,XOUT		3.6864		MHz	
	MCK1,2	XIN		7.3728 11.0592 14.7456		MHz	*1), *2)
High level input voltage	V_{MCK1_IH}	XIN	1.5			V	*1)
Low level input voltage	V_{MCK1_IL}	XIN			0.4	V	*1)
Input amplitude	V_{MCK2}	XIN	0.2		1.0	V_{PP}	*2)

*1) These values apply when the clock signal is input on the XIN pin directly. For details, refer to 6), "Oscillator circuit", in "Recommended External Circuit Examples".
*2) These values apply when the clock signal is input on the XIN pin via DC cut. For details, refer to 6), "Oscillator circuit", in "Recommended External Circuit Examples".

System Reset

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Hardware reset signal input width	t_{RSTN}	RSTN pin	1			us	*1)
Software reset		SRST register					*2)

*1) After power-on and passed 35ms or longer, be sure to perform a hardware reset operation (register initialization). The system is reset by a low pulse input of 1μs (min.) and enters the normal operation state. At this moment, the digital (DI) pins are set as follows: RSTN pin to high, TDATA pin to low, CSN pin to high, SCLK pin to low, ACK pin to high, LOADN pin to high, TEST pin to VSS.



*2) When data 0xAA:10101010 is written to the SRST[8:0] register, a software reset is performed. This setting initializes the registers and the operation mode is set to mode 1 (standby). For details, refer to "Register Functions".

Current Consumption

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption	IDD0	Mode 0 OSC: OFF, DTMF Receiver: OFF, MSK_Tx: OFF, MSK_Rx: OFF		0.1	0.2	mA
	IDD1	Mode 1 OSC: ON, DTMF Receiver: OFF, MSK_Tx: OFF, MSK_Rx: OFF		0.6	1.0	
	IDD2	Mode 2 OSC: ON, DTMF Receiver: OFF, MSK_Tx: ON, MSK_Rx: OFF		1.3	2.1	
	IDD3	Mode 3 OSC: ON, DTMF Receiver: OFF, MSK_Tx: OFF, MSK_Rx: ON		1.1	1.8	
	IDD4	Mode 4 OSC: ON, DTMF Receiver: OFF, MSK_Tx: ON, MSK_Rx: ON		1.7	2.7	
	IDD5	Mode 5 OSC: ON, DTMF Receiver: ON, MSK_Tx: OFF, MSK_Rx: OFF		1.3	2.2	
	IDD6	Mode 6 OSC: ON, DTMF Receiver: ON, MSK_Tx: ON, MSK_Rx: ON		2.4	3.8	

Analog Characteristics

Unless otherwise specified, the following apply: MCLK = 3.6864MHz, f = 1kHz, VR = 0dB
The external circuit constants are set based on the recommended external circuit examples on pages 29 to 31.
dBx is a standardized notation to match the operating voltage and is defined by equation 0dBx = -5 + 20log(VDD/2)dBm.

0dBm = 0.775Vrms

1) MSK modem characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit	Remarks
TX signal	@MOD 1.2kHz signal output	-12	-11	-10	dBx	
TX signal distortion	@MOD 1.2kHz signal output			-32	dB	
RX signal	@RXINO 1.2kHz signal output	-17	-11	-1	dBx	
VR gain deviation	@MSKOUT -6.0dB to +6.0dB, in 0.5dB steps Linearity	-0.5		0.5	dB	

2) DTMF Receiver characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit	Remarks
Tone input level accept (for each tone of composite signal)	@RXINO, AGC Disable, PGA=0dB *2), *3), *6)	-27		0	dBx	
	@RXINO, AGC Enable, *2), *3), *6)	-40		0	dBx	
	@DTMFIN, AGC Disable, PGA=0dB *2), *3), *6)	-27		-2	dBx	
	@DTMFIN, AGC Enable, *2), *3), *6)	-40		-2	dBx	
Twist accept	*3), *6), *8)		±10		dB	
Frequency deviation accept	*2), *6)			±1.5% ±2Hz		
Frequency deviation reject	*2), *6)	±3.5%				
Third tone tolerance	*1), *2), *6), *7)		-16		dB	
Noise tolerance	*1), *2), *4), *6), *7)		-12		dB	
Dial tone tolerance	*1), *2), *5), *6), *7)		+17		dB	
PGA gain deviation	0dB to +12dB, in 4dB steps	-0.5		+0.5	dB	

*1) Refers to nominal DTMF frequencies.
*2) High/low tones have the same amplitudes.
*3) High/low tones are deviated by ±1.5%±2Hz.
*4) Bandwidth is limited from 0 to 3kHz Gaussian noise.
*5) Dialtones of 350Hz and 440Hz ±2%
*6) Error rates better than 1 in 10000
*7) Reference DTMF signal input level is -22dBx or less.
*8) Twist = high tone/low tone

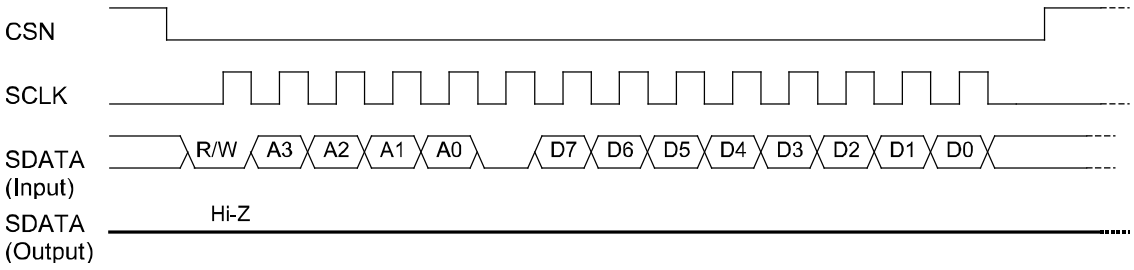
Digital AC Timing

1) Serial interface timing

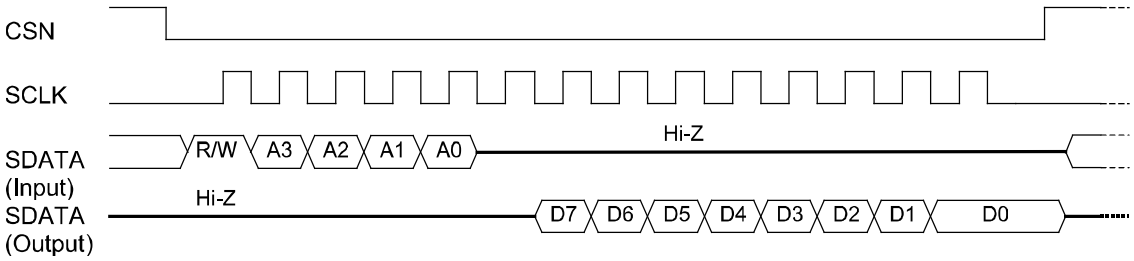
The AK2363 writes and reads data via the three-wire synchronous serial interface by means of CSN, SCLK, and SDATA.

SDATA (serial data) consists of a write/read identification bit (R/W), a register address (starting from the MSB, A3 to A0), and control data (starting from the MSB, D7 to D0).

Write (WRITE instruction)



Read (READ instruction)



R/W: This bit indicates whether an access to a register is a write access or read access. If this bit is **Low**, a **write** is performed; if the bit is **High**, a **read** is performed.

A3 to A0: These bits indicate the address of the register to be accessed.

D7 to D0: Data to be written to or read from the register.

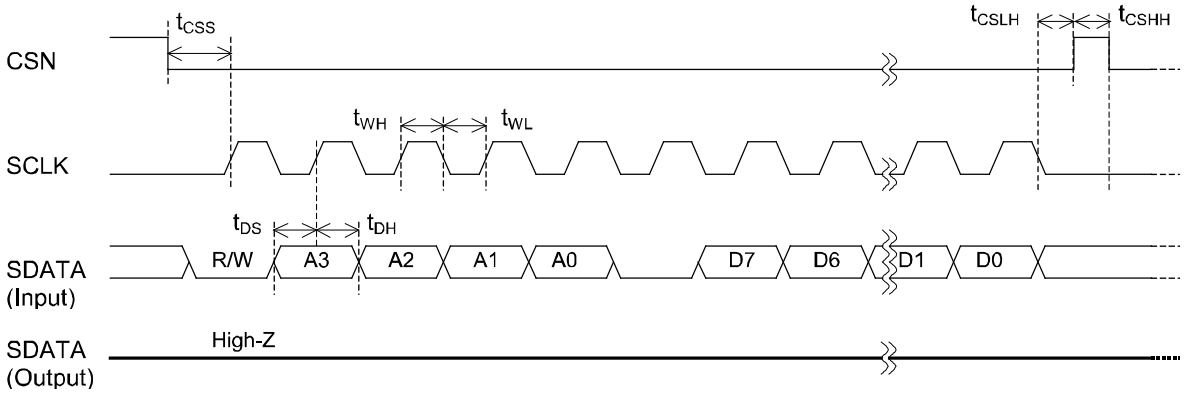
<1> CSN (chip select) is normally set to the high level.
When CSN is set to the low level, the serial interface becomes active.

<2> When a write operation is performed, an identification bit, an address, and data are input from SDATA in synchronization with the rising edges of 14 SCLK clock pulses while CSN is low.
During the time between address A0 and data D7, SDATA must be held low.
When a read operation is performed, an identification bit and an address are input from SDATA in synchronization with the rising edges of the first five clock pulses of SCLK, and data at a specified address is output in synchronization with the falling edges of the following nine clock pulses while CSN is low.
Note that data between address A0 and data D7 is undefined.
During the data output period in the latter nine clock pulses of SCLK, the input to SDATA must be Hi-Z.

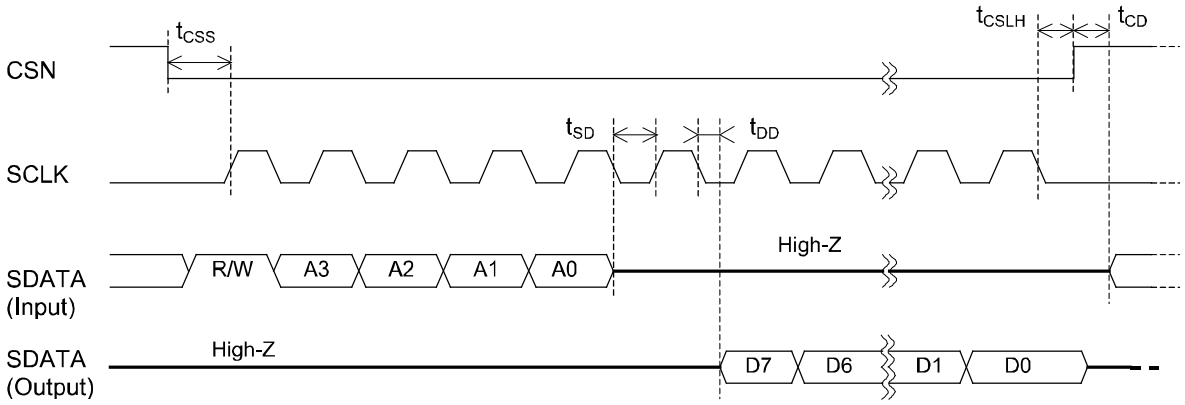
<3> Write and read settings are made on the assumption that 14 clock pulses are input from SCLK while CSN is low.
Note that if clock pulses more than or less than 14 clock pulses are input, data cannot be set correctly.

2) Detail timing

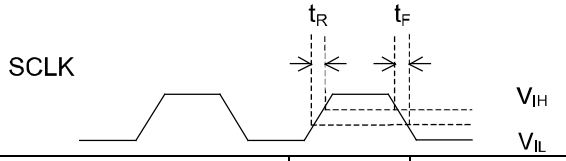
WRITE instruction



READ instruction



Rising and falling times

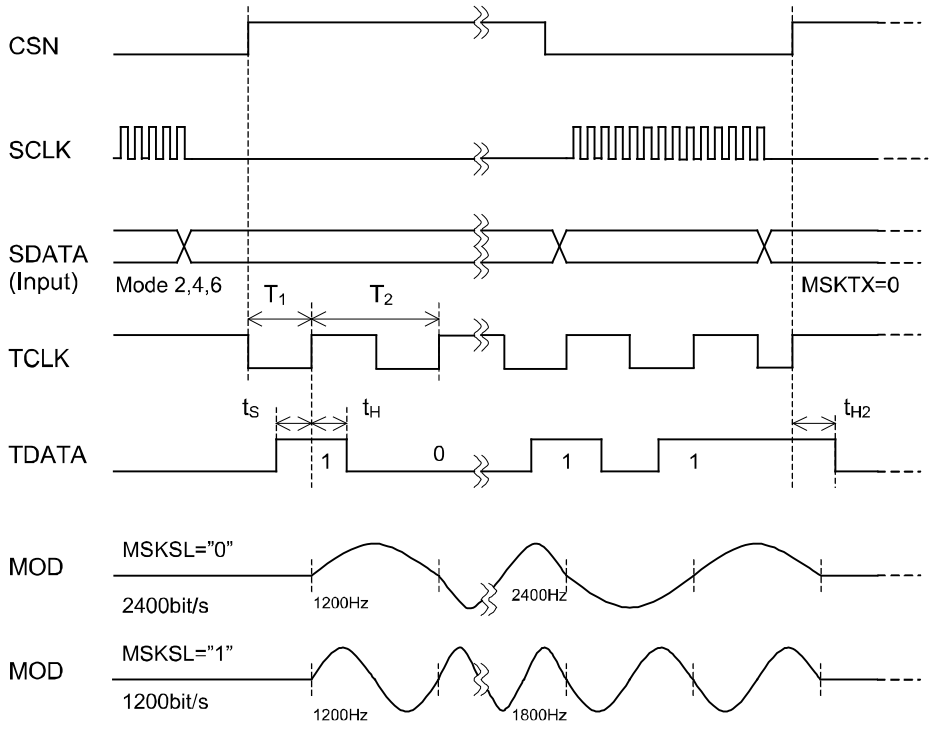


Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CSN setup time	t_{CSS}		100			ns
SDATA setup time	t_{DS}		100			ns
SDATA hold time	t_{DH}		100			ns
SCLK high time	t_{WH}		500			ns
SCLK low time	t_{WL}		500			ns
CSN low hold time	t_{CSLH}		100			ns
CSN high hold time	t_{CSHH}		100			ns
SDATA Hi-Z setup time	t_{SD}		500			ns
SCLK to SDATA output delay time	t_{DD}	Loaded by 20pF			400	ns
CSN to SDATA input delay time	t_{CD}	Loaded by 20pF	200			ns
SCLK rising time	t_R				100	ns
SCLK falling time	t_F				100	ns

Note Digital input timing measurements are made at 0.5VDD for rising edges and falling edges.
Digital output timing measurements are made at 0.5VDD for rising edges and falling edges.

3) MSK Modulator timing

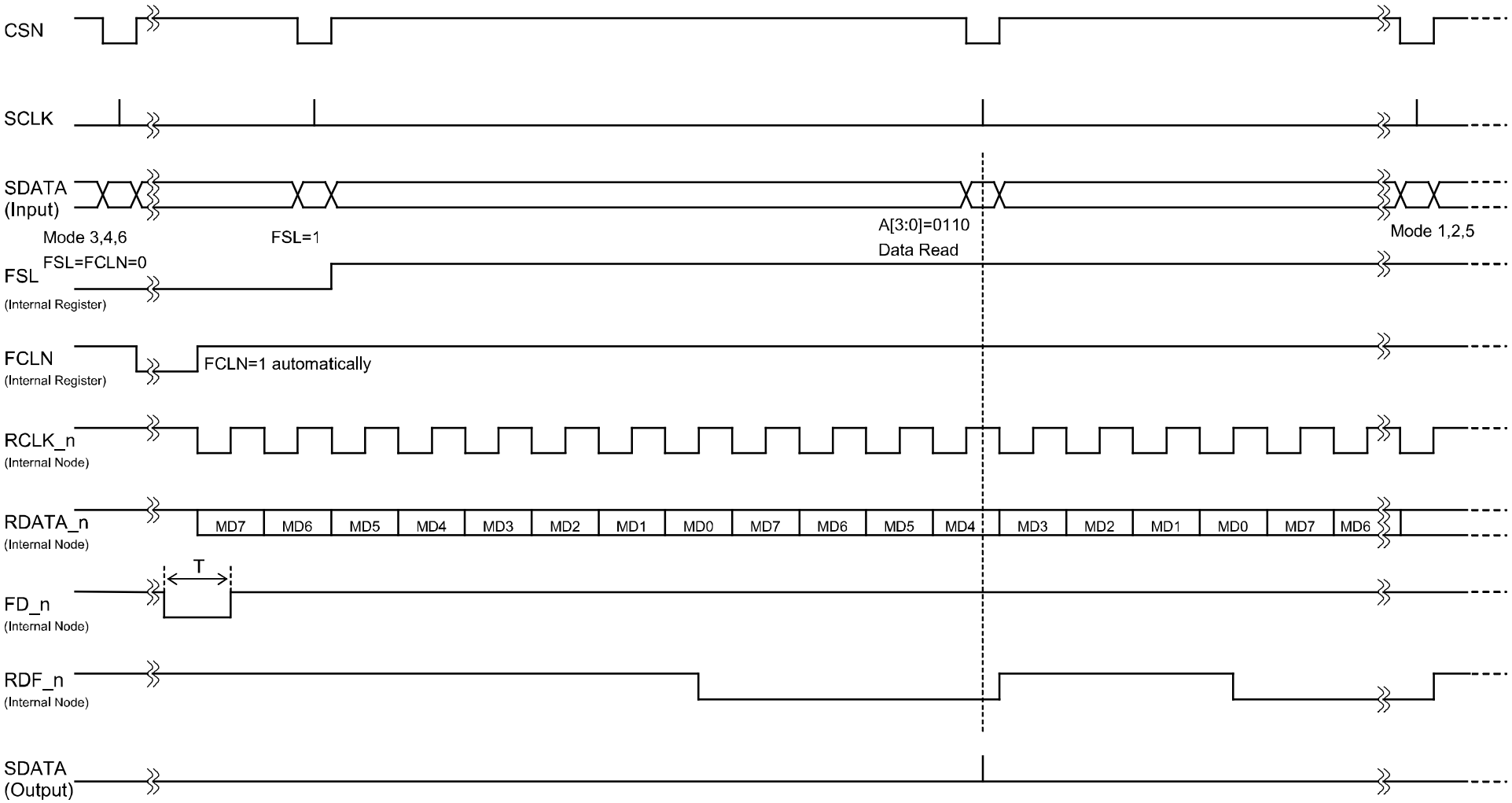
Parameter	Symbol	Min.	Typ.	Max.	Unit
CSN rising to TCLK falling MSKSL = 0 MSKSL = 1	T_1		 208 417		μs
TCLK period MSKSL = 0 MSKSL = 1	T_2		 417 833		μs
TDATA set up time TDATA hold time TDATA hold time2	t_S t_H t_{H2}	1 1 2			μs



Note Register setting is synchronized with the rising edge on the CSN pin.
When the data is maintained for 2μs or longer specified by TDATA hold time2 (t_{H2}), the signal from MOD pin is ended in zero cross point.

4) MSK Demodulator timing

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
RCLK period and FD pulse width MSKSL = 0 MSKSL = 1	T			 417 833		μs

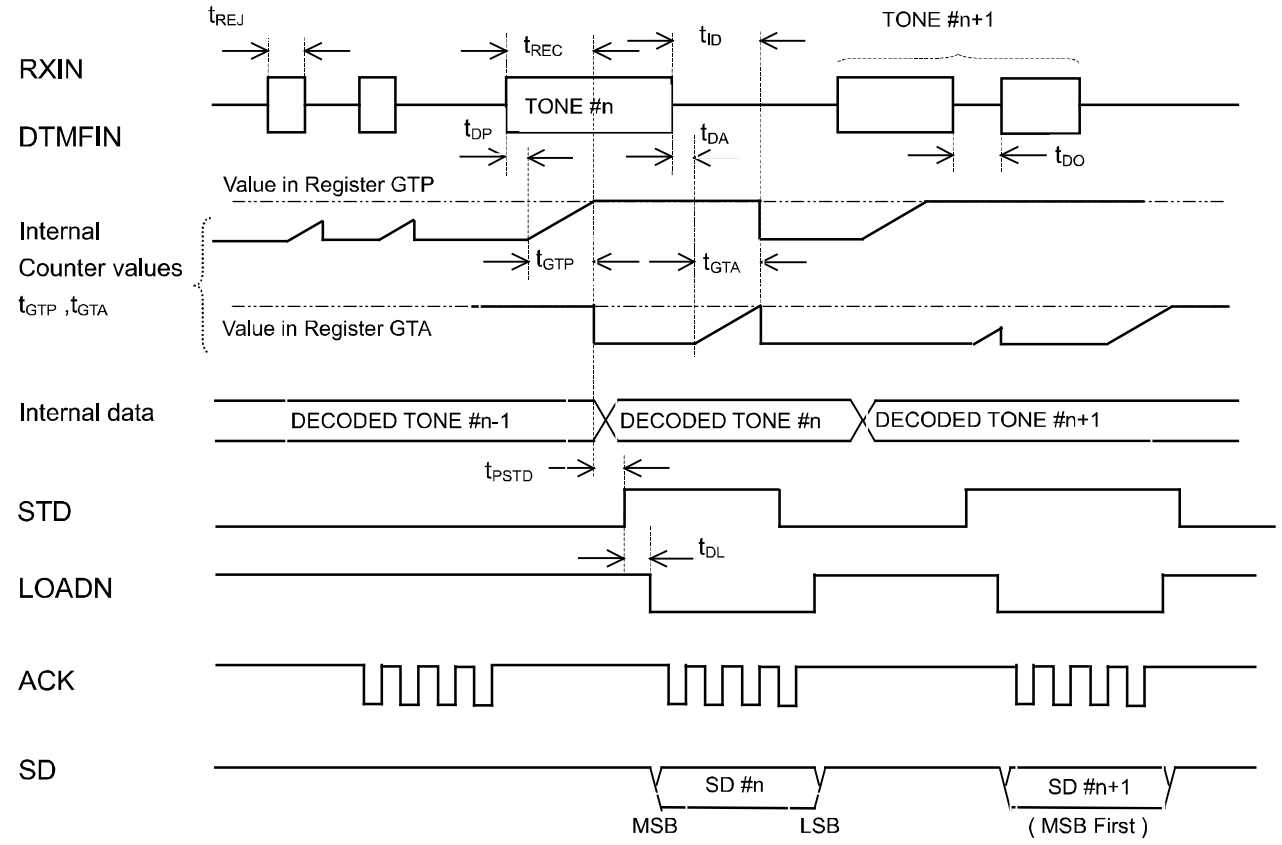

CSN
SCLK
SDATA
(Input)
Mode 3,4,6
FSL=FCLN=0
FSL=1
A[3:0]=0110
Data Read
Mode 1,2,5
FSL
(Internal Register)
FCLN
(Internal Register)
FCLN=1 automatically
RCLK_n
(Internal Node)
RDATA_n
(Internal Node)
MD7 MD6 MD5 MD4 MD3 MD2 MD1 MD0 MD7 MD6 MD5 MD4 MD3 MD2 MD1 MD0 MD7 MD6
T
FD_n
(Internal Node)
RDF_n
(Internal Node)
SDATA
(Output)

5) DTMF Receiver timing

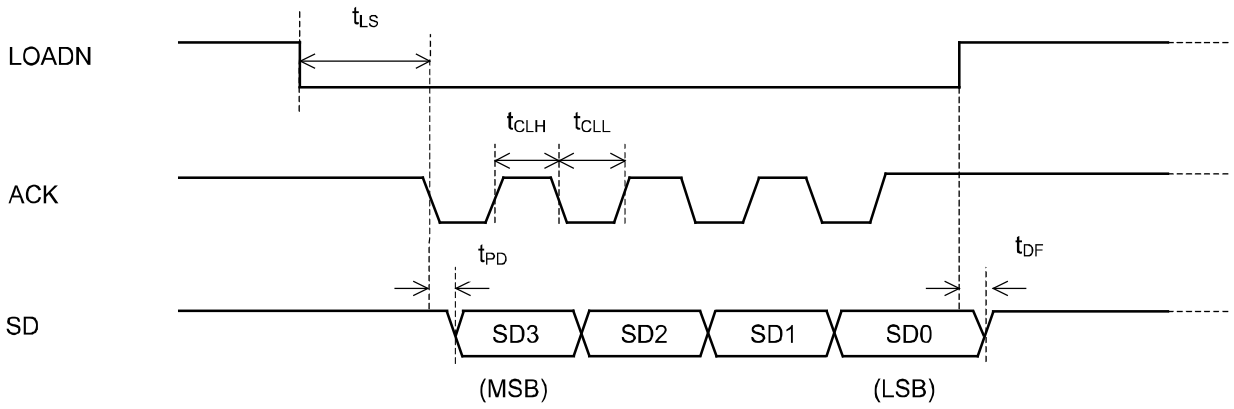
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Tone present detection time(reference value)	t_{DP}	AGC Disable	5	11	16.8	ms
		AGC Enable	5	20	44	ms
Tone absent detection time (reference value)	t_{DA}		0.5	4	8.5	ms
Tone duration accept time *1)	t_{REC}	AGC Disable GTP[3:0]=0100	54.5			ms
		AGC Enable GTP[3:0]=0001	54			ms
Tone duration reject time*1)	t_{REJ}				32.2	ms
Interdigit pause accept time *1)	t_{ID}		28.4			ms
Interdigit pause reject time *1)	t_{DO}				1.6	ms
GT (internal counter) to STD propagation delay	t_{PSTD}			21.7		μs
STD rising to LOADN falling time	t_{DL}		100			ns
ACK low period	t_{CLL}		500			ns
ACK high period	t_{CLH}		500			ns
LOADN setup time	t_{LS}		500			ns
SD output delay time	t_{PD}	Loaded by 20pF			200	ns
SD output disable time	t_{DF}	Loaded by 20pF			200	ns
ACK rising time	t_{CLR}				100	ns
ACK falling time	t_{CLF}				100	ns

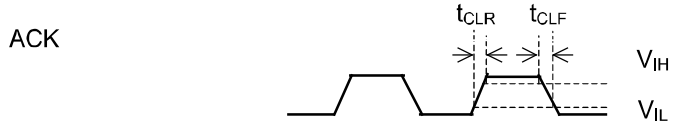
*1) The data shows the values when registers GTPn and GTAn (n = 0 to 3) contain their initial values. This data can be adjusted by setting registers GTPn and GTAn (n = 0 to 3) (refer to pages 26 and 27).

*2) Digital input timing measurements are made at 0.5VDD for rising edges and falling edges.
Digital output timing measurements are made at 0.5VDD for rising edges and falling edges.



Note Internal data of the LSI device is changed by DTMF data immediately before STD goes high.





Register Functions

1) Register configuration

Address				Function	Data							
A3	A2	A1	A0		D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	Control register 1	BS2	BS1	BS0	MSKSL	MSKTX	MSKRCLK	FSL	FCLN
0	0	0	1	Control register 2	MCKSL1	MCKSL0	TXRXA	VR4	VR3	VR2	VR1	VR0
0	0	1	0	DTMF register 1	GTP3	GTP2	GTP1	GTP0	GTA3	GTA2	GTA1	GTA0
0	0	1	1	DTMF register 2	–	STDPGA1	STDPGA0	DTMFSL	AGCSW1	AGCSW0	PGA1	PGA0
0	1	0	0	Modem frame pattern 1	Lower 8 bits of MSK modem frame pattern							
0	1	0	1	Modem frame pattern 2	Upper 8 bits of MSK modem frame pattern							
0	1	1	0	Modem receive data register	MSK receive data (RDATA)							
0	1	1	1	Software reset	SRST[7:0]							
1	0	0	0	Revision register	–	–	–	–	REVNUM[3:0]			
1	0	0	1	Test register 1	Test register 1 for LSI test operation (not accessible)							
1	0	1	0	Test register 2	Test register 2 for LSI test operation (not accessible)							
1	0	1	1	Not used	–	–	–	–	–	–	–	–
↓	↓	↓	↓	Not used	–	–	–	–	–	–	–	–
1	1	1	1	Not used	–	–	–	–	–	–	–	–

Note 1 An access to data indicated by "-" does not have any effect on the LSI operation, and always reads 0.

Note 2 The SRST[7:0] register at address 0111 is write-only.
The MSK receive data register at address 0110 and the REVNUM[3:0] register at address 1000 are read-only.

Note 3 Test registers are located at addresses 1001 and 1010 and cannot be accessed. If an access is made to these addresses inadvertently, the LSI operation is not guaranteed.

2) Descriptions of registers

2.1) Control register 1

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	BS2	BS1	BS0	MSKSL	MSKTX	MSKRCLK	FSL	FCLN
Initial value				0	0	0	1	1	0	0	1

2.1.1) Operation mode setting

BS2	BS1	BS0	Mode name	OSC and AGND	MSK modem TX	MSK modem RX	DTMF Receiver
0	0	0	Mode 0 (power down)	OFF	OFF	OFF	OFF
0	0	1	Mode1 (standby)	ON	OFF	OFF	OFF
0	1	0	Mode 2	ON	ON	OFF	OFF
0	1	1	Mode 3	ON	OFF	ON	OFF
1	0	0	Mode 4	ON	ON	ON	OFF
1	0	1	Mode 5	ON	OFF	OFF	ON
1	1	0	Mode 6	ON	ON	ON	ON

Note: After setting the system reset(Mode 0), select Mode 2 to 6 via setting Mode 1.

2.1.2) MSK modem setting

Data	Item	Function		Remarks
		0	1	
MSKSL	MSK modem transmission speed	2400 bit/s	1200 bit/s	
MSKTX	MSK transmit output	OFF (Mute)	ON (Active)	
MSKRCLK	RCLK output switching	RCLK pin High output	RCLK pin Active	
		RDFFD/RDATA pin Active (RDFFD signal output)	RDFFD/RDATA pin Active (RDATA signal output)	
FSL	RDF/FD output switching	Frame detection signal (FD) output	Receive flag signal (RDF) output	
FCLN	Frame Detect	ON (Enable)	OFF (Disable)	

2.2) Control register 2

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	MCKSL1	MCKSL0	TXRXA	VR4	VR3	VR2	VR1	VR0
Initial value				0	0	0	0	1	1	0	0

MCKSL1	MCKSL0	Function	Remarks
0	0	Master clock: 3.6864MHz	
0	1	Master clock: 7.3728MHz	External input only
1	0	Master clock: 11.0592MHz	External input only
1	1	Master clock: 14.7456MHz	External input only

Data	Item	Function		Remarks
		0	1	
TXRXA	TXA and RXA amplifier operation	OFF (Power OFF)	ON (Power ON)	ORed with operation mode setting; valid in modes 1 to 6

VR4	VR3	VR2	VR1	VR0	VR gain (dB)
0	0	0	0	0	-6.0
0	0	0	0	1	-5.5
0	0	0	1	0	-5.0
0	0	0	1	1	-4.5
0	0	1	0	0	-4.0
0	0	1	0	1	-3.5
0	0	1	1	0	-3.0
0	0	1	1	1	-2.5
0	1	0	0	0	-2.0
0	1	0	0	1	-1.5
0	1	0	1	0	-1.0
0	1	0	1	1	-0.5
0	1	1	0	0	0.0

VR4	VR3	VR2	VR1	VR0	VR gain (dB)
0	1	1	0	1	+0.5
0	1	1	1	0	+1.0
0	1	1	1	1	+1.5
1	0	0	0	0	+2.0
1	0	0	0	1	+2.5
1	0	0	1	0	+3.0
1	0	0	1	1	+3.5
1	0	1	0	0	+4.0
1	0	1	0	1	+4.5
1	0	1	1	0	+5.0
1	0	1	1	1	+5.5
1	1	0	0	0	+6.0

2.3) DTMF register 1

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	GTP3	GTP2	GTP1	GTP0	GTA3	GTA2	GTA1	GTA0
Initial value				0	1	0	0	0	0	1	0

Data	Function	Remarks
GTP3 to GTP0	Register for setting DTMF Receiver guard time t_{GTP}. For details, refer to "DTMF Receiver Operation".	
GTA3 to GTA0	Register for setting DTMF Receiver guard time t_{GTA}. For details, refer to "DTMF Receiver Operation".	

2.4) DTMF register 2

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	–	STDPGA1	STDPGA0	DTMFSL	AGCSW1	AGCSW0	PGA1	PGA0
Initial value				–	0	0	1	0	1	0	0

STDPGA1	STDPGA0	PGA gain (dB)
0	0	0
0	1	+4
1	0	+8
1	1	+12

Note When AGC circuit is enable, automatic set PGA gain can be monitored by STDPGA[1:0] register. This register is read-only and synchronized with the rising edge on the DTMF signal detection pin: STD.

Data	Item	Function		Remarks
		0	1	
DTMFSL	DTMF input switching	DTMFIN pin input	RXIN pin input	

AGCSW1	AGCSW0	Function	Remarks
0	0	AGC circuit Off (Disable) PGA gain can be set with PGA[1:0] register.	
0	1	AGC circuit On (Enable) PGA gain can be monitored by STDPGA[1:0] register. The register data is renewal at every DTMF detection.	Initial value
1	0	AGC circuit Off (Disable) PGA gain may be set with the latest STDPGA[1:0] register, then AGC is off. PGA gain can not be set with PGA[1:0].	
1	1	Not used	

PGA1	PGA0	PGA gain (dB)
0	0	0
0	1	+4
1	0	+8
1	1	+12

Note When the AGC circuit is disabled, the gain of the PGA circuit can be set manually with PGA[1:0].

2.5) Modem frame pattern register (at power-down: specific low-power radio)

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	F07	F06	F05	F04	F03	F02	F01	F00
Initial value				1	0	1	0	1	0	0	0
0	1	0	1	F15	F14	F13	F12	F11	F10	F09	F08
Initial value				0	0	0	1	1	0	1	1

2.6) Modem receive data register

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

Data	Item	MSK receive data		Remarks
		0	1	
RD7 to RD0	MSKSL=0	2.4kHz	1.2kHz	Data received first is RD7.
	MSKSL=1	1.8kHz	1.2kHz	

This register is read-only, and no data can be written to the register.

2.7) Software reset register

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	SRST[7:0]							
Initial value				0	0	0	0	0	0	0	0

When data 0xAA:10101010 is written to the SRST[7:0] register, a software reset is performed.
This sets BS[2:0] to mode 1 (standby) and the registers other than BS[2:0] to their initial values to place the system in the standby state.
This register is write-only, and after completion of software reset, the register is set to 0.

2.8) Revision register

Address				Data							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	–	–	–	–	REVNUM[3:0]			
Initial value				–	–	–	–	0	0	0	0

When the D3 to D0 data is accessed, the revision number for management can be read.
This register is read-only, and no data can be written to the register.

MSK Modem Operation

1) MSK Modulator

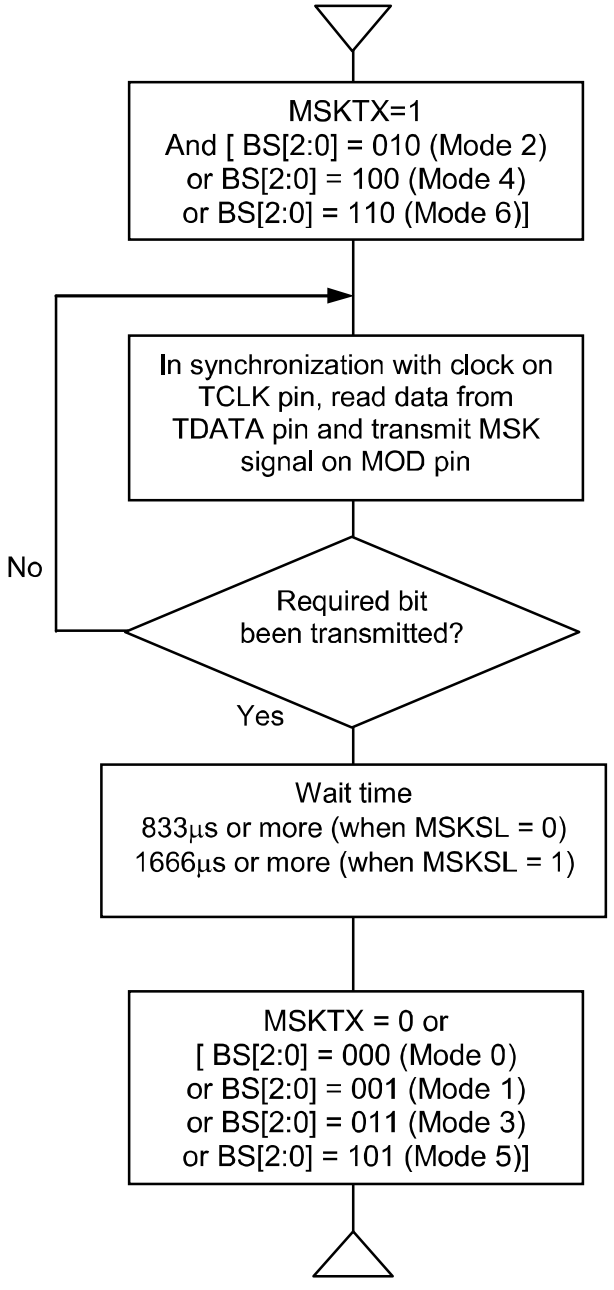
The TX section of the modem interfaces with the Modulator by using the TCLK, TDATA, and MOD pins and register data BS2, BS1, BS0 (referred to as BS[2:0]), and MSKTX as follows:

(1) Set MSKTX to 1 and BS[2:0] to mode 2, 4, or 6 to start MSK transmission.

(2) A 1200Hz or 2400Hz clock is output on the TCLK pin. In synchronization with the rising edge of TCLK, the AK2363 reads MSK transmit data from the TDATA pin and outputs the modulated MSK signal on the MOD pin.

(3) After as many bits as required have been transmitted, wait for two clock periods until the last bit of the MSK signal has been transmitted.

(4) Then, set BS[2:0] to change from mode 2, 4, or 6 to mode 0,1, 3, or 5. Alternatively, set MSKTX to 0 to end signal transmission.



: Start MSK signal transmission.

: MSK signal transmission in progress

: MSK data has been transmitted.

: End MSK signal transmission.

2) MSK Demodulator

2.1) When Frame Detect is not used

The modem interfaces with the Demodulator by using the RXIN, RCLK, and RDFFD/RDATA pins, register data BS[2:0], and MSKRCLK as follows:

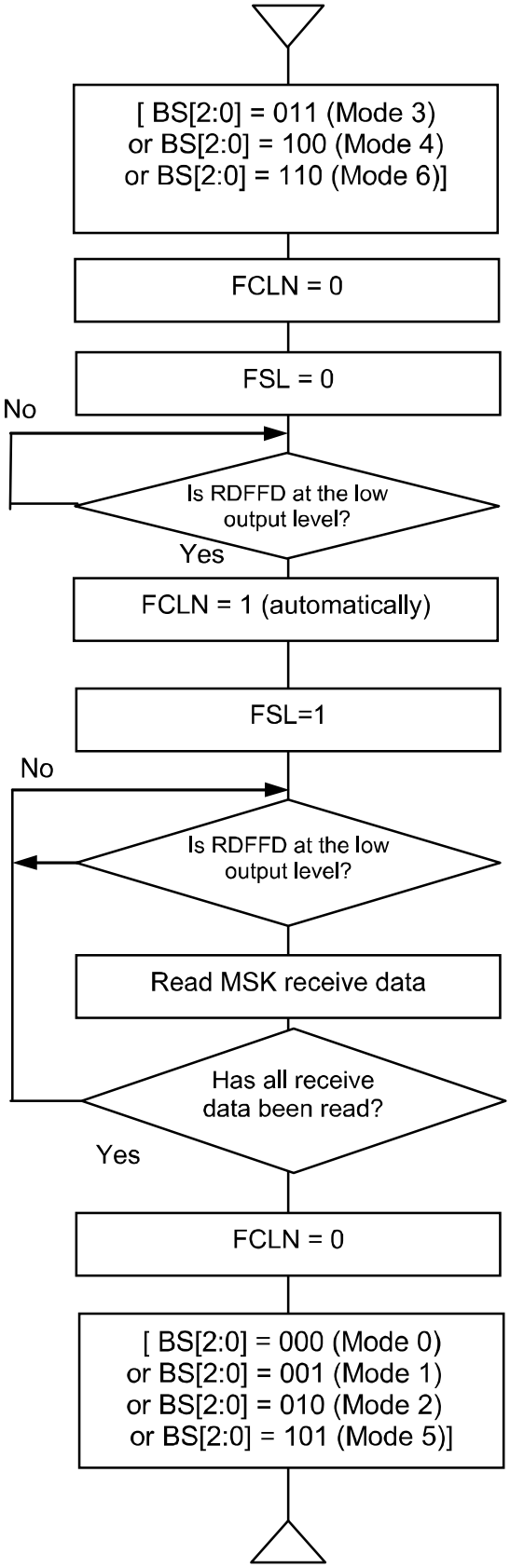
(1) Set BS[2:0] to select mode 3, 4, or 6, and at the same time set MSKRCLK to 1 to start MSK reception.
(2) When the MSK signal is received on the RXIN pin, data demodulated via MSK-BPF, Data-Demodulator, and the Digital-PLL circuit is output successively as RDATA on the RDFFD/RDATA pin in synchronization with the falling edge of the 1200Hz or 2400Hz clock signal output on the RCLK pin.
(3) Set BS[2:0] to select mode 0, 1, 2, or 5. The MSK signal reception operation then ends.

2.2) When Frame Detect is used

The modem interfaces with the Demodulator by using the RXIN, RDFFD/RDATA, SDATA, SCLK, and CSN pins, and register data BS[2:0], MSKRCLK, FSL, and FCLN as follows:

(1) Set BS[2:0] to select mode 3, 4, or 6, and at the same time set MSKRCLK to 0, FSL to 0, and FCLN to 0 to start MSK reception. This setting allows the RDFFD/RDATA pin to function as RDFFD frame detection (FD) and output the high level, waiting for a synchronized frame. At this time, the CSN pin is set to the high input level, and the SCLK pin is set to the low input level.
(2) When a synchronized frame is detected, the RDFFD/RDATA pin performs a frame detection (FD) operation. The pin is at the low output level during period T, and FCLN data is set to 1 automatically.
(3) When the low level on the RDFFD/RDATA pin is monitored, set FSL to 1 so that the MSK receive flag signal (RDF) is output.
(4) After 8-bit receive data (MD7 to MD0) is transferred from internal node RDATA_n to the buffer, the RDFFD/RDATA pin is set to the low output level as an RDF operation.
(5) When the CPU monitors this change, demodulated data (RD7 to RD0) is read from the modem receive data register (address: A[3:0] = 0110).
(6) After the data has been read from the modem receive data register, the RDFFD/RDATA pin is set to the high output level, indicating that data RD7 to RD0 in the buffer has all been read.
(7) By repeating steps (4), (5), and (6) above, demodulated data can be read from the receive data register.
(8) After completing read of necessary data, set FCLN to 0. Then, internal nodes RCLK and RDATA are initialized, and the system waits for another synchronized frame.
(9) Set BS[2:0] to select mode0, 1, 2, or 5. The MSK signal reception operation then ends.

This frame detection circuit does not have a reset feature. Therefore, if the above steps (1) to (8) are canceled in the middle, the steps must be restarted from (1). As mentioned in (2), while the RDFFD/RDATA pin is at the low output level as a result of frame detection (FD), the FCLN data is set to 1 automatically. During this period, an attempt to write 0 is ignored. Setting must be made again after the RDFFD/RDATA pin is set to the high output level.



: Start MSK signal reception.

: Turn on Frame Detect.

: Specify output of frame detection signal (FD).

: Wait until synchronized frame is detected.

: Cancel Frame Detect.

: Specify output of receive flag signal (RDF).

: Wait until 8-bit data is received.

: RDF is set to high level after MSK receive data is read, and it is set to low level after MSK receive data is updated.

: Wait for another synchronized frame.

: End MSK signal reception.

DTMF Receiver Operation

1) DTMF Receiver

The DTMF Receiver detects a received DTMF signal and outputs a 4-bit code.
The output 4-bit codes are listed below.

Output code table

Low tone [Hz]	High tone [Hz]	KEY	SD3 (MSB)	SD2	SD1	SD0 (LSB)
697	1209	1	0	0	0	1
	1336	2	0	0	1	0
	1477	3	0	0	1	1
770	1209	4	0	1	0	0
	1336	5	0	1	0	1
	1477	6	0	1	1	0
852	1209	7	0	1	1	1
	1336	8	1	0	0	0
	1477	9	1	0	0	1
941	1336	0	1	0	1	0
	1209	*	1	0	1	1
	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0

2) Decoding result output

The result of DTMF RX signal decoding is output on the SD pin through the internal output buffer.
The internal output buffer is controlled with the LOADN pin.

LOADN pin input	SD pin output
0	Decoding result output
1	High level output

3) Setting the guard time

The tone duration accept time (t_{REC}), tone duration reject time (t_{REJ}), interdigit pause accept time (t_{ID}), and interdigit pause reject time (t_{DO}) can be set to desired values by adjusting the guard time as shown below. The guard time is set in registers GTPn and GTAn (n = 0 to 3).

Tone duration accept time (t_{REC}) = Tone present detection time (t_{DP}) + Guard time (t_{GTP})
Tone duration accept time (t_{REC}) = Tone present detection time (t_{DP}) + Guard time (t_{GTP}) - Tone absent detection time (t_{DA})

Interdigit pause accept time (t_{ID}) = Tone absent detection time (t_{DA}) + Guard time (t_{GTA})
Interdigit pause reject time (t_{DO}) = Tone absent detection time (t_{DA}) + Guard time (t_{GTA}) - Tone present detection time (t_{DP})

Guard time (t_{GTP}) setting range	10ms to 134ms
Guard time (t_{GTP}) setting step	9ms

Guard time (t_{GTA}) setting range	19ms to 134ms
Guard time (t_{GTA}) setting step	9ms

For the relationships between settings in registers GTPn and GTAn (n = 0 to 3) and guard time values, refer to the tables given below.
The tables also show the relationships with the tone duration accept time (t_{REC}) and interdigit pause accept time (t_{ID}).

Register GTPn (n = 0 to 3) vs. guard time t_{GTP} vs. tone duration accept time t_{REC} (AGC Disable)

t_{DP} (ms)		
Min.	Typ.	Max.
5	11	16.8

GTP register				$t_{GTP\ (ms)}$	t_{REC}(ms) = t_{GTP} + t_{DP}		
3	2	1	0	Typ.	Min.	Typ.	Max.
0	0	0	1	10	15	21	27
0	0	1	0	19	24	30	36
0	0	1	1	28	33	39	45
0	1	0	0	37	42	48	54
0	1	0	1	46	51	57	63
0	1	1	0	54	60	65	71
0	1	1	1	63	68	74	80
1	0	0	0	72	77	83	89
1	0	0	1	81	86	92	98
1	0	1	0	90	95	101	107
1	0	1	1	99	104	110	116
1	1	0	0	108	113	119	125
1	1	0	1	117	122	128	134
1	1	1	0	126	131	137	143
1	1	1	1	134	139	145	151

Register GTAn (n = 0 to 3) vs. guard time t_{GTA} vs. interdigit pause accept time t_{ID}

t_{DA} (ms)		
Min.	Typ.	Max.
0.5	4	8.5

GTA register				$t_{GTA\ (ms)}$	t_{ID}(ms) = t_{GTA} + t_{DA}		
3	2	1	0	Typ.	Min.	Typ.	Max.
0	0	1	0	19	19	23	27
0	0	1	1	28	28	32	36
0	1	0	0	37	37	41	45
0	1	0	1	46	46	50	54
0	1	1	0	54	55	58	63
0	1	1	1	63	64	67	72
1	0	0	0	72	73	76	81
1	0	0	1	81	82	85	90
1	0	1	0	90	91	94	99
1	0	1	1	99	99	103	107
1	1	0	0	108	108	112	116
1	1	0	1	117	117	121	125
1	1	1	0	126	126	130	134
1	1	1	1	134	135	138	143

Cautions

1) t_{GTP} and t_{GTA} in the tables are typical values. A variation of ±1ms should be considered.
2) If guard time GTPn (n = 0 to 3) is set to 0000, a wrong decoding result may be output. Therefore, avoid such setting.
3) If guard time GTAn (n = 0 to 3) is set to 0000 and 0001, the interdigit pause reject time cannot be acquired. Therefore, avoid such settings.

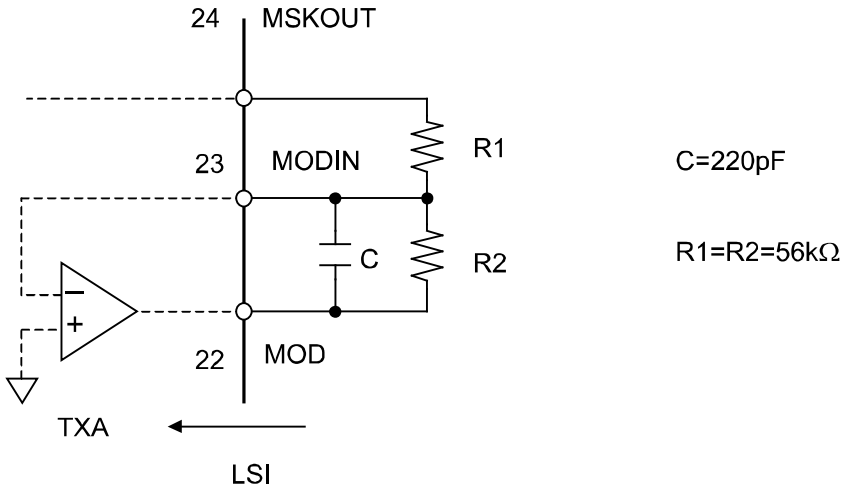
4) AGC circuit operation
When AGCSW [1:0] register is set to 01, AGC circuit is enable to operate as shown below table.

RXINO or DTMFIN pin Input level (dBx)	PGA setting Gain (dB)	PGA=0dB Internal level (dBx)	PGA=+4dB Internal level (dBx)	PGA=+8dB Internal level (dBx)	PGA=+12dB Internal level (dBx)
-21	0	-21	-17	-13	-9
-22	0	-22	-18	-14	-10
-23	0	-23	-19	-15	-11
-24	0	-24	-20	-16	-12
-25	0	-25	-21	-17	-13
-26	0	-26	-22	-18	-14
-27	0	-27	-23	-19	-15
-28	+4	–	-24	-20	-16
-29	+4	–	-25	-21	-17
-30	+4	–	-26	-22	-18
-31	+4	–	-27	-23	-19
-32	+8	–	–	-24	-20
-33	+8	–	–	-25	-21
-34	+8	–	–	-26	-22
-35	+8	–	–	-27	-23
-36	+12	–	–	–	-24
-37	+12	–	–	–	-25
-38	+12	–	–	–	-26
-39	+12	–	–	–	-27

Recommended External Circuit Examples

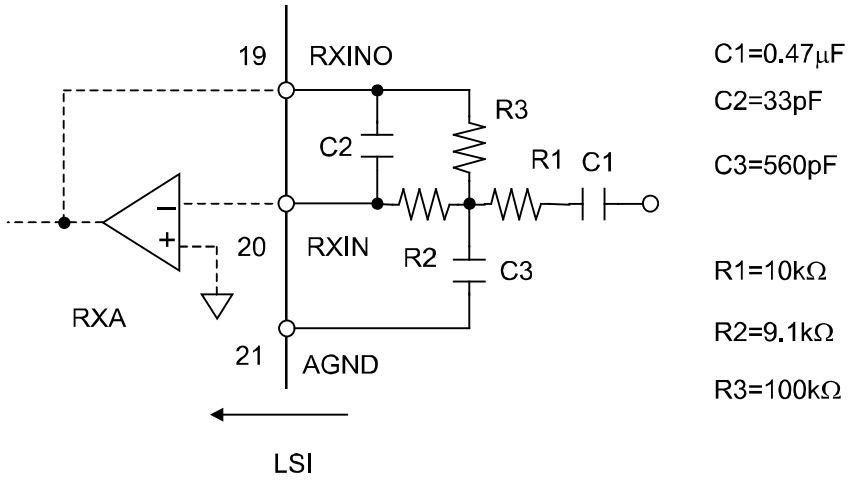
1) TXA amplifier

This amplifier is used to adjust the gain of the TX signal and to form a smoothing filter.
Because the MSKOUT pin output includes a 115.2kHz sampling clock, it is recommended that this amplifier be used for smoothing.
The following gives a sample configuration of a first order LPF with a gain of 0dB and cut-off frequency of 13kHz:



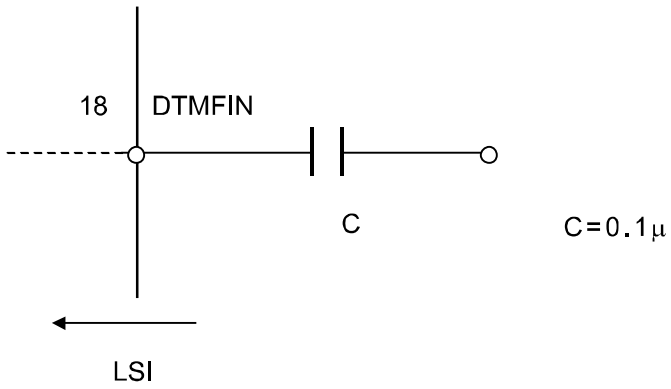
2) RXA amplifier

This amplifier is used for adjusting the gain of the RX signal. Set the gain to 20dB or less. For high frequency noise over 100kHz, form an anti-aliasing filter.
The following gives a sample configuration of a second order LPF with a gain of 20dB and cut-off frequency of 39kHz:



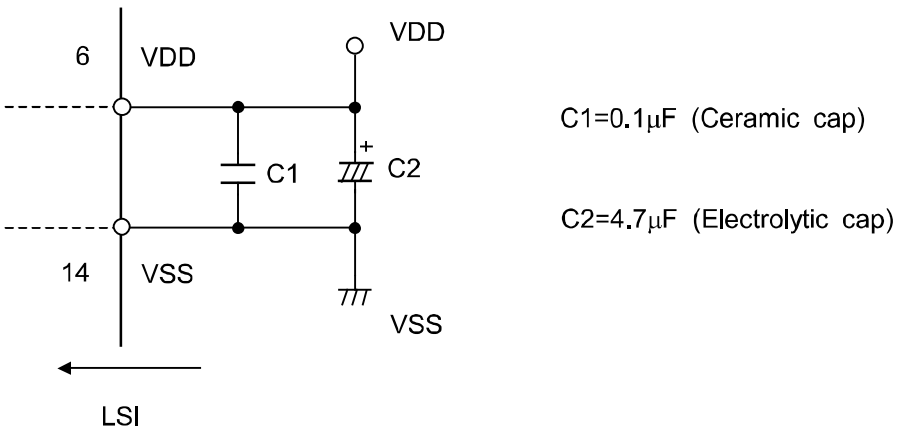
3) External DTMFIN capacitor

Connect a capacitor to the DTMFIN pin to adjust the DC offset of the input signal and the internal operation point in the LSI device. This forms a high-pass filter with fc being about 3Hz.



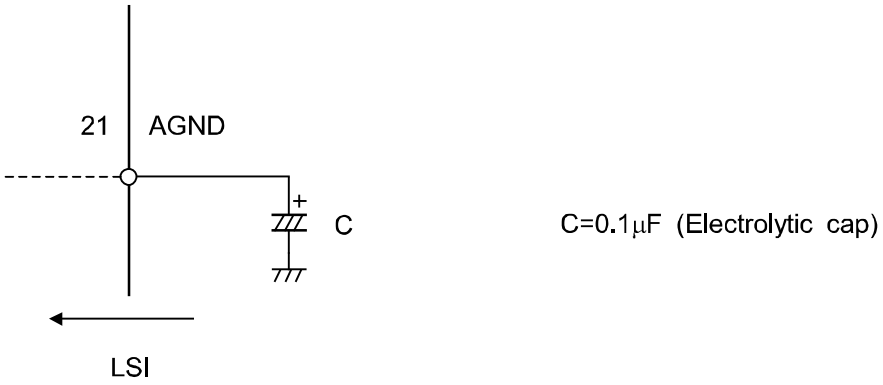
4) Power supply stabilizing capacitors

Connect capacitors between the VDD and VSS pins to eliminate ripple and noise included in power supply as shown below. For maximum effect, the capacitors should be placed at a shortest distance between the pins.



5) AGND stabilizing capacitor

It is recommended that a capacitor with 0.1μF be connected between VSS and the AGND pin to stabilize the AGND signal. The capacitor should be placed as close to the pin as possible.



6) Oscillator circuit

When the built-in oscillator circuit is to be used, connect a 3.6864MHz crystal oscillator, a resistor, and capacitors as shown in Fig. 1. The internal buffer is designed to allow stable oscillation of a crystal oscillator for the electrical equivalent circuitry with a resonance resistance of 150Ω (Max.) and a shunt capacitance of 5pF (Max.).
It is recommended that 22pF capacitors be connected externally so that the total load capacitance is 16pF (5pF + 22pF//22pF) or less. Place the oscillator, resistor, and capacitors as close to the XIN and XOUT pins as possible.

When a clock signal is supplied externally, not only 3.6864MHz but also 7.3728MHz (twice higher than 3.6864MHz), 11.0592MHz (three times higher than 3.6864MHz), and 14.7456MHz (four times higher than 3.6864MHz) are supported. However, the internal frequency must always be set to 3.6864MHz by selecting division by 2, 3, or 4 for the divider in the subsequent stage. Connect the clock signal as shown in Fig. 2 or Fig. 3 according to the clock amplitude level.

The circuit in the first stage of the XIN pin has a constant threshold voltage (0.8V). Therefore, if the high level of the input clock is 1.5V or higher and the low level is 0.4V or lower, connect the clock signal as shown in Fig. 2. If the input clock amplitude (p-p value) is 0.2V or higher and 1.0V or lower, connect the clock signal as shown in Fig. 3.

When the clock is to be shared with peripheral ICs, the clock must be input and output on the XIN pin. The clock amplitude must not exceed the absolute maximum rating.

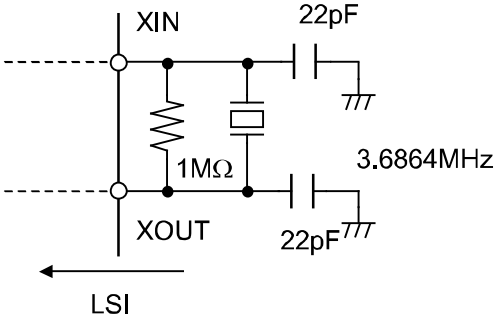


Fig. 1

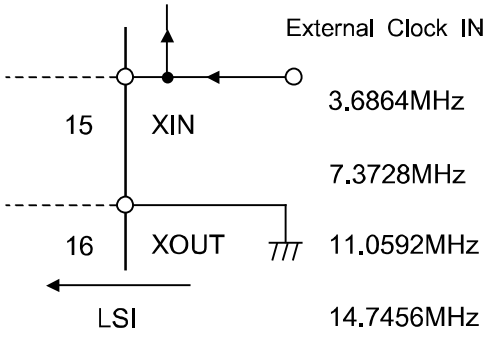


Fig. 2

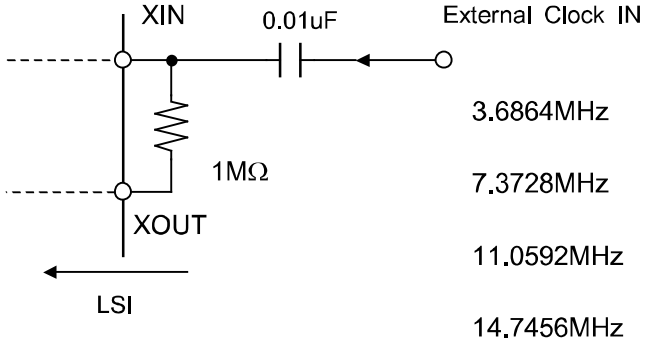
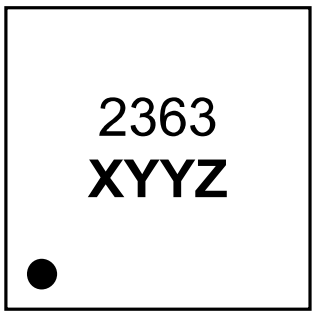


Fig. 3

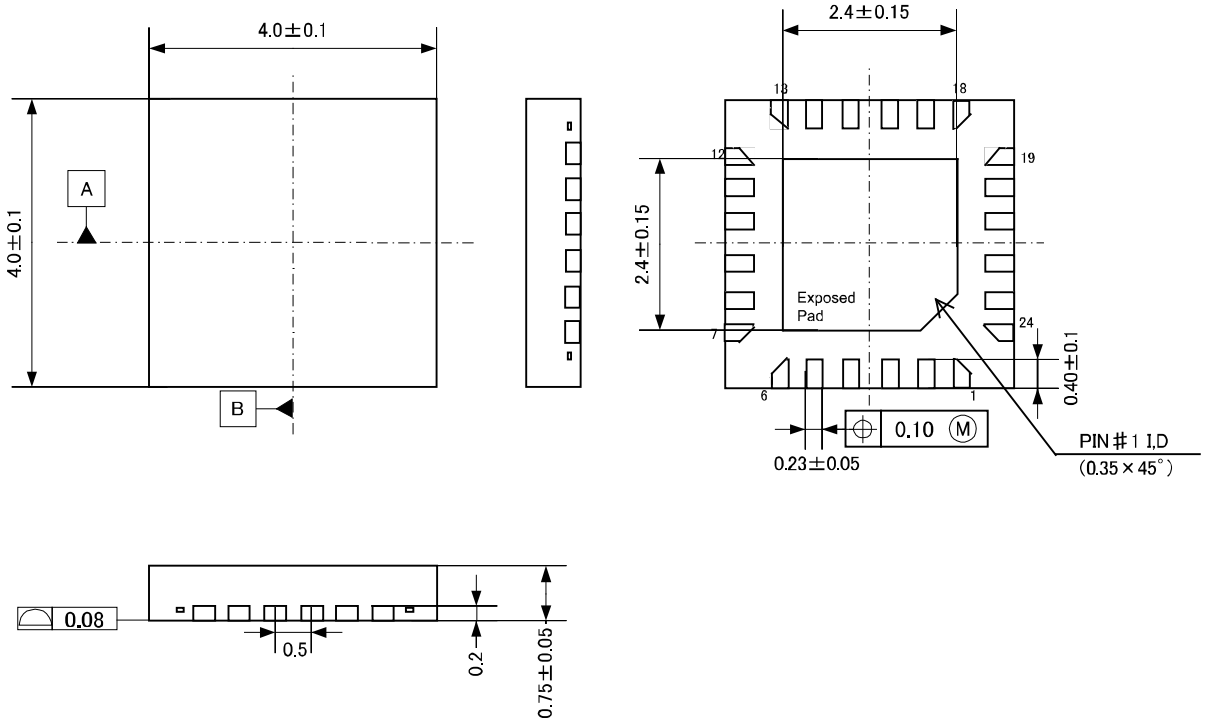
Package

1) Marking



Parts number 2363
Date code X: Date of production Ones digit of the calendar year
Y: Date of production Week
Z: Production lot Identification code

2) Dimensions
Package type: 24-pin QFNJ (4.0 x 4.0 x 0.75mm, 0.5mm pitch)



Cautions: The central backside of the package called Exposes Pad should be connected to VSS or no connects.

Important Notice

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