# AK5397

## 32-Bit Stereo Premium ADC

## 1. Genaral Description

The AK5397 is a high performance 32-bit stereo ADC that achieves class leading performance of 127dB dynamic range for stereo output. This is a flagship addition to AKM's VERITA series of product in the Audio 4 Pro™ family. The AK5397 integrates a newly developed circuit by VELVET SOUND™ technology achieving rich sound field and bass representation that realizes a music playback experience with less distortion. The class leading performance with a maximum 768kHz PCM output is supported for digital output and newly developed 32-bit digital filters are integrated for the best sound quality. The AK5397 is suitable for digital video recorders and high quality sound studio mixers for recording and editing high-resolution sound sources.

## 2. Feartures

- Advanced multi bit Architecture ADC
- Resolution: 32bit
- Sampling Rate: 8kHz ~ 768kHz
- Full Differential Inputs
- S/(N+D): 108dB
- DR, S/N: 127dB (Mono Mode: 130dB)
- Sharp Roll Off Digital Filter (GD=41.5/fs)
  - Passband: 0 ~ 21.82kHz (@ fs=48kHz)
  - Passband Ripple: +0.00010/-0.00015dB
  - Stopband Attenuation: 100dB
- Short Delay Digital Filter (GD=12.5/fs)
  - Passband: 0 ~ 22.22kHz (@ fs=48kHz)
  - Passband Ripple: +0.055/-0.015dB
  - Stopband Attenuation: 93dB
- Minimum Phase Digital Filter (GD=3.5/fs)
  - Passband: 0 ~ 21.75kHz(@ fs=48kHz)
  - Passband Ripple: +0.04/-0.02dB
  - Stopband Attenuation: 93dB
- Master / Slave Mode
- Master Clock:
  - 256fs/512fs (Normal Speed; 8kHz~48kHz)
  - 256fs (Double Speed; 48Hz ~ 96kHz)
  - 128fs (Quad Speed; 96kHz ~ 192kHz)
  - 64fs (Octal Speed; 192kHz ~ 384kHz)
  - 32fs (Hex Speed; 384kHz ~ 768kHz)
- Audio Interface Format: 32bit MSB justified, I2S compatible or TDM
- Cascade TDM I/F: 8ch/48kHz, 4ch/96kHz, 4ch/192kHz
- Digital HPF for Offset Cancel
- Overflow Flag
- Power Supply:
  - 4.75 ~ 5.25V(Analog), 3.0 ~ 3.6V(Digital)
- Power Dissipation: 455mW
- Ta = -10 ~ 70 °C
- Package: 44-pin LQFP

## 3. Block Diagram

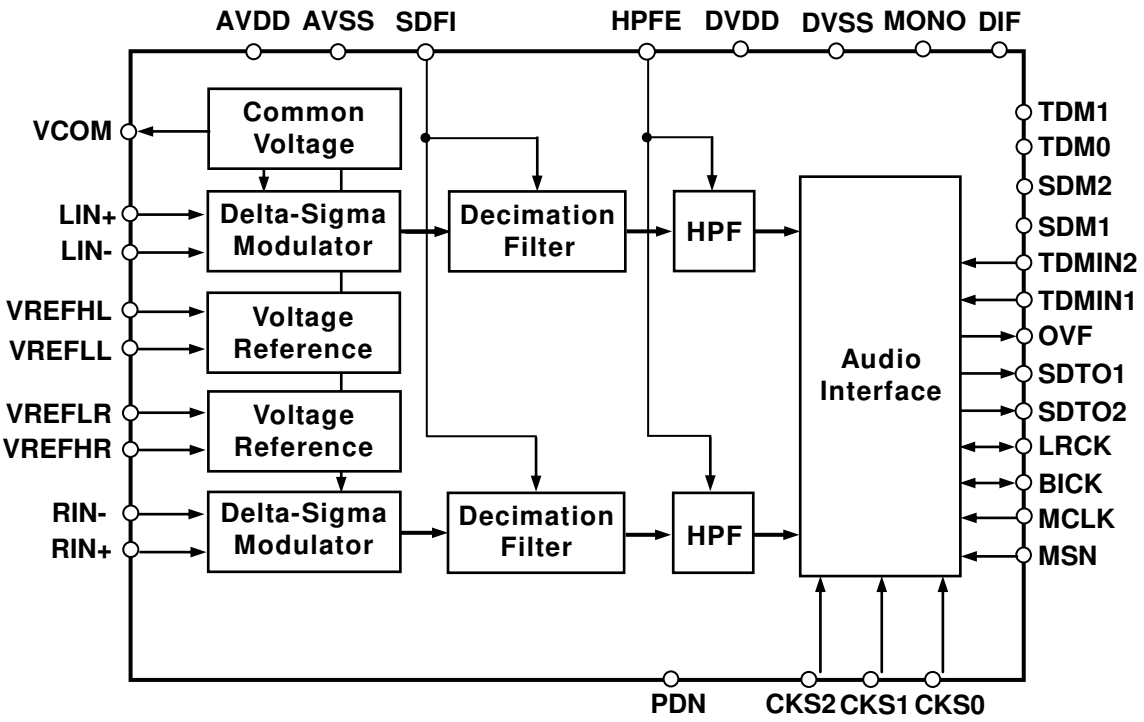


Figure 1. Block Diagram

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## 5. Pin Configurations and Functions

### ■ Pin Configurations

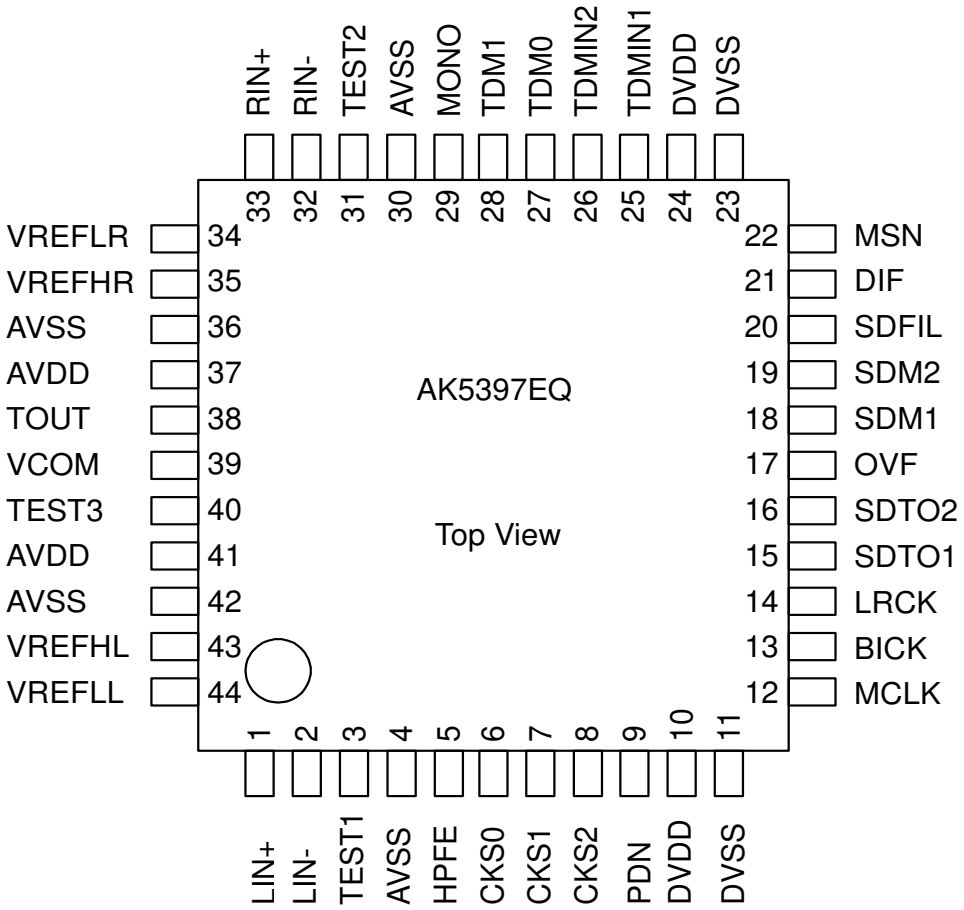



Figure 2. Pin Configurations

## ■ Functions

| No. | Pin Name | Power | I/O | Function |
|---|---|---|---|---|
| 1 | LIN+ | A | I | Lch Positive Analog Input Pin |
| 2 | LIN- | A | I | Lch Negative Analog Input Pin |
| 3 | TEST1 | A | - | Test Pin<br>This pin must be connected to AVSS. |
| 4 | AVSS | A | - | Analog Ground Pin, 0V |
| 5 | HPFE | D | I | HPF Enable Pin<br>“L”: Disable, “H” Enable |
| 6 | CKS0 | D | I | Clock Mode Select #0 Pin |
| 7 | CKS1 | D | I | Clock Mode Select #1 Pin |
| 8 | CKS2 | D | I | Clock Mode Select #2 Pin |
| 9 | PDN | D | I | Power down & Reset pin<br>“L”: All blocks are powered-down and reset.<br>“H”: Normal Operation |
| 10 | DVDD | D | - | Digital Power Supply Pin, 3.0V ~ 3.6V |
| 11 | DVSS | D | - | Digital Ground Pin, 0V |
| 12 | MCLK | D | I | Master Clock Input Pin |
| 13 | BICK | D | I/O | Serial Data Clock Pin<br>When PDN pin = “L”, BICK outputs “L” in master made. |
| 14 | LRCK | D | I/O | L/R Channel Select Clock Pin<br>When PDN pin = “L”, LRCK outputs “L” in master made. |
| 15 | SDTO1 | D | O | Serial Data Output #1 Pin (Sharp Roll Off Filter Output)<br>When PDN pin = “L”, SDTO1 outputs “L”. |
| 16 | SDTO2 | D | O | Serial Data Output #2 Pin (Short Delay or Minimum Phase Filter Output)<br>When PDN pin = “L”, SDTO2 outputs “L”. |
| 17 | OVF | D | O | Analog Input Overflow Detect Pin<br>This pin goes to “H” if any analog inputs overflows<br>When the PDN pin = “L”, the OVF pin outputs “L”. |
| 18 | SDM1 | D | I | SDTO1 Output Mute Pin<br>This function is synchronized with LRCK edges.<br>“L”: Normal Operation, “H”: “L” output |
| 19 | SDM2 | D | I | SDTO2 Output Mute Pin<br>This function is synchronized with LRCK edges.<br>“L”: Normal Operation, “H”: “L” output |
| 20 | SDFIL | D | I | SDTO2 Digital Filter Select Pin<br>“L”: Short Delay, “H”: Minimum Phase |
| 21 | DIF | D | I | Audio Interface Format Pin<br>“L”: 32bit MSB justified, “H”: 32bit $I^2S$ Compatible |
| 22 | MSN | D | I | Master/Slave mode Select Pin<br>“L”: Slave mode, “H”: Master mode |
| 23 | DVSS | D | - | Digital Ground Pin, 0V |
| 24 | DVDD | D | - | Digital Power Supply Pin, 3.0 ~ 3.6V |
| 25 | TDMIN1 | D | I | TDM Data Input #1 Pin |
| 26 | TDMIN2 | D | I | TDM Data Input #2 Pin |
| 27 | TDM0 | D | I | TDM I/F Format Enable Pin<br>“L”: Normal Mode, “H”: TDM Mode |
| 28 | TDM1 | D | I | TDM I/F BICK Frequency Select Pin<br>“L”: 256fs, “H”: 128fs |

| No. | Pin Name | Power | I/O | Function |
|---|---|---|---|---|
| 29 | MONO | D | I | Stereo/Mono mode Select Pin<br>"L": Stereo mode, "H": Mono mode |
| 30 | AVSS | A | - | Analog Ground Pin, 0V |
| 31 | TEST2 | A | I | Test Pin<br>This pin must be connected to AVSS. |
| 32 | RIN- | A | I | Rch Negative Analog Input Pin |
| 33 | RIN+ | A | I | Rch Positive Analog Input Pin |
| 34 | VREFLR | A | I | Rch Negative Reference Voltage Input Pin<br>Normally connected to AVSS. |
| 35 | VREFHR | A | I | Rch Positive Reference Voltage Input Pin, 4.75 ~ 5.25V<br>Normally connected to the VREFLR pin with a large electrolytic capacitor and a 0.1μF ceramic capacitor. |
| 36 | AVSS | A | - | Analog Ground Pin, 0V |
| 37 | AVDD1 | A | - | Analog Power Supply Pin, 4.75 ~ 5.25V |
| 38 | TOUT | A | I | TEST Pin<br>This pin must be Connected to AVSS. |
| 39 | VCOM | A | O | Common Voltage Output Pin, AVDD/2<br>Normally connected to AVSS with a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic capacitor. |
| 40 | TEST3 | A | I | Test Pin<br>This pin must be connected to AVSS. |
| 41 | AVDD2 | A | - | Analog Power Supply Pin, 4.75 ~ 5.25V |
| 42 | AVSS | A | - | Analog Ground Pin, 0V |
| 43 | VREFHL | A | I | Lch Positive Reference Voltage Input Pin, 4.75 ~ 5.25V<br>Normally connected to the VREFLL pin with a large electrolytic capacitor and a 0.1μF ceramic capacitor. |
| 44 | VREFLL | A | I | Lch Negative Reference Voltage Input Pin<br>Normally connected to AVSS. |

Note 1. All digital input pins must not be left floating.

## ■ Handling of Unused Pin

The unused I/O pin must be processed as below.

| Classification | Pin Name | Setting |
|---|---|---|
| Digital | TEST1/2/3, TOUT | This pin must be connected to AVSS. |
| | TDMIN1/2 | This pin must be connected to DVSS. |
| | SDTO1, SDTO2, OVF | This pin must be open. |
| Analog | LIN+, LIN- | Connect the LIN+ pin and the LIN- pin. |
| | RIN+, RIN- | Connect the RIN+ pin and the RIN- pin. |

## 6. Absolute Maximum Ratings

(AVSS=DVSS=0V; Note 2)

| Parameter | | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Power Supplies: | Analog | AVDD | –0.3 | 6.0 | V |
| | Digital | DVDD | –0.3 | 4.6 | V |
| | \|AVSS-DVSS\| (Note 3) | ΔGND1 | – | 0.3 | V |
| Input Current, Any Pin Except Supplies | | IIN | – | ±10 | mA |
| Analog Input Voltage (Note 4) | | VINA | –0.3 | AVDD+0.3 | V |
| Digital Input Voltage (Note 5) | | VIND | –0.3 | DVDD+0.3 | V |
| Ambient Temperature (power applied) | | Ta | –10 | 70 | °C |
| Storage Temperature | | Tstg | –65 | 150 | °C |

Note 2. All voltages with respect to ground.
Note 3. AVSS and DVSS must be connected to the same analog ground plane.
Note 4. VREFHL, VREFLL, VREFHR, VREFLR, LIN+, LIN-, RIN+, RIN-, TEST1-3 and TOUT pins.
Note 5. CKS0, CKS1, CKS2,PDN, SDM1, SDM2, SDFIL, TDMIN1, TDMIN2, MCLK, BICK, LRCK, DIF, MSN, HPFE, MONO, TDM0, TDM1pins

WARING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

## 7. Recommended Operating Conditions

(AVSS=DVSS=0V; Note 2)

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Power Supplies: (Note 6) | Analog | AVDD | 4.75 | 5.0 | 5.25 | V |
| | Digital | DVDD | 3.0 | 3.3 | 3.6 | V |
| Voltage Reference (Note 9) | "H" voltage reference (Note 7) | VREFHL/R | AVDD-0.5 | - | AVDD | V |
| | "L" voltage reference (Note 8) | VREFLL/R | - | AVSS | - | V |
| | (VREFHL/R) – (VREFLL/R) | ΔVREF | AVDD-0.5 | - | AVDD | V |

Note 2. All voltages with respect to ground.
Note 6. AVDD and DVDD are powered up simultaneously.
Note 7. VREFHL pin, VREFHR pin
Note 8. VREFLL pin, VREFLR pin
Note 9. VREFLL and VREFLR pins must be connected to AVSS.
Analog input voltage scales with voltage of {(VREFH) – (VREFL)}.
Vin (typ.) = ±2.8 x {(VREFH) – (VREFL)} / 5 [V]

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

## 8. Electrical Characteristics

### ■ Analog Characteristics

(Ta = 25°C; AVDD=5.0V; DVDD=3.3V; AVSS=DVSS=0V; VREFHL=VREFHR=AVDD, VREFLL=VREFLR=AVSS; fs=48kHz, 96kHz, 192kHz; BICK=64fs; Signal Frequency=1kHz; 32bit Data; Measurement frequency=10Hz~20kHz at fs=48kHz, 40Hz~40kHz at fs=96kHz, 80Hz~80kHz at fs=192kHz; External circuit: Figure 41 "Analog input buffer circuit example 2"; unless otherwise specified)

| Parameter | | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Resolution | | | | | 32 | Bits |
| **Analog Input Characteristics:** | | | | | | |
| S/(N+D) | fs=48kHz<br>BW=20kHz | -1dBFS<br>-1dBFS (Note 10)<br>-2dBFS (Note 10)<br>-20dBFS<br>-60dBFS | 92<br>-<br>-<br>-<br>- | 100<br>108<br>110<br>102<br>64 | | dB<br>dB<br>dB<br>dB |
| | fs=96kHz<br>BW=40kHz | -1dBFS<br>-1dBFS (Note 10)<br>-20dBFS<br>-60dBFS | 92<br>-<br>-<br>- | 99<br>107<br>99<br>60 | | dB<br>dB<br>dB |
| | fs=192kHz<br>BW=80kHz | -1dBFS<br>-1dBFS (Note 10)<br>-20dBFS<br>-60dBFS | 91<br>-<br>-<br>- | 99<br>106<br>94<br>54 | | dB<br>dB<br>dB |
| Dynamic Range (-60dBFS with A-weighted)<br>(Stereo Mode)<br>(Mono Mode) | | | <br>122<br>125 | <br>127<br>130 | | <br>dB<br>dB |
| S/N (A-weighted) fs=48kHz<br>(Stereo Mode)<br>(Mono Mode) | | | <br>122<br>125 | <br>127<br>130 | | <br>dB<br>dB |
| S/N (Without A-weighted) fs=96kHz<br>(Stereo Mode) | | | <br>115 | <br>120 | | <br>dB |
| S/N (Without A-weighted) fs=192kHz<br>(Stereo Mode) | | | <br>111 | <br>116 | | <br>dB |
| Input Resistance | | | 650 | 720 | | Ω |
| Interchannel Isolation | | | 120 | 130 | | dB |
| Interchannel Gain Mismatch | | | | 0.1 | 0.5 | dB |
| Gain Drift | | | | 150 | | ppm/°C |
| Input Voltage (Note 11) | | | ±2.6 | ±2.8 | ±3.0 | Vpp |
| Input DC Bias Voltage | | | | 0.382 × AVDD | | Vpp |
| **Power Supplies:** | | | | | | |
| Power Supply Current<br>AVDD + VREFHL + VREFHR<br>DVDD (fs=48kHz, MSN=H, SDM1=L, SDM2=H)<br>(fs=96kHz, MSN=H, SDM1=L, SDM2=L)<br>(fs=192kHz, MSN=H, SDM1=L, SDM2=L)<br>(fs=384kHz, MSN=H, SDM1=L, SDM2=L)<br>(fs=768kHz, MSN=H, SDM1=L, SDM2=L) | | | | <br>74.6<br>24<br>52<br>53<br>34<br>34 | <br>94.0<br>33<br>71<br>72<br>46<br>46 | <br>mA<br>mA<br>mA<br>mA<br>mA<br>mA |
| Power down current (AVDD + DVDD) | | | | 10 | 100 | uA |
| Power Supply Rejection (Note 12) | | | - | 50 | - | dB |

Note 10. Using the circuit as shown in Figure 40(Analog input buffer circuit example 1)

Note 11. This value is (LIN+) – (LIN-) and (RIN+) - (RIN-). Input voltage is proportional to a difference between VREFP and VREFL voltages.

Vin (typ.) = ±2.8 x {(VREFH) – (VREFL)} / 5 [V]

Note 12. PSRR is applied to AVDD and DVDD with 1kHz, 20mVpp. The VREFHL/R and VREFLL/R pins held a constant voltage.

## ■ Sharp Roll-Off Filter Characteristics

(1) Sharp Roll-Off Filter Characteristics (fs=48kHz)
(Ta=25°C; AVDD=4.75~5.25V; DVDD=3.0~3.6V; fs=48kHz)

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **ADC Digital Filter (Decimation LPF):** | | | | | | |
| Passband (Note 13) Figure 3-(1) | | PB | 0 | | 21.82 | kHz |
| Passband Ripple (Note 14) Figure 3-(3) | | PR | -0.00015 | | +0.00010 | dB |
| Frequency Response (Note 14) | -0.001dB | FR | - | 21.93 | - | kHz |
| | -0.1dB | | - | 22.54 | - | kHz |
| | -3.0dB | | - | 23.62 | - | kHz |
| | -6.0dB | | - | 23.99 | - | kHz |
| Stopband (Note 14) Figure 3-(2) | | SB | 26.17 | | 3072 | kHz |
| Stopband Attenuation Figure 3-(4) | | SA | 100 | | | dB |
| Group Delay Distortion | | ΔGD | | 0 | | 1/fs |
| Group Delay (Note 15) | | GD | | 41.5 | | 1/fs |
| **ADC Digital Filter (HPF):** | | | | | | |
| Frequency response (Note 14) | -3dB | FR | - | 0.93 | - | Hz |
| | -0.1dB | | - | 6.1 | - | Hz |

(2) Sharp Roll-Off Filter Characteristics (fs=96kHz)
(Ta=25°C; AVDD=4.75~5.25V; DVDD=3.0~3.6V; fs=96kHz)

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **ADC Digital Filter (Decimation LPF):** | | | | | | |
| Passband (Note 13) Figure 4-(1) | | PB | 0 | | 43.62 | kHz |
| Pass Band Ripple (Note 14) Figure 4-(3) | | PR | -0.00015 | | +0.00015 | dB |
| Frequency Response (Note 14) | -0.001dB | FR | - | 43.87 | - | kHz |
| | -0.1dB | | - | 45.10 | - | kHz |
| | -3.0dB | | - | 47.25 | - | kHz |
| | -6.0dB | | - | 47.99 | - | kHz |
| Stopband (Note 14) Figure 4-(2) | | SB | 52.36 | | 3072 | kHz |
| Stopband Attenuation Figure 4-(4) | | SA | 100 | | | dB |
| Group Delay Distortion | | ΔGD | | 0 | | 1/fs |
| Group Delay (Note 15) | | GD | | 41.4 | | 1/fs |
| **ADC Digital Filter (HPF):** | | | | | | |
| Frequency response (Note 14) | -3dB | FR | - | 0.93 | - | Hz |
| | -0.1dB | | - | 6.1 | - | Hz |

(3) Sharp Roll-Off Filter Characteristics (fs=192kHz)
(Ta=25°C; AVDD=4.75~5.25V; DVDD=3.0~3.6V; fs=192kHz)

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **ADC Digital Filter (Decimation LPF):** | | | | | | |
| Passband (Note 13) Figure 5-(1) | | PB | 0 | | 87.32 | kHz |
| PassBand Ripple (Note 14) Figure 5-(2) | | PR | -0.005 | | +0.006 | dB |
| Frequency Response (Note 14) | -0.1dB | FR | - | 89.52 | - | kHz |
| | -3.0dB | | - | 94.33 | - | kHz |
| | -6.0dB | | - | 95.97 | - | kHz |
| Stopband (Note 14) Figure 5-(3) | | SB | 105.60 | | 3072 | kHz |
| Stopband Attenuation Figure 5-(4) | | SA | 100 | | | dB |
| Group Delay Distortion | | ΔGD | | 0 | | 1/fs |
| Group Delay (Note 15) | | GD | | 36.3 | | 1/fs |
| **ADC Digital Filter (HPF):** | | | | | | |
| Frequency response (Note 14) | -3dB | FR | - | 0.93 | - | Hz |
| | -0.1dB | | - | 6.1 | - | Hz |

(4) Sharp Roll-Off Filter Characteristics (fs=384kHz)
(Ta=25°C; AVDD=4.75~5.25V; DVDD=3.0~3.6V; fs=384kHz)

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **ADC Digital Filter (Decimation LPF):** | | | | | | |
| Frequency Response (Note 14) | -0.1dB | FR | 0 | 60.67 | - | kHz |
| | -1.0B | | - | 86.93 | - | kHz |
| | -3.0dB | | - | 107.70 | - | kHz |
| | -6.0dB | | - | 125.30 | - | kHz |
| Stopband (Note 14) Figure 6-(1) | | SB | 223.93 | | 3072 | kHz |
| Stopband Attenuation Figure 6-(2) | | SA | 83 | | | dB |
| Group Delay Distortion | | ΔGD | | 0 | | 1/fs |
| Group Delay (Note 15) | | GD | | 10.6 | | 1/fs |

(5) Sharp Roll-Off Filter Characteristics (fs=768kHz)
(Ta=25°C; AVDD=4.75~5.25V; DVDD=3.0~3.6V; fs=768kHz)

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **ADC Digital Filter (Decimation LPF):** | | | | | | |
| Frequency Response (Note 14) | -0.1dB | FR | 0 | 34.01 | - | kHz |
| | -1.0dB | | - | 101.51 | - | kHz |
| | -3.0dB | | - | 163.13 | - | kHz |
| | -6.0dB | | - | 216.16 | - | kHz |
| Stopband (Note 14) Figure 7-(1) | | | 533.42 | | 3072 | KHz |
| Stopband Attenuation Figure 7-(2) | | | 85 | | | dB |
| Group Delay Distortion | | ΔGD | | 0 | | 1/fs |
| Group Delay (Note 15) | | GD | | 8.4 | | 1/fs |

Note 13. The definition of Passband is applied to the frequency which is within the limits of Passband Ripple.
Note 14. The passband and stopband frequencies scales with fs. The reference frequency of these responses is 1kHz.
Note 15. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the setting of 32bit data both of channels to the ADC output register for ADC.

## ■ Short Delay Filter Characteristics

(1) Short Delay Filter Characteristics (fs=48kHz)
(Ta=25°C; AVDD=4.75~5.25V; DVDD=3.0~3.6V; fs=48kHz; SDFIL="L")

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **ADC Digital Filter (Decimation LPF):** | | | | | | |
| Passband (Note 13) Figure 8-(1) | | PB | 0 | | 22.22 | kHz |
| Passband Ripple (Note 14) Figure 8-(2) | | PR | -0.015 | | +0.055 | dB |
| Frequency Response (Note 14) | -0.1dB | FR | - | 22.40 | - | kHz |
| | -3.0dB | | - | 23.70 | - | kHz |
| | -6.0dB | | - | 24.28 | - | kHz |
| Stopband (Note 14) Figure 8-(3) | | SB | 27.93 | | 3072 | kHz |
| Stopband Attenuation Figure 8-(4) | | SA | 93 | | | dB |
| Group Delay Distortion | | ΔGD | | | ±0.1 | 1/fs |
| Group Delay (Note 15) | | GD | | 12.5 | | 1/fs |
| **ADC Digital Filter (HPF):** | | | | | | |
| Frequency response (Note 14) | -3dB | FR | - | 0.93 | - | Hz |
| | -0.1dB | | - | 6.1 | - | Hz |

(2) Short Delay Filter Characteristics (fs=96kHz)
(Ta=25°C; AVDD=4.75~5.25V; DVDD=3.0~3.6V; fs=96kHz; SDFIL="L")

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **ADC Digital Filter (Decimation LPF):** | | | | | | |
| Passband (Note 13) Figure 9-(1) | | PB | 0 | | 44.46 | kHz |
| Passband Ripple (Note 14) Figure 9-(2) | | PR | -0.05 | | +0.02 | dB |
| Frequency Response (Note 14) | -0.1dB | FR | - | 44.68 | - | kHz |
| | -3.0dB | | - | 47.40 | - | kHz |
| | -6.0dB | | - | 48.56 | - | kHz |
| Stopband (Note 14) Figure 9-(3) | | SB | 55.90 | | 3072 | kHz |
| Stopband Attenuation Figure 9-(4) | | SA | 93 | | | dB |
| Group Delay Distortion | | ΔGD | | | ±0.075 | 1/fs |
| Group Delay (Note 15) | | GD | | 12.4 | | 1/fs |
| **ADC Digital Filter (HPF):** | | | | | | |
| Frequency response (Note 14) | -3dB | FR | - | 0.93 | - | Hz |
| | -0.1dB | | - | 6.1 | - | Hz |

(3) Short Delay Filter Characteristics (fs=192kHz)
(Ta=25°C; AVDD=4.75~5.25V; DVDD=3.0~3.6V; fs=192kHz; SDFIL="L")

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **ADC Digital Filter (Decimation LPF):** | | | | | | |
| Passband (Note 13) Figure 10-(1) | | PB | 0 | | 80.71 | kHz |
| Passband Ripple (Note 14) Figure 10-(2) | | PR | -0.05 | | +0.02 | dB |
| Frequency Response (Note 14) | -0.1dB | PB | - | 82.5 | - | kHz |
| | -3.0dB | | - | 92.86 | - | kHz |
| | -6.0dB | | - | 96.31 | - | kHz |
| Stopband (Note 14) Figure 10-(3) | | SB | 116.67 | | 3072 | kHz |
| Stopband Attenuation Figure 10-(4) | | SA | 93 | | | dB |
| Group Delay Distortion | | ΔGD | | | ±0.02 | 1/fs |
| Group Delay (Note 15) | | GD | | 12.2 | | 1/fs |
| **ADC Digital Filter (HPF):** | | | | | | |
| Frequency response (Note 14) | -3dB | FR | - | 0.93 | - | Hz |
| | -0.1dB | | - | 6.1 | - | Hz |

Note 13. The definition of Passband is applied to the frequency which is within the limits of Passband Ripple.
Note 14. The passband and stopband frequencies scales with fs. The reference frequency of these responses is 1kHz.
Note 15. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the setting of 32bit data both of channels to the ADC output register for ADC.

## ■ Minimum Phase Filter Characteristics

(1) Minimum Phase Filter Characteristics (fs=48kHz)
(Ta=25°C; AVDD=4.75~5.25V; DVDD=3.0~3.6V; fs=48kHz; SDFIL="H")

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **ADC Digital Filter (Decimation LPF):** | | | | | | |
| Passband (Note 13) Figure 11-(1) | | PB | 0 | | 21.75 | kHz |
| Passband Ripple (Note 14) Figure 11-(2) | | PR | -0.02 | | +0.04 | dB |
| Frequency Response (Note 14) | -0.1dB | FR | - | 21.97 | - | kHz |
| | -3.0dB | | - | 23.49 | - | kHz |
| | -6.0dB | | - | 24.12 | - | kHz |
| Stopband (Note 14) Figure 11-(3) | | SB | 27.97 | | 3072 | kHz |
| Stopband Attenuation Figure 11-(4) | | SA | 93 | | | dB |
| Group Delay Distortion | | ΔGD | | | ±1.5 | 1/fs |
| Group Delay (Note 15) | | GD | | 3.5 | | 1/fs |
| **ADC Digital Filter (HPF):** | | | | | | |
| Frequency response (Note 14) | -3dB | FR | - | 0.93 | - | Hz |
| | -0.1dB | | - | 6.1 | - | Hz |

(2) Minimum Phase Filter Characteristics (fs=96kHz)
(Ta=25°C; AVDD=4.75~5.25V; DVDD=3.0~3.6V; fs=96kHz; SDFIL="H")

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **ADC Digital Filter (Decimation LPF):** | | | | | | |
| Passband (Note 13) Figure 12-(1) | | PB | 0 | | 43.55 | kHz |
| Passband Ripple (Note 14) Figure 12-(2) | | PR | -0.04 | | +0.02 | dB |
| Frequency Response (Note 14) | -0.1dB | FR | - | 43.87 | - | kHz |
| | -3.0dB | | - | 46.98 | - | kHz |
| | -6.0dB | | - | 48.26 | - | kHz |
| Stopband (Note 14) Figure 12-(3) | | SB | 55.96 | | 3072 | kHz |
| Stopband Attenuation Figure 12-(4) | | SA | 93 | | | dB |
| Group Delay Distortion | | ΔGD | | | ±1.5 | 1/fs |
| Group Delay (Note 15) | | GD | | 3.4 | | 1/fs |
| **ADC Digital Filter (HPF):** | | | | | | |
| Frequency response (Note 14) | -3dB | FR | - | 0.93 | - | Hz |
| | -0.1dB | | - | 6.1 | - | Hz |

(3) Minimum Phase Filter Characteristics (fs=192kHz)
(Ta=25°C; AVDD=4.75~5.25V; DVDD=3.0~3.6V; fs=192kHz; SDFIL="H")

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **ADC Digital Filter (Decimation LPF):** | | | | | | |
| Passband (Note 13) Figure 13-(1) | | PB | 0 | | 80.97 | kHz |
| Passband Ripple (Note 14) Figure 13-(2) | | PR | -0.045 | | +0.015 | dB |
| Frequency Response (Note 14) | -0.1dB | FR | - | 82.55 | - | kHz |
| | -3.0dB | | - | 92.02 | | kHz |
| | -6.0dB | | - | 95.44 | - | kHz |
| Stopband (Note 14) Figure 13-(3) | | SB | 115.57 | | 3072 | kHz |
| Stopband Attenuation Figure 13-(4) | | SA | 93 | | | dB |
| Group Delay Distortion | | ΔGD | | | ±1.6 | 1/fs |
| Group Delay (Note 15) | | GD | | 4.2 | | 1/fs |
| **ADC Digital Filter (HPF):** | | | | | | |
| Frequency response (Note 14) | -3dB | FR | - | 0.93 | - | Hz |
| | -0.1dB | | - | 6.1 | - | Hz |

Note 13. The definition of Passband is applied to the frequency which is within the limits of Passband Ripple.
Note 14. The passband and stopband frequencies scales with fs. The reference frequency of these responses is 1kHz.
Note 15. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the setting of 32bit data both of channels to the ADC output register for ADC.

## ■ Digital Filter Plot

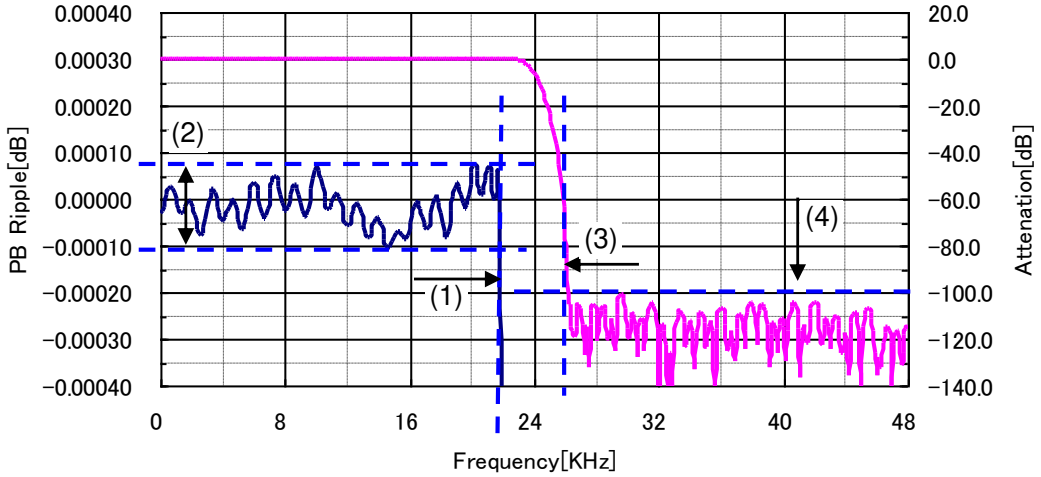



Figure 3. Sharp Roll Off Filter Normal Mode

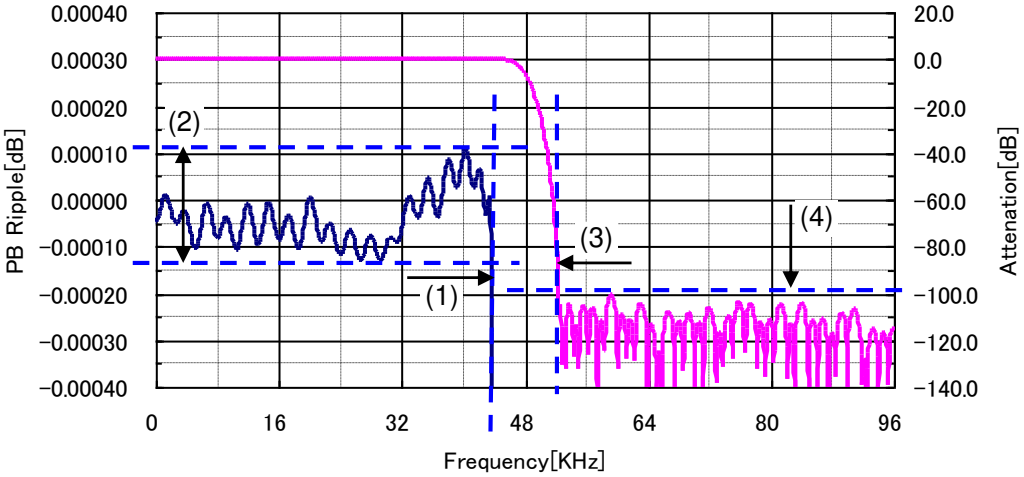



Figure 4. Sharp Roll Off Filter Double Mode

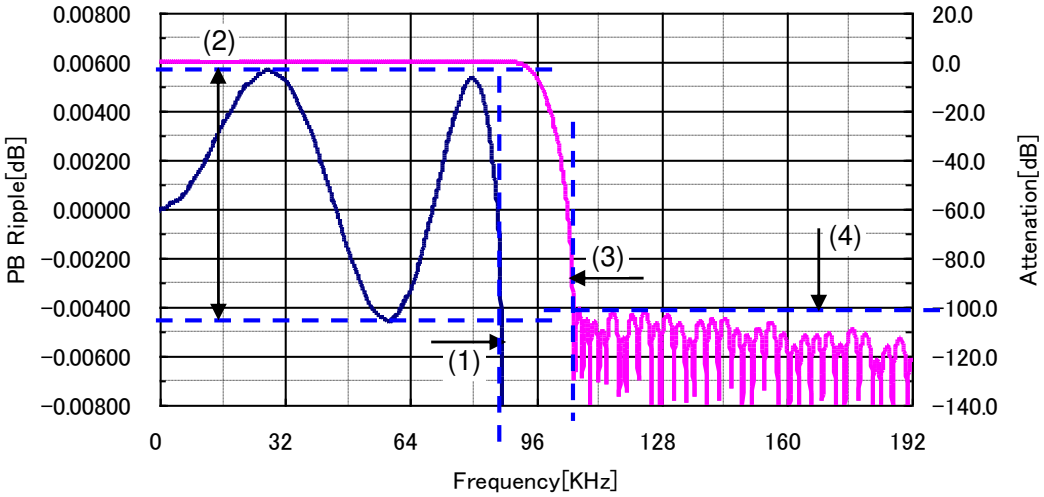



Figure 5. Sharp Roll Off Filter Quad Mode

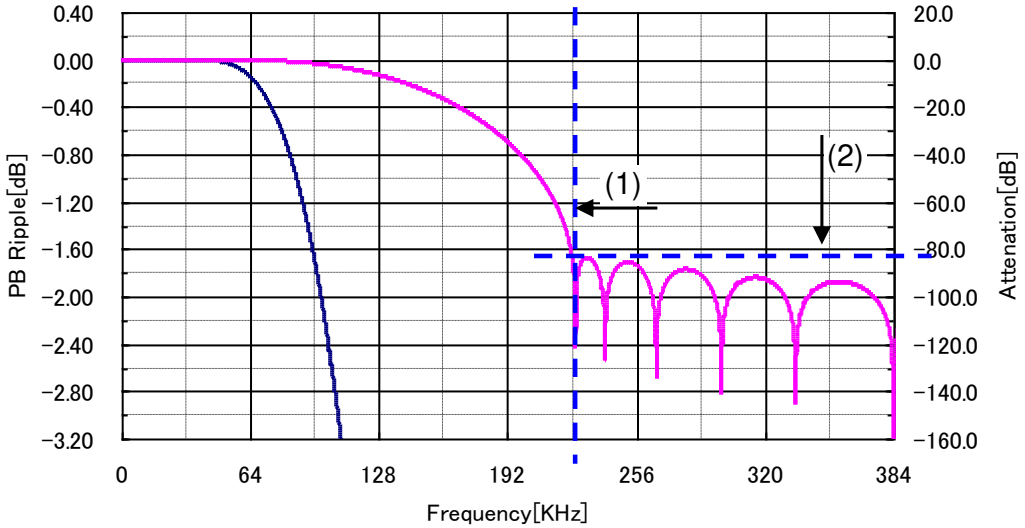



Figure 6. Sharp Roll Off Filter Octal Mode

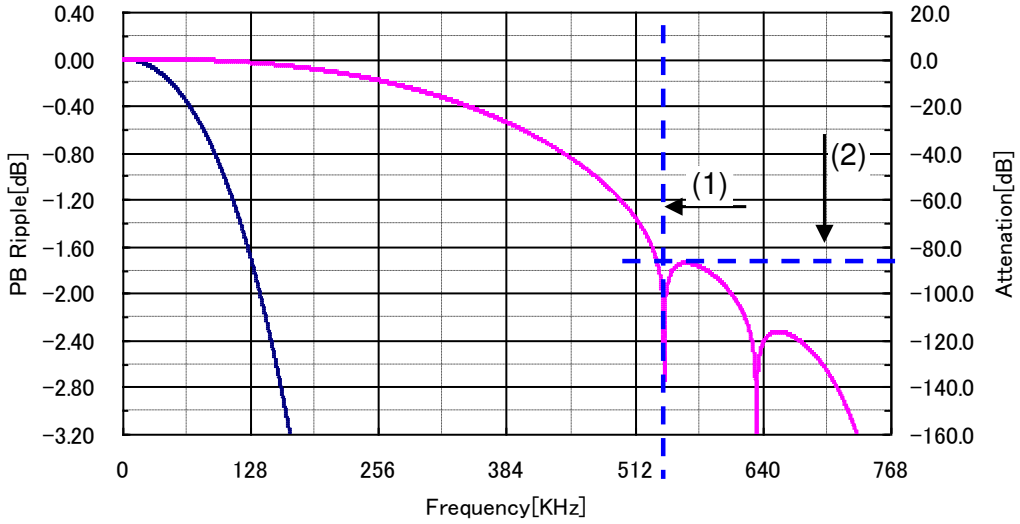



Figure 7. Sharp Roll Off Filter Hex Mode

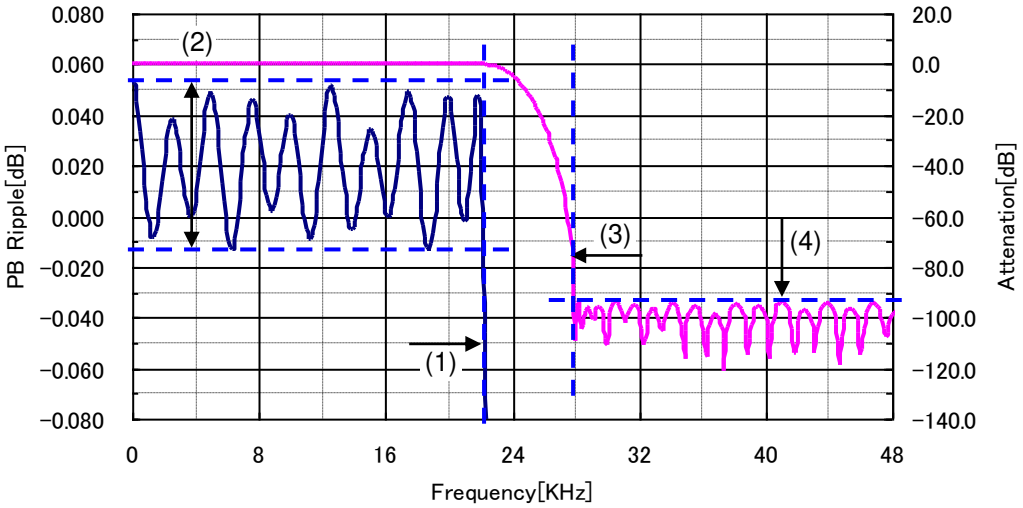



Figure 8 Short Delay Filter Normal Mode

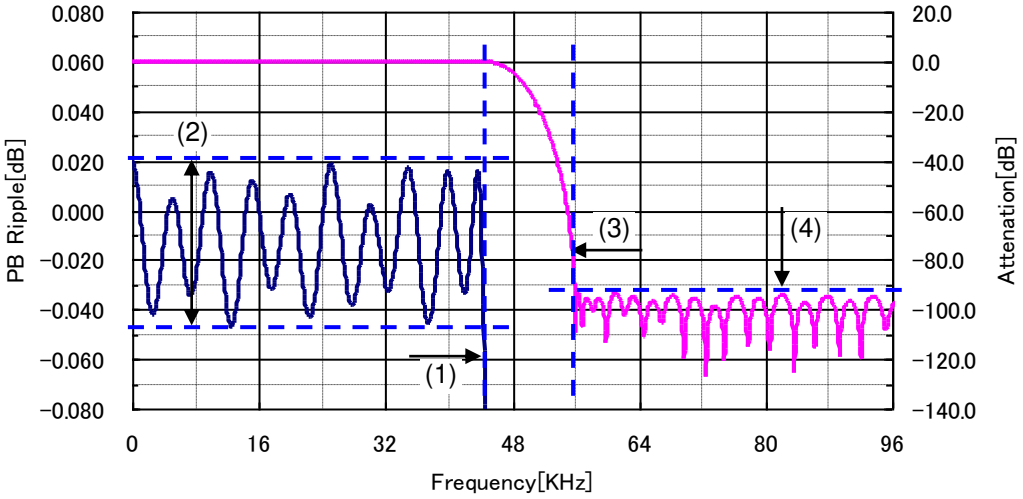



Figure 9. Short Delay Filter Double Mode

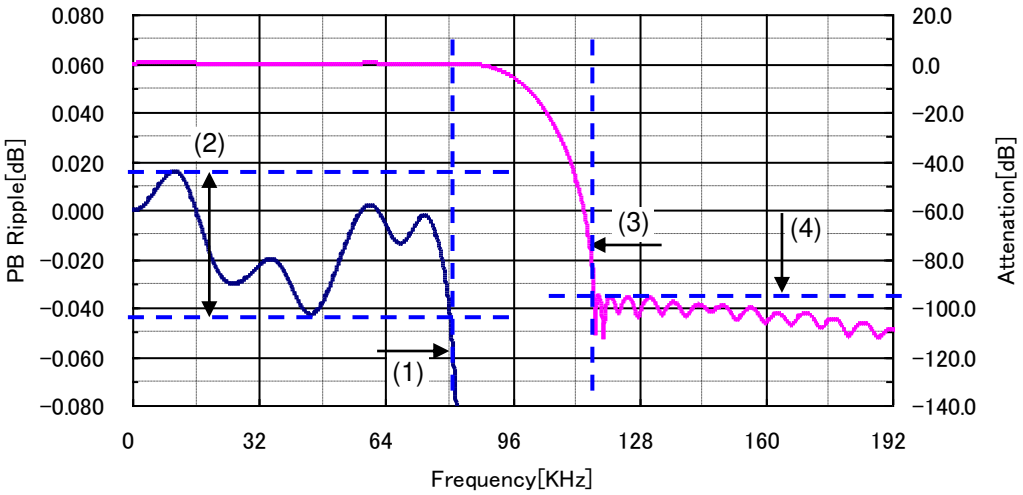



Figure 10. Short Delay Filter Quad Mode

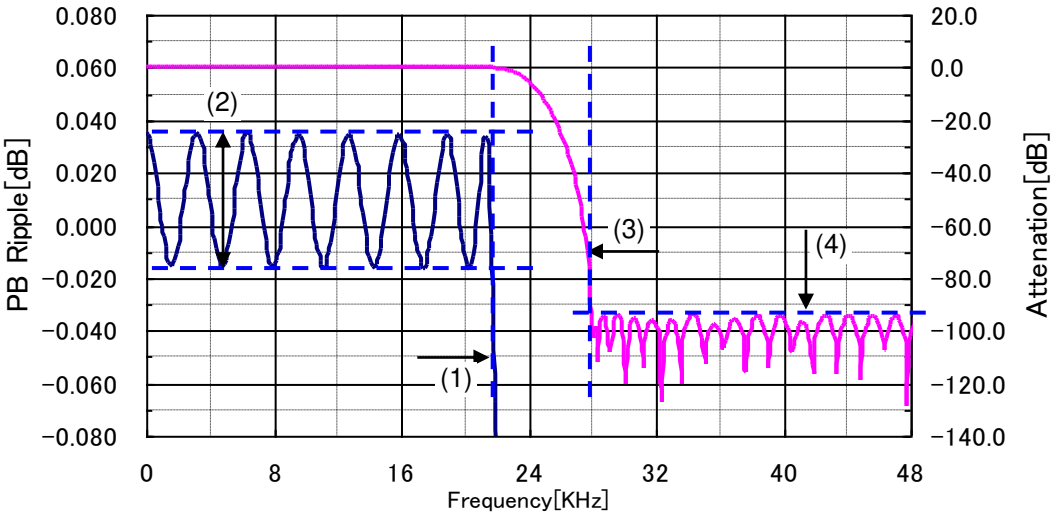



Figure 11. Minimum Phase Filter Normal Mode

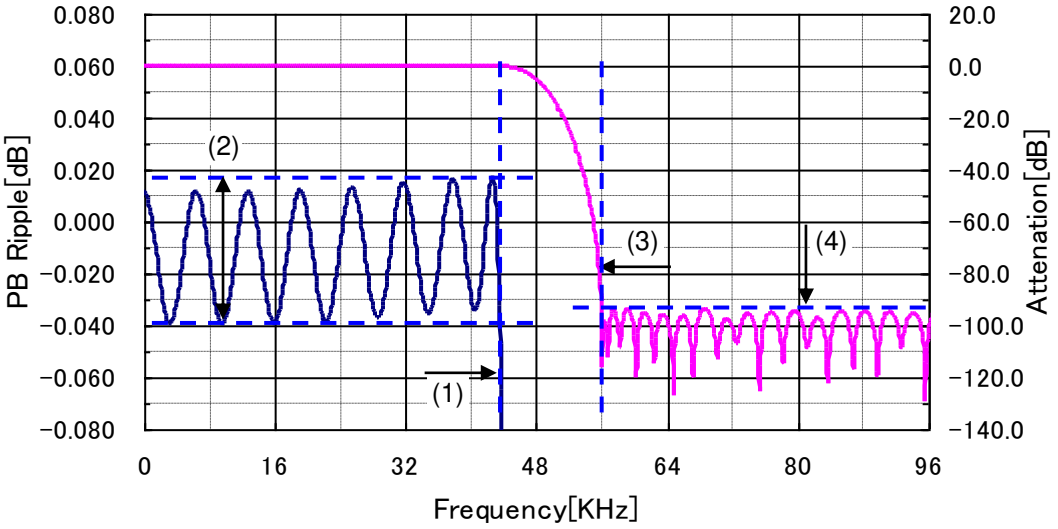



Figure 12. Minimum Phase Filter Double Mode

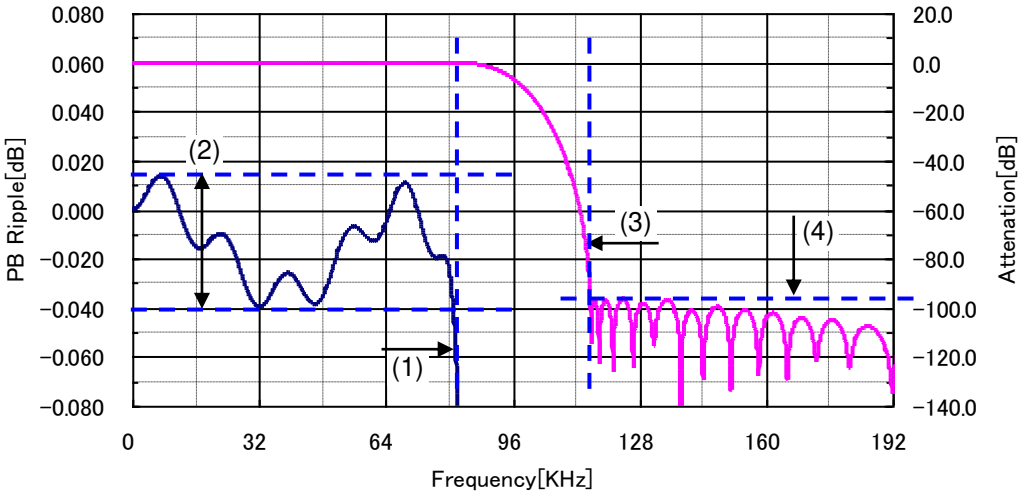



Figure 13. Minimum Phase Filter Quad Mode

## ■ DC Characteristics

(Ta= -10~70°C; AVDD=4.75~5.25V; DVDD=3.0~3.6V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| High-Level Input Voltage (Note 5) | VIH | 70%DVDD | - | - | V |
| Low-Level Input Voltage (Note 5) | VIL | - | - | 30%DVDD | V |
| High-Level Output Voltage (Iout=-100μA) | VOH | DVDD−0.5 | - | - | V |
| Low-Level Output Voltage (Iout= 100μA) | VOL | - | | 0.5 | V |
| Input Leakage Current | Iin | - | - | ±10 | μA |

Note 5. CKS0, CKS1, CKS2,PDN, SDM1, SDM2, SDFIL, TDMIN1, TDMIN2, MCLK, BICK, LRCK, DIF, MSN, HPFE, MONO, TDM0, TDM1pin

## ■ Switching Characteristics

(Ta= -10~70°C; AVDD=4.75~5.25V; DVDD=3.0~3.6V; $C_L$=20pF)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Master Clock Timing** | | | | | |
| Frequency | fCLK | 2.048 | 12.288 | 24.576 | MHz |
| Pulse Width Low | tCLKL | 0.4/fCLK | | | ns |
| Pulse Width High | tCLKH | 0.4/fCLK | | | ns |
| **LRCK Timing (Slave Mode)** | | | | | |
| **Normal mode (TDM1="L", TDM0="L")** | | | | | |
| LRCK Frequency | fs | 8 | | 768 | kHz |
| Duty Cycle | Duty | 45 | | 55 | % |
| **TDM256 MODE (TDM1="L", TDM0="H")** | | | | | |
| LRCK Frequency | fs | 8 | | 48 | kHz |
| "H" time | tLRH | 1/256fs | | | ns |
| "L" time | tLRL | 1/256fs | | | ns |
| **TDM128 MODE (TDM1="H", TDM0="H")** | | | | | |
| LRCK Frequency | fs | 8 | | 192 | kHz |
| "H" time | tLRH | 1/128fs | | | ns |
| "L" time | tLRL | 1/128fs | | | ns |
| **LRCK Timing (Master Mode)** | | | | | |
| **Normal mode (TDM1="L", TDM0="L")** | | | | | |
| LRCK Frequency | fs | 8 | | 768 | kHz |
| Duty Cycle | Duty | | 50 | | % |
| **TDM256 MODE (TDM1="L", TDM0="H")** | | | | | |
| LRCK Frequency | fs | 8 | | 48 | kHz |
| "H" time (Note 16) | tLRH | | 1/8fs | | ns |
| **TDM128 MODE (TDM1="H", TDM0="H")** | | | | | |
| LRCK Frequency | fs | 8 | | 192 | kHz |
| "H" time (Note 16) | tLRH | | 1/4fs | | ns |

Note 16. "L" time at $I^2S$ format.

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Audio Interface Timing (Slave mode)** | | | | | |
| **Normal mode (TDM1="L", TDM0="L")** | | | | | |
| **(8KHz≦fs≦192KHz)** | | | | | |
| BICK Period (8kHz ≤ fs ≤48kHz) | tBCK | 1/128fs | | | ns |
| (48kHz < fs ≤ 192kHz) | tBCK | 1/64fs | | | ns |
| BICK Pulse Width Low | tBCKL | 32 | | | ns |
| Pulse Width High | tBCKH | 32 | | | ns |
| LRCK Edge to BICK "↑" (Note 17) | tLRB | 20 | | | ns |
| BICK "↑" to LRCK Edge (Note 17) | tBLR | 20 | | | ns |
| LRCK to SDTO1/2 (MSB) (Except $I^2S$ mode) | tLRS | | | 20 | ns |
| BICK "↓" to SDTO1/2 | tBSD | | | 20 | ns |
| **Normal mode (TDM1="L", TDM0="L")** | | | | | |
| **(192KHz≦fs≦768KHz)** | | | | | |
| **BICK Period (192kHz ≤ fs ≤384kHz)** | tBCK | 1/64fs | | | ns |
| **(384kHz < fs ≤ 768kHz)** | tBCK | 1/32fs | | | ns |
| BICK Pulse Width Low | tBCKL | 16 | | | ns |
| Pulse Width High | tBCKH | 16 | | | ns |
| LRCK Edge to BICK "↑" (Note 17) | tLRB | 10 | | | ns |
| BICK "↑" to LRCK Edge (Note 17) | tBLR | 10 | | | ns |
| BICK "↓" to SDTO1/2 | tBSD | | | 10 | ns |
| **TDM256 mode (TDM1="L", TDM0="H")** | | | | | |
| BICK Period | tBCK | 1/256fs | | | ns |
| BICK Pulse Width Low | tBCKL | 32 | | | ns |
| Pulse Width High | tBCKH | 32 | | | ns |
| LRCK Edge to BICK "↑" (Note 17) | tLRB | 20 | | | ns |
| BICK "↑" to LRCK Edge (Note 17) | tBLR | 20 | | | ns |
| BICK "↓" to SDTO1/2 | tBSD | | | 20 | ns |
| TDMIN1/2 Setup Time | tTDS | 10 | | | ns |
| TDMIN1/2 Hold Time | tTDH | 10 | | | ns |
| **TDM128 mode (TDM1="H", TDM0="H")** | | | | | |
| **(8kHz ≤ fs ≤ 96kHz)** | | | | | |
| BICK Period | tBCK | 1/128fs | | | ns |
| BICK Pulse Width Low | tBCKL | 32 | | | ns |
| Pulse Width High | tBCKH | 32 | | | ns |
| LRCK Edge to BICK "↑" (Note 17) | tLRB | 20 | | | ns |
| BICK "↑" to LRCK Edge (Note 17) | tBLR | 20 | | | ns |
| BICK "↓" to SDTO1/2 | tBSD | | | 20 | ns |
| TDMIN1/2 Setup Time | tTDS | 10 | | | ns |
| TDMIN1/2 Hold Time | tTDH | 10 | | | ns |
| **TDM128 mode (TDM1="H", TDM0="H")** | | | | | |
| **(96kHz < fs ≤ 192kHz)** | | | | | |
| BICK Period | tBCK | 1/128fs | | | ns |
| BICK Pulse Width Low | tBCKL | 16 | | | ns |
| Pulse Width High | tBCKH | 16 | | | ns |
| LRCK Edge to BICK "↑" (Note 17) | tLRB | 10 | | | ns |
| BICK "↑" to LRCK Edge (Note 17) | tBLR | 10 | | | ns |
| BICK "↓" to SDTO1/2 | tBSD | | | 10 | ns |
| TDMIN1/2 Setup Time | tTDS | 10 | | | ns |
| TDMIN1/2 Hold Time | tTDH | 10 | | | ns |

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Audio Interface Timing (Master mode)** | | | | | |
| **Normal mode (TDM1="L", TDM0="L")** | | | | | |
| BICK Frequency (8kHz ≤ fs ≤ 192kHz) | fBCK | | 64fs | | Hz |
| (192kHz < fs ≤ 384kHz) | fBCK | | 32fs | | Hz |
| BICK Duty | dBCK | | 50 | | % |
| BICK "↓" to LRCK | tMBLR | –12 | | 12 | ns |
| BICK "↓" to SDTO1/2 | tBSD | –20 | | 20 | ns |
| **Normal mode (TDM1="L", TDM0="L") (384KHz < fs ≦ 768KHz)** | | | | | Hz |
| BICK Frequency | fBCK | | 32fs | | Hz |
| BICK Duty | dBCK | | 50 | | % |
| BICK "↓" to LRCK | tMBLR | –6 | | 6 | ns |
| BICK "↓" to SDTO1/2 | tBSD | –10 | | 10 | ns |
| **TDM256 mode (TDM1="L", TDM0="H")** | | | | | |
| BICK Frequency | fBCK | | 256fs | | Hz |
| BICK Duty (Note 18) | dBCK | | 50 | | % |
| BICK "↓" to LRCK | tMBLR | –12 | | 12 | ns |
| BICK "↓" to SDTO1/2 | tBSD | –20 | | 20 | ns |
| TDMIN1/2 Setup Time | tTDS | 10 | | | ns |
| TDMIN1/2 Hold Time | tTDH | 10 | | | ns |
| **TDM128 mode (TDM1="H", TDM0="H") (8kHz ≤ fs ≤ 96kHz)** | | | | | |
| BICK Frequency | fBCK | | 128fs | | Hz |
| BICK Duty | dBCK | | 50 | | % |
| BICK "↓" to LRCK | tMBLR | –12 | | 12 | ns |
| BICK "↓" to SDTO1/2 | tBSD | –20 | | 20 | ns |
| TDMIN1/2 Setup Time | tTDS | 10 | | | ns |
| TDMIN1/2 Hold Time | tTDH | 10 | | | ns |
| **TDM128 mode (TDM1="H", TDM0="H") (96kHz < fs ≤ 192kHz)** | | | | | |
| BICK Frequency | fBCK | | 128fs | | Hz |
| BICK Duty | dBCK | | 50 | | % |
| BICK "↓" to LRCK | tMBLR | –6 | | 6 | ns |
| BICK "↓" to SDTO1/2 | tBSD | –10 | | 10 | ns |
| TDMIN1/2 Setup Time | tTDS | 10 | | | ns |
| TDMIN1/2 Hold Time | tTDH | 10 | | | ns |
| **Reset timing** | | | | | |
| RSTN Pulse width | tRTW | 150 | | | ns |

Note 17. BICK rising edge must not occur at the same time as LRCK edge.
Note 18. This value is MCLK=512fs. Duty cycle is not guaranteed when MCLK=256fs.

## ■ Timing Diagrams

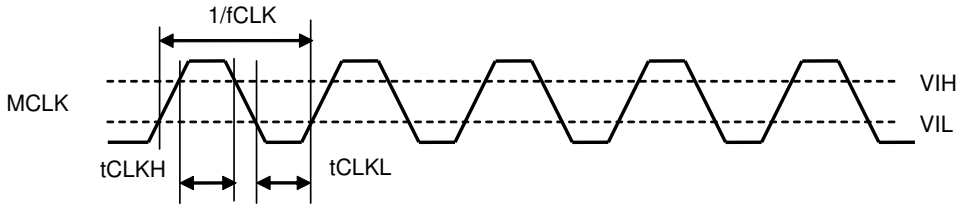



Figure 14. MCLK Timing (TDM0 pin = “L” or “H”)

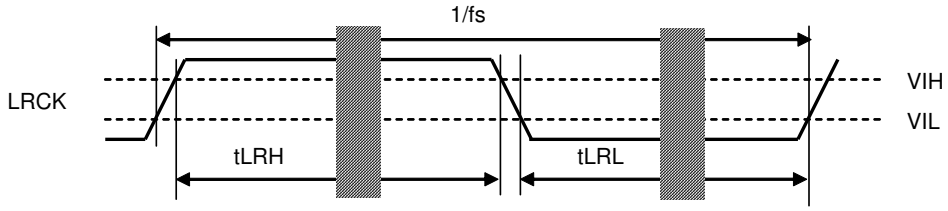



Figure 15. LRCK Timing (TDM0 pin = “L” or “H”)

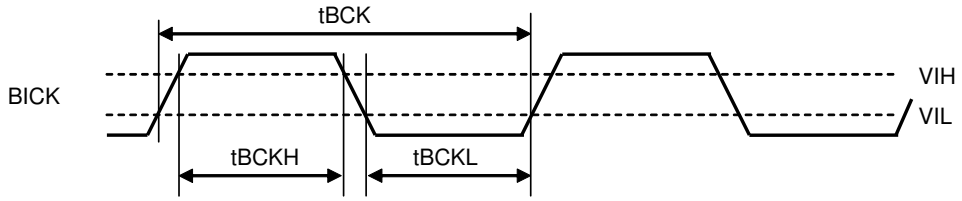



Figure 16.BICK Timing (TDM0 pin = “L” or “H”)

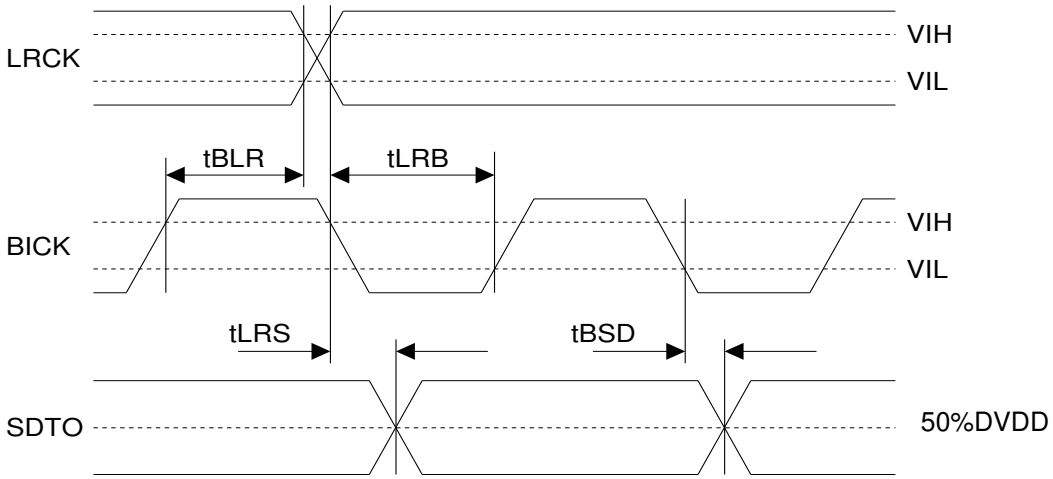



Figure 17. Audio Interface Timing (Slave mode, TDM0 pin = “L”)

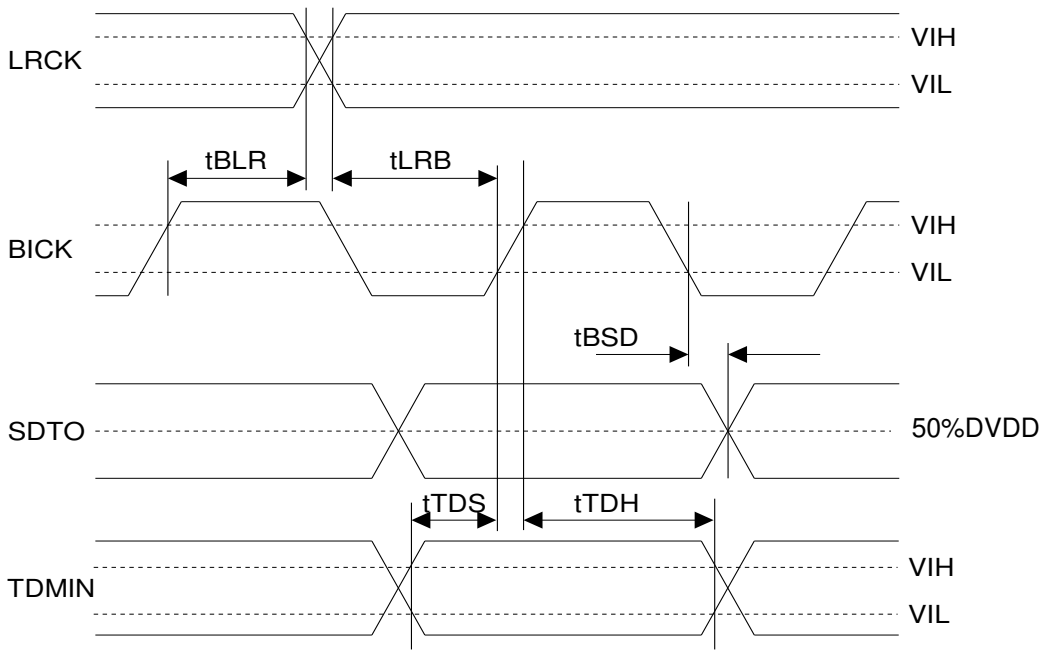



Figure 18. Audio Interface Timing (Slave mode, TDM0 pin = “H”)

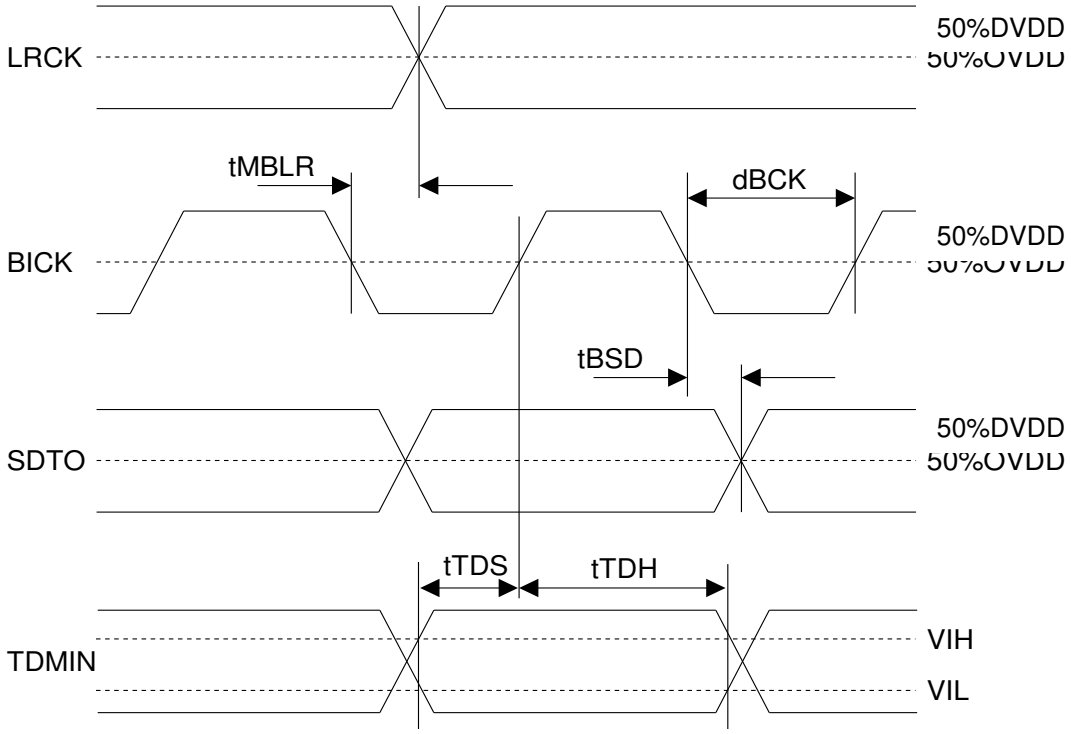



Figure 19. Audio Interface Timing (Master mode, TDM0 pin= “H” or “L”)

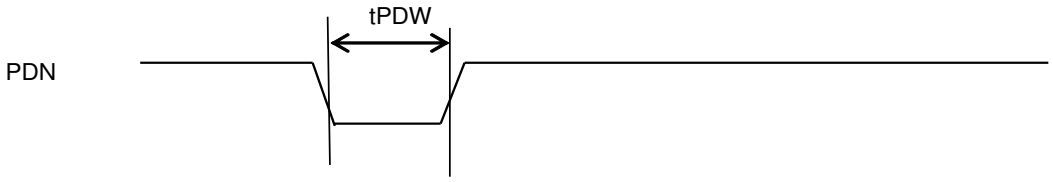



Figure 20. Reset & Calibration Timing

Note: SDTO shows SDTO1 and SDTO2. TDMIN shows TDMIN1 and TDMIN2.

# 9. Functional Descriptions

## ■ System Clock

MCLK, BICK and LRCK (fs) clocks are required in slave mode. A stable clock must be supplied when the AK5397 is in operation (PDN pin = “H”). The LRCK clock input must be synchronized with MCLK, however the phase is not critical. Table 1 shows the relationship of typical sampling frequency and the system clock frequency. MCLK frequency, BICK frequency and master/slave mode are selected by CKS2-0 and MSN pins as shown in Table 2.

The MSN pin controls Master/Slave mode switching. The AK5397 outputs BICK and LRCK in master mode when inputting MCLK. When the AK5397 is in slave mode, MCLK, BICK and LRCK should be input. (Table 4)

For synchronization between multiple devices, the AK5397 should be reset by the PDN pin after an operation clock change, clock mode switching, digital I/F change and Master/Slave mode switching. Clock and Mode changes should only be made during the reset.

| fs | MCLK | | | | |
|---|---|---|---|---|---|
| | 32fs | 64fs | 128fs | 256fs | 512fs |
| 32kHz | N/A | N/A | N/A | 8.192MHz | 16.384MHz |
| 44.1kHz | N/A | N/A | N/A | 11.2896MHz | 22.5792MHz |
| 48kHz | N/A | N/A | N/A | 12.288MHz | 24.576MHz |
| 96kHz | N/A | N/A | N/A | 24.576MHz | N/A |
| 192kHz | N/A | N/A | 24.576MHz | N/A | N/A |
| 384kHz | N/A | 24.576MHz | N/A | N/A | N/A |
| 768kHz | 24.576MHz | N/A | N/A | N/A | N/A |

Table 1. System Clock Example (N/A: Not Available)

| MSN pin | CKS2 pin | CKS1 pin | CKS0 pin | MCLK | BICK | Sampling Speed |
|---|---|---|---|---|---|---|
| L (Slave) | 0 | 0 | 0 | 256fs | 64fs ≤ BICK ≤ 128fs | Normal Speed Mode (8kHz ≤ fs ≤ 48kHz) |
| | 0 | 0 | 1 | (Table 3) | | Auto Setting Mode |
| | 0 | 1 | 0 | 256fs | 64fs | Double Speed Mode (48kHz < fs ≤ 96kHz) |
| | 0 | 1 | 1 | 128fs | 64fs | Quad Speed Mode (96kHz < fs ≤ 192kHz) |
| | 1 | 0 | 0 | 64fs | 64fs | Octal Speed Mode (fs = 384kHz) |
| | 1 | 0 | 1 | 32fs | 32fs | Hex Speed Mode (fs = 768kHz) |
| | 1 | 1 | 0 | N/A | | |
| | 1 | 1 | 1 | | | |
| H (Master) | 0 | 0 | 0 | 256fs | 64fs | Normal Speed Mode (8kHz ≤ fs ≤ 48kHz) |
| | 0 | 0 | 1 | 512fs | 64fs | |
| | 0 | 1 | 0 | 256fs | 64fs | Double Speed Mode (48kHz < fs ≤ 96kHz) |
| | 0 | 1 | 1 | 128fs | 64fs | Quad Speed Mode (96kHz < fs ≤ 192kHz) |
| | 1 | 0 | 0 | 64fs | 64fs | Octal Speed Mode (fs = 384kHz) |
| | 1 | 0 | 1 | 32fs | 32fs | Hex Speed Mode (fs = 768kHz) |
| | 1 | 1 | 0 | N/A | | |
| | 1 | 1 | 1 | | | |

Table 2. Setting of MCLK /BICK/Sampling Speed

| MCLK | BICK | Sampling Speed |
|---|---|---|
| 512fs | 64fs ≤ BICK ≤ 128fs | Normal Speed Mode (8kHz ≤ fs ≤ 48kHz) |
| 256fs | 64fs | Double Speed Mode (48kHz < fs ≤ 96kHz) |
| 128fs | 64fs | Quad Speed Mode (96kHz < fs ≤ 192kHz) |
| 64fs | 64fs | Octal Speed Mode (fs = 384kHz) |
| 32fs | 32fs | Hex Speed Mode (fs = 768kHz) |

Table 3. Auto Setting Mode (Slave Mode)

## ■ Master Mode/Slave Mode

The MSN pin selects either master or slave modes as shown in Table 4. The AK5397 outputs BICK and LRCK in master mode. In slave mode, provide MCLK, BICK and LRCK.

| MSN pin | Mode | BICK, LRCK |
|---|---|---|
| L | Slave Mode | BICK = Input<br>LRCK = Input |
| H | Master Mode | BICK = Output<br>LRCK = Output |

Table 4. Master mode/Slave mode

## ■ Audio Interface Format

12 types of audio data interface can be selected by the TDM1-0, MSN and DIF pins as shown in Table 5. The audio data format can be selected by the DIF pin. In all formats the serial data is MSB-first, 2's complement format. The SDTO1/2 is clocked out on the falling edge of BICK.

In normal mode, Mode 0-1 are the slave mode, and Mode 2-3 are the master mode. BICK frequency is shown in Table 2.

In TDM256 mode, BICK must be fixed to 256fs. In the slave mode, “H” time and “L” time of LRCK must be 1/256fs at least. In the master mode, “H” time (“L” time at $I^2S$ mode) of LRCK is 1/8fs typically. TDM256 mode supports only Normal Speed.

In TDM128 mode, BICK must be fixed to 128fs. In the slave mode, “H” time and “L” time of LRCK must be 1/128fs at least. In the master mode, “H” time (“L” time at $I^2S$ mode) of LRCK is 1/4fs typically. TDM128 mode supports Normal/Double/Quad Speed.

| TDM1 pin | TDM0 pin | MSN pin | DIF pin | Mode | | SDTO | LRCK | | BICK | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | I/O | | I/O |
| L | L | L (Slave) | L | 0 | Normal | 32bit, MSB justified | H/L | I | (Table 2) | I |
| | | | H | 1 | | 32bit, $I^2S$ Compatible | L/H | I | | I |
| | | H (Master) | L | 2 | | 32bit, MSB justified | H/L | O | | O |
| | | | H | 3 | | 32bit, $I^2S$ Compatible | L/H | O | | O |
| L | H | L (Slave) | L | 4 | TDM256 | 32bit, MSB justified | ↑ | I | 256fs | I |
| | | | H | 5 | | 32bit, $I^2S$ Compatible | ↓ | I | 256fs | I |
| | | H (Master) | L | 6 | | 32bit, MSB justified | ↑ | O | 256fs | O |
| | | | H | 7 | | 32bit, $I^2S$ Compatible | ↓ | O | 256fs | O |
| H | H | L (Slave) | L | 8 | TDM128 | 32bit, MSB justified | ↑ | I | 128fs | I |
| | | | H | 9 | | 32bit, $I^2S$ Compatible | ↓ | I | 128fs | I |
| | | H (Master) | L | 10 | | 32bit, MSB justified | ↑ | O | 128fs | O |
| | | | H | 11 | | 32bit, $I^2S$ Compatible | ↓ | O | 128fs | O |
| H | L | N/A | N/A | 12 | N/A | N/A | N/A | N/A | N/A | N/A |

Table 5. Audio Interface Format (N/A: Not available)

| Sampling Speed | Audio Interface Format | The maximum number of channels |
|---|---|---|
| Normal Speed | Normal | 2ch |
| | TDM256 | 8ch |
| | TDM128 | 4ch |
| Double Speed | Normal | 2ch |
| | TDM256 | N/A |
| | TDM128 | 4ch |
| Quad Speed | Normal | 2ch |
| | TDM256 | N/A |
| | TDM128 | 4ch |
| Octal Speed | Normal | 2ch |
| | TDM256 | N/A |
| | TDM128 | N/A |
| Hex Speed | Normal | 2ch (SDTO1: Lch, SDTO2: Rch) |
| | TDM256 | N/A |
| | TDM128 | N/A |

Table 6. Relationship between Sampling Speed and Audio Interface Format (N/A: Not available)

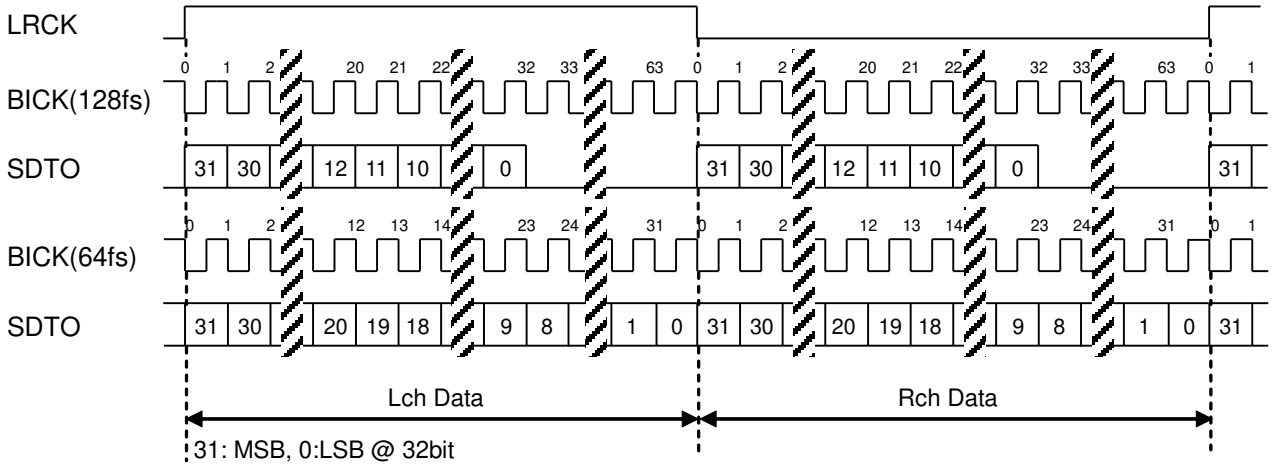



Figure 21. Mode 0/2 Timing (Normal mode, MSB justified, Normal/Double/Quad/Octal speed mode)

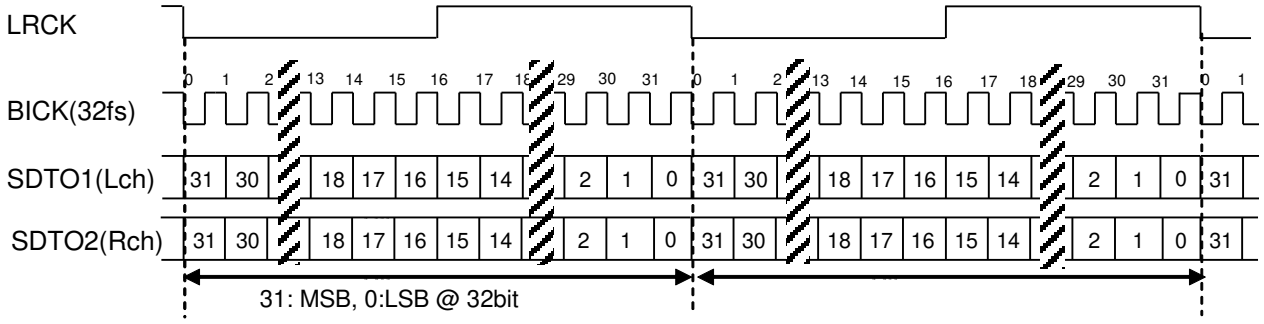



Figure 22. Mode 0/2 Timing (Normal mode, MSB justified, Hex speed mode)

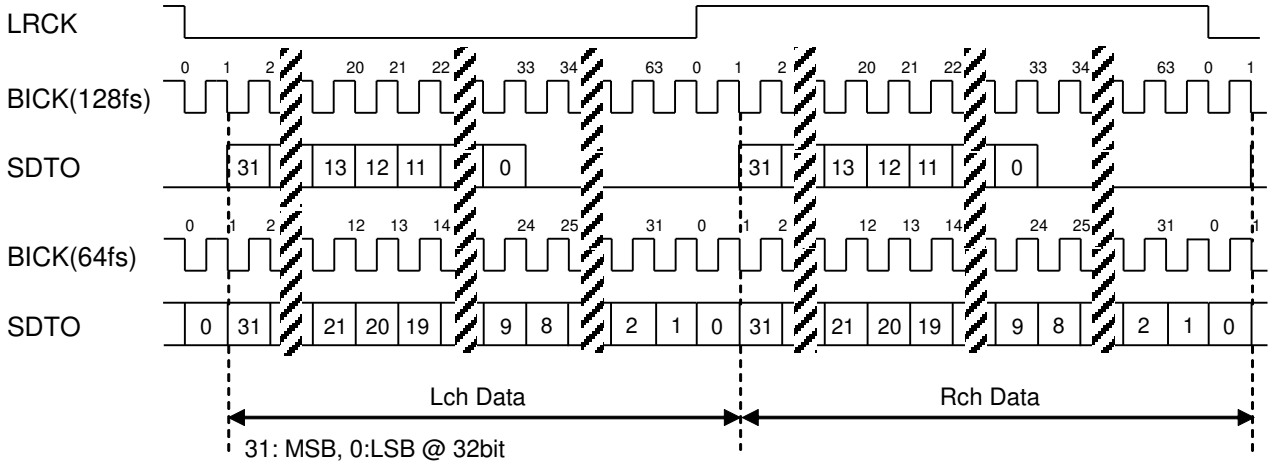



Figure 23. Mode 1/3 Timing (Normal mode, $I^2S$ Compatible, Normal/Double/Quad/Octal Speed)

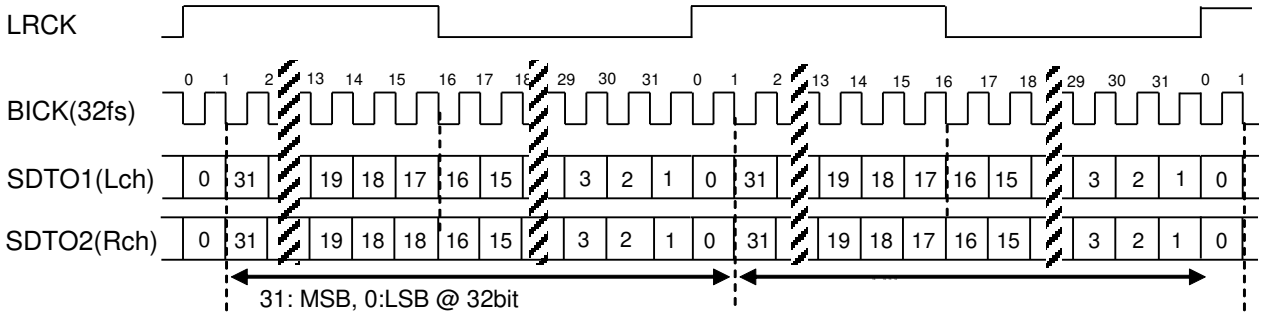



Figure 24. Mode 1/3 Timing (Normal mode, I$^2$S Compatible, Hex Speed)

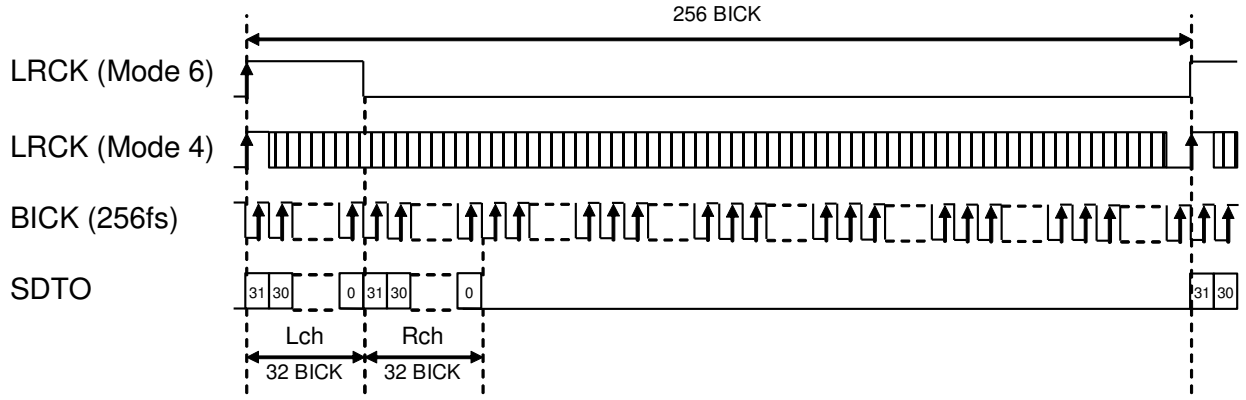



Figure 25. Mode 4/6 Timing (TDM256 mode, MSB justified)

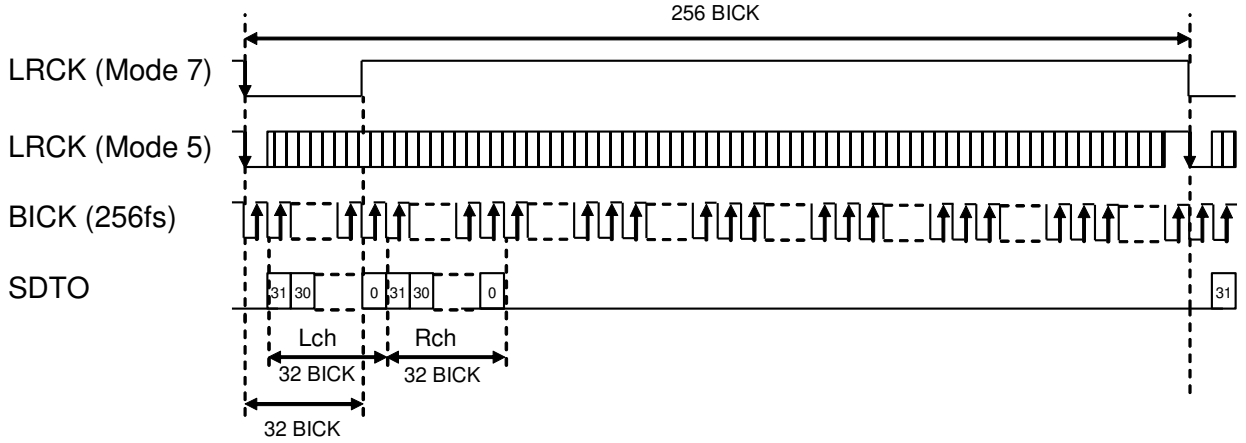



Figure 26. Mode 5/7 Timing (TDM256 mode, I$^2$S Compatible)

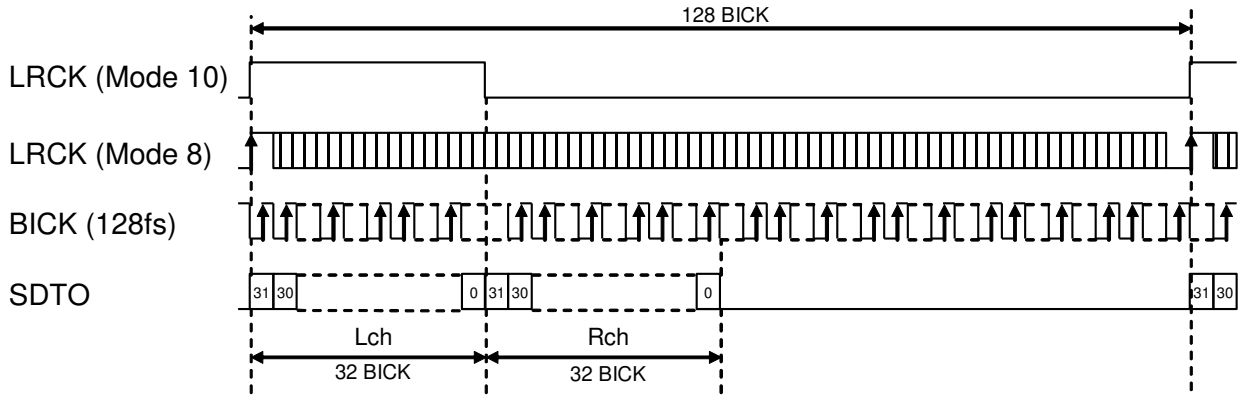



Figure 27. Mode 8/10 Timing (TDM128 mode, MSB justified)

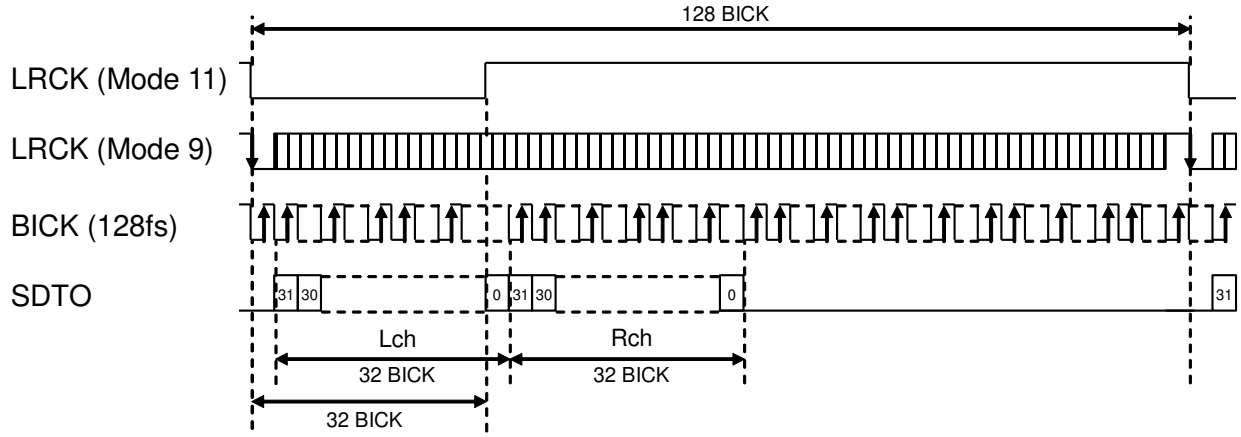



Figure 28. Mode 9/11 Timing (TDM128 mode, $I^2S$ Compatible)

## ■ Cascade TDM Mode

(1) TDM256 mode
The AK5397 supports cascading of up to four devices in a daisy chain configuration at TDM256 mode. In this mode, the SDTO1 pin (SDTO2 pin) is connected to the TDMIN1 pin (TDMIN2 pin) of next device. When four devices are connected by daisy-chaining as Figure 29, the SDTO1 pin (SDTO2 pin) of device #4 can send 8ch TDM data.

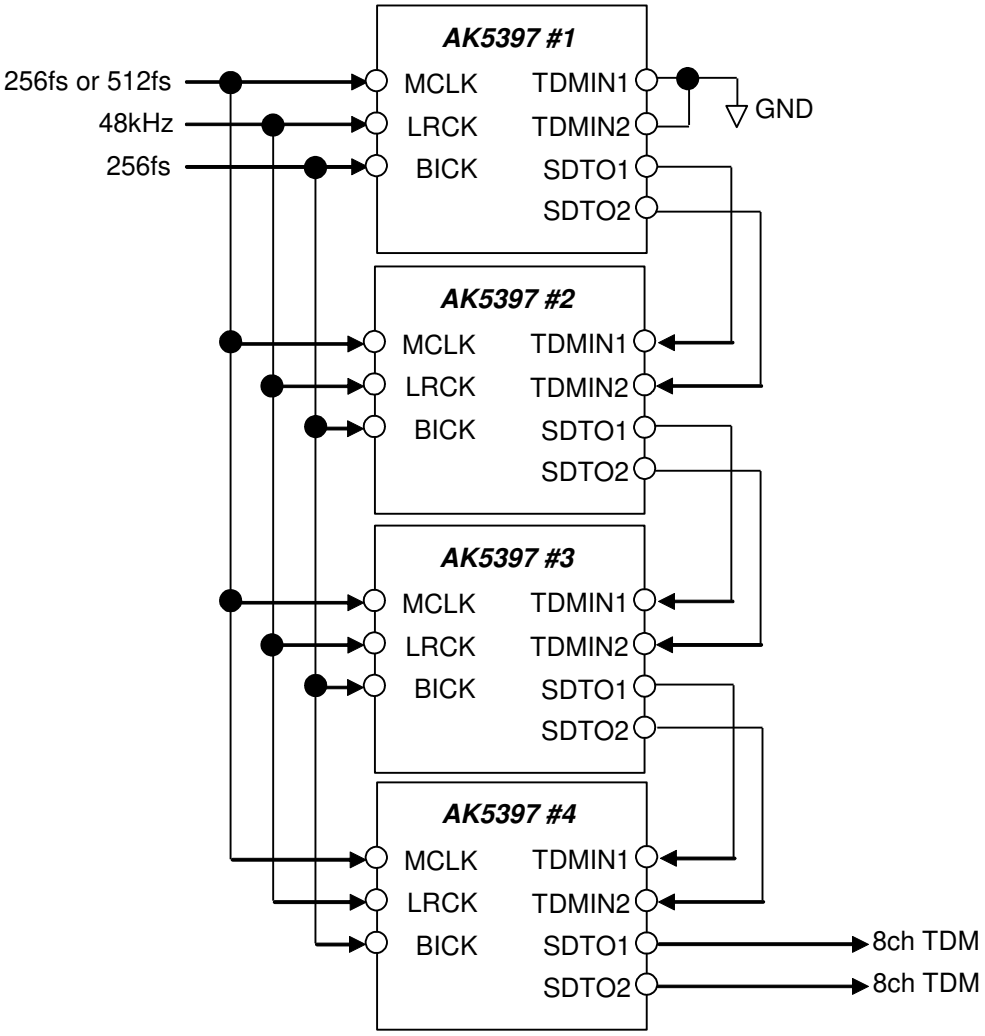



Figure 29. Cascade TDM Connection Diagram

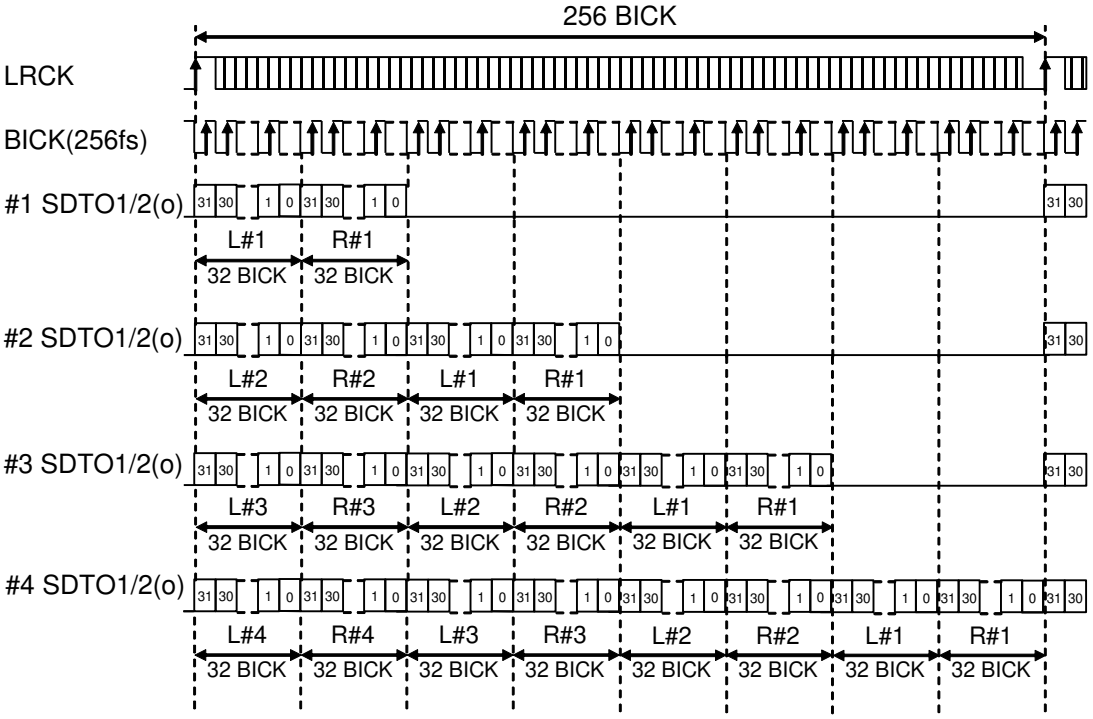



Figure 30. Cascade TDM Timing (Mode 4; TDM256 mode, MSB justified, Slave mode)

(2) TDM128 mode

The AK5397 supports cascading of two devices in a daisy chain configuration at TDM128 mode. In this mode, the SDTO1 pin (SDTO2 pin) is connected to the TDMIN1 pin (TDMIN2 pin) of next device. When two devices are connected by daisy-chaining as Figure 31, the SDTO1 pin (SDTO2 pin) of device #2 can send 4ch TDM data.

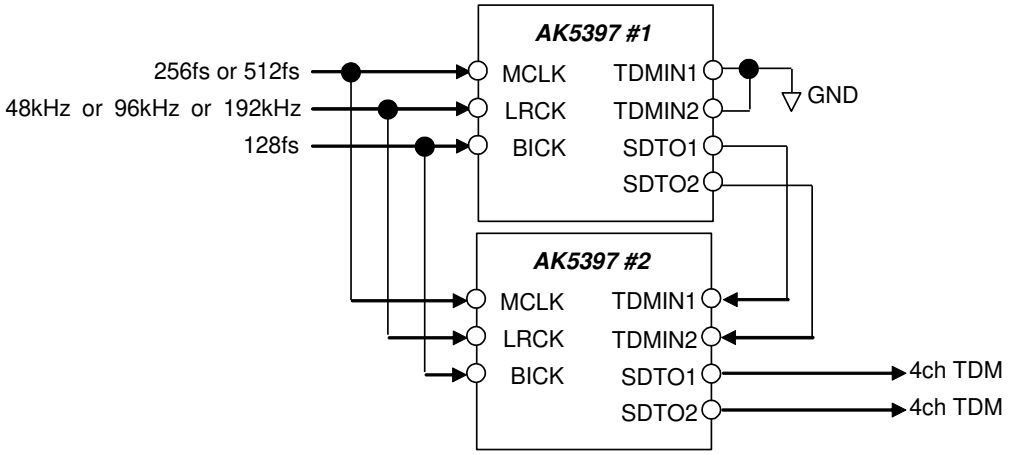



Figure 31. Cascade TDM Connection Diagram

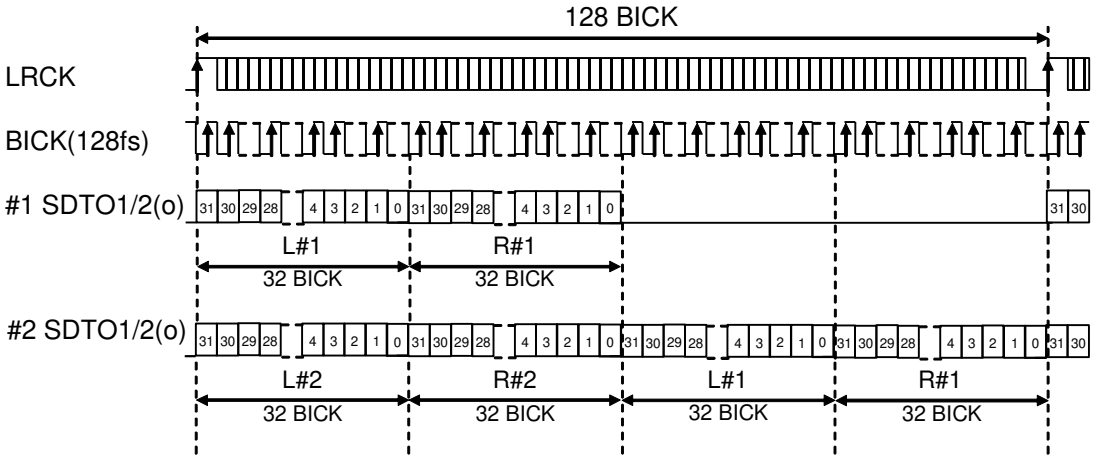



Figure 32. Cascade TDM Timing (Mode 8; TDM128 mode, MSB justified, Slave mode)

When using multiple devices in slave mode on cascade connection, internal operation timing of each device may differ for one MCLK cycle depending on PDN, MCLK and BICK input timings. To prevent this timing difference, BICK "↓" should be more than ± 10ns from MCLK "↑" and PDN "↑" should be more than ± 15ns from MCLK "↑" as shown in Table 7.
This timing can be achieved by inputting BICK divided half on MCLK "↓" when MCLK=2 x BICK (Normal 512fs, Double Speed) (Figure 33), and can be achieved by inputting BICK synchronized to MCLK when MCLK=BICK (Normal 256fs mode, Quad speed) (Figure 34).

| **Parameter** | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| MCLK "↑" to BICK "↓" | tMCB | 10 | | | ns |
| BICK "↓" to MCLK "↑" | tBIM | 10 | | | ns |
| MCLK "↑" to PDN "↑" | tMPD | 15 | | | ns |
| PDN "↑" to MCLK "↑" | tPDM | 15 | | | ns |

Table 7. TDM Mode Clock Timing

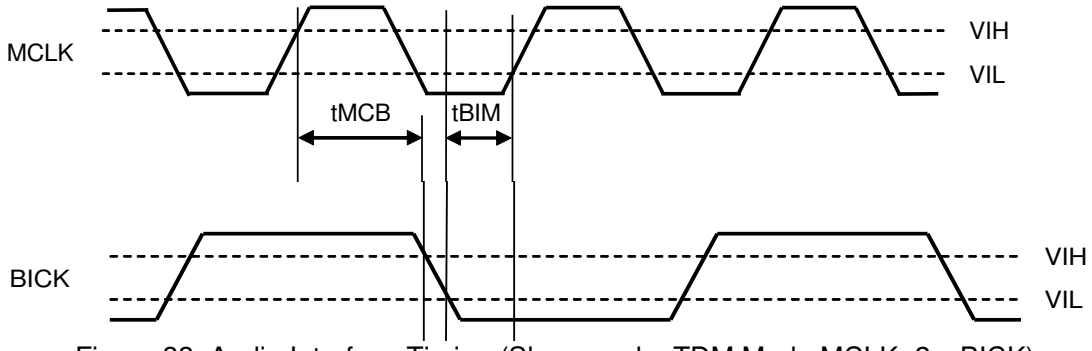



Figure 33. Audio Interface Timing (Slave mode, TDM Mode MCLK=2 x BICK)

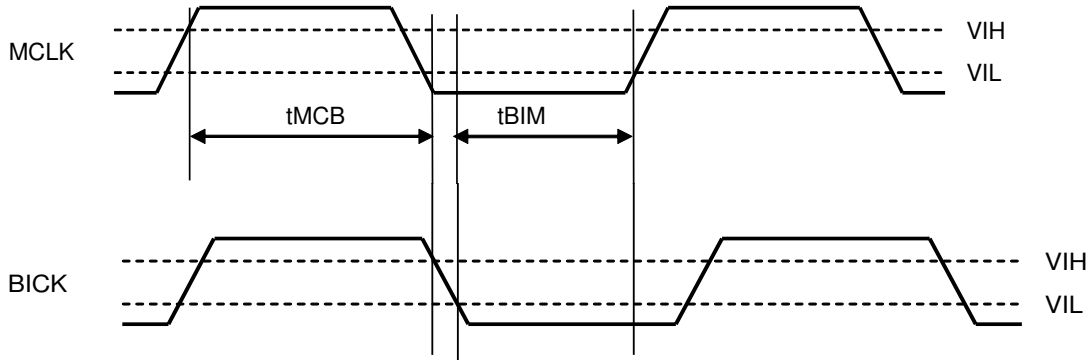



Figure 34. Audio Interface Timing (Slave mode, TDM Mode MCLK=BICK)

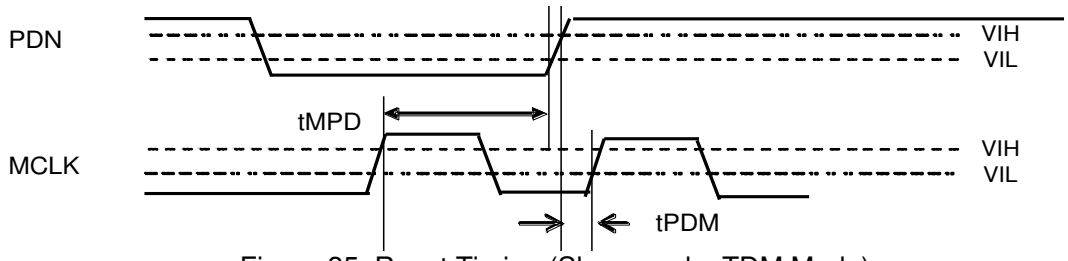



Figure 35. Reset Timing (Slave mode, TDM Mode)

## ■ Digital High Pass Filter

The AK5397 has a digital high pass filter for DC offset cancellation. The high pass filter is controlled by the HPFE pin as shown by Table 8 and is reflected in both SDTO1 and SDTO2. The cut-off frequency of the high pass filter is fixed 1.0Hz. The high pass filter is disabled in fs=384KHz mode or fs=768KHz mode, and the setting of HPFE pin is ignored. The high pass filter setting should only be changed when the PDN pin = “L”.

| HPFE pin | HPF |
|---|---|
| L | OFF |
| H | ON |

Table 8. Setting of HPF

## ■ Overflow Detection

The AK5397 has an overflow detect function for the analog input. The OVF pin becomes “H” for one cycle after LRCK “↑” if either channel overflows (more than -0.276dBFS). The OVF output for overflowed analog input has the same group delay as the ADC. The OVF pin is “L” for 1028/fs (=21.41ms@fs=48kHz) after the PDN pin=“↑”, and then overflow detection is enabled.

## ■ Mono Mode

When the MONO pin is set to “H”, the AK5397 becomes MONO mode. In the Mono mode, L channel and R channel data are summed digitally and divided into half. The dynamic range and S/N can be improved about 3dB when the same analog signal is input to left and right channels. In this mode, the left and right channel data on SDTO1 and SDTO2 are the same data.

| MONO pin | SDTO1/2 Output Data |
|---|---|
| L | Stereo Mode |
| H | Mono Mode |

Table 9. The setting of MONO mode.

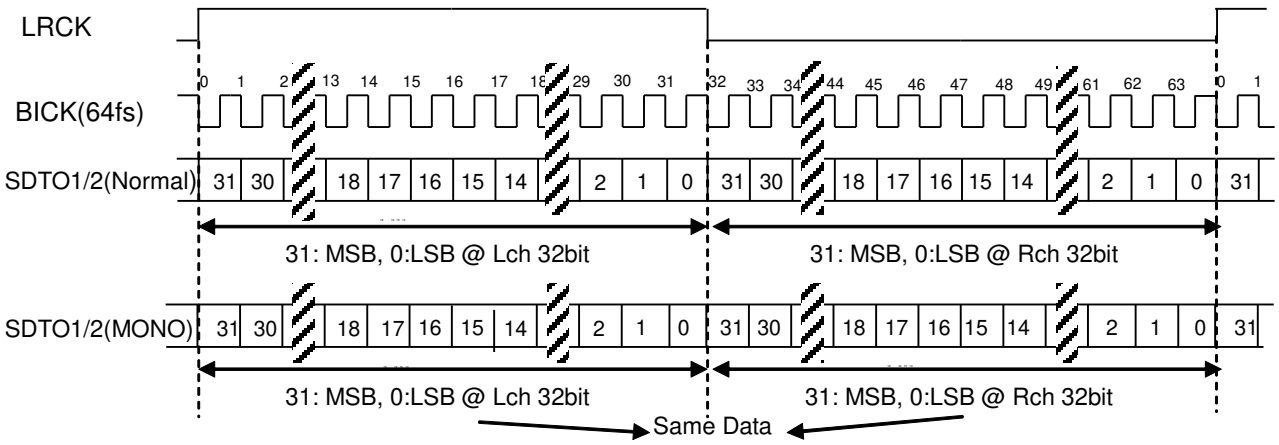



Figure 36. Audio Interface Timing (Normal mode or MONO mode, MSB justified)

## ■ Digital Output Data

The AK5397 has two kinds of output data. These data are sent from SDTO1 and SDTO2 pins at the same time. The SDTO1 pin is passed through “Sharp Roll-off” and the SDTO2 pin is passed through “Short Delay Filter” or “Minimum Phase Filter” selected by the SDFIL pin as shown by Table 12.
When fs=384kHz, 768kHz, the AK5397 does not support “Short Delay Filter” and “Minimum Phase Filter”. When fs=384kHz, the SDTO1 pin is passed through “Sharp Roll-off Filter”, and the SDTO2 pin is “L”. When fs=768kHz, the SDTO1 and SDTO2 pins are passed through “Sharp Roll-off Filter” as shown in Table 10. However, in MONO mode, the SDTO1 pin outputs the data of (Lch+Rch)/2, and the SDTO2 pin is “L” as shown in Table 11.

The output data of SDTO1 and SDTO2 pins can be disabled by using SDM1 and SDM2 pins respectively as shown in Figure 37, Table 13 and Table 14. However, the SDM2 pin can output data if fs=768KHz even when the SDM2 pin = “H”.

| Sampling Speed | SDTO1 Output Data | SDTO2 Output Data |
|---|---|---|
| 48kHz | Sharp Roll-off Filter | Short Delay Filter |
| 96kHz | Sharp Roll-off Filter | Short Delay Filter |
| 192kHz | Sharp Roll-off Filter | Short Delay Filter |
| 384kHz | Sharp Roll-off Filter | “L” Output |
| 768kHz | Sharp Roll-off Filter (Lch) | Sharp Roll-off Filter (Rch) |

Table 10. SDTO1 / SDTO2 Output Data (MONO = “L”)

| Sampling Speed | SDTO1 Output Data | SDTO2 Output Data |
|---|---|---|
| 48kHz | Sharp Roll Off Filter | Short Delay Filter |
| 96kHz | Sharp Roll Off Filter | Short Delay Filter |
| 192kHz | Sharp Roll Off Filter | Short Delay Filter |
| 384kHz, 768kHz | Sharp Roll Off filter (Lch+Rch)/2 | “L “Output |

Table 11. SDTO1 / SDTO2 Output Data (MONO = “H”)

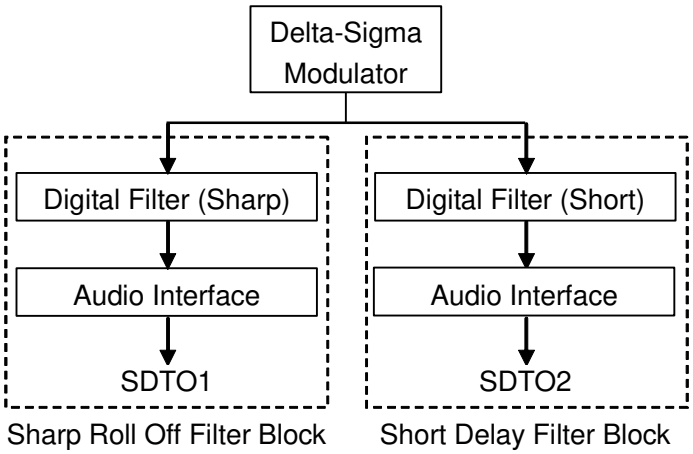



Figure 37. Digital Filter Block

| SDFIL pin | SDTO2 Output Data |
|---|---|
| L | Short Delay Filter |
| H | Minimum Phase Filter |

Table 12. The setting of SDFIL pin

| SDM1 pin | SDTO1 Output Data |
|---|---|
| L | Normal output |
| H | “L” output |

Table 13. The setting of SD1M pin

| SDM2 pin | SDTO2 Output Data |
|---|---|
| L | Normal output |
| H | “L” output |

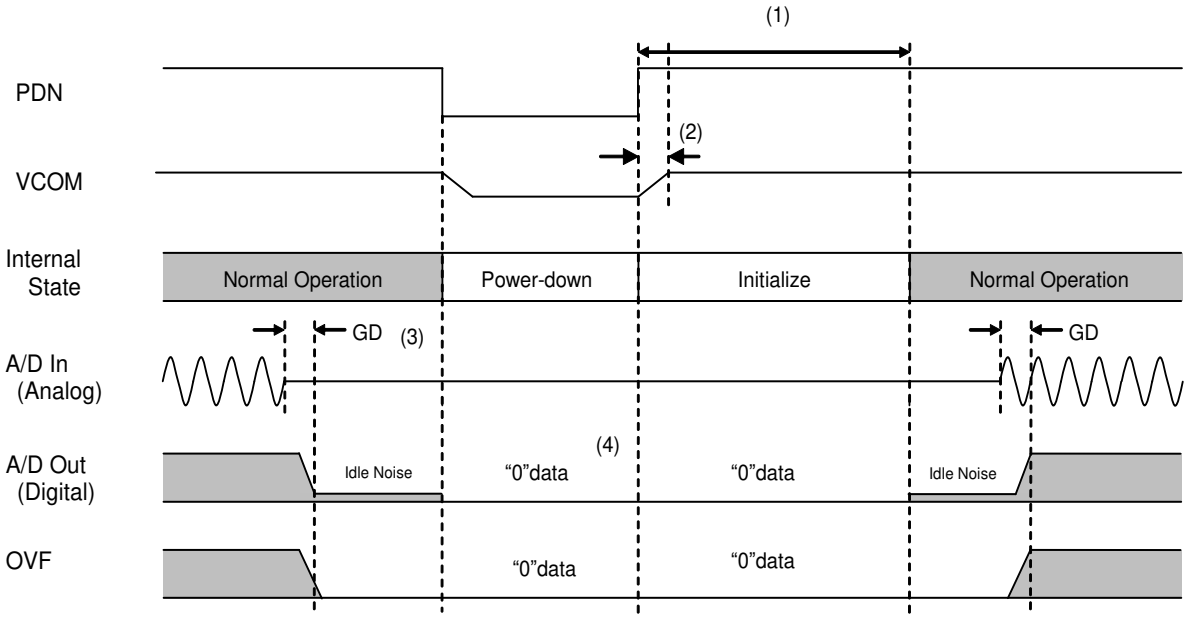
Table 14. The setting of SD2M pin

The SDTO1/2 outputs settle to data correspondent to the analog input signals after group delay time when SDM1/2 pins are changed “H” → “L” and SDTO1/2 pins are in Normal Output Mode.

## ■ Power Down & Reset

The AK5397 is placed in the power-down mode by bringing the PDN pin “L” and the digital filter is also reset at the same time. This reset should always be made after power-up. In the power-down mode, the VCOM is AVSS level. An analog initialization cycle starts after exiting the power-down mode. The output data SDTO1/2 are valid after 1028 cycles of LRCK clock in master mode (1029 cycles in slave mode). During initialization, the ADC digital data outputs of both channels are forced to “0”. The ADC outputs settle to data correspondent to the input signals after the end of initialization (This settling takes approximately the group delay time).

The AK5397 should be reset once by bringing the PDN pin “L” after power-up. The AK5397 exits reset and power down state by MCLK rising edge after setting the PDN pin to “H”. The internal timing starts clocking by the rising edge (falling edge in I2S mode) of LRCK after exiting reset and power down state by MCLK.

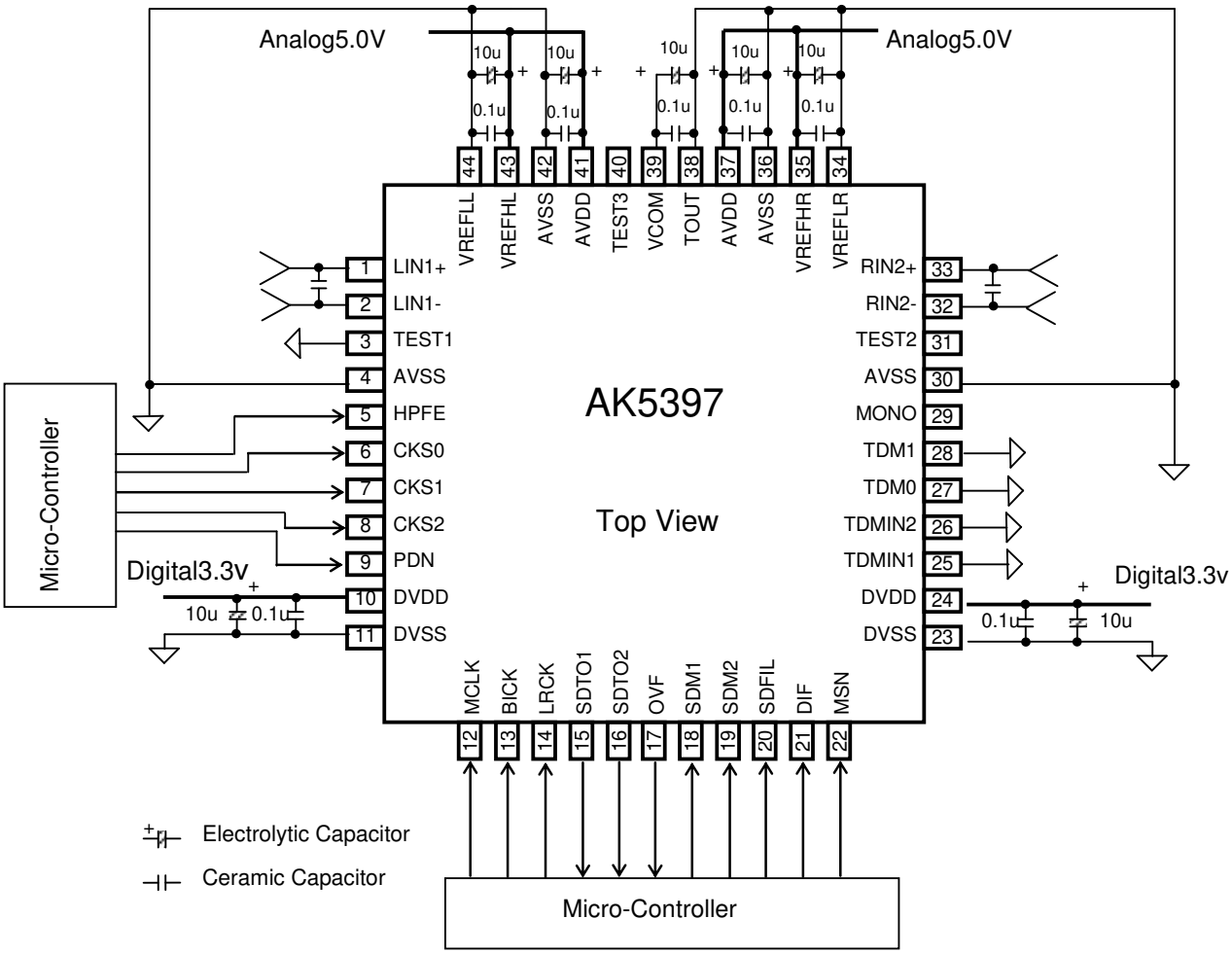



Notes:
(1) 1030/fs in slave mode, 1031/fs in master mode.
(2) The VCOM voltage reaches 2.5V in 1.53 ms (typ), 2.64ms (max) after the PDN pin = “H”.
(3) Analog output corresponding to digital input has group delay (GD).
(4) ADC and OVF outputs are “0” data in the power-down mode.

Figure 38. Power-down/up sequence example

## 10. SYSTEM DESIGN

Figure 39 shows the system connection diagram. An evaluation board (AKD5397) is available for fast evaluation as well as suggestions for peripheral circuitry.




Note:
- AVSS and DVSS of the AK5397 must be distributed separately from the ground of external controllers.
- All digital input pins should not be left floating.

Figure 39. System Design

## 1. Grounding and Power Supply Decoupling

The AK5397 requires careful attention to power supply and grounding arrangements. To minimize digital noise coupling, AVDD and DVDD should be individually de-coupled at the AK5397. AVDD is usually supplied from analog supply in system and DVDD is supplied from digital supply in system. Power lines of AVDD and DVDD should be distributed separately from the point with low impedance of regulator etc. AVSS and DVSS must be connected to the same analog ground plane. Decoupling capacitors for high frequency should be placed as near as possible to the supply pin.

## 2. Voltage Reference Inputs

The reference voltage for A/D converter is the difference between VREFHL/R pin and VREFLL/R pin. VREFLL/R pins are connected to AVSS and an electrolytic capacitor over 10µF parallel with a 0.1µF ceramic capacitor between the VREFHL/R pin and the VREFLL/R pin eliminates the effects of high frequency noise. It is important that a ceramic capacitor should be as near to the pins as possible. All digital signals, especially clocks, should be kept away from the VREFHL/R and VREFLL/R pins in order to avoid unwanted coupling into the AK5397.

VCOM is a signal ground of this chip. A 10µF electrolytic capacitor in parallel with a 0.1µF ceramic capacitor attached to the VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK5397.

## 3. Analog Inputs

The Analog input signal is differentially supplied into the modulator via the LIN+ (RIN+) and the LIN- (RIN-) pins. The input voltage is the difference between the LIN+ (RIN+) and LIN- (RIN-) pins. The full scale signal on each pin is nominally ±2.80V (typ). The output code format is two's complement. The output voltage (VAOUT) is positive full scale for 7FFFFFFFH (@32bit) and negative full scale for 80000000H (@32bit). The ideal VAOUT is 0V for 00000000H (@32bit). The internal HPF removes DC offset.

The AK5397 samples the analog inputs at 128fs (6.144MHz@fs=48kHz, Normal Speed Mode). The digital filter rejects noise above the stop band except for multiples of 128fs. The AK5397 includes an anti-aliasing filter (RC filter) to attenuate a noise around 128fs.

The AK5397 requires a +5V analog supply voltage. Any voltage which exceeds the upper limit of AVDD+0.3V and lower limit of AVSS-0.3V and any current beyond 10mA for the analog input pins (LIN+/-, RIN+/-) should be avoided. Excessive currents to the input pins may damage the device. Hence input pins must be protected from signals at or beyond these limits. Use caution especially when using ±15V for other analog circuits in the system.

## 4. External Analog Circuit Examples

Figure 40 shows an input buffer circuit example 1. (1st order HPF; fc=0.795Hz, 2nd order LPF; fc=438kHz, gain=-9.63dB). The analog signal is able to input through XLR or BNC connectors. (short JP1 and JP2 for BNC input, open JP1 and JP2 for XLR input). The input level of this circuit is 17.0Vpp (AK5397: 5.6Vpp Typ.). When using this circuit, analog characteristics at fs=48kHz is DR=124dB, S/(N+D)=108dB.
Resistor values should be in ±1% accuracy.
When the bias voltage is more than 0.28xAVDD+0.6 [V], the internal diode is powered up.

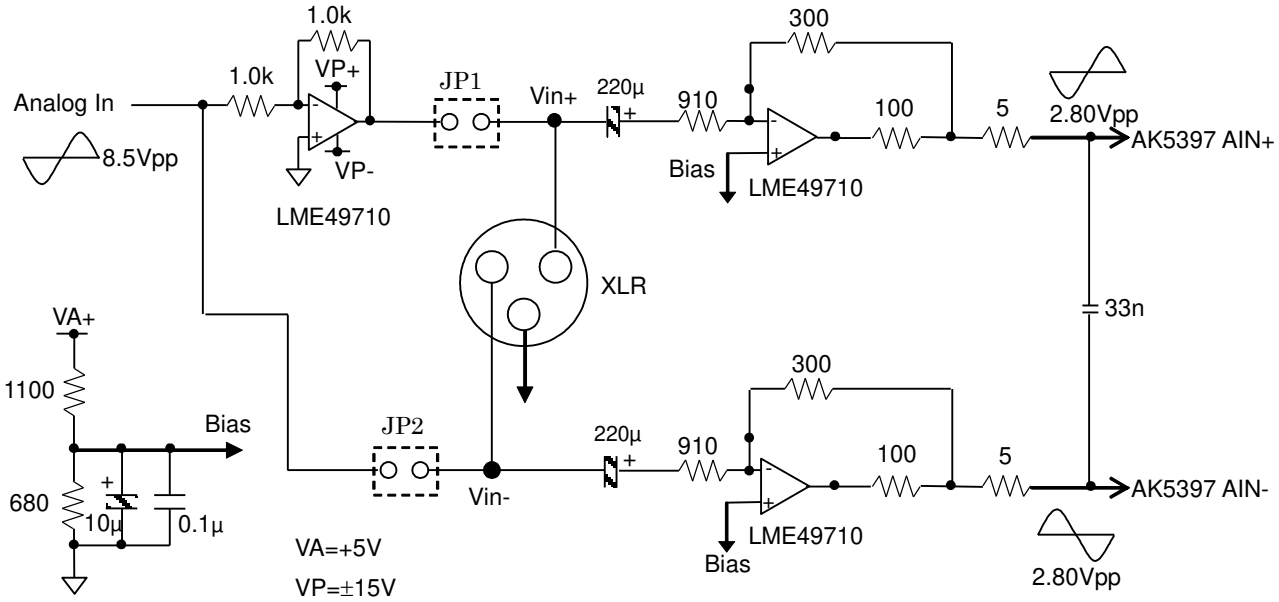



Figure 40. Analog Input Buffer Circuit Example 1

| fin | 1Hz | 10Hz |
|---|---|---|
| Frequency Response | -2.13dB | -0.03dB |

Table 15. Frequency Response of HPF

| fin | 20kHz | 40kHz | 80kHz | 6.144MHz |
|---|---|---|---|---|
| Frequency Response | 0.01dB | -0.04dB | -0.14dB | –30.31dB |

Table 16. Frequency Response of LPF

Figure 41 shows an input buffer circuit example 1. (1st order HPF; fc=0.795Hz, 2nd order LPF; fc=290kHz, gain=963 dB). The analog signal is able to input through XLR or BNC connectors. (short JP1 and JP2 for BNC input, open JP1 and JP2 for XLR input). The input level of this circuit is 17.0Vpp (AK5397: 5.6Vpp Typ.). When using this circuit, analog characteristics at fs=48kHz is DR=127dB, S/(N+D)=100dB. Resistor values should be in ±1% accuracy.
When the bias voltage is more than 0.28xAVDD+0.6 [V], the internal diode is powered up.

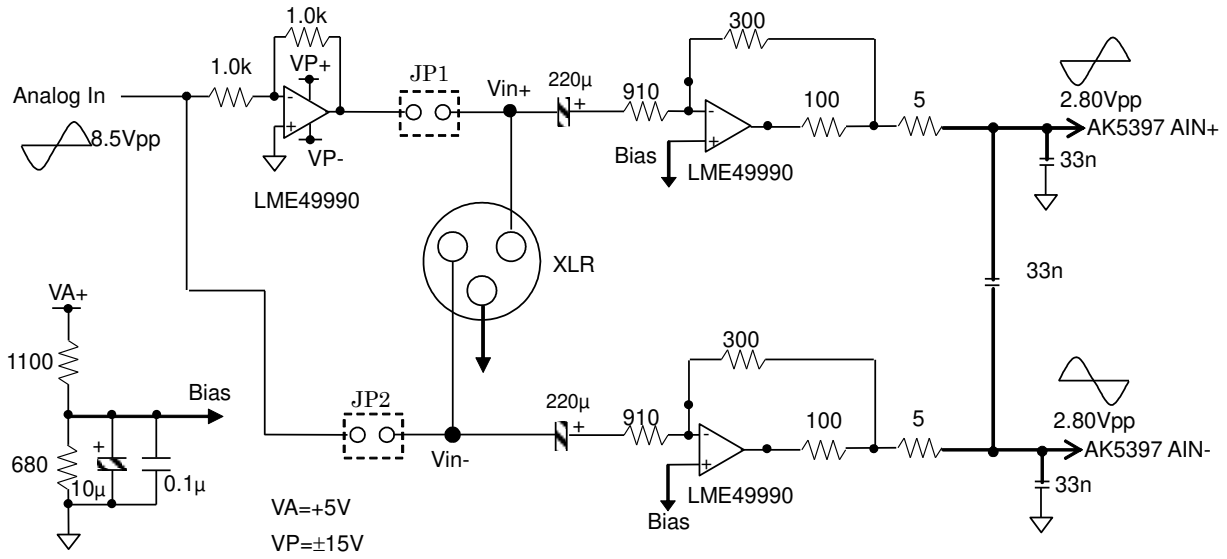



Figure 41. Analog Input Buffer Circuit Example 2

| fin | 1Hz | 10Hz |
|---|---|---|
| Frequency Response | -2.1dB | -0.03dB |

Table 17. Frequency Response of HPF

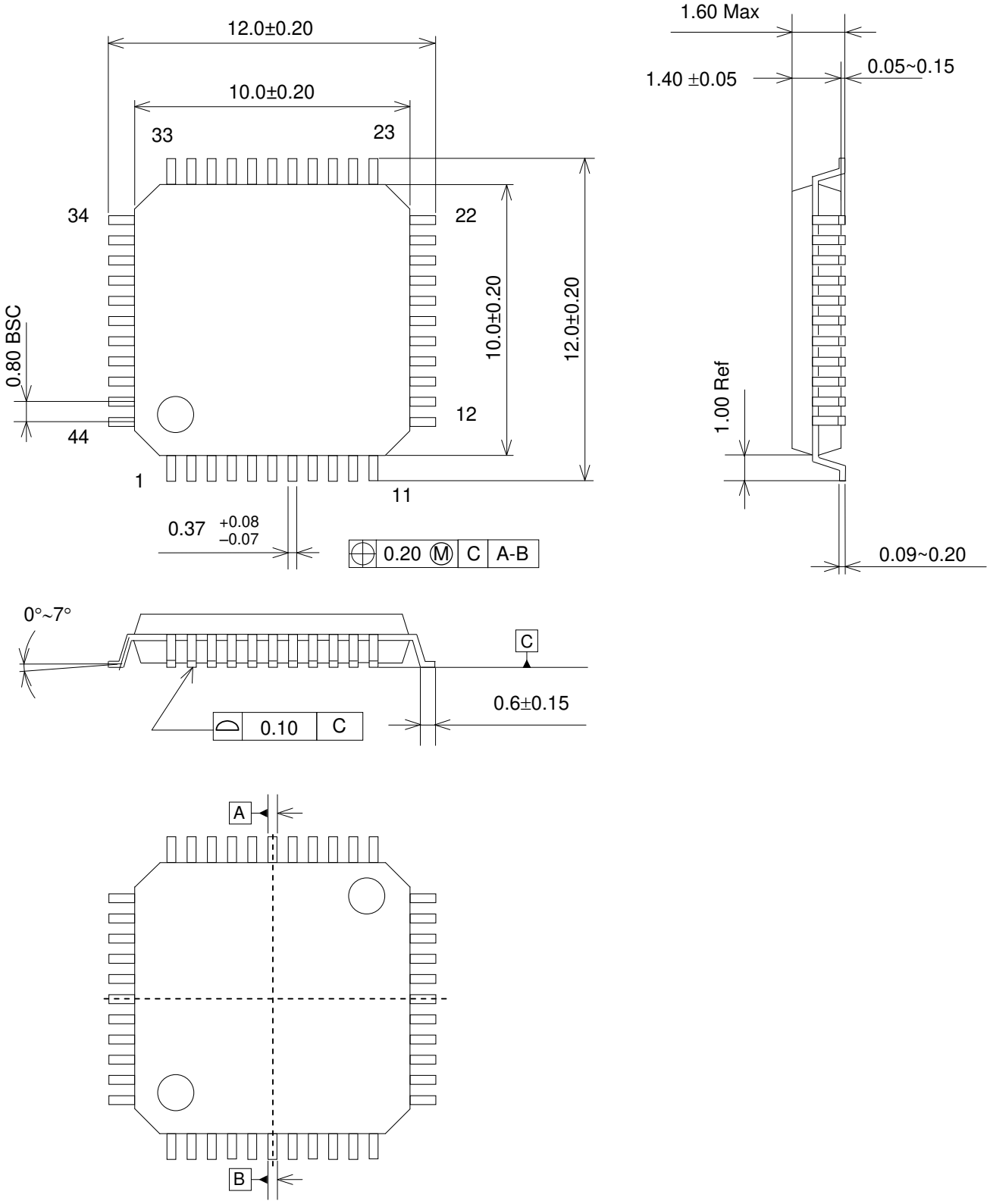
| fin | 20kHz | 40kHz | 80kHz | 6.144MHz |
|---|---|---|---|---|
| Frequency Response | -0.01dB | -0.02dB | -0.08dB | –33.82dB |

Table 18. Frequency Response of LPF

## 11. PACKAGE

### ■ Outline Dimensions

**44pin LQFP (Unit: mm)**



## ■ Material & Lead finish

| | |
|---|---|
| Package molding compound: | Epoxy, Halogen (bromine and chlorine) free |
| Lead frame material: | Cu |
| Lead frame surface treatment: | Solder (Pb free) plate |

## ■ MARKING

1) Pin #1 indication
2) Audio 4 pro Logo
3) Date Code: XXXXXXX(7 digits)
4) Marking Code: AK5397
5) AKM Logo

## 12. Ordering Guide

| | | |
|---|---|---|
| AK5397EQ | −10 ~ +70°C | 44pin LQFP (0.8mm pitch) |
| AKD5397 | Evaluation Board for AK5397 | |

## 13. Revision History

| Date (Y/M/D) | Revision | Reason | Page | Contents |
|---|---|---|---|---|
| 14/11/14 | 00 | First Edition | | |

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