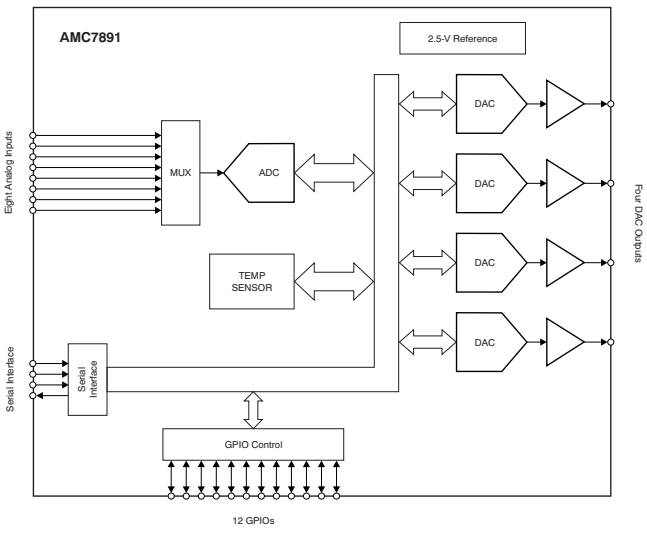
Analog Monitor and Control Circuit with 10-Bit, Multi-Channel ADC and Four DACs, Temperature Sensor, and 12 GPIOs

Check for Samples: AMC7891

FEATURES

- **10-Bit, 500-kSPS SAR ADC:**
  - **8 External Analog Inputs**
  - **V_{REF}, 2 × V_{REF} Input Ranges**
- **Four 10-Bit Monotonic DACs:**
  - **0 to 5-V Output Range**
  - **Up to 10-mA Sink and Source Capability**
  - **Power-On Reset to 0 V**
- **Internal 2.5-V Reference**
- **Internal Temperature Sensor:**
  - **–40°C to +125°C Operation**
  - **Accuracy of ±2.5°C**
- **12 General-Purpose I/O Ports:**
  - **1.8-V to 5.5-V Operation**
- **Low-Power SPI™-Compatible Serial Interface:**
  - **4-Wire Mode, 1.8-V to 5.5-V Operation**
  - **SCLK up to 30 MHz**
- **Temperature Range: –40°C to +105°C**
- **Low Power: 32.5 mW at 5 V, Full Operating Conditions**
- **Space-Saving Package: 36-pin, 6-mm x 6-mm QFN**



APPLICATIONS

- **Cellular Base Stations**
- **RF Communication Systems**
- **Optical Networks**
- **General-Purpose Monitor and Control**

DESCRIPTION

The AMC7891 is a highly-integrated, low-power, complete analog monitoring and control system in a very small package.

For monitoring functions, the AMC7891 has 8 uncommitted inputs multiplexed into a 10-bit SAR analog-to-digital converter (ADC) and an accurate on-chip temperature sensor. Control signals are generated through four, independent, 10-bit digital-to-analog converters (DACs). Additional digital signal monitoring and control is accomplished through twelve configurable GPIOs. An internal reference can be used to drive the ADC and DACs.

Communication to the device is performed through a versatile, four-wire serial interface compatible with industry-standard microprocessors and microcontrollers. The serial interface can operate at clock rates up to 30 MHz, allowing quick access to critical system data.

The device is characterized for operation over the temperature range of –40ºC to 105ºC and is available in a very small, 36-pin, 6-mm x 6-mm QFN package.

The AMC7891's low power, small size and high-integration make it an ideal low-cost, bias control circuit for modern RF transistor modules such as the power amplifiers (PA) and low-noise amplifiers (LNA) found in RF communication systems. The AMC7891 feature set is similarly beneficial in general purpose monitor and control systems.

For applications that require a different channel count, additional features, or converter resolutions, Texas Instruments offers a complete family of Analog Monitor and Control (AMC) Products. See http://www.ti.com/amc.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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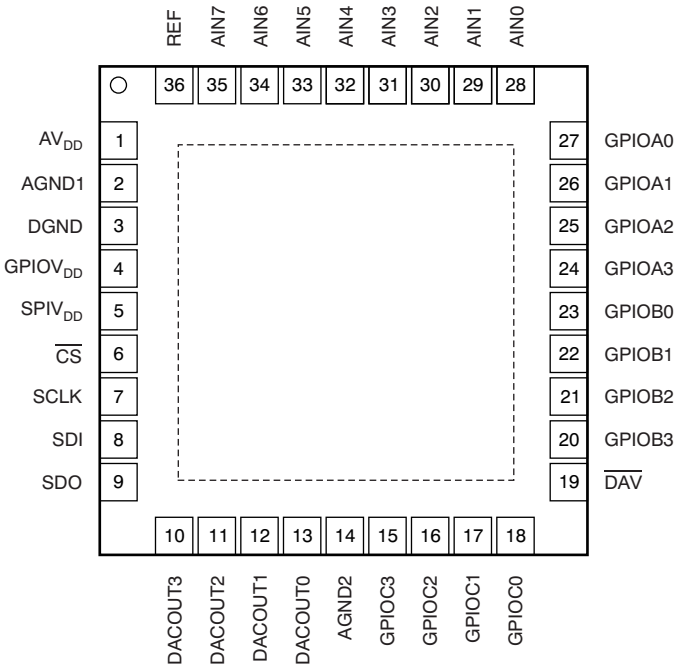
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

RHH PACKAGE
QFN-36
(TOP VIEW)



AMC7891 Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	AV_{DD}	I	Analog supply voltage. (4.75 V to 5.5 V)
2	AGND1	I	Analog ground. Ground reference point for all analog circuitry on the device, AGND. Connect AGND1 and AGND2 to the same potential, AGND.
3	DGND	I	Digital ground. Ground reference point for all digital circuitry on the device. Ideally, AGND and DGND should be at the same potential and must not differ by more than 0.3 V.
4	$GPIOV_{DD}$	I	GPIO supply voltage. (1.8 V to 5.5 V) Sets the GPIO operating voltage and threshold levels.
5	$SPIV_{DD}$	I	Serial interface supply voltage. (1.8 V to 5.5 V) Sets the serial interface operating voltage and threshold levels.
6	$\overline{CS}$	I	Active low serial data enable. Schmitt-trigger logic input. This input is the frame synchronization signal for the serial data. When this signal goes low, it enables the input shift register and data is sampled on subsequent falling clock edges. The DAC output and register settings update following the 24th clock. If $\overline{CS}$ goes high before the 23th clock edge, the command is ignored.
7	SCLK	I	Serial interface clock. Schmitt-trigger logic input. Maximum SCLK rate is 30MHz.
8	SDI	I	Serial interface data input. Schmitt-trigger logic input. Data is clocked into the input shift register on each falling edge of SCLK.
9	SDO	O	Serial interface data output. The SDO pin is in high impedance when $\overline{CS}$ is high. Data is clocked out of the input shift register on each rising edge of SCLK.
10	DACOUT3	O	DAC3 buffered output. (0 V to AV_{DD}). Can source/sink up to 10 mA.

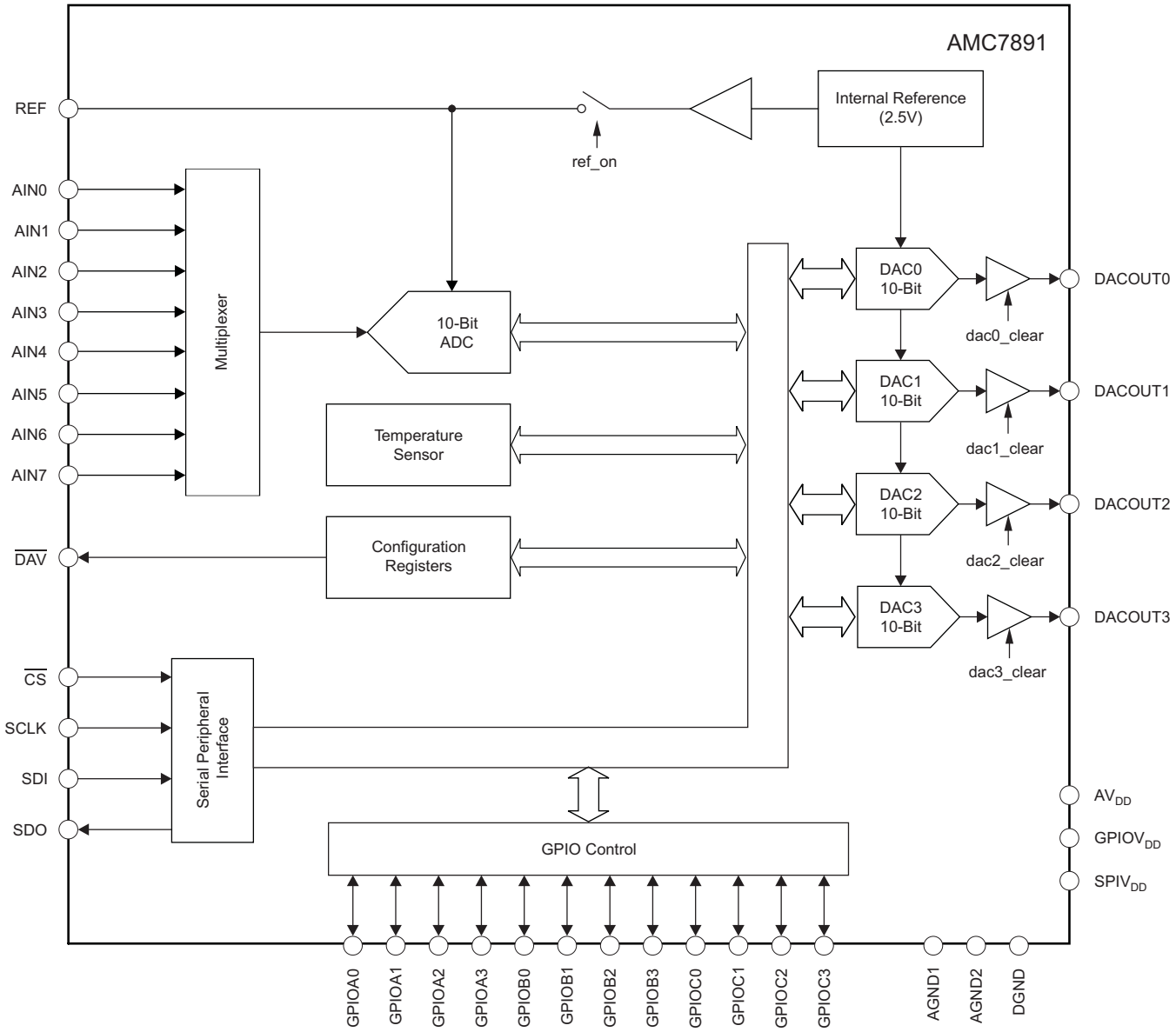
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AMC7891 Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
11	DACOUT2	O	DAC2 buffered output. (0 V to AV_{DD}). Can source/sink up to 10 mA.
12	DACOUT1	O	DAC1 buffered output. (0 V to AV_{DD}). Can source/sink up to 10 mA.
13	DACOUT0	O	DAC0 buffered output. (0 V to AV_{DD}). Can source/sink up to 10 mA.
14	AGND2	I	Analog ground. Ground reference point for all analog circuitry on the device, AGND. Connect AGND1 and AGND2 to the same potential, AGND.
15	GPIOC3	I/O	General purpose digital I/O C3. Maximum voltage is set by $GPIOV_{DD}$
16	GPIOC2	I/O	General purpose digital I/O C2. Maximum voltage is set by $GPIOV_{DD}$
17	GPIOC1	I/O	General purpose digital I/O C1. Maximum voltage is set by $GPIOV_{DD}$
18	GPIOC0	I/O	General purpose digital I/O C0. Maximum voltage is set by $GPIOV_{DD}$
19	$\overline{DAV}$	O	ADC data available indicator. Open-drain, active low output. In direct-mode, $\overline{DAV}$ goes low when an ADC conversion cycle finishes. In auto-mode a 1µs pulse appears on this pin when the conversion cycle finishes (see ADC Operation for details). $\overline{DAV}$ stays high when deactivated. If used, an external 10 kΩ pull-up resistor to $GPIOV_{DD}$ is required. If unused, the pin can be connected to DGND.
20	GPIOB3	I/O	General purpose digital I/O B3. Maximum voltage is set by $GPIOV_{DD}$
21	GPIOB2	I/O	General purpose digital I/O B2. Maximum voltage is set by $GPIOV_{DD}$
22	GPIOB1	I/O	General purpose digital I/O B1. Maximum voltage is set by $GPIOV_{DD}$
23	GPIOB0	I/O	General purpose digital I/O B1. Maximum voltage is set by $GPIOV_{DD}$
24	GPIOA3	I/O	General purpose digital I/O A3. Maximum voltage is set by $GPIOV_{DD}$
25	GPIOA2	I/O	General purpose digital I/O A2. Maximum voltage is set by $GPIOV_{DD}$
26	GPIOA1	I/O	General purpose digital I/O A1. Maximum voltage is set by $GPIOV_{DD}$
27	GPIOA0	I/O	General purpose digital I/O A1. Maximum voltage is set by $GPIOV_{DD}$
28	AIN0	I	Uncommitted analog input 0. (0 V to 5 V)
29	AIN1	I	Uncommitted analog input 1. (0 V to 5 V)
30	AIN2	I	Uncommitted analog input 2. (0 V to 5 V)
31	AIN3	I	Uncommitted analog input 3. (0 V to 5 V)
32	AIN4	I	Uncommitted analog input 4. (0 V to 5 V)
33	AIN5	I	Uncommitted analog input 5. (0 V to 5 V)
34	AIN6	I	Uncommitted analog input 6. (0 V to 5 V)
35	AIN7	I	Uncommitted analog input 7. (0 V to 5 V)
36	REF	I/O	Used as external ADC reference input when the internal reference buffer is disabled in register *AMC_power, ref_on* = '0' (default). A decoupling capacitor is recommended between the external reference output an AGND for noise filtering. Used as internal reference output when the internal reference buffer is enabled in register *AMC_power, ref_on* = '1'. Requires a 4.7 µF decoupling capacitor to AGND when used as reference output. An external buffer amplifier with high impedance input is required to drive an external load.
–	THERMAL PAD	–	The thermal pad is located on the package underside. Connect to the board ground plane using multiple vias.

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FUNCTIONAL BLOCK DIAGRAM



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ORDERING INFORMATION(1)

T_A	ORDER CODE	PACKAGE DRAWING/TYPE(2)(3)	TRANSPORT MEDIA	QUANTITY
–40°C to 105°C	AMC7891SRHHT	RHH / 36-QFN Quad Flatpack No-Lead	Tape and Reel	250
	AMC7891SRHHR			2000

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.
(2) Thermal Pad Size: 4.39 mm x 4.39 mm
(3) MSL Peak Temperature: Level-3-260C-168 HR

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE		UNIT
		MIN	MAX	
Supply voltage range	AV_{DD} to AGND(2)	–0.3	6	V
	$GPIOV_{DD}$ to DGND	–0.3	6	V
	$SPIV_{DD}$ to DGND	–0.3	6	V
	AGND to DGND	–0.3	0.3	V
Pin voltage range	AIN[0:7], DACOUT[0:3], REF to AGND	–0.3	AV_{DD} + 0.3	V
	$\overline{CS}$, SCLK, SDI to DGND	–0.3	6	V
	SDO to DGND	–0.3	$SPIV_{DD}$ + 0.3	V
	GPIOA[0:3], GPIOB[0:3], GPIOC[0:3] to DGND	–0.3	$GPIOV_{DD}$ + 0.3	V
	$\overline{DAV}$ to DGND	–0.3	6	V
Operating free-air temperature range, T_A: AMC7891 (3) (4)		–40	105	°C
Storage temperature range		–40	150	°C
ESD ratings:	Human body model (HBM)		2.5	kV
	Charged device model (CDM)		1.0	kV

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.
(2) AGND1 and AGND2 must be tied together as AGND.
(3) Air flow or heat sinking reduces θ_{JA} and may be required for sustained operation at 105°C and maximum operating conditions.
(4) Soldering the device thermal pad to the board ground plane is strongly recommended.

THERMAL INFORMATION

THERMAL METRIC(1)		AMC7891 RHH PACKAGE 36 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	30.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	16.0	
θ_{JB}	Junction-to-board thermal resistance	5.3	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	5.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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ELECTRICAL CHARACTERISTICS (DAC SPECIFICATIONS)

AV_{DD} = 4.75 to 5.5 V, $GPIOV_{DD}$ = 1.8 to 5.5 V, $SPIV_{DD}$ = 1.8 to 5.5 V, AGND = DGND = 0 V, External ADC reference = AV_{DD}, T_A = –40°C to 105°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC ACCURACY						
	Resolution		10			Bits
INL	Relative accuracy			±0.05	±1	LSB
DNL	Differential nonlinearity	Specified monotonic		±0.1	±1	LSB
	Offset error	Code 0x008		±0.5	±5	mV
	Gain error			±0.025	±0.2	%FSR
	Offset temperature coefficient			±1		ppm/°C
	Gain temperature coefficient			±1		ppm/°C
DAC OUTPUT (1)						
	Full scale output voltage range		0		AV_{DD}	V
	Output voltage settling time	Transition: Code 0x008 to 0x3F8 to within 1/2 LSB, C_L = 2 nF, RL = ∞		5		µs
	Slew rate			2		V/µs
	Short circuit current	Full-scale current shorted to ground or pulled to AVDD		±30		mA
	Load current	Source and/or sink within 300 mV of supply		±10		mA
	Capacitive load stability	R_L = ∞	10			nF
	DC output impedance			1		Ω
	Power-on overshoot	AV_{DD} 0 to 5 V, 2 ms ramp		10		mV
	Glitch energy	Transition: Code 0x1FF to 0x200; 0x200 to 0x1FF		0.15		nV-s
	Output noise	T_A = 25°C, 1 kHz		260		nV/√Hz
		Integrated noise from 0.1 Hz to 10 Hz		20		μV_{PP}

(1) Specified by design and characterization. Not tested during production.

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ELECTRICAL CHARACTERISTICS – (ADC SPECIFICATIONS)

AV_{DD} = 4.75 to 5.5 V, $GPIOV_{DD}$ = 1.8 to 5.5 V, $SPIV_{DD}$ = 1.8 to 5.5 V, AGND = DGND = 0 V, External ADC reference = AV_{DD}, T_A = –40°C to 105°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC ACCURACY						
	Resolution		10			Bits
INL	Integral nonlinearity			±0.1	±1	LSB
DNL	Differential nonlinearity	Specified monotonic		±0.1	±1	LSB
	Offset error			±0.5	±2	LSB
	Offset error match			±0.4		LSB
	Gain error			±0.5	±2	LSB
	Gain error match			±0.4		LSB
CONVERSION TIME						
	ADC conversion rate			500		kSPS
	Autocycle update rate	All 8 ADC input channels enabled		16		µs
	Throughput rate	SCLK ≥ 12 MHz, single analog channel			500	kSPS
	Conversion delay	Delay from trigger to conversion start	2		4	µs
ANALOG INPUT						
	Absolute input voltage range	Independent of gain setting	AGND – 0.2		AV_{DD} + 0.2	V
	Full scale input voltage range	Gain = 1, *adcn_gain* = '0'	0		V_{REF}	V
		Gain = 2, *adcn_gain* = '1'	0		2 × V_{REF}	V
	Input capacitance (1)			40		pF
	DC input leakage current	Measured with ADC in Hold mode			±1	µA
AC PERFORMANCE						
SFDR	Spurious Free Dynamic Range	f_{IN} = 1 kHz, –1 dBFS sine wave		76		dBc
SNR	Signal to Noise Ratio	f_{IN} = 1 kHz, –1 dBFS sine wave		61		dBc
SINAD	Signal to Noise+Distortion Ratio	f_{IN} = 1 kHz, –1 dBFS sine wave		60.5		dBc
THD	Total Harmonic Distortion	f_{IN} = 1 kHz, –1 dBFS sine wave, Measured up to the fifth harmonic		75		dBc
INTERNAL ADC REFERENCE (2)						
V_{REF}	Reference output voltage	Internal ADC reference buffered output at REF pin		2.5		V
	Reference buffer power	AV_{DD} = 5 V		360		µA
	Reference temperature coefficient			10		ppm/°C
EXTERNAL ADC REFERENCE						
V_{REF}	Reference input voltage	External ADC reference input to REF pin	0.3		AVDD	V
	Input resistance (1)	V_{REF} = 5 V, AIN = 5 V		20		kΩ
TEMPERATURE SENSOR						
	Operating range		–40		125	°C
	Accuracy	T_A = –40°C to 125°C, AV_{DD} = 5 V		±1	±2.5	°C
	Resolution	LSB size		0.125		°C
	Conversion time			15		ms

(1) Specified by design. Not tested during production.
(2) Use an external buffer amplifier with high impedance input to drive any external load.

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ELECTRICAL CHARACTERISTICS – GENERAL SPECIFICATIONS

AV_{DD} = 4.75 to 5.5 V, $GPIOV_{DD}$ = 1.8 to 5.5 V, $SPIV_{DD}$ = 1.8 to 5.5 V, AGND = DGND = 0 V, External ADC reference = AV_{DD}, T_A = –40°C to 105°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL PURPOSE I/O						
V_{IH}	High-level input voltage	$GPIOV_{DD}$ = 1.8 V	0.7×$GPIOV_{DD}$			V
		$GPIOV_{DD}$ = 3.3 to 5.5 V	2.1			V
V_{IL}	Low-level input voltage	$GPIOV_{DD}$ = 1.8 V			0.3	V
		$GPIOV_{DD}$ = 3.3 to 5.5 V			0.8	V
V_{OH}	High-level output voltage	I_{load} = 1.6 mA, $GPIOV_{DD}$ = 1.8V, All GPIOs loaded and set to '1'	$GPIOV_{DD}$ - 0.25			V
		I_{load} = 1.6 mA, $GPIOV_{DD}$ = 3.3 to 5.5V, All GPIOs loaded and set to '1'	$GPIOV_{DD}$ - 0.2			V
V_{OL}	Low-level output voltage	I_{load} = -1.6 mA, All GPIOs loaded			0.4	V
	Input capacitance (1)			1		pF
	High impedance output capacitance (1)			1		pF
LOGIC INPUTS: $\overline{CS}$, SDI, SCLK						
V_{IH}	High-level input voltage	$SPIV_{DD}$ = 1.8 V	0.7×$SPIV_{DD}$			V
		$SPIV_{DD}$ = 3.3 to 5.5 V	2.1			V
V_{IL}	Low-level input voltage	$SPIV_{DD}$ = 1.8 V			0.3	V
		$SPIV_{DD}$ = 3.3 to 5.5 V			0.7	V
	Input current				±1	µA
	Input capacitance (1)			1		pF
	High impedance output capacitance (1)			1		pF
LOGIC OUTPUT: SDO						
V_{OH}	High-level output voltage	I_{load} = 1.6 mA	$SPIV_{DD}$ - 0.2			V
V_{OL}	Low-level output voltage	I_{load} = -1.6 mA			0.4	V
LOGIC OUTPUT: $\overline{DAV}$						
V_{OL}	Low-level output voltage	I_{load} = -2 mA			0.4	V
POWER REQUIREMENTS						
	AV_{DD}		4.75	5	5.5	V
	$GPIOV_{DD}$		1.8		5.5	V
	$SPIV_{DD}$		1.8		5.5	V
I_{DD}	Total supply current, AV_{DD} + $GPIOV_{DD}$ + $SPIV_{DD}$	Operating mode (2)		6.5	10	mA
		Power down mode		1.25	2	mA
	Power consumption	Operating mode (2)		32.5	55	mW
		Power down mode		6.25	11	mW
OPERATING RANGE						
	Specified temperature range		–40	25	105	°C

(1) Specified by design. Not tested in production.
(2) AV_{DD} = $GPIOV_{DD}$ = $SPIV_{DD}$ = 5 V. No DAC load, all DACs at 0x200 code and ADC at the fastest auto conversion rate.

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TIMING SPECIFICATIONS(1)(2)

AV_{DD} = 4.75 to 5.5 V, $GPIOV_{DD}$ = 1.8 to 5.5 V, $SPIV_{DD}$ = 1.8 to 5.5 V, AGND = DGND = 0 V, External ADC reference = AV_{DD}, T_A = –40°C to 105°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency	$SPIV_{DD}$ = 5.5 V			30	MHz
		$SPIV_{DD}$ = 2.7 V			15	MHz
		$SPIV_{DD}$ = 1.8 V			10	MHz
t_R	Input rise time	10% to 90% of $SPIV_{DD}$			2	ns
t_F	Input fall time	10% to 90% of $SPIV_{DD}$			2	ns
t_1	SCLK cycle time	$SPIV_{DD}$ = 5.5 V	33			ns
		$SPIV_{DD}$ = 2.7 V	66			ns
		$SPIV_{DD}$ = 1.8 V	100			ns
t_2	SCLK high time	$SPIV_{DD}$ = 5.5 V	13			ns
		$SPIV_{DD}$ = 2.7 V	30			ns
		$SPIV_{DD}$ = 1.8 V	50			ns
t_3	SCLK low time	$SPIV_{DD}$ = 5.5 V	13			ns
		$SPIV_{DD}$ = 2.7 V	26			ns
		$SPIV_{DD}$ = 1.8 V	40			ns
t_4	Frame start time	$\overline{CS}$ falling edge to SCLK rising edge	5			ns
t_5	SDI setup time	SDI valid to falling edge of SCLK	4			ns
t_6	SDI hold time	SDI valid after falling edge of SCLK	12			ns
t_7	Frame stop time	SCLK falling edge to $\overline{CS}$ rising edge	15			ns
t_8	$\overline{CS}$ high time		50			ns
t_9	SDO delay	$SPIV_{DD}$ = 5.5 V, C_L = 10 pF, 1 ns ≤ $t_{R,F(SDO)}$ ≤ 4 ns	5		16	ns
		$SPIV_{DD}$ = 2.7 V, C_L = 10 pF, 1 ns ≤ $t_{R,F(SDO)}$ ≤ 5 ns	6		22	ns
		$SPIV_{DD}$ = 1.8 V, C_L = 10 pF, 2 ns ≤ $t_{R,F(SDO)}$ ≤ 8 ns	8		39	ns
t_{10}	Wait time	$\overline{CS}$ rising edge to next SCLK rising edge	5			ns

(1) Specified by design. Not tested during production.
(2) Digital inputs and outputs timed from a voltage level of $SPIV_{DD}/2$.

TIMING INFORMATION

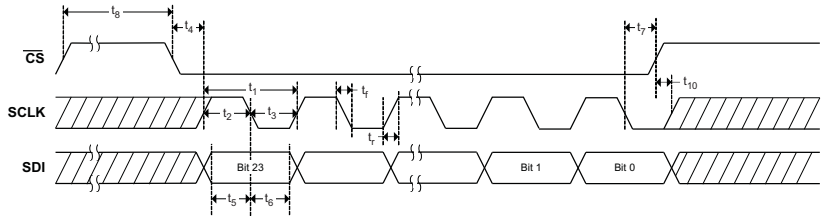


Figure 1. Serial Interface Write Timing Diagram

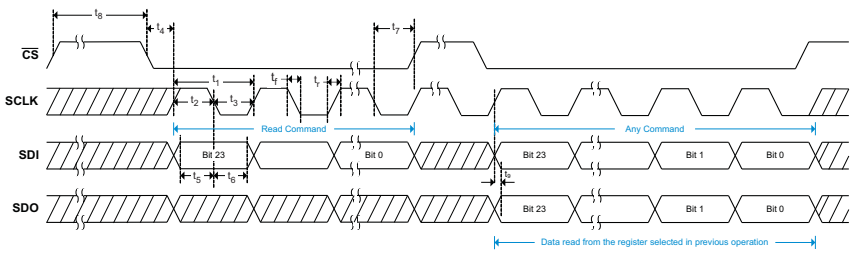


Figure 2. Serial Interface Read Timing Diagram

TYPICAL CHARACTERISTICS: DAC

AV_{DD} = 5 V, $GPIOV_{DD}$ = 5 V, $SPIV_{DD}$ = 5 V, AGND = DGND = 0 V, External ADC reference = AV_{DD} (unless otherwise noted)

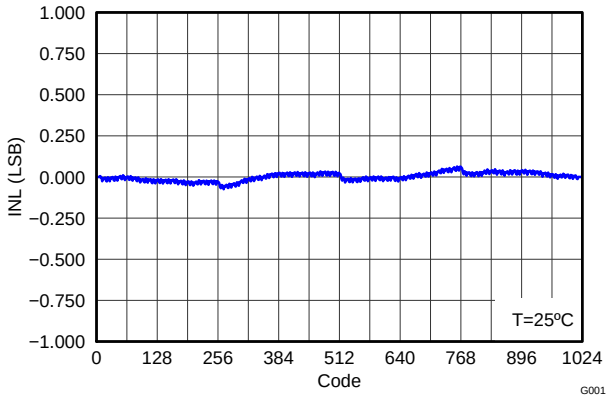


Figure 3. DAC INTEGRAL NON-LINEARITY

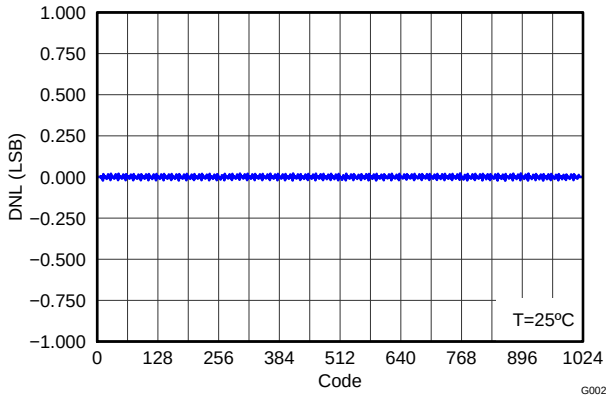


Figure 4. DAC DIFFERENTIAL NON-LINEARITY

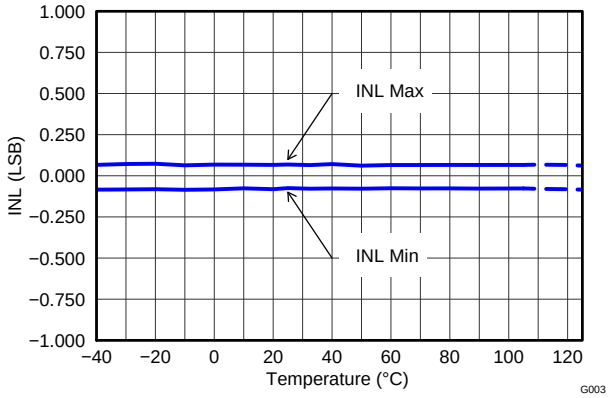


Figure 5. DAC INL vs. TEMPERATURE

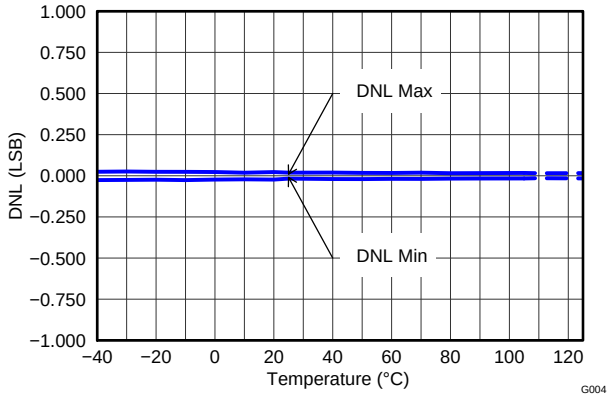


Figure 6. DAC DNL vs. TEMPERATURE

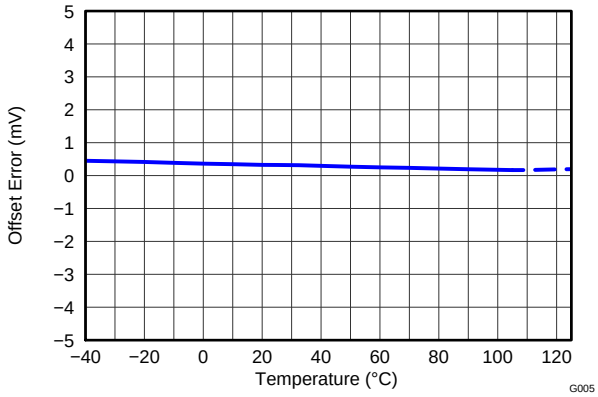


Figure 7. DAC OFFSET ERROR vs. TEMPERATURE

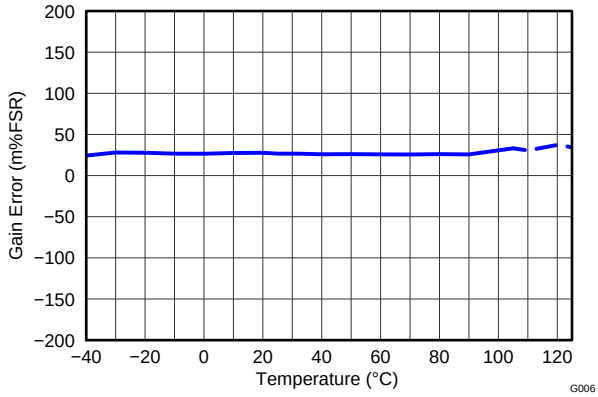


Figure 8. DAC GAIN ERROR vs. TEMPERATURE

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TYPICAL CHARACTERISTICS: DAC (continued)

AV_{DD} = 5 V, $GPIOV_{DD}$ = 5 V, $SPIV_{DD}$ = 5 V, AGND = DGND = 0 V, External ADC reference = AV_{DD} (unless otherwise noted)

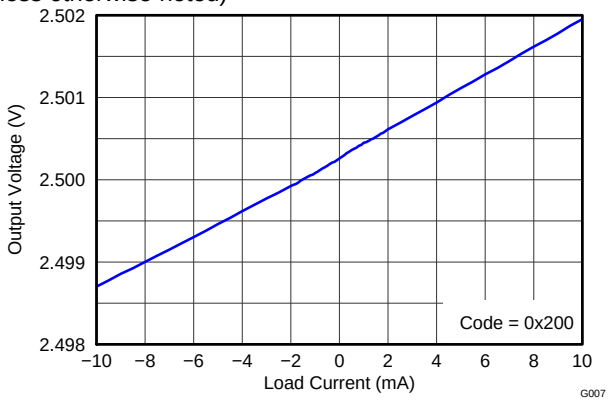


Figure 9. DAC OUTPUT VOLTAGE vs. LOAD CURRENT

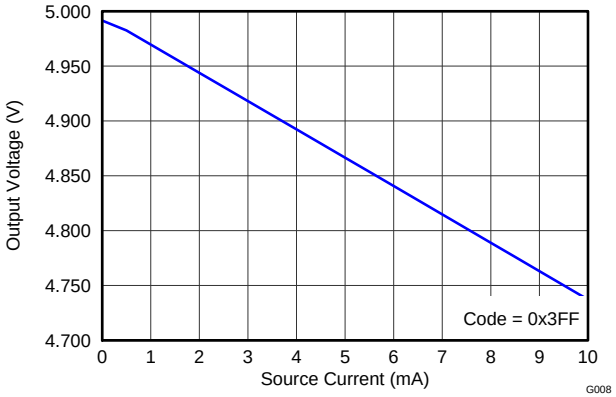


Figure 10. DAC SOURCE CURRENT

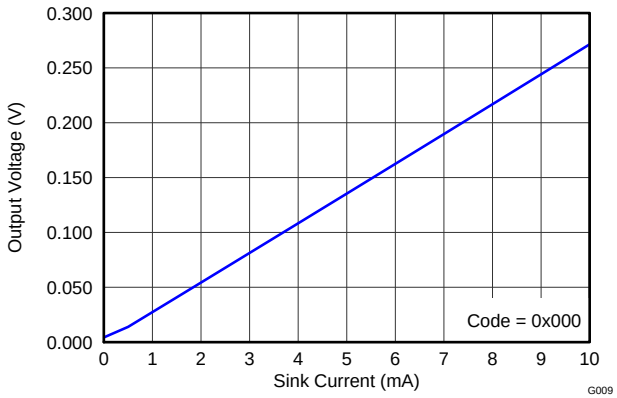


Figure 11. DAC SINK CURRENT

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TYPICAL CHARACTERISTICS: ADC

AV_{DD} = 5 V, $GPIOV_{DD}$ = 5 V, $SPIV_{DD}$ = 5 V, AGND = DGND = 0 V, External ADC reference = AV_{DD} (unless otherwise noted)

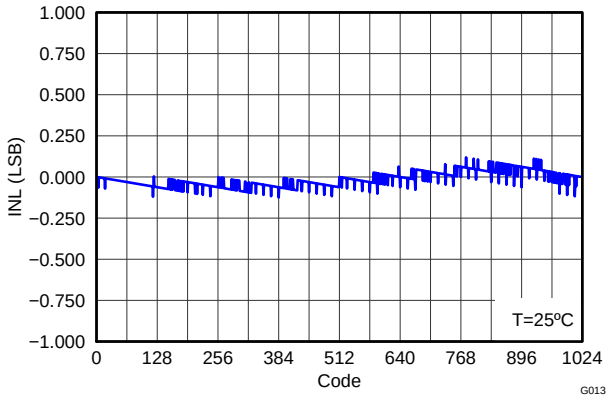


Figure 12. ADC INTEGRAL NON-LINEARITY

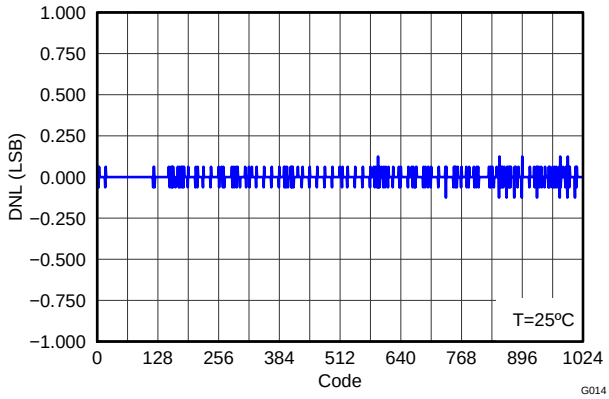


Figure 13. ADC DIFFERENTIAL NON-LINEARITY

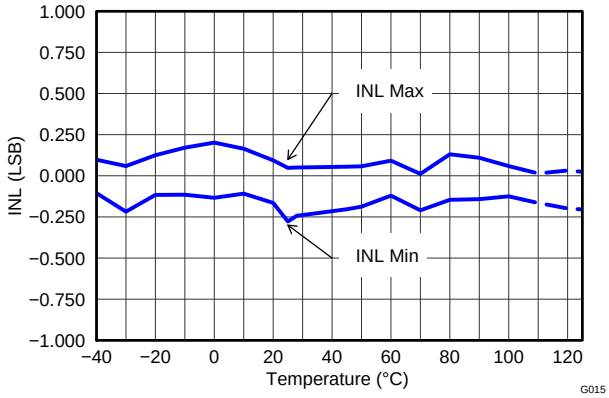


Figure 14. ADC INL vs. TEMPERATURE

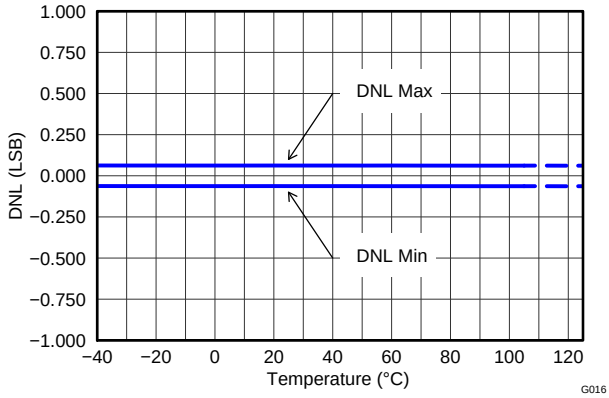


Figure 15. ADC DNL vs. TEMPERATURE

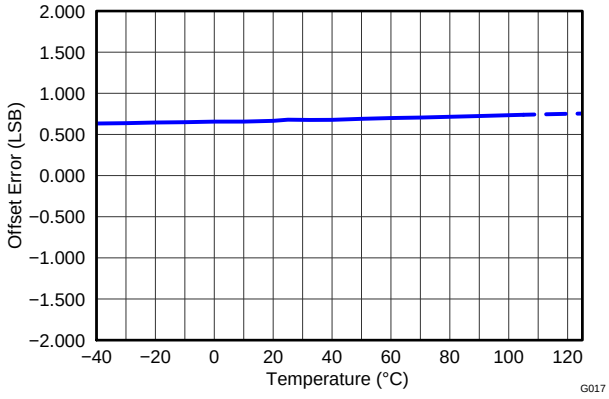


Figure 16. ADC OFFSET ERROR vs. TEMPERATURE

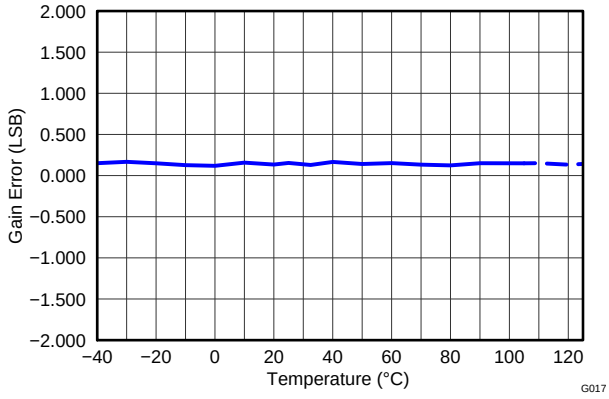


Figure 17. ADC GAIN ERROR vs. TEMPERATURE

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TYPICAL CHARACTERISTICS: ADC (continued)

AV_{DD} = 5 V, $GPIOV_{DD}$ = 5 V, $SPIV_{DD}$ = 5 V, AGND = DGND = 0 V, External ADC reference = AV_{DD} (unless otherwise noted)

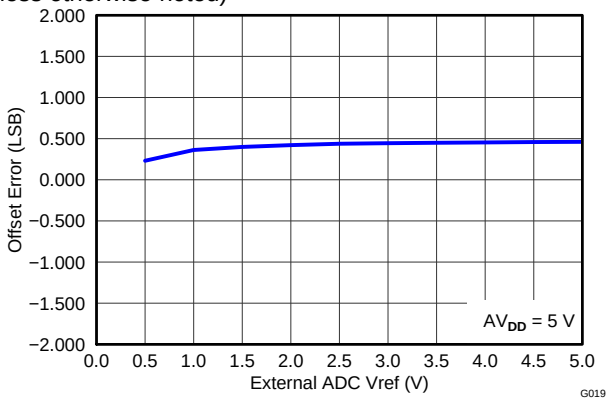


Figure 18. ADC OFFSET ERROR vs. REFERENCE VOLTAGE

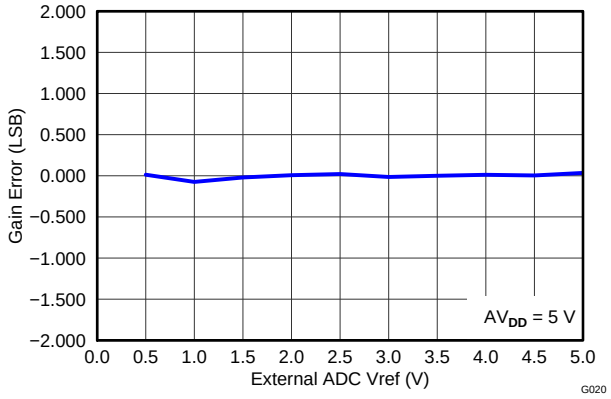


Figure 19. ADC GAIN ERROR vs. REFERENCE VOLTAGE

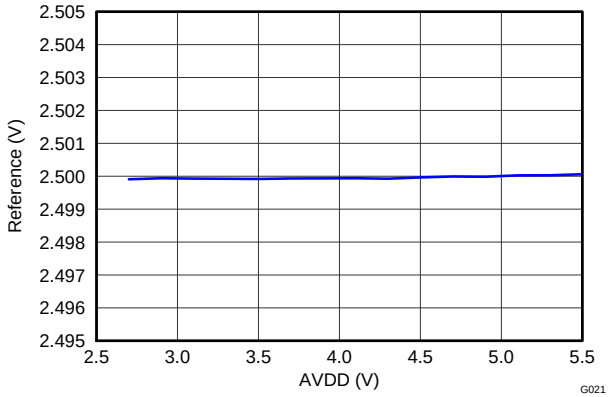


Figure 20. ADC INTERNAL REFERENCE vs. AVDD

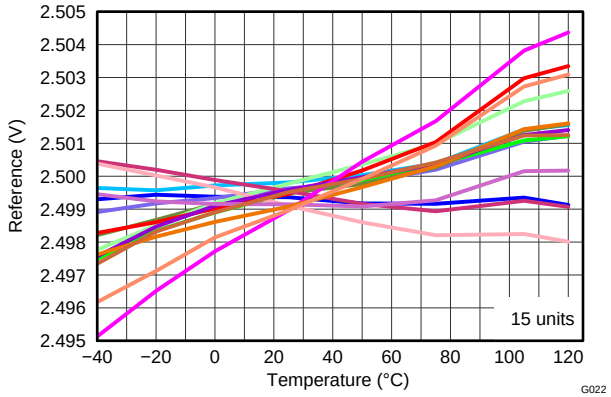


Figure 21. ADC INTERNAL REFERENCE vs. TEMPERATURE

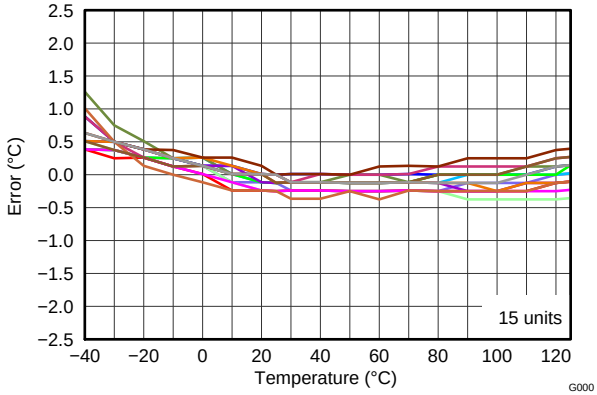


Figure 22. TEMPERATURE SENSOR ERROR vs TEMPERATURE

THEORY OF OPERATION

SERIAL INTERFACE

The AMC7891 is controlled through a flexible four-wire serial interface compatible with industry standard microprocessors and microcontrollers. The interface provides read/write access to all registers of the AMC7891 with clock rates up to 30 MHz.

The interface is compatible with most synchronous transfer formats and is configured as a 4 pin interface. SCLK is the serial interface input clock and $\overline{CS}$ is serial interface enable. Data is input into SDI and latched into the 24-bit wide SPI shift register on SCLK falling edges, while $\overline{CS}$ is low. Data is clocked out of SDO on SCLK rising edges, while $\overline{CS}$ is low. The contents of the SPI shift register are loaded into the device internal register on a $\overline{CS}$ rising edge after some delay. When $\overline{CS}$ is high, both SCLK and SDI inputs are blocked out and the SDO output is in high-impedance state.

The serial interface works with both a continuous and a non-continuous serial clock. A continuous SCLK source can only be used if $\overline{CS}$ is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used and $\overline{CS}$ must be taken high after the final clock to latch the data.

Each SPI command is input to SDI and framed by signal $\overline{CS}$ (Serial Data Enable) asserted low. The frame's first byte into SDI is the instruction cycle which identifies the request as a read or write as well as the 7-bit address to be accessed. The following two bytes in the frame form the data cycle.

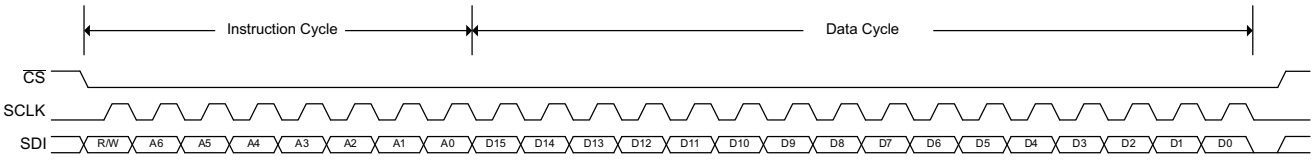


Figure 23. Serial Interface Command

Bit 23 **R/W**. Identifies the communication as a read or write command to the addressed register. Bit = '0' sets the write operation. Bit = '1' sets the read operation.

Bits[22:16] **A[6:0].** Register address; specifies the register to be accessed during the read or write operation.

Bits[15:0] **D[15:0].** Data cycle bits.
If a write command, the data cycle bits are the values to be written to the register with address A[6:0].
If a read command, the data cycle bits are *don't care* values.

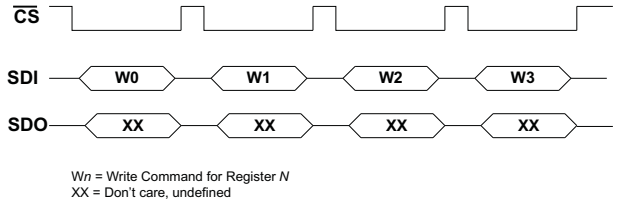
A read command causes an output on the SDO pin during the next SPI command cycle. The SDO read value frame is formed by the previous communication instruction cycle and the data read from the specified register.

Table 1. Serial Data Format

SPI FRAME	PIN	INSTRUCTION CYCLE		DATA CYLE
		Bit 23	Bits [22:16]	Bits [15:0]
Write Command Frame	SDI	0 (R/W)	A[6:0]	Data In[15:0]
	SDO	Undefined or Read Value Frame depending on previous command		
Read Command Frame	SDI	1 (R/W)	A[6:0]	Don't care
	SDO	Undefined or Read Value Frame depending on previous command		
Read Value Frame	SDI	New Write or Read Command Frame		
	SDO	1 (R/W)	A[6:0]	Data Out[15:0]

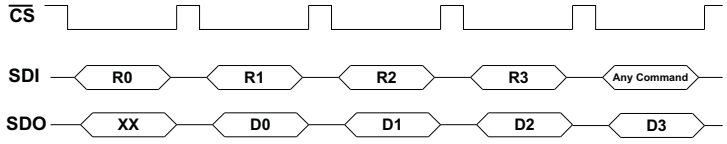
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The serial clock can be continuous or gated as long as there are exactly 24 falling clock edges within the frame. A write command issued in frames whose width is not 24 bits is incorrect and ignored by the AMC7891. A read command frame not equal to 24 bits may result in abnormal data on SDO and must be ignored by the host processor. In order for another serial transfer to occur, $\overline{CS}$ must be brought low again to start a new cycle. Figure 24 and Figure 25 show multiple write and read operations.



W*n* = Write Command for Register *N*
XX = Don't care, undefined

Figure 24. Serial Interface Write Operation



R*n* = Read Command for Register *N*
D*n* = Data from Register *N*
XX = Don't care, undefined

Figure 25. Serial Interface Read Operation

REGISTER MAP

The AMC7891 has 16-bit registers containing device configuration and conversion results. A 7-bit register address indicates the proper register.

Table 2. Register Map

			MSB															LSB
NAME	**ADDR**	**DEFAULT**	**BIT 15**	**BIT 14**	**BIT 13**	**BIT 12**	**BIT 11**	**BIT 10**	**BIT 9**	**BIT 8**	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
TEMP_data	0x00	0x0000	0	0	0	0	*tempdata(11:0)*											
TEMP_config	0x0A	0x0008	0	0	0	0	0	0	0	0	0	0	0	0	*temp_en*	0	0	0
TEMP_rate	0x0B	0x0007	0	0	0	0	0	0	0	0	0	0	0	0	0	*temp_rate(2:0)*		
ADC0_data	0x23	0x0000	0	0	0	0	0	0	*adc0_data(9:0)*									
ADC1_data	0x24	0x0000	0	0	0	0	0	0	*adc1_data(9:0)*									
ADC2_data	0x25	0x0000	0	0	0	0	0	0	*adc2_data(9:0)*									
ADC3_data	0x26	0x0000	0	0	0	0	0	0	*adc3_data(9:0)*									
ADC4_data	0x27	0x0000	0	0	0	0	0	0	*adc4_data(9:0)*									
ADC5_data	0x28	0x0000	0	0	0	0	0	0	*adc5_data(9:0)*									
ADC6_data	0x29	0x0000	0	0	0	0	0	0	*adc6_data(9:0)*									
ADC7_data	0x2A	0x0000	0	0	0	0	0	0	*adc7_data(9:0)*									
DAC0_data	0x2B	0x0000	0	0	0	0	0	0	*dac0_data(9:0)*									
DAC1_data	0x2C	0x0000	0	0	0	0	0	0	*dac1_data(9:0)*									
DAC2_data	0x2D	0x0000	0	0	0	0	0	0	*dac2_data(9:0)*									
DAC3_data	0x2E	0x0000	0	0	0	0	0	0	*dac3_data(9:0)*									
DAC0_clear	0x2F	0x0000	0	0	0	0	0	0	*dac0_clear(9:0)*									
DAC1_clear	0x30	0x0000	0	0	0	0	0	0	*dac1_clear(9:0)*									
DAC2_clear	0x31	0x0000	0	0	0	0	0	0	*dac2_clear(9:0)*									
DAC3_clear	0x32	0x0000	0	0	0	0	0	0	*dac3_clear(9:0)*									
GPIO_config	0x33	0x0000	0	0	0	0	*ioc3_io*	*ioc2_io*	*ioc1_io*	*ioc0_io*	*iob3_io*	*iob2_io*	*iob1_io*	*iob0_io*	*ioa3_io*	*ioa2_io*	*ioa1_io*	*ioa0_io*
GPIO_out	0x34	0x0000	0	0	0	0	*ioc3_out*	*ioc2_out*	*ioc1_out*	*ioc0_out*	*iob3_out*	*iob2_out*	*iob1_out*	*iob0_out*	*ioa3_out*	*ioa2_out*	*ioa1_out*	*ioa0_out*
GPIO_in	0x35	NA	0	0	0	0	*ioc3_in*	*ioc2_in*	*ioc1_in*	*ioc0_in*	*iob3_in*	*iob2_in*	*iob1_in*	*iob0_in*	*ioa3_in*	*ioa2_in*	*ioa1_in*	*ioa0_in*
AMC_config	0x36	0x2000	0	0	*adc_mode*	*adc_trig*	*dac_load*	resvd	*adc_rate(1:0)*		*adc_ready*	0	0	0	0	0	0	0
ADC_enable	0x37	0x0000	0	*adc0_en*	adc1_en	resvd	*adc2_en*	*adc3_en*	resvd	*adc4_en*	*adc5_en*	*adc6_en*	adc7_en	0	0	0	0	0
ADC_gain	0x38	0xFF00	*adc0_gain*	*adc1_gain*	*adc2_gain*	*adc3_gain*	*adc4_gain*	*adc5_gain*	*adc6_gain*	*adc7_gain*	0	0	0	0	0	0	0	0
DAC_clear	0x39	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	*dac3_clear*	*dac2_clear*	*dac1_clear*	*dac0_clear*
DAC_sync	0x3A	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	*dac3_sync*	*dac2_sync*	*dac1_sync*	*dac0_sync*
AMC_power	0x3B	0x0000	0	*adc_on*	*ref_on*	*dac0_on*	*dac1_on*	*dac2_on*	*dac3_on*	0	0	0	0	0	0	0	0	0
AMC_reset	0x3E	0x0000	reset(15:0)															
AMC_ID	0x40	0x0044	device_id(15:0)															

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REGISTER DESCRIPTIONS

Register name: temp_data – Address: 0x00, Default: 0x0000 (READ ONLY)

Register Name	Address	Bit	Name	Function	Default Value
temp_data	0x00	15:12	Reserved	Reserved for factory use.	All zeros
		11:0	temp_data(11:0)	Stores the temperature sensor reading in twos complement format. 0.125°C/LSB.	0x000

Register name: temp_config – Address: 0x0A, Default: 0x0008 (READ/WRITE)

Register Name	Address	Bit	Name	Function	Default Value
temp_config	0x0A	15:4	Reserved	Reserved for factory use.	All zeros
		3	temp_en	When set to '1', the on-chip temperature sensor is enabled.	1
		2:0	Reserved	Reserved for factory use.	All zeros

Register name: temp_rate – Address: 0x0B, Default: 0x0007 (READ/WRITE)

Register Name	Address	Bit	Name	Function	Default Value
temp_rate	0x0B	15:3	Reserved	Reserved for factory use.	All zeros
		2:0	temp_rate(2:0)	Sets the temperature sensor ADC conversion time	111

temp_rate(2:0)	Conversion time
000	128x
001	64x
010	32x
011	16x
100	8x
101	4x
110	2x
111	15 ms

Register name: ADCn_data – Address: 0x23 to 0x2A, Default: 0x0000 (READ ONLY)(1)

Register Name	Address	Bit	Name	Function	Default Value
ADC*n*_data	0x23 to 0x2A	15:10	Reserved	Reserved for factory use.	All zeros
		9:0	adcn_data(9:0)	Stores the 10-bit ADCn conversion results in straight binary format.	All zeros

Input Channel	ADC Register Value	Register Address
AIN_0	*adc0_data(9:0)*	0x23
AIN_1	*adc1_data(9:0)*	0x24
AIN_2	*adc2_data(9:0)*	0x25
AIN_3	*adc3_data(9:0)*	0x26
AIN_4	*adc4_data(9:0)*	0x27
AIN_5	*adc5_data(9:0)*	0x28
AIN_6	*adc6_data(9:0)*	0x29
AIN_7	*adc7_data(9:0)*	0x2A

(1) All ADCn_data registers are formatted in the manner shown here. n = 0, 1, …, 7

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Register name: DACn_data – Address: 0x2B to 0x2E, Default: 0x0000 (READ/WRITE)(1)

Register Name	Address	Bit	Name	Function	Default Value
DAC*n*_ data	0x2B to 0x2E	15:10	Reserved	Reserved for factory use.	All zeros
		9:0	dac*n*_data(9:0)	Stores the 10-bit data to be loaded to the DAC*n* latches in straight binary format.	All zeros

Output Channel	DAC Register Value	Register Address
DACOUT_0	*dac0_data(9:0)*	0x2B
DACOUT_1	*dac1_data(9:0)*	0x2C
DACOUT_2	*dac2_data(9:0)*	0x2D
DACOUT_3	*dac3_data(9:0)*	0x2E

(1) All DAC*n*_data registers are formatted in the manner shown here. *n* = 0, 1, …, 3

Register name: DACn_clear – Address: 0x2F to 0x32, Default: 0x0000 (READ/WRITE)(1)

Register Name	Address	Bit	Name	Function	Default Value
DAC*n*_ clear	0x2F to 0x32	15:10	Reserved	Reserved for factory use.	All zeros
		9:0	dac*n*_clear(9:0)	Stores the 10-bit data to be loaded to the DAC*n* when cleared. Straight binary format.	All zeros

Output Channel	DAC Clear Value	Register Address
DACOUT_0	*dac0_clear(9:0)*	0x2F
DACOUT_1	*dac1_clear(9:0)*	0x30
DACOUT_2	*dac2_clear(9:0)*	0x31
DACOUT_3	*dac3_clear(9:0)*	0x32

(1) All DAC*n*_data registers are formatted in the manner shown here. *n* = 0, 1, …, 3

Register name: GPIO_config – Address: 0x33, Default: 0x0000 (READ/WRITE)

Register Name	Address	Bit	Name	Function	Default Value
GPIO_config	0x33	15:12	Reserved	Reserved for factory use.	All zeros
		11	ioc3_io	When cleared to ‘0’ the corresponding GPIO is configured as an input and set on high-impedance state (default).	0
		10	ioc2_io		0
		9	ioc1_io	When set to ‘1’ the corresponding GPIO is configured as an output.	0
		8	ioc0_io		0
		7	iob3_io		0
		6	iob2_io		0
		5	iob1_io		0
		4	iob0_io		0
		3	ioa3_io		0
		2	ioa2_io		0
		1	ioa1_io		0
		0	ioa0_io		0

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Register name: GPIO_out – Address: 0x34, Default: 0x0000 (READ/WRITE)

Register Name	Address	Bit	Name	Function	Default Value
GPIO_out	0x34	15:12	Reserved	Reserved for factory use.	All zeros
		11	ioc3_out	If the corresponding GPIO is configured as an output in register *GPIO_config, 0x33*, the value on this bit sets the digital output. If the corresponding GPIO is configured as an input in register *GPIO_config, 0x33*, this bit is a don't care.	0
		10	ioc2_out		0
		9	ioc1_out		0
		8	ioc0_out		0
		7	iob3_out		0
		6	iob2_out		0
		5	iob1_out		0
		4	iob0_out		0
		3	ioa3_out		0
		2	ioa2_out		0
		1	ioa1_out		0
		0	ioa0_out		0

Register name: GPIO_in – Address: 0x35, Default: NA (READ ONLY)

Register Name	Address	Bit	Name	Function	Default Value
GPIO_in	0x35	15:12	Reserved	Reserved for factory use.	All zeros
		11	ioc3_in	If the corresponding GPIO is configured as an output in register *GPIO_config*, *0x33*, the value on this bit correspods to the digital output. If the corresponding GPIO is configured as an output in register *GPIO_config 0x33*, this bit matches the corresponding value in register *GPIO_out, 0x34*.	0
		10	ioc2_in		0
		9	ioc1_in		0
		8	ioc0_in		0
		7	iob3_in		0
		6	iob2_in		0
		5	iob1_in		0
		4	iob0_in		0
		3	ioa3_in		0
		2	ioa2_in		0
		1	ioa1_in		0
		0	ioa0_in		0

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Register name: AMC_config – Address: 0x36, Default: 0x2000 (READ/WRITE)

Register Name	Address	Bit	Name	Function	Default Value
AMC_config	0x36	15:4	Reserved	Reserved for factory use.	All zeros
		13	adc_mode	When set to '1', the ADC is in Auto-mode conversion. When cleared to '0', the ADC is in Direct-mode conversion.	1
		12	adc_trig	When set to '1' triggers a new ADC conversion cycle. The bit is cleared to '0' automatically after the ADC conversion cycle starts.	0
		11	dac_load	When set to '1' data is loaded into the DAC output channels set to synchronous mode in register *dac_sync*, 0x3A. The AMC7891 updates the DAC output only if the corresponding *dacn_data* register has been accessed since the last *dac_load* trigger. Any DAC channels that have not been accessed are not reloaded again.	0
		10	Reserved	Reserved for factory use.	0
		9:8	adc_rate(1:0)	Sets the primary ADC conversion rate **adc_rate(1:0)** / **Conversion time (kSPS)** 00 / 500 01 / 250 10 / 125 11 / 62.5	00
		7	adc_ready	ADC data available indicator in Direct-mode conversion. Always cleared to '0' in Auto-mode conversion. A '1' read from this bit indicates the ADC conversion cycle is complete and new data is available. A '0' read from this bit indicates the ADC conversion cycle is in progress or the ADC is in Auto-mode. To clear this bit one of the following events has to occur: 1. Reading the *adcn_data* registers. 2. Starting a new ADC conversion cycle.	0
		6:0	Reserved	Reserved for factory use.	All zeros

Register name: ADC_enable – Address: 0x37, Default: 0x0000 (READ/WRITE)

Register Name	Address	Bit	Name	Function	Default Value
ADC_enable	0x37	15	Reserved	Reserved for factory use.	All zeros
		14	adc0_en	When set to '1' the corresponding analog input channel AIN_n (n = 0, 1, …, 7) is accessed during an ADC conversion cycle. When cleared to '0' the corresponding input channel AIN_n (n = 0, 1, …, 7) is ignored during an ADC conversion cycle.	0
		13	adc1_en		0
		11	adc2_en		0
		10	adc3_en		0
		8	adc4_en		0
		7	adc5_en		0
		6	adc6_en		0
		5	adc7_en		0
		12,9	Reserved	Reserved for factory use. *Must be set to 0 for proper device operation.*	All zeros
		4:0	Reserved	Reserved for factory use.	All zeros

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Register name: ADC_gain – Address: 0x38, Default: 0xFF00 (READ/WRITE)

Register Name	Address	Bit	Name	Function	Default Value
ADC_gain	0x38	15	adc0_gain	When set to '1' the corresponding analog input channel AIN_*n* (*n* = 0, 1, …, 7) input range is 2 × V_{REF}.	1
		14	adc1_gain		1
		13	adc2_gain	When cleared to '0' the corresponding input channel AIN_*n* (*n* = 0, 1, …, 7) input range is V_{REF}.	1
		12	adc3_gain		1
		11	adc4_gain		1
		10	adc5_gain		1
		9	adc6_gain		1
		8	adc7_gain		1
		7:0	Reserved	Reserved for factory use.	All zeros

Register name: DAC_clear – Address: 0x39, Default: 0x0000 (READ/WRITE)

Register Name	Address	Bit	Name	Function	Default Value
ADC_clear	0x39	15:4	Reserved	Reserved for factory use.	All zeros
		3	dac3_clear	When set to '1' clears the corresponding DACout_*n* (*n* = 0, 1, …, 3) output to the value specified in register *dacn_clear*, 0x2F to 0x32.	0
		2	dac2_clear		0
		1	dac1_clear	When cleared to '0' the corresponding DACout_*n* (*n* = 0, 1, …, 3) output returns to normal operation.	0
		0	dac0_clear		0

Register name: DAC_sync – Address: 0x3A, Default: 0x0000 (READ/WRITE)

Register Name	Address	Bit	Name	Function	Default Value
DAC_sync	0x3A	15:4	Reserved	Reserved for factory use.	All zeros
		3	dac3_sync	When set to '1' clears the corresponding DACout_*n* (*n* = 0, 1, …, 3) is set to synchronous-mode.	0
		2	dac2_sync		0
		1	dac1_sync	When cleared to '0' the corresponding DACout_*n* (*n* = 0, 1, …, 3) is set to asynchronous-mode.	0
		0	dac0_sync		0

Register name: AMC_power – Address: 0x3B, Default: 0x0000 (READ/WRITE)

Register Name	Address	Bit	Name	Function	Default Value
AMC_power	0x3B	15	Reserved	Reserved for factory use.	0
		14	adc_on	When cleared to '0' the primary ADC is in power-down mode. When set to '1' the primary ADC is in active mode.	0
		13	ref_on	When cleared to '0' the internal reference buffer is in power-down mode; the device is in External ADC Reference mode and the REF pin is an input. When set to '1' the internal reference buffer is active; the device is in Internal ADC Reference mode and the REF pin is an output.	0
		12	dac0_on	When cleared to '0' DAC0 is in power-down mode. DACout_0 is in high-impedance state. When set to '1' DAC0 is in active mode.	0
		11	dac1_on	When cleared to '0' DAC1 is in power-down mode. DACout_1 is in high-impedance state. When set to '1' DAC1 is in active mode.	0
		10	dac2_on	When cleared to '0' DAC2 is in power-down mode. DACout_2 is in high-impedance state. When set to '1' DAC2 is in active mode.	0
		9	dac3_on	When cleared to '0' DAC3 is in power-down mode. DACout_3 is in high-impedance state. When set to '1' DAC3 is in active mode.	0
		8:0	Reserved	Reserved for factory use.	All zeros

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Register name: AMC_reset – Address: 0x3E, Default: 0x0000 (READ/WRITE)

Register Name	Address	Bit	Name	Function	Default Value
AMC_reset	0x3E	15:0	reset(15:0)	Writing 0x6600 to this register forces a reset operation. During reset, all SPI communication is blocked. After issuing the reset, there is a wait of at least 30 µs before communication can be resumed.	All zeros

Register name: AMC_ID – Address: 0x40, Default: 0x0044 (READ ONLY)

Register Name	Address	Bit	Name	Function	Default Value
AMC_ID	0x40	15:0	device_id(15:0)	A hardwired register that contains the AMC7891 ID.	0x0044

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ADC OPERATION

The AMC7891 has two analog-to-digital converters (ADCs): a primary ADC and a secondary ADC. The primary ADC consists of an 8-channel multiplexer, an on-chip track-and-hold, and a successive approximation register (SAR) ADC based on a capacitive digital-to-analog converter (DAC). This ADC runs at rates up to 500 kSPS and converts the uncommitted analog channel inputs, AIN0 to AIN7.

The analog input range for the device can be selected as 0 V to V_{REF} or 0 V to (2 × V_{REF}). The AMC7891 has an on-chip buffered 2.5V reference that can be disabled when an external reference is preferred. The secondary ADC is a part of the on-chip temperature sensing function.

PRIMARY ADC OPERATION

The following sections describe the operation of the primary ADC. The temperature sensor ADC always operates in the background.

ANALOG INPUT FULL SCALE RANGE

The values in register *ADC_gain* determine the full-scale range of the analog inputs. The full-scale range for input channel AIN*n* is V_{REF} when bit *adcn_gain* = 0, or 2 × V_{REF} when *adcn_gain* = 1. Each input must not exceed the supply value of AV_{DD} + 0.2 V or AGND – 0.2 V.

When internal ADC reference is enabled, the buffered internal reference is used as the ADC reference. When external ADC reference is selected, an external reference voltage applied to the REF pin is the ADC reference.

ANALOG INPUTS

The AMC7891 has 8 uncommitted single-ended analog inputs. Figure 26 shows the equivalent input circuit of the AMC7891. The (peak) input current through the analog inputs depends on the sample rate, input voltage, and source impedance. The current into the AMC7891 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance to a 10-bit settling level within the acquisition time. When the converter goes into hold mode, the input impedance is greater than 1 GΩ.

In applications where the signal source has high impedance, it is recommended to buffer the analog input before applying it to the ADC. The analog input range can be programmed to be either 0 V to V_{REF} or 0 V to (2 × V_{REF}). With a gain of 2, the input is effectively divided by two before the conversion takes place. Note that the voltage with respect to AGND on the ADC analog input cannot exceed AV_{DD}.

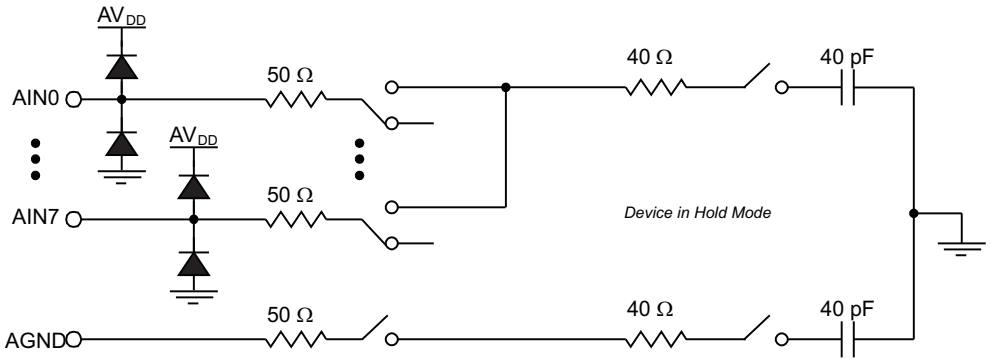


Figure 26. ADC Equivalent Input Circuit

ADC TRIGGER SIGNALS

The ADC can be triggered internally by writing to the *adc_trig* bit in register *AMC_config*. When a new trigger activates, the ADC stops any existing conversion immediately and starts a new cycle. For example, the ADC is programmed to sample input channels 0 to channel 3 repeatedly (auto-mode). During the conversion of channel 1, a trigger is activated. The ADC stops the conversion of channel 1 immediately and starts the conversion of channel 0 again, instead of proceeding to convert channel 2.

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CONVERSION MODES

Two types of ADC conversions are available: direct-mode and auto-mode. *adc_mode bit* (*AMC_config* register, bit 13) sets the conversion mode. The default conversion mode is auto-mode (*adc_mode* = '1').

In direct-mode conversion, each analog channel within the specified group in register *ADC_enable* is converted a single time. After the last channel is converted, the ADC goes into an idle state and waits for a new trigger.

Auto-mode conversion, on the other hand, is a continuous operation. In auto-mode, each analog channel within the specified group is converted sequentially and repeatedly.

The flow chart of the ADC conversion sequence in Figure 27 shows the conversion process.

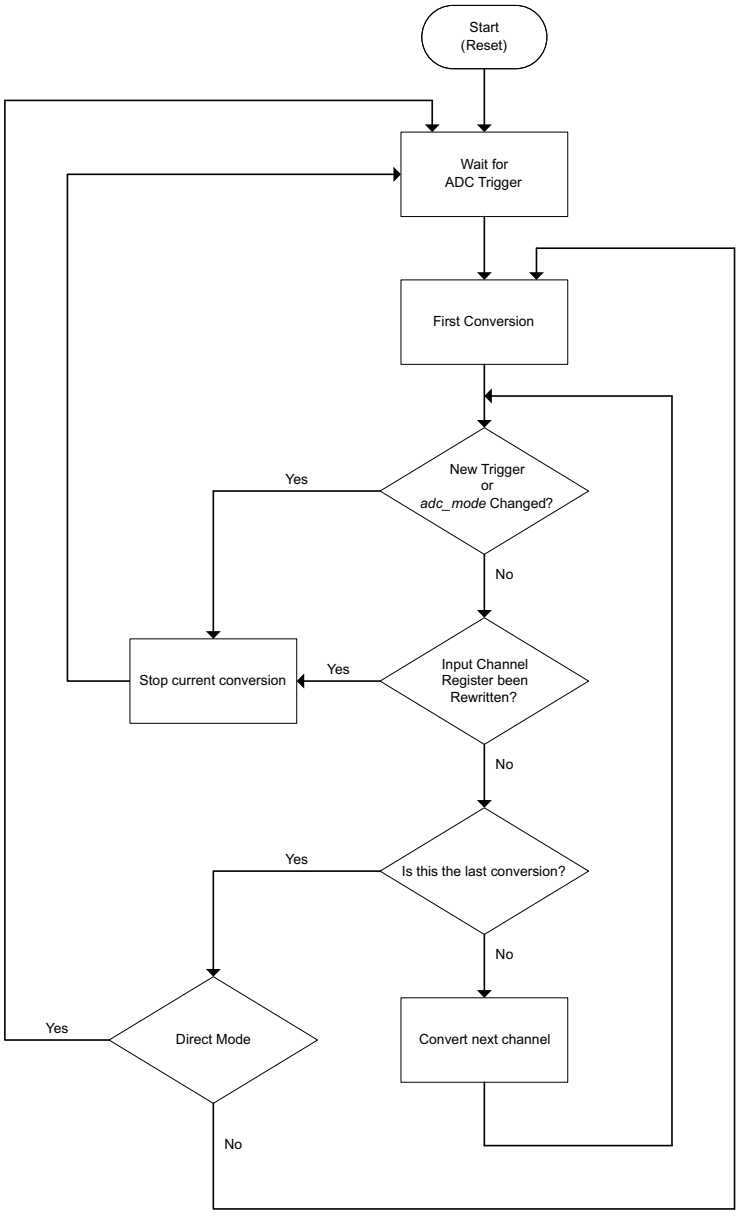


Figure 27. ADC Conversion Sequence

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When any of the following events occur, the current conversion cycle stops immediately:

- A new trigger is issued.
- The conversion mode changes.
- Either ADC channe register is rewritten.

When a new trigger activates, the ADC starts a new conversion cycle. The trigger should not be issued at the same time the conversion mode is changed. If a '1' is simultaneously written to the *adc_trig* bit when changing the adc_mode bit from '0' to '1', the current conversion stops and immediately returns to the *wait for ADC trigger* state.

To avoid noise caused by the bus clock, it is recommended that no bus clock activity occurs for at least the conversion process time immediately after the ADC conversion starts.

DOUBLE-BUFFERED ADC DATA REGISTER

The host can access all eight, double-buffered *ADCn_data* registers, as shown in Figure 28. The conversion result from the analog input with channel address *n*, (where n = 0 to 7) is stored in *adcn_data[9:0]* in straight binary format. When the conversion of an individual channel is completed, the data is immediately transferred into the corresponding *adcn_tmpry* temporary register, the first stage of the data buffer. When the conversion of the last channel completes, all data in the *adcn_tmpry* registers is simultaneously transferred to the corresponding *adcn_data[9:0]* value, the second stage of the data buffer.

In the case when a data transfer is in progress between any *ADCn_data* register and the AMC7891 shift register, all *ADCn_data* registers are not updated until the data transfer is complete.

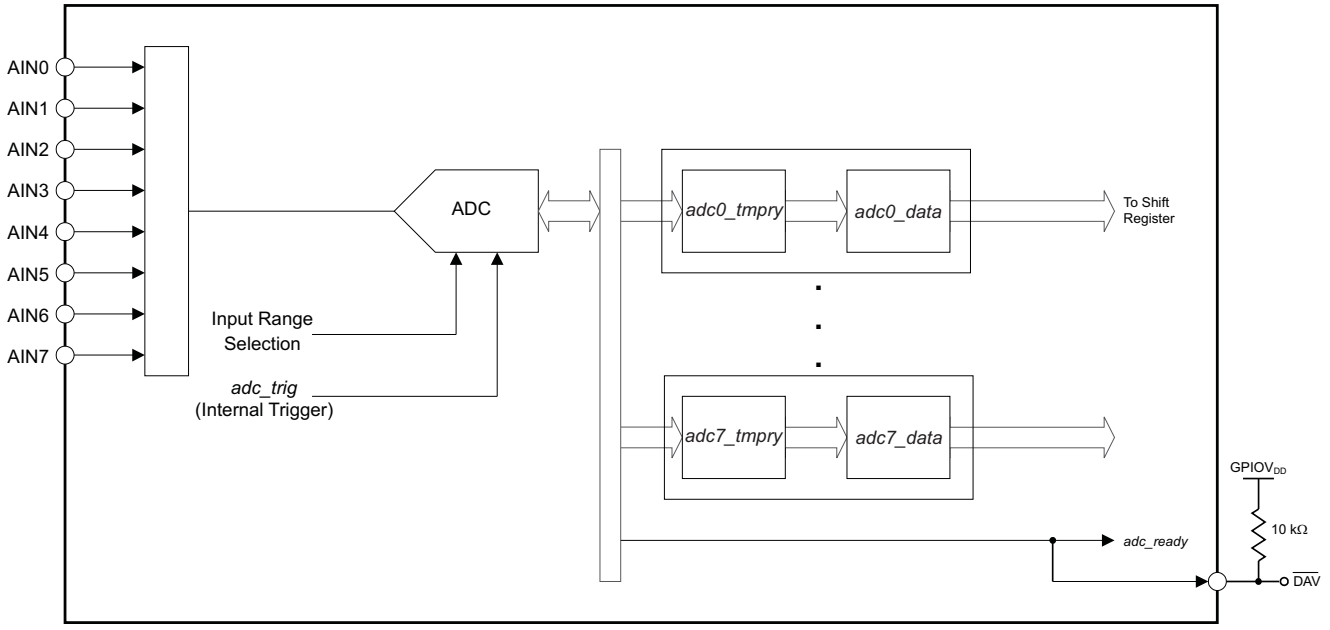


Figure 28. ADC Structure

PROGRAMMABLE CONVERSION RATE

The maximum ADC conversion rate is 500 kSPS for a single channel in auto mode, as shown in Table 3. The conversion rate is programmable through *adc_rate[1:0]* (*AMC_config* register, [9:8] bits). When more than one channel is selected, the conversion rate is divided by the number of channels selected in register *ADC_enable*.

In auto mode, the *adc_rate[1:0]* value determines the actual conversion rate. In direct mode, *adc_rate[1:0]* limits the maximum possible conversion rate. The actual conversion rate in direct mode is determined by the rate of the conversion trigger. Note that when a trigger is issued, there may be a delay of up to 4 µs to internally synchronize and initiate the start of the sequential channel conversion process. In both direct- and auto- modes, when *adc_rate[1:0]* is set to a value other than the maximum rate ('00'), nap mode is activated between conversions. By activating nap mode, the AV_{DD} supply current is reduced.

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Table 3. ADC Conversion Rate

adc_rate[1:0]	t_{ACQ} (µs)	t_{CONV} (µs)	NAP ENABLED	THROUGHPUT (Single-Channel Auto Mode)
00	0.375	1.625	No	500 kSPS (default)
01	2.375	1.625	Yes	250 kSPS
10	6.375	1.625	Yes	125 kSPS
11	14.375	1.625	Yes	62.5 kSPS

HANDSHAKING WITH THE HOST

The $\overline{DAV}$ pin and *adc_ready* bit (*AMC_config* register, bit 7) provide handshaking with the host. The $\overline{DAV}$ pin is an open-drain, active low output. If used, an external 10 kΩ pull-up resistor to $GPIOV_{DD}$ is required. If unused, the pin can be connected to DGND. Pin and bit status depend on the conversion mode (direct or auto), as shown in Figure 29.

In direct mode, after the *ADCn_data* registers of all the selected channels in register *adc_enable* are updated, *adc_ready* is set immediately to '1' and the $\overline{DAV}$ pin is active (low) to signify that new data is available.

The *adc_ready* bit is reset to '0' and the $\overline{DAV}$ pin goes back to inactive (high) either by reading any of the *ADCn_data* registers or when a new ADC conversion is started by issuing a trigger by *adc_trig*. The update takes place immediately after the read command frame indicating the read operation or trigger event.

In auto-mode, after the *adcn_data[9:0]* values are updated, a pulse of 1µs (low) appears on the $\overline{DAV}$ pin to signify that new data is available. However, the *adc_trig* bit is inactive and always set to '0'.

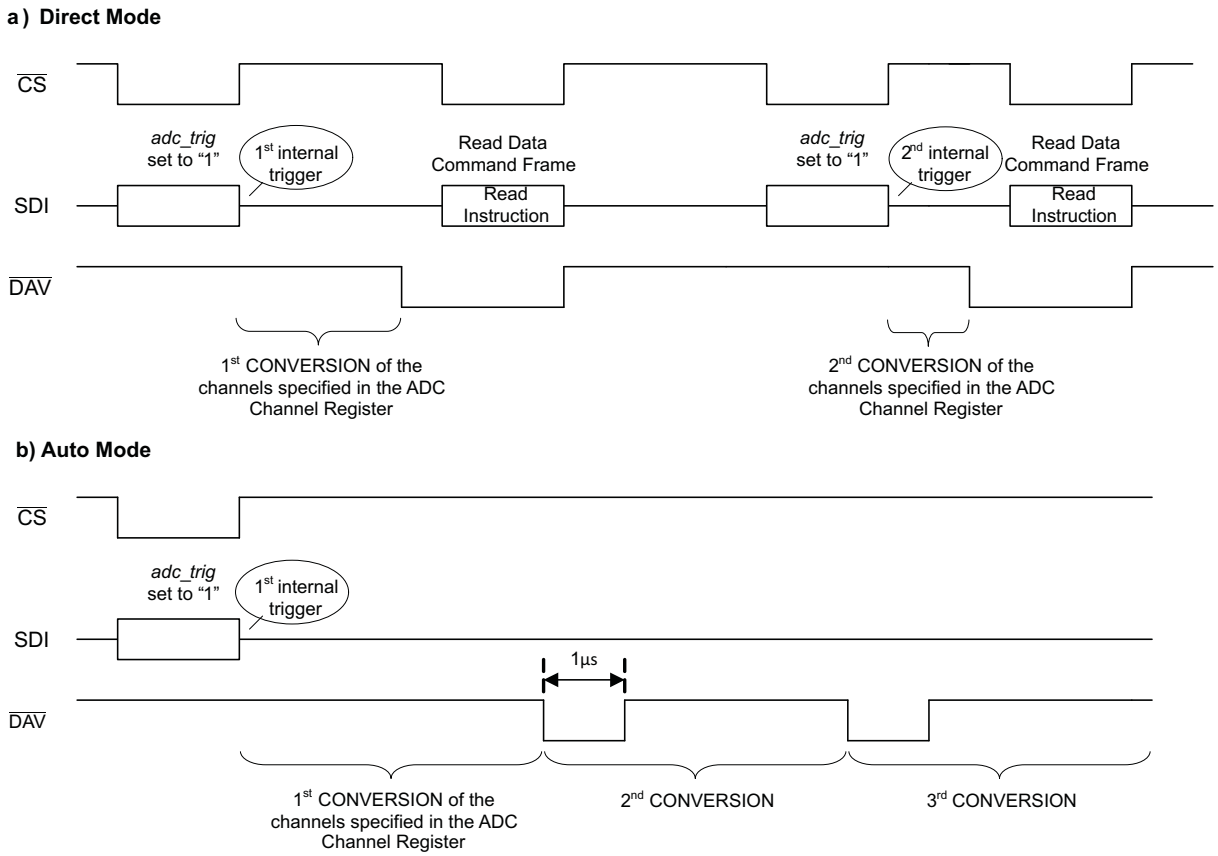


Figure 29. ADC Handshaking

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TEMPERATURE SENSOR OPERATION (SECONDARY ADC)

The AMC7891 contains an on-chip temperature sensor used to measure the device temperature. The temperature sensor is continuously monitoring, and new readings are automatically available every cycle. The analog temperature reading is converted by a secondary ADC that runs in the background at a lower speed than the primary ADC.

The temperature measurement relies on the characteristics of a semiconductor junction operating at a fixed current level. The forward voltage of the diode (V_{BE}) depends on the current passing through it and the ambient temperature. The change in V_{BE} when the diode operates at two different currents (a low current of I_{LOW} and a high current of I_{HIGH}, is shown in Equation 1:

$$V_{BE_HIGH} - V_{BE_LOW} = \eta kT/q \times \ln(I_{HIGH}/I_{LOW}) \quad (1)$$

Where:

k is Boltzmann's constant.
q is the charge of the carrier.
T is the absolute temperature in Kelvins (K).
η is the ideality of the transistor as sensor.

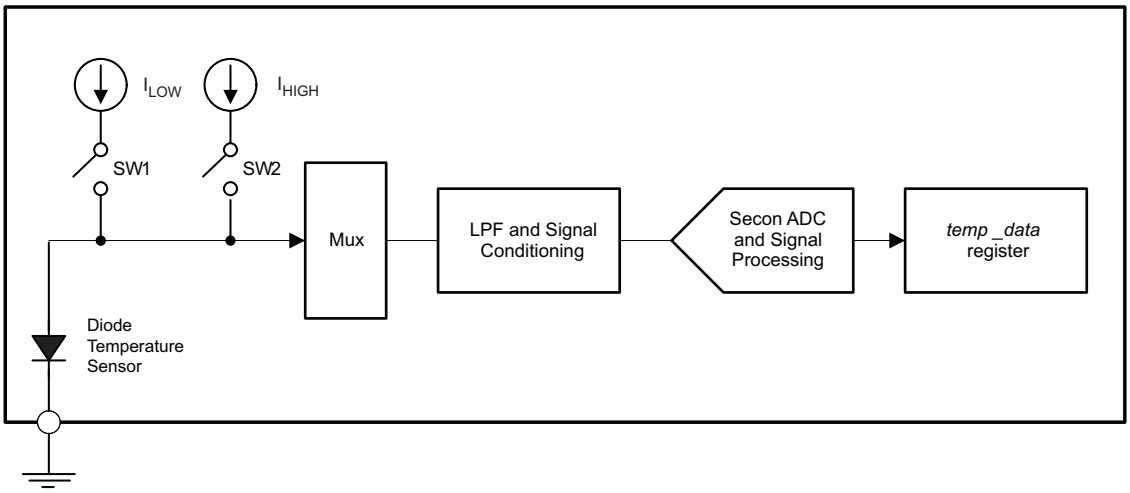


Figure 30. Integrated Temperature Sensor

The temperature sensor can be disabled by clearing to '0' the *temp_en* bit (*TEMP_config* register, bit 3). When disabled, the sensor is not converted. The AMC7891 continuously monitors the temperature sensor in the background, leaving the user free to perform conversions on the primary ADC. When one monitor cycle finishes, a signal passes to the control logic to automatically initiate a new conversion.

The analog sensing signal is preprocessed by a low-pass filter and signal conditioning circuitry, and then digitized by the secondary ADC. The resulting digital signal is further processed by the digital filter and processing unit. The final result is stored as a 12-bit value in the *TEMP_data* register as *tempdata[11:0]*. The format of the final result is in twos complement, as shown in Table 4. Note that the device measures the temperature from –40°C to 150°C.

If a data transfer is in progress between the *TEMP_data* register and the AMC Shift Register, the *TEMP_data* register is frozen until the data transfer is complete.

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Table 4. Temperature Data Format

TEMPERATURE (°C)	DIGITAL CODE
+255.875	011111111111
+150	010010110000
+100	001100100000
+50	000110010000
+25	000011001000
+1	000000001000
0	000000000000
–1	111111111000
–25	111100111000
–50	111001110000
–100	110011100000
–150	101101010000
–256	100000000000

The temperature conversion time is by default 15 ms but it can be increased by setting *temp_rate[2:0]* (*TEMP_rate* register, bits [2:0]) as shown in Table 5.

Table 5. Temperature Conversion Time

adc_rate[2:0]	CONVERSION TIME
000	128x
001	64x
010	32x
011	16x
100	8x
101	4x
110	2x
111	15 ms

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REFERENCE OPERATION

The AMC7891 includes a buffered internal reference for the ADC, DACs and temperature sensor. The internal reference is a 2.5 V, bipolar transistor-based, precision bandgap reference.

The internal reference always drives the DACs and the internal temperature sensor directly (unbuffered); however the ADC can be driven either by the internal reference (buffered) or by an external one as determined by the *ref_on* bit (*AMC_power* register, bit 13). If used, the external reference is applied to the dual purpose REF pin. A decoupling capacitor is recommended between the external reference output an AGND for noise filtering.

In internal ADC reference mode, the buffered internal reference is available at the REF pin. A compensating 4.7µF capacitor is recommended between the internal buffered reference output and AGND.

On power-up, the AMC7891 is configured for ADC external reference (*ref_on* bit cleared to '0'). In this case it is important that the external reference source is not input into the REF pin until AV_{DD} is stable. If using the internal reference to drive the ADC, the *ref_on* must be set to '1' to enable the internal reference buffer.

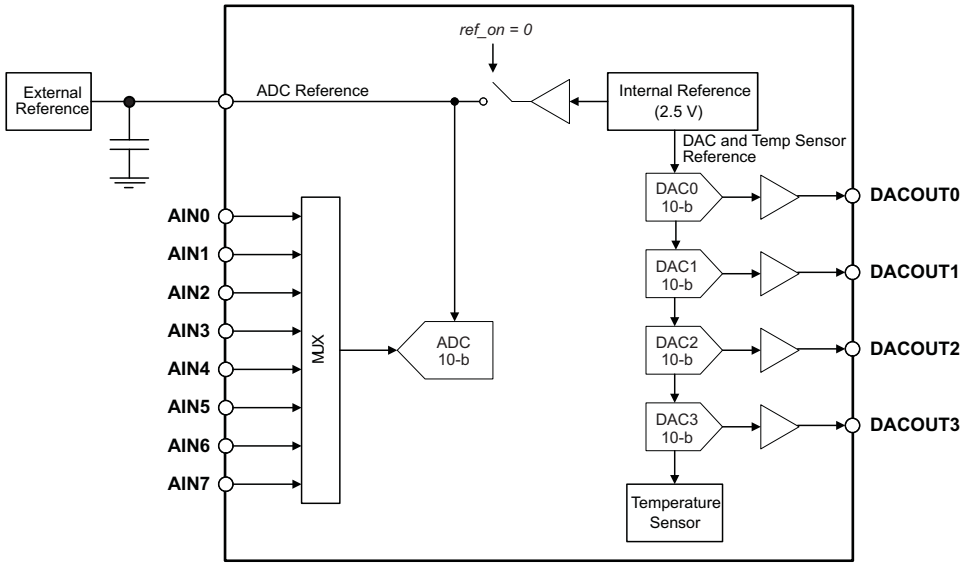


Figure 31. External ADC Reference

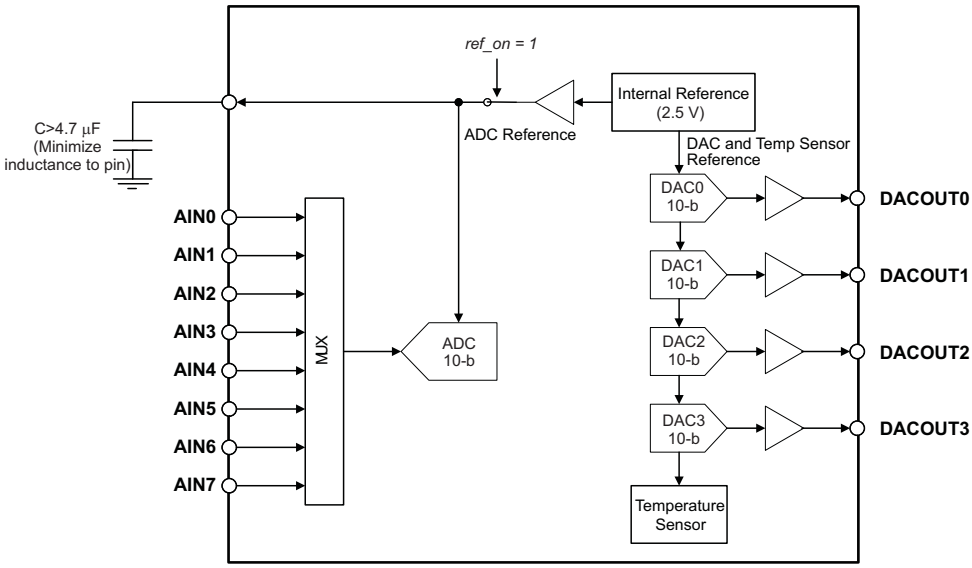


Figure 32. Internal ADC Reference

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DAC OPERATION

The AMC7891 contains 4 independent DACs that provide analog control with 10 bits of resolution using an internal reference. Each DAC core consists of a 10-bit string DAC and an output voltage buffer.

The DAC latch stores the code that determines the output voltage from the DAC string. The code is transferred from the *DACn_data* registers to the DACn data latches when the internal DAC load signal is generated.

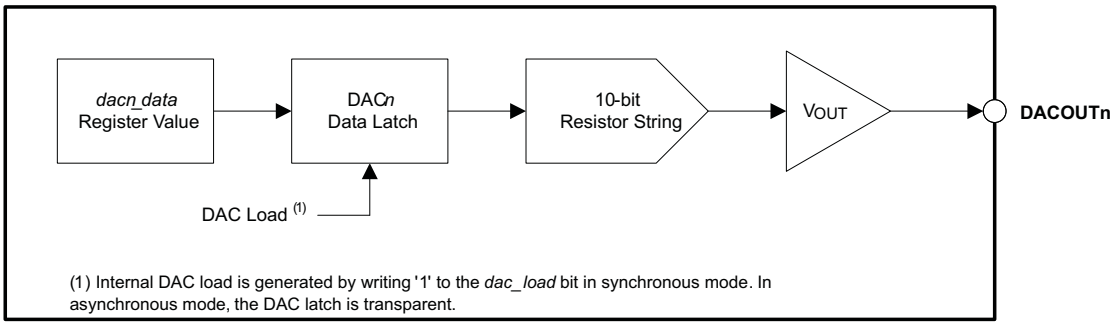


Figure 33. DAC Block Diagram

The resistor string structure is shown in Figure 34. It consists of a string of resistors, each of value R. The code loaded to the DAC Latch determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. This architecture has inherent monotonicity, voltage output, and low glitch. It is also linear because all the resistors are of equal value.

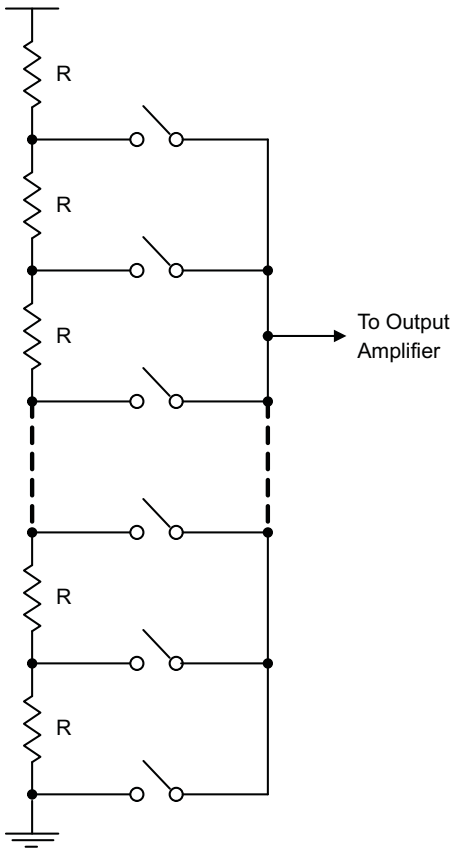


Figure 34. Resistor String

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DAC OUTPUT

The full-scale output range of each DAC is set by the product of the internal reference voltage times a fixed gain of 2 in the DAC output buffer ($2 \times V_{REF}$). The full-scale output range of each DAC is limited by the analog power supply. The maximum and minimum outputs from the DAC cannot exceed AV_{DD} or be lower than AGND, respectively.

After power-on or a reset event, the DAC output buffers are in power-down mode. In this mode all *dacn_data* registers and DAC*n* data latches are set to their default values, the output buffers are in a high-impedance state and each DACout*n* output pin connects to AGND through an internal 10 kΩ resistor.

DOUBLE-BUFFERED DAC DATA REGISTERS

There are 4 double-buffered DAC data registers. Each DAC has an internal latch preceded by a DAC data register. Data is initially written to the individual *DACn_data* register as the value *dacn_data[9:0]* and then transferred to its corresponding DAC*n* latch. When the DAC*n* latch is updated, the output from pin DACout*n* changes to the newly set value. When the host reads from *DACn_data*, the value held in the DAC*n* latch is returned (not the value held in the data register).

The DACs update mode is determined by the *dacn_sync* setting in the *DAC_sync* register. When *dacn_sync* is cleared to '0', the DAC*n* is in asynchronous mode. In asynchronous mode, a write to the *DACn_data* register results in an immediate update of the DACn latch and corresponding DACout*n* output.

Synchronous mode is selected by setting *dacn_sync* to '1'. In synchronous mode writing to the *DACn_data* register does not update the DAC*n* latch DACout*_n* output. Instead, the update occurs only until the *dac_load* bit (*AMC_config* register, bit 11) is set to '1'. By setting the *DAC_sync* register properly, several DACs can be updated at the same time.

Table 6. DAC Output Modes

MODE	*dacn_sync*	WRITING TO *dac_load*	OPERATION
Asynchronous	0	Don't care	Update DACn individually. The DAC*n* latch and DACout*n* output are immediately updated after writing to DACn_data.
Synchronous	1	1	Simultaneously update all DACs by internal trigger. Writing '1' to *dac_load* generates an internal load DAC trigger signal that updates the DAC*n* latches and DACout*n* outputs with the contents of the corresponding *dacn_data[9:0]* register values.

The AMC7891 updates the DAC latches only if it has been accessed since the last time *dac_load* was issued, thereby eliminating any unnecessary glitch. Any DAC channels that have not been accessed are not reloaded again. When the DAC latch is updated, the corresponding output changes to the new level immediately.

CLEAR DACS

Each DAC can be cleared using the *DAC_clear* register. When setting the corresponding *dacn_clear* bit to '1', DAC*n* goes to a clear state in which the DACout*n* is immediately updated with the predefined value in the *DACn_clear* register, regardless of the *dacn_sync* status. The data register value *dacn_data[9:0]* does not change.

When the DAC goes back to normal operation, the DACout*n* output is set back to the DAC*n* latch value regardless of the *dac_sync* status.

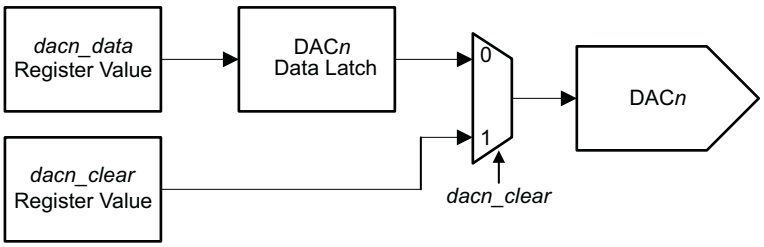


Figure 35. Clear DAC Operation

GENERAL PURPOSE INPUT/OUTPUT PINS

The AMC7891 has twelve GPIO pins. Each GPIO provides a bidirectional, digital I/O signal. These pins can receive an input or produce an output as configured by the *GPIO_config* register.

To configure the GPIOxx pin as an output, the corresponding *ioxx_io* bit needs to be set to '1'. The GPIOxx is an output driver with a pull to the value of the corresponding *ioxx_out* bit in register *GPIO_out*.

To set the *GPIOxx* pin as an input, the corresponding *ioxx_io* bit has to be cleared to '0'. In this mode the GPIOxx pin is in high-impedance state and the read value is stored in the corresponding *ioutxx_in* bit in register *GPIO_in*. When set as an input, writes to the *GPIO_out* register do not affect the GPIO values.

After a power-on or reset event, all the GPIO pins are set as inputs and, hence in high-impedance state.

POWER-UP SEQUENCE

After all supplies are established, serial communication with the AMC7891 is valid only after a 200 µs power-up reset delay. Following this, a software reset should be issued to ensure proper operation of the AMC7891. A software reset is issued by writing the value '0x6600' to *reset[15:0]* in register *AMC_reset*. Communication to the AMC7891 is re-established after a 200 µS delay from the reset operation (measured from the rising edge of $\overline{CS}$ establishing the end of the reset command frame).

At power-up or after a software-reset command all registers are set to the default values (see Table 6). The default state of all analog blocks is off as determined by the default value of the *AMC_power* register.

For the device to work properly, AV_{DD} must power up before applying any inputs to the GPIO pins. In addition, if using an external ADC reference AV_{DD} must power up before the external reference voltage is applied to the REF pin.

The following power-up sequence is recommended for the AMC7891.

1. No input should be applied to the GPIO pins. Also, if using an external ADC reference, it should not be applied to the REF pin.
2. Supply all voltages (AV_{DD}, $GPIOV_{DD}$ and $SPIV_{DD}$). If possible, it is recommended to apply IOV_{DD} before AV_{DD}. However, the supplies can be powered up simultaneously or in any order with no detrimental effect to the device.
3. After AV_{DD} has been applied there is a 200 µs power-up reset delay. No serial communication should be attempted during this time.
4. Issue a software-reset command by writing the value '0x6600' to *reset[15:0]* in register *AMC_reset*.
5. Wait at least 200 µs from the rising edge of $\overline{CS}$ to complete the software-reset.
6. Program the registers according to the desired mode of operation.

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APPLICATION INFORMATION

BASE STATION AMPLIFIER MONITOR AND CONTROL

The AMC7891 is a highly integrated, low-power, complete analog monitoring and control system in a small package; all of these features make the AMC7891's an ideal low-cost, bias control circuit for modern RF transistor modules such as the power amplifiers (PA) and low-noise amplifiers (LNA) found in RF communication systems.

The AMC7891 is used in RF amplifier signal chains to set the transistor's optimal bias condition as well as to monitor for any possible malfunction. The AMC7891 four independent DAC outputs allow control of the transistor's gate bias voltages as well as of any variable-gain amplifiers (VGAs) in the signal chain. The AMC7891 twelve configurable GPIOs enable digital signal control and monitoring. Additionally, the device has 8 uncommitted analog inputs driving a highly precise ADC and an accurate on-chip temperature sensor that allow continuous monitoring of the main factors determining optimal amplifier operation such as temperature, supply voltages as well as drain bias currents through external current shunt monitors. The use of external current shunt monitors gives the system designer the flexibility to choose the optimal number of current measurements for the amplifier topology as well as the accuracy, voltage range and gain setting according to the drain current level to be measured. The Texas Instruments' INA282 family, which includes the INA282, INA283, INA284, INA285 and INA286 devices, are highly-accurate, wide common-mode range current shunt monitors with gains going from 50V/V to 1000V/V.

The circuit in Figure 36 shows a typical multi-stage Doherty PA monitoring and control system using the AMC7891. The AMC7891 DAC outputs are used to set the bias gate voltage of each LDMOS transistor in the PA as well as to set the gain of the VGA driving the PA. The AMC7891 ADC inputs are used to monitor the most important parameters in the PA operation: supply voltages, drain bias currents as well as the TX and RX signal power. The GPIOs give additional system flexibility. In the system example below three GPIOs are used to address an external 8:1 multiplexer used for giving additional inputs to the AMC7891 ADC.

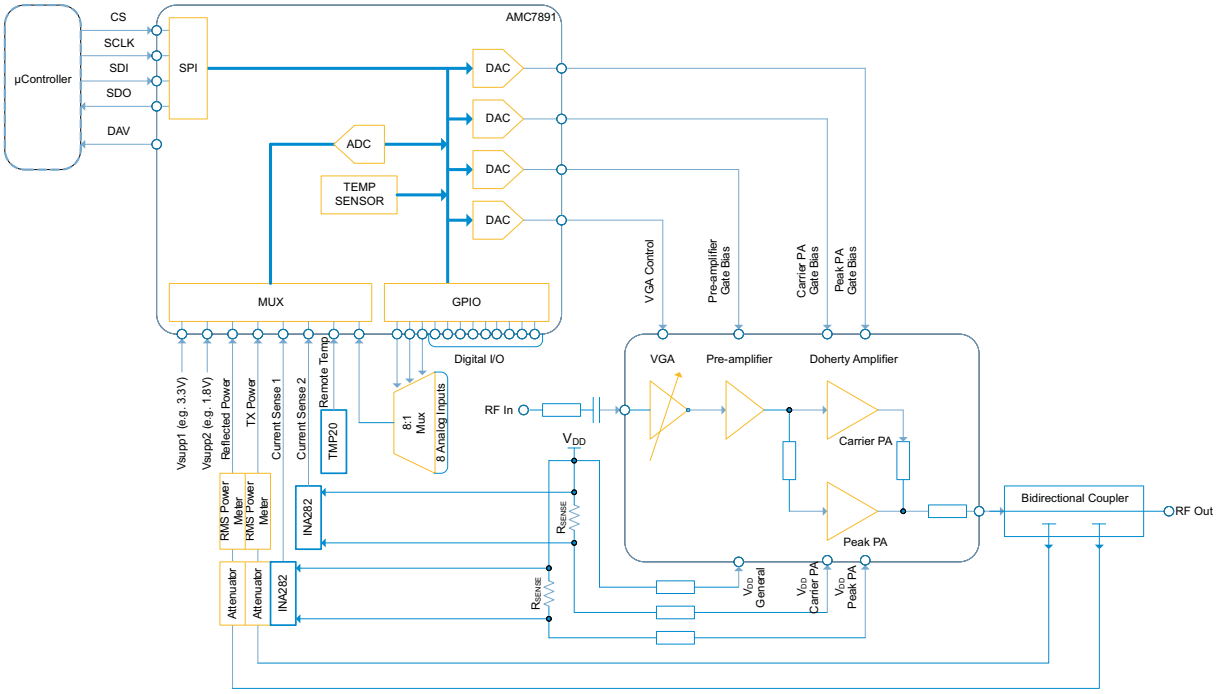


Figure 36. PA Monitor and Control System

REVISION HISTORY

Changes from Original (August 2011) to Revision A **Page**

- Changed from a 3 page Product Preview To a Prodcution Data Sheet 1
- Added the TYPICAL CHARACTERISTICS: DAC section 10
- Added the TYPICAL CHARACTERISTICS: ADC section 12

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AMC7891SRHHR	Active	Production	VQFN (RHH) | 36	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	AMC7891
AMC7891SRHHR.A	Active	Production	VQFN (RHH) | 36	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	AMC7891
AMC7891SRHHT	Active	Production	VQFN (RHH) | 36	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	AMC7891
AMC7891SRHHT.A	Active	Production	VQFN (RHH) | 36	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	AMC7891
AMC7891SRHHTG4	Active	Production	VQFN (RHH) | 36	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	AMC7891
AMC7891SRHHTG4.A	Active	Production	VQFN (RHH) | 36	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	AMC7891

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

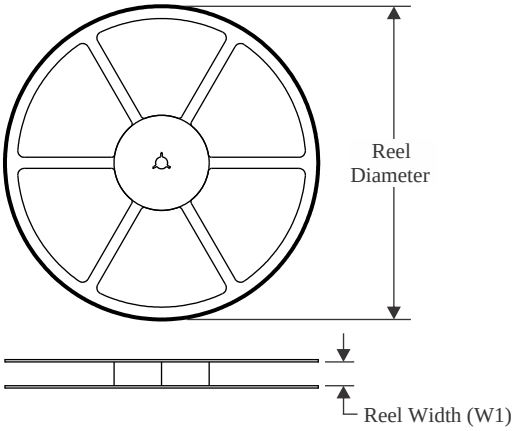
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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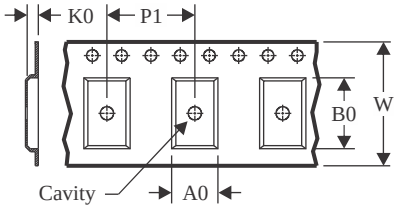
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

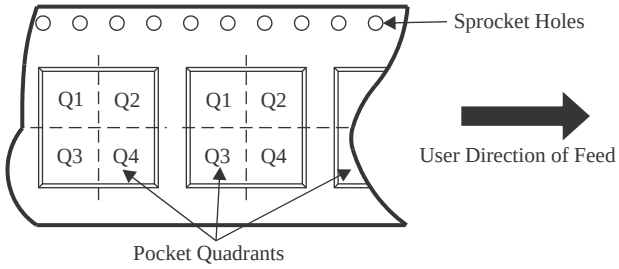


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

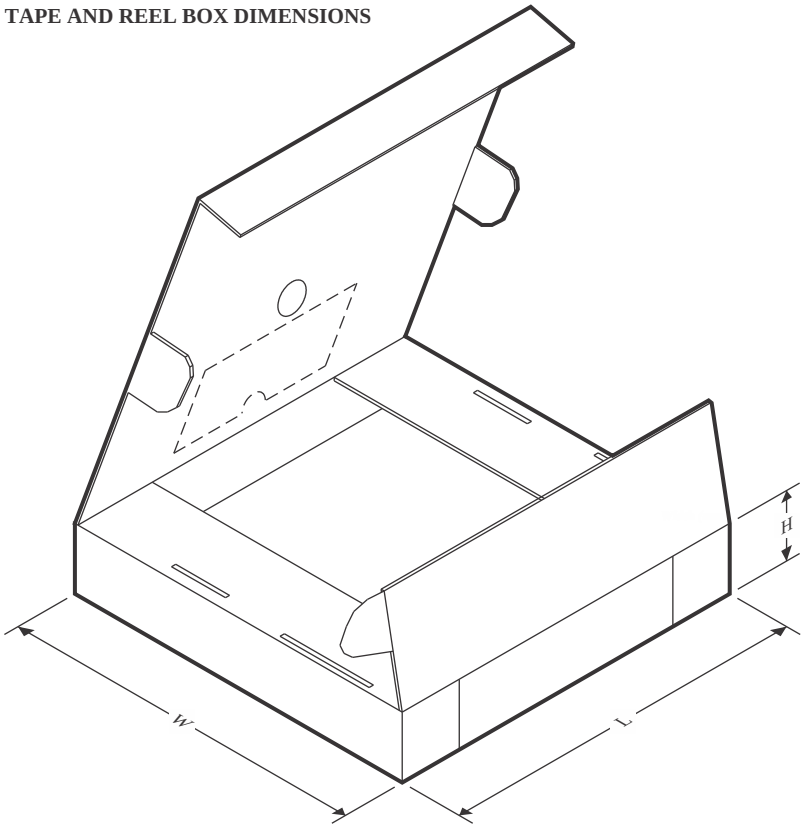
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC7891SRHHR	VQFN	RHH	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
AMC7891SRHHT	VQFN	RHH	36	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
AMC7891SRHHTG4	VQFN	RHH	36	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC7891SRHHR	VQFN	RHH	36	2500	367.0	367.0	38.0
AMC7891SRHHT	VQFN	RHH	36	250	210.0	185.0	35.0
AMC7891SRHHTG4	VQFN	RHH	36	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

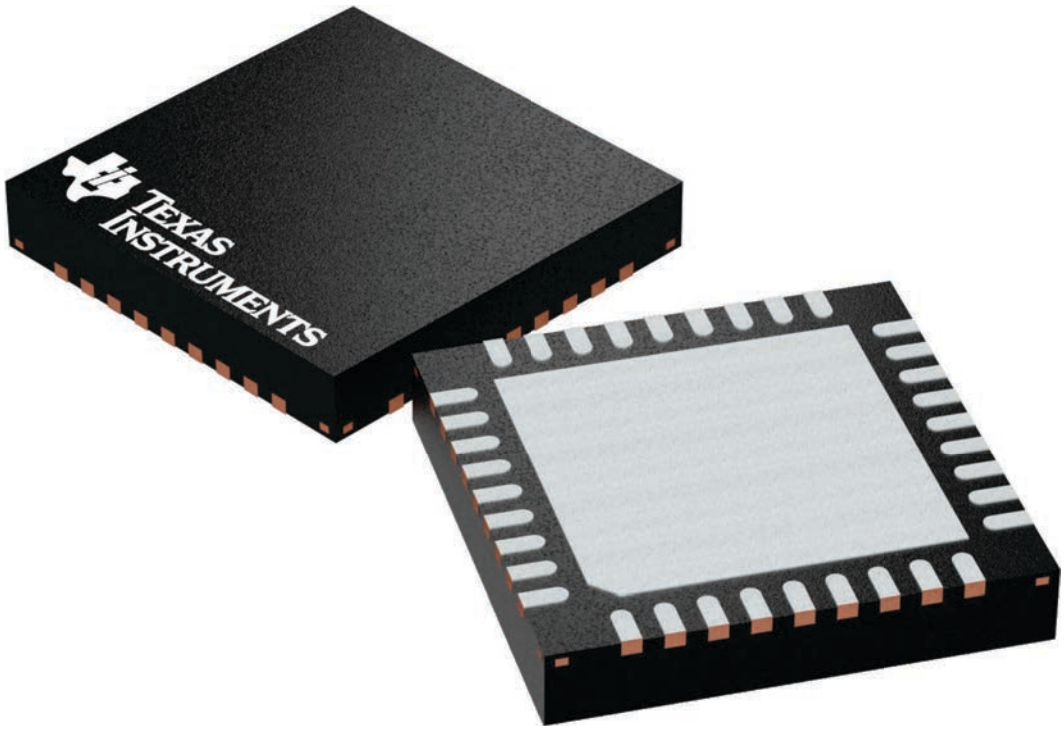
RHH 36

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



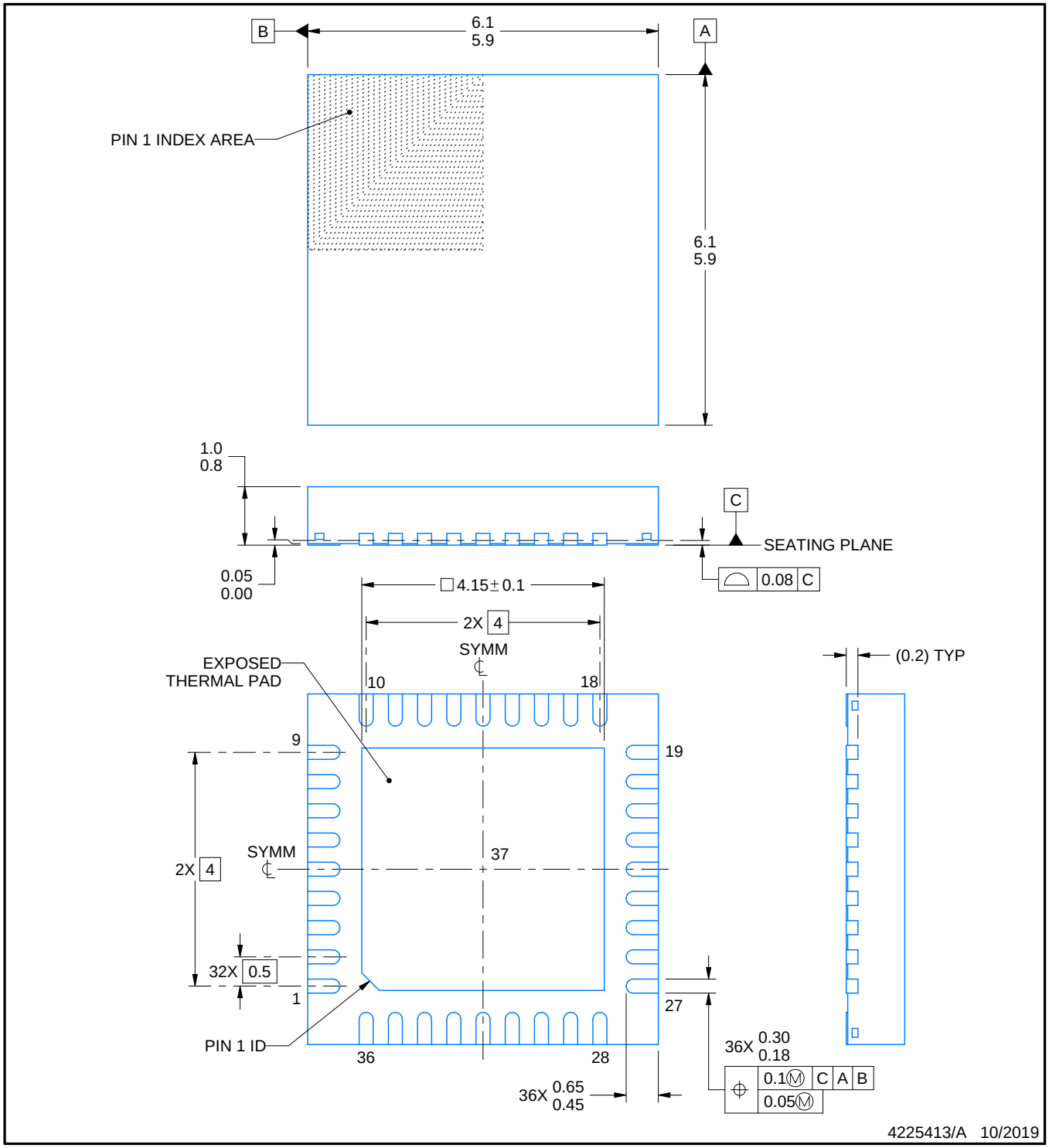
4225440/A

PACKAGE OUTLINE

RHH0036A

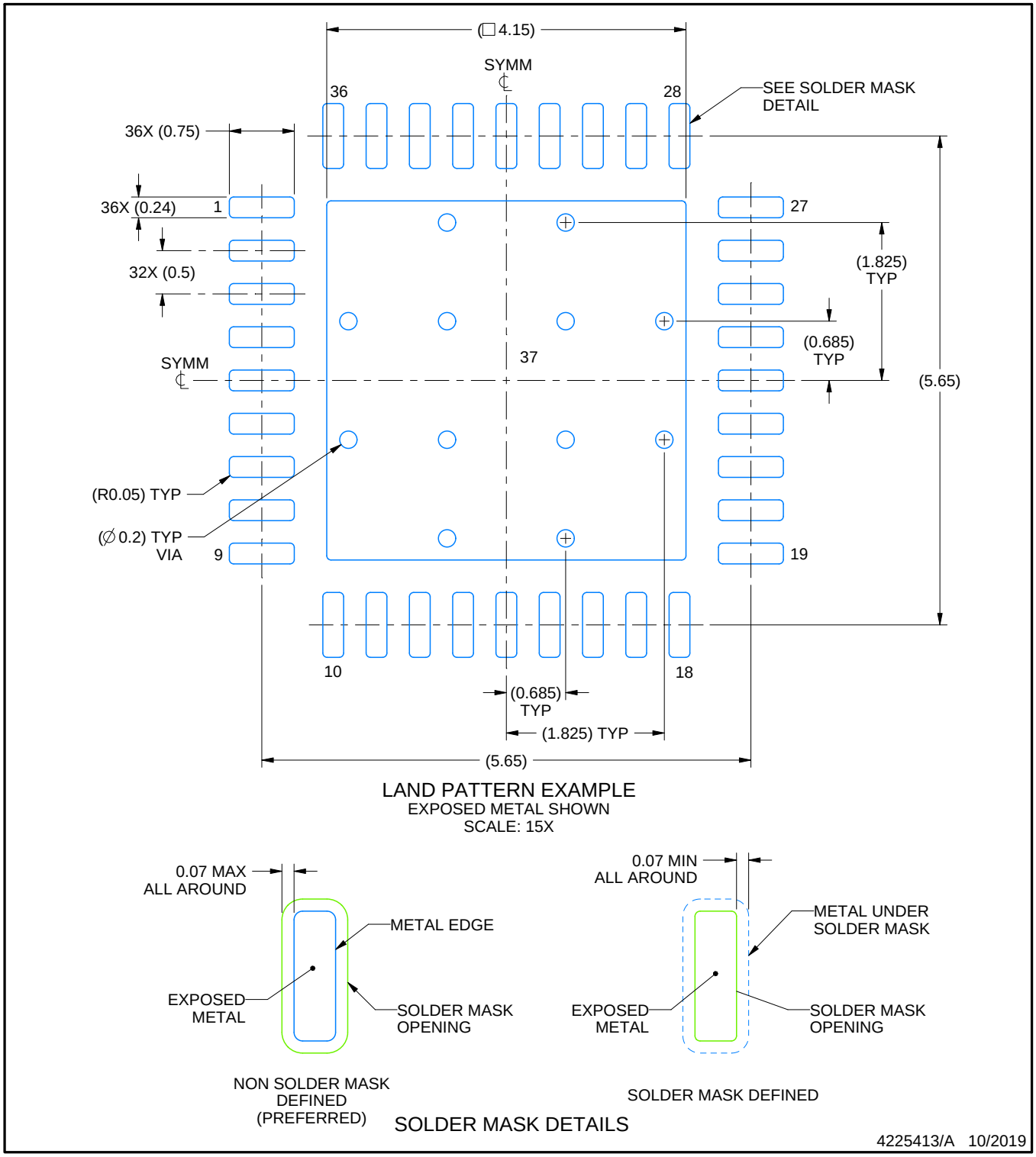
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



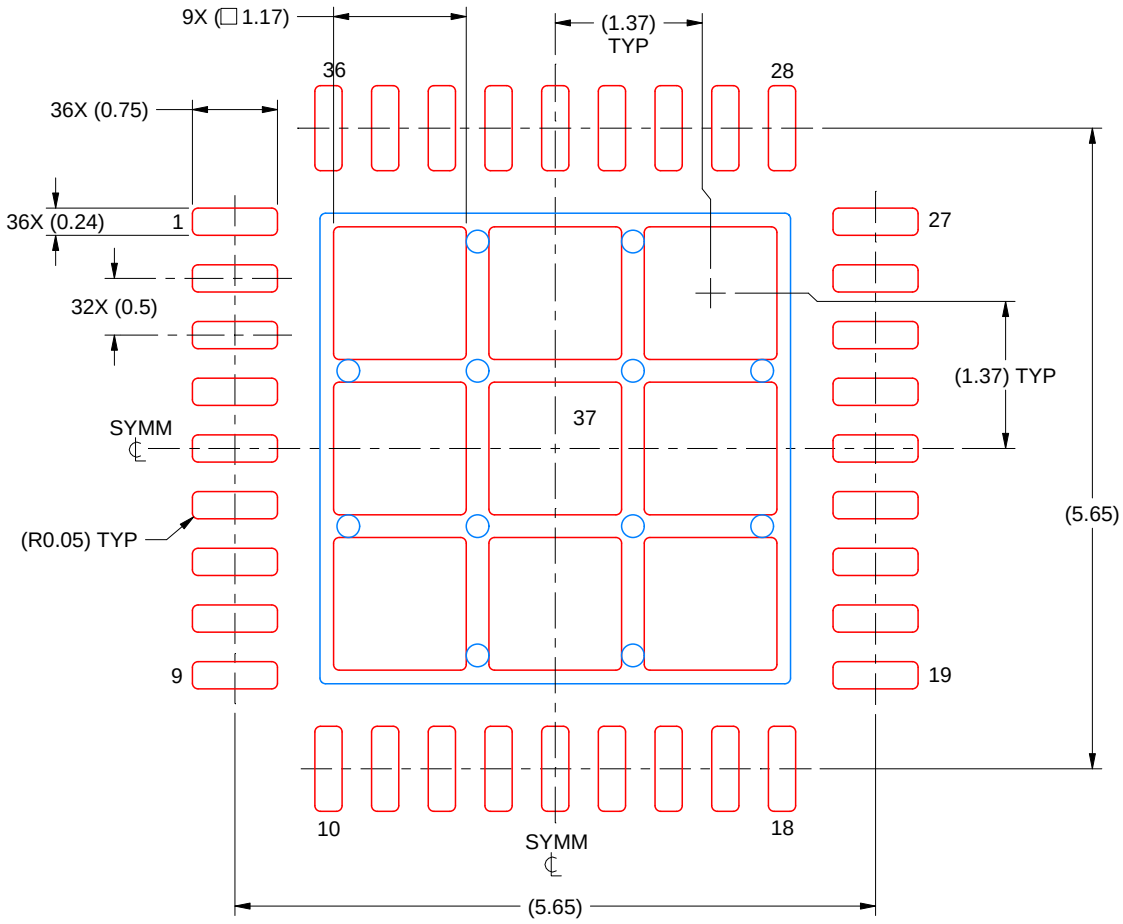
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 37
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225413/A 10/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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