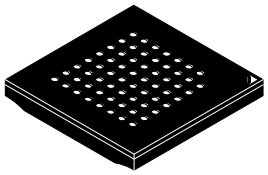
1/4-inch Color CMOS NTSC/PAL Digital Image SOC with Overlay Processor

ASX340AT



IBGA63 7.5 × 7.5
CASE 503AE

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

General Description

The **onsemi** ASX340AT is a VGA−format, single−chip CMOS active−pixel digital image sensor for automotive applications. It captures high−quality color images at VGA resolution and outputs NTSC or PAL interlaced composite video.

The VGA CMOS image sensor features **onsemi**'s breakthrough low−noise imaging technology that achieves superior image quality (based on signal−to−noise ratio and low−light sensitivity) while maintaining the inherent size, cost, low power, and integration advantages of **onsemi**'s advanced active pixel CMOS process technology.

The ASX340AT is a complete camera−on−a−chip. It incorporates sophisticated camera functions on−chip and is programmable through a simple two−wire serial interface or by an attached SPI EEPROM or Flash memory that contains setup information that may be loaded automatically at startup.

The ASX340AT performs sophisticated processing functions including color recovery, color correction, sharpening, programmable gamma correction, auto black reference clamping, auto exposure, 50Hz/60Hz flicker detection and avoidance, lens shading correction, auto white balance (AWB), and on−the−fly defect identification and correction.

The ASX340AT outputs interlaced−scan images at 60 or 50 fields per second, supporting both NTSC and PAL video formats. The image data can be output on one or two output ports:

- Composite analog video (single−ended and differential output support)
- Parallel 8−, 10−bit digital

Features

- Low−Power CMOS Image Sensor with Integrated Image Flow Processor (IFP) and Video Encoder
- 1/4−inch Optical Format, VGA Resolution (640 H x 480 V)
- 2x Upscaling Zoom and Pan Control
- ±40 Additional Columns and ±36 Additional Rows to Compensate for Lens Alignment Tolerances
- Option to Use Single 2.8 V Power Supply with Off−Chip Bypass Transistor
- Overlay Generator for Dynamic Bitmap Overlay
- Integrated Video Encoder for NTSC/PAL with Overlay Capability and 10−bit I−DAC
- Integrated Microcontroller for Flexibility
- On−Chip Image Flow Processor Performs Sophisticated Processing, Such as Color Recovery and Correction, Sharpening, Gamma, Lens Shading Correction, On−the−Fly Defect Correction, Auto White Balancing, and Auto Exposure
- Auto Black−Level Calibration
- 10−Bit, On−Chip Analog−to−Digital Converter (ADC)
- Internal Master Clock Generated by On−Chip Phase−Locked Loop (PLL)
- Two−Wire Serial Programming Interface
- Interface to Low−Cost EEPROM and Flash through SPI Bus
- High−Level Host Command Interface
- Stand−Alone Operation Support
- Comprehensive Tool Support for Overlay Generation and Lens Correction Setup
- Development System with DevWare

Applications

- Automotive Rear View Camera and Side Mirror
- Blind Spot and Surround View

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Table 1. KEY PARAMETERS

Parameter		Typical Value
Pixel Size and Type		5.6 μm x 5.6 μm active pinned−photodiode with high−sensitivity mode for low−light conditions
Sensor Clear Pixels		728 H x 560 V (includes VGA active pixels, demosaic and lens alignment pixels)
NTSC Output		720 H x 487 V
PAL Output		720 H x 576 V
Optical Area (Clear Pixels)		4.077 mm x 3.136 mm
Optical Format		$^1/_4$−inch
Frame Rate		50/60 fields/sec
Sensor Scan Mode		Progressive scan
Color Filter Array		RGB standard Bayer
Chief Ray Angle (CRA)		0°
Shutter Type		Electronic rolling shutter (ERS)
Automatic Functions		Exposure, white balance, black level offset correction, flicker detection and avoidance, color saturation control, on the−fly defect correction, aperture correction
Programmable Controls		Exposure, white balance, horizontal and vertical blanking, color, sharpness, gamma correction, lens shading correction, horizontal and vertical image flip, zoom, windowing, sampling rates, GPIO control
Overlay Support		Utilizes SPI interface to load overlay data from external flash/EEPROM memory with the following features: − Available in Analog output and BT656 Digital output − Overlay Size 360 x 480 pixel rendered into 720 x 480 (NTSC) or 720 x 576 (PAL) − Up to four (4) overlays may be blended simultaneously − Selectable readout: Rotating order user−selected − Dynamic scenes by loading pre−rendered frames from external memory − Palette of 32 colors out of 64 000 − 8 colors per bitmap − Blend factor dynamically−programmable for smooth transitions − Fast update rate of up to 30 fps − Every bitmap object has independent x/y position − Statistic Engine to calibrate optical alignment − Number Generator
Windowing		Programmable to any size
Analog Gain Range		0.5−16x
ADC		10−bit, on−chip
Output Interface		Analog composite video out, single−ended or differential; 8−, 10−bit parallel digital output
Output Data Formats1		Digital: Raw Bayer 8−,10−bit, CCIR656, 565RGB, 555RGB, 444RGB
Data Rate		Parallel: 27 MHz Pixel clock
		NTSC: 60 fields/sec
		PAL: 50 fields/sec
Control Interface		Two−wire I/F for register interface plus high−level command exchange. SPI port to interface to external memory to load overlay data, register settings, or firmware extensions.
Input Clock for PLL		27 MHz
SPI Clock Frequencies		1.6875 − 18 MHz, programmable
Supply Voltage		Analog: 2.8 V + 5%
		Core: 1.8 V + 5% (2.8 V + 5% power supply with off−chip bypass transistor generates a 1.70 − 1.95 V core voltage supply, which is acceptable for performance.)
Supply Voltage		IO: 2.8 V + 5%
Power Consumption	Analog Output Only	Full resolution at 60 fps: 291 mW
	Digital Output Only	Full resolution at 60 fps: 192 mW

Table 1. KEY PARAMETERS (continued)

Parameter		Typical Value
Package		63−BGA, 7.5 mm x 7.5 mm, 0.65 mm pin pitch
Ambient Temperature		Operating: −40°C to 105°C
		Functional: −40°C to + 85°C
		Storage: −50°C to + 150°C
Dark Current		< 200 e/s at 60°C with a gain of 1
Fixed Pattern Noise	Column	< 2 %
	Row	< 2 %
Responsivity		16.5 V/lux−s at 550 nm
Signal to Noise Ratio (S/N)		46 dB
Pixel Dynamic Range		87 dB

New Features

- Temperature sensor for dynamic feedback and sensor control
- Automatic 50 Hz/60 Hz flicker detection
- 2x upscaling zoom and pan/tilt control
- Independent control of colorburst parameters in the NTSC/PAL encoder
- Horizontal field of view adjustment between 700 and 720 pixels on the analog output
- Option to use single 2.8 V power supply with off−chip bypass transistor
- SPI EEPROM support for lower cost system design.

NOTE: Some of product capabilities (features and settings) outlined in this data sheet are not enabled by default. Customer requirements and relevant setting to be reviewed between customer and **onsemi** engineering to aligned on appropriate setting and customer specific performance and requirements.

ORDERING INFORMATION

Table 2. AVAILABLE PART NUMBERS

Part Number	Product Description	Orderable Product Attribute Description
ASX340AT2C00XPED0−DPBR	Rev2, Color, 0deg CRA, iBGA Package	Drypack, Protective Film, Anti−Reflective Glass
ASX340AT2C00XPED0−DRBR	Rev2, Color, 0deg CRA, iBGA Package	Drypack, Anti−Reflective Glass
ASX340AT2C00XPED0−TPBR	Rev2, Color, 0deg CRA, iBGA Package	Tape & Reel, Protective Film, Anti−Reflective Glass
ASX340AT2C00XPED0−TRBR	Rev2, Color, 0deg CRA, iBGA Package	Tape & Reel, Anti−Reflective Glass
ASX340AT2C00XPEDD3−GEVK	Rev2, Color, Demo Kit	
ASX340AT2C00XPEDH3−GEVB	Rev2, Color, Head Board	
ASX340AT3C00XPED0−DPBR	Rev3, Color, 0deg CRA, iBGA Package	Drypack, Protective Film, Anti−Reflective Glass
ASX340AT3C00XPED0−DRBR	Rev3, Color, 0deg CRA, iBGA Package	Drypack, Anti−Reflective Glass
ASX340AT3C00XPED0−TPBR	Rev3, Color, 0deg CRA, iBGA Package	Tape & Reel, Protective Film, Anti−Reflective Glass
ASX340AT3C00XPED0−TRBR	Rev3, Color, 0deg CRA, iBGA Package	Tape & Reel, Anti−Reflective Glass
ASX340AT3C00XPEDD3−GEVK	Rev 3, Color, Demo Kit	
ASX340AT3C00XPEDH3−GEVB	Rev 3, Color, Head Board	

See the **onsemi** Device Nomenclature document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

ARCHITECTURE

System Block Diagram

The system block diagram will depend on the application. The system block diagram in Figure 1 shows all components; optional peripheral components are highlighted. Control information will be received by a microcontroller through the automotive bus to communicate with the ASX340AT through its two−wire serial bus. Optional components will vary by application.

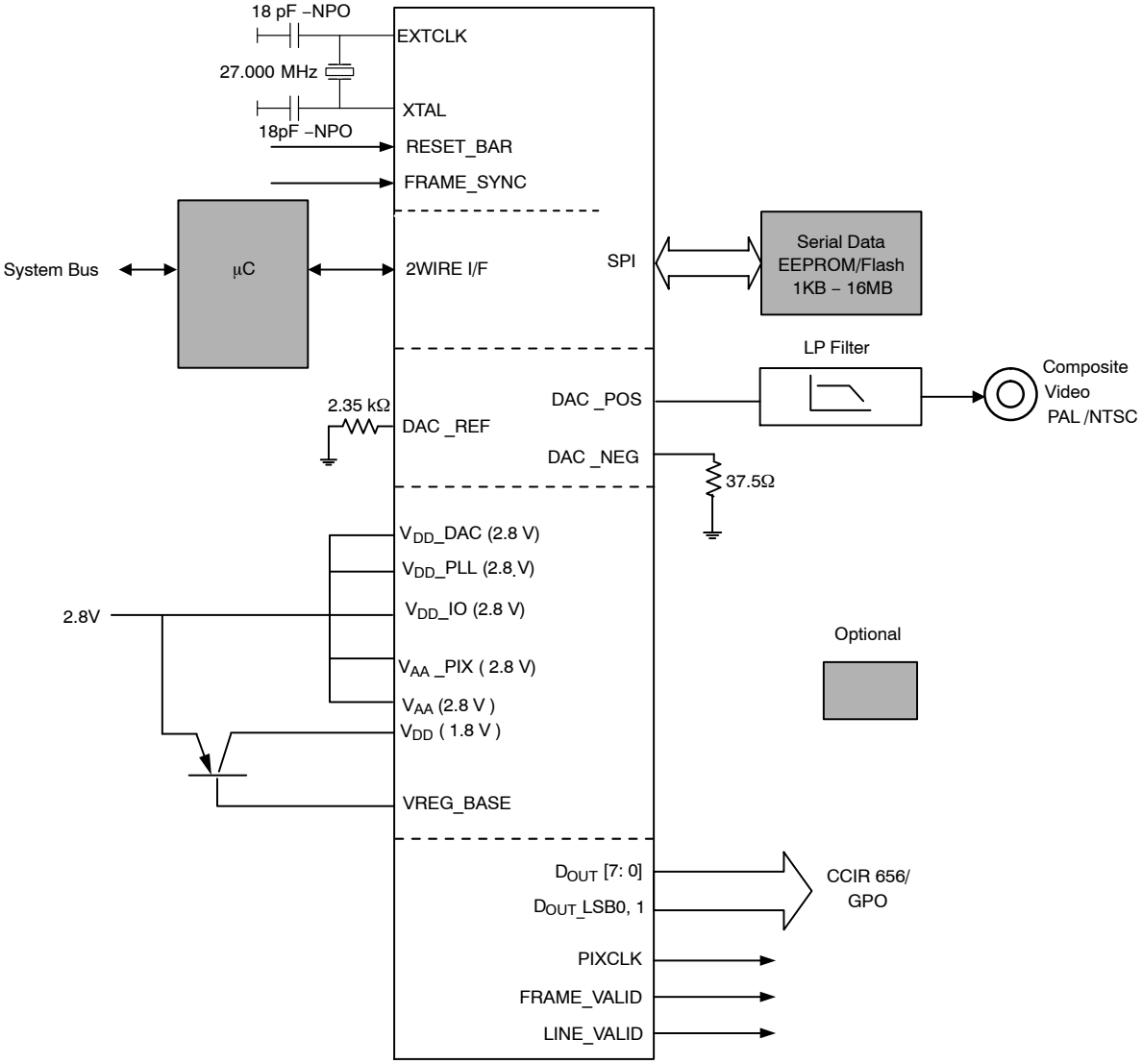


Figure 1. System Block Diagram

Internal Block Diagram

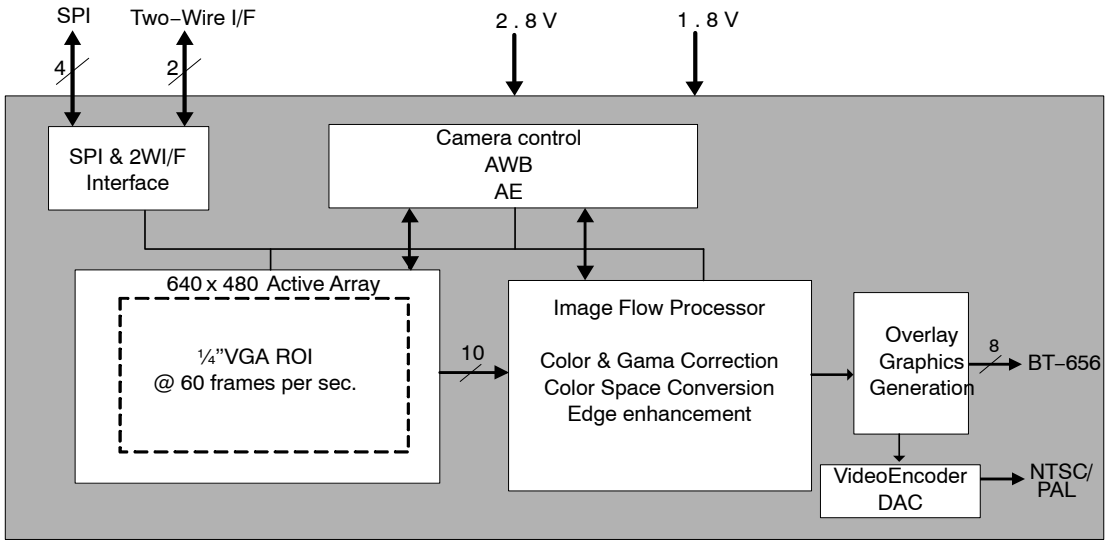
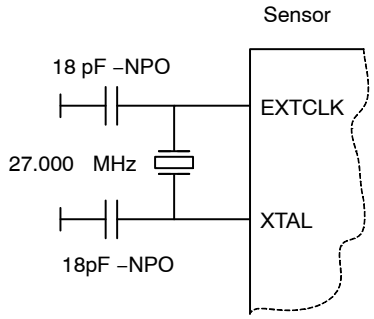


Figure 2. Internal Block Diagram

Crystal Usage

As an alternative to using an external oscillator, a fundamental 27 MHz crystal may be connected between EXTCLK and XTAL. Two small loading capacitors of 10–22 pF of NPO dielectric should be added as shown in Figure 3.

onsemi does not recommend using the crystal option for applications above 85°C. A crystal oscillator with temperature compensation is recommended.



NOTE: Value of load capacitor is crystal dependent. Crystal with small load capacitor is recommended.

Figure 3. Using a Crystal Instead of an External Oscillator

PIN DESCRIPTIONS AND ASSIGNMENTS

Table 3. PIN DESCRIPTION

Pin Number	Pin Name	Type	Description
CLOCK AND RESET			
A2	EXTCLK	Input	Master input clock (27 MHz): This can either be a square−wave generated from an oscillator (in which case the XTAL input must be left unconnected) or connected directly to a crystal
B1	XTAL	Output	If EXTCLK is connected to one pin of a crystal, this signal is connected to the other pin; otherwise this signal must be left unconnected
D2	RESET_BAR	Input	Asynchronous active−low reset: When asserted, the device will return all interfaces to their reset state. When released, the device will initiate the boot sequence. This signal has an internal pull−up resistor
E1	FRAME_SYNC	Input	This input can be used to set the output timing of the ASX340AT to a fixed point in the frame. The input buffer associated with this input is permanently enabled. This signal must be connected to GND if not used
REGISTER INTERFACE			
F1	SCLK	Input	These two signals implement the serial communications protocol for access to the internal registers and variables.
F2	SDATA	Input/Output	
E2	SADDR	Input	This signal controls the device ID that will respond to serial communication commands. Two−wire serial interface device ID selection: 0: 0x90 1: 0xBA
SPI INTERFACE			
D4	SPI_SCLK	Output	Clock output for interfacing to an external SPI memory such as Flash/EEPROM. Tri−state when RESET_BAR is asserted
E4	SPI_SDI	Input	Data in from SPI device. This signal has an internal pull−up resistor
H3	SPI_SDO	Output	Data out to SPI device. Tri−state when RESET_BAR is asserted
H2	SPI_CS_N	Output	Chip selects to SPI device. Tri−state when RESET_BAR is asserted
(PARALLEL) PIXEL DATA OUTPUT			
F7	FRAME_VALID	Input/Output	Pixel data from the ASX340AT can be routed out on this interface and processed externally. To save power, these signals are driven to a constant logic level unless the parallel pixel data output or alternate (GPIO) function is enabled for these pins. This interface is disabled by default. The slew rate of these outputs is programmable. These signals can also be used as general purpose input/outputs
G7	LINE_VALID	Input/Output	
E6	PIXCLK	Output	
F8, D6, D7, C6, C7, B6, B7, A6	DOUT[7:0]	Output	
B3	DOUT_LSB1	Input/Output	When the sensor core is running in bypass mode, it will generate 10 bits of output data per pixel. These two pins make the two LSB of pixel data available externally. Leave DOUT_LSB1and DOUT_LSB0 unconnected if not used. To save power, these signals are driven to a constant logic level unless the sensor core is running in bypass mode or the alternate function is enabled for these pins. The slew rate of these outputs is programmable
C2	DOUT_LSB0	Input/Output	
COMPOSITE VIDEO OUTPUT			
F5	DAC_POS	Output	Positive video DAC output in differential mode. Video DAC output in single−ended mode. This interface is enabled by default using NTSC/PAL signaling. For applications where composite video output is not required, the video DAC can be placed in a power−down state under software control
G5	DAC_NEG	Output	Negative video DAC output in differential mode
A4	DAC_REF	Output	External reference resistor for the video DAC
MANUFACTURING TEST INTERFACE			
D3	TDI	Input	JTAG Test pin (Reserved for Test Mode)
G2	TDO	Output	JTAG Test pin (Reserved for Test Mode)
F3	TMS	Input	JTAG Test pin (Reserved for Test Mode)

Table 3. PIN DESCRIPTION (continued)

Pin Number	Pin Name	Type	Description
MANUFACTURING TEST INTERFACE			
C3	TCK	Input	JTAG Test pin (Reserved for Test Mode)
C4	TRST_N	Input	Connect to GND
G6	ATEST1	Input	Analog test input. Connect to GND in normal operation
F6	ATEST2	Input	Analog test input. Connect to GND in normal operation
GPIO			
C1	GPIO12	Input/Output	Dedicated general−purpose input/output pin
A3	GPIO13	Input/Output	Dedicated general−purpose input/output pin
POWER			
G4	VREG_BASE	Supply	Voltage regulator control. Leave floating if not used
A5, A7, D8, E7, G1, G3	V_{DD}	Supply	Supply for V_{DD} core: 1.8 V nominal. Can be connected to the output of the transistor of the off−chip bypass transistor or an external 1.8 V power supply
B2, B8, C8, E3, E8, G8, H8	V_{DD}_IO	Supply	Supply for digital IOs: 2.8 V nominal
H5	V_{DD}_DAC	Supply	Supply for video DAC: 2.8 V nominal
A8	V_{DD}_PLL	Supply	Supply for PLL: 2.8 V nominal
B4, H6	V_{AA}	Supply	Analog power: 2.8 V nominal
H7	V_{AA}_PIX	Supply	Analog pixel array power: 2.8 V nominal. Must be at same voltage potential as V_{AA}
H4	Reserved		Leave floating for normal operation
B5, C5, D1, D5, H1	D_{GND}	Supply	Digital ground
E5, F4	A_{GND}	Supply	Analog ground

Pin Assignments

Pin 1 is not populated with a ball. That allows the device to be identified by an additional marking.

Table 4. PIN ASSIGNMENTS

	1	2	3	4	5	6	7	8
A		EXTCLK	GPIO13	DAC_REF	VDD	DOUT0	VDD	VDD_PLL
B	XTAL	VDD_IO	DOUT_LSB1	VAA	GND	DOUT2	DOUT1	VDD_IO
C	GPIO12	DOUT_LSB0	TCK	TRST_N	GND	DOUT4	DOUT3	VDD_IO
D	GND	RESET_BAR	TDI	SPI_SCLK	GND	DOUT6	DOUT5	VDD
E	FRAME_SYNC	SADDR	VDD_IO	SPI_SDI	AGND	PIXCLK	VDD	VDD_IO
F	SCLK	SDATA	TMS	AGND	DAC_POS	ATEST2	FRAME_VALID	DOUT7
G	VDD	TDO	VDD	VREG_BASE	DAC_NEG	ATEST1	LINE_VALID	VDD_IO
H	GND	SPI_CS_N	SPI_SDO	Reserved	VDD_DAC	VAA	VAA_PIX	VDD_IO

Table 5. RESET/DEFAULT STATE OF INTERFACES

Name	Reset State	Default State	Notes
EXTCLK	Clock running or stopped	Clock running	Input
XTAL	N/A	N/A	Input
RESET_BAR	Asserted	De−asserted	Input
SCLK	N/A	N/A	Input. Must always be driven to high via a pull−up resistor in the range of 1.5 to 4.7 kΩ
Sdata	High impedance	High impedance	Input/Output. Must always be driven to high via a pull−up resistor in the range of 1.5 to 4.7 kΩ
Saddr	N/A	N/A	Input. Must be permanently tied to Vdd_IO or GND
SPI_SCLK	High impedance	Driven, logic 0	Output. Output enable is R0x0032[13]
SPI_SDI	Internal pull−up enabled	Internal pull−up enabled	Input. Internal pull−up is permanently enabled
SPI_SDO	High impedance	Driven, logic 0	Output enable is R0x0032[13]
SPI_CS_N	High impedance	Driven, logic 1	Output enable is R0x0032[13]
FRAME_VALID	High impedance	High impedance	Input/Output. This interface is disabled by default. Input buffers (used for GPIO function) powered down by default, so these pins can be left unconnected (floating). After reset, these pins are powered up, sampled, then powered down again as part of the auto−configuration mechanism. See Note 2
LINE_VALID			
PIXCLK	High impedance	Driven, logic 0	Output. This interface disabled by default. See Note 1
Dout7			
Dout6			
Dout5			
Dout4			
Dout3			
Dout2			
Dout1			
Dout0			

Table 5. RESET/DEFAULT STATE OF INTERFACES (continued)

Name	Reset State	Default State	Notes
Dout_LSB1	High impedance	High impedance	Input/Output. This interface disabled by default. Input buffers (used for GPIO function) powered down by default, so these pins can be left unconnected (floating). After reset, these pins are powered−up, sampled, then powered down again as part of the auto−configuration mechanism
Dout_LSB0	High impedance	High impedance	
DAC_POS	High impedance	Driven	Output. Interface disabled by hardware reset and enabled by default when the device starts streaming
DAC_NEG			
DAC_REF			
TDI	Internal pull−up enabled	Internal pull−up enabled	Input. Internal pull−up means that this pin can be left unconnected (floating)
TDO	High impedance	High impedance	Output. Driven only during appropriate parts of the JTAG shifter sequence
TMS	Internal pull−up enabled	Internal pull−up enabled	Input. Internal pull−up means that this pin can be left unconnected (floating)
TCK	Internal pull−up enabled	Internal pull−up enabled	Input. Internal pull−up means that this pin can be left unconnected (floating)
TRST_N	N/A	N/A	Input. Must always be driven to a valid logic level. Must be driven to GND for normal operation
FRAME_SYNC	N/A	N/A	Input. Must always be driven to a valid logic level. Must be driven to GND if not used
GPIO12	High impedance	High impedance	Input/Output. This interface disabled by default. Input buffers (used for GPIO function) powered down by default, so these pins can be left unconnected (floating)
GPIO13	High impedance	High impedance	Input/Output. This interface disabled by default. Input buffers (used for GPIO function) powered down by default, so these pins can be left unconnected (floating)
ATEST1	N/A	N/A	Must be driven to GND for normal operation
ATEST2	N/A	N/A	Must be driven to GND for normal operation

1. The reason for defining the default state as logic 0 rather than high impedance is this: when wired in a system (for example, on **onsemi**'s demo boards), these outputs will be connected, and the inputs to which they are connected will want to see a valid logic level. No current drain should result from driving these to a valid logic level (unless there is a pull−up at the system level).
2. These pads have their input circuitry powered down, but they are not output−enabled. Therefore, they can be left floating but they will not drive a valid logic level to an attached device.

SOC DESCRIPTION

Detailed Architecture Overview

Sensor Core

The sensor consists of a pixel array, an analog readout chain, a 10−bit ADC with programmable gain and black offset, and timing and control as illustrated in Figure 4.

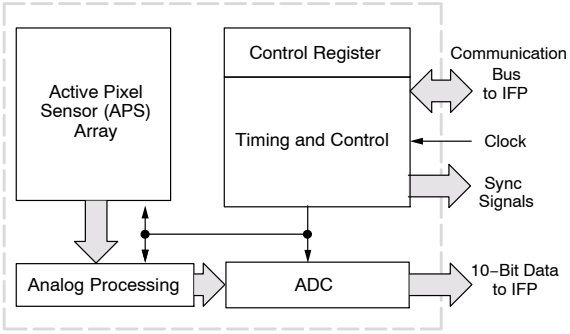


Figure 4. Sensor Core Block Diagram

Pixel Array Structure:

The sensor core pixel array is configured as 728 columns by 560 rows, as shown in Figure 5.

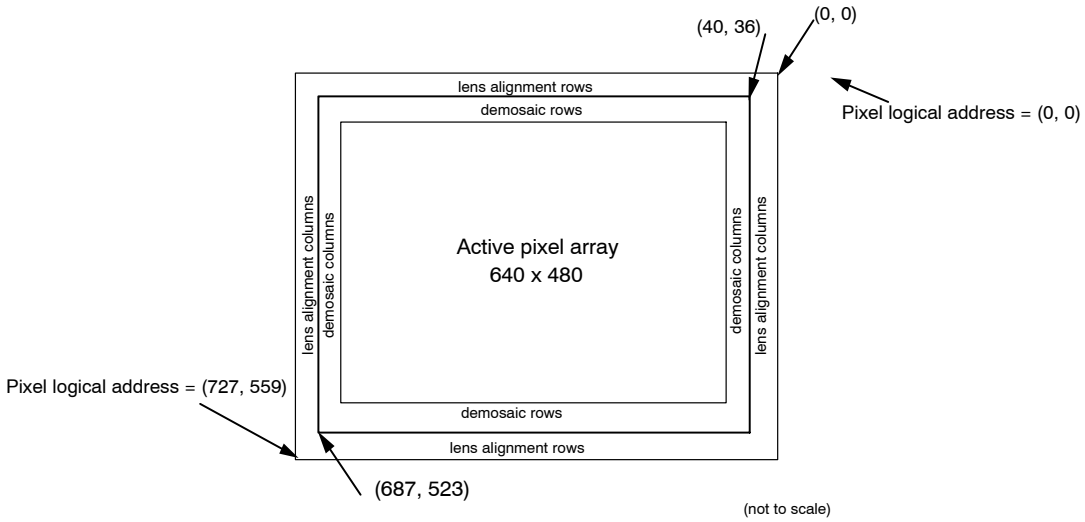


Figure 5. Pixel Array Description

Black rows used internally for automatic black level adjustment are not addressed by default, but can be read out in raw output mode via a register setting.

There are 728 columns by 560 rows of optically−active pixels (that is, clear pixels) that include a pixel boundary around the VGA (640 x 480) image to avoid boundary effects during color interpolation and correction. Among the 728 columns by 560 rows of clear pixels, there are 36 lens alignment rows on the top and bottom, and 40 lens alignment columns on the left and right; and there are 4 demosaic rows and 4 demosaic columns on each side.

Figure 6 illustrates the process of capturing the image. The original scene is flipped and mirrored by the sensor optics. Sensor readout starts at the lower right corner. The image is presented in true orientation by the output display.

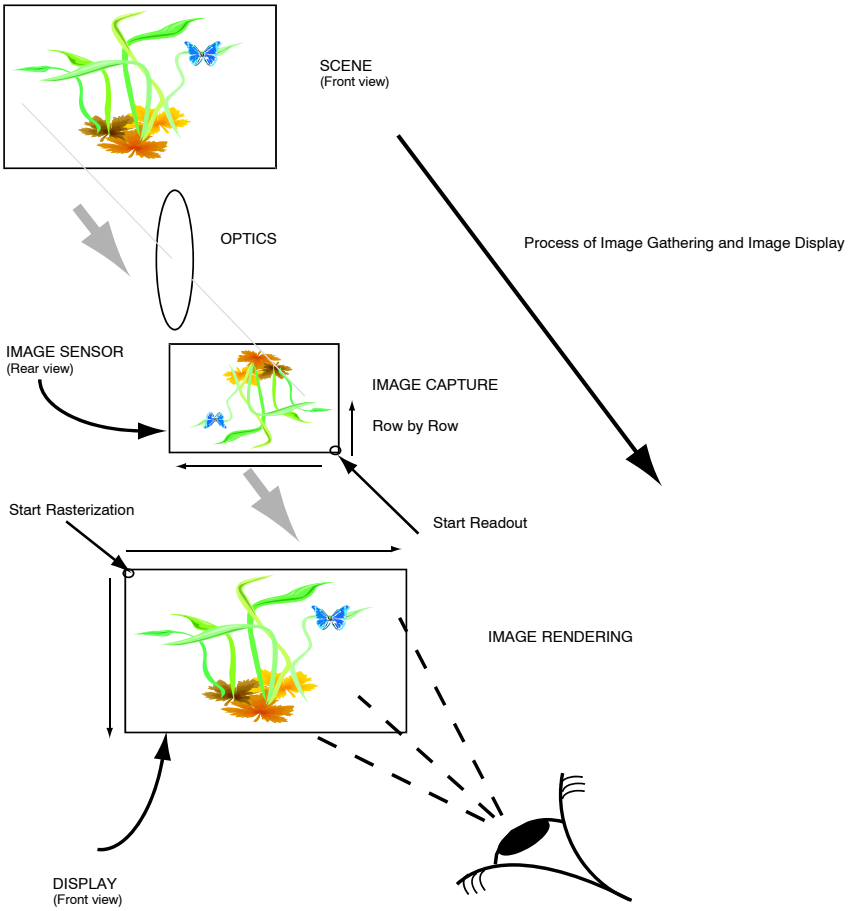


Figure 6. Image Capture Example

SENSOR PIXEL ARRAY

The active pixel array is 640 x 480 pixels. In addition, there are 72 rows and 80 columns for lens alignment and 8 rows and 8 columns for demosaic.

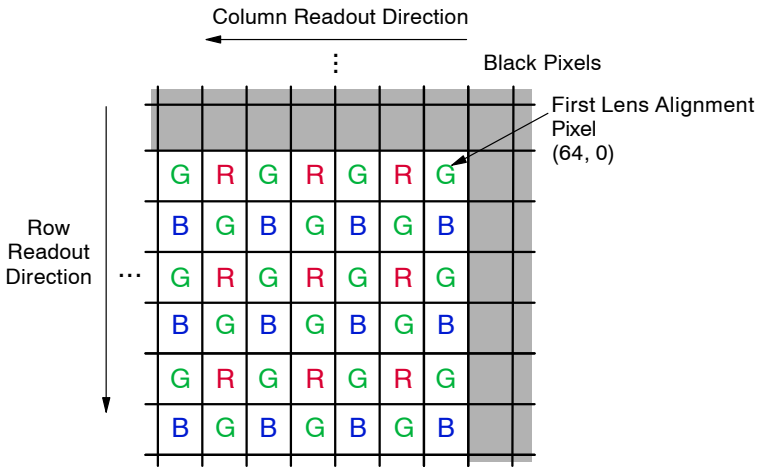


Figure 7. Pixel Color Pattern Detail (Top Right Corner)

Output Data Format:

The sensor core image data are read out in progressive scan order. Valid image data are surrounded by horizontal and vertical blanking, shown in Figure 8.

For NTSC output, the horizontal size is stretched from 640 to 720 pixels. The vertical size is 243 pixels per field; 240 image pixels and 3 dark pixels that are located at the bottom of the image field.

For PAL output, the horizontal size is also stretched from 640 to 720 pixels. The vertical size is 288 pixels per field.

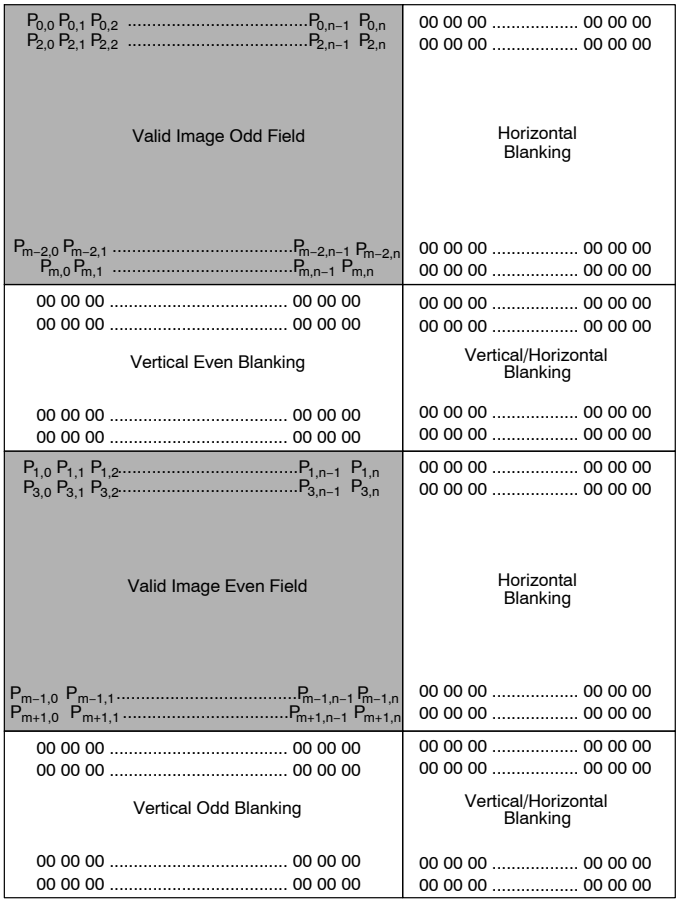


Figure 8. Spatial Illustration on Image Readout

Image Flow Processor

Image and color processing in the ASX340AT are implemented as an image flow processor (IFP) coded in hardware logic. During normal operation, the embedded microcontroller will automatically adjust the operation parameters. The IFP is broken down into different sections, as outlined in Figure 9.

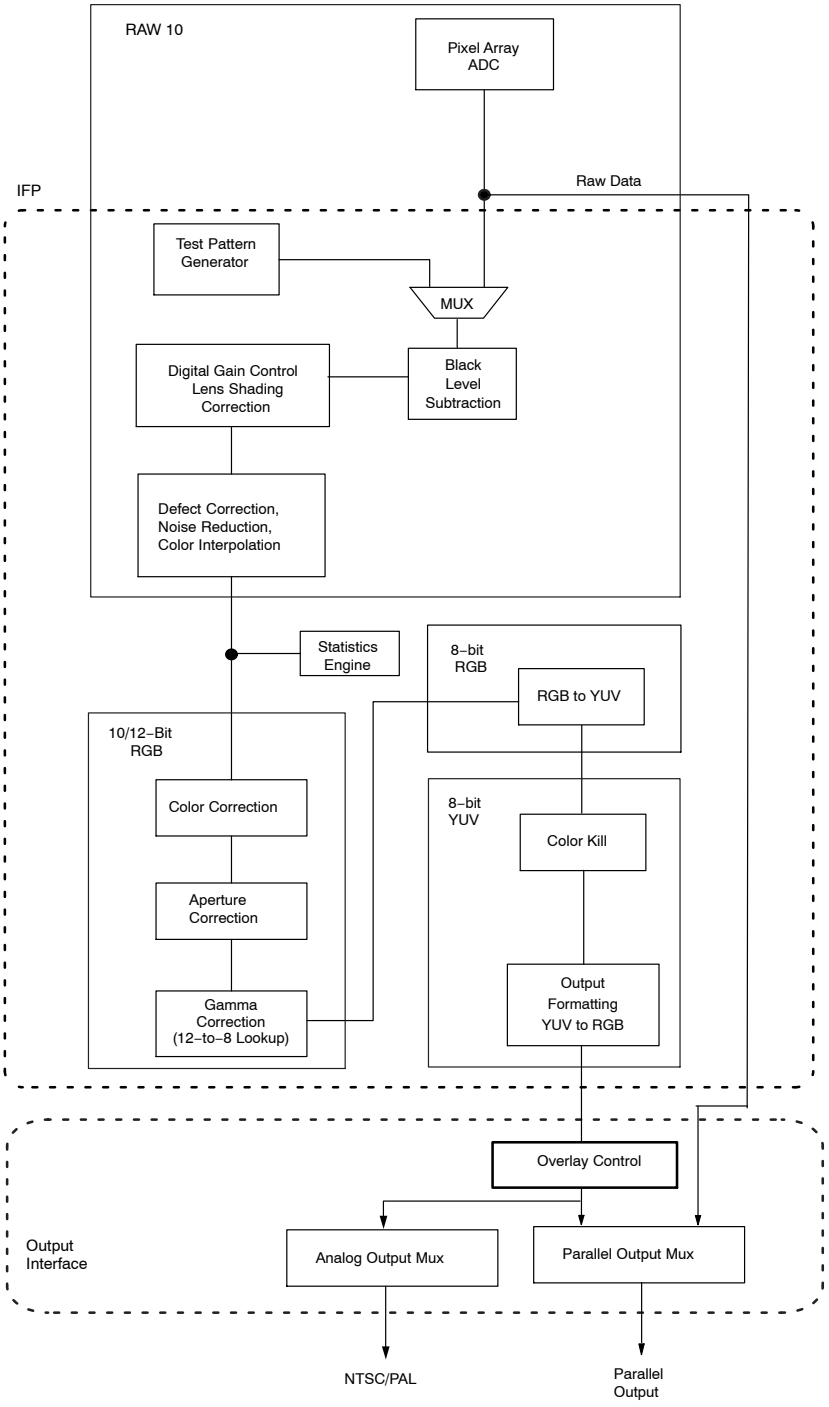


Figure 9. Color Pipeline

Test Patterns

During normal operation of the ASX340AT, a stream of raw image data from the sensor core is continuously fed into the color pipeline. For test purposes, this stream can be replaced with a fixed image generated by a special test module in the pipeline. The module provides a selection of test patterns sufficient for basic testing of the pipeline.

NTSC/PAL Test Pattern Generation

There is a built−in standard EIA (NTSC) and EBU (PAL) color bars to support hue and color saturation characterization. Each pattern consists of seven color bars (white, yellow, cyan, green, magenta, red, and blue). The Y, Cb and Cr values for each bar are detailed in Tables 6 and 7.

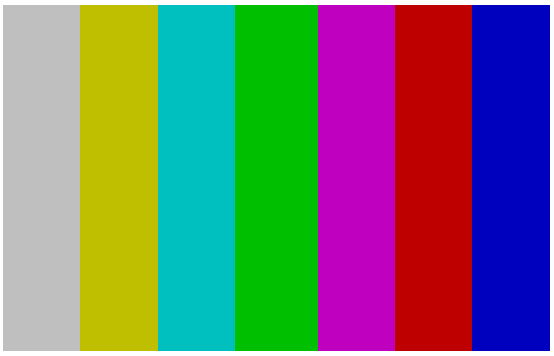


Figure 10. Color Bars

Table 6. EIA COLOR BARS (NTSC)

	Nominal Range	White	Yellow	Cyan	Green	Magenta	Red	Blue
Y	16 to 235	180	162	131	112	84	65	35
Cb	16 to 240	128	44	156	72	184	100	212
Cr	16 to 240	128	142	44	58	198	212	114

Table 7. EBU COLOR BARS (PAL)

	Nominal Range	White	Yellow	Cyan	Green	Magenta	Red	Blue
Y	16 to 235	235	162	131	112	84	65	35
Cb	16 to 240	128	44	156	72	184	100	212
Cr	16 to 240	128	142	44	58	198	212	114

CCIR−656 Format

The color bar data is encoded in 656 data streams. The duration of the blanking and active video periods of the generated 656 data are summarized in Tables 8 and 9.

Table 8. NTSC

Line Numbers	Field	Description
1−3	2	Blanking
4−19	1	Blanking
20−263	1	Active video
264−265	1	Blanking
266−282	2	Blanking
283−525	2	Active Video

Table 9. PAL

Line Numbers	Field	Description
1−22	1	Blanking
23−310	1	Active video
311−312	1	Blanking
313−335	2	Blanking
336−623	2	Active video
624−625	2	Blanking

Black Level Subtraction and Digital Gain

Image stream processing starts with black level subtraction and multiplication of all pixel values by a programmable digital gain. Both operations can be independently set to separate values for each color channel (R, Gr., Gb, B). Independent color channel digital gain can be adjusted with registers. Independent color channel black level adjustments can also be made. If the black level subtraction produces a negative result for a particular pixel, the value of this pixel is set to 0.

Positional Gain Adjustments (PGA)

Lenses tend to produce images whose brightness is significantly attenuated near the edges. There are also other factors causing fixed pattern signal gradients in images captured by image sensors. The cumulative result of all these factors is known as image shading. The ASX340AT has an embedded shading correction module that can be programmed to counter the shading effects on each individual R, Gb, Gr., and B color signal.

The Correction Function

The correction functions can then be applied to each pixel value to equalize the response across the image as follows:

$$P_{corrected}(row, col) = P_{sensor}(row, col) \times f(row, col) \quad \text{(eq. 1)}$$

where P is the pixel values and f is the color dependent correction functions for each color channel.

Color Interpolation

In the raw data stream fed by the sensor core to the IFP, each pixel is represented by a 10−bit integer number, which can be considered proportional to the pixel's response to a one−color light stimulus, red, green, or blue, depending on the pixel's position under the color filter array. Initial data processing steps, up to and including the defect correction, preserve the one−color−per−pixel nature of the data stream, but after the defect correction it must be converted to a three−colors−per−pixel stream appropriate for standard color processing. The conversion is done by an edge−sensitive color interpolation module. The module pads the incomplete color information available for each pixel with information extracted from an appropriate set of neighboring pixels. The algorithm used to select this set and extract the information seeks the best compromise between preserving edges and filtering out high frequency noise in flat field areas. The edge threshold can be set through register settings.

Color Correction and Aperture Correction

To achieve good color fidelity of the IFP output, interpolated RGB values of all pixels are subjected to color correction. The IFP multiplies each vector of three pixel colors by a 3 x 3 color correction matrix. The three components of the resulting color vector are all sums of three 10−bit numbers. Since such sums can have up to 12 significant bits, the bit width of the image data stream is widened to 12 bits per color (36 bits per pixel). The color correction matrix can be either programmed by the user or automatically selected by the auto white balance (AWB) algorithm implemented in the IFP. Color correction should ideally produce output colors that are corrected for the spectral sensitivity and color crosstalk characteristics of the image sensor. The optimal values of the color correction matrix elements depend on those sensor characteristics and on the spectrum of light incident on the sensor. The color correction parameters can be adjusted through register settings.

To increase image sharpness, a programmable 2D aperture correction (sharpening filter) is applied to color−corrected image data. The gain and threshold for 2D correction can be defined through register settings.

Gamma Correction

The ASX340AT includes a block for gamma correction that can adjust its shape based on brightness to enhance the performance under certain lighting conditions. Two custom gamma correction tables may be uploaded corresponding to a brighter lighting condition and a darker lighting condition. At power−up, the IFP loads the two tables with default values. The final gamma correction table used depends on the brightness of the scene and takes the form of an interpolated version of the two tables.

The gamma correction curve (as shown in Figure 11) is implemented as a piecewise linear function with 19 knee points, taking 12−bit arguments and mapping them to 8−bit output. The abscissas of the knee points are fixed at 0, 64, 128, 256, 512, 768, 1024, 1280, 1536, 1792, 2048, 2304, 2560, 2816, 3072, 3328, 3584, 3840, and 4096. The 8−bit ordinates are programmable through registers.

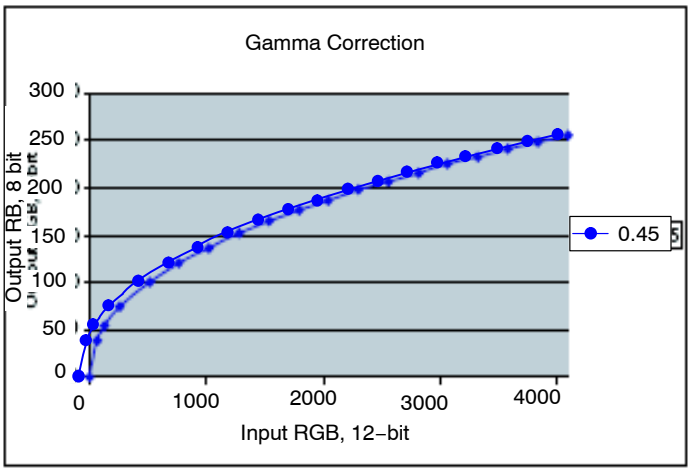


Figure 11. Gamma Correction Curve

RGB to YUV Conversion

For further processing, the data is converted from RGB color space to YUV color space.

Color Kill

To remove high−or low−light color artifacts, a color kill circuit is included. It affects only pixels whose luminance exceeds a certain preprogrammed threshold. The U and V values of those pixels are attenuated proportionally to the difference between their luminance and the threshold.

YUV Color Filter

As an optional processing step, noise suppression by one−dimensional low−pass filtering of Y and/or UV signals is possible. A 3− or 5−tap filter can be selected for each signal.

YUV−to−RGB/YUV Conversion and Output Formatting

The YUV data stream emerging from the colorpipe can either exit the color pipeline as−is or be converted before exit to an alternative YUV or RGB data format.

Output Format and Timing

YUV/RGB Data Ordering

The ASX340AT supports swapping YCbCr mode, as illustrated in Table 10.

Table 10. YCBCR OUTPUT DATA ORDERING

Mode	Data Sequence			
Default (no swap)	Cb_i	Y_i	Cr_i	Y_{i+1}
Swapped CbCr	Cr_i	Y_i	Cb_i	Y_{i+1}
Swapped YC	Y_i	Cb_i	Y_{i+1}	Cr_i
Swapped CbCr, YC	Y_i	Cr_i	Y_{i+1}	Cb_i

Table 11. RGB ORDERING IN DEFAULT MODE

Mode (Swap Disabled)	Byte	$D_7D_6D_5D_4D_3D_2D_1D_0$
565RGB	Odd	$R_7R_6R_5R_4R_3G_7G_6G_5$
	Even	$G_4G_3G_2B_7B_6B_5B_4B_3$
555RGB	Odd	0 $R_7R_6R_5R_4R_3G_7G_6$
	Even	$G_5G_4G_3B_7B_6B_5B_4B_3$
444 x RGB	Odd	$R_7R_6R_5R_4G_7G_6G_5G_4$
	Even	$B_7B_6B_5B_4$ 0 0 0 0
x444RGB	Odd	0 0 0 0 $R_7R_6R_5R_4$
	Even	$G_7G_6G_5G_4B_7B_6B_5B_4$

Uncompressed 10−Bit Bypass Output

Raw 10−bit Bayer data from the sensor core can be output in bypass mode in two ways:

- Using 8 data output signals (DOUT[7:0]) and GPIO[1:0]. The GPIO signals are the least significant 2 bits of data.
- Using only 8 signals (DOUT[7:0]) and a special 8 + 2 data format, shown in Table 12.

Table 12. 2−BYTE BAYER FORMAT

Byte	Bits Used	Bit Sequence
Odd bytes	8 data bits	$D_9D_8D_7D_6D_5D_4D_3D_2$
Even bytes	2 data bits + 6 unused bits	0 0 0 0 0 0 D_1D_0

Readout Formats

Progressive format is used for raw Bayer output.

Output Formats

ITU−R BT.656 and RGB Output:

TheASX340AT can output processed video as a standard ITU−R BT.656 (CCIR656) stream, an RGB stream, or as unprocessed Bayer data. The ITU−R BT.656 stream contains YCbCr 4:2:2 data with embedded synchronization codes. This output is typically suitable for subsequent display by standard video equipment or JPEG/MPEG compression.

Colorpipe data (pre−lens correction and overlay) can also be output in YCbCr 4:2:2 and a variety of RGB formats in 640 by 480 progressive format in conjunction with LINE_VALID and FRAME_VALID.

The ASX340AT can be configured to output 16−bit RGB (565RGB), 15−bit RGB (555RGB), and two types of 12−bit RGB (444RGB). Refer to Table 20 and Table 21 for details.

Bayer Output:

Unprocessed Bayer data are generated when bypassing the IFP completely−that is, by simply outputting the sensor Bayer stream as usual, using FRAME_VALID, LINE_VALID, and PIXCLK to time the data. This mode is called sensor bypass mode.

Output Ports

Composite Video Output:

The composite video output DAC is external−resistor−programmable and supports both single−ended and differential output. The DAC is driven by the on−chip video encoder output.

Parallel Output:

Parallel output uses either 8−bit or 10−bit output. Eight−bit output is used for ITU−R BT.656 and RGB output. Ten−bit output is used for raw Bayer output.

Zoom Support

The ASX340AT supports zoom x1 and x2 modes, in interlaced and progressive scan modes. The progressive support is limited to the VGA at either 60 fps or 50 fps.

In the zoom x2 modes, the sensor is configured for QVGA (320 x 240), and the zoom x2 window can be configured to pan around the VGA window.

FOV Stretch Support

The ASX340AT supports the ability to control the active “width” of the TV output line, between 692 and 720 pixels. The hardware supports two margins, each a maximum of 14 pixels width, and has to be an even number of pixels.

SYSTEM CONFIGURATION AND USAGE MODES

How a camera based on the ASX340AT will be configured depends on what features are used. There are essentially three configuration modes for ASX340AT: Auto−Config Mode, Flash−Config Mode, and Host−Config Mode. Refer to System Configuration and Usage.

MULTICAMERA SUPPORT

Two or more ASX340AT sensors may be synchronized to a frame by asserting the FRAME_SYNC signal. At that point, the sensor and video encoder will reset without affecting any register settings. The ASX340AT may be triggered to be synchronized with another ASX340AT or an external event.

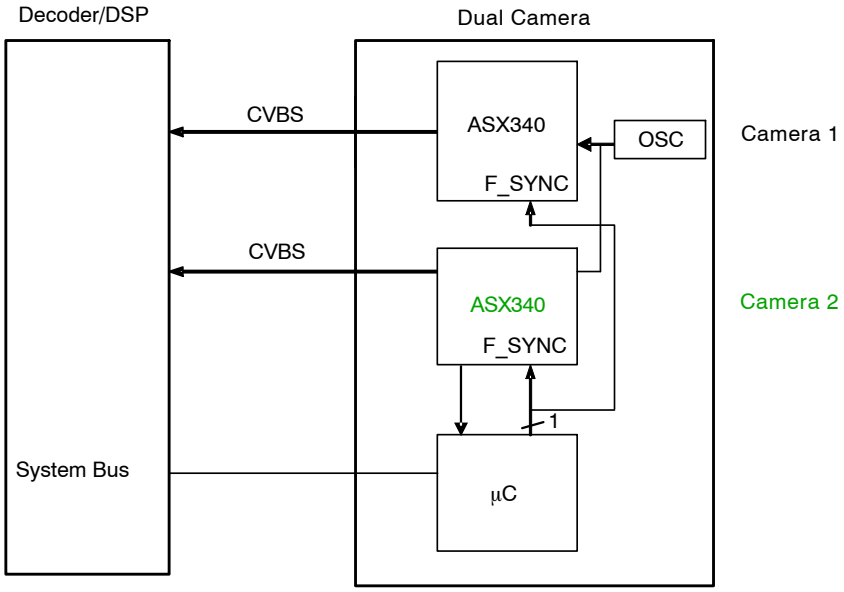


Figure 12. Multicamera System Block Diagram

EXTERNAL SIGNAL PROCESSING

An external signal processor can take data from ITU656 or raw Bayer output format and post−process or compress the data in various formats.

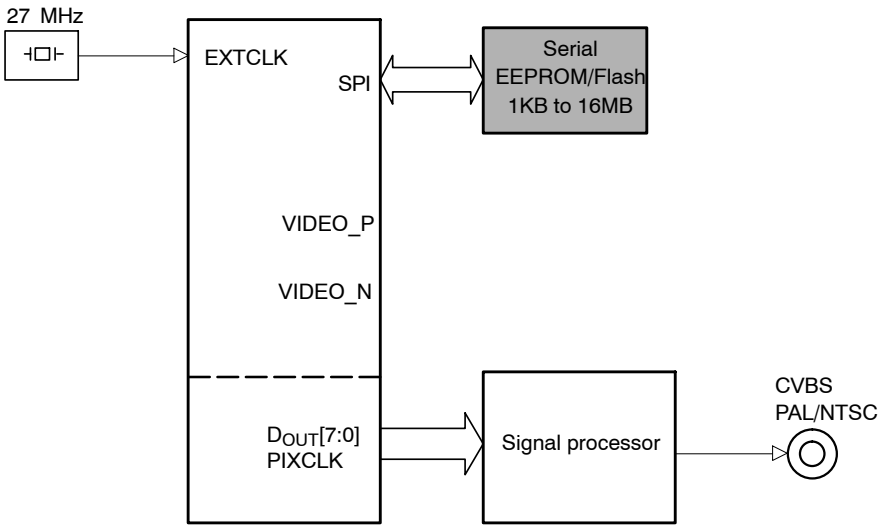


Figure 13. External Signal Processing Block Diagram

Device Configuration

After power is applied and the device is out of reset by de−asserting the RESET_BAR pin, it will enter a boot sequence to configure its operating mode. There are essentially three three configuration modes: Flash/EEPROM Config, Auto Config, and Host Config. Figure 14: “Power−Up Sequence – Configuration Options Flow Chart,” contains more details on the configuration options.

The SOC firmware supports a System Configuration phase at start−up. This consists of five modes of execution:

1. Flash Detection
2. Flash−Config
3. Auto−Config
4. Host−Config
5. Change−Config (commences streaming – completes the System Configuration mode)

The System Configuration phase is entered immediately after the firmware initializes following SOC power−up or reset. By default, the firmware first enters the Flash Detection mode.

The Flash Detection mode attempts to detect the presence of an SPI Flash or EEPROM device:

- If no device is detected, the firmware then samples the SPI_SDI pin state to determine the next mode:
  - If SPI_SDI = 0 then it enters the Host−Config mode
  - If SPI_SDI = 1 then it enters the Auto−Config mode
- If a device is detected, the firmware switches to the Flash−Config mode

In the Flash−Config phase, the firmware interrogates the device to determine if it contains valid configuration records:

- If no records are detected, then the firmware enters the Auto−Config mode
- If records are detected, the firmware processes them. By default, when all Flash records are processed the firmware switches to the Host−Config mode. However, the records encoded into the Flash can optionally be used to instruct the firmware to proceed to one of the other mode (auto−config/change−config)

The Auto−Config mode uses the FRAME_VALID, LINE_VALID, DOUT_LSB0 and DOUT_LSB1 pins to configure the operation of the device, such as video format and pedestal (refer to the Developer Guide for more details). After Auto−Config completes the firmware switches to the Change−Config mode.

In the Host−Config mode, the firmware performs no configuration, and remains idle waiting for configuration and commands from the host. The System Configuration phase is effectively complete and the SOC will take no actions until the host issues commands.

In the Change−Config mode, the firmware performs a “Change−Config” operation. This applies the current configuration settings to the SOC, and commences streaming. This completes the System Configuration phase.

Power Sequence

In power−up, refer to the power−up sequence in Figure 39: “Power Up Sequence.”

In power down, refer to Figure 40: “Power Down Sequence”, for details.

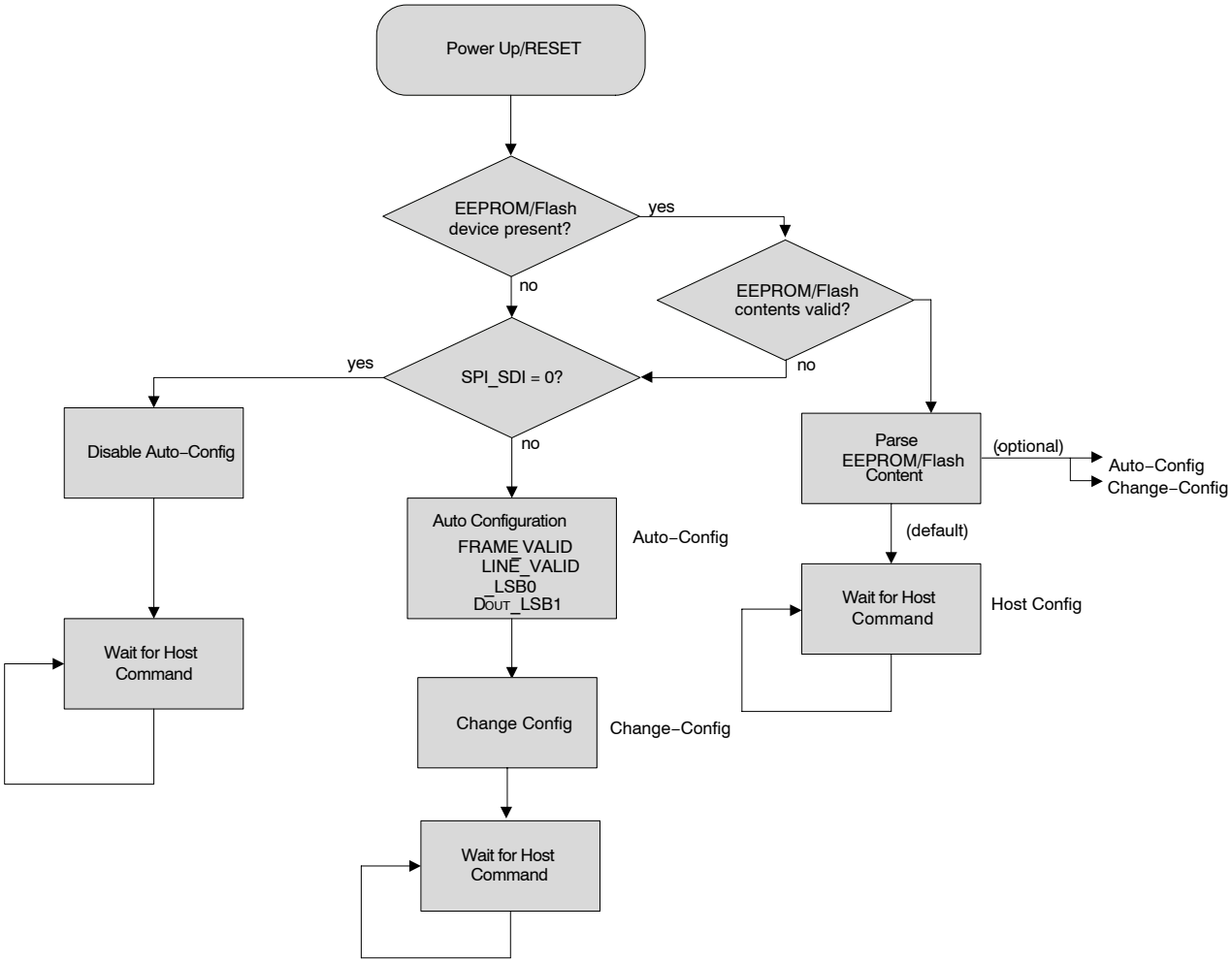


Figure 14. Power−Up Sequence – Configuration Options Flow Chart

Supported NVM Devices

The ASX340AT supports a variety of SPI non−volatile memory (NVM) devices. Refer to Flash/EEPROM Programming section in Developer Guide document for details.

Host Command Interface

onsemi sensors and SOCs contain numerous registers that are accessed through a two−wire interface with speeds up to 400 kHz.

The ASX340AT in addition to writing or reading straight to/from registers or firmware variables, has a mechanism to write higher level commands, the Host Command Interface (HCI). Once a command has been written through the HCI, it will be executed by on−chip firmware and the results are reported back. In general, registers should not be accessed with the exception of registers that are marked for “User Access.”

EEPROM or Flash memory is also available to store commands for later execution. Under DMA control, a command is written into the SOC and executed.

For a complete description of host commands, refer to the ASX340AT Host Command Interface Specification.

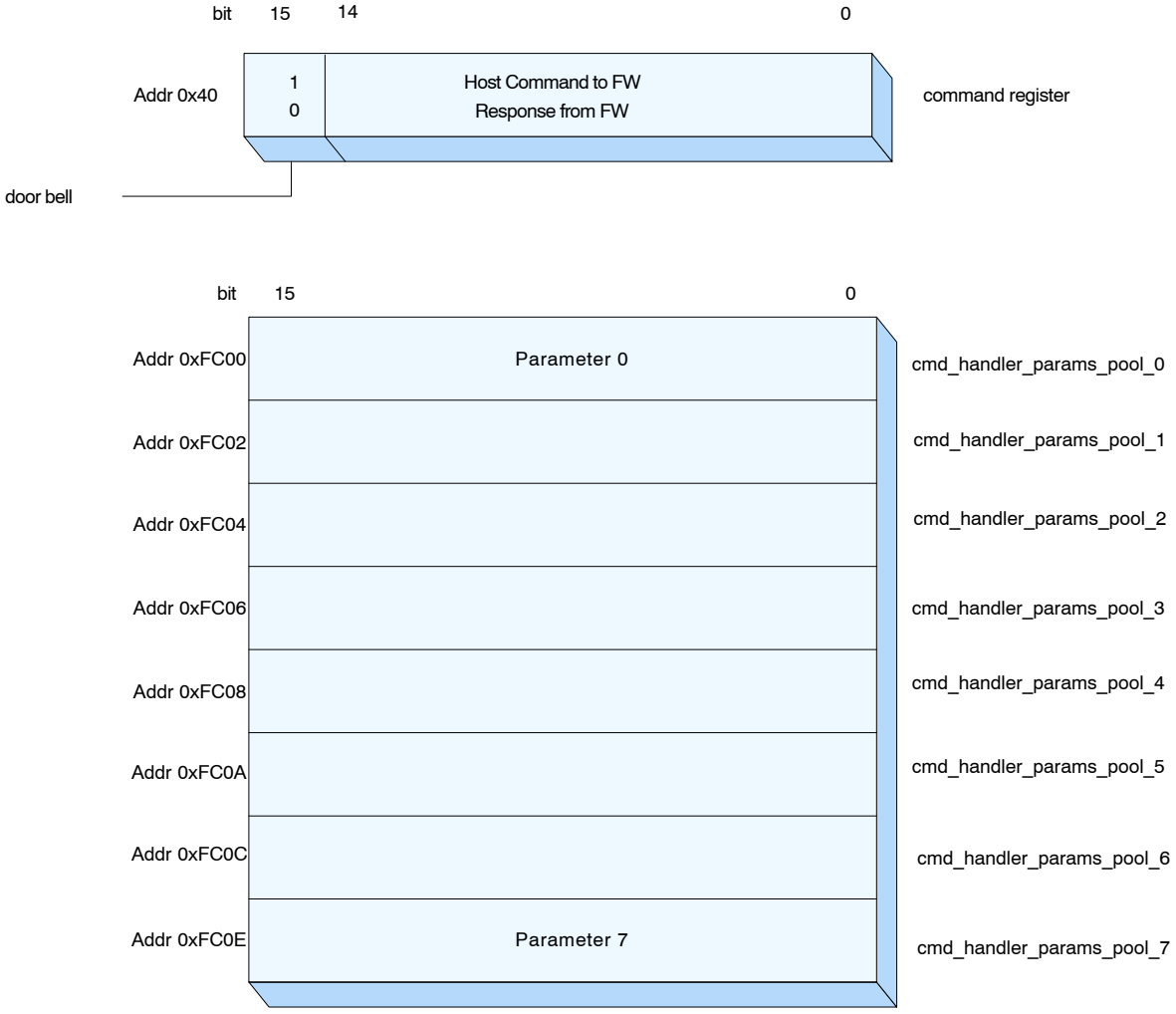


Figure 15. Interface Structure

Host Command Process Flow

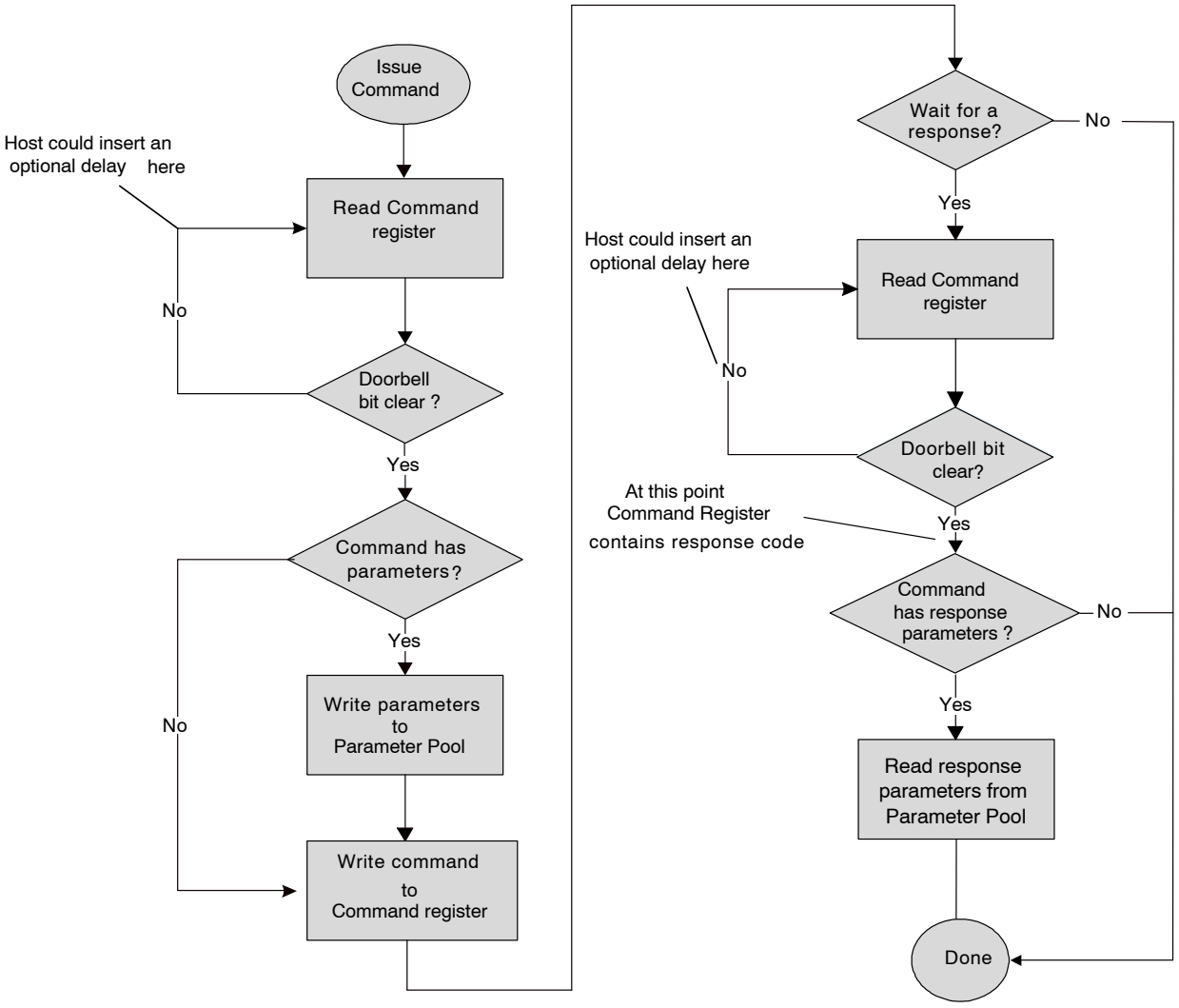


Figure 16. Host Command Process Flow

COMMAND FLOW

The host issues a command by writing (through a two−wire interface bus) to the command register. All commands are encoded with bit 15 set, which automatically generates the host command (doorbell) interrupt to the microprocessor.

Assuming initial conditions, the host first writes the command parameters (if any) to the parameters pool (in the command handler's logical page), then writes the command to command register. The firmware interrupt handler then signals the Command Handler task to process the command.

If the host wishes to determine the outcome of the command, it must poll the command register waiting for the doorbell bit to be cleared. This indicates that the firmware completed processing the command. When the doorbell bit is cleared, the contents of the command register indicate the command's result status. If the command generated response parameters, the host can now retrieve these from the parameters pool.

NOTE: The host must not write to the parameters pool, nor issue another command, until the previous command completes. This is true even if the host does not care about the result of the previous command. Therefore, the host must always poll the command register to determine the state of the doorbell bit, and ensure the bit is cleared before issuing a command.

For a complete command list and further information consult the Host Command Interface Specification.

An example of how (using DevWare) a command may be initiated in the form of a "Preset" follows.

Issue the SYSMGR_SET_STATE Command

All DevWare presets supplied by **onsemi** poll and test the doorbell bit after issuing the command. Therefore there is no need to check if the doorbell bit is clear before issuing the next command.

```
# Set the desired next state in the parameters pool(SYS_STATE_ENTER_CONFIG_CHANGE)
REG= 0xFC00, 0x2800 // CMD_HANDLER_PARAMS_POOL_0
# Issue the HC_SYSMGR_SET_STATE command
REG= 0x0040, 0x8100 // COMMAND_REGISTER
# Wait for the FW to complete the command (clear the Doorbell bit)
POLL_FIELD= COMMAND_REGISTER, DOORBELL,!=0, DELAY=10, TIMEOUT=100
# Check the command was successful
ERROR_IF= COMMAND_REGISTER, HOST_COMMAND,!=0, ”Set State command failed”,
```

Summary of Host Commands

Tables 13 through 18 show summaries of the host commands. The commands are divided into the following sections:

- System Manager
- Overlay
- GPIO
- Flash Manager
- Sequencer
- Patch Loader
- Miscellaneous
- Calibration Stats

Following is a summary of the Host Interface commands. The description gives a quick orientation. The “Type” column shows if it is an asynchronous or synchronous command. For a complete list of all commands including parameters, consult the Host Command Interface Specification document.

Table 13. SYSTEM MANAGER COMMANDS

System Manager Host Command	Value	Type	Description
Set State	0x8100	Synchronous	Request the system enter a new state
Get State	0x8101	Synchronous	Get the current state of the system

Table 14. OVERLAY HOST COMMANDS

Overlay Host Command	Value	Type	Description
Enable Overlay	0x8200	Synchronous	Enable or disable the overlay subsystem
Get Overlay State	0x8201	Synchronous	Retrieve the state of the overlay subsystem
Set Calibration	0x8202	Synchronous	Set the calibration offset
Set Bitmap Property	0x8203	Synchronous	Set a property of a bitmap
Get Bitmap Property	0x8204	Synchronous	Get a property of a bitmap
Set String Property	0x8205	Synchronous	Set a property of a character string
Load Buffer	0x8206	Asynchronous	Load an overlay buffer with a bitmap (from Flash)
Load Status	0x8207	Synchronous	Retrieve status of an active load buffer operation
Write Buffer	0x8208	Synchronous	Write directly to an overlay buffer
Read Buffer	0x8209	Synchronous	Read directly from an overlay buffer
Enable Layer	0x820A	Synchronous	Enable or disable an overlay layer
Get Layer Status	0x820B	Synchronous	Retrieve the status of an overlay layer
Set String	0x820C	Synchronous	Set the character string
Get String	0x820D	Synchronous	Get the current character string
Load String	0x820E	Asynchronous	Load a character string (from Flash)

Table 15. GPIO HOST COMMANDS

GPIO Host Command	Value	Type	Description
Set GPIO Property	0x8400	Synchronous	Set a property of one or more GPIO pins
Get GPIO Property	0x8401	Synchronous	Retrieve a property of a GPIO pin
Set GPO State	0x8402	Synchronous	Set the state of a GPO pin or pins
Get GPIO State	0x8403	Synchronous	Get the state of a GPI pin or pins
Set GPI Association	0x8404	Synchronous	Associate a GPI pin state with a Command Sequence stored in SPI Flash
Get GPI Association	0x8405	Synchronous	Retrieve an GPIO pin association

Table 16. FLASH MANAGER HOST COMMANDS

Flash Manager Host Command	Value	Type	Description
Get Lock	0x8500	Asynchronous	Request the Flash Manager access lock
Lock Status	0x8501	Synchronous	Retrieve the status of the access lock request
Release Lock	0x8502	Synchronous	Release the Flash Manager access lock
Config	0x8503	Synchronous	Configure the Flash Manager and underlying SPI Flash subsystem
Read	0x8504	Asynchronous	Read data from the SPI Flash
Write	0x8505	Asynchronous	Write data to the SPI Flash
Erase Block	0x8506	Asynchronous	Erase a block of data from the SPI Flash
Erase Device	0x8507	Asynchronous	Erase the SPI Flash device
Query Device	0x8508	Asynchronous	Query device−specific information
Status	0x8509	Synchronous	Obtain status of current asynchronous operation
Config Device	0x850A	Synchronous	Configure the attached SPI NVM device

Table 17. SEQUENCER HOST COMMANDS

Flash Manager Host Command	Value	Type	Description
Refresh	0x8606	Synchronous	Refresh the automatic image processing algorithm configuration
Refresh Status	0x8607	Synchronous	Retrieve the status of the last Refresh operation

Table 18. PATCH LOADER HOST COMMANDS

Patch Loader Host Command	Value	Type	Description
Load Patch	0x8700	Asynchronous	Load a patch from SPI Flash and automatically apply
Status	0x8701	Synchronous	Get status of an active Load Patch or Apply Patch request
Apply Patch	0x8702	Asynchronous	Apply a patch (already located in Patch RAM)
Reserve RAM	0x8706	Synchronous	Reserve RAM to contain a patch

Table 19. MISCELLANEOUS HOST COMMANDS

Miscellaneous Host Command	Value	Type	Description
Invoke Command Seq	0x8900	Synchronous	Invoke a sequence of commands stored in NVM
Config Command Seq Processor	0x8901	Synchronous	Configures the Command Sequencer processor
Wait For Event	0x8902	Synchronous	Wait for a system event to be signalled

Table 20. CALIBRATION STATS HOST COMMANDS

Calibration Stats Host Command	Value	Type	Description
Control	0x8B00	Asynchronous	Start statistics gathering
Read	0x8B01	Synchronous	Read the results back

SLAVE TWO−WIRE SERIAL INTERFACE

The two−wire serial interface bus enables read/write access to control and status registers within the ASX340AT. This interface is designed to be compatible with the MIPI Alliance Standard for Camera Serial Interface 2 (CSI−2) 1.0, which uses the electrical characteristics and transfer protocols of the two−wire serial interface specification.

The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (SCLK) that is an input to the sensor and used to synchronize transfers.

Data is transferred between the master and the slave on a bidirectional signal (SDATA). SDATA is pulled up to VDD_IO off−chip by a pull−up resistor in the range of 1.5 to 4.7 kΩ.

Protocol

Data transfers on the two−wire serial interface bus are performed by a sequence of low−level protocol elements, as follows:

- a start or restart condition
- a slave address/data direction byte
- a 16−bit register address
- an acknowledge or a no−acknowledge bit
- data bytes
- a stop condition

The bus is idle when both SCLK and SDATA are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

The SADDR pin is used to select between two different addresses in case of conflict with another device. If SADDR is LOW, the slave address is 0 x 90; if SADDR is HIGH, the slave address is 0 x BA. See Table 21.

Table 21. TWO−WIRE INTERFACE ID ADDRESS SWITCHING

SADDR	Two−Wire Interface Address ID
0	0x90
1	0xBA

Start Condition

A start condition is defined as a HIGH−to−LOW transition on SDATA while SCLK is HIGH. At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a “repeated start” or “restart” condition.

Data Transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no−acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes.

One data bit is transferred during each SCLK clock period. SDATA can change when SCLK is low and must be stable while SCLK is HIGH.

Slave Address/Data Direction Byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A “0” in bit [0] indicates a write, and a “1” indicates a read. The default slave addresses used by the ASX340AT are 0 x 90 (write address) and 0 x 91 (read address). Alternate slave addresses of 0 x BA (write address) and 0 x BB (read address) can be selected by asserting the SADDR input signal.

Message Byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data. The protocol used is outside the scope of the two−wire serial interface specification.

Acknowledge Bit

Each 8−bit data transfer is followed by an acknowledge bit or a no−acknowledge bit in the SCLK clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases SDATA. The receiver indicates an acknowledge bit by driving SDATA LOW. As for data transfers, SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

No−Acknowledge Bit

The no−acknowledge bit is generated when the receiver does not drive SDATA low during the SCLK clock period following a data transfer. A no−acknowledge bit is used to terminate a read sequence.

Stop Condition

A stop condition is defined as a LOW−to−HIGH transition on SDATA while SCLK is HIGH.

Typical Operation

A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8−bit slave address/data direction byte. The last bit indicates whether the request is for a READ or a WRITE, where a “0” indicates a WRITE and a “1” indicates a READ. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

If the request was a WRITE, the master then transfers the 16−bit register address to which a WRITE will take place. This transfer takes place as two 8−bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master will then transfer the 16−bit data, as two 8−bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master stops writing by generating a (re)start or stop condition. If the request was a READ, the master sends the 8−bit write slave address/data direction byte and 16−bit register address, just as in the write request. The master then generates a (re)start condition and the 8−bit read slave address/data direction byte, and clocks out the register data, 8 bits at a time. The master generates an acknowledge bit after each 8−bit transfer. The data transfer is stopped when the master sends a no−acknowledge bit.

Single READ from Random Location

Figure 17 shows the typical READ cycle of the host to the ASX340AT. The first two bytes sent by the host are an internal 16−bit register address. The following 2−byte READ cycle sends the contents of the registers to host.

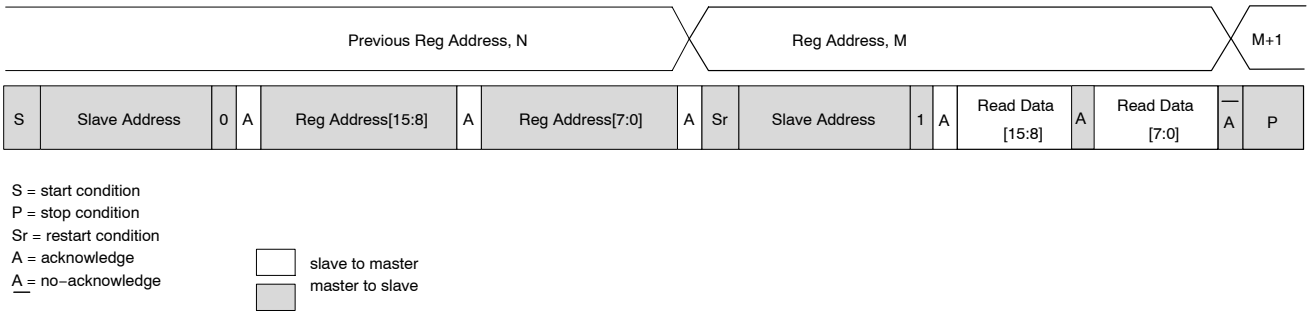


Figure 17. Single READ from Random Location

Single READ from Current Location

Figure 18 shows the single READ cycle without writing the address. The internal address will use the previous address value written to the register.

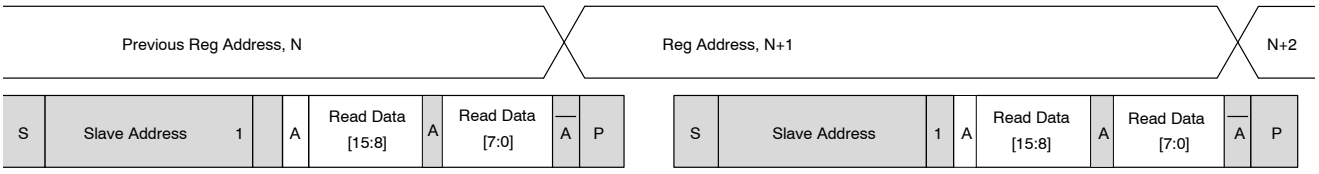


Figure 18. Single READ from Current Location

Sequential READ, Start from Random Location

This sequence (Figure 19) starts in the same way as the single READ from random location (Figure 17). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

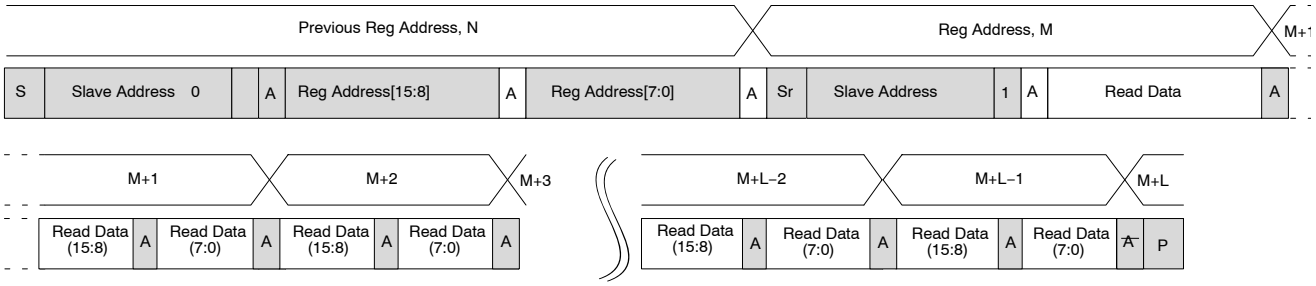


Figure 19. Sequential READ, Start from Random Location

Sequential READ, Start from Current Location

This sequence (Figure 20) starts in the same way as the single READ from current location (Figure 18). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte reads until “L” bytes have been read.

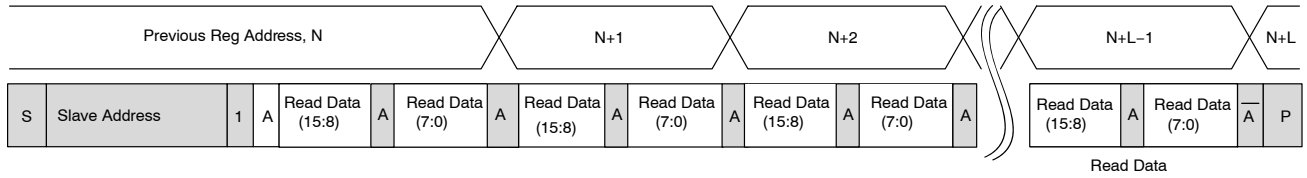


Figure 20. Sequential READ, Start from Current Location

Single Write to Random Location

Figure 21 shows the typical WRITE cycle from the host to the ASX340AT. The first 2 bytes indicate a 16−bit address of the internal registers with most−significant byte first. The following 2 bytes indicate the 16−bit data.

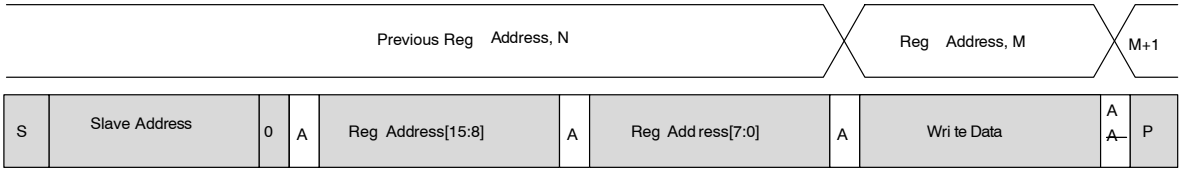


Figure 21. Single WRITE to Random Location

Sequential WRITE, Start at Random Location

This sequence (Figure 22) starts in the same way as the single WRITE to random location (Figure 21). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte writes until “L” bytes have been written. The WRITE is terminated by the master generating a stop condition.

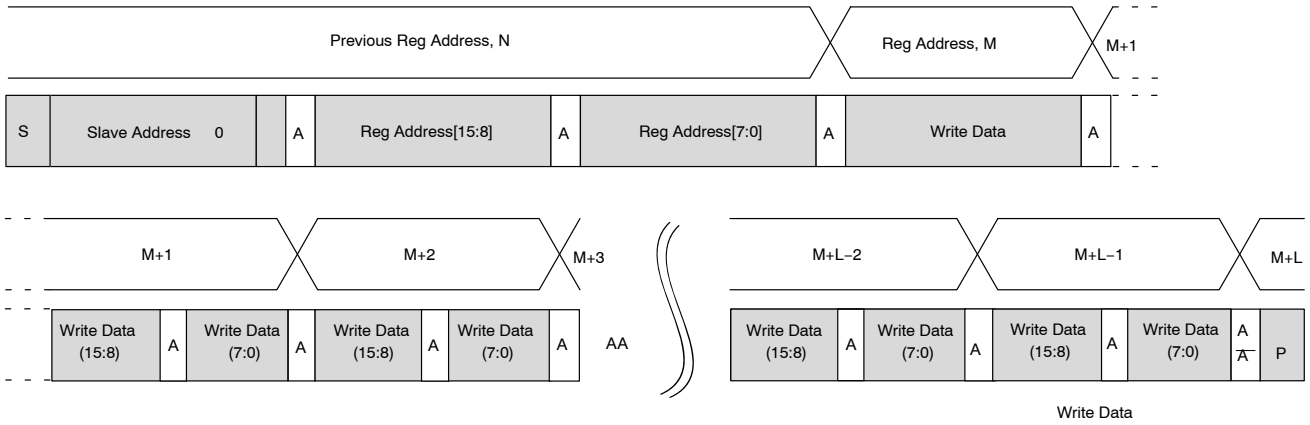


Figure 22. Sequential WRITE, Start at Random Location

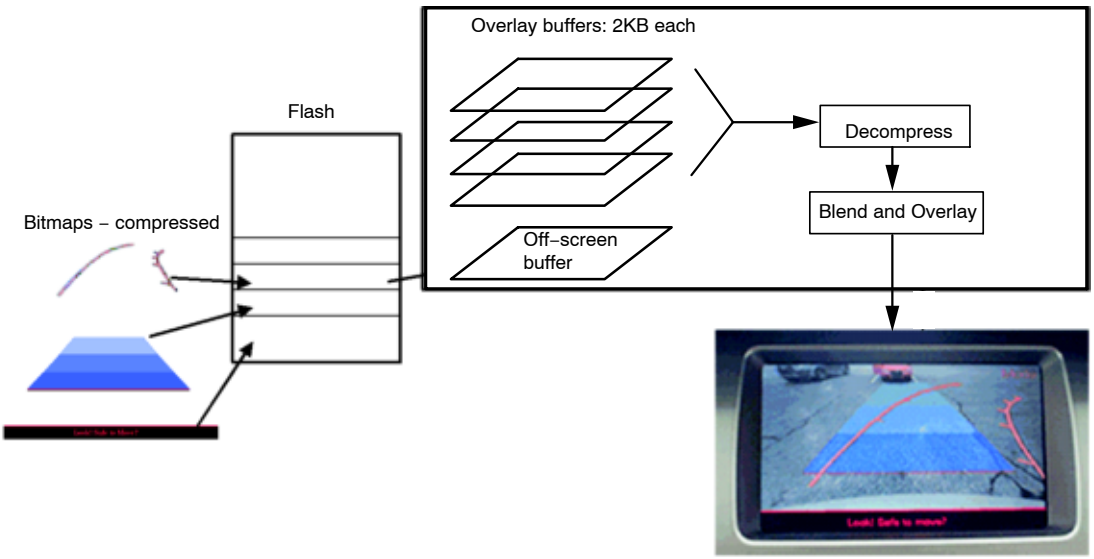
OVERLAY CAPABILITY

Figure 23 highlights the graphical overlay data flow of theASX340AT. The images are separated to fit into 2 KB blocks of memory after compression.

- Up to four overlays may be blended simultaneously
- Overlay size 360 x 480 pixels rendered into a display area of 720 x 480 pixels (NTSC) or 720 x 576 (PAL)
- Selectable readout: rotating order is user programmable
- Dynamic movement through predefined overlay images
- Palette of 32 colors out of 64,000 with eight colors per bitmap
- Blend factors may be changed dynamically to achieve smooth transitions

The host commands allow a bitmap to be written piecemeal to a memory buffer through the two−wire serial interface, and also through DMA direct from SPI Flash memory. Multiple encoding passes may be required to fit an image into a 2 KB block of memory; alternatively, the image can be divided into two or more blocks to make the image fit. Every graphic image may be positioned in the horizontal and vertical direction and overlap with other graphic images.

The host may load an image at any time. Under control of DMA assist, data are transferred to the off−screen buffer in compressed form. This assures that no display data are corrupted during the replenishment of the four active overlay buffers.



NOTE: These images are not actually rendered, but show conceptual objects and object blending.

Figure 23. Overlay Data Flow

NVM PARTITION

The contents of the Flash/EEPROM memory partition logically into three blocks (see Figure 24):

- Memory for overlay data and descriptors
- Memory for register settings, which may be loaded at boot−up
- Firmware extensions or software patches; in addition to the on−chip firmware, extensions reside in this block of memory

These blocks are not necessarily contiguous.

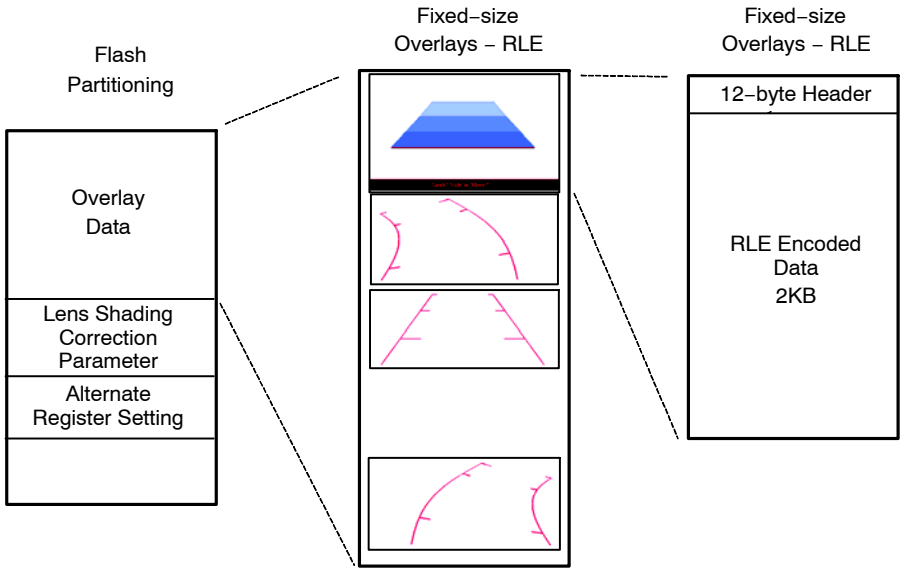


Figure 24. Memory Partitioning

External Memory Speed Requirement

For a 2 kb block of overlay to be transferred within a frame time to achieve maximum update rate, the SPI NVM must operate at a certain minimum speed.

Table 22. TRANSFER TIME ESTIMATE

Value	Type	Description
33.3 ms	4.5 MHz	1 ms

OVERLAY ADJUSTMENT

To ensure a correct position of the overlay to compensate for assembly deviation, the overlay can be adjusted with assistance from the overlay statistics engine:

- The overlay statistics engine supports a windowed 8−bin luma histogram, either row−wise (vertical) or column−wise (horizontal)
- The calibration statistics can be used to perform an automatic successive−approximation search of a cross−hair target within the scene
- On the first frame, the firmware performs a coarse horizontal search, followed by a coarse vertical search in the second frame
- In subsequent frames, the firmware reduces the region−of−interest of the search to the histogram bins containing the greatest accumulator values, thereby refining the search
- The resultant row and column location of the cross−hair target can be used to assign a calibration value to offset selected overlay graphic image positions within the output image
- The calibration statistics patch also supports a manual mode, which allows the host to access the raw accumulator values directly

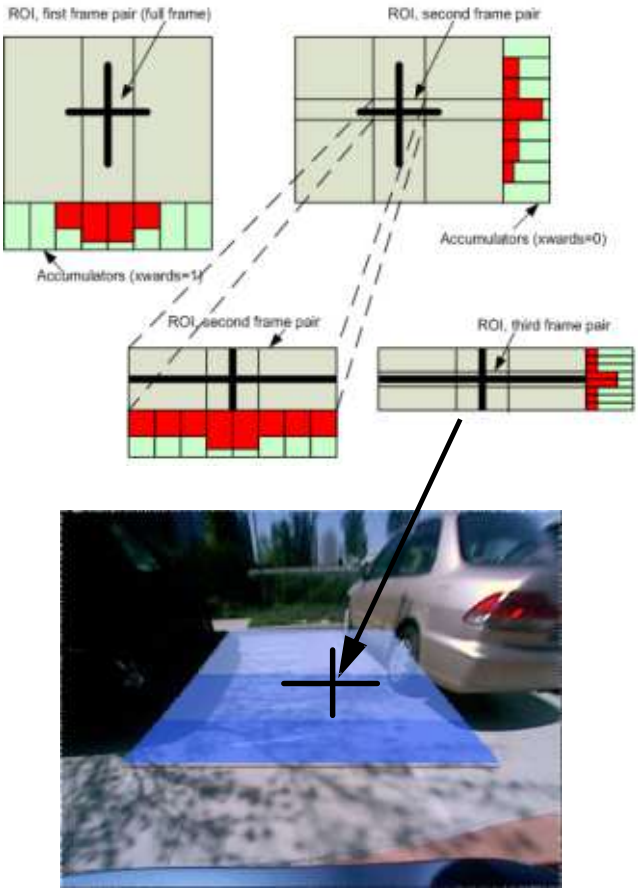


Figure 25. Overlay Calibration

The position of the target will be used to determine the calibration value that shifts the row and column position of adjustable overlay graphics.

The overlay calibration is intended to be applied on a device by device basis “in system,” which means after the camera has been installed. **onsemi** provides basic programming scripts that may reside in the SPI Flash memory to assist in this effort.

OVERLAY CHARACTER GENERATOR

In addition to the four overlay layers, a fifth layer exists for a character generator overlay string.

There are a total of:

- 16 alphanumeric characters available
- 22 characters maximum per line
- 16 x 32 pixels with 1−bit color depth

Any update to the character generator string requires the string to be passed in its entirety with the Host Command. Character strings have their own control properties aside from the Overlay bitmap properties.

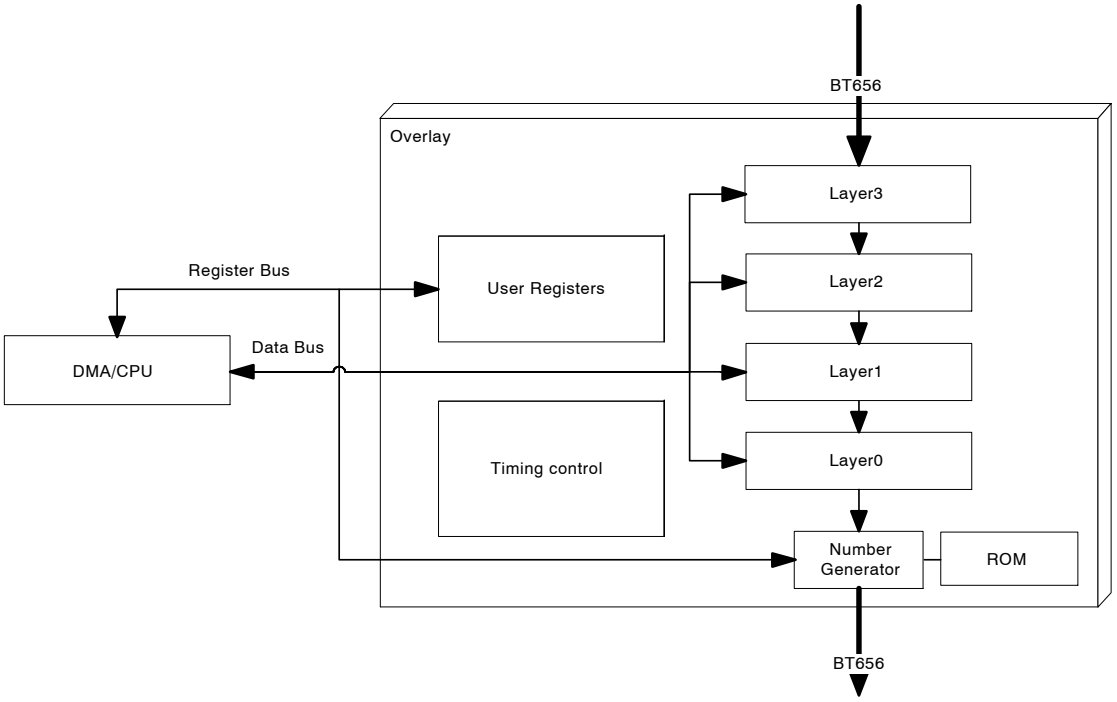


Figure 26. Internal Block Diagram Overlay

Character Generator

The character generator can be seen as the fifth top layer, but instead of getting the source from RLE data in the memory buffers, it has 16 predefined characters stored in ROM.

All the characters are 1−bit depth color and are sharing the same YCbCr look up table.

ROM	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x02	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
0x06	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0
0x08	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
0x0a	0	0	0	1	1	1	1	0	0	1	1	1	1	0	0	0
0x0c	0	0	0	1	1	1	0	0	0	0	1	1	1	1	0	0
0x0e	0	0	1	1	1	1	0	0	0	0	0	1	1	1	0	0
0x10	0	0	1	1	1	0	0	0	0	0	0	1	1	0	0	0
0x12	0	0	1	1	1	0	0	0	0	0	0	1	1	1	1	0
0x14	0	1	1	1	1	0	0	0	0	0	0	0	1	1	1	0
0x16	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x18	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x1a	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x1c	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x1e	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x20	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x22	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x24	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x26	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x28	0	0	1	1	1	0	0	0	0	0	0	0	1	1	1	0
0x2a	0	0	1	1	1	0	0	0	0	0	0	1	1	1	1	0
0x2c	0	0	1	1	1	0	0	0	0	0	0	1	1	1	0	0
0x2e	0	0	1	1	1	1	0	0	0	0	0	1	1	1	0	0
0x30	0	0	0	1	1	1	0	0	0	0	1	1	1	0	0	0
0x32	0	0	0	1	1	1	1	0	0	1	1	1	1	0	0	0
0x34	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
0x36	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0
0x38	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
0x3a	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x3c	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x3e	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

…

Figure 27. Example of Character Descriptor 0 Stored in ROM

It can show a row of up to 22 characters of 16 x 32 pixels resolution (32 x 32 pixels when blended with the BT 656 data).

Character Generator Details

Table 23. CHARACTER GENERATOR DETAILS

Item	Quantity	Description
16−bit character	22	Code for one of these characters: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, /, (space), :, −, (comma), (period)
1 bpp color	1	Depth of the bit map is 1 bpp

It is the responsibility of the user to set up proper values in the character positioning to fit them in the same row (that is one of the reasons that 22 is the maximum number of characters).

NOTE: No error is generated if the character row overruns the horizontal or vertical limits of the frame.

Full Character Set for Overlay

Figure 28 shows all of the characters that can be generated by the ASX340AT.

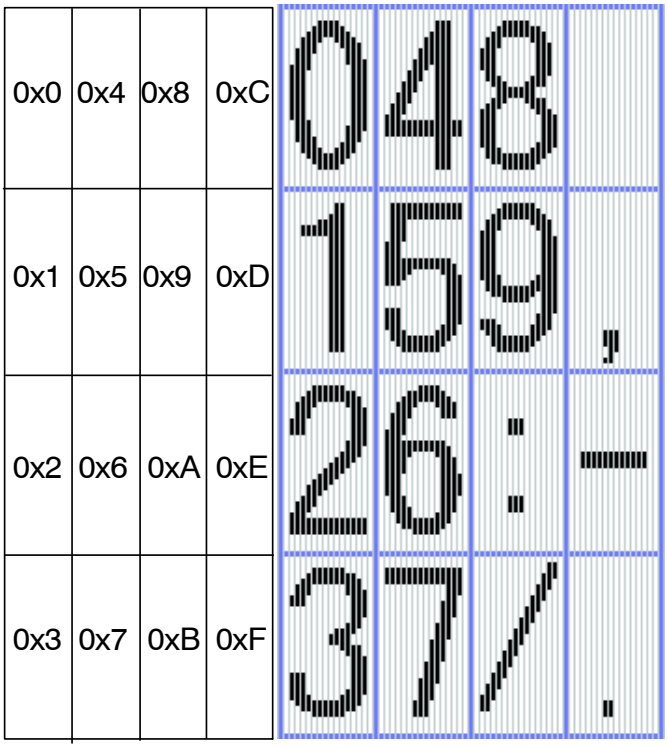


Figure 28. Full Character Set for Overlay

MODES AND TIMING

This section provides an overview of the typical usage modes and related timing information for the ASX340AT.

Composite Video Output

The external pin DOUT_LSB0 can be used to configure the device for default NTSC or PAL operation (auto−config mode). This and other video configuration settings are available as register settings accessible through the serial interface.

NTSC

Both differential and single−ended connections of the full NTSC format are supported. The differential connection that uses two output lines is used for low noise or long distance applications. The single−ended connection is used for PCB tracks and screened cable where noise is not a concern. The NTSC format has three black lines at the bottom of each image for padding (which most LCDs do not display).

PAL

The PAL format is supported with 576 active image rows.

Single−Ended and Differential Composite Output

The composite output can be operated in a single−ended or differential mode by simply changing the external resistor configuration. Refer to the Developer Guide for configuration options.

Parallel Output (DOUT)

The DOUT[7:0] port supports both progressive and Interlaced mode. Progressive mode (with FV and LV signal) include raw bayer(8 or 10 bit), YCbCr, RGB. Interlaced mode is CCIR656 compliant.

Figure 29 shows the data that is output on the parallel port for CCIR656. Both NTSC and PAL formats are displayed. The blue values in Figure 29 represent NTSC (525/60). The red values represent PAL (625/50).

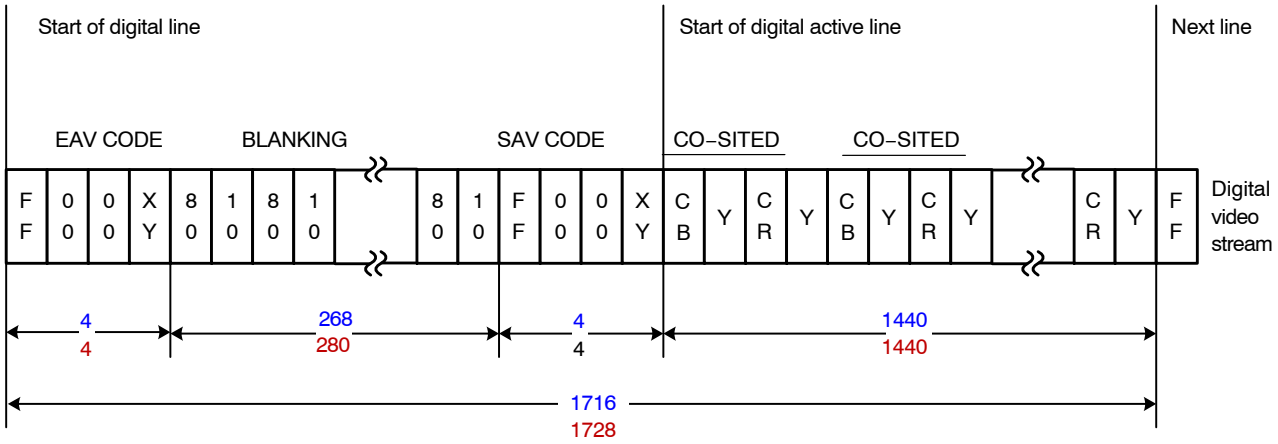


Figure 29. CCIR656 8−Bit Parallel Interface Format for 525/60 (625/50) Video Systems

Figure 30 shows detailed vertical blanking information for NTSC timing. Table 24 for data on field, vertical blanking, EAV, and SAV states.

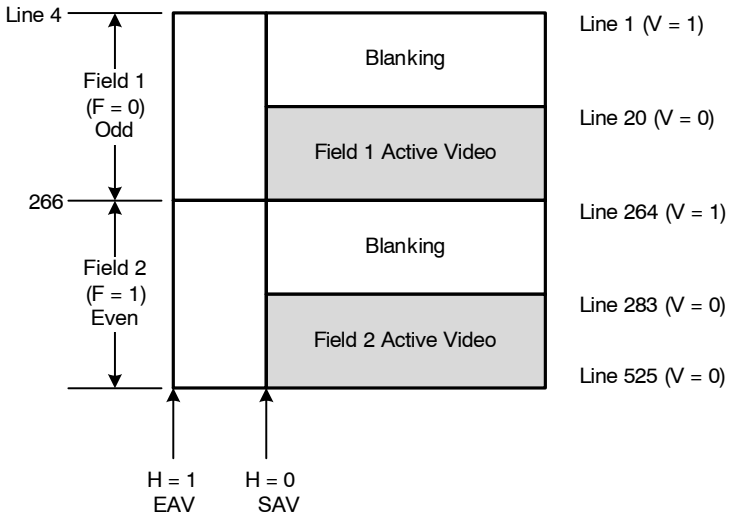


Figure 30. Typical CCIR656 Vertical Blanking Intervals for 525/60 Video System

Table 24. FIELD, VERTICAL BLANKING, EAV, AND SAV STATES 525/60 VIDEO SYSTEM

Line Number	F	V	H (EAV)	H (SAV)
1–3	1	1	1	0
4–9	0	1	1	0
20–263	0	0	1	0
264–265	0	1	1	0
266–282	1	1	1	0
283–525	1	0	1	0

3. NTSC defines active video from line 20 to line 263 (corresponding to a field). This allows up to 244 active video lines in a field.
4. ASX340 image output is configured to 240 lines per field; this is common practice of digital video formatting.
5. When 240 lines are displayed within a field of 244 lines, the image content should start from line 22 to line 261 of the field. This ensures center of the image and the center of the field is aligned.
6. Similar consideration applies to Odd & Even fields.

Figure 31 shows detailed vertical blanking information for PAL timing. See Table 25 for data on field, vertical blanking, EAV, and SAV states.

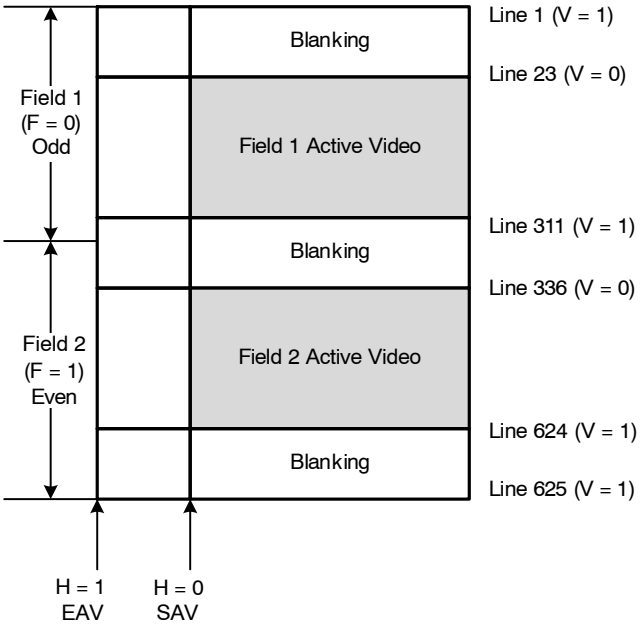


Figure 31. Typical CCIR656 Vertical Blanking Intervals for 625/50 Video System

Table 25. FIELD, VERTICAL BLANKING, EAV, AND SAV STATES FOR 625/50 VIDEO SYSTEM

Line Number	F	V	H (EAV)	H (SAV)
1–22	0	1	1	0
23–310	0	0	1	0
311–312	0	1	1	0
313–335	1	1	1	0
336–623	1	0	1	0
624–625	1	1	1	0

Reset and Clocks

Reset

Power−up reset is asserted or de−asserted with the RESET_BAR pin, which is active LOW. In the reset state, all control registers are set to default values. See “Device Configuration” for more details on Auto, Host, and Flash configurations.

Soft reset is asserted or de−asserted by the two−wire serial interface. In soft−reset mode, the two−wire serial interface and the register bus are still running. All control registers are reset using default values.

Clocks

The ASX340AT has two primary clocks:

- A master clock coming from the EXTCLK signal.
- In default mode, a pixel clock (PIXCLK) running at 2 × EXTCLK. In raw Bayer bypass mode, PIXCLK runs at the same frequency as EXTCLK.

When the ASX340AT operates in raw Bayer bypass mode, the image flow pipeline clocks can be shut off to conserve power.

The sensor core is a master in the system. The sensor core frame rate defines the overall image flow pipeline frame rate. Horizontal blanking and vertical blanking are influenced by the sensor configuration, and are also a function of certain image flow pipeline functions. The relationship of the primary clocks is depicted in Figure 32.

The image flow pipeline typically generates up to 16 bits per pixel − for example, YCbCr or 565RGB − but has only an 8−bit port through which to communicate this pixel data.

To generate NTSC or PAL format images, the sensor core requires a 27 MHz clock.

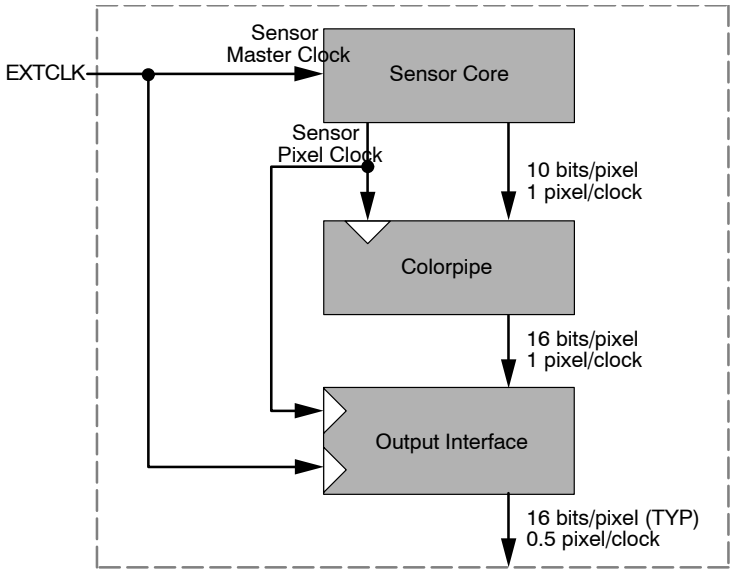


Figure 32. Primary Clock Relationships

Floating Inputs

The following ASX340AT pins cannot be floated:

- SDATA–This pin is bidirectional and should not be floated
- FRAME_SYNC
- TRST_N
- SCLK
- SADDR
- ATEST1
- ATEST2

Output Data Ordering

Table 26. OUTPUT DATA ORDERING IN DOUT RGB MODE

Mode (Swap Disabled)	Byte	D7	D6	D5	D4	D3	D2	D1	D0
565RGB	First	R7	R6	R5	R4	R3	G7	G6	G5
	Second	G4	G3	G2	B7	B6	B5	B4	B3
555RGB	First	0	R7	R6	R5	R4	R3	G7	G6
	Second	G5	G4	G3	B7	B6	B5	B4	B3
444xRGB	First	R7	R6	R5	R4	G7	G6	G5	G4
	Second	B7	B6	B5	B4	0	0	0	0
x444RGB	First	0	0	0	0	R7	R6	R5	R4
	Second	G7	G6	G5	G4	B7	B6	B5	B4

7. PIXCLK is 54 MHz when EXTCLK is 27 MHz.

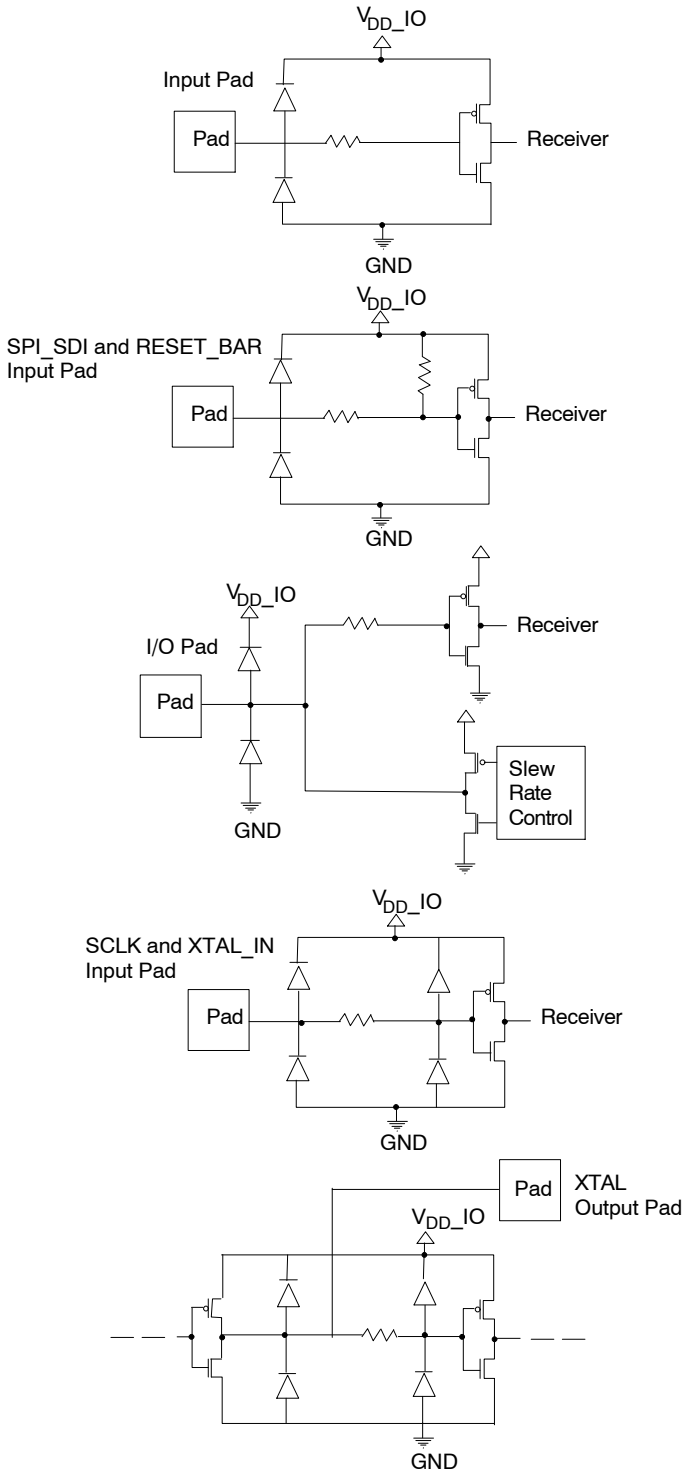
Table 27. OUTPUT DATA ORDERING IN SENSOR STAND−ALONE MODE

Mode	D7	D6	D5	D4	D3	D2	D1	D0	DOUT_LSB1	DOUT_LSB0
10−bit Output	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

8. PIXCLK is 27 MHz when EXTCLK is 27 MHz.

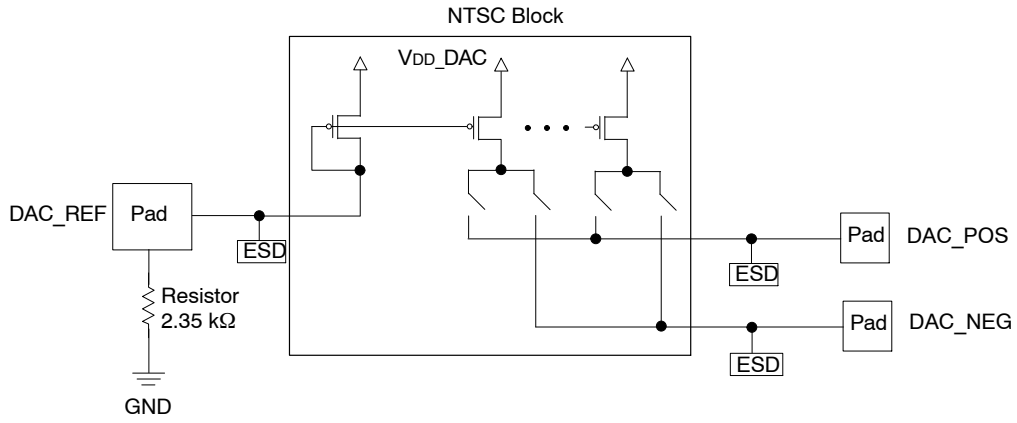
I/O Circuitry

Figure 33 illustrates typical circuitry used for each input, output, or I/O pad.



NOTE: All I/O circuitry shown above is for reference only. The actual implementation may be different.

Figure 33. Typical I/O Equivalent Circuits



NOTE: All I/O circuitry shown above is for reference only. The actual implementation may be different.

Figure 34. NTSC Block

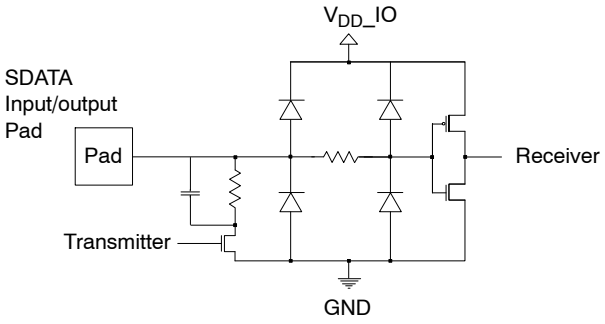


Figure 35. Serial Interface

I/O Timing

Digital Output

By default, the ASX340AT launches pixel data, FV, and LV synchronously with the falling edge of PIXCLK. The expectation is that the user captures data, FV, and LV using the rising edge of PIXCLK. The timing diagram is shown in.

As an option, the polarity of the PIXCLK can be inverted from the default by programming R0x0016[14].

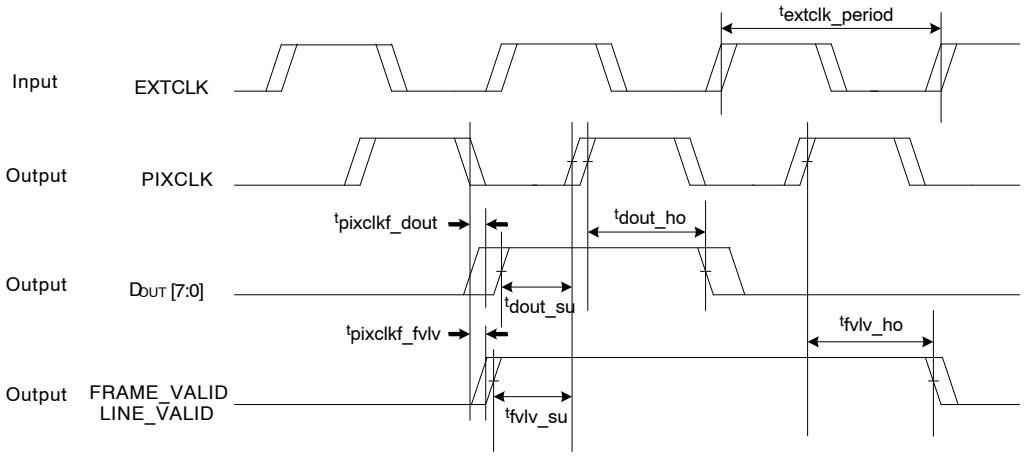


Figure 36. Digital Output I/O Timing

Table 28. PARALLEL DIGITAL OUTPUT I/O TIMING
(^{f}EXTCLK = 27 MHz; V_{dd} = 1.8 V; V_{dd}_IO = 2.8 V; V_{aa} = 2.8 V; V_{aa}_PIX = 2.8 V; V_{dd}_PLL = 2.8 V; V_{dd}_DAC = 2.8 V; Default slew rate)

Signal	Parameter	Conditions	Min	Typ	Max	Unit
EXTCLK	^{f}extclk		6	27	54	MHz
	^{t}extclk_period		18.52	37	166.67	ns
EXTCLK	Duty cycle		45	50	55	%
PIXCLK (Note 9)	^{f}pixclk		6	27	54	MHz
	^{t}pixclk_period		18.52	37.04	166.67	ns
	Duty cycle		45	50	55	%
DATA[7:0]	^{t}pixclkf_dout		1.55	–	1.9	ns
	^{t}dout_su		18	–	20	ns
	^{t}dout_ho		18	–	20	ns
FV/LV	^{t}pixclkf_fvlv		1.6	–	3.05	ns
	^{t}fvlv_su		15	–	16	ns
	^{t}fvlv_ho		20	–	21	ns

9. PIXCLK can be inverted from the default by programming R0x0016[14].

Table 29. SLEW RATE FOR PIXCLK AND D_{OUT}
(^{f}EXTCLK = 27 MHz; V_{dd} = 1.8 V; V_{dd}_IO = 2.8 V; V_{aa} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{dd}_PLL = 2.8 V; V_{dd}_DAC = 2.8 V; T = 25°C; C_{load} = 40 pF)

PIXCLK			DOUT[7:0]			Unit
R0x1E [10:8]	Rise Time	Fall Time	R0x1E [2:0]	Rise Time	Fall Time	
000	NA	NA	000	15.0	13.5	ns
001	NA	NA	001	9.0	8.5	ns
010	7.0	6.9	010	6.8	6.0	ns
011	5.2	5.0	011	5.2	4.8	ns
100	4.0	3.8	100	3.8	3.5	ns
101	3.0	2.8	101	3.3	3.3	ns
110	2.4	2.2	110	3.0	3.0	ns
111	1.9	1.7	111	2.8	2.8	ns

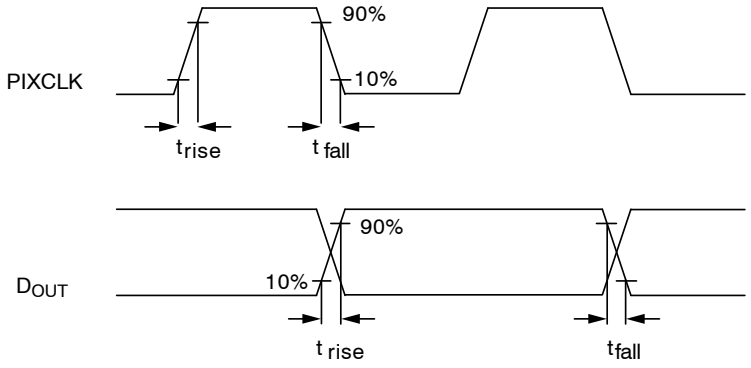


Figure 37. Slew Rate Timing

Configuration Timing

During start−up, the Dout_LSB0, LV and FV are sampled. Setup and hold timing for the RESET_BAR signal with respect to Dout_LSB0, LV, and FV are shown in Figure 38 and Table 30. These signals are sampled once by the on−chip firmware, which yields a long thold time.

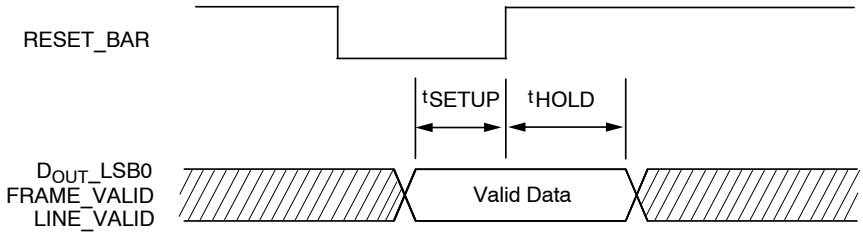


Figure 38. Configuration Timing

Table 30. CONFIGURATION TIMING

Signal	Parameter	Min	Typ	Max	Unit
Dout_LSB0, FRAME_VALID, LINE_VALID	tsetup	0			μs
	thold	50			μs

10. Table data is based on EXTCLK = 27 MHz.

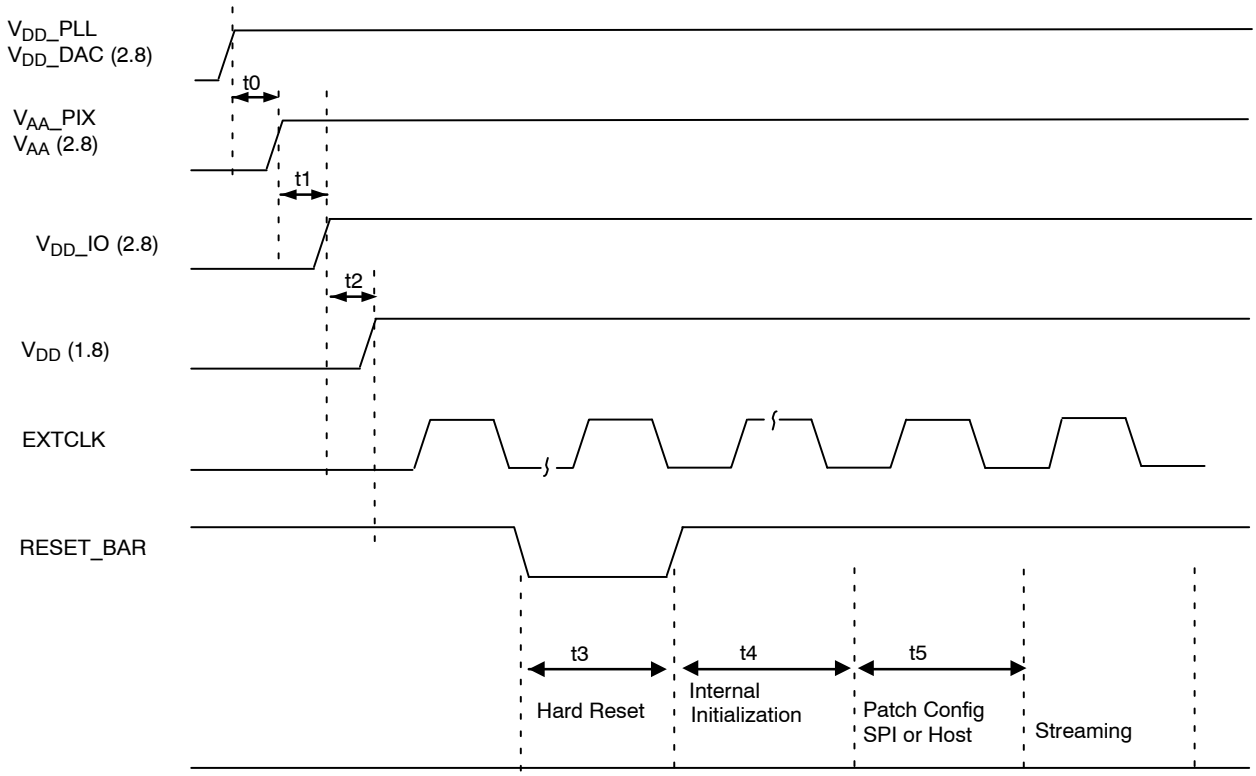


Figure 39. Power Up Sequence

Table 31. POWER UP SEQUENCE

Definition	Symbol	Min	Typical	Max	Unit
Vdd_PLL to Vaa/Vaa_PIX	t0	0	–	–	μs
Vaa/Vaa_PIX to Vdd_IO	t1	0	–	–	μs

Table 31. POWER UP SEQUENCE (continued)

Definition	Symbol	Min	Typical	Max	Unit
Vdd_IO to Vdd	t2	0	–	–	µs
Hard Reset	t3	2	–	–	µs
Internal Initialization	t4	14	–	–	ms

11. Delay between VDD and EXTCLK depends on customer devices, i.e. Xtal, Oscillator, and so on. There is no requirement on this from the sensor.
12. Hard reset time is the minimum time required after power rails are settled. Ten clock cycles are required for the sensor itself, assuming all power rails are settled. In a circuit where Hard reset is performed by the RC circuit, then the RC time must include the all power rail settle time and Xtal.
13. The time for Patch Config SPI or Host, that is, t5, depends on the patches being applied.

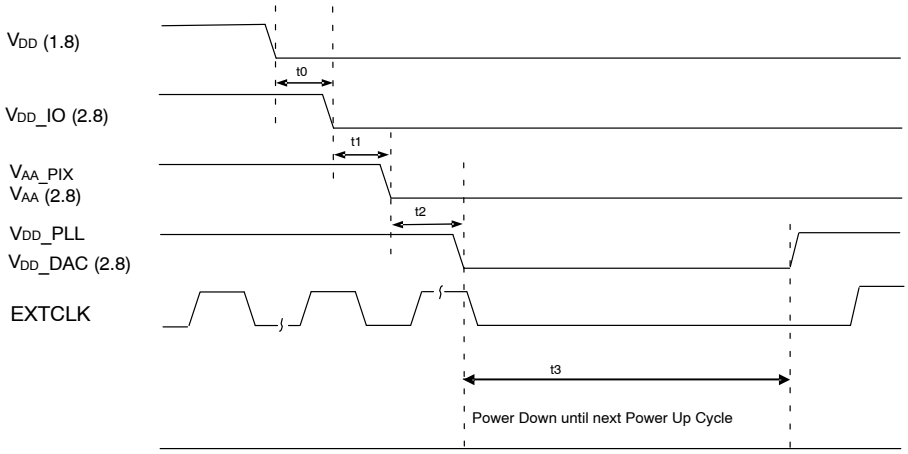


Figure 40. Power Down Sequence

Table 32. POWER DOWN SEQUENCE

Definition	Symbol	Min	Typical	Max	Unit
Vdd to Vdd_IO	t0	0	–	–	µs
Vdd_IO to Vaa/Vaa_PIX	t1	0	–	–	µs
Vaa/Vaa_PIX to Vdd_PLL/DAC	t2	0	–	–	µs
Power Down until Next Power Up Time	t3	100 (Note 14)	–	–	ms

14. t3 is required between power down and next power up time, all decoupling caps from regulators must completely discharge before next power up.

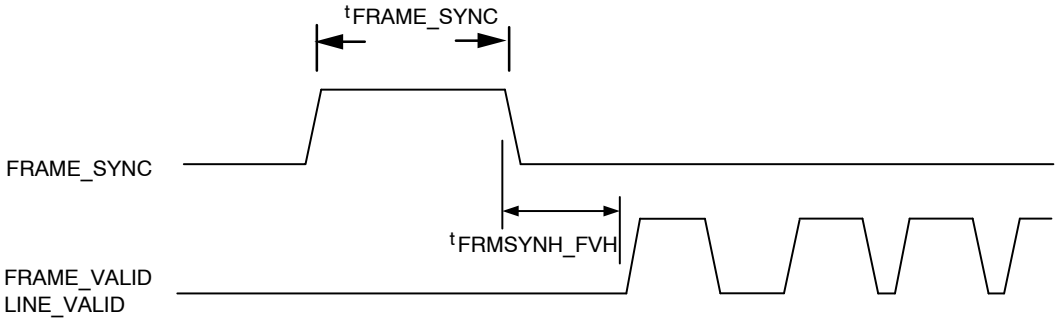


Figure 41. FRAME_SYNC to FRAME_VALID/LINE_VALID

Table 33. FRAME_SYNC TO FRAME_VALID/LINE_VALID PARAMETERS

Parameter	Name	Conditions	Min	Typical	Max	Unit
FRAME_SYNC to FV/LV	^{t}FRMSYNC_FVH	Interlaced mode	1.22	–	–	ms
^{t}FRAME_SYNC	^{t}FRAMESYNC		1			µs

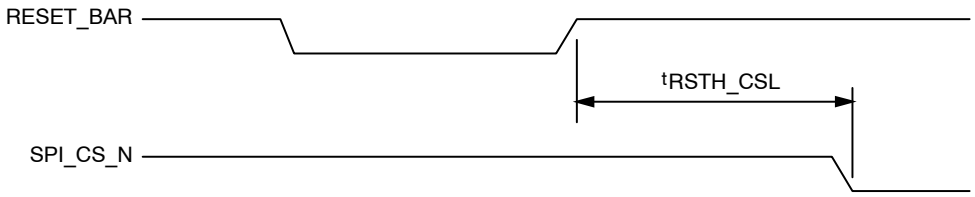


Figure 42. Reset to SPI Access Delay

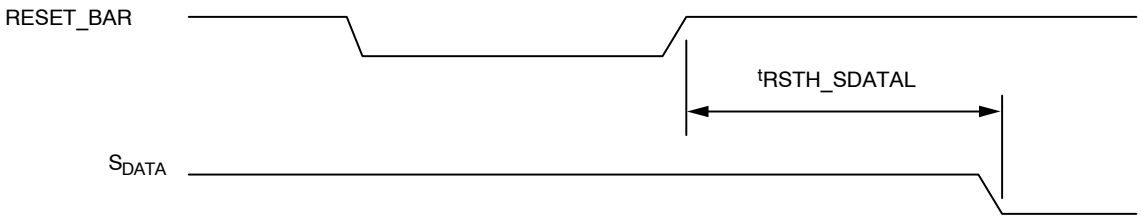


Figure 43. Reset to Serial Access Delay

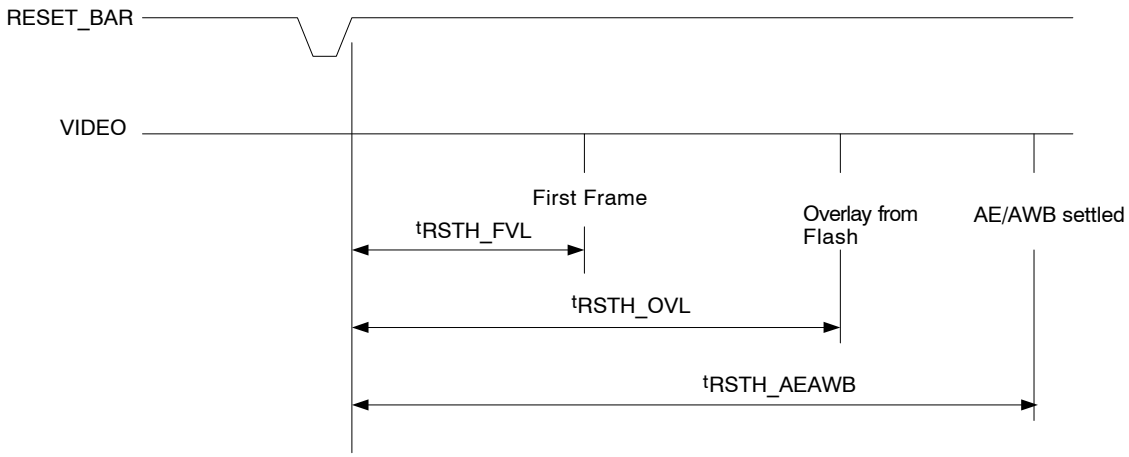


Figure 44. Reset to AE/AWB Image

Table 34. RESET_BAR DELAY PARAMETERS

Parameter	Name	Conditions	Min	Typical	Max	Unit
RESET_BAR HIGH to SPI_CS_N LOW	tRSTH_CSL		13	–	–	ms
RESET_BAR HIGH to Sdata LOW	tRSTH_SDATAL		18	–	–	ms
RESET_BAR HIGH to FRAME_VALID	tRSTH_FVL		14	–	–	ms
RESET_BAR HIGH to first Overlay	tRSTH_OVL	Overlay size dependent	–	–	–	ms
RESET_BAR HIGH to AE/AWB settled	tRSTH_AEAWB	Scene dependent	–	–	–	ms

Table 34. RESET_BAR DELAY PARAMETERS (continued)

Parameter	Name	Conditions	Min	Typical	Max	Unit
RESET_BAR HIGH to first NTSC frame	tRSTH_NTSC		47	–	–	ms
RESET_BAR HIGH to first PAL frame	tRSTH_PAL		53	–	–	ms

ELECTRICAL SPECIFICATIONS

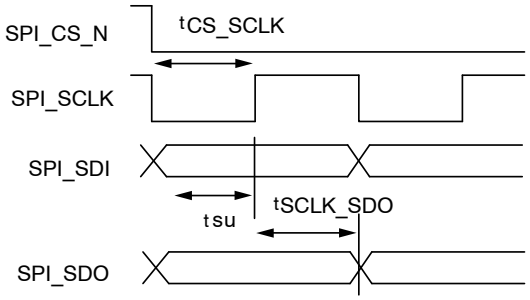


Figure 45. SPI Output Timing

Table 35. SPI DATA SETUP AND HOLD TIMING

Parameter	Name	Conditions	Min	Typical	Max
^{f}SPI_SCLK	SPI_SCLK Frequency	1.6875	4.5	18	MHz
t_{SPI_SCLK}	SPI_SCLK Period	55.556		592.593	ns
^{t}su	Setup time			0.5 × $^{t}_{SPI_SCLK}$	ns
^{t}SCLK_SDO	Hold time			0.5 × $^{t}_{SPI_SCLK}$ + 20	ns
^{t}CS_SCLK	Delay from falling edge of SPI_CS_N to rising edge of SPI_SCLK		230		ns

Table 36. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating		Unit
		Min	Max	
Vdd	Digital power (1.8 V)	−0.3	2.4	V
Vdd_IO	I/O power (2.8 V)	−0.3	4	V
Vaa	Vaa analog power (2.8 V)	−0.3	4	V
Vaa_PIX	Pixel array power (2.8 v)	−0.3	4	V
Vdd_PLL	PLL power (2.8 V)	−0.3	4	V
Vdd_DAC	DAC power (2.8 V)	−0.3	4	V
Vin	DC Input Voltage	−0.3	Vdd_IO + 0.3	V
Vout	DC Output Voltage	−0.3	Vdd_IO + 0.3	V
Tstg	Storage temperature	−50	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
15. “Rating” column gives the maximum and minimum values that the device can tolerate.

Table 37. ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

Parameter (Note 16)	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Core digital voltage (Vdd)	–	1.70	1.8	1.95	V
IO digital voltage (Vdd_IO)	–	2.66	2.8	2.94	V
Video DAC voltage (Vdd_DAC)	–	2.66	2.8	2.94	V
PLL Voltage (Vdd_PLL)	–	2.66	2.8	2.94	V
Analog voltage (Vaa)	–	2.66	2.8	2.94	V
Pixel supply voltage (Vaa_pix)	–	2.66	2.8	2.94	V
Imager operating temperature (Note 17)	–	–40		+105	°C
Functional operating temperature (Note 18)		–40		+85	°C
Storage temperature	–	–50		+150	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

16. V_{AA} and V_{AA}_PIX must all be at the same potential to avoid excessive current draw. Care must be taken to avoid excessive noise injection in the analog supplies if all three supplies are tied together.
17. The imager operates in this temperature range, but image quality may degrade if it operates beyond the functional operating temperature range.
18. Image quality is not guaranteed at temperatures equal to or greater than this range.

Table 38. VIDEO DAC ELECTRICAL CHARACTERISTICS–SINGLE−ENDED MODE

(^{f}EXTCLK = 27 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 2.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V; V_{DD}_DAC = 2.8 V)

Parameter	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Resolution		–	10	–	bits
DNL		–	0.2	0.4	bits
INL		–	0.7	3.5	bits
Output local load	Output pad (DAC_POS)	–	37.5	–	Ω
	Unused output (DAC_NEG)	–	37.5	–	Ω
Output voltage	Single−ended mode, code 000h	–	.021	–	V
	Single−ended mode, code 3FFh	–	1.392	–	V
Output current	Single−ended mode, code 000h	–	0.560	–	mA
	Single−ended mode, code 3FFh	–	37.120	–	mA
Supply current	Estimate	–	–	25.0	mA
DAC_REF	DAC Reference	–	1.200	–	V
R DAC_REF	DAC Reference	–	2.4	–	kΩ

19. DAC_POS, DAC_NEG, and DAC_REF are loaded with resistors to simulate video output driving into a low pass filter and achieve a full output swing of 1.4 V. Their resistor loadings may be different from the loadings in a real single−ended or differential−ended video output system with an actual receiving end. Please refer to the Developer Guide for proper resistor loadings.

Table 39. VIDEO DAC ELECTRICAL CHARACTERISTICS–DIFFERENTIAL MODE

(^{f}EXTCLK = 27 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 2.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V; V_{DD}_DAC = 2.8 V)

Parameter	**Condition**	**Min**	**Typ**	**Max**	**Unit**
DNL		–	0.2	0.4	Bits
INL		–	0.7	3.5	Bits
Output local load	Differential mode per pad (DAC_POS and DAC_NEG)	–	37.5	–	Ω

Table 39. VIDEO DAC ELECTRICAL CHARACTERISTICS–DIFFERENTIAL MODE (continued)
(^{f}EXTCLK = 27 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 2.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V; V_{DD}_DAC = 2.8 V)

Parameter	Condition	Min	Typ	Max	Unit
Output voltage	Differential mode, code 000h, pad dacp	–	.022	–	V
	Differential mode, code 000h, pad dacn	–	1.421	–	V
	Differential mode, code 3FFh, pad dacp	–	1.421	–	V
	Differential mode, code 3FFH, pad dacn	–	.022	–	V
Output current	Differential mode, code 000h, pad dacp	–	.587	–	mA
	Differential mode, code 000h, pad dacn	–	37.893	–	mA
	Differential mode, code 3FFh, pad dacp	–	37.893	–	mA
	Differential mode, code 3FFH, pad dacn	–	.587	–	mA
Supply current	Estimate	–	–	50	mA
DAC_REF	DAC Reference	–	1.2		V
R DAC_REF	DAC Reference		2.4		kΩ

20. DAC_POS, DAC_NEG, and DAC_REF are loaded with resistors to simulate video output driving into a low pass filter and achieve a full output swing of 1.4 V. Their resistor loadings may be different from the loadings in a real single−ended or differential−ended video output system with an actual receiving end. Please refer to the Developer Guide for proper resistor loadings.

Table 40. DIGITAL I/O PARAMETERS (T_A = Ambient = 25°C; All supplies at 2.8 V)

Signal	Parameter	Definition	Condition	Min	Typ	Max	Unit
All Outputs		Load capacitance		5	–	30	pF
	Voh	Output high voltage		0.7 × Vdd_IO		–	V
	Vol	Output low voltage		–	–	0.3 × Vdd_IO	V
	Ioh	Output high current	Voh = Vdd_IO – 0.4 V	20	–	35	mA
	Iol	Output low current	Vol = 0.4 V	29	–	53	mA
All Inputs	Vih	Input high voltage		0.7 × Vdd_IO	–	Vdd_IO + 0.5	V
	Vil	Input low voltage		–0.3	–	0.3 × Vdd_IO	V
	Iih	Input high leakage current		0.02	–	0.26	μA
	Iil	Input low leakage current		0.01	–	0.05	μA
	Signal CAP	Input signal capacitance		–	6.5	–	pF

21. All inputs are protected and may be active when all supplies (2.8 V and 1.8 V) are turned off.

Power Consumption, Operating Mode

Table 41. POWER CONSUMPTION – CONDITION 1
(f_{EXTCLK} = 27 MHz; T = 25°C, dark condition (lens with cover))

Power Plane	Supply	Condition 1	Typ Power	Max Power	Unit
Vdd	1.8		48.2	72	mW
Vdd_IO	2.8	Parallel off	2.2	10	mW
Vaa	2.8		96	140	mW
VAA_PIX	2.8		2.2	5	mW
Vdd_DAC	2.8	Single 75 Ω	122.9	146	mW
Vdd_PLL	2.8		18.8	25	mW
		Total	290.3	398	mW

Analog output uses single−ended mode: DAC_Pos = 75 Ω, DAC_Neg = 37.5 Ω, DAC_Ref = 2.4 kΩ, parallel output is disabled.

Table 42. POWER CONSUMPTION – CONDITION 2
(f_{EXTCLK} = 27 MHz; T = 25°C, dark condition (lens with cover), Cload = 40 pF)

Power Plane	Supply	Condition 1	Typ Power	Max Power	Unit
Vdd	1.8		47.5	72	mW
Vdd_IO	2.8	Parallel on	26.6	50	mW
Vaa	2.8		95.5	140	mW
VAA_PIX	2.8		2.2	5	mW
Vdd_DAC	2.8	VDAC off	1.1	5	mW
Vdd_PLL	2.8		18.8	25	mW
		Total	191.7	297	mW

Analog output is disabled; parallel output is enabled.

VIDEO Signal Parameters

Table 43. KEY VIDEO SIGNAL PARAMETER TABLE
(f_{EXTCLK} = 27 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 2.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V; V_{DD}_DAC = 2.8 V)

Parameter	NTSC	PAL	UNITS	Notes
Number of lines per frame	525	625	Hz	
Line Frequency	15734.264	15625	Hz	
Field Frequency	59.94	50	Hz	
Sync Level	40	43	IRE	23, 24
Burst Level	40	43	IRE	23, 24
Black Level	7.5	0	IRE	22, 23, 24
White Level	100	100	IRE	22, 23, 24

22. Black and white levels are referenced to the blanking level.
23. 1 IRE ~ 7.14 mV.
24. DAC ref = 2.8 kΩ; load = 37.5 Ω.
25. Reference to ITU−R BT.470−6.

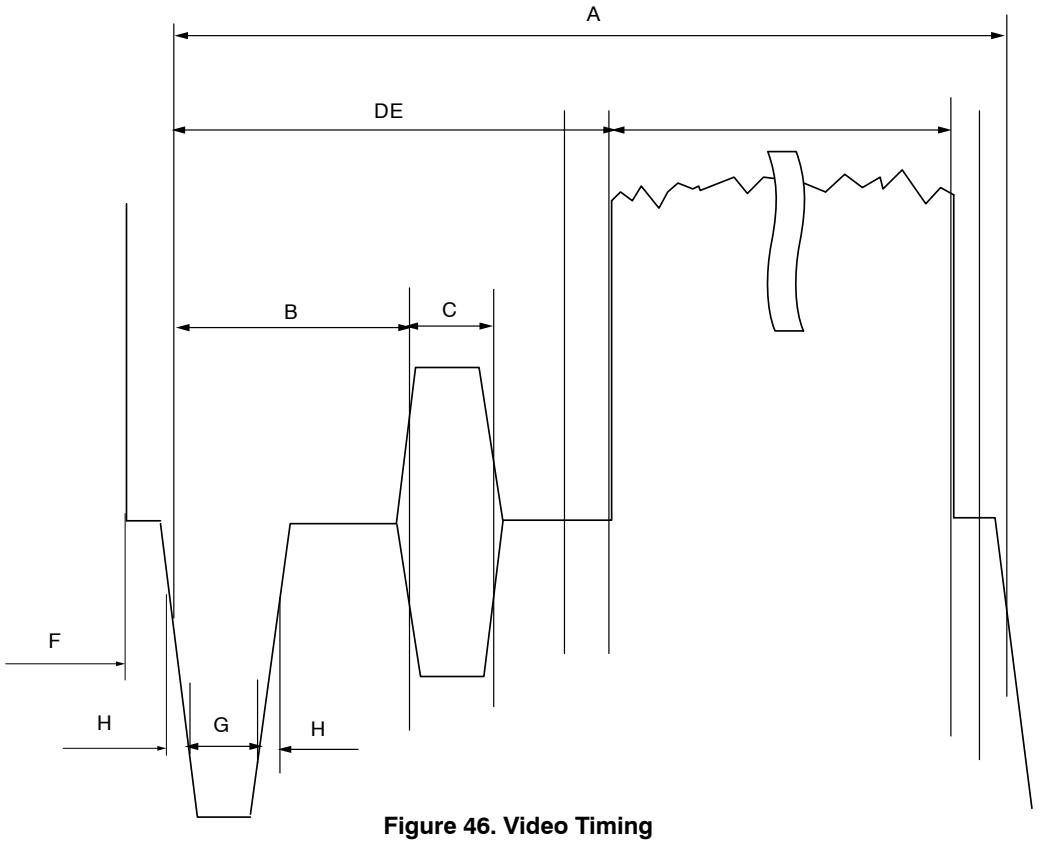


Figure 46. Video Timing

Table 44. VIDEO TIMING: SPECIFICATION FROM REC. ITU−R BT.470−6

Parameter	Signal	NTSC (27 MHz)	PAL (27 MHz)	Unit
A	H Period	63.556	64.00	µs
B	Hsync to burst	4.71 to 5.71	5.60 ±0.10	µs
C	burst	2.23 to 3.11	2.25 ±0.23	µs
D	Hsync to Signal	9.20 to 10.30	10.20 ±0.30	µs
E	Video Signal	52.655 ±0.20	52 +0, −0.3	µs
F	Front	1.27 to 2.22	1.5 +0.3, −0.0	µs
G	Hsync Period	4.70 ± 0.10	4.70 ±0.20	µs
H	Sync rising/falling edge	≤ 0.25	0.20 ±0.10	µs

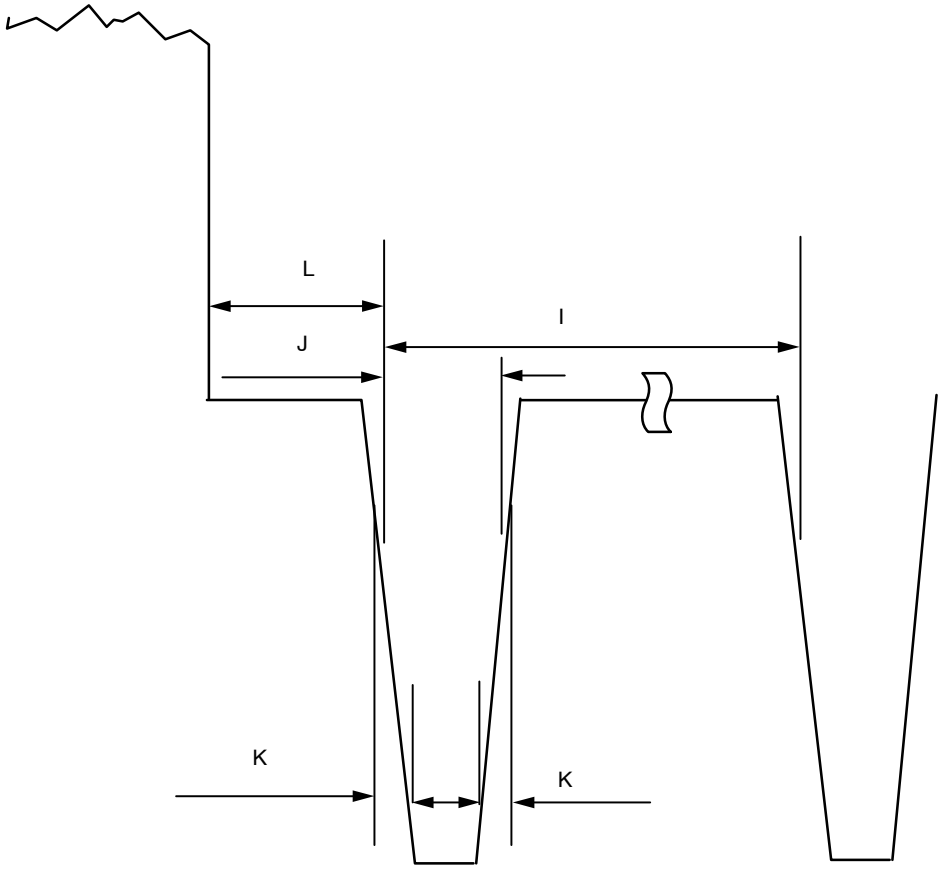


Figure 47. Equalizing Pulse

Table 45. EQUALIZING PULSE: SPECIFICATION FROM REC. ITU−R BT.470−6

Parameter	Signal	NTSC (27 MHz)	PAL (27 MHz)	Units
I	H/2 Period	31.778	32.00	µs
J	Pulse width	2.30 ±0.10	2.35 ±0.10	µs
K	Pulse rising/falling edge	≤0.25	0.25 ±0.05	µs
L	Signal to pulse	1.50 ±0.10	3.0 ±2.0	µs

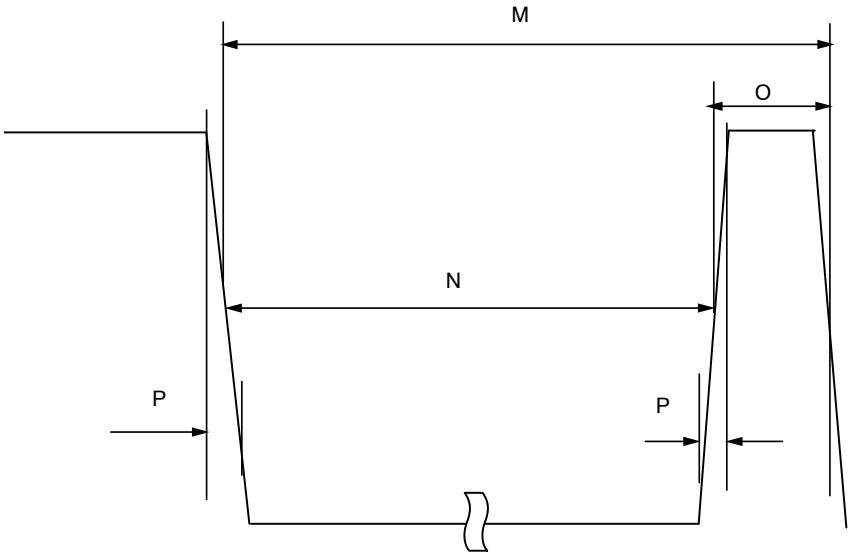


Figure 48. V Pulse

Table 46. V PULSE: SPECIFICATION FROM REC. ITU−R BT.470−6

Parameter	Signal	NTSC (27 MHz)	PAL (27 MHz)	Unit
M	H/2 Period	31.778	32.00	µs
N	Pulse width	27.10 (nominal)	27.30 ±0.10	µs
O	V pulse interval	4.70 ±0.10	4.70 ±0.10	µs
P	Pulse rising/falling edge	≤0.25	0.25 ±0.05	µs

Two−Wire Serial Bus Timing

Figure 49 and Table 47 describe the timing for the two−wire serial interface.

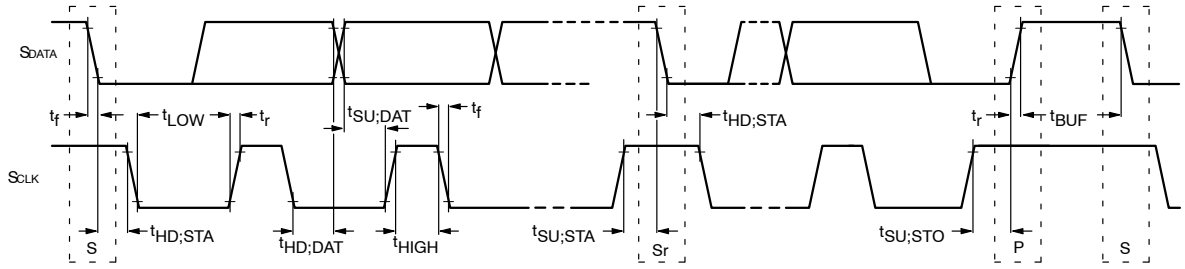


Figure 49. Two−Wire Serial Bus Timing Parameters

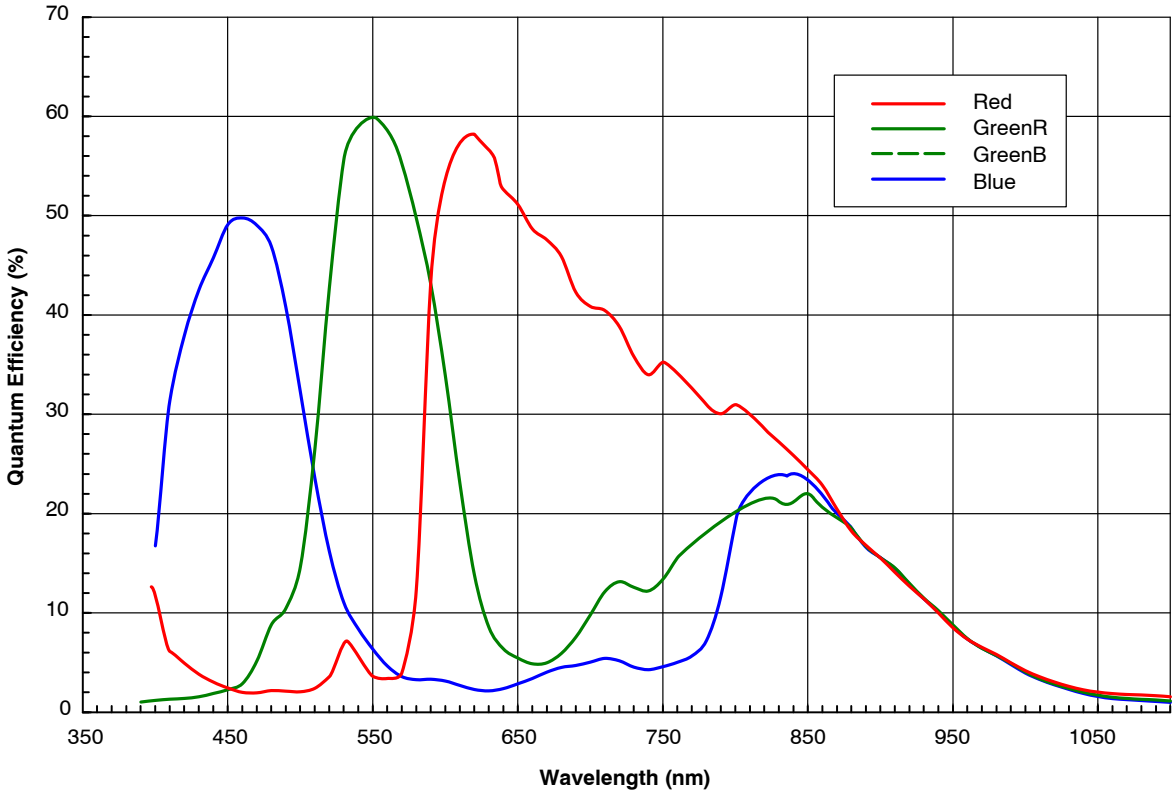
Table 47. TWO−WIRE SERIAL BUS CHARACTERISTICS

(f_{EXTCLK} = 27 MHz; V_{dd} = 1.8 V; V_{dd}_IO = 2.8 V; V_{aa} = 2.8 V; V_{aa}_PIX = 2.8 V; V_{dd}_PLL = 2.8 V; V_{dd}_DAC = 2.8 V; T_A = 25°C)

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
Sclk Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition						
After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	–	0.6	–	μs
LOW period of the Sclk clock	t_{LOW}	4.7	–	1.3	–	μs
HIGH period of the Sclk clock	t_{HIGH}	4.0	–	0.6	–	μs
Se−up time for a repeated START condition	$t_{SU;STA}$	4.7	–	0.6	–	μs
Data hold time	$t_{HD;DAT}$	0 (Note 29)	3.45 (Note 30)	0[6]	0.9 (Note 30)	μs
Data set−up time	$t_{SU;DAT}$	250	–	100 (Note 31)	–	ns
Rise time of both Sdata and Sclk signals	t_r	–	1000	20 + 0.1Cb (Note 32)	300	ns
Fall time of both Sdata and Sclk signals	t_f	–	300	20 + 0.1Cb (Note 32)	300	ns
Set−up time for STOP condition	$t_{SU;STO}$	4.0	–	0.6	–	μs
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	1.3	–	μs
Capacitive load for each bus line	C_b	–	400	–	400	pF
Serial interface input pin capacitance	C_{IN_SI}	–	3.3	–	3.3	pF
Sdata max load capacitance	C_{LOAD_SD}	–	30	–	30	pF
Sdata pull−up resistor	R_{SD}	1.5	4.7	1.5	4.7	kΩ

26. This table is based on I²C standard (v2.1 January 2000).
27. Two−wire control is I²C−compatible.
28. All values referred to V_{IHmin} = 0.9 VDD and V_{ILmax} = 0.1VDD levels. Sensor EXCLK = 27 MHz.
29. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of SCLK.
30. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCLK signal.
31. A Fast−mode I²C−bus device can be used in a Standard−mode I²C−bus system, but the requirement $t_{SU;DAT}$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must output the next data bit to the SDATA line t_r max + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard−mode I²C−bus specification) before the SCLK line is released.
32. Cb = total capacitance of one bus line in pF.

SPECTRAL CHARACTERISTICS

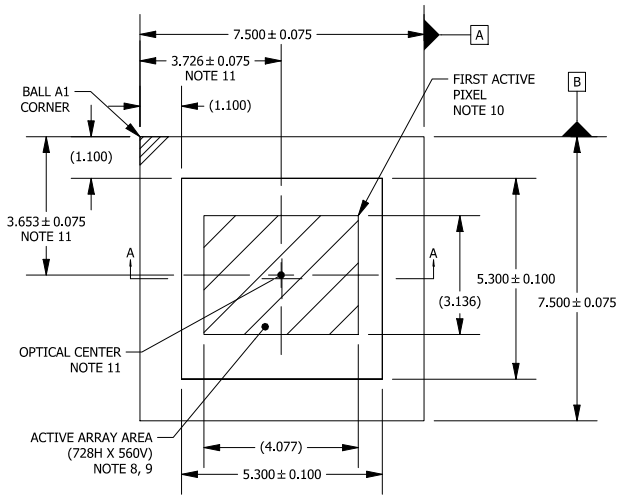


NOTE: The measurements were done on packaged parts with regular glass coating (that is, without Anti−Reflective Glass (ARC) coating).

Figure 50. Quantum Efficiency

IBGA63 7.5x7.5
CASE 503AE
ISSUE A

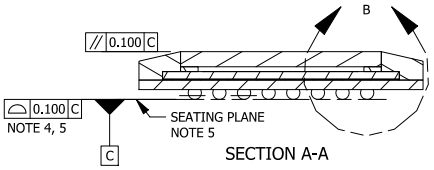
DATE 10 MAR 2020



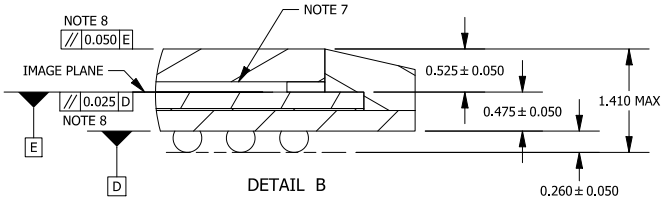
TOP VIEW

NOTES:

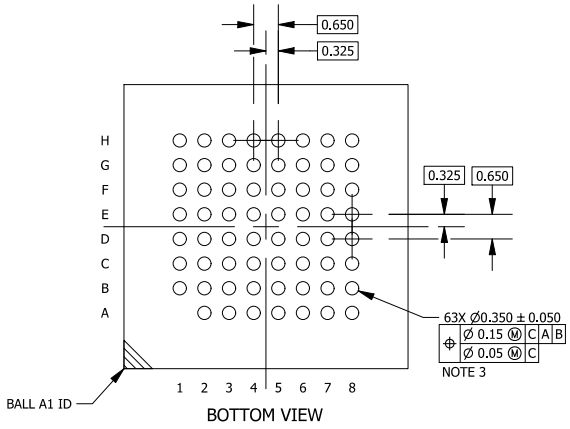
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS [mm].
3. SOLDER BALL DIAMETER IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DATUM C, THE SEATING PLANE IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. GLASS: 0.400 THICKNESS; REFRACTIVE INDEX = 1.52; AR COATING R<1% 420-850nm (EACH SIDE).
7. AIR GAP BETWEEN GLASS AND PIXEL ARRAY: 0.125 THICKNESS.
8. PARALLELISM APPLIES ONLY TO THE ACTIVE ARRAY.
9. MAXIMUM ROTATION OF ACTIVE ARRAY RELATIVE TO DATUMS A AND B IS ± 0.5°.
10. REFER TO THE DEVICE DATA SHEET FOR TOTAL PIXEL ARRAY DEFINITIONS.
11. OPTICAL CENTER RELATIVE TO PACKAGE CENTER (X, Y) = (-0.024, 0.097).
12. PACKAGE CENTER (X, Y) = (0.000, 0.000).



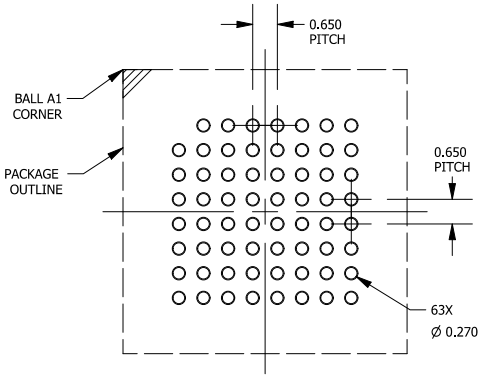
SECTION A-A



DETAIL B



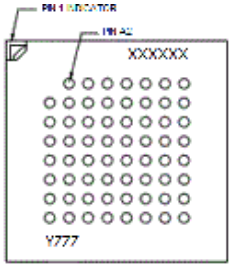
BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
Y = Year
ZZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**IBGA63 7.5X7.5**	**PAGE 1 OF 1**

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