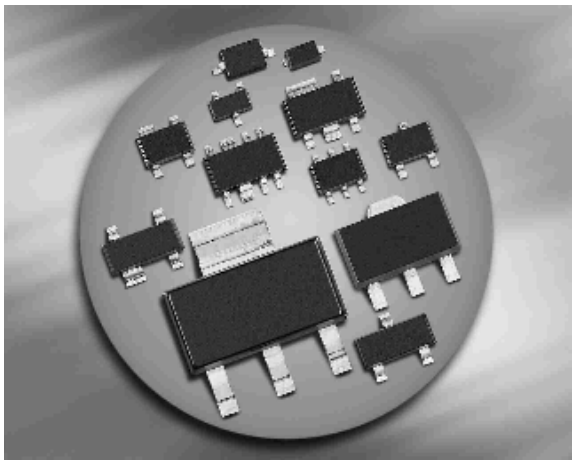
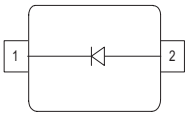
Silicon Tuning Diode

- For SAT tuners
- High capacitance ratio
- Low series resistance
- Excellent uniformity and matching due to "in-line" matching assembly procedure
- Pb-free (RoHS compliant) package



RoHS

BB837
BB857
BB857-02V



Type	Package	Configuration	Marking
BB837	SOD323	single	white M
BB857*	SCD80	single	OO
BB857-02V	SC79	single	P

* Not for new design

Maximum Ratings at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Value	Unit
Diode reverse voltage	V_R	30	V
Peak reverse voltage $R \geq 5k\Omega$	V_{RM}	35	
Forward current	I_F	20	mA
Operating temperature range	T_{op}	-55 ...150	°C
Storage temperature	T_{Stg}	-55 ...150	

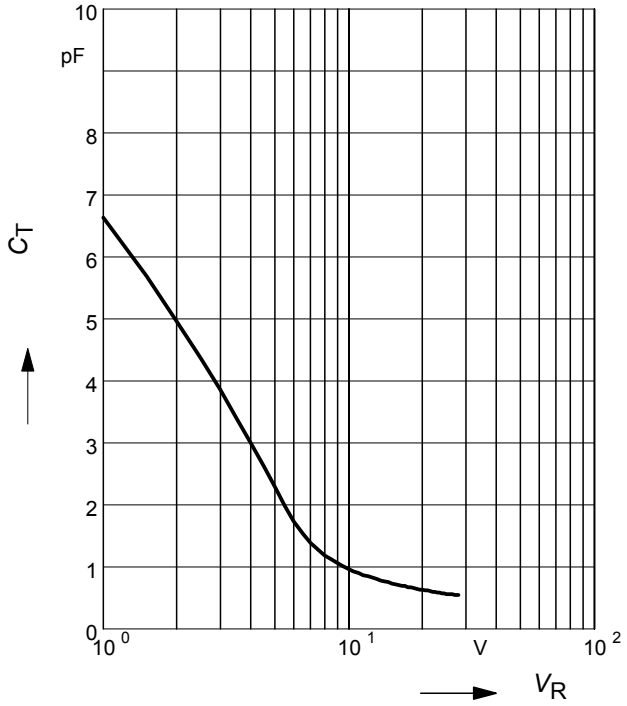
Electrical Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Reverse current	I_R				nA
V_R = 30 V		-	-	10	
V_R = 30 V, T_A = 85 °C		-	-	200	
AC Characteristics					
Diode capacitance	C_T				pF
V_R = 1 V, f = 1 MHz		6	6.6	7.2	
V_R = 25 V, f = 1 MHz		0.5	0.55	0.65	
V_R = 28 V, f = 1 MHz		0.45	0.52	-	
Capacitance ratio	C_{T1}/C_{T25}	10.2	12	-	-
V_R = 1 V, V_R = 25 V, f = 1 MHz					
Capacitance ratio	C_{T1}/C_{T28}	9.7	12.7	-	
V_R = 1 V, V_R = 28 V, f = 1 MHz					
Capacitance matching[1)]	$\Delta C_T/C_T$	-	-	5	%
V_R = 1V ... 28V, f = 1 MHz, 7 diodes sequence					
Series resistance	r_S	-	1.5	-	Ω
V_R = 5 V, f = 470 MHz					

[1]For details please refer to Application Note 047

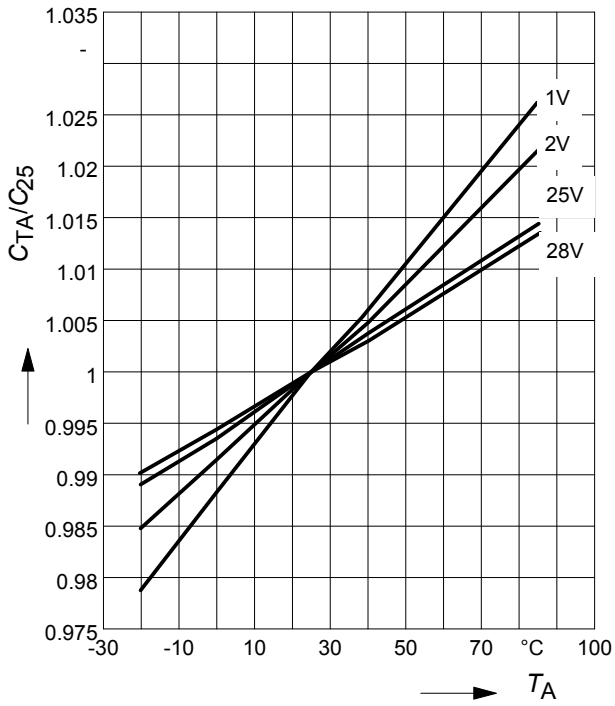
Diode capacitance $C_T = f(V_R)$

f = 1MHz



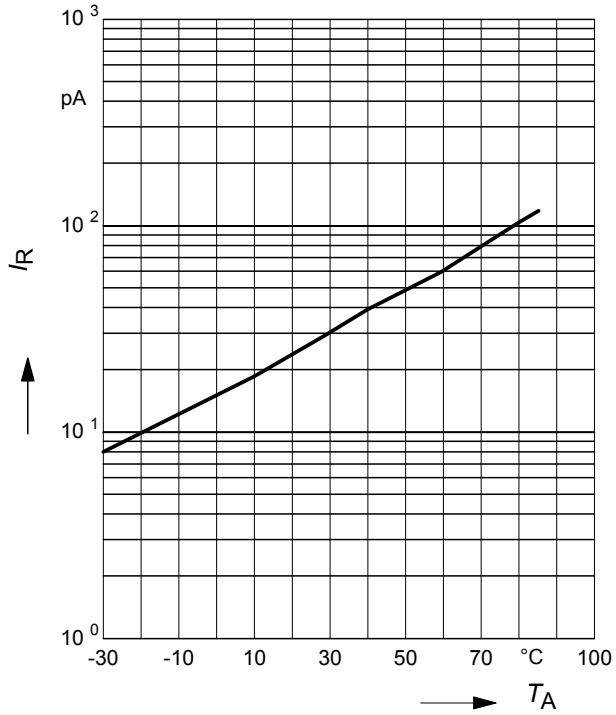
Normalized diode capacitance

$C_{(TA)}/C_{(25°C)} = f(T_A)$; f = 1MHz



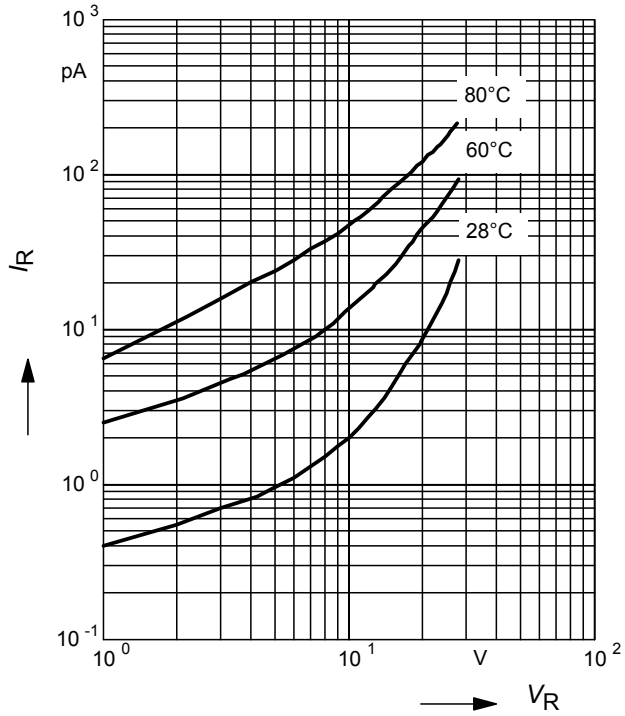
Reverse current $I_R = f(T_A)$

V_R = 28V

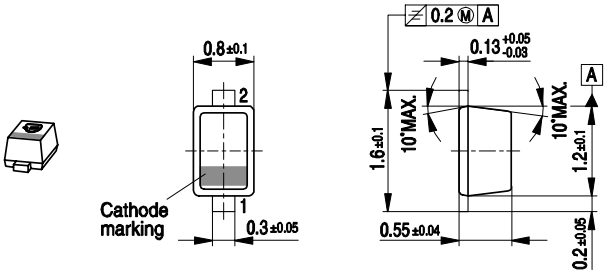


Reverse current $I_R = f(V_R)$

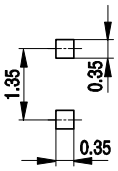
T_A = Parameter



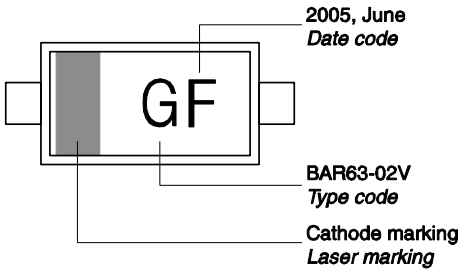
Package Outline



Foot Print

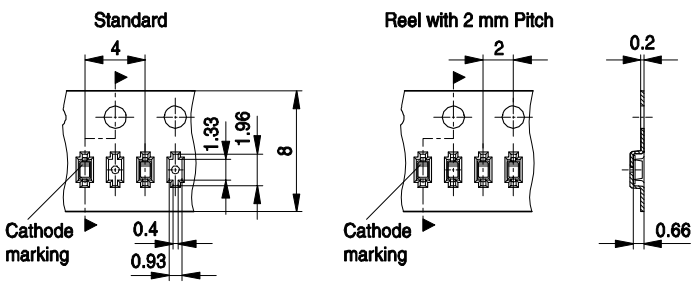


Marking Layout (Example)

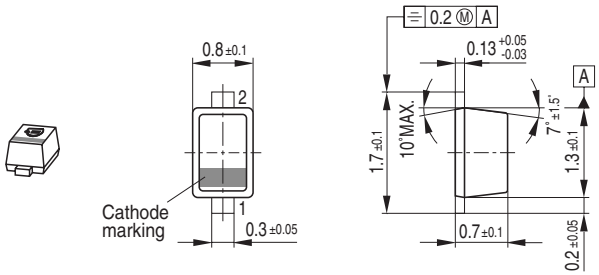


Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel
Reel ø180 mm = 8.000 Pieces/Reel (2 mm Pitch)
Reel ø330 mm = 10.000 Pieces/Reel



Package Outline



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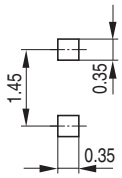

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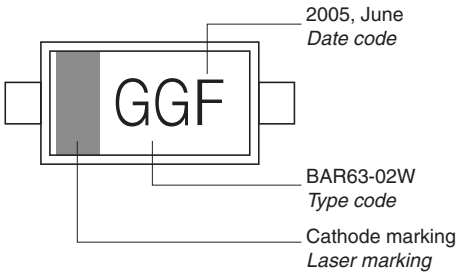

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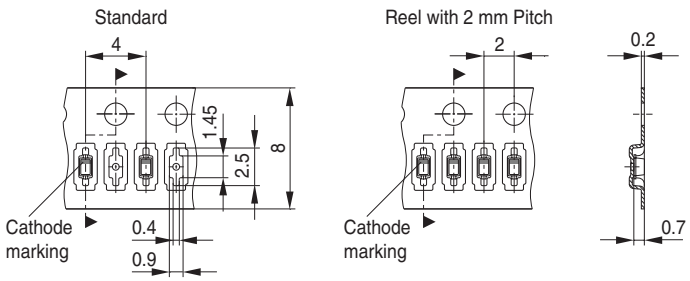
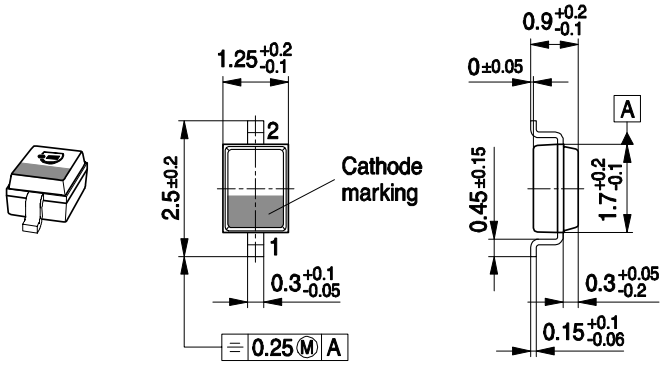


Date Code marking for discrete packages with one digit (SCD80, SC79, SC75[1]) CES-Code

Month	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014
01	a	p	A	P	a	p	A	P	a	p	A	P
02	b	q	B	Q	b	q	B	Q	b	q	B	Q
03	c	r	C	R	c	r	C	R	c	r	C	R
04	d	s	D	S	d	s	D	S	d	s	D	S
05	e	t	E	T	e	t	E	T	e	t	E	T
06	f	u	F	U	f	u	F	U	f	u	F	U
07	g	v	G	V	g	v	G	V	g	v	G	V
08	h	x	H	X	h	x	H	X	h	x	H	X
09	j	y	J	Y	j	y	J	Y	j	y	J	Y
10	k	z	K	Z	k	z	K	Z	k	z	K	Z
11	l	2	L	4	l	2	L	4	l	2	L	4
12	n	3	N	5	n	3	N	5	n	3	N	5

1) New Marking Layout for SC75, implemented at October 2005.

Package Outline



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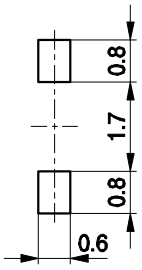
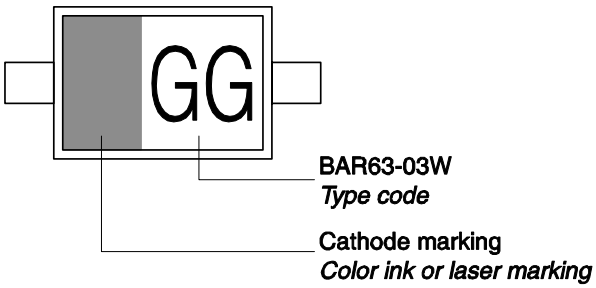


Marking Layout (Example)



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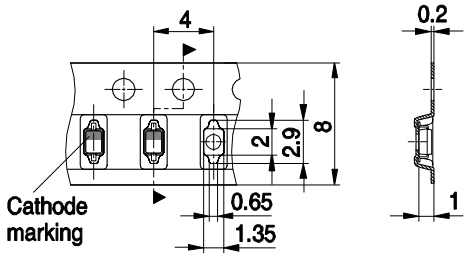

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