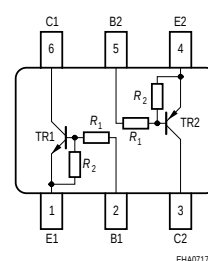
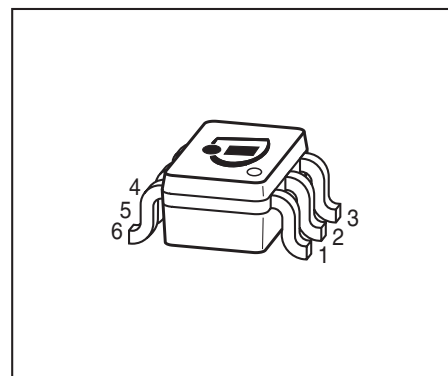


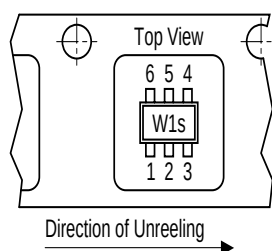
NPN/PNP Silicon Digital Transistor Array

- Switching circuit, inverter, interface circuit, driver circuit
- Two (galvanic) internal isolated NPN/PNP Transistors in one package
- Built in bias resistor NPN and PNP ($R_1=2.2\text{ k}\Omega$, $R_2=47\text{ k}\Omega$)
- Pb-free (RoHS compliant) package
- Qualified according AEC Q101



EHA07176

Tape loading orientation



Marking on SOT-363 package
(for example W1s)
corresponds to pin 1 of device

Position in tape: pin 1
opposite of feed hole side

EHA07193

Type	Marking	Pin Configuration						Package
BCR08PN	WFs	1=E1	2=B1	3=C2	4=E2	5=B2	6=C1	SOT363

Maximum Ratings for NPN and PNP Types

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CEO}	50	V
Collector-base voltage	V_{CBO}	50	
Input forward voltage	$V_{i(fwd)}$	20	
Input reverse voltage	$V_{i(rev)}$	5	
DC collector current	I_C	100	mA
Total power dissipation, $T_S = 115\text{ }^{\circ}\text{C}$	P_{tot}	250	mW
Junction temperature	T_j	150	$^{\circ}\text{C}$
Storage temperature	T_{stg}	-65 ... 150	

Thermal Resistance

Junction - soldering point ¹⁾	R_{thJS}	≤ 140	K/W
--	------------	------------	-----

¹⁾For calculation of R_{thJA} please refer to Application Note AN077 (Thermal Resistance Calculation)

Electrical Characteristics at $T_A=25^{\circ}\text{C}$, unless otherwise specified

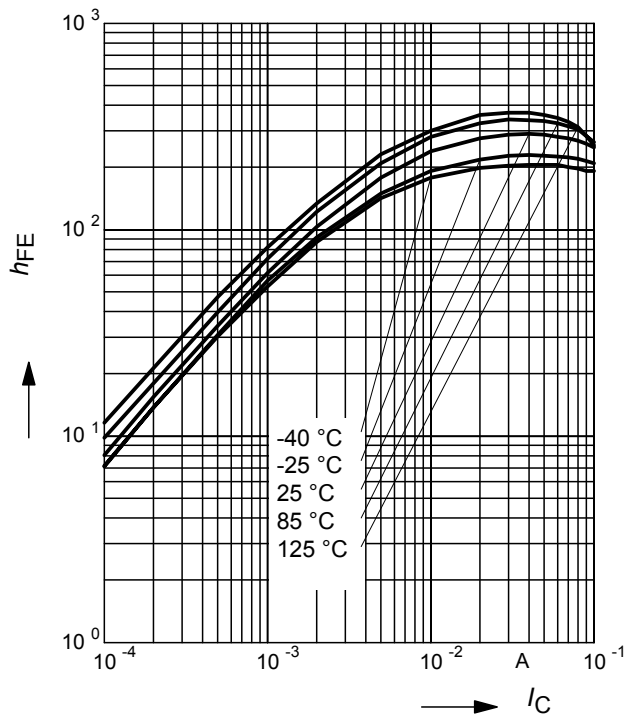
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics for NPN and PNP Types					
Collector-emitter breakdown voltage $I_C = 100\text{ }\mu\text{A}$, $I_B = 0$	$V_{(BR)CEO}$	50	-	-	V
Collector-base breakdown voltage $I_C = 10\text{ }\mu\text{A}$, $I_E = 0$	$V_{(BR)CBO}$	50	-	-	
Collector cutoff current $V_{CB} = 40\text{ V}$, $I_E = 0$	I_{CBO}	-	-	100	nA
Emitter cutoff current $V_{EB} = 5\text{ V}$, $I_C = 0$	I_{EBO}	-	-	164	μA
DC current gain 1) $I_C = 5\text{ mA}$, $V_{CE} = 5\text{ V}$	h_{FE}	70	-	-	-
Collector-emitter saturation voltage1) $I_C = 10\text{ mA}$, $I_B = 0.5\text{ mA}$	V_{CEsat}	-	-	0.3	V
Input off voltage $I_C = 100\text{ }\mu\text{A}$, $V_{CE} = 5\text{ V}$	$V_{i(off)}$	0.4	-	0.8	
Input on Voltage $I_C = 2\text{ mA}$, $V_{CE} = 0.3\text{ V}$	$V_{i(on)}$	0.5	-	1.1	
Input resistor	R_1	1.5	2.2	2.9	k Ω
Resistor ratio	R_1/R_2	0.042	0.047	0.052	-
AC Characteristics for NPN and PNP Types					
Transition frequency $I_C = 10\text{ mA}$, $V_{CE} = 5\text{ V}$, $f = 100\text{ MHz}$	f_T	-	170	-	MHz
Collector-base capacitance $V_{CB} = 10\text{ V}$, $f = 1\text{ MHz}$	C_{cb}	-	2	-	pF

1) Pulse test: $t < 300\mu\text{s}$; $D < 2\%$

NPN Type

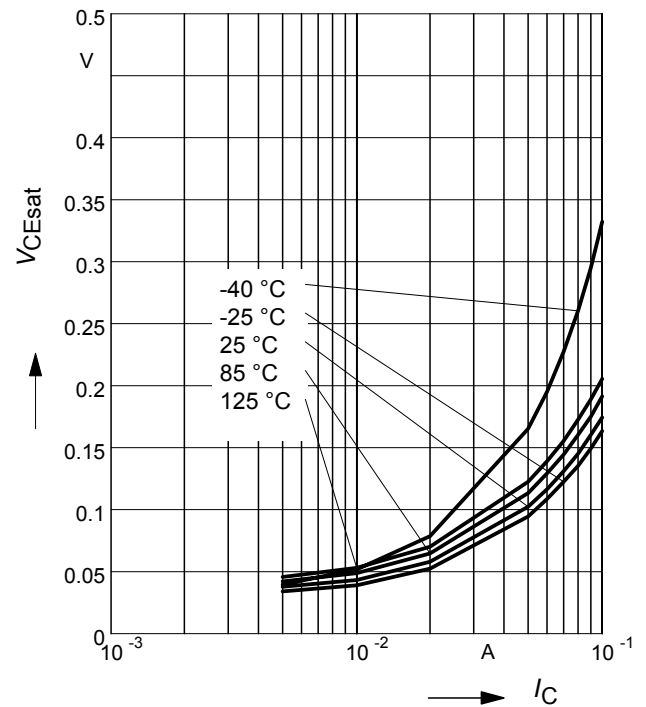
DC Current Gain $h_{FE} = f(I_C)$

$V_{CE} = 5V$ (common emitter configuration)



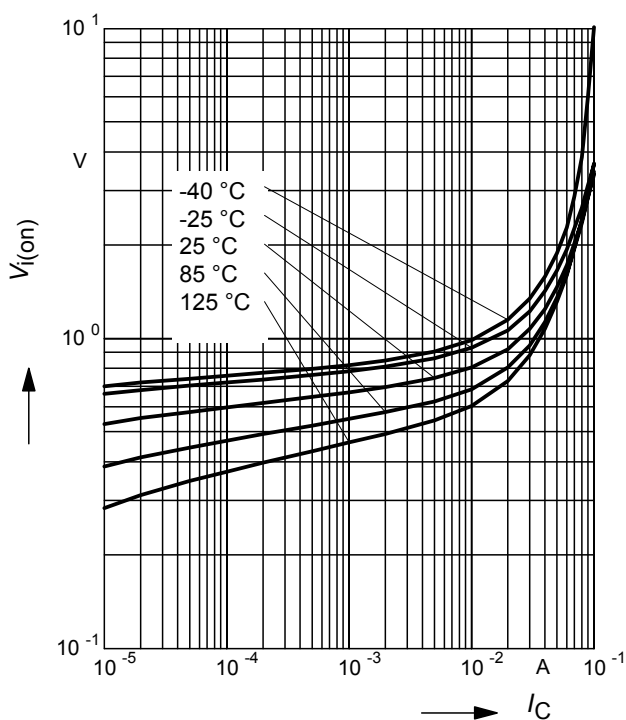
Collector-Emitter Saturation Voltage

$V_{CEsat} = f(I_C)$, $I_C/I_B = 20$



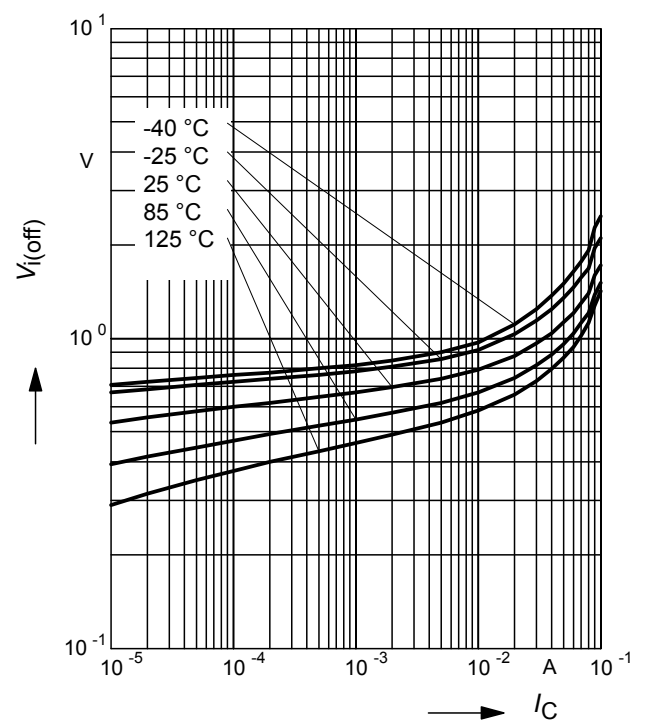
Input on Voltage $V_{i(on)} = f(I_C)$

$V_{CE} = 0.3V$ (common emitter configuration)



Input off voltage $V_{i(off)} = f(I_C)$

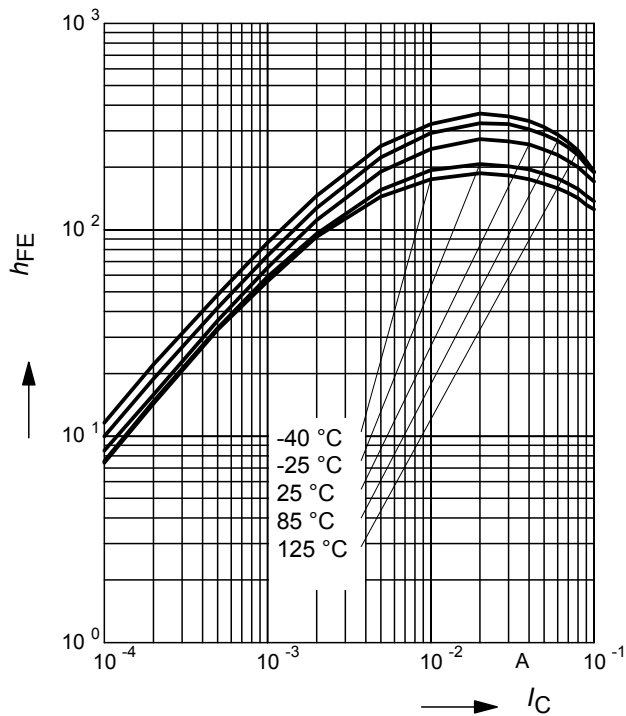
$V_{CE} = 5V$ (common emitter configuration)



PNP Type

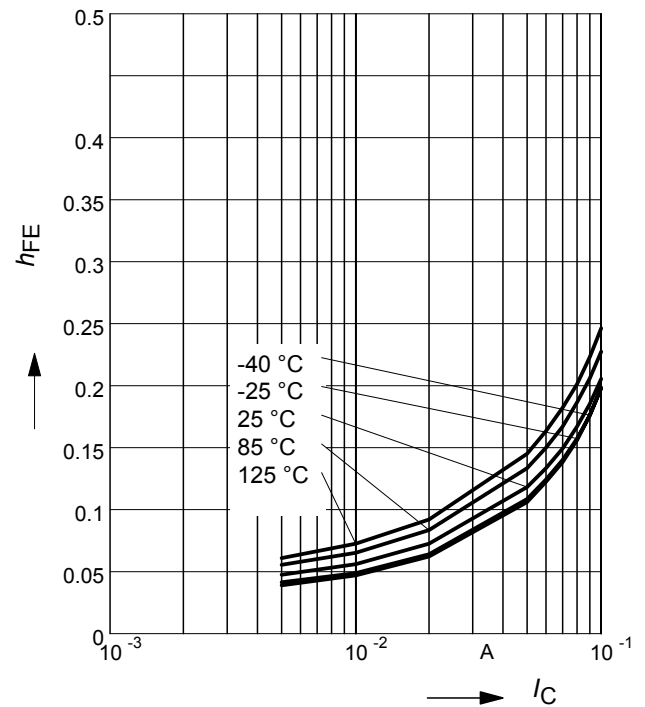
DC Current Gain $h_{FE} = f(I_C)$

$V_{CE} = 5V$ (common emitter configuration)



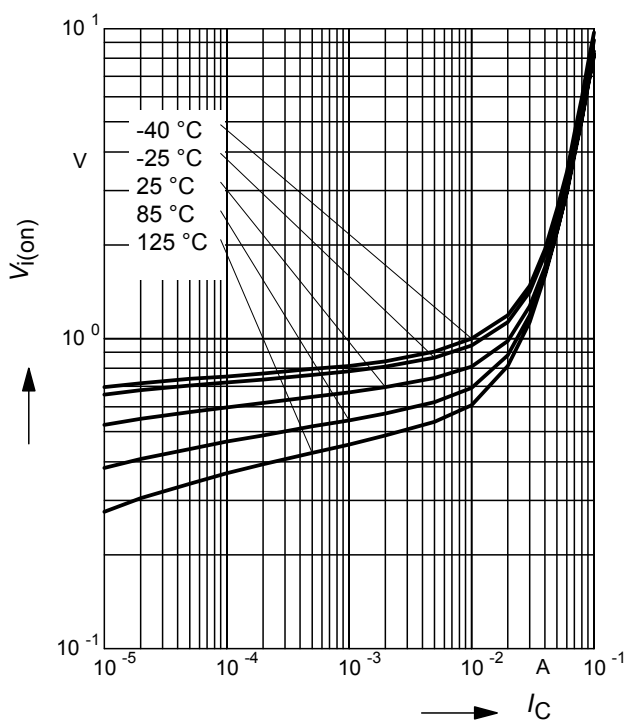
Collector-Emitter Saturation Voltage

$V_{CEsat} = f(I_C)$, $I_C/I_B = 20$



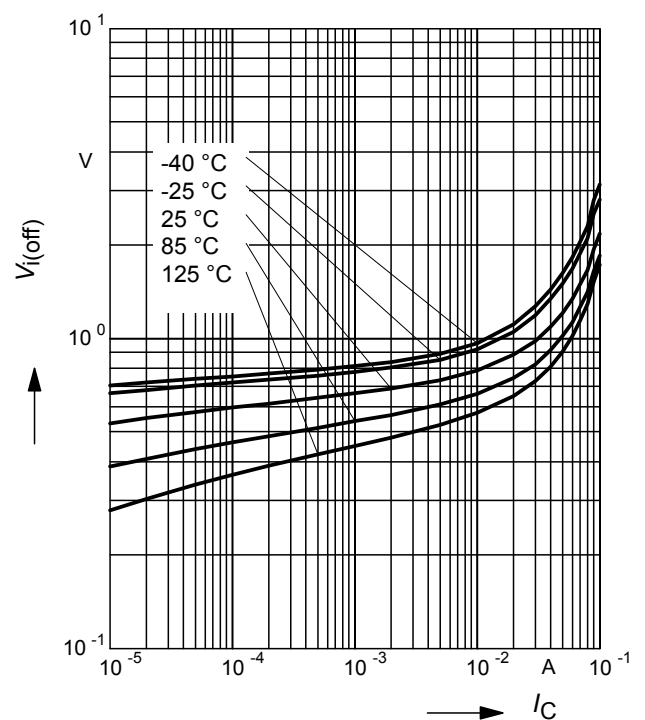
Input on Voltage $V_{i(on)} = f(I_C)$

$V_{CE} = 0.3V$ (common emitter configuration)

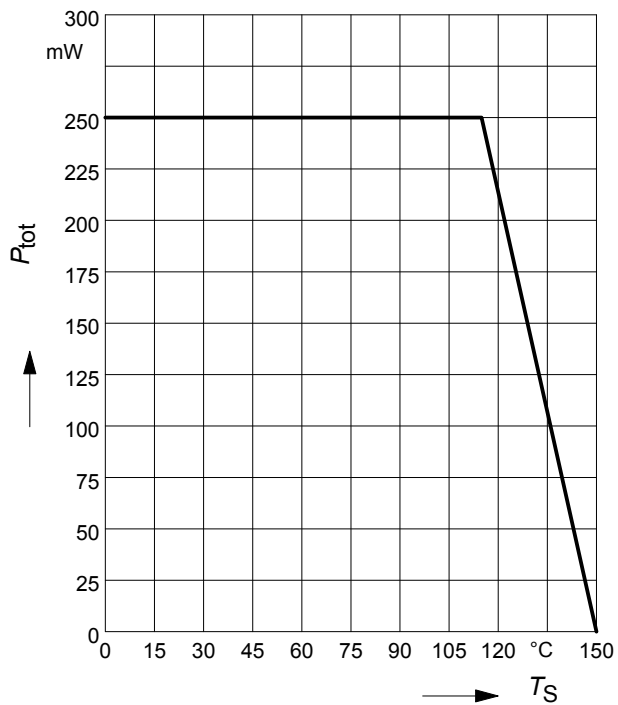


Input off voltage $V_{i(off)} = f(I_C)$

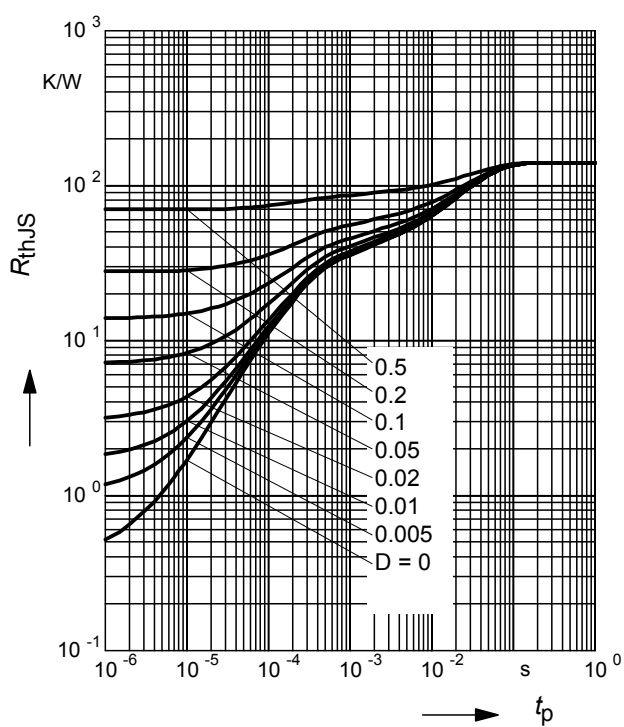
$V_{CE} = 5V$ (common emitter configuration)



Total power dissipation $P_{\text{tot}} = f(T_S)$

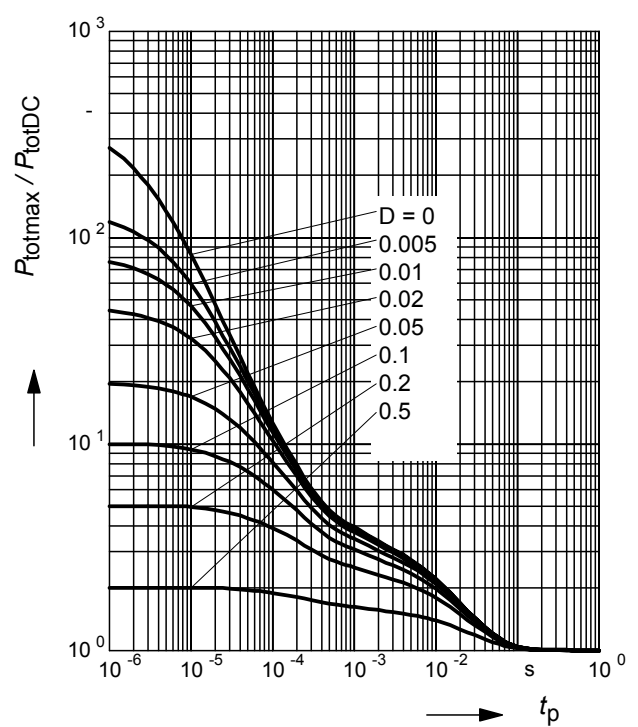


Permissible Pulse Load $R_{\text{thJS}} = f(t_p)$

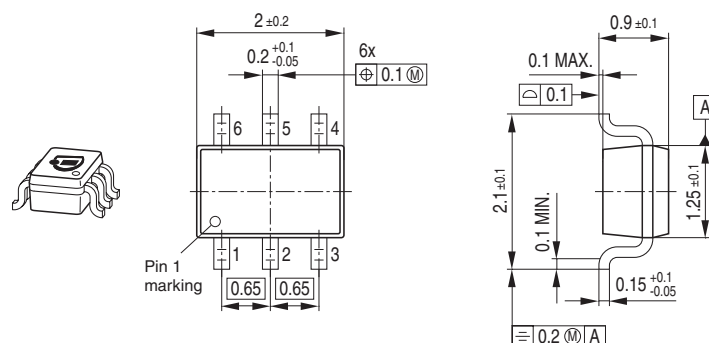


Permissible Pulse Load

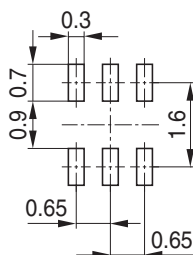
$P_{\text{totmax}} / P_{\text{totDC}} = f(t_p)$



Package Outline

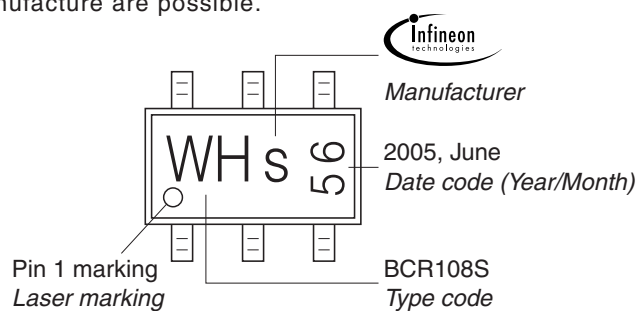


Foot Print



Marking Layout (Example)

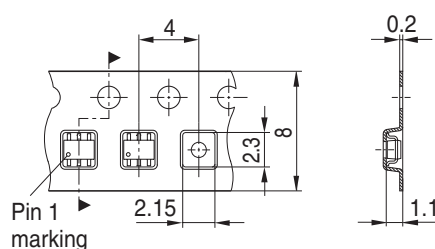
Small variations in positioning of Date code, Type code and Manufacture are possible.



Standard Packing

Reel $\varnothing 180$ mm = 3.000 Pieces/Reel
Reel $\varnothing 330$ mm = 10.000 Pieces/Reel

For symmetric types no defined Pin 1 orientation in reel.



Edition 2009-11-16

**Published by
Infineon Technologies AG
81726 Munich, Germany**

**© 2009 Infineon Technologies AG
All Rights Reserved.**

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office ([<www.infineon.com>](http://www.infineon.com)).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.