TWO-CELL, THREE-CELL, AND FOUR-CELL LITHIUM-ION OR LITHIUM-POLYMER BATTERY PROTECTION AFE

FEATURES

- **2-, 3-, or 4-Cell Series Protection Control**
- **Can Directly Interface With the bq2084 Gas Gauges**
- **Provides Individual Cell Voltages and Battery Voltage to Battery Management Host**
- **Integrated Cell Balancing Drive**
- **I²C Compatible User Interface Allows Access to Battery Information**
- **Programmable Threshold and Delay for Overload and Short Circuit During Charge and Discharge**
- **System Alert Interrupt Output**
- **Host Control Can Initiate Sleep Power Mode and Ship Mode**
- **Integrated 3.3-V, 25-mA LDO**
- **Supply Voltage Range From 4.5 V to 25 V**
- **Low Supply Current of 60-µA Typical**
- **bq29312A is 100% specification compatible with the bq29312**

APPLICATIONS

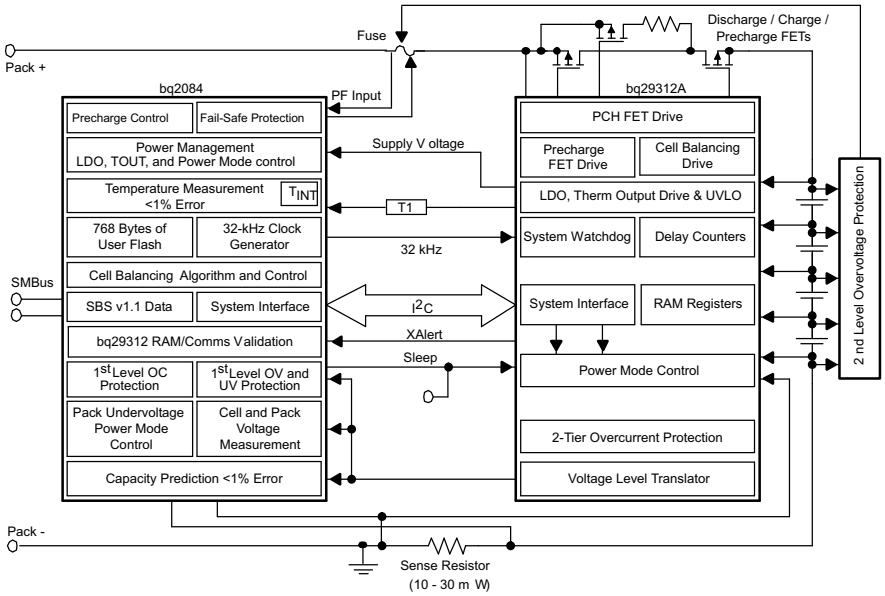
- **Notebook PCs**
- **Medical and Test Equipment**
- **Portable Instrumentation**

DESCRIPTION

The bq29312A is a 2-, 3-, or 4-cell lithium-ion battery pack protection analog front end (AFE) IC that incorporates a 3.3-V, 25-mA low-dropout regulator (LDO). The bq29312A also integrates an I²C compatible interface to extract battery parameters such as cell voltages and control output status. Other parameters such as current protection thresholds and delays can be programmed into the bq29312A to increase the flexibility of the battery management system.

The bq29312A provides safety protection for overcharge, overload, short-circuit, overvoltage, and undervoltage conditions with the battery management host. In overload and short-circuit conditions, the bq29312A turns the FET drive off autonomously dependant on the internal configuration setting.

SYSTEM PARTITIONING DIAGRAM



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (Continued)

The communications interface allows the host to observe and control the current status of the bq29312A. It enables cell balancing, enters different power modes, sets overload levels, sets the overload blanking delay time, sets short-circuit threshold levels for charge and discharge, and sets the short-circuit blanking delay time.

Cell balancing of each cell is performed via a cell bypass path, which is enabled via the internal control register accessible via the I^2C compatible interface. The maximum bypass current is set via an external series resistor and internal FET on resistance (typical 400 Ω).

ORDERING INFORMATION(1)

T_A	PACKAGED	
	TSSOP (PW)(2)	QFN (RTH) (3)
–40°C to 85°C	bq29312APWR-SA	bq29312ARTH

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) The bq29312A can be ordered in tape and reel by adding the suffix R to the orderable part number, ie: bq29312APWR bq29312ARTHR.
(3) The QFN package is also made available in mini reel, add suffix T to the orderable part number, ie: bq29312ARTHT.

PACKAGE DISSIPATION RATINGS

PACKAGE	POWER RATING $T_A \le 25°C$	DERATING FACTOR ABOVE $T_A \le 25°C$	POWER RATING	
			$T_A \le 70°C$	$T_A = 85°C$
PW	874 mW	6.99 W/°C	559 mW	454 mW

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)(2)

			bq29312A
V_{CC}	Supply voltage range	PACK, BAT	–0.3 V to 34 V
V_I	Input voltage range	VC1, VC2, VC3, VC4	–0.3 V to 34 V
		SR1, SR2	–1.0 V to 1.0 V
		VC5	–1.0 V to 4.0 V
		VC1 to VC2, VC2 to VC3, VC3 to VC4, VC4 to VC5	–0.3 to 8.5 V
		WDI, SLEEP, SCLK, SDATA	–0.3 to 8.5 V
		ZVCHG	–0.3 V to 34 V
V_O	Output voltage range	DSG, CHG	–0.3 V to BAT
		OD	–0.3 V to 34 V
		PMS	–0.3 V to PACK–0.2 V
		TOUT, SCLK, SDATA, CELL, XALERT	–0.3 to 7 V
	Current for cell balancing		10 mA
	Continuous total power dissipation		See Dissipation Rating Table
T_{stg}	Storage temperature range		–65°C to 150°C
	Lead temperature (soldering, 10 s)		300°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground of this device except VCn–VC(n+1), where n = 1-, 2-, 3-, 4-cell voltage.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
	Supply Voltage (BAT or PACK)		4.5(1)		25	V
$V_{I(STARTUP)}$	Start-up voltage (PACK)		5.0			V
V_I	Input voltage range	VC1, VC2, VC3, VC4	0		BAT	V
		SR1, SR2	–0.5		0.5	
		VC5	–0.5		3.0	
		VCn – VC(n+1), (n = 1, 2, 3, 4)	0		5.0	
		PMS	0		PACK	
		SLEEP	0		REG	
V_{IH}	Logic level input voltage	SCLK, SDATA, WDI	0.8 × REG		REG	V
V_{IL}			0		0.2 × REG	
V_{IH}	PMS logic level	PMS	$V_{(PACK)}$ – 0.2		$V_{(PACK)}$	V
V_{IL}			0		0.2	
	PMS pullup/pulldown resistance	RPMS	100		1000	kΩ
V_O	Output voltage	OD			25	V
I_O	Output current	XALERT, SDATA			200	µA
I_I	Input current, External 3.3-V REG capacitor	CELL			±10	µA
		SLEEP	-0.5		1.0	µA
		$C_{(REG)}$	4.7			µF
	Extend CELL output filter	$R_{(CELL)}$		100		Ω
		$C_{(CELL)}$		100		nF
I_{OL}	Input frequency	OD			1	mA
		WDI		32.768		kHz
	WDI high time		2		28	µs
T_A	Operating temperature		–40		85	°C

(1) $V_{(PACK)}$ supply voltage must rise above start-up voltage on power up to enable the internal regulator which drives REG and TOUT as required. Once $V_{(PACK)}$ is above the start-up voltage, it can fall down to the minimum supply voltage and still meet the specifications of the bq29312A.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, $C_{(REG)}$ = 4.7 µF, BAT = 14 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	Supply current 1	No load at REG, TOUT, XALERT, SCLK, and SDATA. ZVCHG = off ,VMEN = on, WDI no clock, Select VC5 = VC4 = 0 V			60	90	µA
			T_A = –25°C to 85°C			100	
I_{CC2}	Supply current 2(Depends of VM topology selected)	No load at REG, TOUT, XALERT, SCLK, and SDATA. ZVCHG = off, VMEN = off, WDI no clock	T_A = –25°C to 85°C		25	50	µA
$I_{(SLEEP)}$	Sleep current	No load at REG, TOUT, XALERT, SCLK, and SDATA.CHG, DSG and ZVCHG = off, REG = on, VMEN = off, WDI no clock, SLEEP = REG or OPEN	T_A = –25°C to 85°C		20	40	µA
$I_{(SHIP)}$	Ship current	REG, CHG, DSG and ZVCHG = off, REG = off, VMEN = off, WDI no clock, VPACK= 0 V	T_A = –25°C to 85°C		0.1	1.0	µA
3.3 V LDO							
$V_{(REG)}$	Regulator output voltage	8.0 V < BAT or PACK ≤ 25 V, I_{OUT} ≤ 25 mA	T_A = –25°C to 85°C	–4%	3.3	2%	V
		6.5 V < BAT or PACK ≤ 8 V, I_{OUT} ≤ 25 mA		–9%	3.3	2%	
		5.4 V ≤ BATor PACK ≤ 6.5 V, I_O ≤ 16 mA		–9%	3.3	2%	V
		4.5 V ≤ BAT or PACK ≤ 25 V, I_O ≤ 2 mA		–2%	3.3	2%	V
$\Delta V_{(EGTEMP)}$	Regulator output change with temperature	5.4 V ≤ BAT ≤ 25 V, I_O = 2 mA,	T_A = –25°C to 85°C		±0.2%		
$\Delta V_{(REGLINE)}$	Line regulation	5.4 V ≤ BAT or PACK ≤ 25 V, I_O = 2 mA			10	20	mV
$\Delta V_{(REGLOAD)}$	Load regulation	BAT = 14 V, 0.2 mA ≤ I_O ≤ 2 mA			7	15	mV
		BAT = 14 V, 0.2 mA ≤ I_O ≤ 25 mA			40	100	
I_{MAX}	Current limit	BAT = 14 V, REG = 3 V		25		100	mA
		BAT = 14 V, REG = 0 V		12		50	
CELL VOLTAGE MONITOR							
$V_{(CELL\ OUT)}$	CELL output	$V_{(Cn)} – V_{(Cn + 1)}$ = 0 V, 8 V ≤ BAT or PACK ≤ 25 V			0.975		V
		$V_{(Cn)} – V_{(Cn + 1)}$ = 4.5 V, 8 V ≤ BAT or PACK ≤ 25 V			0.3		
REF	CELL output	Mode(1), 8 V ≤ BAT or PACK ≤ 25 V		–1%	0.975	1%	V
PACK	CELL output	Mode(2)		–5%	PACK/ 25	5%	V
K	CELL scale factor	K = (CELL output (VC5 = 0 V, VC4 = 4.5 V) –CELL output (VC5 = VC4 = 0 V)/ 4.5		0.147	0.150	0.153	
		K = (CELL output (VC2 = 13.5 V, VC1 = 18 V) –CELL output (VC2 = VC1 = 13.5 V)/ 4.5		0.147	0.150	0.153	
VICR	CELL output offset error	CELL output (VC2 = 17 V, VC1 = 17 V) CELL output (VC2 = VC1 = 0 V)			–1		mV
$R_{(BAL)}$	Cell balance internal resistance	$rds_{(ON)}$ for internal FET switch at V_{DS} = 2 V		200	400	800	Ω

(1) Register Address =0x04, b2(CAL0) = b3(CAL1) = 1, Register Address = 0x03, b0(VMEN) = 1
(2) Register Address = 0x03, b1(PACKOUT) = 1, b0(VMEN) = 1

ELECTRICAL CHARACTERISTICS (Continued)

T_A = 25°C, $C_{(REG)}$ = 4.7 µF, BAT = 14 V (unless otherwise noted)

PARAMETER		TEST CONDITION		MIN	NOM	MAX	UNIT
OVERLOAD (OL) AND SHORT-CIRCUIT (SC) DETECTION							
V_{OL}	OL detection threshold range, typical(1)			–50		–205	mV
ΔV_{OL}	OL detection threshold program step				5		mV
$V_{HYS(OL)}$	OL detection threshold hysteresis			7	10	13	mV
$V_{(SC)}$	SC detection threshold range, typical(2)	Charge		100		475	mV
		Discharge		–100		–475	
$\Delta V_{(SC)}$	SC detection threshold program step	Charge			25		mV
		Discharge			–25		
$V_{HYS(SC)}$	SC detection threshold hysteresis	Charge and Discharge		40	50	60	mV
$V_{(OL_acr)}$	OL detection threshold accuracy(1)	Discharge	V_{OL} = 50 mV (min)	40	50	60	mV
			V_{OL} = 100 mV	90	100	110	
			V_{OL} = 205 mV (max)	184	205	226	
$V_{(SC_acr)}$	SC detection threshold accuracy(2)	Charge and Discharge	V_{SC} = 100 mV (min)	80	100	120	mV
			V_{SC} = 200 mV	180	200	220	
			V_{SC} = 475 mV (max)	426	475	523	
FET DRIVE CIRCUIT							
$V_{(FETON)}$	Output voltage, charge, and discharge FETs on	$V_{(FETOND)}$= $V_{(BAT)}$– $V_{(DSG)}$VGS connect 1 MΩ	BAT= 20 V	12	15	18	V
		$V_{(FETONC)}$=$V_{(PACK)}$– $V_{(CHG)}$VGS connect 1 MΩ	PACK = 20 V	12	15	18	
$V_{(ZCHG)}$	ZVCHG clamp voltage		PACK= 4.5 V	3.3	3.5	3.7	V
$V_{(FETOFF)}$	Output voltage, charge and discharge FETs off	$V_{(FETOFF)}$= $V_{(PACK)}$– $V_{(DSG)}$	PACK= 16 V			0.2	V
		$V_{(FETOFF)}$=$V_{(BAT)}$– $V_{(CHG)}$	BAT = 16 V			0.2	
t_r	Rise time	C_L = 4700 pF	V_{DSG} :10%–90%		40	200	µs
			V_{CHG} :10%–90%		40	200	
t_f	Fall time	C_L = 4700 pF	V_{DSG} :90%–10%		40	200	µs
			V_{CHG} :90%–10%		40	200	
THERMISTOR DRIVE							
$r_{DS(on)}$	TOUT pass-element series resistance	I_O = –1 mA at TOUT pin, $rds_{(ON)}$ = (V_{REG}– V_O (TOUT))/1 mA, T_A = –25°C to 85°C			50	100	Ω
LOGIC							
$R_{(PUP)}$	Internal pullup resistance	XALERT	T_A = –25°C to 85°C	60	100	200	kΩ
		SDATA, SCLK,	T_A = –25°C to 85°C	6	10	20	
V_{OL}	Logic level output voltage	XALERT, I_O = 200 µA,	T_A = –25°C to 85°C			0.2	V
		SDATA, I_O = 50 µA,	T_A = –25°C to 85°C			0.4	
		OD I_O=1 mA,	T_A = –25°C to 85°C			0.6	

(1) See OL register for setting detection threshold
(2) See SC register for setting detection threshold

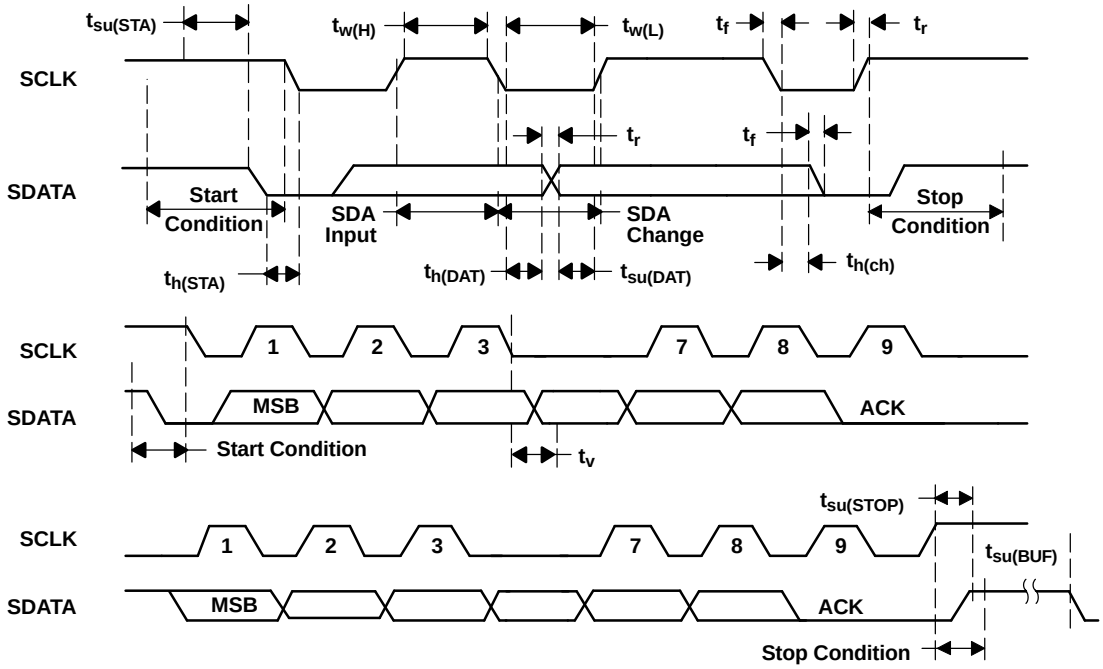
AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, $C_{(REG)}$ = 4.7 µF, BAT = 14 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
$t_{(WDTINT)}$	WDT start-up detect time		250	700	2000	ms
$t_{(WDWT)}$	WDT detect time			100		µs

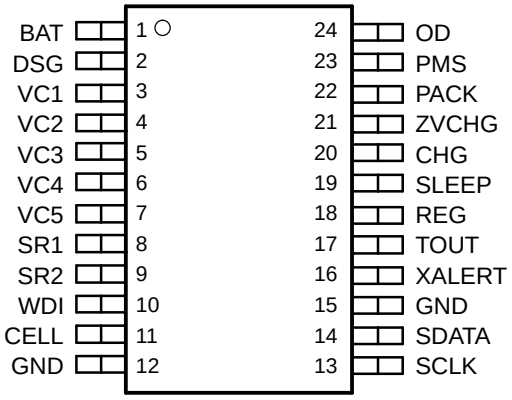
AC TIMING SPECIFICATIONS (I^2C COMPATIBLE SERIAL INTERFACE)

PARAMETER		MIN	MAX	UNIT
t_r	SCLK SDATA rise time		1000	ns
t_f	SCLK SDAT fall time		300	ns
$t_{w(H)}$	SCLK pulse width high	4.0		µs
$t_{w(L)}$	SCLK pulse width low	4.7		µs
$t_{su(STA)}$	Setup time for START condition	4.7		µs
$t_{h(STA)}$	START condition hold time after which first clock pulse is generated	4.0		µs
$t_{su(DAT)}$	Data setup time	250		ns
$t_{h(DAT)}$	Data hold time	0		µs
$t_{su(STOP)}$	Setup time for STOP condition	4.0		µs
$t_{su(BUF)}$	Time the bus must be free before new transmission can start	4.7		µs
t_V	Clock low to data out valid		900	ns
$t_{h(CH)}$	Data out hold time after clock low	0		ns
f_{SCL}	Clock frequency	0	100	kHz

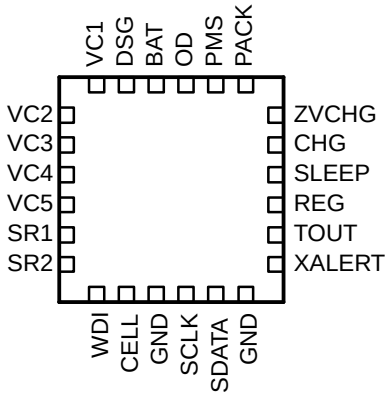


PIN ASSIGNMENTS

PW PACKAGE
(TOP VIEW)



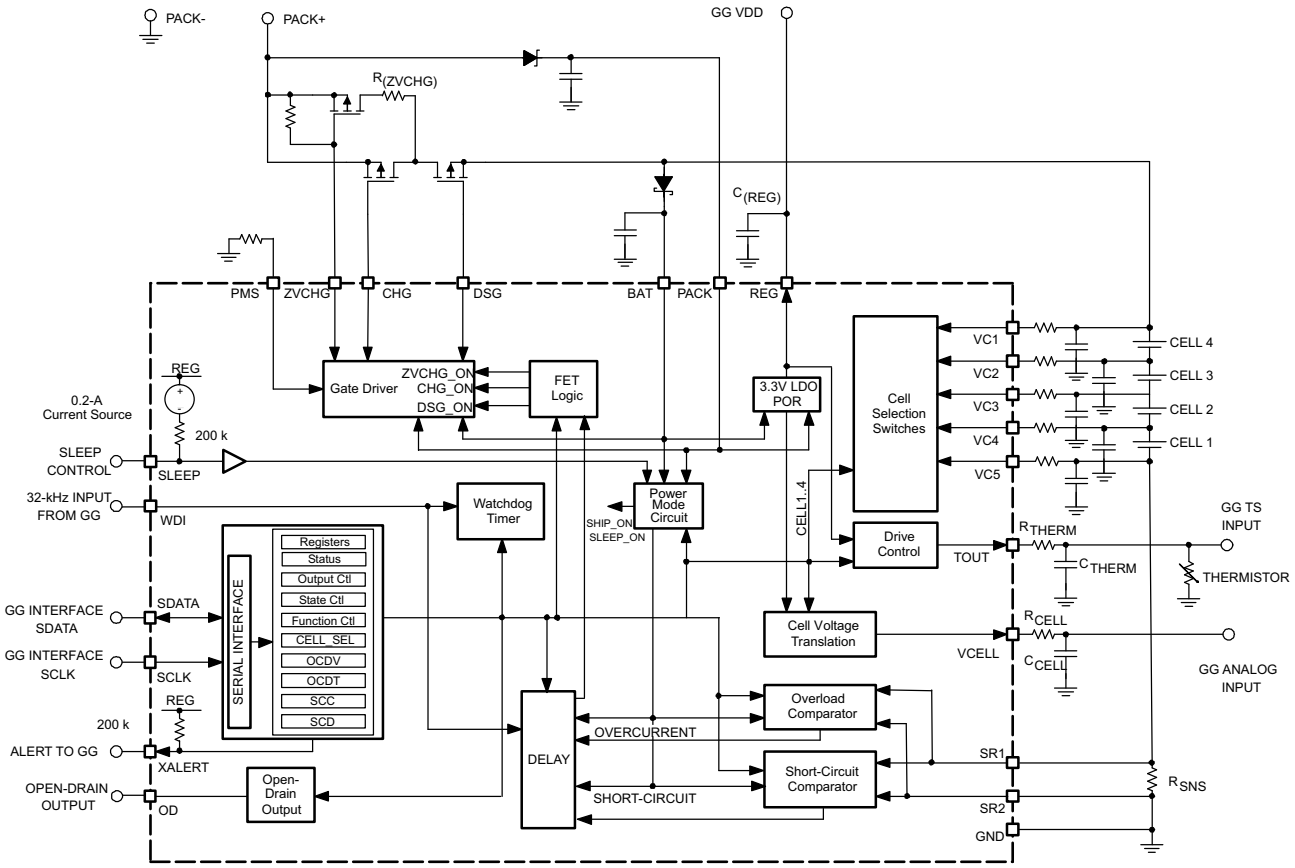
RTH PACKAGE
(TOP VIEW)



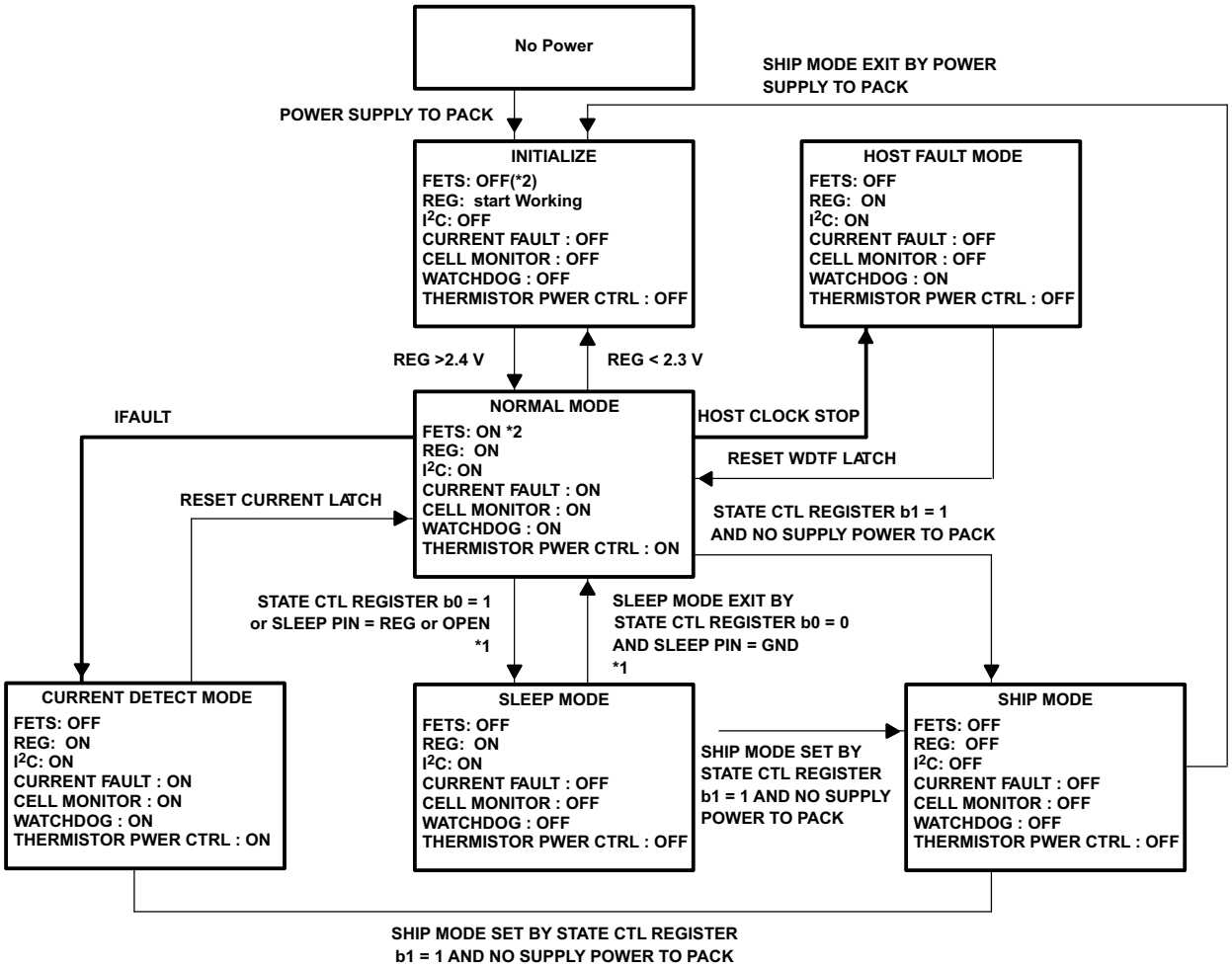
Terminal Functions

TERMINAL			DESCRIPTION
NAME	PIN NO.		
	RTH	PW	
BAT	22	1	Diode protected BAT+ terminal and primary power source.
DSG	23	2	Push-pull output discharge FET gate drive
VC1	24	3	Sense voltage input terminal for most-positive cell and balance current input for most-positive cell.
VC2	1	4	Sense voltage input terminal for second most-positive cell, balance current input for second most-positive cell and return balance current for most-positive cell.
VC3	2	5	Sense voltage input terminal for third most-positive cell, balance current input for third most-positive cell and return balance current for second most-positive cell.
VC4	3	6	Sense voltage input terminal for least-positive cell, balance current input for least-positive cell and return balance current for third most-positive cell.
VC5	4	7	Sense voltage input terminal for most-negative cell, return balance current for least-positive cell.
SR1	5	8	Current sense positive terminal when charging relative to SR2
SR2	6	9	Current sense negative terminal when discharging relative to SR2 current sense terminal
WDI	7	10	Digital input that provides the timing clock for the OC and SC delays and also acts as the watchdog clock.
CELL	8	11	Output of scaled value of the measured cell voltage.
GND	9	12	Analog ground pin and negative pack terminal
SCLK	10	13	Open-drain bidirectional serial interface clock with internal 10-kΩ pullup to $V_{(REG)}$.
SDATA	11	14	Open-drain bidirectional serial interface data with internal 10-kΩ pullup to $V_{(REG)}$.
GND	12	15	Connect to GND
XALERT	13	16	Open-drain output used to indicate status register changes. With internal 100-kΩ pullup to $V_{(REG)}$
TOUT	14	17	Provides thermistor bias current
REG	15	18	Integrated 3.3-V regulator output
SLEEP	16	19	This pin is pulled up to $V_{(REG)}$ internally, open or H level makes Sleep mode
CHG	17	20	Push-pull output charge FET gate drive
ZVCHG	18	21	The ZVCHG FET drive is connected here
PACK	19	22	PACK positive terminal and alternative power source
PMS	20	23	0-V charge configuration select pin, CHG terminal ON/OFF is determined by this pin.
OD	21	24	NCH FET open-drain output

FUNCTIONAL BLOCK DIAGRAM



STATE DIAGRAM



Interrupt Request When Enrering These States

*1: Interrupt Request is Granted When Only External Sleep Pin Changes

*2: When PMS connect to Pack, Default State of CHG FET is ON.

FUNCTIONAL DESCRIPTION

Low-Dropout Regulator (REG)

The inputs for this regulator can be derived from the battery cell stack (BAT) or the pack positive terminal (PACK). The output is typically 3.3 V with the minimum output capacitance for stable operation is 4.7 µF and is also internally current limited. During normal operation, the regulator limits output current to typically 50 mA.

Initialization

The bq29312A internal control circuit is powered by the REG voltage, which it also monitors. When the voltage at REG falls below 2.3 V, the internal circuit turns off the FETs and disables all controllable functions, including the REG and TOUT outputs. REG does not start up unless a voltage above $V_{(STARTUP)}$ is supplied to the PACK terminal. After the regulator has started, based on PACK voltage, it keeps operating through the BAT input, even if the PACK voltage is removed. If the BAT input is below the minimum operating range, then the bq29312A does not operate if the supply to the PACK input is removed. After start up, when the REG voltage is above 2.4 V, the bq29312A is in Normal mode.

The initial state of the CHG output depends on the PMS input. If PMS = PACK, then CHG = ON, however, if PMS = GND, then CHG = OFF.

Overload Detection

The overload detection is used to detect abnormal currents in the discharge direction. This feature is used to protect the pass FETs, cells and any other inline components from excessive current conditions. The detection circuit also incorporates a blanking delay before driving the control for the pass FETs to the OFF state. The overload sense voltage is set in the OLV register, and delay time is set in the OLT register. The overload threshold can be programmed from 50 mV to 205 mV in 5-mV steps with the default being 50 mV and hysteresis of 10 mV.

Short-Circuit Detection

The short current circuit detection is used to detect abnormal current in either the charge or discharge direction. This safety feature is used to protect the pass FETs, cells, and any other inline components from excessive current conditions. The detection circuit also incorporates a blanking delay before driving the control for the pass FETs to the OFF state. The short-circuit thresholds and delay time are set in the SCC and SCD registers, respectively, where SCC is for charging and SCD is for discharge. The short-circuit threshold can be programmed from 100 mV to 475 mV in 25-mV steps with the default being 100 mV and hysteresis of 50 mV.

Overload and Short-Circuit Delay

The overload delay (default =1 ms) allows the system to momentarily accept a high current condition without disconnecting the supply to the load. The delay time can be increased via the OLT register, which can be programmed for a range of 1 ms to 31 ms with steps of 2 ms.

The short-circuit delay (default = 0 µs) is programmable in the SCC and SCD registers. This register can be programmed from 0 µs to 915 µs with steps of 61 µs.

Overload and Short-Circuit Response

When an overload or short-circuit fault is detected, the FETs are turned off. The STATUS (b0…b2) register reports the details of short-circuit (charge), short-circuit (discharge), and overload. The respective STATUS (b0…b2) bits are set to 1 and the XALERT output is triggered. This condition is latched until the CONTROL (b0) is set and then reset. If a FET is turned on via resetting CONTROL (b0) and the error condition is still present on the system, then the device reenters the protection response state.

FUNCTIONAL DESCRIPTION (continued)

Cell Voltage

The cell voltage is translated to allow a system host to measure individual series elements of the battery. The series element voltage is translated to a GND-based voltage equal to 0.15 ±0.002 of the series element voltage. This provides a range from 0 V to 4.5 V. The translation output is inversely proportional to the input using the following equation.

Where, $V_{(CELL\ OUT)} = -K \times V_{(CELL\ IN)} + 0.975$ (V)

Programming CELL_SEL (b1, b0) selects the individual series element. The CELL_SEL (b3, b2) selects the voltage monitor mode, cell monitor, offset, etc.

Calibration of Cell Voltage Monitor Amplifier Gain

The cell voltage monitor amplifier has an offset, and to increase accuracy, this can be calibrated.

There are a couple of methods by calibration circumstance.

The following procedure shows how to measure and calculate the offset and gain as an example.

- **Step 1**
  - Set CAL1=1, CAL0=1, CELL1=0, CELL0=0, VMEN=1
  - V_{REF} is trimmed to 0.975 V within ±1%, measuring V_{REF} eliminates its error.
  - Measure internal reference voltage V_{REF} from VCELL directly.
  - VREF=measured reference voltage
- **Step 2**
  - Set CAL1=0, CAL0=0, CELL1=0, CELL0=1, VMEN=1
  - The output voltage includes the offset and represented by:
    $V_{O(4-5)} = V_{REF} + (1 + K) \times V_{OS}$ (V)
    Where K = CELL Scaling Factor
  - V_{OS} = Offset voltage at input of the internal operational amplifier
- **Step 3**
  - Set CAL1=1, CAL0=0, CELL1=0, CELL0=0, VMEN=1
  - Measuring scaled REF voltage through VCELL amplifier.
  - The output voltage includes the scale factor error and offset and is represented by:
    $V_{(OUTR)} = V_{REF} + (1 + K) \times V_{OS} - K \times V_{REF}$ (V)
- **Step 4**
  - Calculate $(V_{O(4-5)} - V_{(OUTR)})/V_{REF}$
  - The result is the actual scaling factor, $K_{(ACT)}$, and is represented by:
    $K_{(ACT)} = (V_{O(4-5)} - V_{(OUTR)})/V_{REF} = (V_{REF} + (1 + K) \times V_{OS}) - (V_{REF} + (1 + K) \times V_{OS} - K \times V_{REF})/ V_{REF} = K \times V_{REF}/V_{REF} = K$
- **Step 5**
  - Calculate the actual offset value where:
    $V_{OS(ACT)} = (V_{O(4-5)} - V_{REF})/(1 + K_{(ACT)})$
- **Step 6**
  - Calibrated cell voltage is calculated by:
    $VCn - VC(n+1) = \{V_{REF} + (1 + K_{(ACT)}) \times V_{OS(ACT)} - V_{(CELLOUT)}\}/K_{(ACT)} - \{V_{O(4-5)} - V_{(CELLOUT)}\}/K_{(ACT)}$

For improved measurement accuracy, $V_{OS(ACT)}$ for each cell voltage should be measured.

- Set CAL1=0, CAL0=0, CELL1=0, CELL0=1, VMEN=1
- Set CAL1=0, CAL0=0, CELL1=1, CELL0=0, VMEN=1
- Set CAL1=0, CAL0=0, CELL1=1, CELL0=1, VMEN=1

FUNCTIONAL DESCRIPTION (continued)

Measuring $V_{O(3-4)}$, $V_{O(2-3)}$, $V_{O(1-2)}$,

- VC4 – VC5 = {$V_{O(4-5)}$– $V_{(CELLOUT)}$}/ $K_{(ACT)}$
- VC3 – VC4 = {$V_{O(3-4)}$– $V_{(CELLOUT)}$}/ $K_{(ACT)}$
- VC2 – VC3 = {$V_{O(2-3)}$– $V_{(CELLOUT)}$}/ $K_{(ACT)}$
- VC1 – VC2 = {$V_{O(1-2)}$– $V_{(CELLOUT)}$}/ $K_{(ACT)}$

Cell Balance Control

The cell balance control allows a small bypass path to be controlled for any one series element. The purpose of this bypass path is to reduce the current into any one cell during charging to bring the series elements to the same voltage. Series resistors placed between the input pins and the positive series element nodes control the bypass current value. Individual series element selection is made using bits 4 through 7 of the CELL_SEL register.

Thermistor Drive Circuit (TOUT)

The TOUT pin can be enabled to drive a thermistor from REG. The typical thermistor resistance is 10 kΩ at 25°C. The default-state is OFF to conserve power. The maximum output impedance is 100 Ω. TOUT is enabled in FUNCTION CTL register (bit 5).

Open-Drain Drive Circuit (OD)

The open-drain output has 1-mA current source drive with a maximum output voltage of 25 V. The OD output is enabled or disabled by OUTPUT CTL register (bit 4) and has a default state of OFF.

XALERT (XALERT)

XALERT is driven low when an OL or SC current fault is detected, if the SLEEP pin changes state or a watchdog fault occurs. To clear XALERT, toggle (from 0, set to 1 then reset to 0) OUTPUT CTL (bit 0), then read the STATUS register.

Latch Clear (LTCLR)

When a current limit fault or watchdog timer fault occurs, the state is latched. To clear these faults, toggle (from 0, set 1 then reset to 0) LTCLR in the OUTPUT CTL register (bit 0).

Figure 1 is the LTCLR and XALERT clear example after sensing a short-circuit.

FUNCTIONAL DESCRIPTION (continued)

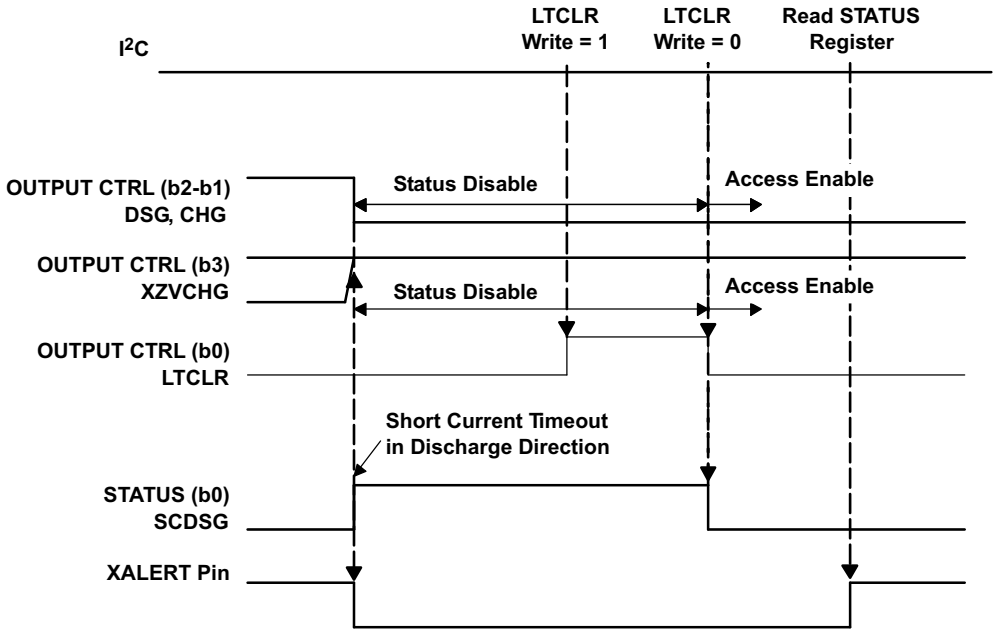


Figure 1. LTCLR and XALERT Clear Example After Sensing Short LTCLR and XALER Clear Example

FUNCTIONAL DESCRIPTION (continued)

2-, 3-, or 4-Cell Configuration

In a 3-cell configuration, VC1 is shorted to VC2. In a 2-cell configuration, VC1 and VC2 are shorted to VC3.

Watchdog Input (WDI)

The WDI input is required as a time base for delay timing when determining overload and short-circuit delay periods and is used as part of the system watchdog.

Initially, the watchdog monitors the host oscillator start up; if there is no response from the host within 700 ms of the bq29312A reaching its minimum operating voltage, then the bq29312A turns both CHG, DSG, and ZVCHG FETs OFF.

Once the watchdog has been started during this wake-up period, it monitors the host for an oscillation stop condition, which is defined as a period of 100 µs (typ), where no clock input is received. If an oscillator stop condition is identified, then the watchdog turns the CHG, DSG, and ZVCHG FETs OFF. When the host clock oscillation is started, WDF is released, but the flag is latched until LTCLR is toggled.

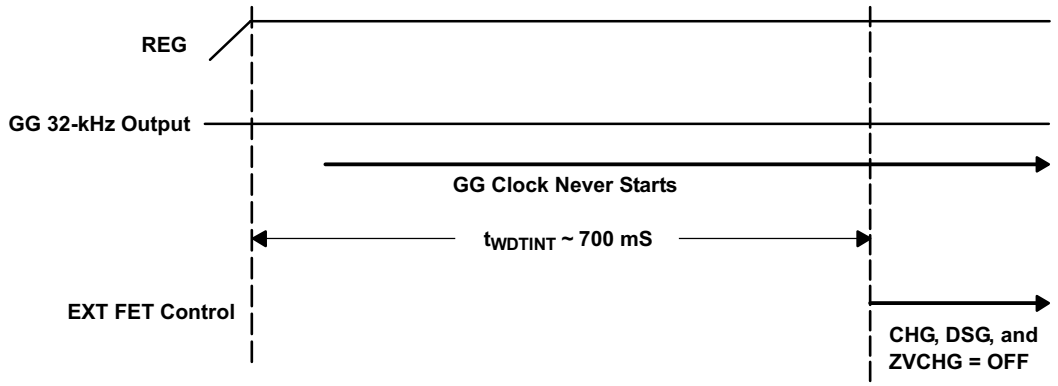


Figure 2. Watchdog Timing Chart—WDI Fault at Startup

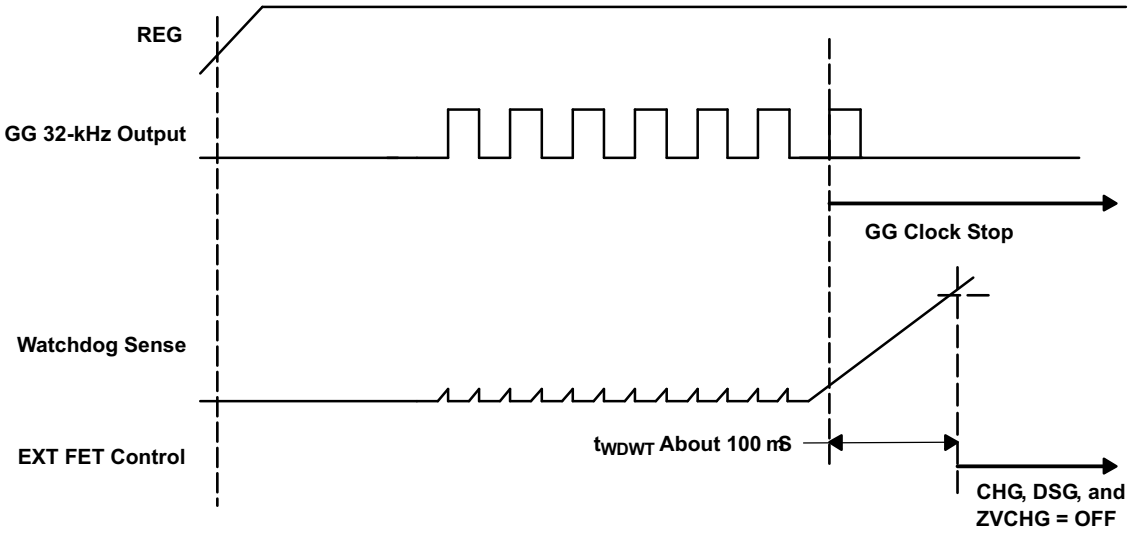


Figure 3. Watchdog Timing Chart—WDI Fault After Startup

DSG and CHG FET Driver Control

The bq29312A drives the DSG, CHG, and ZVCHG FET off if an OL or SC safety threshold is breached depending on the current direction. The host can force any FET on or off only if the bq29312A integrated protection control allows. The DSG and CHG FET drive gate-to-drain voltage is clamped to 15 V (typ).

FUNCTIONAL DESCRIPTION (continued)

The default-state of the CHG and DSG FET drive is off, when PMS = GND. A host can control the FET drive by programming OUTPUT CTL (b3...b1) where b1 is used to control the discharge FET, b2 is used to control the charge FET, and b3 is used to control the ZVCHG FET. These controls are only valid when not in the initialized state. The CHG drive FET can be powered by PACK and the DSG FET can be powered by BAT.

Precharge and 0-V Charging—Theory of Operation

The bq29312A supports both a charger that has a precharge mode and one that does not. The bq29312A also supports charging even when the battery falls to 0 V. Detail is described in the application section.

SLEEP Control Input (SLEEP)

The SLEEP input is pulled-up internally to REG. When SLEEP is pulled to REG, the bq29312A enters the SLEEP mode. The SLEEP mode disables all the FET outputs and the OL, SC, and watchdog faults are also disabled. The RAM configuration is still valid on exit of the SLEEP mode. The host can force the bq29312A into SLEEP mode via register control also.

Table 1. SLEEP Control Input

ITEM	SLEEP		EXIT SLEEP
	FUNCTION	I²C READ/WRITE	
I²C Read/Write	Active	Write is available, but read is disabled	Last pre-sleep entry configuration is valid. (If change configuration, latest write data is valid.)
REG Output	Active		
External pin control: CHG, DSG, ZVCHG, TOUT, OD OC and SC protection: SCD, SCC and OCD CELL Translation PACKOUT, VMEN Cell Balancing: CB[3:0] Watchdog: WDDIS	Disabled		

Power Modes

The bq29312A has three power modes, Normal, Sleep, and Ship. The following table outlines the operational functions during these power modes.

Table 2. Power Modes

POWER MODE	TO ENTER POWER MODE	TO EXIT POWER MODE	MODE DESCRIPTION
Normal	SLEEP = GND and STATE CTL(b0) = 0 and STATE CTL(b1) = 0		The battery is in normal operation with protection, power management, and battery monitoring functions available and operating. The supply current of this mode varies as the host can enable and disable various power management features.
Sleep	{SLEEP = REG (floating) or STATE CTL(b0) = 1 } and STATE CTL(b1) = 0	SLEEP = GND and STATE CTL(b0) = 0	All functions stop except LDO and I²C interface. On entry to this mode, all registers are masked off keeping their state. The host controller can change the RAM registers via the I²C interface, but reading data is disabled until exit of Sleep mode.
Ship	STATE CTL(b1) = 1 And supply at the PACK pin is removed	Supply voltage to PACK	The bq29312A is completely shut down as in the sleep mode. In addition, the REG output is disabled, I²C interface is powered down, and memory is not valid.

Communications

The I²C compatible serial communications provides read and write access to the bq29312A data area. The data is clocked via separate data (SDATA) and clock (SCLK) pins. The bq29312A acts as a slave device and does not generate clock pulses. Communication to the bq29312A is provided from GPIO pins or an I²C supporting port of a host system controller. The slave address for the bq29312A is 7 bits and the value is 0100 000 (0x20).

	(MSB)	I²C ADDRESS +R/W BIT					(LSB)
	(MSB)	I²C ADDRESS (0x20)				(LSB)	
Write(1)	0	1	0	0	0	0	0	0
Read								1

(1) Bit 0: 0 = write, 1= read

The bq29312A does *not* have the following functions compatible with the I²C specification.

- The bq29312A is always regarded as a slave.
- The bq29312A does not return a NACK for an invalid register address.
- The bq29312A does not support the general code of the I²C specification, and therefore does not return an ACK.
- The bq29312A does *not* support the address auto increment, which allows continuous reading and writing.
- The bq29312A allows data to be written to or read from the same location without resending the location address.

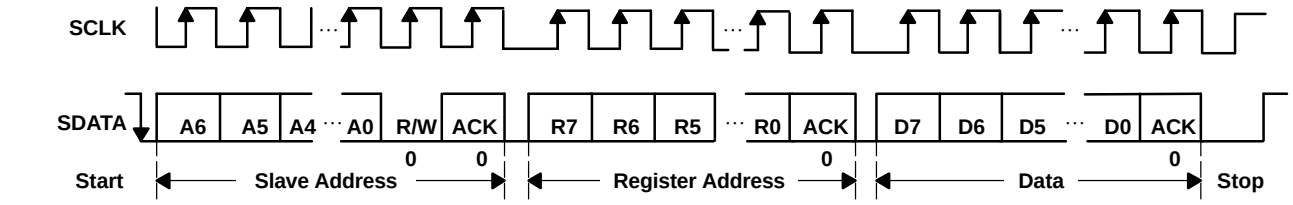


Figure 4. I²C-Bus Write to bq29312A

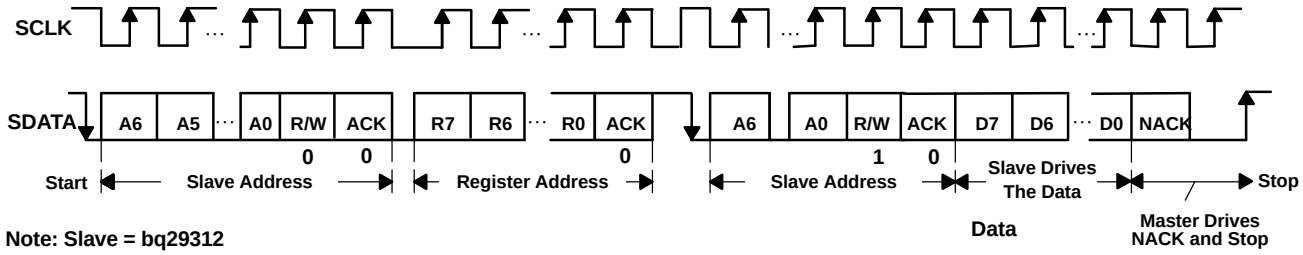


Figure 5. I²C-Bus Read from bq29312A: Protocol A

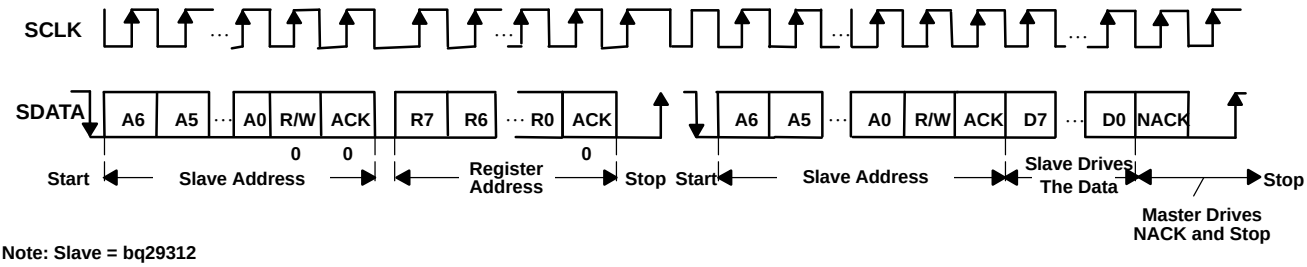


Figure 6. I²C-Bus Read from bq29312A: Protocol B

Register Map

The bq29312A has nine addressable registers. These registers provide status, control, and configuration information for the battery protection system.

Table 3. Addressable Registers

NAME	ADDR	TYPE	DESCRIPTION
STATUS	0x00	R	Status register
OUTPUT CTL	0x01	R/W	Output pin control from system host
STATE CTL	0x02	R/W	State control
FUNCTION CTL	0x03	R/W	Function control
CELL _SEL	0x04	R/W	Battery cell select for cell translation and balance bypass and select mode for calibration
OLV	0x05	R/W	Overload threshold voltage
OLT	0x06	R/W	Overload delay time
SCC	0x07	R/W	Short-circuit current threshold voltage and delay for charge
SCD	0x08	R/W	Short-circuit current threshold voltage and delay for discharge

STATUS : Status register

STATUS REGISTER (0x00)							
7	6	5	4	3	2	1	0
0	0	ZVCLMP	SLEEPDET	WDF	OL	SCCHG	SCDSG

The STATUS register provides information about the current state of the bq29312A. Reading the STATUS register clears the XALERT pin.

STATUS b0 (SCDSG): This bit indicates a short-circuit in the discharge direction.

0 = Current below the short-circuit threshold in the discharge direction (default).

1 = Current greater than or equal to the short-circuit threshold in the discharge direction.

STATUS b1 (SCCHG): This bit indicates a short-circuit in the charge direction.

0 = Current below the short-circuit threshold in the charge direction (default).

1 = Current greater than or equal to the short-circuit threshold in the charge direction.

STATUS b2 (OL): This bit indicates an overload condition.

0 = Current less than or equal to the overload threshold (default).

1 = Current greater than overload threshold.

STATUS b3 (WDF): This bit indicates a watchdog fault condition has occurred.

0 = 32-kHz oscillation is normal (default).

1 = 32-kHz oscillation stopped or not started and the watchdog has timed out.

STATUS b4 (SLEEPDET): This bit indicates the bq29312A is SLEEP mode.

0 = bq29312A is not in SLEEP mode (default).

1 = bq29312A is in SLEEP mode.

STATUS b5 (ZVCLMP): This bit indicates ZVCHG output is clamped.

0 = ZVCHG pin is not clamped (default).

1 = ZVCHG pin is clamped.

OUTPUT CTL: Output Control Register

OUTPUT CTL REGISTER (0x01)							
7	6	5	4	3	2	1	0
0	0	0	OD	XZVCHG	CHG	DSG	LTCLR

The OUTPUT CTL register controls the outputs of the bq29312A and can be used to clear certain states.

OUTPUT CTL b0 (LTCLR): When a current limit fault or watchdog timer fault is latched, this bit releases the fault latch when toggled from 0 to 1 and back to 0 (default =0).

0 = (default)

0->1 ->0 clears the fault latches

OUTPUT CTL b1 (DSG): This bit controls the external discharge FET.

0 = discharge FET is off and is controlled by the system host (default).

1 = discharge FET is on and the bq29312A is in normal operating mode.

OUTPUT CTL b2 (CHG): This bit controls the external charge FET.

PMS=GND

0 = charge FET is off and is controlled by the system host (default).

1 = charge FET is on and the bq29312A is in normal operating mode.

PMS=PACK

0 = charge FET is off and is controlled by the system host.

1 = charge FET is on and the bq29312A is in normal operating mode (default).

OUTPUT CTL b3 (XZVCHG): This bit controls the external ZVCHG FET.

0 = ZVCHG FET is on and is controlled by the system host (default).

1 = ZVCHG FET is off and the bq29312A is in normal operating mode.

OUTPUT CTL b4 (OD): This bit enables or disables the OD output.

0 = OD is high impedance (default).

1 = OD output is active (GND).

STATE CTL: State Control Register

STATE CTL REGISTER (0x02)							
7	6	5	4	3	2	1	0
0	0	0	0	0	WDDIS	SHIP	SLEEP

The STATE CTL register controls the state of the bq29312A.

STATE CTL b0 (SLEEP): This bit is used to enter the sleep power mode.

0 = bq29312A exits sleep mode (default).

1 = bq29312A enters the sleep mode.

STATE CTL b1 (SHIP): This bit is used to enter the ship power mode when pack supply voltage is not applied.

0 = bq29312A in normal mode (default).

1 = bq29312A enters ship mode when pack voltage is removed.

STATE CTL b2 (WDDIS): This bit is used to enable or disable the watchdog timer function.

0 = enable clock monitoring (default).

1 = disable clock monitoring.

NOTE:

Use caution when setting the WDDIS. For example, when the 32-kHz input fails, the overload and short-circuit delay timers no longer function because they use the same WDI input. If the WDI input clock stops, these current protections do not function. WDF should be enabled at any time for maximum safety. If the watchdog function is disabled, the CHG and DSG FETs should be turned off.

FUNCTION CTL: Function Control Register

FUNCTION CTL REGISTER (0x03)							
7	6	5	4	3	2	1	0
0	0	TOUT	XSCD	SSCC	XOL	PACKOUT	VMEN

The FUNCTION CTL register enables and disables functions of the bq29312A.

FUNCTION CTL b0 (VMEN): This bit enables or disables the cell and battery voltage monitoring function.

0 = disable voltage monitoring (default). CELL output is pulled down to GND level.

1 = enable voltage monitoring.

FUNCTION CTL b1 (PACKOUT): This bit is used to translate the PACK input to the CELL pin when VMEN=1. The pack voltage is divided by 25 and is presented on CELL regardless of the CELL_SEL register settings.

0 = disable PACK OUT (default).

1 = enable PACK OUT.

FUNCTION CTL b2 (XOL): This bit enables or disables the overcurrent sense function.

0 = enable overload sense (default).

1 = disable overload sense.

FUNCTION CTL b3 (XSCC): This bit enables or disables the short current sense function of charging.

0 = enable short-circuit current sense in charge direction (default).

1 = disable short-circuit current sense in charge direction.

FUNCTION CTL b4 (XSCD): This bit enables or disables the short current sense function of discharge.

0 = enable short-circuit current sense in discharge direction (default).

1 = disable short-circuit current sense in discharge direction.

FUNCTION CTL b5 (TOUT): This bit controls the power to the thermistor.

0 = thermistor power is off (default).

1 = thermistor power is on.

CELL SEL: Cell Select Register

CELL_SEL REGISTER (0x04)							
7	6	5	4	3	2	1	0
CB3	CB2	CB1	CB0	CAL1	CAL0	CELL1	CELL0

This register determines cell selection for voltage measurement and translation, cell balancing, and the operational mode of the cell voltage monitoring.

CELL_SEL b0–b1 (CELL0–CELL1): These two bits select the series cell for voltage measurement translation.

CELL1	CELL0	SELECTED CELL
0	0	VC4–VC5, Bottom series element (default)
0	1	VC4–VC3, Second lowest series element
1	0	VC3–VC2, Second highest series element
1	1	VC1–VC2, Top series element

CELL_SEL b2–b3 (CAL1, CAL0): These bits determine the mode of the voltage monitor block.

CAL1	CAL0	SELECTED MODE
0	0	Cell translation for selected cell (default)
0	1	Offset measurement for selected cell
1	0	Monitor the V_{REF} value for gain calibration
1	1	Monitor the V_{REF} directly value for gain calibration, bypassing the translation circuit

CELL_SEL b4–b7 (CB0–CB3): These 4 bits select the series cell for cell balance bypass path.

CELL SEL b4 (CB0): This bit enables or disables the bottom series cell balance charge bypass path.

0 = disable bottom series cell balance charge bypass path (default).

1 = enable bottom series cell balance charge bypass path.

CELL SEL b5 (CB1): This bit enables or disables the second lowest series cell balance charge bypass path.

0 = disable series cell balance charge bypass path (default).

1 = enable series cell balance charge bypass path.

CELL SEL b6 (CB2): This bit enables or disables the second highest cell balance charge bypass path.

0 = disable series cell balance charge bypass path (default).

1 = enable series cell balance charge bypass path.

CELL SEL b7 (CB3): This bit enables or disables the highest series cell balance charge bypass path.

0 = disable series cell balance charge bypass path (default).

1 = enable series cell balance charge bypass path.

OLV: Overload Voltage Threshold Register

OLV REGISTER (0x05)							
7	6	5	4	3	2	1	0
0	0	0	OLV4	OLV3	OLV2	OLV1	OLV0

OLV (b4–b0): These five bits select the value of the overload threshold with a default of 00000.

OLV (b4–b0) configuration bits with corresponding voltage threshold

00000	**0.050 V**	**01000**	**0.090 V**	**10000**	**0.130 V**	**11000**	**0.170 V**
00001	0.055 V	01001	0.095 V	10001	0.135 V	11001	0.175 V
00010	0.060 V	01010	0.100 V	10010	0.140 V	11010	0.180 V
00011	0.065 V	01011	0.105 V	10011	0.145 V	11011	0.185 V
00100	0.070 V	01100	0.110 V	10100	0.150 V	11100	0.190 V
00101	0.075 V	01101	0.115 V	10101	0.155 V	11101	0.195 V
00110	0.080 V	01110	0.120 V	10110	0.160 V	11110	0.200 V
00111	0.085 V	01111	0.125 V	10111	0.165 V	11111	0.205 V

OLT: Overload Blanking Delay Time Register

OLT REGISTER (0x06)							
7	6	5	4	3	2	1	0
0	0	0	0	OLT3	OLT2	OLT1	OLT0

OLT(b3–b0): These four bits select the value of the delay time for overload with a default of 0000.

OLT(b3–b0) configuration bits with corresponding delay time

0000	**1 ms**	**0100**	**9 ms**	**1000**	**17 ms**	**1100**	**25 ms**
0001	3 ms	0101	11 ms	1001	19 ms	1101	27 ms
0010	5 ms	0110	13 ms	1010	21 ms	1110	29 ms
0011	7 ms	0111	15 ms	1011	23 ms	1111	31 ms

SCC: Short Circuit in Charge Configuration Register

SCC REGISTER (0x07)							
7	6	5	4	3	2	1	0
SCCT3	SCCT2	SCCT1	SCCT0	SCCV3	SCCV2	SCCV1	SCCV0

This register selects the short-circuit threshold voltage and delay for charge.

SCC(b3–b0) : These bits select the value of the short-circuit voltage threshold with 0000 as the default.

SCC(b3–b0) with corresponding SC threshold voltage

0000	**0.100 V**	**0100**	**0.200 V**	**1000**	**0.300 V**	**1100**	**0.400 V**
0001	0.125 V	0101	0.225 V	1001	0.325 V	1101	0.425 V
0010	0.150 V	0110	0.250 V	1010	0.350 V	1110	0.450 V
0011	0.175 V	0111	0.275 V	1011	0.375 V	1111	0.475 V

SCC(b7–b4): These bits select the value of the short-circuit delay time. Exceeding the short-circuit voltage threshold for longer than this period turns off the corresponding CHG, DSG, and ZVCHG output. 0000 is the default.

SCC(b7–b4) with corresponding SC delay time

0000	**0 µs**	**0100**	**244 µs**	**1000**	**488 µs**	**1100**	**732 µs**
0001	61 µs	0101	305 µs	1001	549 µs	1101	793 µs
0010	122 µs	0110	366 µs	1010	610 µs	1110	854 µs
0011	183 µs	0111	427 µs	1011	671 µs	1111	915 µs

SCD: Short Circuit in Discharge Configuration Register

SCD REGISTER (0x08)							
7	6	5	4	3	2	1	0
SCDT3	SCDT2	SCDT1	SCDT0	SCDV3	SCDV2	SCDV1	SCDV0

This register selects the short-circuit threshold voltage and delay for discharge.

SCD(b3–b0) with corresponding SC threshold voltage with 0000 as the default.

SCD(b3–b0): These bits select the value of the short-circuit voltage threshold

0000	**0.10 V**	**0100**	**0.20 V**	**1000**	**0.30 V**	**1100**	**0.40 V**
0001	0.125 V	0101	0.225 V	1001	0.325 V	1101	0.425 V
0010	0.150 V	0110	0.250 V	1010	0.350 V	1110	0.450 V
0011	0.175 V	0111	0.275 V	1011	0.375 V	1111	0.475 V

SCD(b7–b4): These bits select the value of the short-circuit delay time. Exceeding the short-circuit voltage threshold for longer than this period turns off the corresponding CHG, DSG, and ZVCHG output as has 0000 as the default.

SCD(b7-b4) with corresponding SC delay time

0000	**0 µs**	**0100**	**244 µs**	**1000**	**488 µs**	**1100**	**732 µs**
0001	61 µs	0101	305 µs	1001	549 µs	1101	793 µs
0010	122 µs	0110	366 µs	1010	610 µs	1110	854 µs
0011	183 µs	0111	427 µs	1011	671 µs	1111	915 µs

APPLICATION INFORMATION

Precharge and 0-V Charging—Theory of Operation

In order to charge, the charge FET (CHG-FET) must be turned on to create a current path. When the $V_{(BAT)}$ is 0 V and CHG-FET = ON, the $V_{(PACK)}$ is as low as the battery voltage. In this case, the supply voltage for the device is too low to operate. There are three possible configurations for this function and the bq29312A can be easily configured according to the application needs. The three modes are 0-V Charge FET Mode, Common FET Mode, and Precharge FET Mode.

1. 0-V Charge FET Mode – Dedicates a precharge current path using an additional FET (ZVCHG-FET) to sustain the PACK+ voltage level. The host charger is expected to provide a precharge function.
2. Common FET Mode – Does not use a dedicated precharge FET. The charge FET (CHG-FET) is assured to be set to ON state as default. The charger is expected to provide a precharge function.
3. Precharge FET Mode – Dedicates a precharge current path using an additional open-drain (OD) pin drive FET (PCHG-FET) FET to sustain the PACK+ voltage level. The charger does not provide any precharge function.

0-V Charge FET Mode

In this mode, a dedicated precharge current path using an additional FET (ZVCHG-FET) is required to sustain a suitable PACK+ voltage level. The charger is expected to provide the precharge function in this mode where the precharge current level is suitable to charge cells below a set level, typically below 3 V per cell. When the lowest cell voltage rises above this level, then a fast charging current is applied by the charger.

The circuit diagram for this method is shown in Figure 7, showing how the additional FET is added in parallel with the charge FET (CHG-FET).

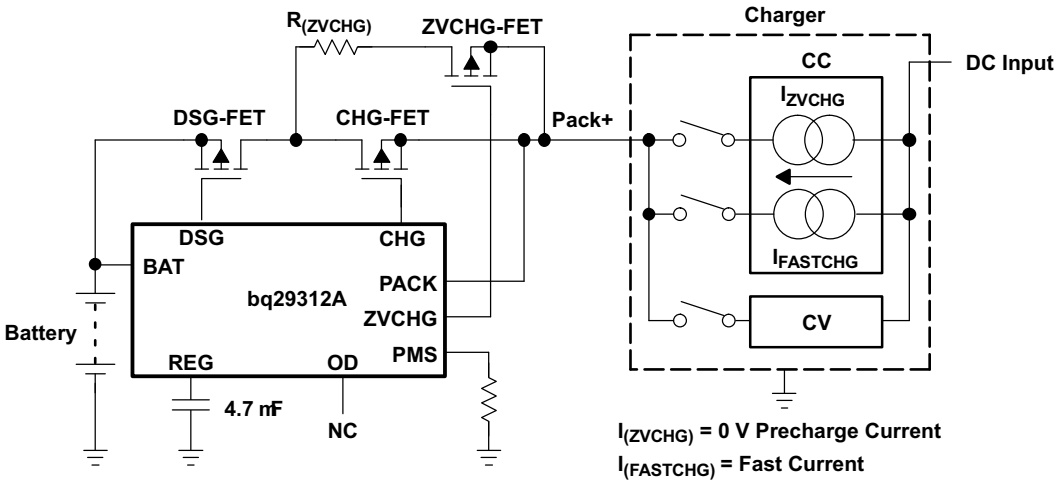


Figure 7. 0-V Charge FET Mode Circuit

APPLICATION INFORMATION (continued)

In order to pass 0 V or precharge current, an appropriate gate-source voltage $V_{(GS)}$, for ZVCHG-FET must be applied. Here, $V_{(PACK)}$ can be expressed in terms of $V_{(GS)}$ as follows:

$V_{(PACK)} = V_{(ZVCHG)} + V_{(GS)}$ (ZVCHG-FET gate - source voltage)

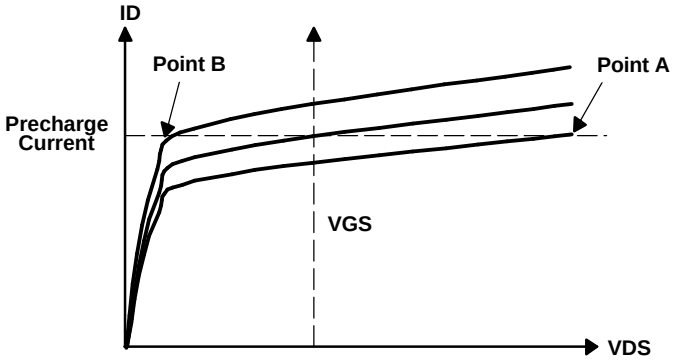


Figure 8. Drain Current vs Drain-Source Voltage Characteristics

In the bq29312A, the initial state is for CHG-FET = OFF and ZVCHG-FET = ON with the $V_{(ZVCHG)}$ clamped at 3.5 V initially. Then, the charger applies a constant current and raises $V_{(PACK)}$ high enough to pass the precharge current, point A. For example, if the $V_{(GS)}$ is 2 V at this point, $V_{(PACK)}$ is 3.5 V + 2 V = 5.5 V. Also, the ZVCHG-FET is used in its MOS saturation region at this point so that $V_{(DS)}$ is expressed as follows:

$V_{(PACK)} = V_{(BAT)} + V_F + V_{DS(ZVCHG\text{-}FET)}$

where $V_{(F)}$ = 0.7 V is the forward voltage of a DSG-FET back diode and is typically 0.7 V.

This derives the following equation:

$V_{DS} = 4.8\ V - V_{(BAT)}$

As the battery is charged $V_{(BAT)}$ increases and the $V_{(DS)}$ voltage decreases reaching its linear region. For example: If the linear region is 0.2 V, this state continues until $V_{(BAT)}$ = 4.6 V, (4.8 V - 0.2 V).

As $V_{(BAT)}$ increases further, $V_{(PACK)}$ and the $V_{(GS)}$ voltage increase. But the V_{DS} remains at 0.2 V because the ZVCHG-FET is driven in its MOS linear region, point B.

$V_{(PACK)} = V_F + 0.2\ V + V_{(BAT)}$

where V_F = 0.7 V is the forward voltage of a DSG-FET back diode and is typically 0.7 V

The $R_{(ZVCHG)}$ purpose is to split heat dissipation across the ZVCHG-FET and the resistor.

ZVCHG pin behavior is shown in Figure 9 where $V_{(ZVCHG)}$ is set to 0 V at the beginning.

APPLICATION INFORMATION (continued)

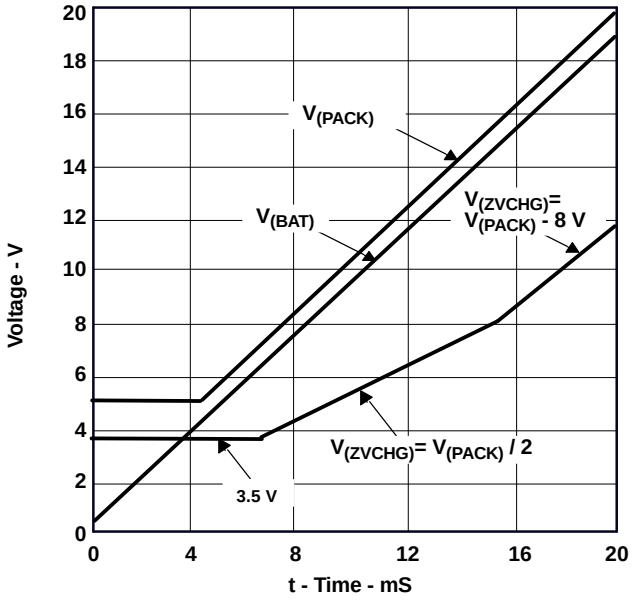


Figure 9. Voltage Transition at ZVCHG, PACK, and BAT

As $V_{(PACK)}$ exceeds 7 V, $V_{(ZVCHG)} = V_{(PACK)}/2$. However, $V_{(ZVCHG)}$ is maintained to limit the voltage between PACK and ZVCHG at a maximum of 8 V(typ). This limitation is intended to avoid excessive voltage between the gate and the source of ZVCHG-FET.

The signal timing is shown in Figure 10. When precharge begins, ($V_{(BAT)}$ = 0 V) $V_{(PACK)}$ is clamped to 3.5 V and holds the supply voltage for bq29312A operation. After $V_{(BAT)}$ reaches sufficient voltage high enough for bq29312A operation, the CHG-FET and the DSG-FET are turned ON and ZVCHG-FET is turned OFF.

Although the current path is changed, the same precharging current is still applied. When $V_{(BAT)}$ reaches the fast charging voltage (typical 3 V per cell), the charger switches into fast charging mode.

APPLICATION INFORMATION (continued)

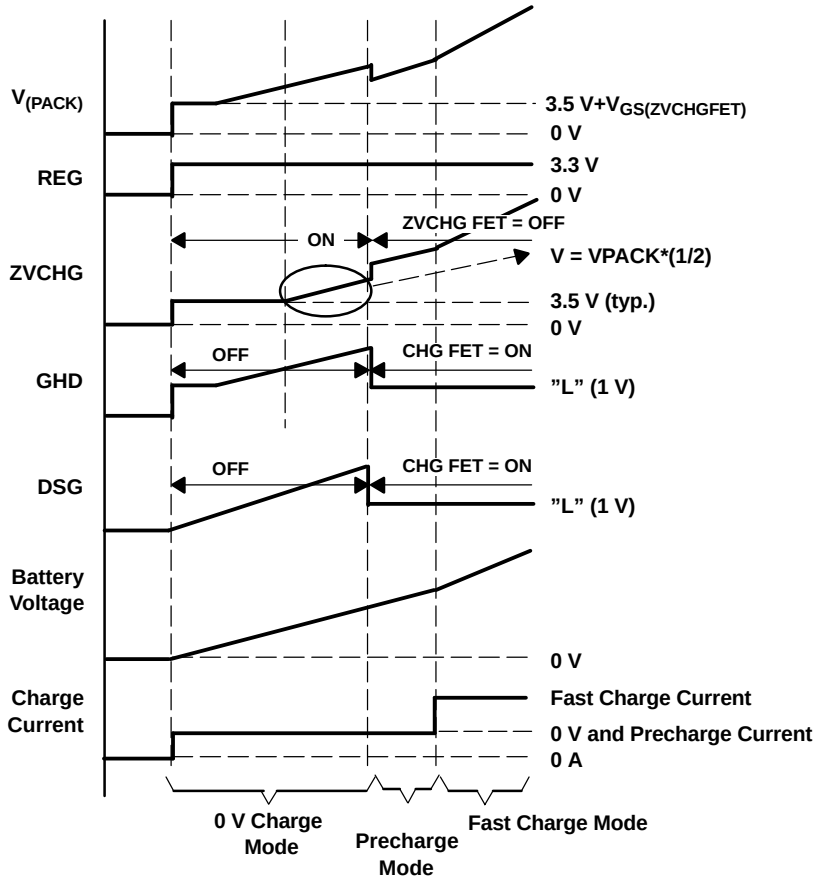


Figure 10. Signal Timing of Pins During 0-V Charging and Precharging (0-V Charge FET)

Common FET

This mode does not require a dedicated precharge FET (ZVCHG-FET). The charge FET (CHG-FET) is ON at initialization of the bq29312A when PMS = $V_{(PACK)}$, allowing for 0 V or precharge current to flow. The application circuit is shown in Figure 11. The charger is expected to provide the precharge function in this mode, where the charger provides a precharge current level suitable to charge cells below a set level, typically below 3 V per cell. When the lowest cell voltage rises above this level, then a fast charging current is applied.

When the charger is connected, the voltage at PMS rises. Once it is above 0.7 V, the CHG output is driven to GND which turns ON the CHG-FET. The charging current flows through the CHG-FET and a back diode of DSG-FET. The pack voltage is represented by the following equation.

$$V_{(PACK)} = V_{(BAT)} + V_F + V_{DS(CHG\text{-}FET)}$$

Where V_F = 0.7 V is the forward voltage of a DSG-FET back diode and is typically 0.7 V.

While $V_{(PACK)}$ is maintained above 0.7 V, the precharging current is maintained. While $V_{(PACK)}$ and $V_{(BAT)}$ are under the bq29312A supply voltage, then the bq29312A regulator is inactive and the host controller is not functional. Thus, any protection features of this chipset do not function during this period. This state continues until $V_{(PACK)}$ goes higher than the bq29312A minimum supply voltage.

When $V_{(BAT)}$ rises and $V_{(PACK)}$ reaches bq29312A minimum supply voltage, the REG output is active providing a 3.3-V (typ) supply to the host. When this level is reached, the CHG pin changes its state from GND to the level controlled with CHG bit in bq29312A registers. In this state, the CHG output level is driven by a clamp circuit so that its voltage level changes from 0 V to 1 V. Also, the host controller is active and can turn ON the DSG-FET.

APPLICATION INFORMATION (continued)

The disadvantages is that during 0-V charging, bq29312A is inactive. The device does not protect the battery and does not update battery information (now is 0 V charging) to the PC.

There are two advantage of this configuration:

1. The voltage between BAT and PACK is lower. Higher precharge current is allowed due to less heat loss in the FET, and no external resistor is required.
2. The charge FET is turned on during precharging. The precharge current can be fully controlled by the charger.

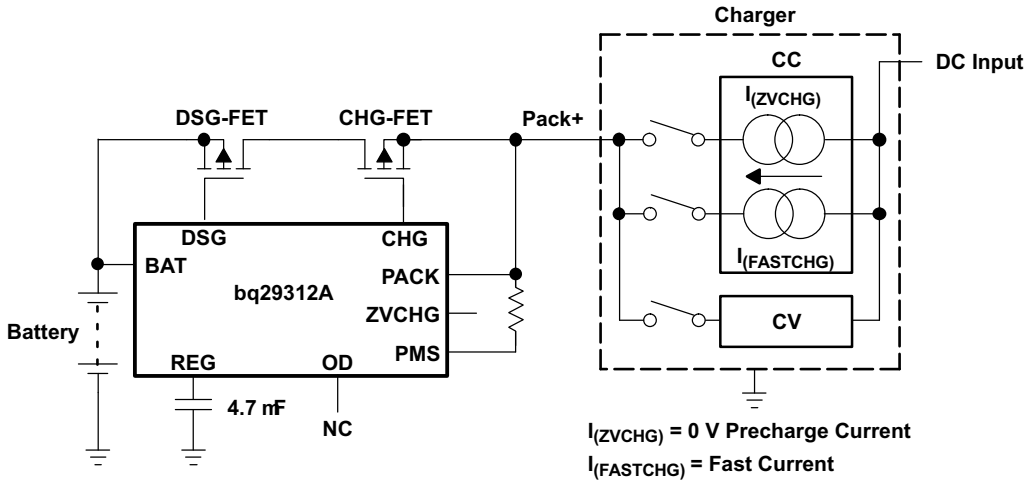


Figure 11. Common FET Mode Circuit Diagram

The signal timing during the common FET mode is shown in Figure 12. The CHG-FET is turned on when the charger is connected. As $V_{(BAT)}$ rises and $V_{(PACK)}$ reaches the bq29312A minimum supply voltage, the REG output becomes active and the host controller starts to work.

When $V_{(PACK)}$ becomes high enough, the host controller turns ON the DSG-FET. The charger enters the fast charging mode when $V_{(BAT)}$ reaches the fast charge level.

APPLICATION INFORMATION (continued)

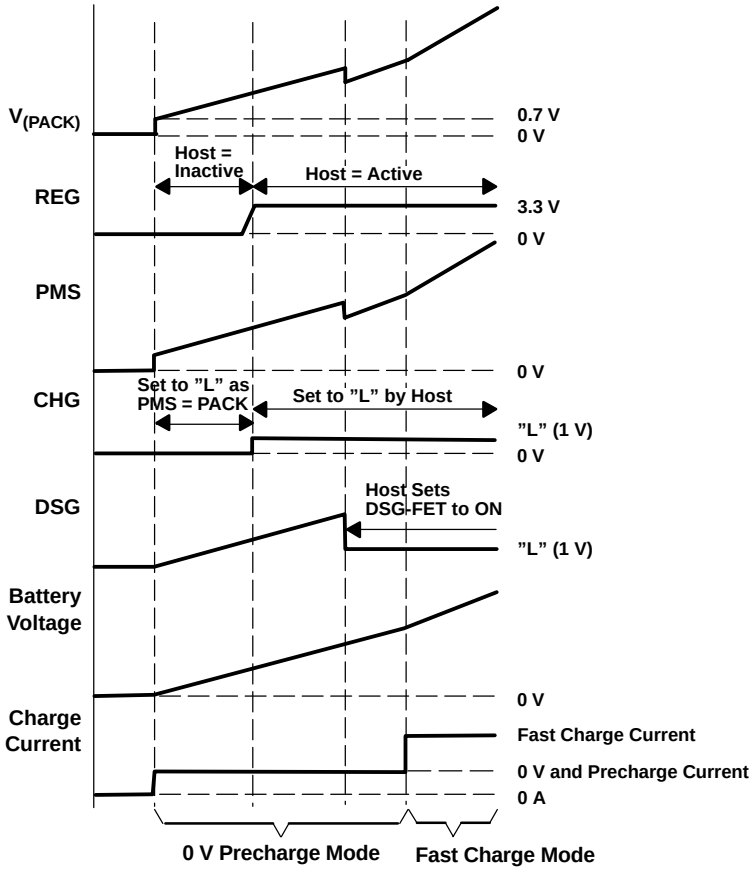


Figure 12. Signal Timing of Pins During 0-V Charging and Precharging (Common FET)

Precharge FET

This mode has a dedicated precharge current path using an additional open drain driven FET (PCHG-FET) and sustains the $V_{(PACK)}$ level. In this mode, where the PMS input is connected to GND, the bq29312A and host combine to provide the precharge function by limiting the fast charge current which is provided by the system side charger.

Figure 13 shows the bq29312A application circuit in this mode.

APPLICATION INFORMATION (continued)

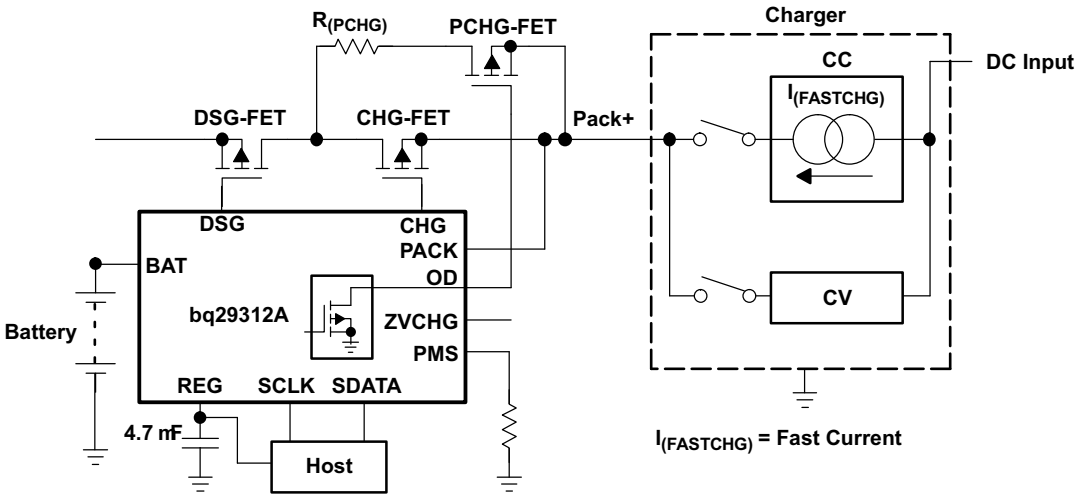


Figure 13. Precharge FET Mode Circuit Diagram

The PCHG-FET is driven by the OD output, and the resister $R_{(PCHG)}$ in the precharge path limits the precharge current. When OD = GND, then the PCHG-FET is ON. The precharge current is represented by the following equation:

$I_{(PCHG)} = ID = (V_{(PACK)} - V_{(BAT)} - V_{DS})/R_{(PCHG)}$

- A load curve of the PCHG-FET is shown in Figure 14. When the drain-source voltage (V_{DS}) is high enough, the PCHG-FET operates in the linear region and has low resistance. By approximating V_{DS} as 0 V, the precharge current, $I_{(PCHG)}$ is expressed as below.
- $I_{(PCHG)} = (V_{(PACK)} - V_{(BAT)})/R_{(PCHG)}$

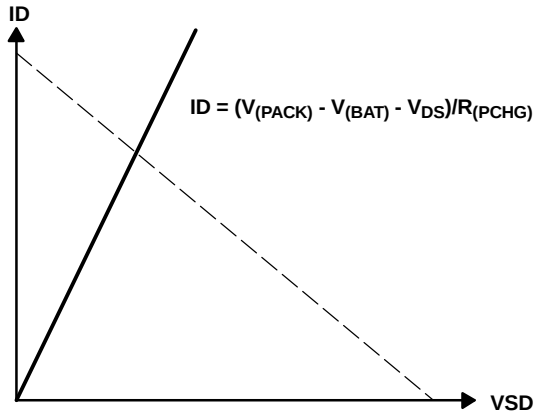


Figure 14. PCHG-FET ID—VDS Characteristic

During the precharge phase, CHG-FET is turned OFF and PCHG-FET is turned ON. When all the cell voltages measured by the host reach the fast charge threshold, the host controller turns ON CHG-FET and turns OFF PCHG-FET. The signal timing is shown in Figure 15.

When the charger is connected, CHG-FET, DSG-FET and PCHG-FET are already in the OFF state. When the charger in connected, it applies $V_{(PACK)}$. The bq29312A REG output then becomes active and supplies power to the host controller. As the host controller starts up, it turns on the OD pin and the precharge current is enabled.

APPLICATION INFORMATION (continued)

In this configuration, attention must be paid to high power consumption in the PCHG-FET and the series resistor $R_{(PCHG)}$. The highest power is consumed when V_{BAT} = 0 V, where it is the highest differential between the PACK and BAT pins. For example, the power consumption in 4-series cells with 17.4 V fast charge voltage and $R_{(PCHG)}$ = 188 Ω is expressed below.

- I_{PCHG} = (17.4 V – 0.0 V)/188 Ω = 92.6 mA
- 17.4 V × 92.6 mA = 1.61 W

An optional solution is to combine a thermistor with a resistor to create $R_{(PCHG)}$; therefore, as temperature increases, the current reduces.

Once the lowest cell voltage reaches the fast charge level (typ 3.0 V per cell), the host controller turns ON CHG-FET and DSG-FET, and turns OFF PCHG-FET.

It is also appropriate to turn on DSG-FET during precharge in order to supply precharge current efficiently, as shown in Figure 15.

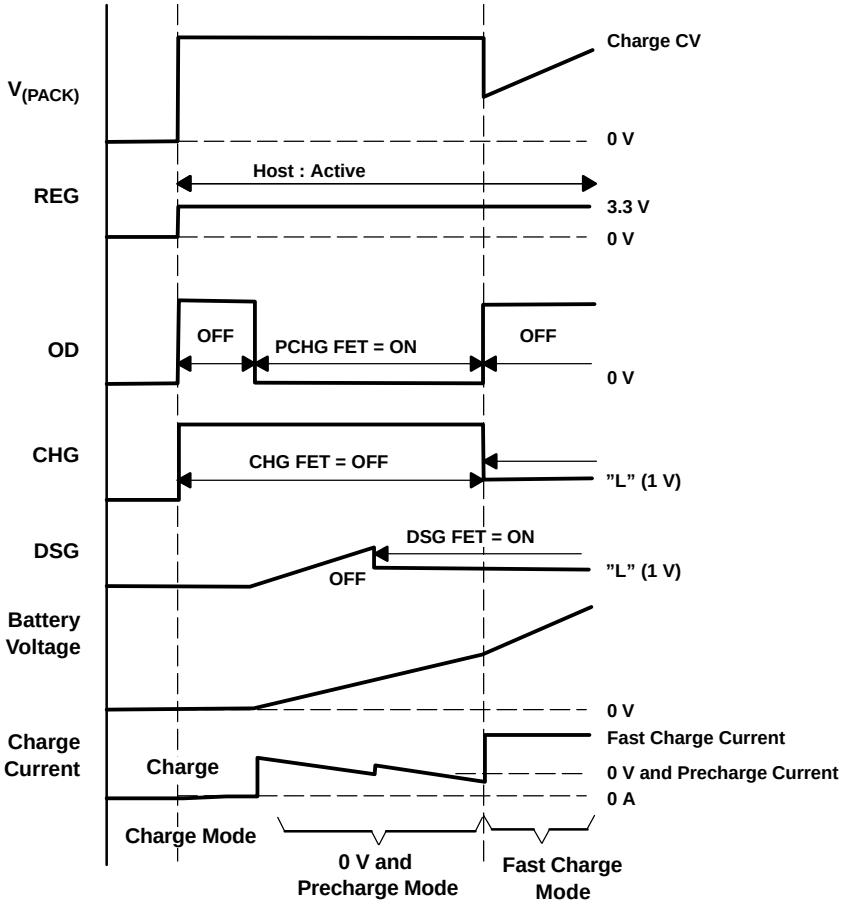


Figure 15. Signal Timing of Pins During 0-V Charging and Precharging (Precharge FET)

APPLICATION INFORMATION (continued)

Summary

The three types of 0-V charge options available with the bq29312A are summarized in Table 4.

Table 4. Charge Options

CHARGE MODE TYPE	HOST CHARGE CAPABILITIES	KEY APPLICATION CIRCUIT NOTES
1) 0-V Charge FET	Fast charge and precharge	PMS = GND ZVCHG: Drives 0-V charge FET (ZVCHG-FET) OD: Not used
2) Common FET	Fast charge and precharge	PMS = PACK ZVCHG: Not used OD: Not used
3) Precharge FET	Fast charge but no precharge function	PMS = GND ZVCHG: Not used OD: Drives the precharge FET (PCHG-FET)

There a number of tradeoffs between the various 0-V charge modes which are discussed as follows:

- **0-V Charge FET (1) vs Common FET (2)**

When the charger has both precharge and charging functions, two types of circuit configuration are available.

1. 0-V Charge FET – The bq29312A is active even during precharge. Therefore, the host can update the battery status to the system and protect the battery pack by detecting abnormal conditions.
   - A high voltage is applied on the 0-V charge FET at 0-V cell voltage. In order to avoid excessive heat generation, the 0-V charge current must be limited.
2. Common FET – During 0-V charge the bq29312A and the host are not active. Therefore, they cannot protect the cells and cannot update the battery status to the system.
   - The bq29312A can tolerate high 0-V charge current as heat generation is not excessive.
   - A dedicated FET for the 0-V charge is not required.

- **0-V Charge FET (1) vs Precharge FET (3)**

The current paths of the 0-V charge FET (1) and Precharge FET (3) modes are the same. If the 0-V charge FET (1) mode is used with chargers without precharge function, the bq29312A consumes extra current of up to 1 mA in order to turn ON the ZVCHG output.

1. If the charger has a precharge function, ZVCHG-FET is turned ON only during 0-V charging. In this case, a 1-mA increase is not a concern because the charger is connected during the 0-V charging period.
2. If the charger does not have precharge function, the ZVCHG-FET must be turned ON during 0-V charging and also precharging. When the battery reaches an overdischarged state, it must turn OFF DSG-FET and CHG-FET and turn ON ZVCHG-FET. The reason for this is the battery must keep the 0-V charge path while waiting for a charger to be connected to limit the current.
   - Consuming 1 mA, while waiting for a charger to be connected in overdischarge state, is significant if compared to current consumption of other modes.

- **Precharge FET (3)**

If the precharge FET (3) mode is used with a charger with precharge function, care must be taken as limiting the 0-V charge current with resistance may cause some issues. The charger may start fast charge immediately, or detect an abnormal condition.

When the charger is connected, the charger may raise the output voltage to force the precharge current. In order to ensure a supply voltage for the bq29312A during 0-V charging, the resistance of a series resister (R_{PCHG}) must be high enough. This may result in a high V_{PACK}, and some chargers may detect it as an abnormal condition.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ29312APW	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	29312APW
BQ29312APW.A	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	29312APW
BQ29312APWR	NRND	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	29312APW
BQ29312APWR.A	NRND	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	29312APW
BQ29312APWRG4	NRND	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	29312APW
BQ29312ARTHR	Active	Production	VQFN (RTH) | 24	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	29312 A
BQ29312ARTHR.A	Active	Production	VQFN (RTH) | 24	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	29312 A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

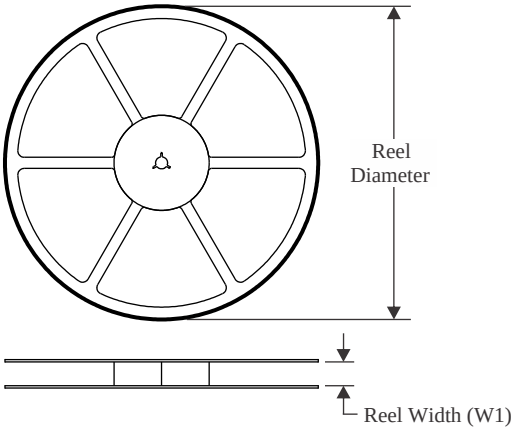
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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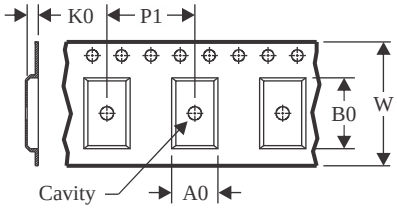
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

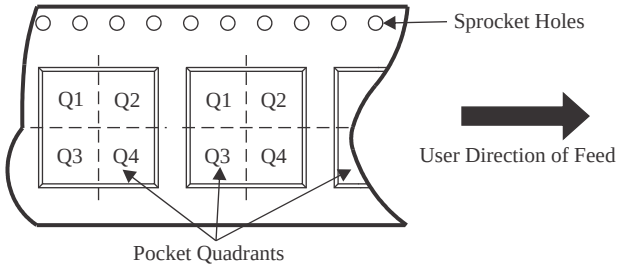


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

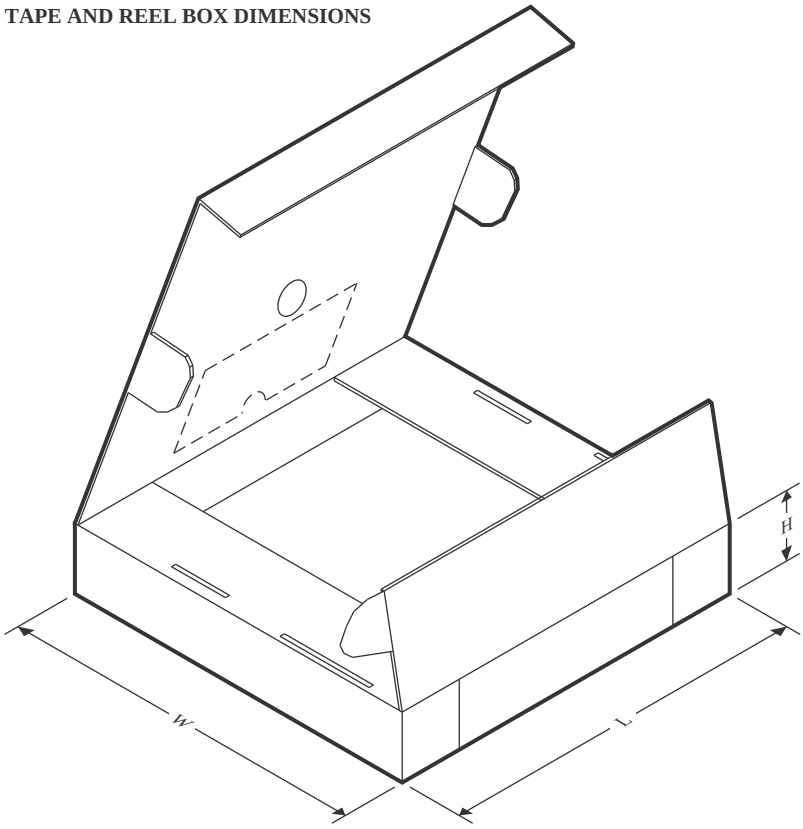
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ29312APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

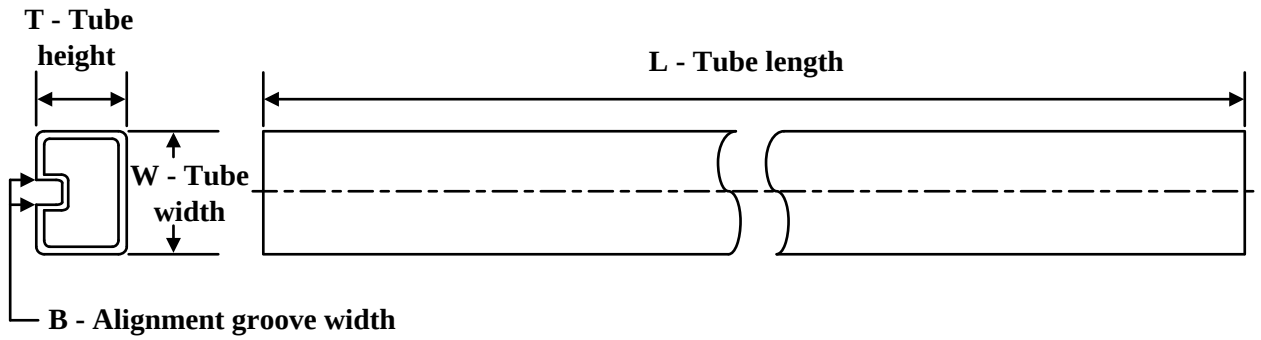
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ29312APWR	TSSOP	PW	24	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

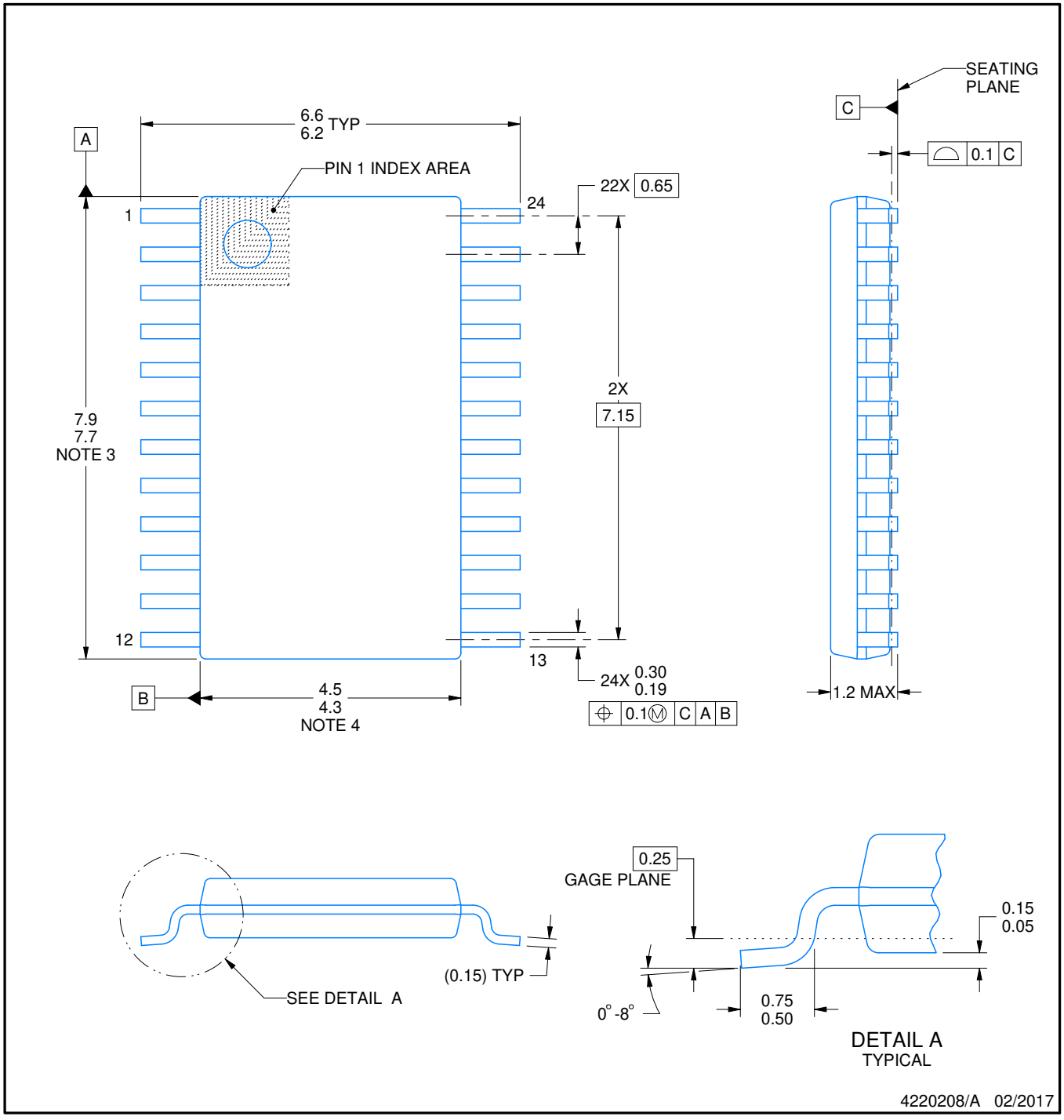
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
BQ29312APW	PW	TSSOP	24	60	530	10.2	3600	3.5
BQ29312APW.A	PW	TSSOP	24	60	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0024A

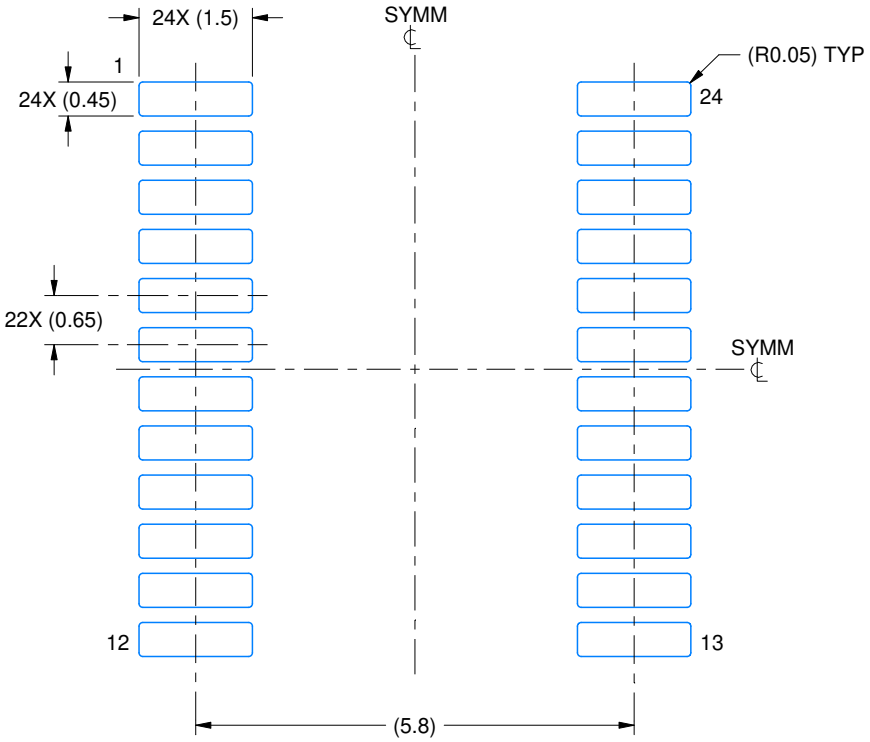
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

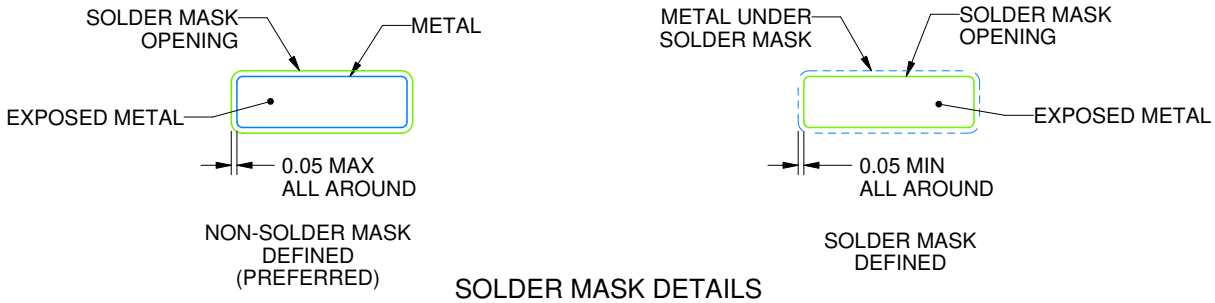


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

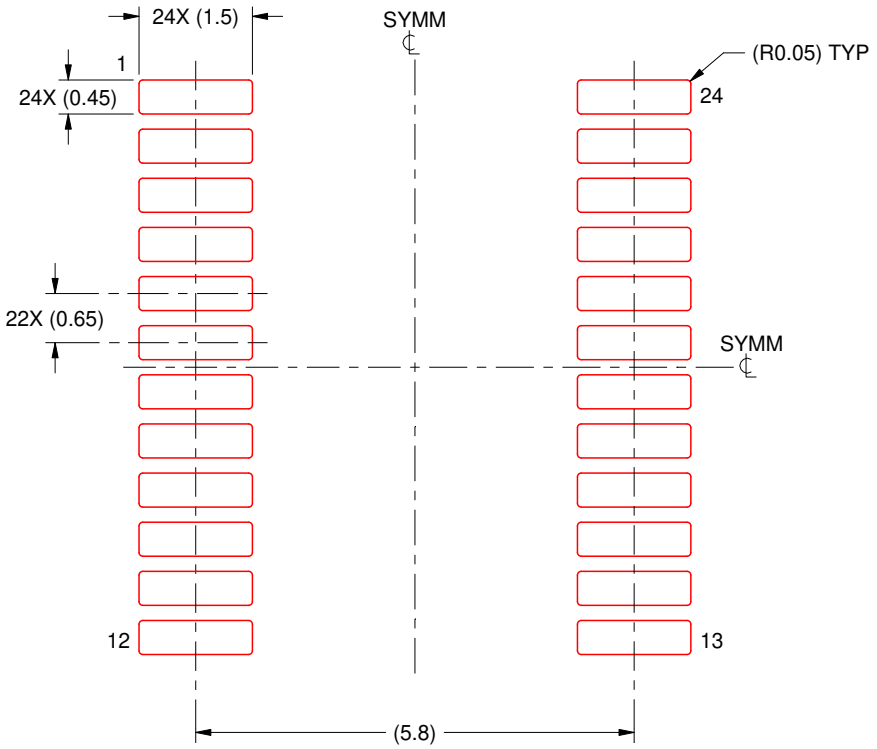


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



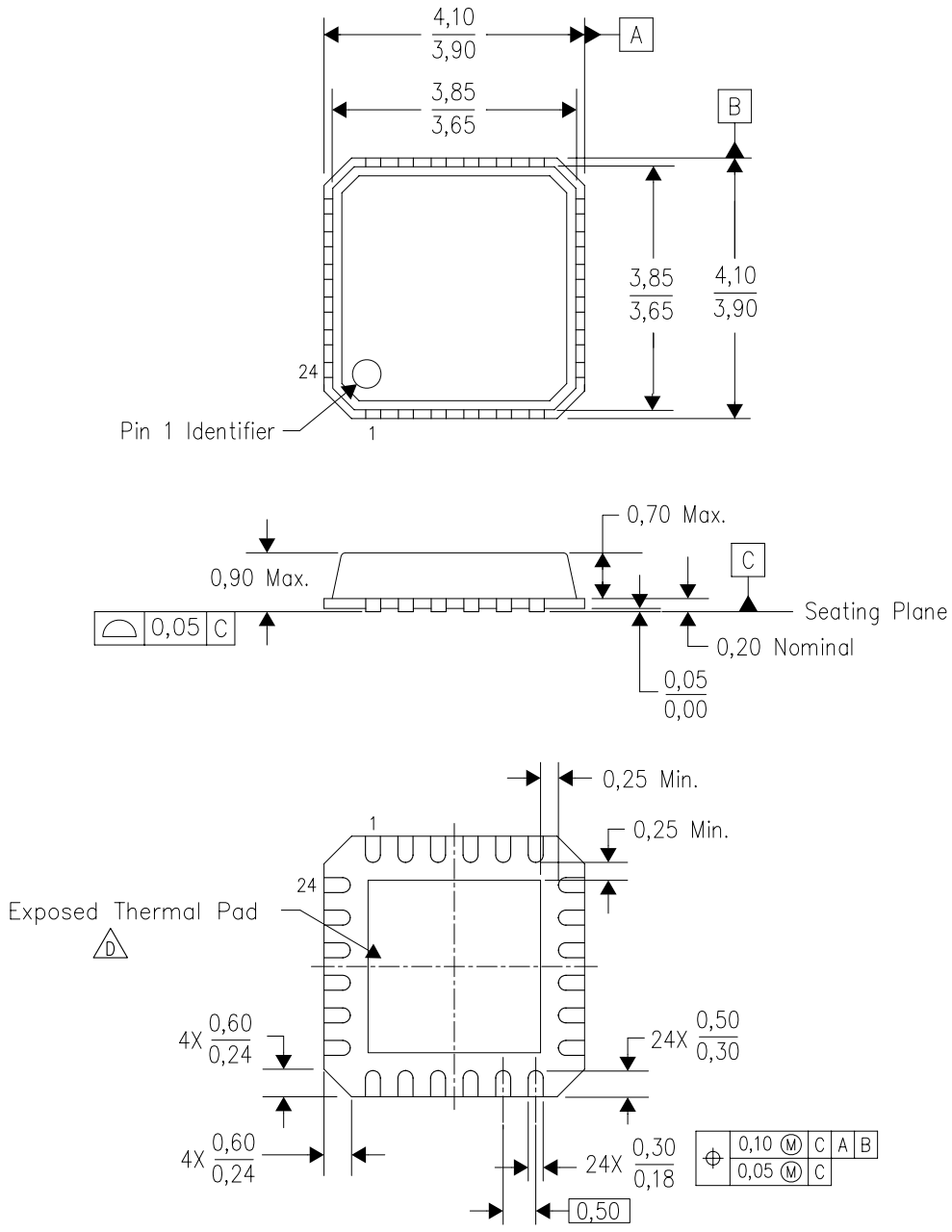
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RTH (S–PVQFN–N24) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

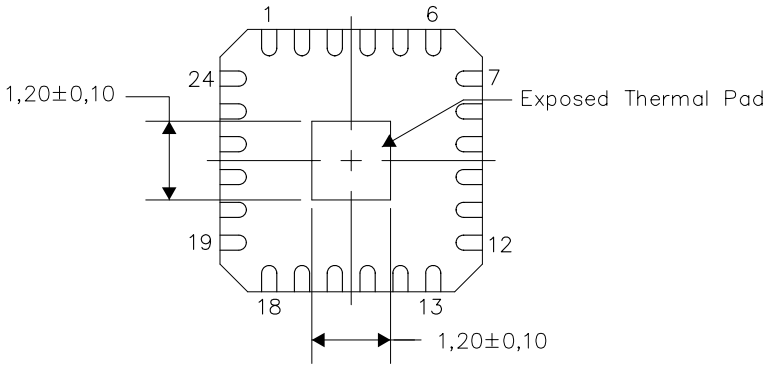
RTH (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206566–3/F 02/11

NOTE: A. All linear dimensions are in millimeters

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